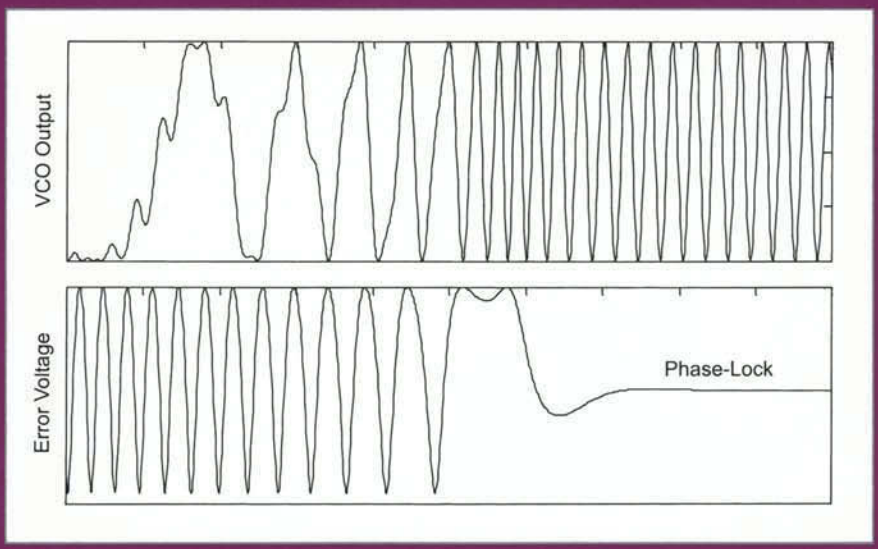
# PHASE-LOCKED LOOPS FOR WIRELESS COMMUNICATIONS

## Digital, Analog and Optical Implementations, Second Edition




DONALD R. STEPHENS

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*Digital, Analog and Optical Implementations*

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## *Digital, Analog and Optical Implementations*

## Second Edition

*by*

**Donald R. Stephens**

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This book could not have been completed without the loving support of my family. Many thanks to Tracy, Andrew, and John

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# Preface to the Second Edition

This book is intended for the graduate or advanced undergraduate engineer. The primary motivation for developing the text was to present a complete tutorial of phase-locked loops with a consistent notation. I believe this is critical for the practicing engineer who uses the text as a self-study guide.

Three years after the first printing, I discovered there was a need for a second edition. I had taught several short courses from the text, and discovered that today's engineers needed less time devoted to discrete-time theory, but wanted more practical information on implementing phase-locked loops. As a result, I have deleted discussions on topics such as multi-rate sampling and the Jury test, and replaced them with new content. Included in the new material are additional loop filters and reduction of reference feed-through in frequency synthesizers. Indeed, frequency synthesis is itself a new topic in the text.

Since most hardware phase-locked loops utilize charge pumps, I developed a new chapter that spotlights charge pumps and its complementary sequential phase detector. Several students in the short courses were asking for design examples on delay-locked loops used to synchronize circuits on CPUs and ASICS. The second printing includes new material for this very purpose.

Another change was the increased use of MATLAB™. Many of the original graphics have been replaced with graphics generated by MATLAB's

SIMULINK™ or Control System Toolbox. Since MATLAB has emerged as the leading simulation tool for the communications engineer, the graphics should be familiar and provide more information such as gain and phase margins. I have also taken the opportunity to correct typographical errors and further improve the consistency in notation.

New material has been added on digital dividers. These devices can easily dominate a frequency synthesizer's noise floor, but the literature has not provided many solutions. In this second edition, I added sections discussing the origin of phase noise in digital dividers and possible solutions. Also included are some techniques to analytically estimate the phase noise of a divider before it is even fabricated.

In the past year, many students in the short courses have been asking for design help on optical phase-locked loops. A new chapter has been added on this topic. Because many designers will be new to optical communications, I have included short sections discussing components such as lasers and photodetectors. Since coherent phase-locked loops are so very difficult to implement, I have included a section on automatic frequency control to provide frequency-locking of the lasers instead of phase-locking.

This second edition begins with the early history of phase-locked loops. I believe that historical knowledge can provide insight to the development and progress of a field, and phase-locked loops are no exception. Although all-analog phase-locked loops are becoming atypical, the continuous-time nature of analog loops allows an easy introduction to phase-locked loop theory. This foundation then allows us to proceed to the many implementations and discussions of phase-locked loops.

I wish to thank the readers of the first edition for their many suggestions and comments. Likewise the short course students have also strengthened this new edition with their participation and comments. I have tried to incorporate these suggestions within the intended scope of the text.

Donald R. Stephens

October 2001

# 1 The Early History of Phase-Locked Loops

## 1.1 History

A browse through the phase-locked loop literature of the past is humbling. Although we often consider phase-locked loops as relatively new structures, historical literature dates the concept as early as 1919 [2]. Vincent [2] and Appleton [3] experimented and analyzed, respectively, the practical synchronization of oscillators.

After these initial papers, research and development continued up until the 1940s. At that time, the initial interest in synchronization was for a) a local oscillator in FM demodulation and b) the exciter for an atomic particle accelerator amplifier [4].

The control theory for phase-locked loops was based on the well-developed theory for feedback amplifiers. Early pioneers in the feedback analysis included the Bell Labs researchers Bode [5] and Nyquist [6]. Their techniques for analyzing the stability of feedback structures are still used by researchers today.

In 1935, Travis published "Automatic Frequency Control", [7] which suggested two reasons for controlling the local oscillator of a receiver. "Oscillator drift, if not corrected by more or less frequency manual readjustment, is capable of mistuning the signal by many channels in the course of a few hours run" [7]. His second reason for oscillator control is more entertaining, "It seems to be quite true that the average listener does not tune his set well enough to obtain the best quality it is capable of giving,

partly from negligence, and partly from lack of the necessary skill, in which case the mechanical design of the set is a possible contributing factor." [7]

Travis' design was completely electronic. He did not want to increase the number of mechanical parts in the receiver. (The manual frequency tuning required the rotation of a mechanical variable condenser gang.) In his discussion of the theory of operation, he noted that the operation was similar to the automatic volume control loops which had been used in receivers for several years.

There were two primary elements in Travis' design. The first was the oscillator itself which was tuned by electrodynamic methods. The second was the frequency discriminator which developed the error control voltage to control the oscillator. His first discriminator was a differential rectifier, similar to the discriminator developed by Foster and Seely in 1939 [8]. This circuit today is known as the Foster-Seely discriminator.

Foster and Seely presented a number of innovative circuits, but surprisingly, there was no control theory presented for their frequency control circuits. R.V. Pound's description of automatic frequency control for microwave oscillators was similar [1]. It was mainly concerned with the art of circuit design. (Of course the circuits were all tube-based during this era.)

In 1939, Vincent Rideout described a servomechanical automatic frequency control circuit [9]. At this time, the DC stability of amplifiers was poor, and maintaining a constant control voltage was difficult. As he noted, a servomechanical tuning was desirable because the electronic control amplifier did not have to accumulate the error voltage. The control circuit only had to make differential corrections to the oscillator frequency. His 4 GHz synthesizer used a Foster-Seely discriminator and a two-phase induction motor to tune a waveguide resonator. Later in 1960, T.J. Rey wrote, "[phase-locked loops have] developed from a method of motor tuning in which the oscillation and the reference are combined to generate a field that rotates at the error frequency." [19]

During World War II, there were new requirements and expectations for servomechanisms. To meet this challenge, great advances were made in control theory during the war years. When MacColl published his text, Fundamental Theory of Servomechanisms [10] in 1945, control theory was considered an old art. However, it was at this time that the order of the differential equations became so high that new analysis techniques were needed. (Of course these evolved to the Laplace techniques that we use today.)

For many years; generally until the 60's, the early radios did not have automatic frequency synchronization or Automatic Fine Tune (AFC). To help consumers tune their radios, visual indicators were provided for some receivers. Figure 1.1 shows a representation of the tube indicator and the visual cues provided to the user [11]. The control voltages were much larger than today's small signal levels. The discriminator voltage to the General Electric 6AL7-GT tube shown in Figure 1.1 was ± 10 Volts.

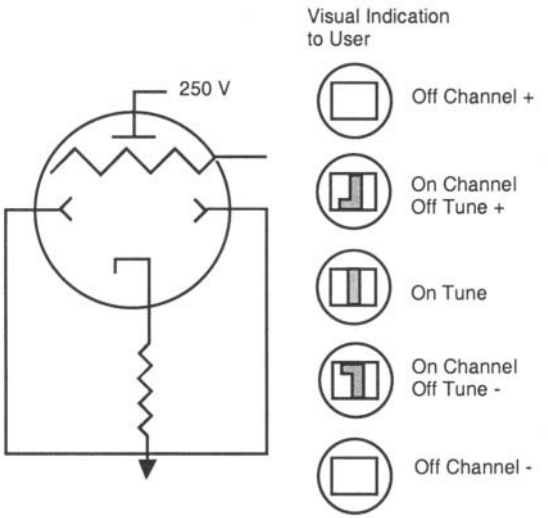


Figure 1.1 Frequency Tuning Indicator in Early Radios [11]

The applicability of feedback amplifier theory to automatic volume control circuits was presented by Oliver in 1948 [12]. Oliver's analysis of the volume control circuit included the use of Nyquist diagrams and Bode plots.

Also in 1948, the Collins Radio Company of Cedar Rapids, Iowa, produced an exciter for commercial FM transmitters that used a quartz crystal discriminator to stabilize the center frequency [13]. (Collins was previously the Crosley Broadcasting Corporation of Cincinnati, Ohio.) The Federal Communications Commission (FCC) required the center frequency of the FM broadcasters to be within 2000 Hz of their assigned frequency.

In 1952, Ruston developed a simple crystal discriminator for FM local oscillators [14]. Although variable capacitance diodes now replace the

reactance tube, his block diagram of the system in Figure 1.2 is similar to today's frequency control loops. Without the automatic frequency control, consumer radios had a frequency stability of about 0.1%. With that era's high gain amplifiers (G=250), the control circuit of Figure 1.2 would yield a frequency stability of about 0.0004%.

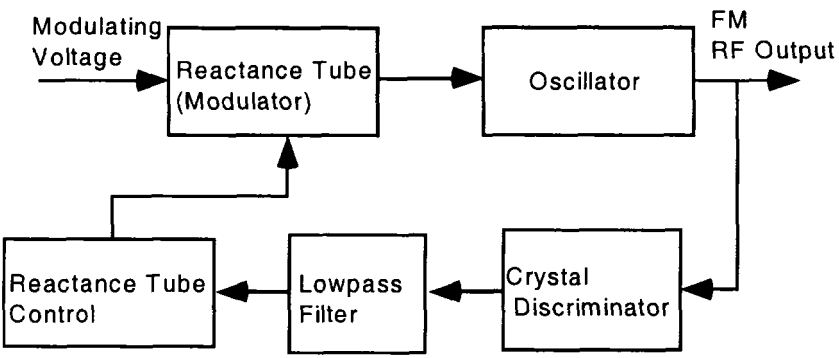


Figure 1.2 Ruston's Automatic Frequency Control Loop [14]

About 1953, phase-locked loop designers began studying the nonlinear operation of the circuits. Curiously, some of the analysis techniques came from unrelated fields. The second order differential equation of the phase-locked loop, $\frac{d^2\phi}{d\tau^2} + \frac{\lambda\, d\phi}{d\tau} - Cos[\phi] = -\nu$, was analyzed with a technique associated with the pull-out torque of synchronous motors [15,16]. This was the technique used by Rey [19] and Viterbi [21] to generate the phase-plane portraits of phase-locked loop acquisition.

Color television would not have been possible without the advancement of phase-locked loop technology. In particular, the color subcarrier at 3.158 MHz required precise phase control to maintain color picture stability in the NTSC format. Richman [17] was the first to develop equations describing acquisition time for a first order phase-locked loop. It is a fascinating history of television, to read the derived requirements of these first phase-locked loops.

In the early 1950s, a "good" phase-locked loop would adjust the television's color within a second. A "fair" phase-locked loop would adjust the color within 10 seconds. The phase-locked loop in the color subcarrier circuit was originally to replace a phase control "knob" that the consumer

would adjust manually as a new station was tuned. Of course, the oscillators were all tube-based, and the frequency of the loop was tuned with a reactance tube.

A block diagram of Richman's Automatic Phase Control (APC) circuit is shown in Figure 1.3. The passive loop filter in Figure 1.3 presented a dilemma to the early designers. Five rms degrees of dynamic phase error was the subjective threshold for consumer acceptance. Static phase error would produce the wrong hue in the received picture. Dynamic phase error, however, generated fluctuating horizontal color streaks. In order to keep the phase jitter at acceptable levels, a 100 Hz loop bandwidth was required. Yet this noise bandwidth would limit acquisition to 25 seconds for an oscillator frequency offset of 2.5 kHz [18].

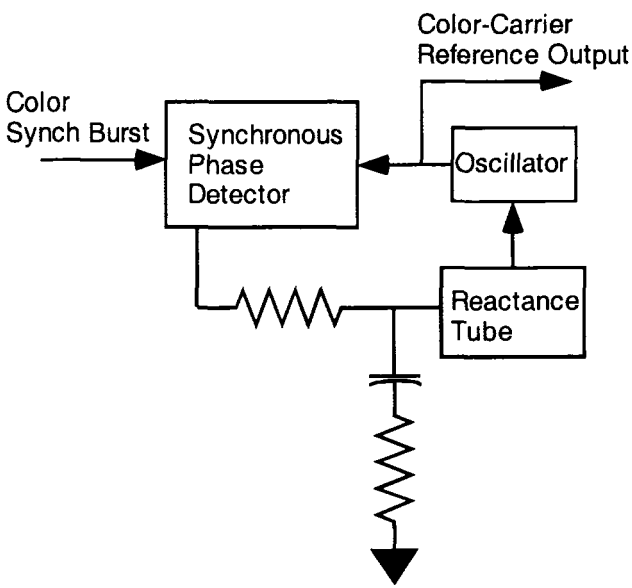


Figure 1.3 Automatic Phase Control Circuit [18]

By 1959, analog phase-locked loop theory and design was approaching maturity. The textbooks and literature at the time still emphasized the analog to servomechanisms. The wider applicability of phase-locked loops resulted from the acceptance of the PLL as a lowpass filter for FM inputs and a highpass filter to the output oscillator. McAleer [21] wrote that there were three uses for phase-locked loops: 1) In a receiver to increase the power level and attenuate the noise of a weak FM signal, 2) can be used to reduce the

jitter or frequency noise of a high-powered oscillator, 3) as a narrowbandwidth filter.

The history of phase-locked loops becomes difficult to write after 1960 due to an explosive interest and publications in the field. The availability of phase-locked loop integrated circuits in 1965 [22] facilitated the rapid introduction of phase-locked loops into consumer products. About 1970, digital or sampled, phase-locked loops began appearing in the literature and products. Gupta's [23] 1975 survey paper provides some of the history of analog loops and Lindsey and Chie's [24] 1981 paper provides some insight to the development of the digital phase-locked loops.

The history of optical phase-locked loops is more recent, since the laser was not invented until 1960 [25]. The first laser phase-locked loop was demonstrated four years later [26]. A block diagram is shown in Figure 1.4.

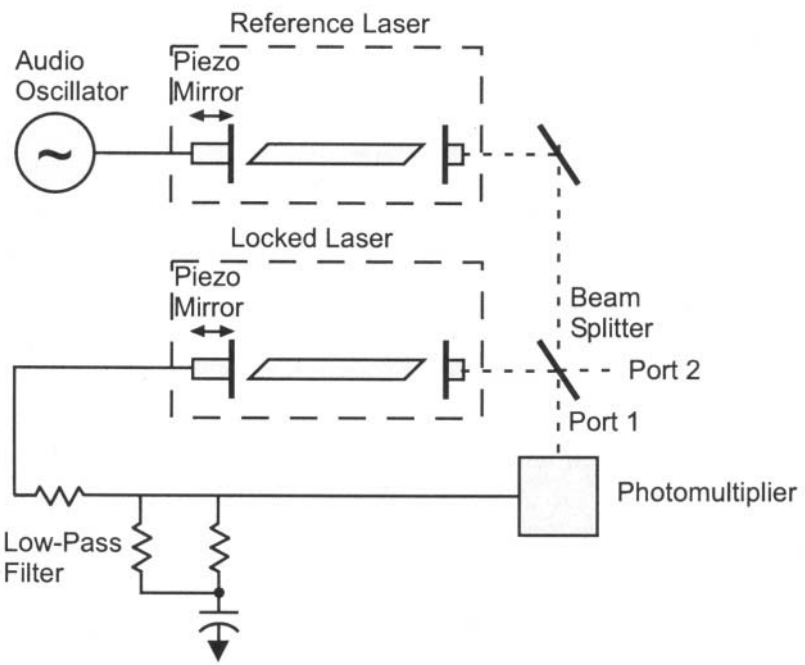


Figure 1.4 Laser Phase-Locked Loop [26]

Helium-neon lasers were locked in quadrature using the photomultiplier (a RCA-7265) to provide error feedback to the piezo mirror in Figure 1.4.

The piezo mirror changes the length of the laser cavity, thus changing the operating frequency of the laser.

Earlier attempts or experiments had been failures because of acoustical and mechanical disturbances. The first success was achieved through placing the lasers on a shock-mounted concrete and cinder block table enclosed in a concrete vault. Inside this vault, the lasers were able to remain phase-locked for several hours. Temperature drift eventually caused the lasers to lose lock [26].

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# 2

# Analog Phase-Locked Loops

## 2.1 Time Domain Analysis of Phase-Locked Loops

A complete Phase-Locked Loop (PLL) block diagram is shown in Figure 2.1. The PLL is receiving a signal s(t), with an unknown phase, $\theta(t)$. Viterbi [18] has described the phase-locked loop as a communications receiver that adjusts the local oscillator frequency and phase according to its measured phase error. Although PLLs are found in applications besides receivers, the PLL in Figure 2.1 is performing as a local oscillator to coherently demodulate the received signal. (Recall from communication theory that coherent demodulation provides a 3 dB improvement in signal-to-noise. In Chapter 11 we will show that the signal-to-noise improvement is 6 dB inside a synchronization loop.)

In Figure 2.1, we assign an amplitude, $\sqrt{2P}$, to the received signal, s(t), where P is the power in the signal. Initially, the magnitude $\sqrt{2P}$ for the received signal may seem awkward. Recall however, the power in the signal $x(t)=A\cos(2\pi f t)$ is $P = A^2/2$. Algebraic manipulation yields $A = \sqrt{2P}$, the assumed magnitude for the input phasor in Figure 2.1. In some applications such as frequency synthesizers, the signal into the phase-locked loop has a fixed signal level and a high Signal-to-Noise Ratio (SNR). More stressful on loop performance however, are those applications with varying

signal levels and low SNRs. In our subsequent derivations we will see that these two parameters affect the performance of the loop.

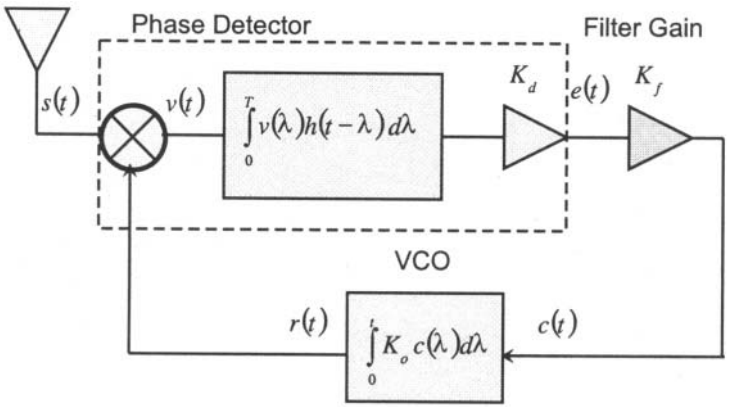


Figure 2.1 Simple Phase-Locked Loop

The phase detector for a PLL measures the phase difference between the input signal and the PLL's voltage controlled oscillator. This phase difference is converted to a voltage in the phase detector, which is then used to provide feedback control to the local oscillator. Associated with the phase detector is a gain, $K_{\det ector} = K_d$, which represents the mapping of the phase error in radians to an output with units, volts/radians. In Figure 2.1, the phase detector is represented as a mixer with a lowpass filter, which is a common implementation. An ideal mixer will produce a frequency difference component and frequency summation component,

$$Cos[2\pi f_0 t + \theta] \times Sin[2\pi f_0 t + \hat{\theta}] = \frac{1}{2}Sin[4\pi f_0 t + \theta + \hat{\theta}] + \frac{1}{2}Sin[\theta - \hat{\theta}] \quad 2\text{-}1$$

where

$\theta$ is the signal's unknown phase

$\hat{\theta}$ is the PLL's estimate of the phase, $\theta$

In analog phase-locked loops, we are most interested in the baseband component, $\frac{1}{2}Sin\left[\theta - \hat{\theta}\right]$ that is used to generate an error voltage for correcting the loop's oscillator. In most instances, the high frequency component, $\frac{1}{2}Sin\left[4\pi f_0 t + \theta + \hat{\theta}\right]$ will be ignored by the loop filter and oscillator, but we include a lowpass filter to eliminate this term inside the phase detector.

Later in the analysis of analog phase-locked loops, we will discuss the s-domain representation and then represent the lowpass filter inside the phase detector as $H(s) = \frac{\alpha}{\alpha + s}$. However, the other functions in Figure 2.1 are time-domain functions, and for the initial presentation of the phase-locked loop, we choose to represent the function in the time domain for consistency. If the cutoff frequency of the filter is much greater than the carrier frequency, $f_c$, then the indicated convolution can be approximated by a sifting function, and then the error voltage is approximately

$$e(t) \approx \sqrt{2P}K_d K_o Sin\left[\int c(t)dt - \theta(t)\right] \qquad 2\text{-}2$$

Figure 2.1 has a filter consisting of a simple gain scalar, $K_{filter} = K_f$. The lowpass filter in Figure 2.1 used to eliminate the mixer sum products adds additional poles to the loop transfer function, so it cannot be a first order loop. (When we introduce the s-domain representation, we will make a formal definition of loop order and type.)

The local oscillator's output, r(t), may appear troubling at first, because of the integral inside the sine argument. Historically, analog Voltage Controlled Oscillators (VCOs) have received a voltage as an input, and generated a frequency output. However, in Figure 2.1, the error voltage from the mixer, c(t), (Equation 2-1) represents a phase error rather than a frequency error.

Recall the phase of a sinusoid is the accumulation, or integral of all instantaneous frequency components. The phase of the local oscillator can be written as

$$\theta(t) = 2\pi\int_0^t f(\tau)\, d\tau + \theta(t = 0) \qquad 2\text{-}3$$

Equation 2-3 shows that the VCO performs an integration with respect to the phase error. In Figure 2.1, the error voltage, c(t) corresponds to a phase error, so the VCO in a phase-locked loop effectively integrates c(t), to produce a phase correction. The transducer gain of the VCO is $K_{oscillator} = K_o$ *radians/Volt.*

To generate the phase error, e(t), we have performed a simple lowpass filter function on the output of a mixer. The mixer's output prior to the lowpass filter is

$$v(t) = 2\sin\left(2\pi f_c t + \int c(t)dt\right) \times \sqrt{2P}\cos\left(2\pi f_c t + \theta(t)\right) \qquad 2\text{-}4$$

After performing trigonometric reductions,

$$v(t) = \sqrt{2P}\sin\left(4\pi f_c t + \int c(t)dt + \phi(t)\right) + \sqrt{2P}\sin\left(\int c(t)dt - \theta(t)\right) \qquad 2\text{-}5$$

Notice that the last term of Equation 2-5 represents the phase difference between the received signal and the local oscillator. For this reason, it is named a phase detector, rather than frequency detector. Frequency detectors are sometimes used in control loops (Automatic Frequency Control (AFC)), but they are more complex than the simple mixer shown in Figure 2.1 [1].

Equation 2-5 implies the error voltage is a sinusoidal function. Because $\sin[\theta] = \sin[\theta + k\,2\pi]$, where k is an integer, the phase detector of Equation 2-5 is invariant to a $k\,2\pi$ radian phase shift. In Chapter 11, we will discuss phase detectors that are invariant to $\pi$ or even $\pi/2$ phase shifts. (This presents problems in synchronizing to digital modulation waveforms such as BPSK or QPSK.)

For our initial study of Figure 2.1, we need to linearize Equation 2-5 so that we can write a simple control loop equation. To linearize Equation 2-5, we expand a first-order Taylor series of the sine function around zero, $\sin[x] \approx \sin[0] + (x-0)\sin'[0] = x$. (The double frequency is discarded because it is removed by the lowpass filter.) From this we obtain,

$$e(t) = \sqrt{2P}\left(\int c(t)dt - \theta(t)\right) \qquad 2\text{-}6$$

After the linearization, we can simplify the loop block diagram to the more familiar form shown in Figure 2.2.

A frequency-dependent loop filter is not included in the loop configuration of Figure 2.2. The loop filter is really a scalar gain term, $K_f$. This is the only variable to alter the first-order loop's performance. Because the phase detector is represented by an arithmetic summer (traditional control loop representation) [2-3] rather than a multiplier, the magnitude $\sqrt{2P}$ of the received signal is included within the phase detector.

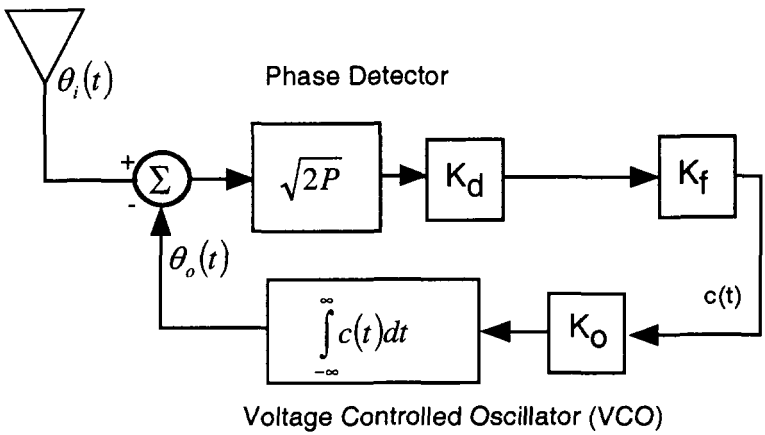


Figure 2.2 Linearized Phase-Locked Loop

The output of the phase detector, $\theta_e(t)$, represents the difference between the input $\theta_i(t)$, and the VCO's estimate of the input, $\theta_o(t)$. By solving for this difference, $\theta_e(t)$, we obtain a mathematical representation of how well the phase-locked loop is tracking the input.

$$c(t) = K_f\ \theta_e(t) \qquad 2\text{-}7$$

$$\theta_e(t) = \sqrt{2P}\,K_d\left(\theta_i(t) - K_o\int c(t)dt\right) \qquad 2\text{-}8$$

Substituting Equation 2-7 into Equation 2-8 yields

$$\theta_e(t) = \sqrt{2P}\,K_d\left(\theta_i(t) - K_o\int K_f\ \theta_e(t)dt\right) \qquad 2\text{-}9$$

Integral equations such as Equation 2-9 are difficult to solve, so we use the differential form of Equation 2-9.

$$\theta_e'(t) + \sqrt{2P}\,K_d\,K_f\,K_o\,\theta_e(t) = \sqrt{2P}\,K_d\,\theta_i'(t) \qquad 2\text{-}10$$

This is a first-order differential equation. Recall the following theorem for first-order differential equations [16]:

if $f' + \alpha f = g$ on interval I

$$\Leftrightarrow f = e^{-A}\left(\int g e^{A}\right) + ce^{-A} \quad \text{for some constant c} \qquad 2\text{-}11$$

where A denotes any indefinite integral of the function $\alpha$

For Equation 2-10, $A(t) = \int \alpha(t)dt = \sqrt{2P}\,K_d\,K_f\,K_o\,t$, so substituting this into Equation 2-11 yields

$$\theta_e(t) = e^{-\sqrt{2P}K_dK_fK_ot}\int\left\{e^{\sqrt{2P}K_dK_fK_ot}\theta'(t)\right\}dt + ce^{-\sqrt{2P}K_dK_fK_ot} \qquad 2\text{-}12$$

where c is a constant

For most phase-locked loop applications, the phase input, $\theta(t)$, to the loop is a combination of three different phase functions.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant. This corresponds to a constant phase offset between the input signal's phase and the initial VCO's phase. Of course, the PLL will correct the phase difference to zero by changing the phase of the VCO.

Since $\theta'(t) = 0$, the solution of Equation 2-12 provides

$$\theta_e(t) = ce^{-\sqrt{2P}K_dK_fK_ot} \qquad 2\text{-}13$$

If we let error(0)=$\Delta\theta$, (the loop error at time t=0 is equal to the step in phase) we can solve for the constant c, and obtain

$$\theta_e(t) = \Delta\theta e^{-\sqrt{2P}K_dK_fK_ot} \qquad 2\text{-}14$$

By taking the limit as $t \to \infty$, for Equation 2-14, the steady-state response is computed as $\lim_{t\to\infty}\left\{\Delta\theta e^{-\sqrt{2P}K_dK_fK_ot}\right\} = 0$. This indicates that the first order phase-locked loop will completely adjust the VCO's phase to compensate for an input phase offset. The steady-state error is zero.

**Case II.** $\theta(t) = 2\pi f_\Delta t$ This signal input to a phase-locked loop is equivalent to a constant frequency.

(Recall radian frequency = $\frac{d}{dt}\{2\pi f_\Delta t\} = 2\pi f_\Delta$). With this signal, the input has a constant frequency offset from the initial frequency of the VCO. In a communications receiver, this would correspond to the receiver's local oscillator not being centered at the correct frequency. However, if the PLL is able, it will reduce the initial frequency difference. For this input, $\theta'(t) = 2\pi f_\Delta$, and the solution of Equation 2-10 is

$$\theta_e(t) = e^{-\sqrt{2P}K_d K_f K_o t}\int\left\{e^{\sqrt{2P}K_d K_f K_o t} 2\pi f_\Delta\right\}dt + ce^{-\sqrt{2P}K_d K_f K_o t} \qquad 2\text{-}15$$

$$\theta_e(t) = \frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} + c\,e^{\sqrt{2P}K_d K_f K_o t} \qquad 2\text{-}16$$

With $\theta(t) = 2\pi f_\Delta t$, at time t=0, the initial error, $\theta_e(0) = 0$. This initial condition allows us to solve for the constant c, and we obtain

$$\theta_e(t) = \frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} - \frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} e^{-\sqrt{2P}K_d K_f K_o t} \qquad 2\text{-}17$$

We are interested in the steady-state error, after the loop has attempted correcting this changing phase input. By taking the limit as $t \to \infty$, for Equation 2-17, the steady-state response is computed as $\lim_{t\to\infty}\left\{\frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} - \frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} e^{-\sqrt{2P}K_d K_f K_o t}\right\}$. The limit, or steady-state response is computed as

$$\lim_{t\to\infty}\theta_e(t) = \frac{2\pi f_\Delta}{\sqrt{2P}K_d K_f K_o} \qquad 2\text{-}18$$

Equation 2-18 indicates that the first-order phase-locked loop will have a constant error when the input phase is constantly increasing. (Note that our analysis so far is only for a first-order phase-locked loop that has

$F(s) = \mathrm{K_f}$.) If the phase-locked loop has a large DC gain corresponding to the product $\sqrt{2P}\,K_d \mathrm{K_f}\, K_o$, then the steady-state phase error may be small and acceptable. The magnitude of the error may be reduced by increasing the gain factor $\mathbf{K_f}$, or the input signal power, P.

**Case III.** $\theta(t) = 2\pi \dot{f}_\Delta t^2$ This signal corresponds to a constant accelerating phase input. With respect to frequency, the input frequency is a linear function (frequency ramp), and with respect to phase, it is a parabolic ramp. This type of input occurs frequently with communications or GPS receivers [5]. In the communications literature this is termed a Doppler input because it generally is created by a moving transmitter or receiver [9]. With $\theta'(t) = 4\pi \dot{f}_\Delta t$, we substitute into Equation 2-12,

$$\theta_e(t) = e^{-\sqrt{2P}K_d \mathrm{K_f} K_o t} \int e^{\sqrt{2P}K_d \mathrm{K_f} K_o t} 4\pi \dot{f}_\Delta t \, dt + c e^{-\sqrt{2P}K_d \mathrm{K_f} K_o t} \qquad 2\text{-}19$$

Since $\theta(t)$ is a function of time, and $\theta(0) = 0$, it is reasonable to assume $\theta_e(0) = 0$. As before, it allows us to solve for the constant c. The phase error can then be written as

$$\theta_e(t) = \frac{-4\pi \dot{f}_\Delta}{\left(\sqrt{2P}K_d \mathrm{K_f} K_o\right)^2} + \frac{4\pi \dot{f}_\Delta t}{\sqrt{2P}K_d \mathrm{K_f} K_o} + \frac{4\pi \dot{f}_\Delta}{\left(\sqrt{2P}K_d \mathrm{K_f} K_o\right)^2} e^{-\sqrt{2P}K_d \mathrm{K_f} K_o t} \qquad 2\text{-}20$$

Note that with the frequency ramp input, the phase-locked loop has an increasing phase error, indicated by the second right-hand term of Equation 2-20. This is not necessarily unacceptable, because the requirements of the phase-locked loop may have an accelerating input for only a short time duration. In such a situation, the error of Equation 2-20 might not cause loss of lock or degradation of the phase-locked loop's system. However, if the Doppler input lasts for several seconds as with the space shuttle communications [15], then the error is unacceptable and second-order or third-order phase-locked loops are required. Regardless, in Equation 2-20, we can reduce the initial magnitude of the error by increasing the signal power, $\sqrt{2P}$, or loop gain factor, $K_d \mathrm{K_f}\, K_o$.

These three signal inputs are important considerations for phase-locked loop design. We will discuss the second order loop responses later. Figure 2.3 graphs the error responses, $\theta_e(t)$, for the three different inputs.

In Equations 2-14, 2-17, and 2-20, the error function is exponentially affected by the amplitude, $\sqrt{2P}$, of the received signal, s(t). When actually implementing a PLL, the designer must control the input amplitude. Otherwise, the varying amplitude value will change the time response of the system.

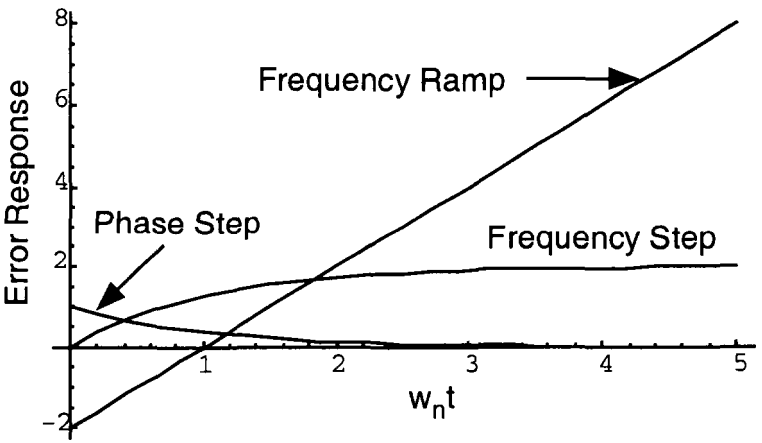


Figure 2.3 First Order Loop Responses for Different Phase Inputs

This is a particular problem with communication receivers. Often a limiter is placed ahead of the phase detector or an Automatic Gain Control (AGC) circuit (or algorithm) is used to control the amplitude [6]. Both solutions have limitations and can affect the designed PLL performance.

## 2.2 Frequency Domain Analysis of Phase-Locked Loops

Reconsider the simple phase-locked loop of Figure 2.2. In Case II and Case III above, we noted that improvements must be made to the loop filter to accommodate frequency steps and ramps, which are characteristic of received signals. As an example, suppose we design a filter with impulse function $h(t) = \frac{b}{a}\delta(t) + \frac{1}{a}u(t)$. To obtain a differential equation for the phase-locked loop's output, we must perform continuous-time convolutions, because the different time functions in Figure 2.2 are cascaded in series.

After performing the convolutions we then must solve a difficult differential equation to obtain the equivalent of Equation 2-12, although solutions do exist for a limited number of higher order differential equations [16].

To simplify the analysis of higher order phase-locked loops, we make use of Transform Theory. For the analog phase-locked loops we will utilize the Laplace transform and later for the digital phase-locked loops, we will use the Z-Transform. The transforms are convenient because they eliminate the troublesome convolutions and the difficult differential equations. For the analysis of phase-locked loops, there are seven fundamental properties of the Laplace transform: [2-4]

$$F(s) = \int_{-\infty}^{\infty} f(t) e^{-st}\, dt \qquad \text{Forward Transform} \qquad 2\text{-}21$$

$$f(t) = \frac{1}{j2\pi} \int_{\alpha - j\infty}^{\alpha + j\infty} F(s) e^{st}\, ds \qquad \text{Inverse Transform} \qquad 2\text{-}22$$

$$\frac{d}{dt} f(t) \leftrightarrow sF(s) - f(0) \qquad \text{Differentiation Theorem} \qquad 2\text{-}23$$

$$\int_0^{t_1}\int_0^{t_2}\cdots\int_0^{t_n} f(\tau) dt_1 dt_2 \cdots dt_n \leftrightarrow \frac{F(s)}{s^n} \qquad \text{Integration Theorem} \qquad 2\text{-}24$$

$$F(s)G(s) \leftrightarrow f(t) * g(t) \qquad \text{Convolution Theorem} \qquad 2\text{-}25$$

$$\lim_{t \to 0} \{f(t)\} = \lim_{s \to \infty} \{sF(s)\} \qquad \text{Initial Value Theorem} \qquad 2\text{-}26$$

$$\lim_{t \to \infty} \{f(t)\} = \lim_{s \to 0} \{sF(s)\} \qquad \text{Final Value Theorem} \qquad 2\text{-}27$$

Equation 2-21 is the forward transform, which defines how to convert a time-domain function to an s-domain function. The definition is rarely used in practice, as Laplace transform tables [2-4] (and Appendix A) provide conversions for all but the most unusual time-domain functions. As we will see in subsequent analysis, the Laplace transform of a phase-locked loop usually results in a polynomial equation. Because the equations are in

convenient polynomial form, roots of the equations can be easily computed. This reduces the difficulty of obtaining the inverse transform. The inverse transform is defined in Equation 2-22, but is rarely used, as tables and root techniques allow the computation of most functions. (In Equation 2-22, the integral limits assume $\alpha$ is within the region of convergence for the Laplace transform [2].)

The differentiation theorem expressed in Equation 2-23 will be used frequently to include initial conditions of a phase-locked loop into its transfer function. If the initial condition is zero, then the last term of Equation 2-23 is zero, and not necessary. The integration theorem, Equation 2-24, is useful in computing the Laplace transforms of the different types of phase inputs.

The main reason for using Laplace transforms in phase-locked loop analysis is shown in Equation 2-25. Instead of the difficult convolution of time-domain functions such as the VCO's $\int c(t)dt$ and the loop filter's h(t), the Laplace equivalents of 1/s and H(s) can be simply multiplied together. Polynomial multiplication provides the cascaded response of complex loop configurations.

Earlier, we found it necessary to find the steady-state response of the phase-locked loop with a specified signal input. Equation 2-27 allows the computation of the steady-state response in the Laplace domain. This is useful, because it allows the steady-state response to be computed without an inverse transformation to the time-domain. The initial value theorem, Equation 2-26 provides similar utility in computing the initial condition of a phase-locked loop.

## 2.3 Partial Fraction Expansion

Generally in the analysis or design of phase-locked loops, the Laplace transform tables of [2-4] and Appendix A are sufficient if a partial fraction expansion of the transfer function is performed. The concept behind partial fraction expansion is to express the transfer function as a sum of fractions with a simple pole in each denominator. When this is done, the individual terms can use simple transforms such as,

$$\frac{\chi}{s+\alpha} \leftrightarrow \chi e^{-\alpha t} \qquad 2\text{-}28$$

If all of the poles of a transfer function are simple (not repeated), the transfer function can be written as [4]

$$F(s)=\frac{N(s)}{D(s)}=\frac{N(s)}{(s+\alpha_1)(s+\alpha_2)\cdots(s+\alpha_n)} \qquad 2\text{-}29$$

With partial fraction expansion, Equation 2-29 can be written as

$$F(s)=\frac{K_{s1}}{(s+\alpha_1)}+\frac{K_{s2}}{(s+\alpha_2)}+\ldots\frac{K_{sn}}{(s+\alpha_n)} \qquad 2\text{-}30$$

The coefficients for the individual fractions in Equation 2-30 are obtained by multiplying the complete transfer function by the denominator's $(s+\alpha_n)$ and evaluating the resulting expression at $s=-\alpha_n$. To demonstrate, [4]

$$K_{s1}=(s+\alpha_1)\frac{N(s)}{D(s)}\bigg|_{s=-\alpha_n} \qquad 2\text{-}31$$

The other numerators of Equation 2-30 are obtained through similar computations. Equation 2-30 is also used to find the coefficients for roots which appear as conjugate pairs. Example 2.1 shows the partial fraction expansion of a transfer function with conjugate pairs.

The more difficult partial fraction expansion occurs when the transfer function of Equation 2-29 contains poles that are repeated. As an example, consider

$$F(s)=\frac{N(s)}{(s+\alpha)^n} \qquad 2\text{-}32$$

The partial expansion of Equation 2-32 is performed as

$$F(s)=\frac{K_{2,\alpha}}{(s+\alpha)}+\frac{K_{2,\alpha}}{(s+\alpha)^2}+\cdots\frac{K_{n,\alpha}}{(s+\alpha)^n} \qquad 2\text{-}33$$

Note in Equation 2-33, a single repeated root results in n terms. The numerators are not obtained through the same expression as the simple poles, but a different set of computations, [4]

$$K_{\alpha,n} = \left\{(s+\alpha)^n F(s)\right\}_{s=-\alpha} \qquad 2\text{-}34$$

$$K_{\alpha,n-1} = \frac{d}{ds}\left\{(s+\alpha)^n F(s)\right\}\Big|_{s=-\alpha} \qquad 2\text{-}35$$

$$K_{\alpha,n-2} = \frac{1}{2!}\frac{d^2}{ds^2}\left\{(s+\alpha)^n F(s)\right\}\Big|_{s=-\alpha} \qquad 2\text{-}36$$

$$K_{\alpha,1} = \frac{1}{(n-1)!}\frac{d^{n-1}}{ds^{n-1}}\left\{(s+\alpha)^n F(s)\right\}\Big|_{s=-\alpha} \qquad 2\text{-}37$$

## *Example 2.1*

Using partial fraction expansion, find the inverse Laplace Transform of

$$F(s) = \frac{9}{s+9}\frac{3}{s^2}\frac{10^2}{s^2+10^2} \qquad 2\text{-}38$$

From Equations 2-30 and 2-33, the partial fraction expansion of Equation 2-38 is expected to be of the form,

$$F(s) = \frac{K_{-9}}{s+9} + \frac{K_{0,1}}{s} + \frac{K_{0,2}}{s^2} + \frac{K_{-j10}}{s+j10} + \frac{K_{+j10}}{s-j10} \qquad 2\text{-}39$$

The first numerator, $K_{-9}$ corresponds to the pole at s=-9. Using Equation 2-31, we compute

$$K_{-9} = \left\{(s+9)\frac{9}{s+9}\frac{3}{s^2}\frac{10^2}{s^2+10^2}\right\}_{s=-9} = \frac{100}{543} \qquad 2\text{-}40$$

The next two coefficients, $K_{0,1}$ and $K_{0,2}$ are obtained from Equations 2-34 and 2-35.

$$K_{0,2} = \left\{ s^2 \frac{9}{s+9} \frac{3}{s^2} \frac{10^2}{s^2+10^2} \right\}_{s=0} = 3 \qquad 2\text{-}41$$

$$K_{0,1} = \frac{1}{(2-1)!} \frac{d^{2-1}}{ds^{2-1}} \left\{ s^2 \frac{9}{s+9} \frac{3}{s^2} \frac{10^2}{s^2+10^2} \right\}_{s=0} = -\frac{1}{3} \qquad 2\text{-}42$$

Although the complex pair poles are computed in the same manner as $K_{-9}$, we have saved them for last because of their complex nature.

$$K_{-j10} = \left\{ (s+j10) \frac{9}{s+9} \frac{3}{s^2} \frac{10}{s+j10} \frac{10}{s-j10} \right\}_{s=-j10} = \frac{27}{362} - j\frac{243}{3620} \qquad 2\text{-}43$$

$$K_{+j10} = \left\{ (s-j10) \frac{9}{s+9} \frac{3}{s^2} \frac{10}{s+j10} \frac{10}{s-j10} \right\}_{s=+j10} = \frac{27}{362} + j\frac{243}{3620} \qquad 2\text{-}44$$

Substituting the coefficients into the partial fraction expansion equation, Equation 2-39,

$$F(s) = \frac{\frac{100}{543}}{s+9} + \frac{-\frac{1}{3}}{s} + \frac{3}{s^2} + \frac{\frac{27}{362} - j\frac{243}{3620}}{s+j10} + \frac{\frac{27}{362} + j\frac{243}{3620}}{s-j10} \qquad 2\text{-}45$$

Because Equation 2-45 is composed completely of simple poles, transform tables can be used to compute the inverse Laplace transform. From Appendix A, using the transforms, $\frac{1}{s} \leftrightarrow u(t)$, $\frac{1}{s^2} \leftrightarrow t$, and $\frac{1}{s+\alpha} \leftrightarrow e^{-\alpha t}$,

$$f(t) = \frac{100}{543} e^{-9t} - \frac{1}{3} + 3t + \left( \frac{27}{362} - j\frac{243}{3620} \right) e^{-j10t} + \left( \frac{27}{362} + j\frac{243}{3620} \right) e^{-j10t} \qquad 2\text{-}46$$

Noting the complex exponentials, this can be simplified,

$$f(t)=\frac{100}{543}e^{-9t}-\frac{1}{3}+3t+\frac{27(10\,Cos[10t]-9\,Sin[10t])}{1810} \qquad 2\text{-}47$$

The disadvantage of Transform theory is that it hides the subtleties of time-domain operation and performance. This is particularly true for digital control loops where a time delay is a fundamental processing element. In this text we will use Transform theory where it is helpful, but we will always stress the importance of the time domain representation.

In Figure 2.4, the phase-locked loop of Figure 2.2 has been represented in the Laplace domain. Instead of representing the various elements and signal positions in the time-domain, everything has been converted to the s-domain. It is functionally equivalent to the time-domain phase-locked loop representation of Figure 2.2.

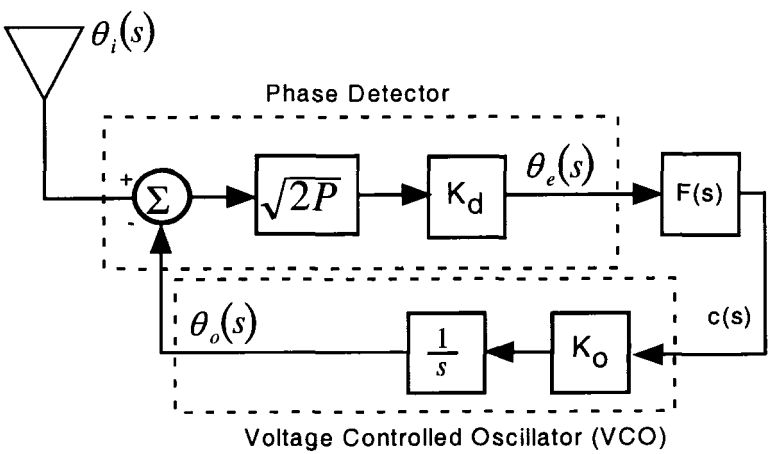


Figure 2.4 Block Diagram of Typical Phase-Locked Loop

In Figure 2.4, we have included separate gains $K_o$ and $K_d$ for the VCO and phase detector. (One VCO might have a response of 100 MHz/Volt, but another might have 10 Hz/Volt.) Similar to Lindsey and Chie's analysis of digital phase-locked loops [7], we have included a gain corresponding to the input level. Most analog phase detectors are actually multiplicative, and the

output of the phase detector will be a function of the input level. For this reason, we have $\sqrt{2P}$ assigned as a gain within the loop.

There are many phase detectors that do not have a $\sqrt{2P}$ scalar for the output. The popular sequential phase detector discussed in Chapter 6 does not have this scalar. The optical phase detectors presented in Chapter 12 typically include the optical light power within the computation of $K_d$, and the additional scalar is not used. In most of our presentations, we will include the scalar, but the reader should be alert for applications where the power is either included in the phase detector gain, or the $\sqrt{2P}$ is effectively unity.

In Figure 2.4, we have used the Laplace transform equivalents of Figure 2.2. In particular, $\int(\,)dt \leftrightarrow 1/s$ is the transformation for the voltage controlled oscillator. Similarly, we have used the Laplace transform F(s) for the loop filter as well.

Due to the advantages of the Laplace transform previously discussed, we can express the s-domain transfer functions of Figure 2.4. H(s) is the transfer function most common in the literature. Using the Laplace Transform, the closed loop transfer function of Figure 2.4 is written as

$$H_o(s) \equiv \frac{\theta_o(s)}{\theta_i(s)} = \frac{\sqrt{2\ P}K_o K_d F(s)}{s + \sqrt{2\ P}K_o K_d F(s)} \qquad 2\text{-}48$$

Note the subscript on $H_o(s)$. The "o" subscript refers to the transfer function using $\theta_o(s)$ as the output, not the open loop transfer function which will be discussed later. To compute Equation 2-48, traditional control loop analysis with negative feedback is performed, $H_o(s) = \dfrac{\text{Forward Gain}}{1 + \text{Total Loop Gain}}$ [2-4]. The forward gain is the gain from the input to the output, in this case, $\theta_o(s)$. In Figure 2.4, the forward gain is computed by inspection as $\dfrac{\sqrt{2P}K_o K_d F(s)}{s}$. The total loop gain is the gain from the input to the output, which for $H_o(s)$, is the same as the forward gain. Some phase-locked loop configurations might have several feedback

points, in which case an analysis technique such as Mason's Rule [2-4] allows the loop transfer function to be readily computed.

Instead of $\theta_o(s)$, sometimes the error signal, $\theta_e(s)$, is often of interest. The magnitude of $\theta_e(s)$ is an indication of how well the PLL is dynamically tracking the input signal, $\theta_i(s)$. In this case, $\text{Forward Gain} = \sqrt{2P}K_d$, and the $\text{Total Loop Gain} = \dfrac{\sqrt{2P}K_o K_d F(s)}{s}$. This definition of $H_e(s)$ may differ with other definitions in the literature. The definition above includes the gain of the phase detector and the amplitude of the input signal, exactly what would be measured in a real implementation. Often this is neglected, and $H_e(s)$ is written without gain terms in the numerator. The transfer function for $\theta_e(s)$ as the output is

$$H_e(s) \equiv \frac{\theta_e(s)}{\theta_i(s)} = \frac{\sqrt{2P}K_d s}{s + \sqrt{2P}K_o K_d F(s)} \qquad 2\text{-}49$$

The reader is cautioned to note the presence of the s-variable in the numerator of Equation 2-49 and not in Equation 2-48. Dropping this term presents difficulties when computing the error responses to different inputs.

## 2.4 First Order Loop Responses

The simple first-order loop of Figure 2.2 has a filter, $f(t) = F(s) = K_f$. Substituting this first-order filter into Equation 2-48 yields

$$H_o(s) = \frac{\sqrt{2P}K_o K_d K_f}{s + \sqrt{2P}K_o K_d K_f} \qquad 2\text{-}50$$

In Equation 2-50, the gain of the phase-locked loop, $\sqrt{2P}K_o K_d K_f$, is the dominant characteristic of the loop transfer function. For a first-order PLL, the only variable available to the designer is the loop gain,

$\sqrt{2P}K_o K_d K_f$. The error transfer function, $H_e(s)$ for the first order loop is

$$H_e(s) = \frac{\sqrt{2P}K_d s}{s + \sqrt{2P}K_o K_d K_f} \qquad 2\text{-}51$$

The error output, $\theta_e(s)$, is obtained from $H_e(s)$ by

$$\theta_e(s) = \theta_i(s) H_e(s) \qquad 2\text{-}52$$

Using Equation 2-52, we can recompute the three signal cases previously computed for the first order loop. We will compute all of these cases with the Laplace Transform technique and compare them to the solutions we obtained from the differential equations.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant. The Laplace transform of this input is $\theta_i(s) = \frac{\Delta\theta}{s}$. From Equations 2-51 and 2-52,

$$\theta_e(s) = \frac{\Delta\theta}{s} \frac{\sqrt{2P}K_d s}{s + \sqrt{2P}K_o K_d K_f} \qquad 2\text{-}53$$

The inverse Laplace transform of $\theta_e(s)$, using Equation 2-22, or transform tables in Appendix A, yields

$$\theta_e(t) = \sqrt{2P}K_d \Delta\theta e^{-\sqrt{2P}K_o K_d K_f t} u(t) \qquad 2\text{-}54$$

This matches our result in Equation 2-14, which we obtained through direct solution of the differential equation. (Note that we have included the gain of the phase detector and input amplitude in Equation 2-54.)

**Case II.** $\theta(t) = 2\pi f_\Delta t$ The Laplace transform of $\theta(t)$ is $\theta_i(s) = \frac{2\pi f_\Delta}{s^2}$.

Again using Equations 2-51 and 2-52, and performing the inverse Laplace transform of $\theta_e(s)$,

$$\theta_e(t) = \frac{\sqrt{2P}K_d 2\pi f_\Delta}{\sqrt{2P}K_o K_d K_f}\left\{1 - e^{-\sqrt{2P}K_o K_d K_f t}\right\}u(t) \qquad 2\text{-}55$$

This agrees with the previous result of Equation 2-17.

**Case III.** $\theta(t) = 2\pi \dot{f} t^2$ The Laplace transform of $\theta(t)$ is $2\frac{2\pi \dot{f}}{s^3}$.

Again using Equations 2-51 and 2-52, and performing the inverse Laplace transform of $\theta_e(s)$,

$$\theta_e(t) = \frac{\sqrt{2P}K_d 2d\Delta\theta}{\left(\sqrt{2P}K_o K_d K_f\right)^2}\left\{\left(\sqrt{2P}K_o K_d K_f\right) + e^{-\sqrt{2P}K_o K_d K_f t} - 1\right\}u(t) \qquad 2\text{-}56$$

This matches the result of Equation 2-20.

## 2.5 Definition of Loop Order

Recall the form of the phase-locked loop's transfer function, $H_o(s) \equiv \frac{\theta_o(s)}{\theta_i(s)} = \frac{\sqrt{2P}K_o K_d F(s)}{s + \sqrt{2P}K_o K_d F(s)}$. The order of the PLL is defined as the highest order of s in the denominator of the loop transfer function. For the first order loop, corresponding to Equation 2-50, the highest order of s is one. In the next section, we will study second order loops which have a term $s^2$ in the numerator. As the phase-locked loop's order is increased, it tends to compensate for an instantaneous change in the next higher derivative of the input [12].

The type of the loop refers to the number of perfect integrators in the loop. A PLL has an implicit perfect integrator with the VCO, so the first order loop is a first order, type 1, loop. A filter, F(s), with a perfect integrator would yield a type 2 loop.

## 2.6 Second Order Phase-Locked Loops

The first order loop analysis for the three different inputs suggests a general equation for the loop filter,

$$f(t) = c_0\delta(t) + c_1 + c_2 t + \cdots + c_{n-1}t^{n-1} \qquad 2\text{-}57$$

The variable n, represents the desired order of the phase-locked loop. Jaffe and Rechtin [17] investigated the optimum loop filters for phase-locked loops for different inputs to the phase-locked loop. Their approach is similar to Weiner filter theory, and for a frequency step input, the optimum filter is found to have the form of the active lead-lag filter discussed below.

The first order loop failed with an input response $\theta(t) = a\,t$, so to provide a matched response to this particular input, we would like a term corresponding *to at.* From Equation 2-57, a second order loop requires a loop filter of the form $f(t) = c_0\delta(t) + c_1$. The Laplace Transform of this filter is

$$F(s) = c_0 + \frac{c_1}{s} = \frac{c_1 + c_0 s}{s} \qquad 2\text{-}58$$

With the appropriate substitutions, this filter can be rewritten in the form

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s} \qquad 2\text{-}59$$

Three traditional filters for a second order loop are shown in Figure 2.5. Note the active loop filter is identical to Equation 2-59, where we attempted to match the filter's response to the phase input. Any of the filters yields a second order loop, although the active lead-lag filter provides superior performance.

The second order control loop is distinguished by the appearance of a second-degree polynomial in the denominator of Equation 2-48. However, specifying the denominator does not uniquely determine performance, because only the active lead-lag filter in Figure 2.5 will produce a type-2 loop. (The other filters do not have perfect integrators.)

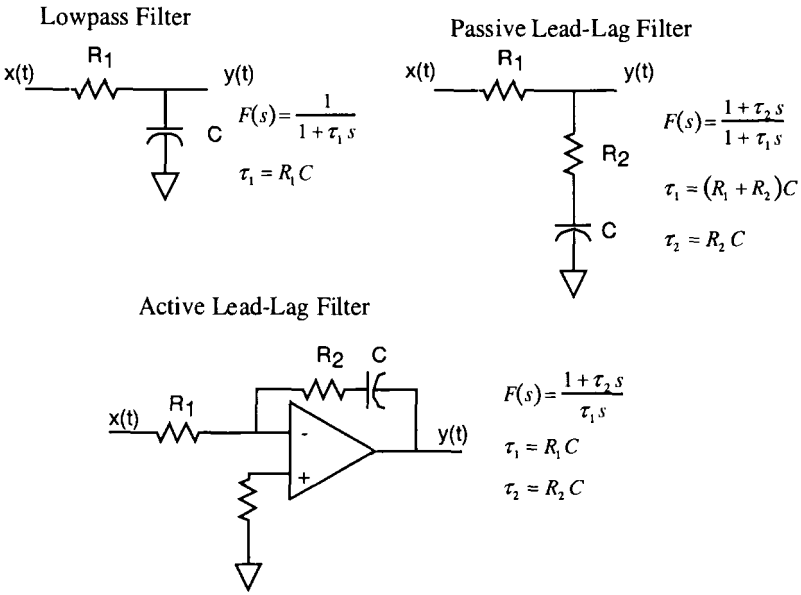


Figure 2.5 Analog Loop Filters [11]

In the first edition, we did not provide the responses for the second order loops with the passive filters, because we felt most current PLL design was being performed with the active filters. However, most low-power designs, especially those with charge pumps are using the passive filters.

We also encountered a modem design where an initial acquisition transient would generate a bias error that remained in the active filter's perfect integrator. Because of the interaction between the carrier and symbol tracking loops, the carrier loop would adjust out the error so that there was no opportunity to remove the bias that had accumulated in the symbol tracking loop's filter. However, the bias remained and caused the modem to eventually lose symbol tracking because the timing bias marched the symbol timing right out of lock.

The solution to this particular problem was the passive lead-lag filter of Figure 2.5. The imperfect integrators of the passive lowpass and lead-lag can help in applications just described.

### 2.6.1 Lowpass Filter Transfer Equations

Substituting the lowpass filter of Figure 2.5 into Equation 2-48 gives a second order, type 1 phase-locked loop,

$$H_{0,Lowpass}(s) = \frac{\sqrt{2P}K_o K_d \dfrac{1}{1+\tau_1 s}}{s + \sqrt{2P}K_o K_d \dfrac{1}{1+\tau_1 s}} = \frac{\sqrt{2P}K_o K_d}{s^2\tau_1 + s + \sqrt{2P}K_o K_d} \qquad 2\text{-}60$$

This is rewritten in the form of traditional control loop analysis [2-4] as

$$H_{0,Lowpass}(s) = \frac{w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 2\text{-}61$$

$$\text{where } w_n = \sqrt{\frac{\sqrt{2P}K_o K_d}{\tau_1}} \quad , \quad \zeta = \frac{1}{2\tau_1}\frac{1}{w_n}$$

The coefficients $w_n$ (loop natural frequency) and $\zeta$ (damping factor) in Equation 2-61 will be discussed in Chapter 3, but note that the loop response is a function of the input power to the loop. Substituting the loop filter's function, $F(s) = (\tau_1 s + 1)^{-1}$, into Equation 2-49, and using the variables defined in Equation 2-61, provides the error response function,

$$H_{e,Lowpass}(s) = \frac{\sqrt{2P}K_d\left(s^2 + 2\zeta w_n s\right)}{s^2 + 2\zeta\, w_n s + w_n^2} \qquad 2\text{-}62$$

The filter's parameters may be computed from the following relationships.

$$\tau_1 = \left(2\sqrt{2P}\,K_O\,K_d\,\zeta\right)^{-1} \qquad 2\text{-}63$$

$$\omega_n = \sqrt{2P}\,K_O\,K_d/\zeta \qquad 2\text{-}64$$

### 2.6.2 Passive Lead-Lag Filter Transfer Functions

Substituting the passive lead-lag filter of Figure 2.5 into Equation 2-48 yields a second order, type 1 phase-locked loop,

$$H_{0,Passive}(s) = \frac{s\sqrt{2P}K_o K_d \tau_2 + \sqrt{2P}K_o K_d}{s^2 \tau_1 + s\left(1 + \sqrt{2P}K_o K_d \tau_2\right) + \sqrt{2P}K_o K_d} \qquad 2\text{-}65$$

To write this transfer function in the normalized servo-mechanism form, we make the substitutions

$$w_n = \sqrt{\sqrt{2P}K_o K_d / \tau_1} \quad , \quad \zeta = \frac{1 + \sqrt{2P}K_o K_d \tau_2}{2\sqrt{\sqrt{2P}K_o K_d \tau_1}} \qquad 2\text{-}66$$

Substituting Equation 2-66 into Equation 2-65, we obtain,

$$H_{0,Passive}(s) = \frac{\tau_2 \omega_n^2 s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \qquad 2\text{-}67$$

Using the definitions of Equation (2-66), we can write the error response of a loop using the lead-lag passive filter as

$$H_{e,Passive}(s) = \frac{s^2 \tau_1 \omega_n^2 / K_O + s\omega_n^2 / K_O}{s^2 + 2\zeta \omega_n s + \omega_n^2} \qquad 2\text{-}68$$

The filter's parameters may be computed from:

$$\tau_1 = \frac{\sqrt{2P}K_O K_d}{\omega_n^2} \qquad 2\text{-}69$$

$$\tau_2 = \frac{2\zeta\sqrt{\sqrt{2P}K_O K_d} - 1}{\sqrt{2P}K_O K_d} \qquad 2\text{-}70$$

### 2.6.3 Active Lead-Lag Filter Transfer Functions

Substituting the active lead-lag filter, $F(s)=\dfrac{\tau_2 s+1}{\tau_1 s}$, into Equation 2-48 yields a second order, type 2 loop,

$$H_{O,active}(s)=\frac{\sqrt{2P}K_o K_d\dfrac{\tau_2 s+1}{\tau_1 s}}{s+\sqrt{2P}K_o K_d\dfrac{\tau_2 s+1}{\tau_1 s}}=\frac{\sqrt{2P}K_o K_d(\tau_2 s+1)}{\tau_1 s^2+\sqrt{2P}K_o K_d(\tau_2 s+1)} \qquad 2\text{-}71$$

Again, we rewrite the transfer function in the form of traditional control loop analysis [2-4],

$$H_{o,active}(s)=\frac{2\zeta w_n s+w_n^2}{s^2+2\zeta w_n s+w_n^2} \qquad 2\text{-}72$$

$$\text{where } w_n=\sqrt{\frac{\sqrt{2P}K_o K_d}{\tau_1}}=\sqrt{\frac{\sqrt{2P}K_o K_d}{R_1 C}}\,,\quad \zeta=\frac{\tau_2 w_n}{2}$$

To help in the design of the physical loop filter, the loop filter coefficients are solved in terms of the servomechanism literature as

$$\tau_1=\frac{\sqrt{2P}K_o K_d}{\omega_n^2} \qquad 2\text{-}73$$

$$\tau_2=\frac{2\zeta}{w_n} \qquad 2\text{-}74$$

The second order active filter of Figure 2.5 is designed by first determining the necessary values of $\tau_1$ and $\tau_2$. Then the relationships $\tau_1=R_1 C$ and $\tau_2=R_2 C$ are used to specify the resistor and capacitor values.

Note that there are three components and only two equations. This allows the independent selection of a convenient value for the capacitor, C, and then computing the values of $R_1$ and $R_2$ that satisfy the requirements of $\tau_1$ and $\tau_2$.

The error response for the loop with the active filter is computed as

$$H_{e,Active}(s) = \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 2\text{-}75$$

Although Equation 2-75 is similar to Equation 2-67, we caution that the definitions of the normalized loop $(\zeta, \omega_n)$parameters are defined differently!

These two error responses may differ from other literature, because we have included the gains associated with the phase detector, which is sometimes not included. Our reasoning is that any laboratory measurement will include these gains, because the measurement will be at the output of the phase detector.

The form of $H_{e,Active}(s)$ in Equation 2-75 is informative. Suppose that we wanted the denominator of $H_{e,Active}(s)$ to have a Butterworth response. The second order Butterworth filter has a prototype transfer function of the form [8]

$$F(p) = \left(p^2 + \sqrt{2}\,p + 1\right)^{-1} \qquad 2\text{-}76$$

This is the normalized form of a Butterworth filter, corresponding to a cutoff frequency of 1 rad/sec. To design a filter with 3-dB roll-off frequency of $w_n$, (instead of the prototype's 1 rad/sec) the substitution $p = s/w_n$ is made to Equation 2-76. This converts the filter to the desired cutoff frequency. With the substitution, the filter's transfer function is

$$F(s) = \left(\frac{s^2}{w_n^2} + \sqrt{2}\frac{s}{w_n} + 1\right)^{-1} = \frac{w_n^2}{s^2 + \sqrt{2}w_n s + w_n^2} \qquad 2\text{-}77$$

Compare $H_{0,Lowpass}(s)$ (Equation 2-61) or $H_{o,Active}(s)$ (Equation 2-72) to the Butterworth filter transfer function in Equation 2-77. If $\zeta = 1/\sqrt{2}$, $H_{0,Lowpass}(s)$ is exactly a Butterworth filter response. If $\zeta = 1/\sqrt{2}$, the denominator of $H_{o,Active}(s)$ has the form of a Butterworth filter. The different parameters of the filters will be discussed in a later chapter, but the value $\zeta = 1/\sqrt{2}$ yields excellent performance, and is used in many PLL designs.

Equations 2-61, 2-67, and 2-72 suggest the phase-locked loop can be considered a bandpass filter centered at the nominal frequency of the VCO. The filtering characteristics of the PLL are the lowpass characteristics of the loop's transfer function. This is illustrated by Figure 2.6 which shows the closed loop responses for different loop damping factors, $\zeta$ of the second order active filter loop.

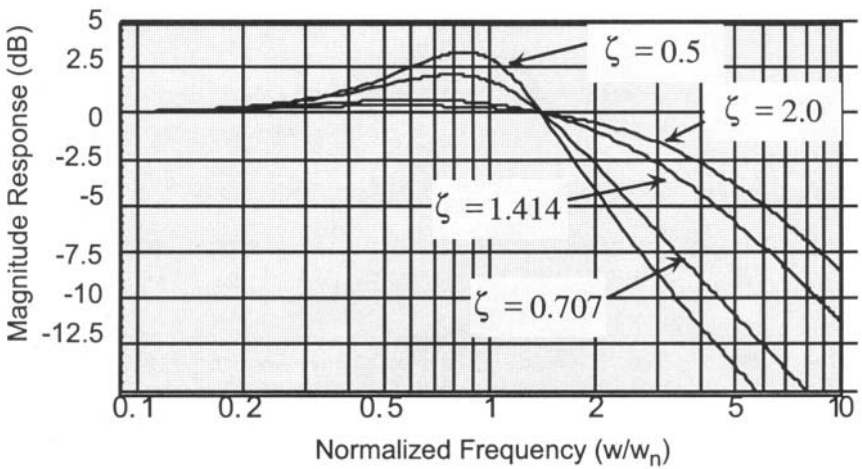


Figure 2.6 Closed Loop Responses of the Second-Order Phase-Locked Loops

Note how the closed loop response resembles a traditional lowpass filter. The peaking of the more responsive loops $\zeta < 1$, may sometimes cause problems in meeting phase noise requirements or spectral containment.

Using Equation 2-75, we re-compute the three signal cases for the active filter, second order loop. The responses will be summarized at the end.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant. The Laplace transform of this input is $\theta_i(s) = \Delta\theta/s$. From Equations 2-52 and 2-75,

$$\theta_e(s) = \frac{\Delta\theta}{s} \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 2\text{-}78$$

The inverse Laplace transform of $\theta_e(s)$, using Equation 2-22, or the transform tables of Appendix A, yields

$$\theta_e(t) = \Delta\theta\sqrt{2P}K_d e^{-\zeta w_n t}\, z(t) \qquad 2\text{-}79$$

$$z(t) = \left( \cos\left(w_n\sqrt{1-\zeta^2}\,t\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(w_n\sqrt{1-\zeta^2}\,t\right)\right) \quad \zeta < 1$$

$$z(t) = (1 - w_n t) \quad \zeta = 1$$

$$z(t) = \left( \cosh\left(w_n\sqrt{\zeta^2-1}\,t\right) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right)\right) \quad \zeta > 1$$

These results are not too difficult to derive. A partial fraction expansion of the error response is first performed. After taking the inverse transform of the two parts, substitutions can be performed to obtain the same form as Equations 2-79. The Laplace Final Value Theorem, Equation 2-27 can be used to obtain the limiting condition of Equation 2-79.

$$\lim_{t\to\infty}\{\theta_e(t)\} = \lim_{s\to 0}\left\{ s\,\frac{\Delta\theta}{s}\,\frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2}\right\} = 0 \qquad 2\text{-}80$$

Observe the second order loop with the active loop filter has a steady-state error response of zero for an input phase step.

**Case II.** $\theta(t) = 2\pi f_\Delta t$ The Laplace transform of $\theta(t)$ is $\theta_i(s) = 2\pi f_\Delta / s^2$ . The s-domain response to this frequency step input is

$$\theta_e(s) = \frac{2\pi f_\Delta}{s^2} \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 2\text{-}81$$

Again using Equations 2-52 and 2-75, then performing the inverse Laplace transform of $\theta_e(s)$,

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-\zeta w_n t} \frac{\sin\left(w_n\sqrt{1-\zeta^2}\,t\right)}{\sqrt{1-\zeta^2}} \quad , \ \zeta < 1 \qquad 2\text{-}82$$

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-w_n t} w_n t \quad , \zeta = 1$$

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-\zeta w_n t} \frac{\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right)}{\sqrt{\zeta^2-1}} \quad , \zeta > 1 \qquad 2\text{-}83$$

The steady state response to the frequency step (phase ramp) is obtained from the final value theorem and Equation 2-75,

$$\lim_{t\to\infty}\{\theta_e(t)\} = \lim_{s\to 0}\left\{ s\frac{2\pi f_\Delta}{s^2} \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \right\} = 0 \qquad 2\text{-}84$$

This is the advantage of using the active filter configuration for the loop filter. Recall the first order loop had a steady-state frequency error for a frequency step. The other filters of Figure 2.5 will also exhibit a steady-state error, although they technically form a second-order phase-locked loop.

**Case III.** $\theta(t) = 2\pi \dot{f} t^2$ The Laplace transform is $\theta_i(s) = 2\frac{2\pi f}{s^3}$ . The Laplace domain response to this frequency ramp input (constantly increasing frequency) is

$$\theta_e(s) = 2\,\frac{2\pi \dot{f}}{s^3} \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 2\text{-}85$$

Again using Equations 2-52 and 2-75; then performing the inverse Laplace transform of $\theta_e(s)$,

$$\theta_e(t) = 2\times 2\pi \dot{f}/w_n^2 - 2\times 2\pi \dot{f}/w_n^2\, e^{-\zeta w_n t}\; z(t) \qquad 2\text{-}86$$

$$z(t) = \left( \cos\left(w_n\sqrt{1-\zeta^2}\,t\right) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(w_n\sqrt{1-\zeta^2}\,t\right) \right) \quad ,\zeta < 1 \qquad 2\text{-}87$$

$$z(t) = w_n t \quad ,\zeta = 1$$

$$z(t) = \left( \cosh\left(w_n\sqrt{\zeta^2-1}\,t\right) + \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right) \right) \quad ,\zeta > 1 \qquad 2\text{-}88$$

The steady-state response to the frequency ramp is obtained from the Final Value Theorem and Equation 2-75,

$$\lim_{t\to\infty}\{\theta_e(t)\} = \lim_{s\to 0}\left\{ s^2 \frac{2\pi \dot{f}}{s^3}\, \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} \right\} = 2\frac{2\pi \dot{f}\sqrt{2P}K_d}{w_n^2} \qquad 2\text{-}89$$

This is a limitation of the second-order loop. A constantly increasing frequency input can soon develop a significant error in the loop's output. This is particularly true for loops with small $w_n$. The three loop responses for the active second order loop are shown in Figure 2.7 through 2.12. Because the damping factor, $\zeta$, is an independent design parameter, the responses are shown for different values of $\zeta$.

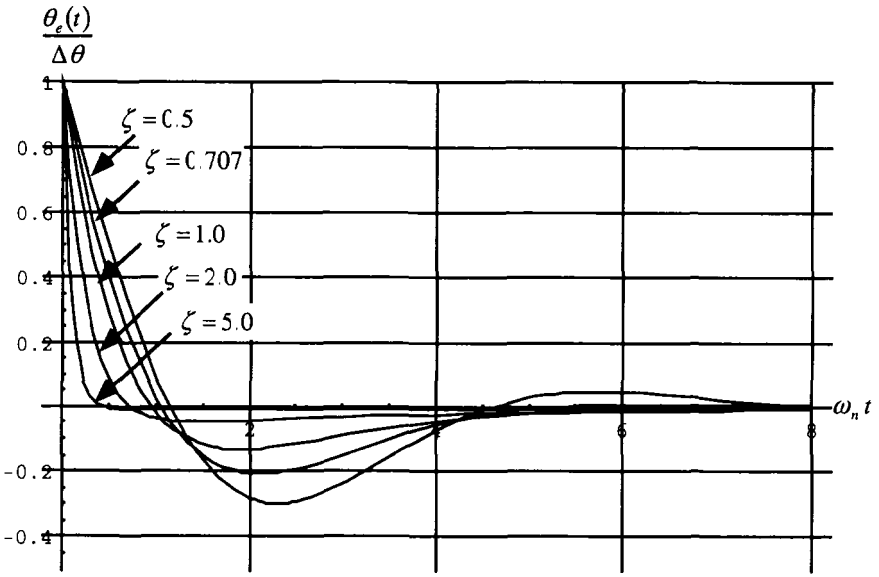


Figure 2.7 Phase Step Response of Second Order Active Filter Loop

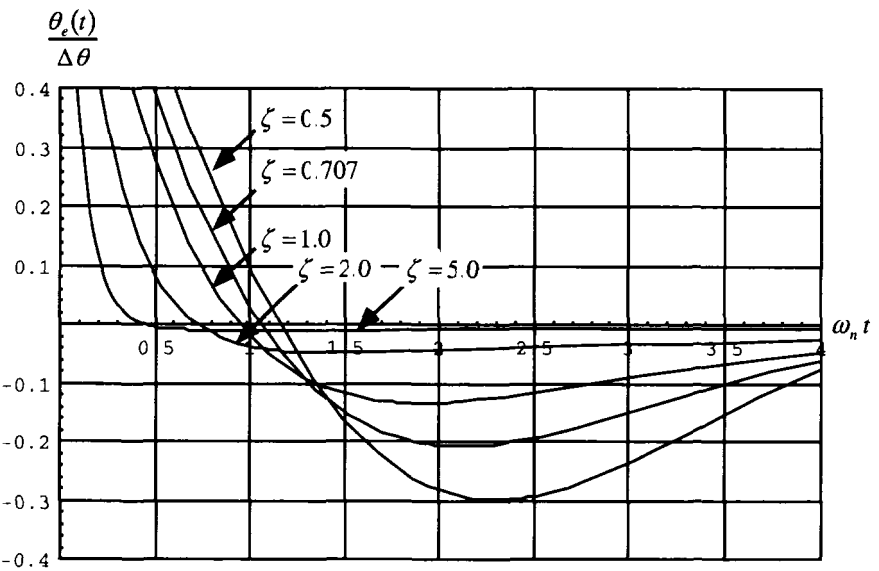


Figure 2.8 Phase Step Response of Second Order Active Filter Loop (Magnified)

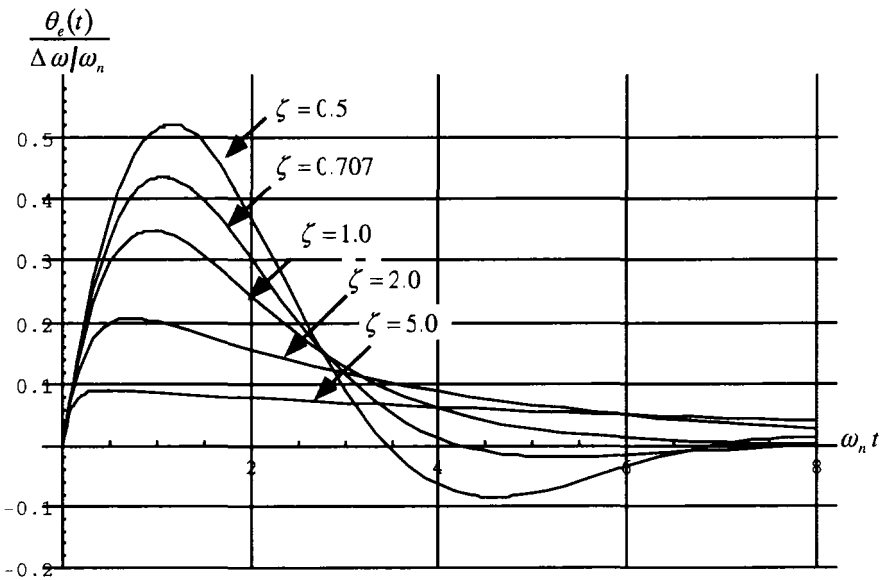


Figure 2.9 Frequency Step Response of Second Order Active Filter Loop

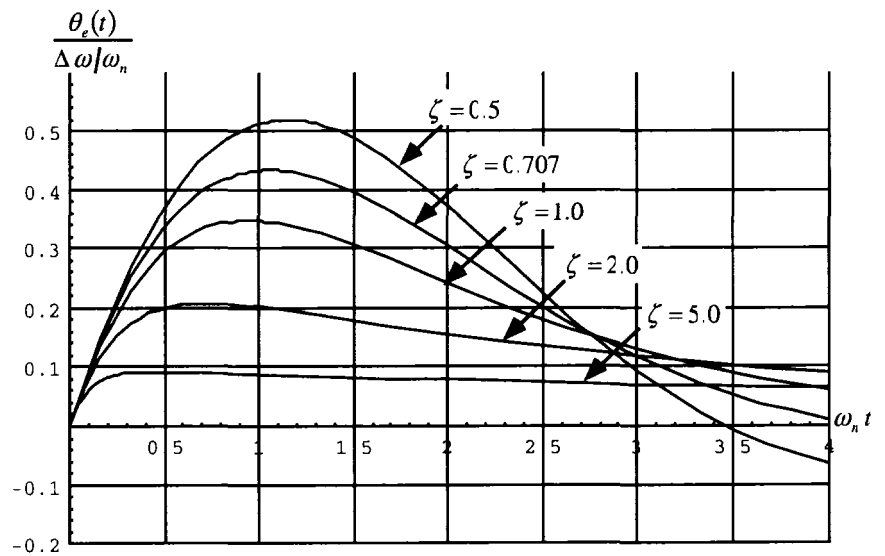


Figure 2.10 Frequency Step Response of Second Order Active Filter Loop (Magnified)

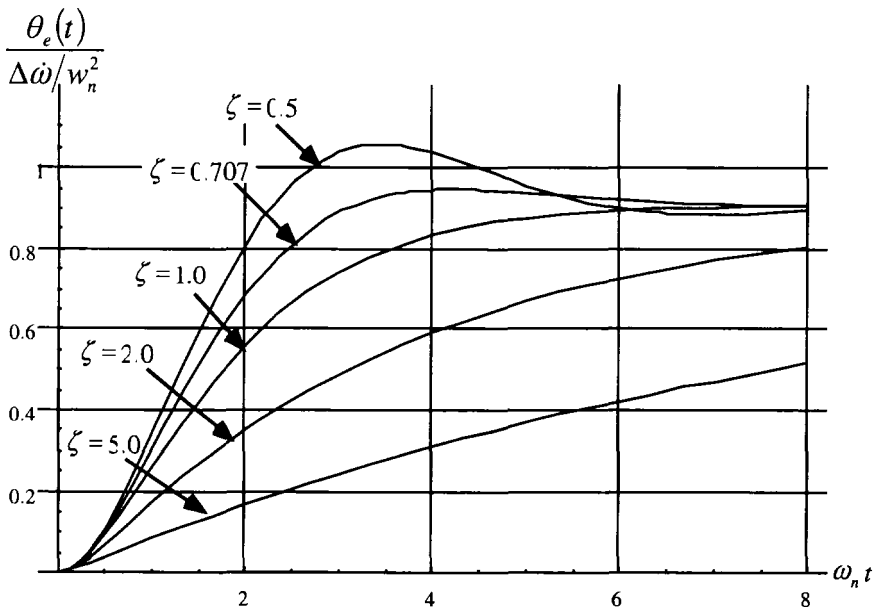


Figure 2.11 Frequency Ramp Response of Second Order Active Filter Loop

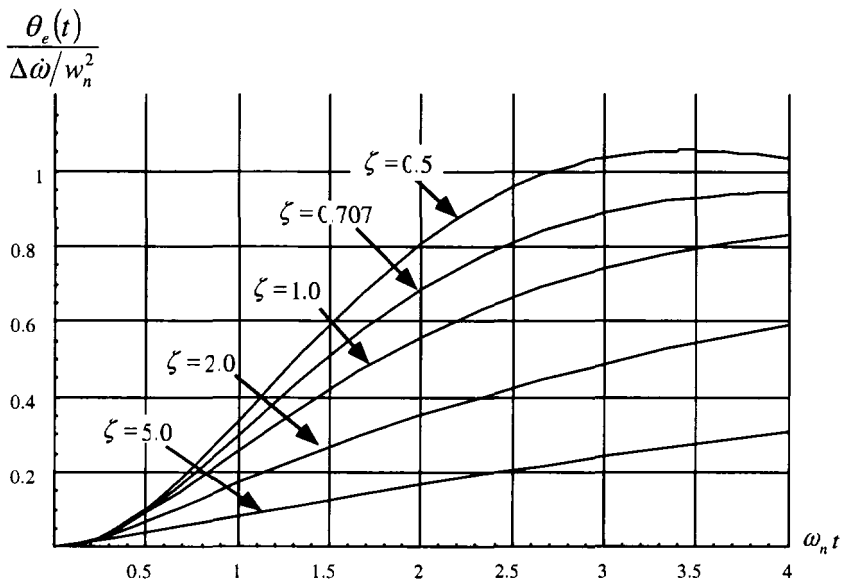


Figure 2.12 Frequency Ramp Response of Second Order Active Filter Loop (Magnified)

## *Example 2.2*

Design a PLL. Compute the necessary filter coefficients for an active second order filter with the following parameters and specifications:

VCO: $K_o$ = 10 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian, Input Power: 0 dBm (1mW), Natural Frequency (Specified) 3 Hz, Damping Factor (Specified) 0.707

To obtain the coefficients for our loop filter, we use Equation 2-74,

$$\tau_2 = \frac{2\zeta}{w_n} = \frac{2 \times 0.707}{3 \times 2 \times \pi} \qquad 2\text{-}90$$

$= 0.075015.$

To obtain the value of $\tau_1$, we substitute into Equation 2-73,

$$\tau_1 = \frac{\sqrt{2P}K_o K_d}{\omega_n^2} = \frac{\sqrt{2 \times 50 \times 10^{-3}}10 \times 2 \times \pi \times 0.5}{(3 \times 2 \times \pi)^2} \qquad 2\text{-}91$$

$= 0.0280$

It is important to note that our equations for $\tau_1$ and $\tau_2$ require all of the units to be in radians. Usually, PLL specifications are given in units of Hz, which requires a conversion to radians, as shown in Equations 2-90 and 2-91. Also note that $P = 10^{-3} \times 50$ because the units dBm imply a 50 ohm load resistance. The loop filter can now be written as

$$F(s) = \frac{1 + 0.075015s}{0.028\,s} \qquad 2\text{-}92$$

Using the closed loop transfer function for the second order active filter, Equation 2-67, we obtain

$$H_o(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} = \frac{2\times 0.707\times(3\times 2\times\pi)\times s + (3\times 2\times\pi)^2}{s^2 + 2\times 0.707\times(3\times 2\times\pi)\times s + (3\times 2\times\pi)^2}$$

$$= \frac{26.53s + 355.306}{s^2 + 26.53s + 355.306} \qquad 2\text{-}93$$

The error response is computed using Equation 2-68,

$$H_e(s) = \frac{\sqrt{2P}K_d s^2}{s^2 + 2\zeta w_n s + w_n^2} = \frac{\sqrt{2\times 50\times 10^{-3}}\times 0.5 s^2}{s^2 + 2\times 0.707\times(3\times 2\times\pi)\times s + (3\times 2\times\pi)^2} \qquad 2\text{-}94$$

$$= \frac{0.158114 s^2}{s^2 + 26.53 s + 355.306}$$

This analog loop will be used for comparison to the digital loops that we will derive later in the text. For completeness, the error response to a phase step input is shown in Figure 2.13. From the normalized plot of Figure 2.8, the peak undershoot should occur at $\omega_n t \approx 2.2$, or $t \approx 2.2/\omega_n$ . For this example, $\omega_n = 3\,Hz = 6\pi$ radians/sec, and then $t = \frac{2.2}{6\pi} = 0.117$. Note the agreement with Figure 2.13, which demonstrates how the graphs of Figures 2.7-2.12 are used in the design and analysis of phase-locked loops.

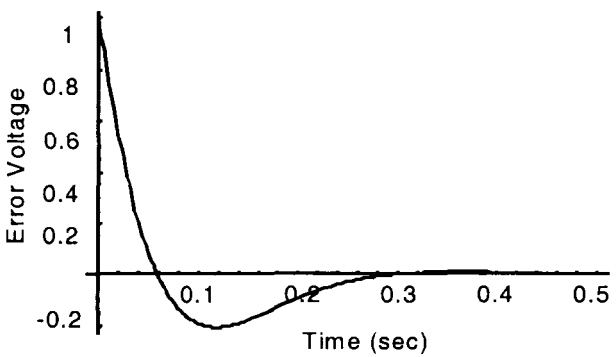


Figure 2.13 Example 2.1's Loop Response to a Phase Step

### 2.6.4 Time Response of the Second Order Loop With the Lowpass Filter

Using *Mathematica*™, we obtained the following time responses for Equation 2-62.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant.

$$\theta_e(t) = \left\{ \begin{array}{l} \sqrt{2P}\, K_d\, \Delta e^{-t\xi\omega_n} \left(\sqrt{\xi^2 - 1}\right) \\ \times Cosh\left(t\,\omega_n \sqrt{\xi^2 - 1}\right) + \xi\, Sinh\left(t\,\omega_n \sqrt{\xi^2 - 1}\right) \end{array} \right\} \Big/ \sqrt{\xi^2 - 1} \qquad 2\text{-}95$$

**Case II.** $\theta(t) = 2\pi f_\Delta t$

$$\theta_e(t) = \frac{1}{\omega_n \sqrt{\xi^2 - 1}} \left( \sqrt{2P}\, \pi\, e^{-t\omega_n\left(\xi + \sqrt{\xi^2 - 1}\right)} \right) \left( \begin{array}{l} -2\left(1 + e^{2t\omega_n\sqrt{\xi^2-1}} - 2e^{t\omega_n\left(\xi+\sqrt{\xi^2-1}\right)}\right) \\ \xi\sqrt{\xi^2 - 1} - \left(e^{2t\omega_n\sqrt{\xi^2-1}} - 1\right)\left(2\xi^2 - 1\right) K_d\, f_\Delta \end{array} \right) \qquad 2\text{-}96$$

**Case III.** $\theta(t) = 2\pi \dot{f} t^2$

$$\theta_e(t) = \frac{\sqrt{2P}\, 2\pi\, K_d\, \dot{f}}{\omega_n^2 \left(\xi + \sqrt{\xi^2 - 1}\right)^2} \left( \begin{array}{l} e^{-t\omega_n\left(\xi+\sqrt{\xi^2-1}\right)} \left(\sqrt{\xi^2 - 1} - \xi\right) \Big/ \sqrt{\xi^2 - 1} \\ + e^{t\omega_n\left(-\xi+\sqrt{\xi^2-1}\right)} \left(\xi + \sqrt{\xi^2 - 1}\right)^3 \\ \left(2\xi + \dfrac{2\xi^2 - 1}{\sqrt{\xi^2 - 1}}\right) + \dfrac{2 - 8\xi^2 + 4t\xi\omega_n}{\left(\xi - \sqrt{\xi^2 - 1}\right)^2} \end{array} \right) \qquad 2\text{-}97$$

### 2.6.5 Time Response of the Second Order Loop With the Passive Lead- Lag Filter

Using *Mathematica*™, we obtained the following time responses for Equation 2-68.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant.

$$\theta_e(t) = \frac{\Delta\omega_n \tau_1 e^{-t\xi\omega_n}\left(\begin{array}{l}\omega_n \tau_1 \sqrt{\xi^2-1}\, Cosh\left(t\omega_n\sqrt{\xi^2-1}\right) \\ +\left(1-\omega_n \tau_1 \xi\right) Sinh\left(t\omega_n\sqrt{\xi^2-1}\right)\end{array}\right)}{K_O\sqrt{\xi^2-1}} \qquad 2\text{-}98$$

**Case II.** $\theta(t) = 2\pi f_\Delta t$

$$\theta_e(t) = \frac{1}{K_O\sqrt{\xi^2-1}}\left(\begin{array}{l}\pi f_\Delta e^{-t\omega_n\left(\xi+\sqrt{\xi^2-1}\right)} \\ \left(\begin{array}{l}-\left(1+e^{2t\omega_n\sqrt{\xi^2-1}}-2e^{t\omega_n\left(\xi+\sqrt{\xi^2-1}\right)}\right)\sqrt{\xi^2-1} \\ -\left(e^{2t\omega_n\sqrt{\xi^2-1}}-1\right)\left(\xi-\tau_1\omega_n\right)\end{array}\right)\end{array}\right) \qquad 2\text{-}99$$

**Case III.** $\theta(t) = 2\pi \dot{f} t^2$

$$\theta_e(t) = \frac{2\pi\dot{f}}{K_O\omega_n}\left(\begin{array}{l}-4\xi+2\left(t+\tau_1\right)\omega_n+e^{t\omega_n\left(-\xi+\sqrt{\xi^2-1}\right)} \\ \left(2\xi+\dfrac{2\xi^2-1}{\sqrt{\xi^2-1}}\right)\left(1+\left(-\xi+\sqrt{\xi^2-1}\right)\tau_1\omega_n\right) \\ +\dfrac{e^{-t\omega_n\left(\xi+\sqrt{\xi^2-1}\right)}\left(-1+\left(\xi+\sqrt{\xi^2-1}\right)\tau_1\omega_n\right)}{\sqrt{\xi^2-1}\left(\xi+\sqrt{\xi^2-1}\right)^2}\end{array}\right) \qquad 2\text{-}100$$

## 2.7 Third Order Phase-Locked Loops

### 2.7.1 Reasons for Designing Third Order Loops

Third order phase-locked loops provide the desirable characteristic of being able to track an accelerating frequency input. In communications this occurs frequently when the receiver or transmitter is in motion. As an example, Figure 2.14 shows a satellite antenna on the mast of a ship. As the ship rolls with waves, the mast experiences a significant position displacement. The displacement is sufficient to generate a considerable frequency ramp. (32 Hz/sec is a common specification for UHF SATCOM receivers.)

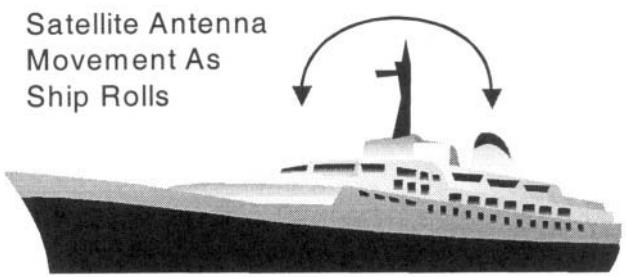


Figure 2.14 Doppler Induced by Ship Rolling at Sea

An important class of receivers for the Global Positioning System (GPS) have significant Doppler induced by the satellites moving with respect to the receiver [5]. The rate of frequency change is dependent upon the satellite's relative position to the receiver.

A non-Doppler reason for using 3rd order phase-locked loops is that the filter can be used to optimize the phase noise performance of the loop. The 3rd order loop has an additional degree of freedom available to the designer attempting to optimize the phase noise contributions of different sources in the phase-locked loop. This will be discussed in Chapter 12.

Yet another advantage of the third order filter is in phase-locked modulators for Continuous Phase Modulation (CPM) waveforms. For frequency waveforms more complex than REC, [10] the accelerated phase during a symbol interval will create tracking errors for second order phase-locked loops.

### 2.7.2 Third Order Loop Filters

With the additional degree of freedom in specifying the loop filter for the third order system, loop filters have a variety of configurations. Often, it is desirable to specify the closed loop response have the form of a Butterworth polynomial. Another possibility is the ITAE response [2]. Stability is a major concern for third order loops and analysis must be made of the inherent stability and possible degradation due to component tolerances or quantization. A third order loop with transfer functions of $\frac{K}{s^3}$, $\frac{K}{s^2(s\tau_1+1)}$, or $\frac{K(s\tau_a+1)}{s^3}$ is inherently unstable [2].

Gardner [11] suggests a loop filter of the form

$$F(s)=\frac{(s\tau_2+1)^2}{(s\tau_1)^2} \qquad 2\text{-}101$$

This filter will yield a third-order, type 3 loop. The filter's two poles at zero, along with the VCO's pole at zero, provides the loop with three perfect integrators. An advantage of Equation 2-84 is that it can be synthesized by cascading two second-order active filters. Substituting Equation 2-101 into the basic PLL equation of 2-48 yields

$$H_c(s)=\frac{\sqrt{2P}K_oK_d\frac{\tau_2^2}{\tau_1^2}\left(s^2+s\frac{2}{\tau_2}+\frac{1}{\tau_2^2}\right)}{s^3+\sqrt{2P}K_oK_d\frac{\tau_2^2}{\tau_1^2}\left(s^2+s\frac{2}{\tau_2}+\frac{1}{\tau_2^2}\right)} \qquad 2\text{-}102$$

Selection of $\tau_1$ and $\tau_2$ for a specific design is best accomplished by Root Locus design (presented in Chapter 3). This permits the closed loop poles to be placed in a stable position, and the magnitude of the real component will determine the damping of the closed loop response. The actual pole positions will be affected by the input signal gain, $\sqrt{2P}$. If the

instantaneous gains drops too much, then the resulting phase-locked loop is unstable.

The error response with a third-order, type 3 loop is

$$H_e(s) = \frac{\sqrt{2P}K_o K_d s^3 \tau_1^2}{s^3 \tau_1^2 + \sqrt{2P}K_o K_d (1 + s\tau_2)^2} \qquad 2\text{-}103$$

Przedpelski [13] suggests a third-order, type-2 filter than can be synthesized with only a single operation amplifier. The disadvantage is that it creates a type-2 loop contrasted with the type-3 generated with third-order, type-3 filter. Przedpelski's Laplace transform of the filter is

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s(\tau_3 s + 1)} \qquad 2\text{-}104$$

Substitution into the basic PLL equation provides

$$H_c(s) = \frac{\sqrt{2P}K_o K_d \tau_2 s + \sqrt{2P}K_o K_d}{\tau_1 \tau_3 s^3 + \tau_1 s^2 + \sqrt{2P}K_o K_d \tau_2 s + \sqrt{2P}K_o K_d} \qquad 2\text{-}105$$

The transfer function for the error response of this type-2 loop is

$$H_e(s) = \frac{\sqrt{2P}K_d \tau_1 \tau_3 s^3 + \sqrt{2P}K_d \tau_1 s^2}{\tau_1 \tau_3 s^3 + \tau_1 s^2 + \sqrt{2P}K_o K_d \tau_2 s + \sqrt{2P}K_o K_d} \qquad 2\text{-}106$$

The third order, type-3 and third order, type-2 filters are shown in Figure 2.15. These are implemented with operational amplifiers and are found in many actual applications. As noted previously, the third order type-3 is obtained by cascading two of the active filters used for second order loops.

Note that opening the connection to $C_2$ results in the active second order filter. This suggests that a switch can be placed in series with $C_2$, so that loop acquisition can be obtained with a second order configuration, and then

switching to a third order configuration after acquisition. Gardner [11] writes that switching in additional integrators can cause loss of phase-lock. The author's personal experience is that this technique can work, although each application is different.

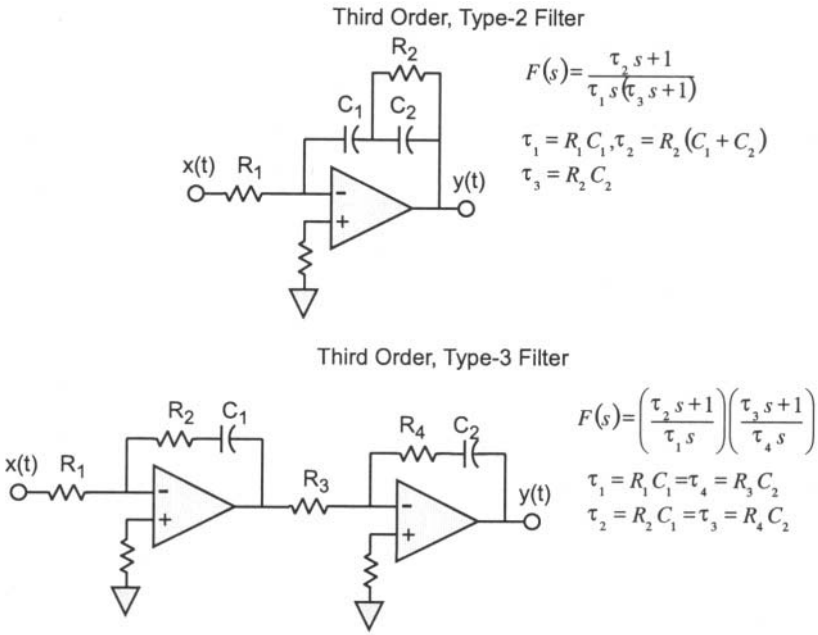


Figure 2.15 Typical Filters for Third-Order Loops

A different third-order loop response is suggested by Blinchikoff [14] which has no zeroes in the closed loop response. The filter is

$$F(s) = \frac{K_l}{s^2 + a_1 s + a_0} \qquad 2\text{-}107$$

This configuration yields a transfer function with a Butterworth closed loop response. Although this type of response is sometimes desirable for classical control applications, it finds limited applicability for phase-locked loops. The filter has no perfect integrators, and as a consequence, the resulting third-order loop is type-1. As will be discussed shortly, the cost of reducing a third-order loop to a type 2 or type 1 is significantly reduced Doppler tracking capability.

A filter for a type-3 loop can be composed from hypothesizing the filter needs a time response of the form $f(t) = c_0\delta(t) + c_1 + c_2 t$. The corresponding loop filter is of the form

$$F(s) = c_0 + \frac{c_1}{s} + \frac{c_2}{s^2} = \frac{c_2 + c_1 s + c_0 s^2}{s^2} \qquad 2\text{-}108$$

This filter is more applicable for digital filter transformations than used in analog phase-locked loop. Substitution of this loop filter into the basic PLL equation gives

$$H_o(s) = \frac{\sqrt{2P}K_o K_d\left(c_2 + c_1 s + c_0 s^2\right)}{s^3 + \sqrt{2P}K_o K_d\left(c_2 + c_1 s + c_0 s^2\right)} \qquad 2\text{-}109$$

The transfer function for the error response is

$$H_e(s) = \frac{\sqrt{2P}K_d s^3}{s^3 + \sqrt{2P}K_o K_d\left(c_2 + c_1 s + c_0 s^2\right)} \qquad 2\text{-}110$$

### 2.7.3 Filtering Reference Pulses

A sequential phase detector is used in most frequency synthesizers. (The sequential phase detector is discussed in Chapter 9.) Because the outputs from the phase detector are pulses, there is a significant amount of energy at the reference frequency applied to the loop filter. The phase-locked loop designer has to somehow remove these reference pulses or they will appear as undesired tones on the output of the frequency synthesizer.

Figure 2.16 shows a SIMULINK™ model of a frequency synthesizer. The synthesizer will phase-lock its output (the 500 kHz VCO) to the 100 kHz reference signal. Because the VCO's output frequency is not the same as the reference, a divide-by-five is used to apply 100 kHz frequencies to the phase detector.

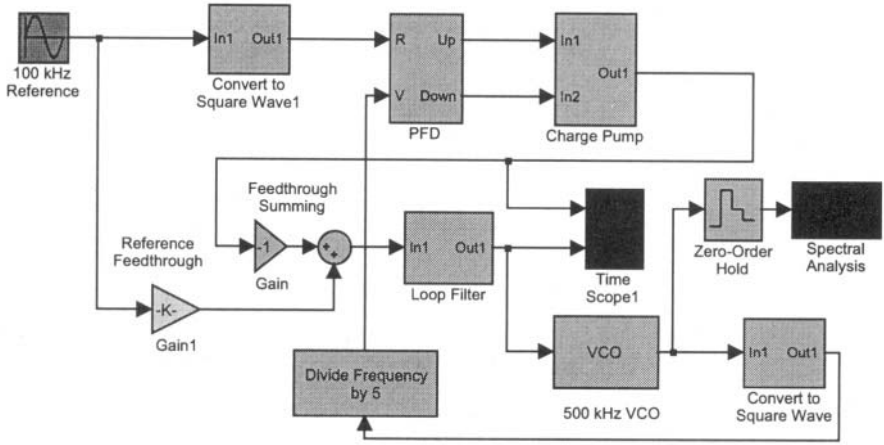


Figure 2.16 Model of a Frequency Synthesizer With Reference Feed-through

The phase detector in this example is not a mixer, but a sequential phase detector and charge pump. These two elements will be discussed later in Chapter 6, but they perform the basic phase detection of the mixers we have just discussed. The error voltage from the charge pump is applied to an analog loop filter which then corrects the VCO's output frequency and phase.

In the model, we have a reference feed-through path that represents parasitic coupling between the reference generator and the output of the charge pump. (This can occur because of power supply coupling or other mechanisms.) The reference feed-through will cause an undesired modulation of the output signal. Figure 2.17 shows the frequency synthesizer output without feed-through, whereas Figure 2.18 shows the synthesizer output with reference feed-through.

A common technique to reduce reference feed-through is the additional filter shown in Figure 2.19. This filter consists of a additional pole, and when cascaded with a second-order filter, yields a third-order loop.

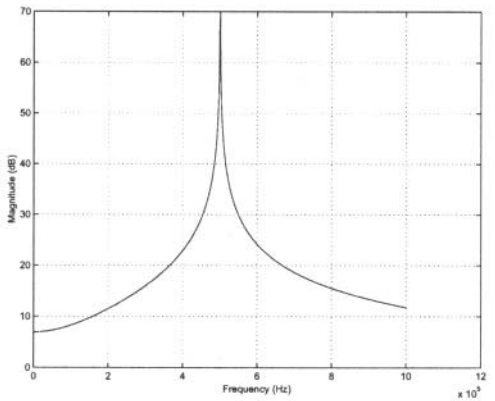


Figure 2.17 Frequency Synthesizer Spectrum Without Reference Feed-through

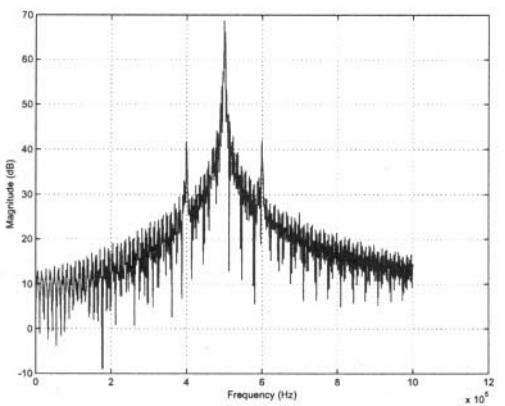


Figure 2.18 Frequency Synthesizer Spectrum With Reference Feed-through

The mathematical form of this loop is a lowpass function shown in Equation 2-111. (In a hardware implementation, the designer needs to be concerned with the impedance interactions between the reference rejection filter and the actual loop filter, but we neglect that in our considerations.)

$$F_r(s) = \frac{1}{1+\tau_3 s} \qquad 2\text{-}111$$

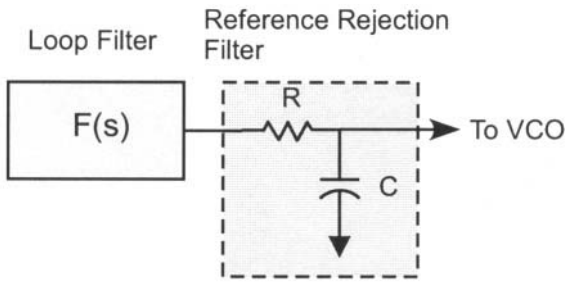


Figure 2.19 Reference Rejection Filter

As an example, suppose F(s) in Figure 2.16 is an active second order filter. Substitution of the filters into Equation 2-48 yields

$$H_{o,rr} = \frac{\sqrt{2P}\,K_d\,K_o\,\tau_2\,s + \sqrt{2P}\,K_d\,K_o}{\tau_1\,\tau_3\,s^3 + \tau_1\,s^2 + \sqrt{2P}\,K_d\,K_o\,\tau_2\,s + \sqrt{2P}\,K_d\,K_o} \qquad 2\text{-}112$$

$$H_{o,rr} = \frac{\tau_1\,\tau_3\sqrt{2P}\,K_d\,s^3 + \sqrt{2P}\,K_d\,\tau_1\,s^2}{\tau_1\,\tau_3\,s^3 + \tau_1\,s^2 + \sqrt{2P}\,K_d\,K_o\,\tau_2\,s + \sqrt{2P}\,K_d\,K_o} \qquad 2\text{-}113$$

A typical design approach for the reference rejection filter is to design a second order filter such that the highest pole frequency is a factor of ten lower than the reference rejection filter's pole [19].

### 2.7.4 Third Order Loop Responses

As with the second-order loops, we evaluate the response of the third-order loops to the different input stimuli. Of the five third-order loops just discussed, we will analyze only the type-2 and type-3 filters. The responses for the other loop filters are left as exercises.

**Case I.** $\theta(t) = \Delta\theta$, where $\Delta\theta$ is constant. The Laplace transform of this input is $\theta_i(s) = \Delta\theta/s$.

#### Third Order, Type-3

From Equations 2-52 and 2-102,

$$\theta_e(s) = \frac{\frac{\Delta\theta}{s}\sqrt{2P}K_d s^3}{s^3 + \sqrt{2P}K_o K_d s^2 + \frac{2\sqrt{2P}K_o K_d \tau_2 s}{\tau_1^2} + \frac{\sqrt{2P}K_o K_d}{\tau_1^2}} \qquad 2\text{-}114$$

The steady-state time response, obtained from the Final Value Theorem, is $\lim_{t\to\infty}\{\theta_e(t)\} = 0$. The time response is obtained from the inverse Laplace Transform of Equation 2-114, but is too lengthy to place in the text.

**Third Order, Type-2**

$$\theta_e(s) = \frac{\Delta\theta}{s}\frac{\sqrt{2P}K_d\tau_1\tau_3 s^3 + \sqrt{2P}K_d\tau_1 s^2}{\tau_1\tau_3 s^3 + \tau_1 s^2 + \sqrt{2P}K_o K_d \tau_2 s + \sqrt{2P}K_o K_d} \qquad 2\text{-}115$$

As with the type-3 filter, the steady-state time response is $\lim_{t\to\infty}\{\theta_e(t)\} = 0$. The inverse Laplace transform of Equation 2-115 yields the time response, but again, the time response is too long to place on the page.

**Case II.** $\theta(t) = 2\pi f_\Delta t$ The Laplace transform of $\theta(t)$ is $\theta_i(s) = 2\pi f_\Delta / s^2$.

**Third Order, Type-3**

$$\theta_e(s) = \frac{\frac{2\pi f_\Delta}{s^2}\sqrt{2P}K_d s^3}{s^3 + \sqrt{2P}K_o K_d s^2 + \frac{2\sqrt{2P}K_o K_d \tau_2 s}{\tau_1^2} + \frac{\sqrt{2P}K_o K_d}{\tau_1^2}} \qquad 2\text{-}116$$

The steady-state time response is $\lim_{t\to\infty}\{\theta_e(t)\} = 0$.

**Third Order, Type-2**

$$\theta_e(s) = \frac{2\pi f_\Delta}{s^2} \frac{\sqrt{2P}K_d\tau_1\tau_3 s^3 + \sqrt{2P}K_d\tau_1 s^2}{\tau_1\tau_3 s^3 + \tau_1 s^2 + \sqrt{2P}K_o K_d\tau_2 s + \sqrt{2P}K_o K_d} \qquad 2\text{-}117$$

The steady-state time response for this type-2 loop is $\underset{t\to\infty}{Lim}\{\theta_e(t)\} = 0$.

**Case III.** $\theta(t) = 2\pi\dot{f}t^2$ The Laplace transform is $\theta_i(s) = 2\frac{2\pi\dot{f}}{s^3}$.

**Third Order, Type-3**

$$\theta_e(s) = \frac{2\frac{2\pi\dot{f}}{s^3}\sqrt{2P}K_d s^3}{s^3 + \sqrt{2P}K_o K_d s^2 + \frac{2\sqrt{2P}K_o K_d\tau_2 s}{\tau_1^2} + \frac{\sqrt{2P}K_o K_d}{\tau_1^2}} \qquad 2\text{-}118$$

The steady-state time response of this type-3 loop is $\underset{t\to\infty}{Lim}\{\theta_e(t)\} = 0$.

**Third Order, Type-2**

$$\theta_e(s) = 2\frac{2\pi\dot{f}}{s^3} \frac{\sqrt{2P}K_d\tau_1\tau_3 s^3 + \sqrt{2P}K_d\tau_1 s^2}{\tau_1\tau_3 s^3 + \tau_1 s^2 + \sqrt{2P}K_o K_d\tau_2 s + \sqrt{2P}K_o K_d} \qquad 2\text{-}119$$

The steady-state time response for this type-2 loop is $\underset{t\to\infty}{Lim}\{\theta_e(t)\} = \frac{4\pi\dot{f}\tau_1}{K_o}$. Note the steady-state response is a function of the frequency ramp, which means the loop will not be able to maintain phase coherence if the input's frequency ramp is changing with time. In such conditions, this loop is unsuitable for coherent communications.

In subsequent chapters we will expand the analysis of phase-locked loops with these basic transfer functions.

## 2.8 References

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## 2.9 Problems

2.1 Solve $y'(t) = y(t) - a\,t$.

2.2 Solve $y'(t) = b\,y(t) - a\,t^2$.

2.3 Solve $y''(t) = y(t) - a$.

2.4 Solve $y''(t) = y'(t) - a\,y(t)$.

2.5 Find the inverse Laplace Transform for $F(s) = \left(\frac{1}{s+a}\right)\left(\frac{1}{s+b}\right)$.

2.6 Find the inverse Laplace Transform for $F(s) = \left(\frac{1}{s+a}\right)\left(\frac{s}{s+b}\right)$.

2.7 Find the Laplace Transform for $f(t) = at^2 \sin(2\pi f t)$.

2.8 For a first order phase-locked loop with:

VCO: $K_O$ = 100 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian
Input Power: P=0.01 W, Loop Filter $K_f = 0.1$
Input Phase Step = 1.0 Volts

Find how long it takes for the phase-locked loop error voltage to be less than 20 μVolts.

2.9 Power supply noise is often a problem for phase-locked loops. For the PLL of Problem 2.8, what is the error response of the phase-locked loop to a sinusoidal input of 30 mV at 60 Hz?

2.10 Derive the error response functions for the second order phase-locked loop with the passive loop filter.

2.11 For a second order active filter phase-locked loop with:

VCO: $K_O$ = 100 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian
Input Power: P=0.001 W, Damping Factor, $\zeta = 0.707$
Input Phase Step = 1.0 Volts

Design the loop filter so that the peak error response for a phase step input occurs at 50 ms. Graph the error response for the designed loop.

2.12 For a second order active filter phase-locked loop with:

VCO: $K_O$ = 100 kHz/Volt, Phase Detector: Kd = 1 Volt/Radian
Input Power: P=0.001 W, Damping Factor, $\zeta = 0.50$

Design the loop filter so that the steady-state error response for a frequency ramp with $\dot{f} = 200Hz$ is 12°.

2.13 For a second order active filter phase-locked loop with:

VCO: $K_O$ = 100 kHz/Volt, Phase Detector: Kd = 0.5 Volt/Radian
Input Power: P=0.01 W, Damping Factor, $\zeta = 1.0$
Design the loop filter so that the peak error occurs at 100 ms.

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# 3

# Root Locus and Frequency Analysis

In Chapter 2, we presented the basic configurations for phase-locked loops. We would like to present the performance and dynamics of phase-locked loops next, but at this point, we don't have enough theory to design the loops. Recall in Chapter 2, we mentioned terms such as damping factors, and with the third-order loop, unity gain crossover. So before we can discuss the true performance of phase-locked loops, we need to build expand the theoretical foundation.

## 3.1 Root Locus

In Chapter 2, we developed the transfer functions $H_o(s)$ and $H_e(s)$. $H_o(s)$ represents the transfer function for the output of the VCO. $H_e(s)$ is the transfer function relative to the output of the phase detector. These transfer functions permit us to write the outputs of the phase-locked loop as

$$\theta_o(s) = \theta_i(s) H_o(s) \qquad 3\text{-}1$$

Assuming the input $\theta_i(t)$, is bounded, $(|\theta_i(t)| < \infty)$, we are interested in knowing whether the output, $\theta_o(t)$, is also bounded. From linear systems

theory, a linear system is stable if and only if the integral of the absolute value of the impulse function is finite [1]. In other words,

$$\int_0^\infty |h(t)|\, dt < \infty \qquad 3\text{-}2$$

Recall the $H_O(s)$ for the second order, type-2 loop (the active filter configuration) is

$$H_o(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 3\text{-}3$$

The poles of a transfer function correspond to the roots of the denominator's polynomial equation. In other words, for Equation 3-3, the solutions for $s^2 + 2\zeta w_n s + w_n^2 = 0$. When the denominator has a value of zero, then the transfer function assumes an infinite value, thus the name "poles" for these roots. A transfer function's zero, is the complement to a pole and is a root of the numerator. For Equation 3-3, these are the solutions to $2\zeta w_n s + w_n^2 = 0$.

The poles for the two terms of Equation 3-3 can be obtained from the quadratic formula and are $s = -w_n\zeta \pm w_n\sqrt{\zeta^2 - 1}$. Algebraically, we see that if $\zeta < 1$, then the poles will be complex numbers, consisting of a real and imaginary component. There is a single zero for Equation 3-3, which is $s = -\frac{w_n}{2\zeta}$. These are depicted graphically in Figure 3.1. The pole locations are denoted with a "x", and the zero with a "0". The angle $\psi$ describes the damping factor, $\zeta$, and will be discussed shortly.

In Figure 3.1, there are two complex roots which mirror each other across the real axis. The vector length of these roots is $w_n$, called the loop natural frequency. The real and imaginary components of the roots are determined by both the natural frequency, and the damping factor, $\zeta$. If we had graphed the poles and zeros for the second order loop with the passive lead-lag filter, (Equation 2-37), the poles would be the same ("X"), but there would be no zero.

A partial fraction expansion takes an algebraically complex transform and places it in the form of $H_o(s) = \frac{A}{s+\alpha} + \frac{B}{s+\beta}$. After this expansion, we

can use Laplace Transform tables [2] to obtain the complete time-domain function. As an example, the partial fraction expansion of Equation 3-3 is

$$H_o(s) = \frac{1}{2w_n\sqrt{\zeta^2-1}}\left(\begin{array}{c}\dfrac{w_n^2 - 2w_n^2\zeta^2 + 2w_n^2\zeta\sqrt{\zeta^2-1}}{s + w_n\zeta - w_n\sqrt{\zeta^2-1}} \\ +\dfrac{-w_n^2 + 2w_n^2\zeta^2 + 2w_n^2\zeta\sqrt{\zeta^2-1}}{s + w_n\zeta + w_n\sqrt{\zeta^2-1}}\end{array}\right) \qquad 3\text{-}4$$

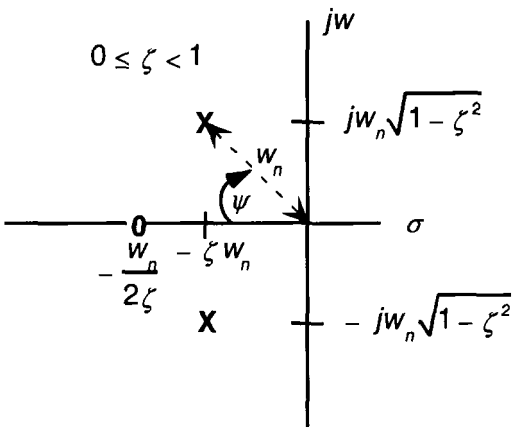


Figure 3.1 Graphical Representation of Symbols in Equation 3-3

Let's assume Equation 3-4 can be written as

$$H_o(s) = K\left(\frac{A_1}{s+\alpha+j\beta} + \frac{A_2}{s+\alpha-j\beta}\right) \qquad 3\text{-}5$$

A simple pole like $\dfrac{A_1}{s+\alpha+j\beta}$ has a time-domain equivalent of $A_1 e^{-(\alpha+j\beta)t}$. If the pole (root of $s+\alpha+j\beta=0$) has a positive real component, the exponential will increase with time, causing an unbounded response. The term $e^{-j\beta t}$ indicates the time response will be oscillatory, with the frequency established by the imaginary component of the pole, $\beta$.

We will show later that the time response and stability of a phase-locked loop are opposing values. A phase-locked loop with the damping factor $\zeta > 1$ is much more stable than a loop with $\zeta < 1$. Unfortunately, a loop with $\zeta > 1$ can be too sluggish (the loop takes too long to react to an input change) for some applications, and thus selection of $\zeta$ is a compromise between stability and time response.

The damping factor, $\zeta$, also has the graphical interpretation shown in Figure 3.1. $\psi$ corresponds to the angle of the pole relative to the real axis (when the damping factor $\zeta < 1.0$). The exact relationship is

$$\psi = \cos^{-1}(\zeta), \quad \zeta \leq 1 \qquad 3\text{-}6$$

As $\zeta$ decreases, the angle $\psi$ increases. This places the poles closer to the right-hand plane. The loop stability margin decreases with a decreasing damping factor.

A stable system must have a bounded response, so it is necessary for the real component of the poles to be negative, or to reside in the left-hand side of the s-plane. If the integral of h(t) is to be finite, we must have the real arguments of the exponentials as positive numbers. If they are negative, then h(t) is growing with time, which will not meet the criterion for a stable system.

In general, when evaluating the stability of a closed loop, we are interested in the denominator of the transfer function $H_o(s)$. The reader has probably already noted that $H_o(s)$ and $H_e(s)$ have the same denominator, which implies that the same stability test is true for both functions. Specifically, if the roots of the denominator (values of s for which the polynomial is zero) are in the left-hand s-plane, then the system is stable. If the roots are in the right-hand plane, then the system is unstable. A root on the *j w* axis yields a marginally stable system.

Equation 3-3 was obtained by substituting the loop filter's transfer function into Equation 2-27. Returning to this form, we can write the denominator of Equation 3-3 as

$$K\sqrt{2P}K_oK_d\frac{F(s)}{s} \qquad 3\text{-}7$$

The term in braces represents the forward gain of the phase-locked loop, beginning at the input to the phase detector, and ending with the VCO's output to the phase detector. Note the gain terms $\sqrt{2P}K_oK_d$ all affect the polynomial, which consequently changes the roots of the denominator. As noted previously, in a receiver, $\sqrt{2P}$ is often outside of the control of the designer or analyst, and can significantly change the response of the phase-locked loop.

A graphical display of the loop's sensitivity to gain changes is called a root locus plot. To generate a root locus plot, we introduce a gain scalar into Equation 3-7, as shown in Equation 3-8, and compute the pole and zero locations as the gain scalar, K, is varied.

$$1+K\left\{\sqrt{2P}K_oK_d\frac{F(s)}{s}\right\} \qquad 3\text{-}8$$

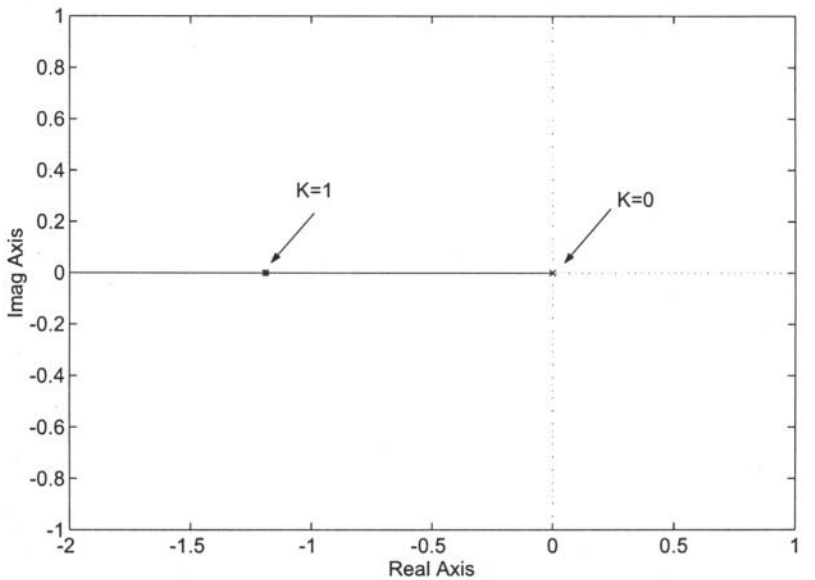


Figure 3.2 Root Locus Plot for First Order Phase-Locked Loop

K represents a scaling of the nominal gain of the phase-locked loop. If K<1, that implies the other gain terms of the loop are smaller than their

nominal or design values. Figure 3-2 shows the root locus plot of the first order phase-locked loop, corresponding to Equation 2-27. Regardless of the value of K, the first order loop is unconditionally stable. The single root of the denominator is always in the left-hand plane. In Figure 3.2, we have normalized the forward gain of the loop so that $\sqrt{2P}K_o K_d K_f = 1$. Likewise, we have normalized the forward gain and filter constants for Equation 2-37, $H_{0,lowpass}(s)$ and plotted the root locus for the second order loop with a passive filter in Figure 3.3. As shown in this root locus, the passive second order loop is also unconditionally stable.

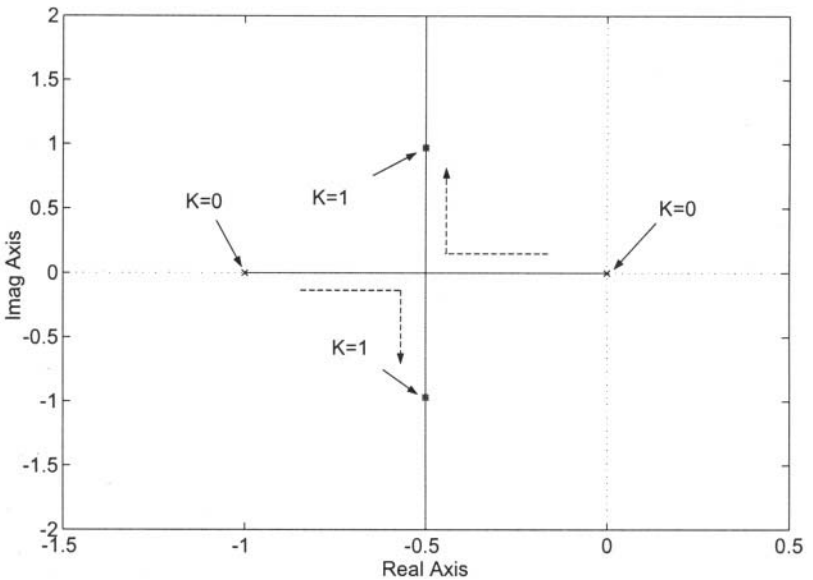


Figure 3.3 Root Locus for Second Order Loop With Passive Filter

Figure 3.4 shows the pole locations for the second order, type-2 phase-locked loop. At K=0, the two poles begin at s=0, and then follow the elliptical trajectory shown. At a specific value of K (K=3.4 in this example), the poles both become real, corresponding to $\zeta > 1$. Because the exponentials corresponding to Equation 3.5 have real components, the loop response will not exhibit any sinusoidal behavior. Instead, the loop will have a slowly decaying error response.

## 3.2 Propagation Delays in PLLs

Figure 3.4 is somewhat misleading, because even though the root locus shows the second order loop is unconditionally stable, physical implementations of the loop can be unstable. Generally, this is the result of time delays in the phase-locked loop implementation. The transform pair for a time delay, $t_d$, is $x(t-t_d) \leftrightarrow e^{-st_d} X(s)$.

Although $e^{-st_d}$ is the mathematically correct expression for a time delay in a continuous system, many of our analysis tools will fail for such a system because they are restricted to rational polynomials.

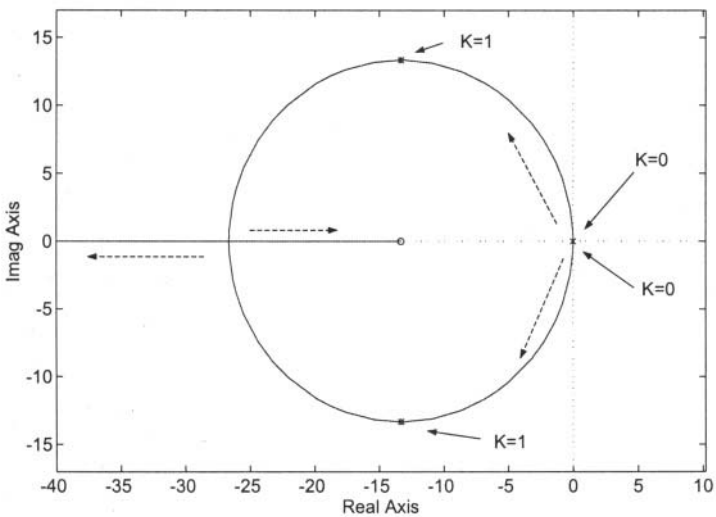


Figure 3.4 Root Locus for Second Order Loop With Active Filter

### 3.2.1 Representing Delays With a Lowpass Filter

A reasonable approximation is to model the time delay with a single pole Butterworth filter. The approximation is

$$D(s) = \frac{c}{s+c} \qquad \text{where } c = \frac{2.3}{t_d} \tag{3-9}$$

If $D(s)$ is placed in cascade with the forward transfer function of the second order loop, the block diagram of the phase-locked loop appears as shown in Figure 3.5. We note that Equation 3-9 is only an engineering approximation, but it allows us to perform analysis whereas otherwise it is an intractable problem.

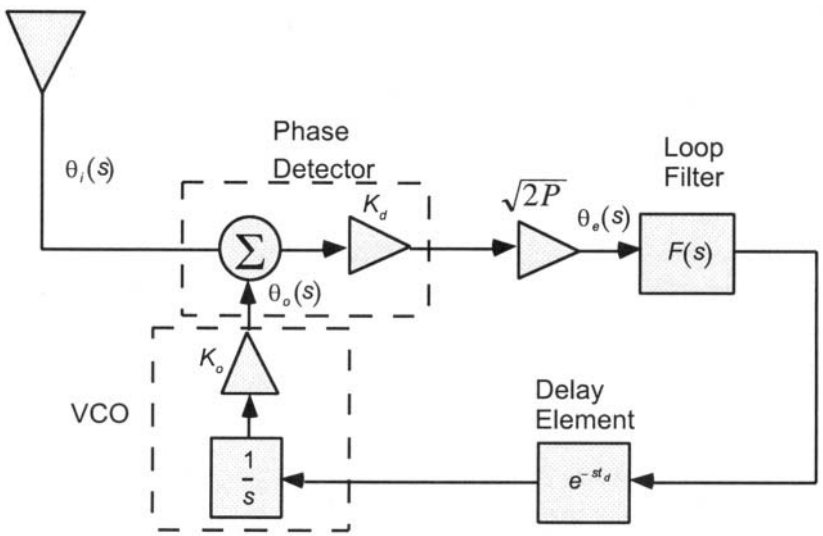


Figure 3.5 Phase-Locked Loop With Delay Element

### 3.2.2 Representing Time Delays With Pade's Approximation

A better approximation for $e^{-st_d}$ used in control systems is the Pade approximation. A two-term Pade approximation for the time delay is [10].

$$e^{-s\tau_d} \approx \frac{1-\tau_d s/2}{1+\tau_d s/2} \tag{3-10}$$

If the delay element of Equation 3-10 is included with the second order loop, the extra pole of $D(s)$ in the forward gain results in a third order loop.

### 3.2.3 Complications Due to Time Delays

Figure 3.6 shows the root locus of the same loop as in Figure 3.4, but with a delay element. The delay element now yields an marginally stable loop, which explains why otherwise well-designed second order loops can be unstable in real implementations. (Just a small gain increase causes this loop to become unstable as the poles migrate to the right-hand plane.)

The root locus plots for the two third-order filters discussed in Chapter 2 are shown in Figures 3.7 and 3.8. The actual appearance of the root locus is dependent upon the position of the poles and how close they are to each other.

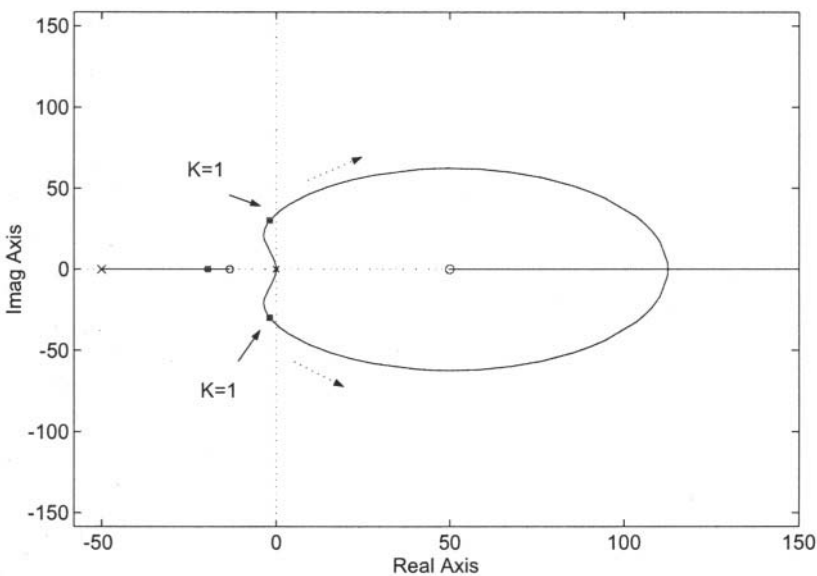


Figure 3.6 Second Order Root Locus With Time Delay

Unlike the second order loops, the third order loops are not inherently stable. The poles of the third order loops migrate significantly with the value of the loop gain. In particular, the third order loop type-3 filter is unstable at low values of gain. This is indicated by two of the roots at s={0,0}, moving

in the right hand plane before returning to the left hand plane and stability. For both filters, two of the roots are complex, and the third root has only a real component.

This possibility of instability with the third order loop is merely a nuisance for some applications such as modulators or synthesizers where the input level can be controlled. (Although algorithm or circuit start-up can be interesting.) For FM demodulators or bit synchronizers it can be disastrous, and can exhibit instability. As an example, suppose the automatic gain control does not respond to a drop in signal level. Because the signal level corresponds to the loop's gain, the phase-locked loop could become unstable as illustrated by Figure 3.7.

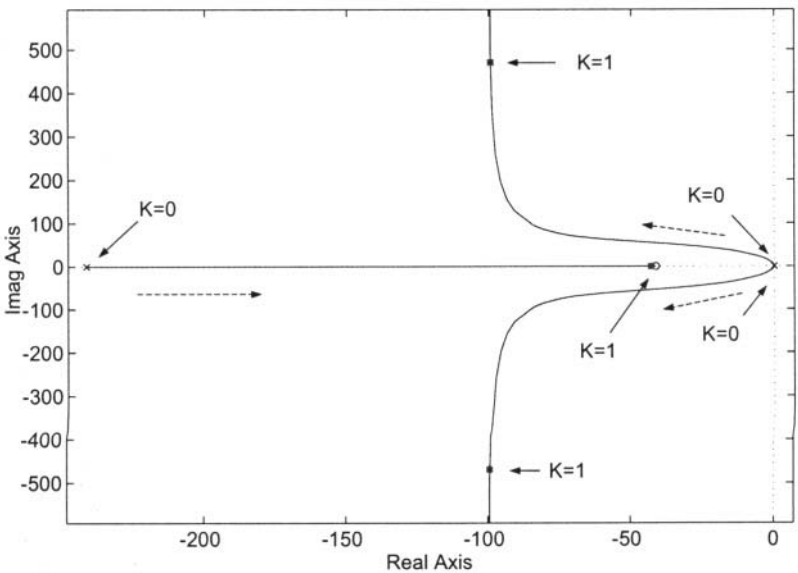


Figure 3.7 Root Locus of Third Order Loop Type-2 Filter

The design equations for the third order loop need to be deferred a little while later, until after we examine the frequency response of phase-locked loops. (We need some results from Bode Analysis in order to formulate the design equations.)

There are techniques for generating root locus plots [1]. The simple cases are easy to describe, but the special cases require lengthy discussion. To compute the root locus plots of the phase-locked loop, we recommend consulting Dorf [1], or utilizing a root locus plotting utility such as Mathematica's Signals and Systems Pack [3] or MATLAB's Control System Toolbox [11].

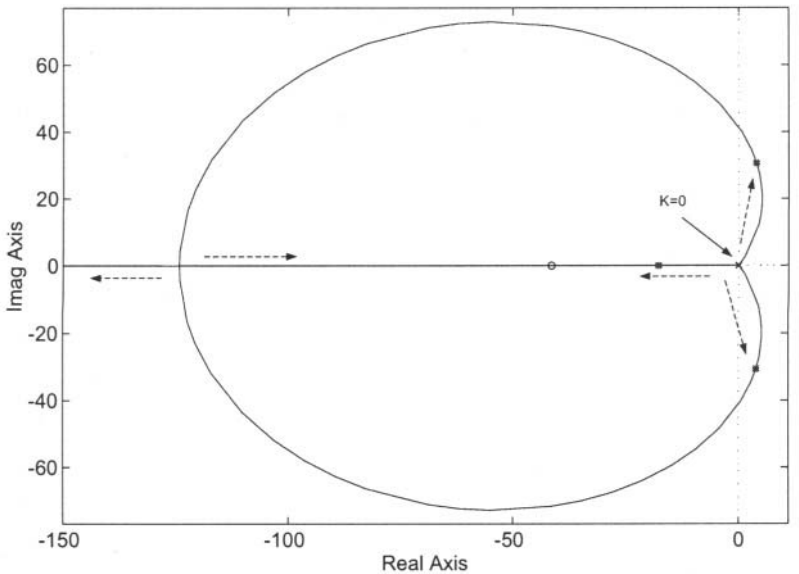


Figure 3.8 Root Locus of Third Order Loop Type-3 Filter

## *Example 3.1*

Plot the root locus for the second order phase-locked loop of Example 2.2.

If we add the multiplicative factor K, to the open loop gain for the active filter, second-order PLL, the symbolic representation of the closed loop transfer function is

$$H_o(s) = \frac{\sqrt{2P}KK_dK_o(1+\tau_2 s)}{\tau_1 s^2 + \sqrt{2P}KK_dK_o(1+\tau_2 s)} \qquad 3\text{-}11$$

Substituting the various loop components and filter coefficients from Example 2.2, we obtain

$$H_o(s) = \frac{9.93459K(1+0.075s)}{0.028s^2 + 9.93459K(1+0.075s)} \qquad 3\text{-}12$$

Using the MATLAB's sisotool, we plot the root locus of Equation 3-12 in Figure 3.9. For K just greater than zero, the transfer function of Equation 3-12 has complex poles, and then as the gain is increased to K=2.01, the poles become real. One pole goes to negative infinity, and the other pole goes to the zero at $s = -13.3$.

From a systems perspective, we can think of Figure 3.9 representing the roots of the phase-locked loop as either the signal, $\sqrt{2P}$ changes amplitude, or the loop coefficients change due to component tolerances. This design is unconditionally stable (assuming there are no other delays or filtering). It is counter-intuitive that as the signal level increases, the loop response could become sluggish due to the poles becoming real.

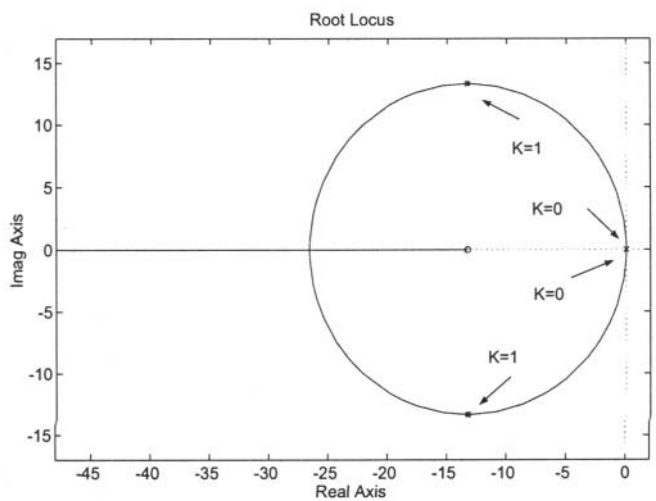


Figure 3.9 Root Locus of Example 3.1

## 3.3 Frequency Analysis

Frequency domain analysis also provides insight to the stability of phase-locked loops. (The Laplace transform with $s = jw$, is actually a frequency domain analysis.) Although a computer doesn't particularly care whether it computes a root locus or Bode analysis, the latter has some advantages.

Laboratory data is typically measured in the frequency domain and if the design analysis was done in the frequency domain, it aids comparisons between theoretical and actual performance. Bode analysis also permits accurate modeling of time delays. Recall with the root locus analysis, the $e^{-st_d}$ term produced by the pure time delay presents problems in finding the roots of the characteristic equation. To work around this problem, we approximated the delay with a lowpass filter. Bode analysis, however, allows us to exactly represent the time delay.

The closed loop equation for the phase-locked loop is

$$H_o(s) = \frac{\sqrt{2P}K_oK_dF(s)/s}{1+\sqrt{2P}K_oK_dF(s)/s} \qquad 3\text{-}13$$

A singularity (infinite value) of Equation 3-13 occurs when the characteristic equation, $1+\sqrt{2P}K_oK_dF(s)/s=0$. To satisfy this condition,

$$\left|\sqrt{2P}K_oK_dF(s)/s\right| = 1 \qquad 3\text{-}14$$

$$Arg\left|\sqrt{2P}K_oK_dF(s)/s\right| = 180° \qquad 3\text{-}15$$

These two equations define the stability of the phase-locked loop. Note that with Equations 3-14 and 3-15, we need only evaluate the open loop gain, $\sqrt{2P}K_oK_dF(s)/s$ for the stability boundary conditions above. This implies we can graph the magnitude and phase response of the open loop gain and determine whether the phase-locked loop is stable. For stability, the magnitude of the open loop gain should be less than unity when the phase of the open loop gain is 180°.

Figure 3.10 is a linearized Bode plot of the second order phase-locked loop from Example 2.2. The open loop gain for this example is

$$\sqrt{2P}K_o K_d \frac{F(s)}{s} = 9.94\frac{0.075\,s+1}{0.028\,s^2} \qquad 3\text{-}16$$

The important radian frequency of Figure 3.10 is at $w = 29.3$, where the open loop gain is unity. The phase angle at w=29.3 is $\theta = -114.5°$. The difference between $-114.5°$ and $-180°$ provides a measure of the loop's stability. We define the phase margin as

$$\text{Phase Margin} = 180° - \text{Arg}\left[\sqrt{2P}K_o K_d \frac{F(jw)}{jw}\right]_{w=\text{unity gain}} \qquad 3\text{-}17$$

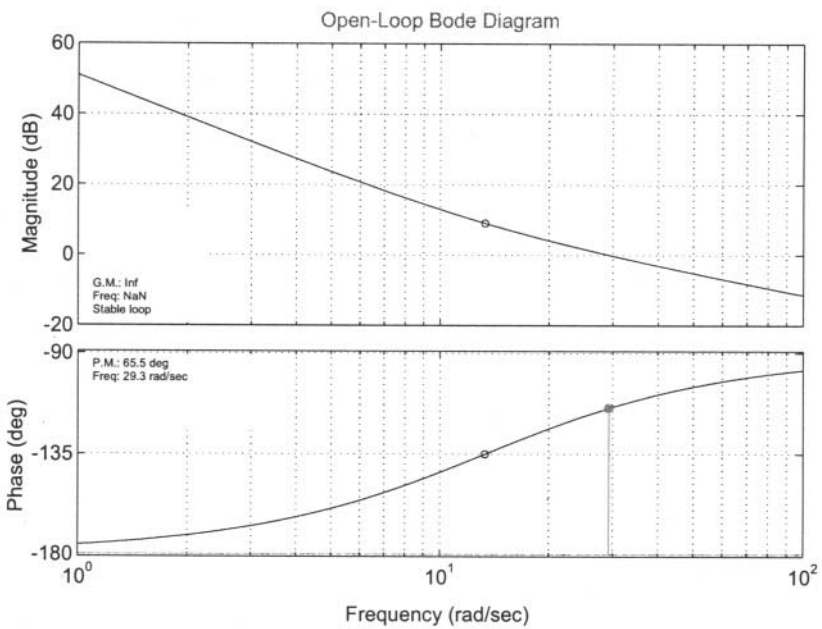


Figure 3.10 Bode Plot

In Figure 3.10, using Equation 3-17, the phase margin is 65.5°, and shown as the difference between the actual phase angle at unity gain, and the $-180°$ axis. A gain margin is the corresponding measure of gain stability when the phase angle is 180°. Although Figure 3.10 does not have a defined gain margin, we define it as the actual open loop gain (in dB) when the phase angle is 180°.

$$\text{Gain Margin} = -20\text{Log}\left[\sqrt{2P}K_o K_d \frac{F(jw)}{jw}\right]_{w=180^\circ \text{ phase angle}} (dB) \qquad 3\text{-}18$$

The general form for the open loop gain is [1]

$$G(jw) = \frac{K_b \prod_{i=1}^{Q}(1 + jw\tau_i)}{(jw)^N \prod_{m=1}^{M}(1 + jw\tau_m) \prod_{k=1}^{R}\left(1 + \frac{2\zeta_k}{w_{nk}} jw - \left(\frac{w}{w_{nk}}\right)^2\right)} \qquad 3\text{-}19$$

The numerator has Q real roots, corresponding to the zeros of the transfer function. The denominator has N perfect integrators, M real roots corresponding to the real roots and R complex pairs of roots, which are pole pairs. The significance of the log function in Equation 3-19, is that we can replace the product terms in Equation 3-18 with summations as [1]

$$20Log[G(jw)] = 20Log[|K_b|] + \sum_{i=1}^{Q} 20Log\ |1 + jw\tau_i| - 20N\,Log[|jw|]$$
$$- \sum_{m=1}^{M} 20Log\ |1 + jw\tau_m| - \sum_{k=1}^{R} 20Log\ \left|1 + \frac{2\zeta_k}{w_{nk}} jw - \left(\frac{w}{w_{nk}}\right)^2\right| \qquad 3\text{-}20$$

Similarly, we can write the phase response as a sum of the individual terms of Equation 3-17,

$$\phi(w) = \sum_{i=1}^{Q} \tan^{-1}[w\tau_i] - N \cdot 90^\circ - \sum_{m=1}^{M} \tan^{-1}[w\tau_m]$$
$$- \sum_{k=1}^{R} \tan^{-1}\left[\frac{2\zeta_k w_{nk} w}{w_{nk}^2 - w^2}\right] \qquad 3\text{-}21$$

The simplicity of Equations 3-20 and 3-21 allows an easy calculation of the gain and phase margins for the phase-locked loop. An exact Bode plot can be generated with computer analysis, but a graphical approximation of the two equations provides insight to the loop performance.

## *Example 3.2*

Suppose we have a third order phase-locked loop with Przedpelski 's filter, yielding an open loop gain of

$$G(s) = \sqrt{2P}K_o K_d \frac{\tau_2 s + 1}{\tau_1 s^2(\tau_3 s + 1)} \qquad 3\text{-}22$$

The specific equation for this example is

$$G(s) = \sqrt{2P}\, K_o K_d \frac{1s + 1}{s^2(100s + 1)} \qquad 3\text{-}23$$

We write the open loop gain in the form of Equations 3-20 and 3-21.

$$20Log|G(jw)| = 20Log\left|\frac{\sqrt{2P}K_o K_d}{\tau_1}\right| + 20Log\ |1 + jw\tau_2| \qquad 3\text{-}24$$
$$-40Log[|jw|] - 20Log\ |1 + jw\tau_3|$$

$$\phi(w) = \tan^{-1}[w\tau_2] - 180° - \tan^{-1}[w\tau_3] \qquad 3\text{-}25$$

The graphical approximation to Equations 3-24 and 3-25 are shown in Figure 3.11. The magnitude of the open loop gain is first plotted at a frequency such as w=0.1. (Because of the perfect integrators, the gain at 0 Hz is infinite.} From 0 Hz, the loop gain is decreasing by $\frac{20 \bullet N \text{ dB}}{\text{decade}}$. In this example, there are two perfect integrators, which cause the 40 dB per decade decrease in gain from 0 Hz. (Decade refers to a factor of 10 in frequency. 0.1 rad/sec to 1 rad/sec corresponds to 1 decade.) The $\tau_2 s + 1$ factor in the numerator, corresponding to the filter's zero, has a break frequency corresponding to $\tau_2 = 1$ rad/sec.

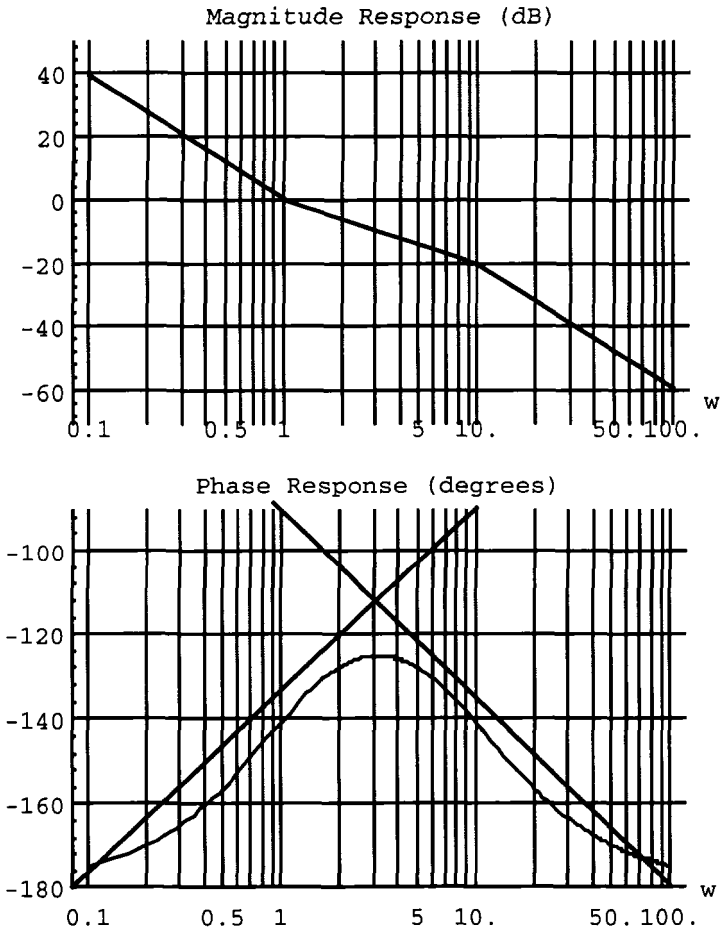


Figure 3.11 Linearized approximation to Exact Bode Analysis

The simple zero (as compared to a complex pair) results in a positive gain of 20 dB/decade, beginning at $\tau_2 = 1$ rad/sec. Because of the summation indicated in Equation 3-24, the net gain is a $-20\ \text{dB/decade}$, obtained from summing the gain of the perfect integrators and the filter's zero.

At $\tau_1 = 100$ rad/sec, the simple pole begins influencing the open loop gain with a factor of $-20\ \text{dB/decade}$. The net gain from this frequency forward, is then, $-40\ \text{dB/decade}$.

The phase response is slightly more difficult, because the zeros and poles begin affecting the phase much before significantly impacting the gain. A linearized rule is the simple pole or zero will change the phase by 90 degrees, beginning at 0.1 × breakpoint frequency and ending at 10 × breakpoint frequency.

In this example, the two perfect integrators have a phase angle of – 180° at 0 Hz. The zero corresponding to $\tau_2 = 1$ rad/sec will begin changing the phase at $+45°/\text{decade}$ at $w = 0.1$ rad/sec . The phase change due to the zero will complete at w=10 rad/sec. The non-zero pole of Equation 3-22 will decrease the phase at $-45°/\text{decade}$, beginning at $w = 10$ rad/sec , completing at $w = 1000$ rad/sec .

In this example, we did not consider a filter with complex poles or zeros. Typical phase-locked loops will not utilize such filters, but techniques are available for approximating the Bode plot with these filters [1].

Frequently in phase-locked loop design, we encounter time delays within the loop components. Often the time delays are associated with discrete-time components such as sample-and-holds, digital dividers, or sequential phase detectors which we will discuss in later chapters. In analog loops, there are still pure time delays due to propagation through filters or amplifiers.

## *Example 3.3*

Consider the phase-locked loop of Figure 3.12. The time delay is $t_d = 20ms$. Assuming all of the design parameters from Example 2.2, compute the gain and phase margins of the phase-locked loop.

We modify Equation 2-60 which expressed the open loop gain of the Example 2.2's phase-locked loop to include the time delay element.

$$H_{OL}(s) = \frac{\sqrt{2\times10^{-3}\times50}}{1}\left(\frac{2\pi 10\,rad}{sV\times\sec}\right)\left(\frac{\frac{1}{2}V}{1}\right)\left(\frac{0.075s+1}{0.028s}\right)e^{-s\left(20\times10^{-3}\right)} \qquad 3\text{-}26$$

We simplify this to the form

$$H_{OL}(s) = 9.94\frac{0.075s+1}{0.028s^2}e^{-s(20\times10^{-3})} \qquad 3\text{-}27$$

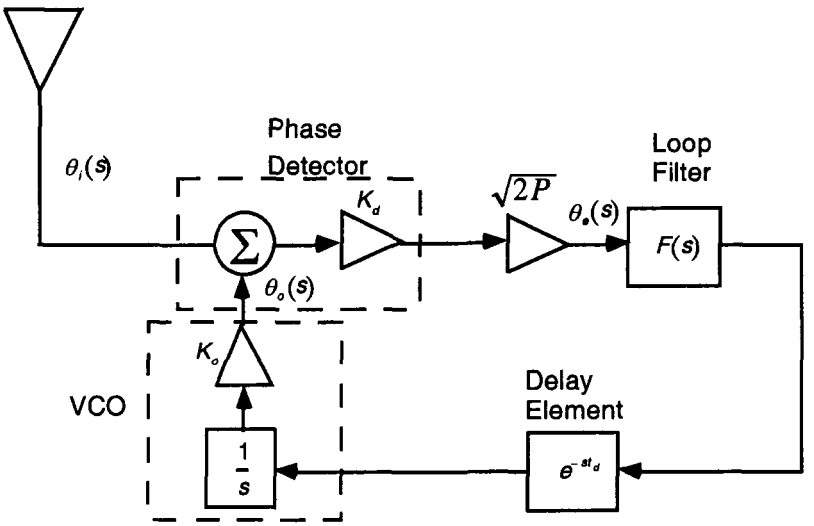


Figure 3.12 Phase-Locked loop With Pure Time Delay

This is similar to Example 3.1, with the exception of the exponential delay. This exponential factor has a magnitude, $\left|e^{-s(20\times10^{-3})}\right| = 1$. The phase angle can be written as $\phi(w) = -wt_d$, where $t_d = 20ms$. The Bode analysis can be performed exactly, or Equations 3-24 and 3-25 can be used with approximations shown in Example 3.2. Figure 3.13 shows the exact Bode Plot. The time delay has significantly reduced the phase margin of the phase-locked loop and it is now $\approx 30°$. The gain margin of 8 dB can be obtained from Figure 3.13.

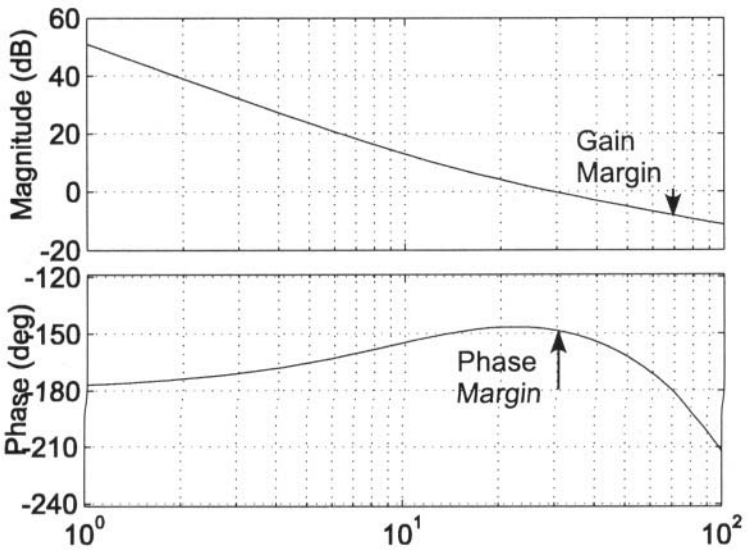


Figure 3.13 Second Order Loop With Time Delay

## 3.4 FM Demodulator

For many phase-locked loops, the concept of signal-to-noise is fictitious, because there is nowhere to measure the signal-to-noise. As such, it can become difficult to define the noise bandwidth of the PLL. Figure 3.14 shows a PLL used as an FM demodulator. We assume in Figure 3.14 that the PLL is tracking the FM signal [4] and the output of the loop constitutes the analog message.

Since we assume that the PLL is tracking the FM input, this implies that $\theta_o = \theta_i$. The FM modulated signal contains information in the derivative of $\theta_i$, or $\frac{d\theta_i}{dt}$. Neglecting the output amplifier with gain G, $\theta_m(s)$ represents the demodulated output.

$$\frac{\theta_m(s)}{\theta_i(s)} = \frac{s\sqrt{2P}K_d F(s)}{s + \sqrt{2P}K_d K_o F(s)} \qquad 3\text{-}28$$

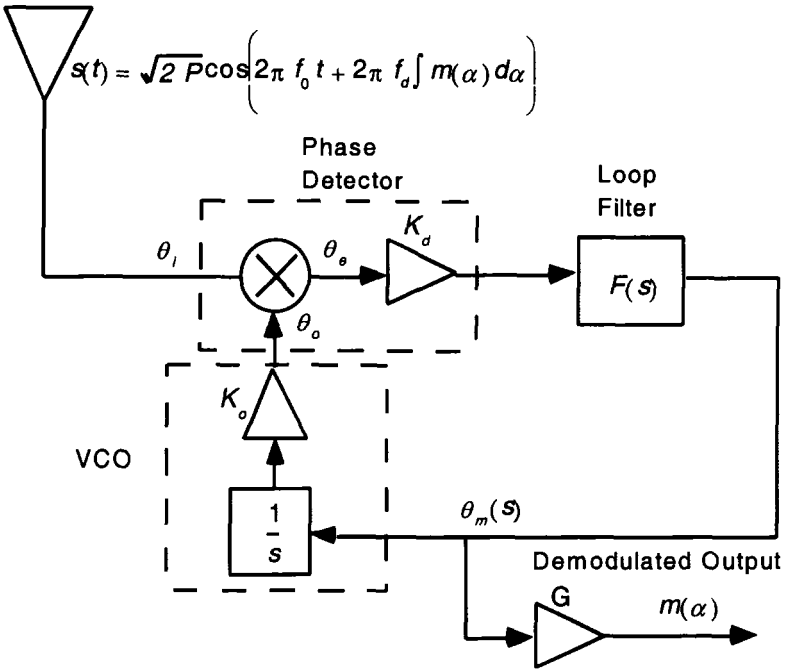


Figure 3.14 Phase-Locked Loop Used as FM Demodulator

The transfer function for Equation 3-28 includes a factor of s in the numerator because the demodulator's output is prior to the $\frac{K_o}{s}$ representing the VCO. Because of the Laplace Transform pair, $s \leftrightarrow \frac{d}{dt}$, the transfer function of Equation 3-28 can be considered as a differentiator for the input, $\theta_i(t)$ [7]. For FM modulation of the signal m(t), $m(t) = \frac{d\theta_i(t)}{dt} \leftrightarrow M(s) = s\theta_i(s)$ which we can substitute into Equation 3-28. This yields

$$\theta_m(s) = \frac{M(s)}{s} \frac{s\sqrt{2P}K_d F(s)}{s + \sqrt{2P}K_d K_o F(s)} \qquad 3\text{-}29$$

$$\theta_m(s) = M(s)\frac{H_o(s)}{K_o} \qquad 3\text{-}30$$

The final result of Equation 3-29 is from recognizing the form of the transfer function that was originally developed for the PLL of Figure 2.4. (See Equation 2-23.) The result for $\theta_m(s)$ in Equation 3-30 implies that the input message m(t), can be recovered by the PLL demodulator. The only requirement is that the message have a bandwidth much less than the bandwidth of the PLL's $H_o(s)$.

In Equation 3-30, the output of the demodulator is a function of the VCO's tuning gain, $K_o$ [7]. Usually with most hardware VCOs, the tuning element is a voltage-controlled capacitor which results in a nonlinear tuning characteristic as a function of frequency. In such a situation, the VCO's $K_o$ transducer gain will produce distortion in the output.

The closed loop frequency response $H_o(s)$ for Example 2.2 is shown in Figure 3.15. (This frequency response is graphed similar to the Bode Plots previously discussed, but Figure 3.15 is the *closed* loop response instead of the open loop response used for Bode analysis.)

Note the "peaking" that occurs in the frequency response just beyond 10 rad/sec. This is typical of a PLL's closed loop frequency response, and can present problems when attempting to meet phase noise specifications that will be discussed in Chapter 12. If the message m(t) has an information bandwidth less than 10 rad/sec, then the phase-locked loop will perform well as an FM demodulator.

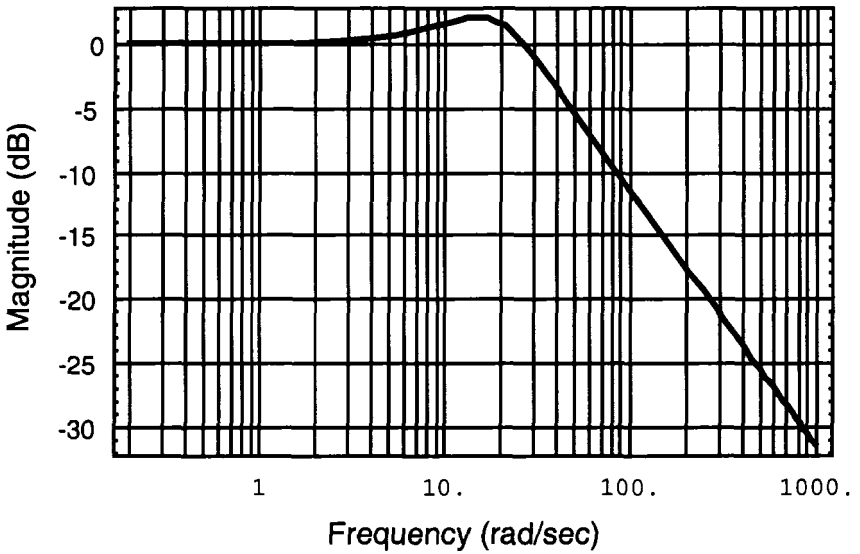


Figure 3.15 Closed Loop Frequency Response for Example 2.2

The closed loop frequency response $H_o(s)$, of Equation 3-30, represents how well the VCO is tracking the input $\theta_i(s)$. When the ratio is unity, there is zero error in the loop's output. This shows that we can indeed think of a PLL as having a signal, so the concept of signal-to-noise for the PLL is valid.

In digital communication, phase-locked loops are often used as demodulators for Frequency Shift Keying (FSK) or Continuous Phase Frequency Shift Keying (CPFSK) signals. Instead of allowing discontinuous phase transitions as in FSK, CPFSK requires all phase transitions to be continuous. This has the advantage of reducing the out-of-band spectral power for CPFSK modulation [8].

A transmitted FSK signal can be written as [9]

$$s(t;\overline{\alpha}) = \sqrt{\frac{2E_s}{T_s}} Cos[2\pi \quad f_0 \quad t + \varphi(t;\overline{\alpha}) + \varphi_0] \qquad 3\text{-}31$$

$$\dot{\varphi}(t;\overline{\alpha}) = 2\pi\Delta f \sum_{k=-\infty}^{\infty} \alpha_k \, p(t - kT_s) \qquad 3\text{-}32$$

$E_s$ is the symbol energy

$T_s$ is the symbol period

$\Delta f$ is the single - sided frequency deviation

$\overline{\alpha} = (\ldots, \alpha_{-2}, \alpha_{-1}, \alpha_0, \alpha_1, \alpha_2)$ is a specific data sequence

p(t) is a frequency pulse - shape function

As Equation 3-32 shows, a binary FSK signal consists of instantaneous frequency tones at $f_0 + \Delta f$ or $f_0 - \Delta f$, depending on whether the binary data symbol is +1 or -1. Prior to the development of phase-locked loops, the traditional receiver consisted of two matched filters followed by envelope detectors [4]. An alternative receiver uses a phase-locked loop that can quickly acquire the instantaneous frequency, whether it is $f_0 + \Delta f$ or $f_0 - \Delta f$. Every $T_s$ seconds it will have to quickly de-acquire (drop lock) and then re-acquire (phase-lock) the transmitted frequency which indicates what binary symbol was transmitted.

To demodulate the FSK or CFSK signal, a demodulator using a phase-locked loop is shown in Figure 3.16. This particular implementation assumes that the frequency pulse p(t) is a rectangular frequency pulse; otherwise a correlation against the transmitted pulse shape p(t) is required. (Pulse shaping is frequently used to reduce out-of-band spectral components.)

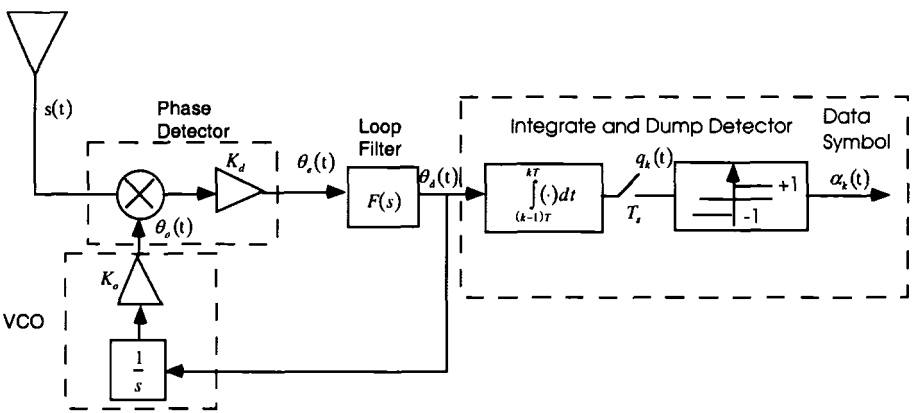


Figure 3.16 Phase-Locked Loop Demodulator for FSK [9]

To analyze the FSK demodulator in Figure 3.16, we assume a first order phase-locked loop that has already acquired the previous transmitted symbol. Because the first order loop has a steady-state error to a frequency step, the integrate-and-dump detector will have a steady state voltage applied to it

from the phase-locked loop. The linearized phase-locked loop in Figure 3.17 has a scalar loop filter gain, $K_f$, corresponding to the first order loop.

We assume that the FSK binary modulation in Equation 3-31 corresponds to $\pm\Delta f$ frequency steps. Note that when successive symbol values do not change, then the transmitted frequency will not change. In this case, the loop will not have to acquire a new frequency because it continues to track the continuously transmitted frequency. As discussed in Chapter 2, the first order loop will have a steady-state error to the frequency step, resulting in

$$\theta_{e\ \text{steady state}}(t) = \frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o} \qquad 3\text{-}33$$

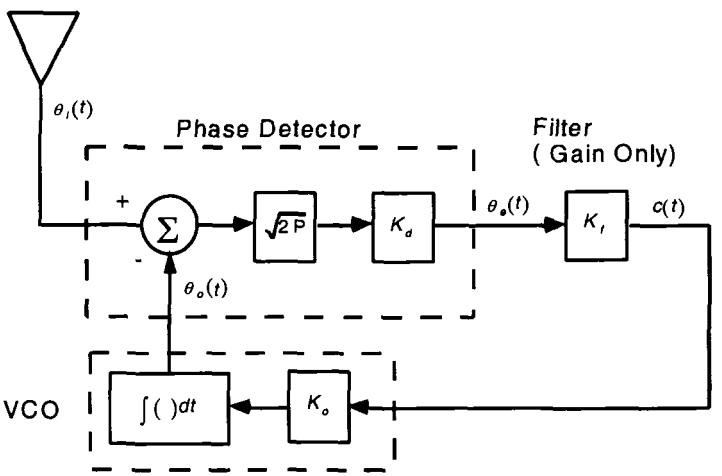


Figure 3.17 Linearized First Order Phase-Locked Loop for the FSK Demodulator

Equation 3-33 represents an initial condition that must be included in the transfer function for Figure 3.17. To develop the transfer function, the differential equation for the loop is first written as

$$\theta_e(t) = \theta_i(t) - \sqrt{2P}K_d K_f K_o \int \theta_e(t)dt \qquad 3\text{-}34$$

We differentiate this loop equation, to remove the unwieldy integral,

$$\theta_e'(t) + \sqrt{2P}K_d K_f K_o \theta_e(t) = \theta_i'(t) \qquad 3\text{-}35$$

To solve this differential equation, we will use the Laplace transform, but the initial conditions must first be included. Recall the Laplace transform pair, $\frac{d}{dt}f(t) \leftrightarrow sF(s) - f(0)$, which includes the initial conditions in the transfer function. Using this transform pair, the first order phase-locked loop equation is written as

$$s\theta_e(s) - \theta_e(t=0) + \sqrt{2P}K_d K_f K_o \theta_e(s) = s\theta_i(s) - \theta_i(t=0) \qquad 3\text{-}36$$

For this analysis, we assume the previously transmitted symbol corresponded to a $+\Delta f$ frequency step, and the current symbol has a $-\Delta f$ frequency step. With these assumptions for the previous and current symbols, $\theta_e(t=0) = 2\pi\Delta f / \sqrt{2P}K_d K_f K_o$ and $\theta_i(s) = -2\pi\Delta f / s^2$. The initial condition for the input, $\theta_i(t=0) = 0$ because $\theta_i(t) = -2\pi\Delta f t$. Substituting these into Equation 3-36, we obtain

$$s\theta_e(s) - \frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o} + \sqrt{2P}K_d K_f K_o \theta_e(s) = s\frac{-2\pi\Delta f}{s^2} - 0 \qquad 3\text{-}37$$

Simplification yields

$$\theta_e(s) = \frac{2\pi\Delta f / \sqrt{2P}K_d K_f K_o}{s + \sqrt{2P}K_d K_f K_o} + \frac{-2\pi\Delta f}{s\left(s + \sqrt{2P}K_d K_f K_o\right)} \qquad 3\text{-}38$$

To obtain the time response necessary for the integrate and dump section of the FSK demodulator, it is necessary to perform the inverse Laplace transform of Equation 3-38. The first term is easily recognized as an exponential response, but the second term requires partial fraction expansion. Using the partial fraction expansion techniques of Chapter 2, the loop equation is rewritten as

$$\theta_e(s) = \frac{\frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o}}{s+\sqrt{2P}K_d K_f K_o} - \frac{\frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o}}{s} + \frac{\frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o}}{s+\sqrt{2P}K_d K_f K_o} \quad 3\text{-}39$$

The inverse Laplace Transform of each term in Equation 3-39 can be computed either by the Laplace inverse equation or the tables in Appendix A. Using the tables, we obtain

$$\theta_e(t) = \frac{-2\pi\Delta f}{\sqrt{2P}K_d K_f K_o} + \frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o} e^{-\sqrt{2\pi}K_d K_f K_o t} - \frac{2\pi\Delta f}{\sqrt{2P}K_d K_f K_o} e^{-\sqrt{2\pi}K_d K_f K_o t} \quad 3\text{-}40$$

In Equation 3-40, we see that at time t=0, $\theta_e(t) = 2\pi\Delta f / \sqrt{2P}K_d K_f K_o$ from the previous symbol. For time t=∞, $\theta_e(t) = -2\pi\Delta f / \sqrt{2P}K_d K_f K_o$. Thus, the integrate and dump detector in Figure 3.16 is operating with input voltages of $\pm 2\pi\Delta f / \sqrt{2P}K_d K_f K_o$, depending upon the data value of the symbol.

Heuristically, we want the loop to acquire as quickly as possible after a symbol transition, to maximize the signal energy in the detector's integrator. Lindsey [9] investigates the noise statistics of this loop.

In Chapter 2, it was shown that $\theta_e(t)_{\text{steady state}} = 0$ for a frequency step input to a second order phase-locked loop. Yet, the integrate and dump in Figure 3.16 is dependent upon $\theta_e(t)_{\text{steady state}} \neq 0$ for the symbol decision. One strategy would be to use a time constant for the filter approximately equal to the symbol interval. Lindsey [9] states with this filter, the performance of the second order loop is not too different from the first order loop.

In modern receivers, a maximum likelihood receiver would be the preferred implementation for a FSK modulation.

## 3.5 Noise Bandwidth

The concept of noise bandwidth can be confusing because of the different definitions of noise bandwidth; single-sided, double-sided, etc. Consider a signal of the form,

$$r(t) = \sqrt{2P}\cos[2\pi f_c t + \theta] + n(t) \qquad 3\text{-}41$$

where $f_c$ is the carrier frequency, $\theta$, is the arbitrary phase of the signal, and $n(t)$ is additive, Gaussian band-limited noise with power spectral density $\frac{N_o}{2}$. Figure 3.18 shows the power spectrum of this signal. Observe half the signal power is at the positive frequency, $f_c$, and the other half at $-f_c$.

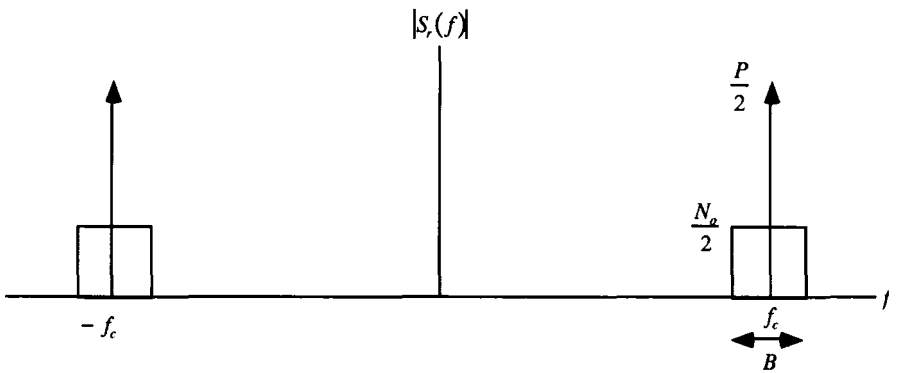


Figure 3.18 Power Spectrum of Received Signal

Figure 3.18 depicts bandlimited noise around the desired signal, s(t). Such a bandlimited signal is generated when the receiver has an IF bandpass filter with bandwidth B. Note the traditional power spectral density of additive Gaussian noise is $N_o/2$, for both the positive and negative frequencies.

We compute the total noise power in the received signal (assuming additive Gaussian noise with $S_n(f) = N_o/2$) as

$$\sigma_n^2 = \int_{-\infty}^{\infty} S_n(f)\, df = N_o B \qquad 3\text{-}42$$

The desired signal in Equation 3-41 has carrier frequency, $f_c$, and the analysis is easier if we express the additive noise as sinusoids with frequency, $f_c$. The noise n(t) can be expressed as a sum of narrowband sinusoids, [4]

$$n(t) = n_c(t)\cos[2\pi f_c t + \theta] - n_s(t)\sin[2\pi f_c t + \theta] \qquad 3\text{-}43$$

The two sinusoids, $n_c(t)$, and $n_s(t)$, are conceptual narrowband noise processes generated by Figure 3.19.

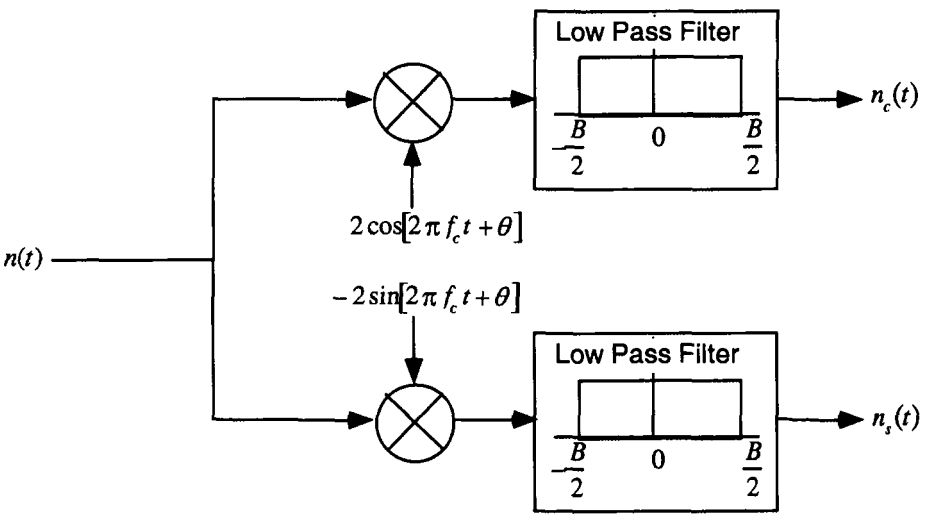


Figure 3.19 Representation of the Quadrature Noise Processes [4]

To obtain the power spectral densities of $n_c(t)$ and $n_s(t)$, we first compute the autocorrelation function of $z_1(t) = 2n(t)Cos[2\pi f_c t]$ [4]

$$
\begin{aligned}
R_{z1}(\tau) &= E\{(2\,n(t)Cos[2\pi f_c t])(2\,n(t+\tau)Cos[2\pi f_c (t+\tau)])\} \\
&= 2E\{n(t)n(t+\tau)\}Cos[2\pi f_c \tau] \\
&\quad + 2E\{n(t)n(t+\tau)\}Cos[4\pi f_c t + 2\pi f_c \tau] \\
&= 2R_n(\tau)Cos[2\pi f_c \tau]
\end{aligned}
\qquad 3\text{-}44
$$

The final form of Equation 3-44 results because the double frequency term is zero. Equation 3-44 can be translated to the frequency domain by recalling that $Cos[2\pi f_c \tau] \leftrightarrow \delta(f - f_c)/2 + \delta(f + f_c)/2$ and then convolving the phasor with $S_n(f)$ to obtain

$$
\begin{aligned}
S_{z1}(f) &= 2S_n(f) * (\delta(f - f_c)/2 + \delta(f + f_c)/2) \\
&= S_n(f + f_c) + S_n(f - f_c)
\end{aligned}
\qquad 3\text{-}45
$$

From Figure 3.19, $S_{nc}(f)$ is the lowpass filtered version of $S_{z1}(f)$, or

$$S_{nc}(f) = L_p\{S_n(f + f_c) + S_n(f - f_c)\} \qquad 3\text{-}46$$

Where $L_p$ denotes the lowpass filtering operation. Similar analysis can be performed to obtain $S_{ns}(f)$. Hint: Use the autocorrelation of $z_2(t) = -2\,n(t)Sin[2\pi f_c t]$, rather than attempting to solve $S_{ns}(f)$ directly from Figure 3.19.

$$S_{ns}(f) = L_p\{S_n(f + f_c) + S_n(f - f_c)\} \qquad 3\text{-}47$$

By integrating $S_{nc}(f)$ and $S_{ns}(f)$ over all frequencies, we obtain the noise variances of the quadrature noise components, $\sigma_{n_c}^2 = \sigma_{n_s}^2 = \sigma_n^2$. The two quadrature noise components are statistically independent if the IF bandpass receiver of the filter is symmetrical about the center frequency $f_c$. This is an important property, because if the filter is skewed, the resulting noise does not have an autocorrelation, $R_n(\tau) = 0, \forall\, \tau$ [5].

Assume the output from the phase detector in Figure 3.16 can be represented by multiplying the input signal, *s(t),* with the VCO's $v_o(t)$,

$$\theta_e(t) = s(t) \times v_o(t) \tag{3-48}$$

$$\theta_e(t) = \left\{\sqrt{2P}\cos[2\pi f_c t + \theta] + n(t)\right\} \times 2\sin[2\pi f_c t + \phi] \tag{3-49}$$

After substituting the quadrature noise representation, and performing some trigonometric substitutions we obtain,

$$\begin{aligned}\theta_e(t) &= \sqrt{2P}\sin[\phi - \theta] + n_c(t)\sin[\phi - \theta] - n_s(t)\cos[\phi - \theta] \\ &+ \sqrt{2P}\sin[4\pi f_c t + \phi + \theta] + n_c(t)\sin[4\pi f_c t + \phi + \theta] \\ &+ n_s(t)\cos[4\pi f_c t + \phi + \theta]\end{aligned} \tag{3-50}$$

The phase detector output in Equation 3-50 has three baseband terms and three double frequency terms (last three terms). We assume that the double frequency terms are removed with lowpass filtering and define the new variable $\varphi = \phi - \theta$.

$$\theta_e(t) = \sqrt{2P}\sin[\varphi] + n_c(t)\sin[\varphi] - n_s(t)\cos[\varphi] \tag{3-51}$$

Under phase-lock conditions, $\sin[\varphi] \approx \varphi$. This approximation allows us to write the linearized phase detector output as

$$\theta_e(t) = \sqrt{2P}\varphi + n_c(t)\sin[\varphi] - n_s(t)\cos[\varphi] \tag{3-52}$$

To further our analysis, we label the noise terms as $n'(t)$, where

$$n'(t) = \frac{n_c(t)}{\sqrt{2P}}\sin[\varphi] - \frac{n_s(t)}{\sqrt{2P}}\cos[\varphi] \tag{3-53}$$

In representing $n'(t)$, we divide by the factor $\sqrt{2P}$. Because this factor $\sqrt{2P}$ appears in our loop transfer functions, $H(f)$, the normalization of $n'(t)$ allows us to use the transfer functions directly, even though the noise

does not have the multiplier $\sqrt{2P}$ . The power spectral density of $n'(t)$ is obtained by first performing the autocorrelation of Equation 3-53 and then a subsequent Fourier Transform.

$$S_{n'}(f) = \frac{1}{2P}\left[S_{ns}(f)Sin^2[\varphi] + S_{ns}(f)Cos^2[\varphi]\right] \qquad 3\text{-}54$$

Suppose the loop is tracking such that $\varphi \to 0$. (This is our usual linear approximation for the phase detector.) Under these conditions, we can write

$$\begin{aligned} S_{n'}(f) &\approx \frac{1}{2P} S_{ns}(f) \\ &\approx L_p\{S_n(f + f_c) + S_n(f - f_c)\} \end{aligned} \qquad 3\text{-}55$$

Figure 3.20 shows the different noise spectrums of Equation 3-55. We have placed the traditional Gaussian noise spectrums inside braces. Note that $S_{n'}(f)$ is centered around DC, and we have folded the upper and lower sidebands into this bandwidth B, centered about 0 Hz.

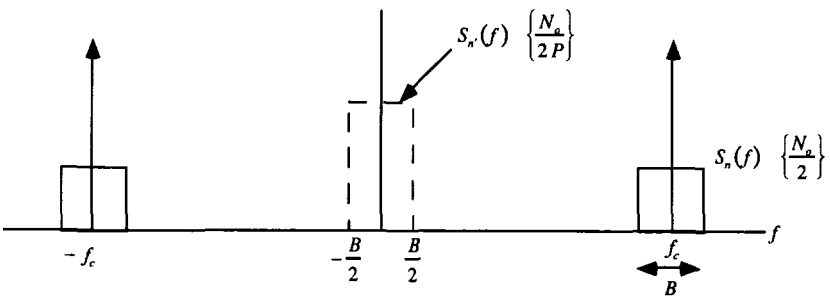


Figure 3.20 Noise Spectrums of Phase-Locked Loop (Traditional Gaussian noise densities in braces)

We note that the narrowband noise process, $n'(t)$ without the scaling factor of 2P, has the same normalized noise power as the original noise process. The noise power inside the loop is

$$\sigma_{n'}^2 = \int_{-\frac{B}{2}}^{\frac{B}{2}} S_{n'}(f)df = \frac{N_o B}{2P} \qquad 3\text{-}56$$

The numerator of $\sigma_{n'}^2$ matches $\sigma_n^2$. The denominator's factor of $2P$ is because of the normalization to the phase-locked loop's gain of $\sqrt{2P}$ embedded within the loop's transfer function.

The phase-locked loop can be modeled by Equation 3-57. Figure 3.21 shows this linearized noise model for the phase-locked loop.

$$\theta_e(t) = \sqrt{2P}\varphi + n'(t) \qquad 3\text{-}57$$

The power spectral density of the system is

$$S_{\theta_o}(f) = S_{\theta_e}(f)|H(f)|^2 \qquad 3\text{-}58$$

Considering noise only, we compute the noise variance at the output, $\theta_o(t)$, of the VCO as

$$\sigma_{n\theta_o}^2 = \int_{-\infty}^{\infty} S_{n\theta_e}(f)|H(f)|^2 df \qquad 3\text{-}59$$

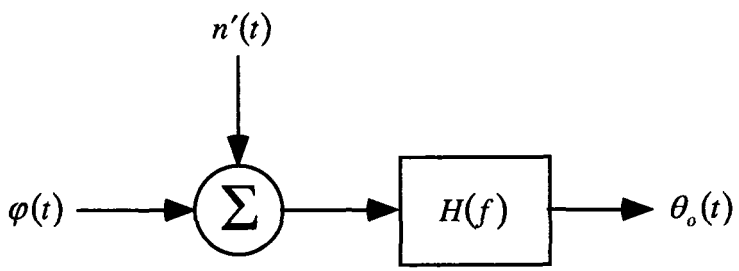


Figure 3.21 Equivalent Noise Model of Phase-Locked Loop

Note that $S_{n\theta_e}(f) = S_{n'}(f) = N_o/2P$, so the phase-locked loop's output noise variance is

$$\sigma^2_{n\theta_o} = \frac{N_o}{2P}\int_{-\infty}^{\infty}|H(f)|^2 df \qquad 3\text{-}60$$

Observe that H(f) is symmetrical, so we can rewrite $\sigma^2_{n\theta_o}$ with a single-sided integral (corresponding to a single sided definition) as

$$\sigma^2_{n\theta_o} = \frac{2N_o}{2P}\int_{0}^{\infty}|H(f)|^2 df \qquad 3\text{-}61$$

The traditional definition of loop bandwidth is one-sided, as shown in Equation 3-62,

$$B_L = \int_0^{\infty}|H(f)|^2 \quad df \qquad 3\text{-}62$$

This definition of a phase-locked loop's bandwidth permits us to express $\sigma^2_{n\theta_o}$ as a function of the loop bandwidth,

$$\sigma^2_{n\theta_o} = \frac{2N_o}{2P}B_L \qquad 3\text{-}63$$

The concept of loop bandwidth also allows us to rewrite the input signal-to-noise ratio of the phase-locked loop as

$$SNR_L = \frac{P}{N_o B_L} \text{ (text definition of loop signal - to - noise)} \qquad 3\text{-}64$$

Equation 3-64 is the definition of loop signal-to-noise used in this text. Gardner includes a factor of 0.5, [5]

$$SNR_L = \frac{P}{2N_o B_L} \quad \text{(Gardner's definition of loop signal - to - noise)} \quad 3\text{-}65$$

The literature is confusing, and the reader is cautioned to check an author's definitions when comparing different results in the literature. $SNR_L$ is a parametric which is useful in describing the performance of a PLL to noisy signals, much like $w_n$ is a parametric for the dynamic response. To avoid confusion, we will specify $P/N_o B_L$ in our analysis and graphs, rather than $SNR_L$.

To obtain the noise bandwidths for the different loop configurations, we substitute the closed loop transfer function into Equation 3-47 and perform the integration. Figure 3.22 shows the noise bandwidths for the different configurations [5].

In Chapter 4, we will study the effects of noise upon phase-locked loop acquisition and tracking.

| Description | |
|---|---|
| First Order H(s) | $H(s)=\frac{\sqrt{2P}K_oK_dK_f}{s+\sqrt{2P}K_oK_dK_f}$ |
| First Order Noise Bandwidth (Hz) | $B_L=\frac{\sqrt{2P}K_oK_dK_f}{4}$ |
| Second Order Lowpass Filter H(s) | $H_{0,Lowpass}(s)=\frac{w_n^2}{s^2+2\zeta w_n s+w_n^2}$ |
| Second Order Lowpass Filter Noise Bandwidth (Hz) | $B_L=\frac{\omega_n^4}{16\sqrt{\gamma}}\left(\frac{1}{\sqrt{-2\sqrt{\gamma}+\lambda}}-\frac{1}{\sqrt{2\sqrt{\gamma}+\lambda}}\right)$ where $\gamma=\omega_n^4\xi^2\left(\xi^2-1\right),\lambda=\omega_n^2\left(2\xi^2-1\right)$ |
| Second Order Passive Lead-Lag Filter H(s) | $H_{0,Passive}(s)=\frac{\tau_2\omega_n^2 s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$ |
| Second Order Passive Lead-Lag Filter Noise Bandwidth (Hz) | $B_L=\frac{K_O K_d\left(K_O K_d \tau_2^2\right)}{4\left(K_O K_d \tau_1 \tau_2+\tau_1\right)}$ |
| Second Order Active Lead-Lag Filter H(s) | $H_{O,Active}(s)=\frac{2\zeta w_n s+w_n^2}{s^2+2\zeta w_n s+w_n^2}$ |
| Second Order Active Lead-Lag Filter Noise Bandwidth (Hz) | $B_L=\frac{w_n}{2}\left(\zeta+\frac{1}{4\zeta}\right)$ |
| Third Order Loop Type-3 Transfer Function | $H_{o,3rd}(s)=\frac{\sqrt{2P}K_oK_d\frac{\tau_2^2}{\tau_1^2}\left(s^2+s\frac{2}{\tau_2}+\frac{1}{\tau_2^2}\right)}{s^3+\sqrt{2P}K_oK_d\frac{\tau_2^2}{\tau_1^2}\left(s^2+s\frac{2}{\tau_2}+\frac{1}{\tau_2^2}\right)}$ |
| Third Order Loop Type-3 Noise Bandwidth | $B_L=\frac{3K_dK_o\sqrt{P}\tau_1^{\,2}\tau_2^{\,2}+2\sqrt{2}K_d^{\,2}K_o^{\,2}P\tau_2^{\,5}}{-2\sqrt{2}\tau_1^{\,4}+8K_dK_o\sqrt{P}\tau_1^{\,2}\tau_2^{\,3}}$ |

Figure 3.22 Noise Bandwidths for Different PLL Configurations

## 3.6 Third Order Phase-Locked Loop Design

### 3.6.1 Third Order Type-2 Filter

We delayed the design procedure for third order phase-locked loops until we presented the frequency domain analysis of the loops. At this time, we can proceed with some design guidelines for third order loops. Przedpelski [6] defined a procedure for the third order filter of the form,

$$F(s)=\frac{\tau_2 s+1}{\tau_1 s(\tau_3 s+1)} \qquad 3\text{-}66$$

(This loop filter configuration was shown in Figure 2.14.) The first performance parameter to be established is the phase margin, which we described previously with Bode analysis. (The phase margin corresponds to the loop stability at the open loop unity gain crossover.) The unity gain crossover frequency is defined as $f_0$, and the desired phase margin as $\phi$. With these definitions, the filter parameter $\tau_3$ can be computed as

$$\tau_3=\frac{Sec[\phi]-Tan[\phi]}{2\pi f_0} \qquad 3\text{-}67$$

It may seem non-intuitive to specify the loop filter through the open loop's unity gain frequency. In the applications most appropriate for this filter, it is a readily computed parameter, dependent upon the phase noise performance desired from the loop. Once $\tau_3$ is defined, then we can obtain $\tau_2$,

$$\tau_2=\left(4\pi^2 f_0^2 \tau_3\right)^{-1} \qquad 3\text{-}68$$

This allows us to specify the third filter parameter, $\tau_1$,

$$\tau_1=\left|\frac{\sqrt{2P}K_o K_d}{w^2}\left\{\frac{-jw\tau_2-1}{jw\tau_3+1}\right\}\right|_{w=2\pi f_0} \qquad 3\text{-}69$$

## *Example 3.4*

Design a third order PLL, using the third order type-2 loop filter. Compute the necessary filter coefficients for the loop filter with the following parameters and specifications:

VCO: $K_O$ = 10 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian, Input Power: 0 dBm (1mW), Unity Gain Frequency: 30 Hz, Phase Margin: 45°

Following our analysis in Example 2.1, we compute the gain of the VCO, phase detector, and input signal level,

$$\sqrt{2P}K_oK_d = \frac{\sqrt{2\times 1\times 10^{-3}\times 50}}{1}\left(\frac{2\pi 10\ \text{rad}}{V\times\text{sec}}\right)\left(\frac{\frac{1}{2}V}{\text{rad}}\right) \qquad 3\text{-}70$$

We substitute the specified phase margin of 45° into Equation 3-67 to obtain $\tau_3$,

$$\tau_3 = \frac{Sec[45°]-Tan[90°]}{2\pi(30)} = 0.002198 \qquad 3\text{-}71$$

Substituting the unity gain frequency and $\tau_3$, into Equation 3-68, we obtain

$$\tau_2 = \left(4\pi^2 f_0^2 \tau_3\right)^{-1} = 0.01281 \qquad 3\text{-}72$$

The final filter parameter for the third-order loop is obtained by substitution into Equation 3-69,

$$\tau_1 = \left|\frac{\sqrt{2P}K_oK_d}{w^2}\left\{\frac{-jw\tau_2-1}{jw\tau_3+1}\right\}\right|_{w=2\pi f_0} = 0.0006750 \qquad 3\text{-}73$$

The open loop transfer function is computed as

$$H_{OL}(s)=\frac{9.935\left(1+1.281\times10^{-3}s\right)}{9.935+0.1274s+6.750\times10^{-4}s^2+1.483\times10^{-6}s^3} \qquad 3\text{-}74$$

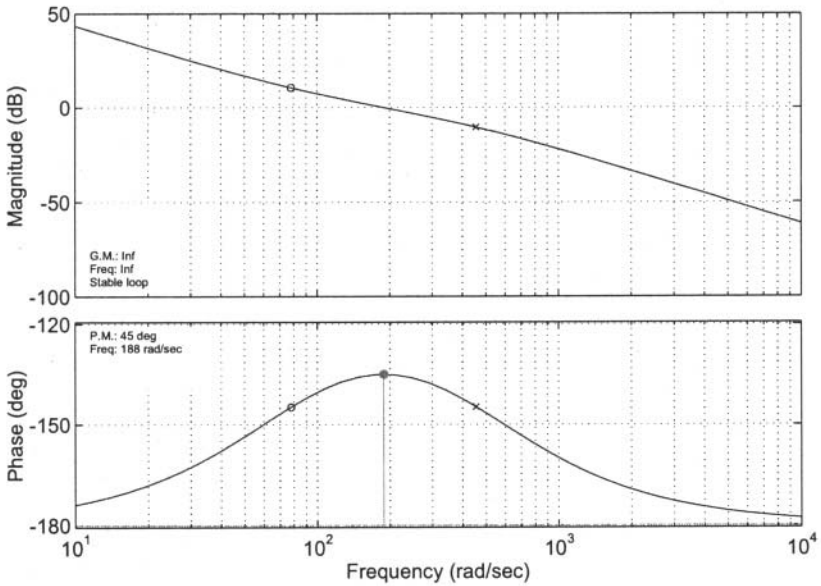


Figure 3.23 Bode Analysis of Example 3.4

Figure 3.23 shows the Bode Analysis of the open loop transfer function. The loop's unity gain crossover (0 dB) is at 30 Hz, just as specified. From 1 Hz to 30 Hz, the open loop phase is constantly increasing due to the integrators. By placing the pole corresponding to $\tau_3$, at **f= 72.4 Hz,** we force the phase to start decreasing at **f= 30 Hz**. This allows us to meet the specified 45° phase margin. (This phase margin may be insufficient, because the time response may have too much of an overshoot.)

The parameter $\tau_2$ establishes the breakpoint frequency **(f=12.4 Hz)** of the transfer functions' zero. The positive 90° slope of the zero begins at **f=1.24** Hz and completes at **f=124 Hz.** We begin the negative 90° slope of the pole at **f=7.24 Hz,** and end at **f=724 Hz.** The noise bandwidth is obtained by numerically integrating,

$$\text{Noise Bandwidth} = \int_0^{\infty} |H(f)|^2 \, df \qquad 3\text{-}75$$

$$\text{where } |H(f)|^2 \equiv \frac{K\left(1+4f^2\pi^2\tau_2^2\right)}{\left(\begin{array}{l} K^2 - 8f^2K\pi^2\tau_1 + 16f^4\pi^4\tau_1^2 + 4f^2K^2\pi^2\tau_2^2 \\ -32f^4K\pi^4\tau_1\tau_2\tau_3 + 64f^6\pi^6\tau_1^2\tau_3^2 \end{array}\right)} \qquad 3\text{-}76$$

$$\text{and } K = \sqrt{2P}K_oK_d \qquad 3\text{-}77$$

Numeric integration yields Noise **Bandwidth** $= 80.4Hz$. The closed loop magnitude response is shown in Figure 3.24. This frequency response is important, because it provides insight to the noise performance of the loop. If the closed loop response exhibits excessive peaking, then the noise bandwidth will be unnecessarily higher than without the peaking. (Ideally, we want Figure 3.24 to have flat frequency response until the amplitude roll-off.) If excessive peaking exists, then the loop should be redesigned with a larger phase margin.

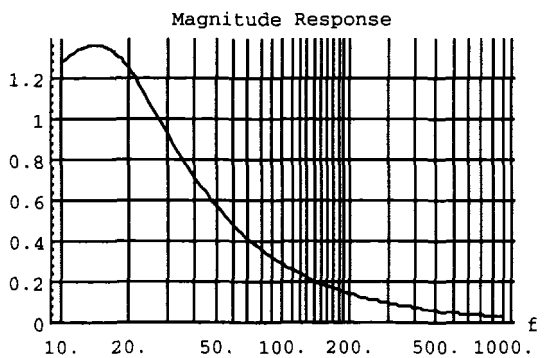


Figure 3.24 Closed Loop Magnitude Response

### 3.6.2 Third Order Filter Type-3 Filter

Designing a third order phase-locked loop with the third order type-3 filter is slightly different. (The filter was shown in Figure 2.14.) Consider the open loop transfer function for a third order loop with third order type-3 filter,

$$H_{OL}(s) = \frac{\sqrt{2P}K_o K_d}{s}\frac{(s\tau_2 + 1)^2}{(s\tau_1)^2} \qquad 3\text{-}78$$

To perform a Bode Analysis of this third order loop, we place Equation 3-78 in the form of Equations 3-20 and 3-21.

$$20Log|H_O(jw)| = 20Log\left|\sqrt{2P}K_o K_d/\tau_1^2\right| + 40Log|1 + jw\tau_2| - 60Log|jw| \qquad 3\text{-}79$$

$$\angle H_O(jw) = 2\tan^{-1}[w\tau_2] - 270° \qquad 3\text{-}80$$

To obtain Equations 3-79 and 3-80, we note that N=3, because of the three perfect integrators in the open loop transfer function, $H_{OL}(jw)$. There are the two repeated zeros corresponding to $(s\tau_2 + 1)$, and no poles other than the perfect integrators. Of particular interest is Equation 3-80, which indicates the open loop phase is a function only of the parameter, $\tau_2$. This provides our design concept.

The first term of Equation 3-79 provides a constant gain term, which is graphed as the horizontal line. The filter's $\tau_1$ parameter adds additional DC gain to the other gain parameters, $\sqrt{2P}K_o K_d$. The three poles at the origin create a 60 dB/decade slope from 0 Hz. The parameter $\tau_2$ counteracts the negative slope of the three perfect integrators with a positive 40 dB/decade slope at $w = 1/\tau_2$. After $w = 1/\tau_2$, the frequency roll-off is a negative 20 dB/decade slope. The primary affect of $\tau_2$ is to change the unity gain frequency of the open loop transfer function, because the slope due to the perfect integrators alone would intersect the 0 dB axis at a much lower frequency than with the double zeros. The bold line in Figure 3.25 shows an approximate composite of the three different terms in Equation 3-79.

The phase angle of the open loop transfer function is calculated with Equation 3-80. It has a constant – 270° term due to the three perfect integrators. Recall that we approximate the + 90° phase shift due to a single zero beginning at $w = 0.1/\tau_2$. The + 90° phase shift is completed at $w = 10.0/\tau_2$. The bold line in the phase plot shows the approximate composite phase response.

As with the third order type-2 filter, a reasonable phase margin of 45 degrees could be the design guideline for specifying $\tau_2$. We caution that 45 degrees may be insufficient, and the loop may have excessive peaking in the closed loop frequency response. This tends the loop toward instability, and also unnecessarily increases the noise bandwidth. In Example 3.5, which follows, we found 65 degrees as a better design compromise.

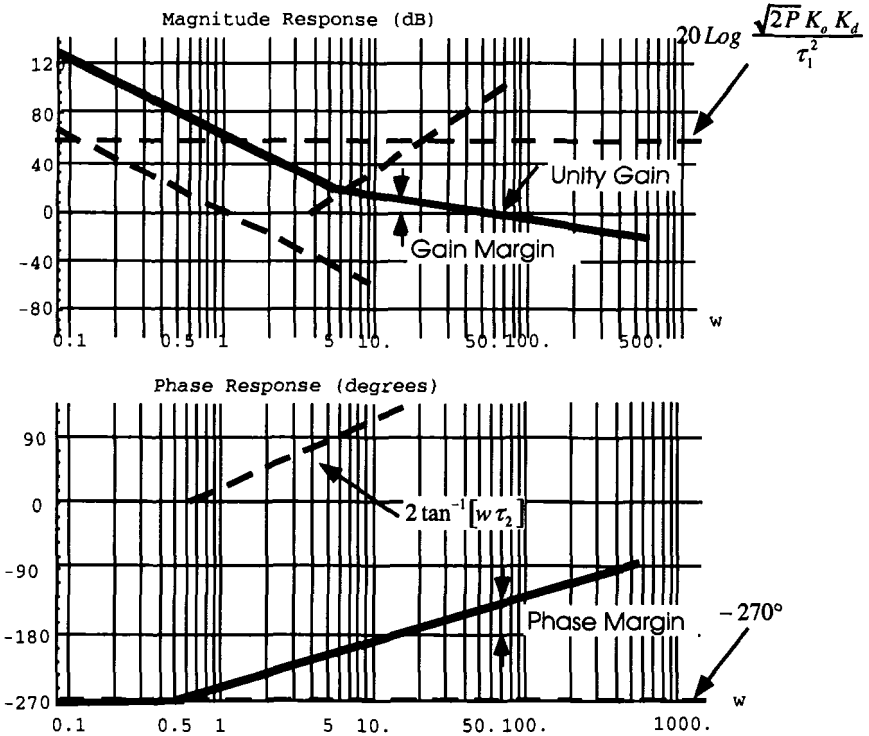


Figure 3.25 Bode Analysis of Third Order Loop With Gardner's Filter

From Equation 3-80, we define $\tau_2$ from

$$90° + \text{Phase Margin} = 2\tan^{-1}[w_0\tau_2] \qquad 3\text{-}81$$

where $w_0$ = unity gain frequency

Solving Equation 3-81 for $\tau_2$,

$$\tau_2 = \frac{1}{w_0}\tan\left[\frac{90° + \text{Phase Margin}}{2}\right] \qquad 3\text{-}82$$

Once we have established a value for $\tau_2$ , we can solve for $\tau_1$,

$$\tau_1 = \sqrt{\frac{\sqrt{2P}K_o K_d}{w_0^{\,3}}\left(1 + w_0^{\,2}\tau_2^2\right)} \qquad 3\text{-}83$$

A disadvantage to this design approach is that we cannot directly specify a noise bandwidth and then obtain $\tau_1$ and $\tau_2$. To obtain a desired noise bandwidth, we suggest setting a reasonable phase margin, and then iterating the unity gain crossover frequency until the desired noise bandwidth is obtain. To obtain the noise bandwidth, a numeric integration can be performed, using the closed loop transfer function and Equation 3-62.

## *Example 3.5*

Design a third order PLL, using the third order type-3 loop filter. Compute the necessary filter coefficients for the loop filter with the following parameters and specifications:

**VCO: $K_O$ = 10 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian,**

Input Power: 0 dBm (1mW), Unity Gain Frequency: 30 Hz,
Phase Margin: 65°

In this example, the unity gain frequency is specified, along with the phase margin. Along with the loop elements, this is sufficient to define the filter. Following Example 2.1, we calculate the gain of the fixed loop components,

$$\sqrt{2P}K_o K_d = \frac{\sqrt{2 \times 1 \times 10^{-3} \times 50}}{1}\left(\frac{2\pi 10 \ \text{rad}}{V \times \text{sec}}\right)\left(\frac{\frac{1}{2}V}{\text{rad}}\right) \qquad 3\text{-}84$$

The phase margin specification of 65° establishes the filter's $\tau_2$ parameter.

$$\tau_2 = \frac{1}{2\pi(30)} \tan\left[\frac{90° + 65°}{2}\right] = 2.393 \times 10^{-2} \qquad 3\text{-}85$$

Once the breakpoint of the repeated zeros is established, we can compute the filter's DC gain parameter, $\tau_1$,

$$\tau_1 = \sqrt{\frac{\sqrt{2\ P} K_o K_d}{w_0^{\ 3}} \left(1 + w_0^{\ 2} \tau_2^2\right)} = 5.627 \times 10^{-3} \qquad 3\text{-}86$$

The open loop transfer function is obtained by substituting $\tau_1$ and $\tau_2$ into the open loop Equation 3-78,

$$H_{OL}(s) = \frac{313745(1 + 0.2393\,s)^2}{s^3} \qquad 3\text{-}87$$

The closed loop transfer function is obtained from $H_{OL}(s)$,

$$H_o(s) = \frac{H_{OL}(s)}{1 + H_{OL}(s)} = \frac{313745(1 + 0.2393\,s)^2}{313745 + 15015.9\,s + 179.665\,s^2 + s^3} \qquad 3\text{-}88$$

The noise bandwidth is obtained by

$$\text{Noise Bandwidth} = \int_0^\infty |H_o(f)|^2\, df \qquad 3\text{-}89$$

Numeric integration yields Noise Bandwidth = 68.8 *Hz*.

Figure 3.26 shows the Bode Analysis of the open loop transfer function, Equation 3-87. The repeated zeros, corresponding to the $(s\tau_2 + 1)^2$ term in the loop filter, have a breakpoint of $f = \frac{1}{2\pi}\frac{1}{\tau_2} = 6.65\ \text{Hz}$. Recall from the linear phase approximation, the composite phase angle will be increasing at 90°/ decade (remember there are two zeros), beginning at f=0.66 Hz, and ending at 66.5 Hz.

Figure 3.26 shows that we have a gain of 18 dB when the phase angle is 180° (f=7 Hz). This is a gain margin of -18 dB. (This implies that if the loop gain is less than designed, the loop can be unstable, which can be a problem for phase-locked loops used in applications where the signal level may vary.) The unity gain crossover (0 dB) occurs at **f = 30 Hz,** with a phase angle of -115°, which yields the desired 65° phase margin.

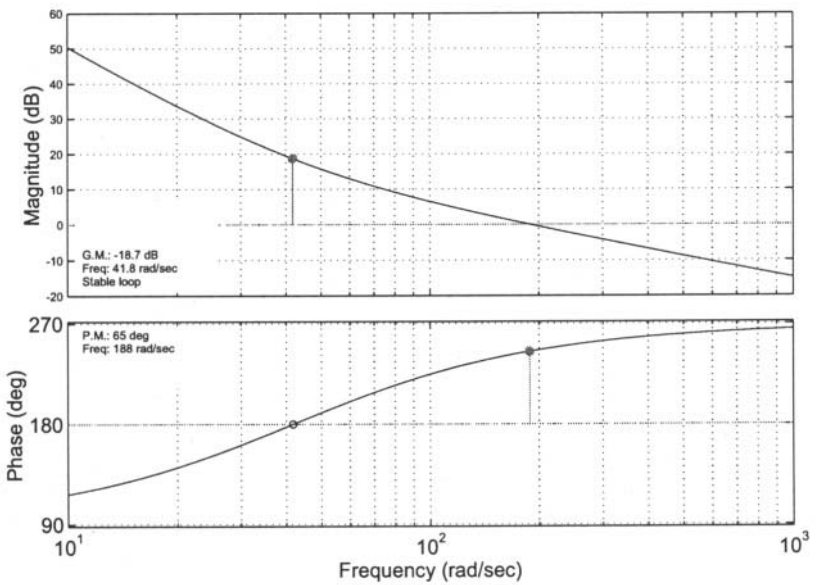


Figure 3.26 Bode Analysis of the Third Order Loop

The closed loop frequency response is shown in Figure 3.27. It shows a moderate amount of frequency peaking around **f=15 Hz,** which is generally acceptable. (Frequency peaking is usually of interest to designers when there is a difficult phase noise specification. Frequency peaking permits extra phase noise energy into the loop bandwidth, which can degrade the bit error rate performance of a receiver.) If not, then increasing the phase margin will yield less frequency peaking.

A design with 45° phase margin resulted in the magnitude response of Figure 3.28. Note the excessive frequency peaking, which unnecessarily increased the noise bandwidth to 91.8 Hz. (Almost a 50% increase.) From experience, we would also be suspicious of this loop's stability.

The root locus of the loop design is shown in Figure 3.29. The position of the closed loop poles at the design specification **(k=1)** is sufficiently in the left-hand plane that a loss of loop gain due to component tolerances (more typically, the input signal level) will still allow a stable loop. However, at low gain levels (as predicted by the negative gain margin in the Bode Analysis) the loop has poles in the right hand plane, and is unstable.

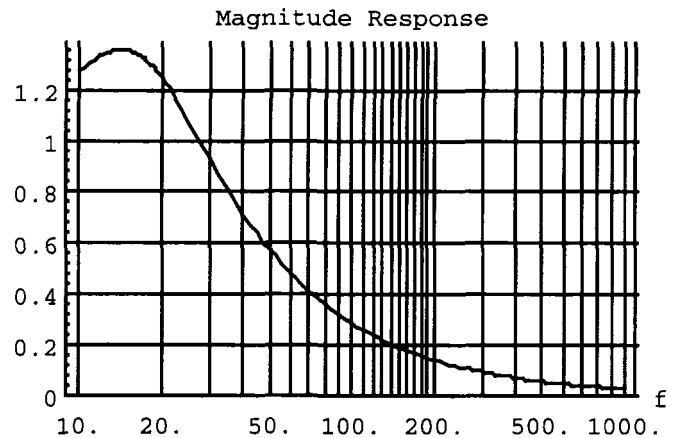


Figure 3.27 Closed Loop Frequency Response With Specified 65° Phase Margin

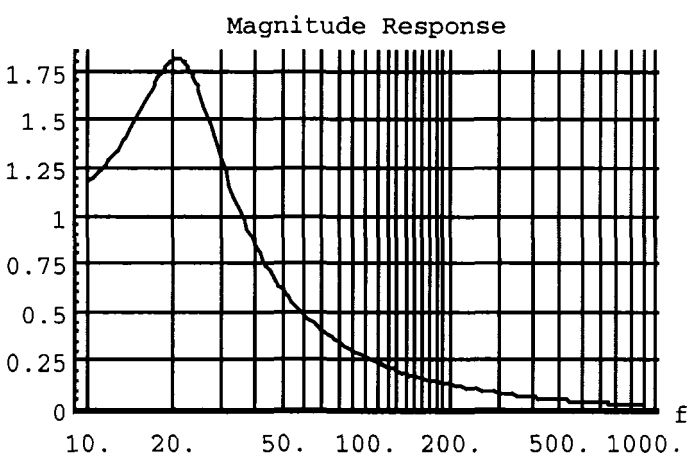


Figure 3.28 Closed Loop Frequency Response with 45° Phase Margin

In this root locus, note that the **k=0** position of the poles corresponds to the poles of the open loop transfer function. As **k->infinity,** the closed loop poles correspond to the zeros of the open loop transfer function.

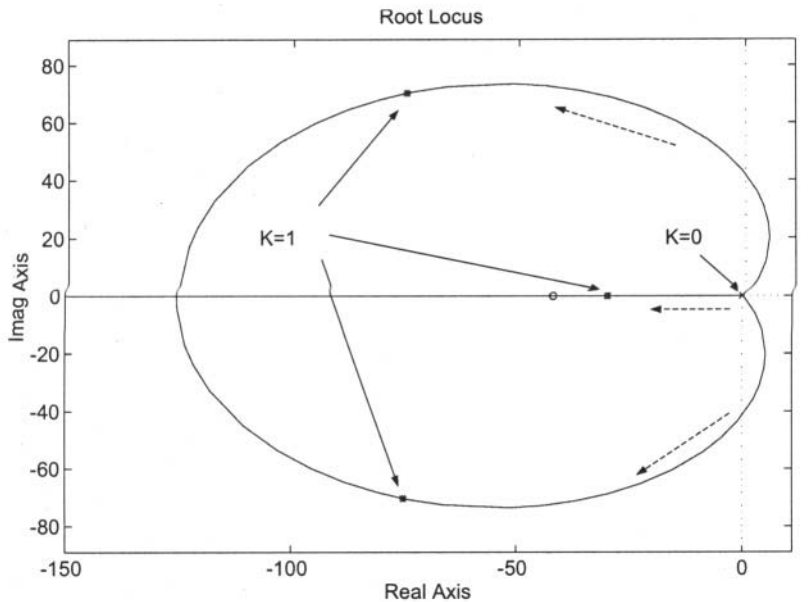


Figure 3.29 Root Locus of Example 3.5

## 3.7 References

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## 3.8 Problems

3.1 Compute the root locus for the open loop transfer function, $H_{OL}(s)=\frac{k}{s+3}$. Consider $0 \le k \le 4$.

3.2 Compute the root locus for the open loop transfer function, $H_{OL}(s)=\frac{k}{s^2+3}$. Consider $0 \le k \le 4$.

3.3 Compute the root locus for the open loop transfer function, $H_{OL}(s)=k\frac{s+2}{s^2+3}$. Consider $0 \le k \le 4$.

3.4 Compute the root locus for the second order phase-locked loop's open loop transfer function, $H_{OL}(s)=k\frac{1}{s}\frac{s\tau_2+1}{s\tau_1}$. For this particular design, $\tau_1 = 2.81222 \times 10^{-5}$ and $\tau_2 = 7.49849 \times 10^{-3}$. Consider $0 \le k \le 4$. What is the value of k when the roots become real?

3.5 Compute the root locus for the second order phase-locked loop's open loop transfer function, $H_{OL}(s)=k\frac{1}{s}\frac{s\tau_2+1}{s\tau_1}$. For this particular design, $\tau_1 = 6.94444 \times 10^{-3}$ and $\tau_2 = 0.117833$. Consider $0 \le k \le 2$. What is the value of k when the roots become real?

3.6 Compute the root locus for the third order phase-locked loop using Gardner's loop filter. The open loop transfer function is $H_{OL}(s)=k\frac{1}{s}\left(\frac{s\tau_2+1}{s\tau_1}\right)^2$. For this particular design, $\tau_1 = 5.23382 \times 10^{-3}$ and $\tau_2 = 0.0456903$. Consider $0 \le k \le 2$. What is the value of k when the roots become real?

3.7 Compute the root locus for the third order phase-locked loop using Gardner's loop filter. The open loop transfer function is

$H_{OL}(s) = k\frac{1}{s}\left(\frac{s\tau_2 + 1}{s\tau_1}\right)^2$. For this particular design, $\tau_1 = 9.93489 \times 10^{-3}$ and $\tau_2 = 0.0454594$. Consider $0 \le k \le 8$. What is the value of k when the roots become real?

3.8 Plot the magnitude and phase graphs for a Bode analysis of a second order phase-locked loop. The open loop transfer function is $H_{OL}(s) = k\frac{1}{s}\frac{s\tau_2 + 1}{s\tau_1}$. For this particular design, $\tau_1 = 2.81222 \times 10^{-5}$ and $\tau_2 = 7.49849 \times 10^{-3}$. Plot magnitude and phase for $1\ \text{Hz} \le f \le 1\ \text{kHz}$. What are the gain and phase margins?

3.9 Plot the magnitude and phase graphs for a Bode analysis of a second order phase-locked loop. The open loop transfer function is $H_{OL}(s) = k\frac{1}{s}\frac{s\tau_2 + 1}{s\tau_1}$. For this particular design, $\tau_1 = 5.23382 \times 10^{-3}$ and $\tau_2 = 0.0456903$. Plot magnitude and phase for $1\ \text{Hz} \le f \le 1\ \text{kHz}$. What are the gain and phase margins?

3.10 Plot the magnitude and phase graphs for a Bode analysis of a third order phase-locked loop. The open loop transfer function is $H_{OL}(s) = k\frac{1}{s}\left(\frac{s\tau_2 + 1}{s\tau_1}\right)^2$. For this particular design, $\tau_1 = 694444 \times 10^{-3}$ and $\tau_2 = 0.117833$. Plot magnitude and phase for $1\ \text{Hz} \le f \le 1\ \text{kHz}$. What are the gain and phase margins?

3.11 Plot the magnitude and phase graphs for a Bode analysis of a third order phase-locked loop. The open loop transfer function is $H_{OL}(s) = k\frac{1}{s}\left(\frac{s\tau_2 + 1}{s\tau_1}\right)^2$. For this particular design, $\tau_1 = 9.93489 \times 10^{-3}$ and $\tau_2 = 0.0454594$. Plot magnitude and phase for $1\ \text{Hz} \le f \le 1\ \text{kHz}$. What are the gain and phase margins?

3.12 Compute the noise bandwidth of a loop with an open loop transfer function of $H_{OL}(s)=\frac{1}{s+3}$.

3.13 Compute the noise bandwidth of a loop with an open loop transfer function of $H_{OL}(s)=\frac{2}{s^2+3}$.

3.14 Compute the noise bandwidth of the second order phase-locked loop with an open loop transfer function of $H_{OL}(s)=k\frac{1}{s}\frac{s\tau_2+1}{s\tau_1}$. For this particular design, $\tau_1=2.81222\times10^{-5}$ and $\tau_2=7.49849\times10^{-3}$.

3.15 Compute the noise bandwidth of the second order phase-locked loop with an open loop transfer function of $H_{OL}(s)=k\frac{1}{s}\frac{s\tau_2+1}{s\tau_1}$. For this particular design, $\tau_1=694444\times10^{-3}$ and $\tau_2=0.117833$.

3.16 Compute the noise bandwidth of the third order phase-locked loop with an open loop transfer function of $H_{OL}(s)=k\frac{1}{s}\left(\frac{s\tau_2+1}{s\tau_1}\right)^2$. For this particular design, $\tau_1=694444\times10^{-3}$ and $\tau_2=0.117833$.

3.17 Compute the noise bandwidth of the third order phase-locked loop with an open loop transfer function of $H_{OL}(s)=k\frac{1}{s}\left(\frac{s\tau_2+1}{s\tau_1}\right)^2$. For this particular design, $\tau_1=9.93489\times10^{-3}$ and $\tau_2=0.0454594$.

3.18 Design a first order loop filter that meets the following requirements:
VCO: $K_O$ = 100 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian
Input Power = 20mW
Bandwidth = 30 Hz.

3.19 Design a second order loop filter that meets the following requirement

VCO: KO = 1000 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian
Input Power = 10mW
Design the loop for =10 Hz and. What is the noise bandwidth? What are the gain and phase margins for the design. For what gain value do the roots become real?

3.20 Design a third order loop filter that meets the following requirements:
VCO: KO = 13 KHz/Volt, Phase Detector: Kd = 1/2 Volt/Radian
Input Power = 100mW, Damping factor:.
Design the loop for a unity gain frequency of 1400 Hz and a phase margin of 45°. What value of gain corresponds to a marginally stable loop? (roots on the jw axis). What is the noise bandwidth?

# 4

# Acquisition and Tracking

In Chapter 2, the basic configurations for phase-locked loops were presented. In Chapter 3, we reviewed frequency analysis and stability, which allowed us to introduce design procedures for third order phase-locked loops. In this chapter, we will be examining the subtleties of phase-locked loop acquisition and tracking. In Chapters 2 and 3, we were interested in the linearized performance, but in this chapter, we want to examine acquisition, which requires consideration of the nonlinear phase detector.

The reader is cautioned not to be disheartened by the nonlinear equations presented early in this chapter, as they are only used to derive some estimating quantities for acquisition. For loop tracking, noise bandwidth, stability, etc, we will return to the linearized equations of Chapter 2.

## 4.1 First Order Acquisition

Figure 4.1 is a modification of the loop architecture that we evaluated in Chapter 2. The primary difference between Figure 2.2 and Figure 4.1 is the nonlinear function *Sin*[...], within the modeled phase detector. The filter has also been changed to a generic F(s) instead of the fixed gain, $K_f$, which was appropriate for a first order loop.

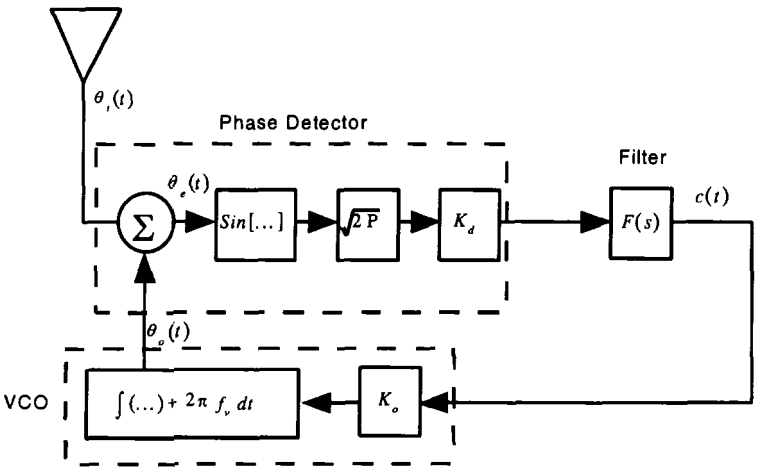


Figure 4.1 Nonlinear Phase-Locked Loop for Acquisition Analysis

Note the VCO in Figure 4.1 includes a center frequency, $f_v$. With a zero volt error input into the VCO (c(t)=0), the VCO produces the frequency $f_v$. This permits the downconversion of the input signal without requiring large signal voltages into the VCO. (A $0Hz \rightarrow \infty$ VCO is textbook fiction.)

Our analysis follows that first presented by Viterbi [1]. Assuming a first order loop, with $F(s) = K_f$, we can write the phase error, $\theta_e(t)$, as

$$Sin[\theta_e(t)] = Sin\left[\theta_i(t) - \sqrt{2P}K_o K_f K_d \int Sin[\theta_e(t)]dt - 2\pi f_v t\right] \qquad 4\text{-}1$$

Trigonometric and calculus operations yield

$$\theta_e'(t) = \theta_i'(t) - \sqrt{2P}K_o K_f K_d Sin[\theta_e(t)] - 2\pi f_v \qquad 4\text{-}2$$

In physical terms, the derivative of the phase variables, $\theta_e(t)$ and $\theta_i(t)$, is frequency. With this insight, the left-hand side of Equation 4-2 represents the frequency error of the loop with the loop phase input, $\theta_i(t)$.

The term, $\theta_i'(t) - 2\pi f_v$, represents a static frequency offset, which we define as

$$\Omega = \theta_i'(t) - 2\pi f_v \qquad 4\text{-}3$$

The numerous multipliers representing gain and power multipliers in front of the Sin[.] function of Equation 4-2 can be represented with the single variable,

$$K = \sqrt{2P}K_o K_f K_d \qquad 4\text{-}4$$

With these definitions, Equation 4-2 can be expressed as [1]

$$\theta_e'(t) = \Omega - K\,Sin[\theta_e(t)] \qquad 4\text{-}5$$

Equation 4-5 is graphed in Figure 4.2. The graph is somewhat confusing at first, because the phase error, $\theta_e(t)$ is the independent variable, and the phase error's derivative, $\theta_e'(t)$ is the dependent variable. In other words, we are graphing the loop's frequency error for a specific phase error.

For the loop to be phase-locked, the derivative of the error, (frequency) must be zero, i.e. $\theta_e'(t) = 0$. Figure 4.2 indicates this condition only occurs at the points on the abscissa. The intersection with the vertical axis corresponds to the VCO operating at its nominal frequency, $f_v$, with an error voltage, $\theta_e(t) = 0$. (This also describes the VCO's initial condition at time t=0.)

Figure 4.2 illustrates that the phase-lock acquisition process is dependent upon the initial value of $\theta_e'(t)$. As an example, suppose the initial coordinate pair $\left(\theta_e', \theta_e\right)$ is at point A on the graph. The phase-locked loop will follow the indicated trajectory to B, which is a stable null. Figure 4.2 thus graphs how the PLL will converge to a zero error condition, by following the exact path between point A and point B. Because the first order loop graphed in Figure 4.2 has a frequency offset, it is impossible to obtain simultaneously $\theta_e' = 0$ and $\theta_e = 0$. When the loop is locked, we have a static phase error denoted by the value of $\theta_e$ at point B.

As shown in Figure 4.2, not all of the $\theta_e' = 0$ points on the graph are stable nulls. Only nulls with a negative $\theta_e' / \theta_e$ slope are stable. For example, consider point D, which might correspond to a noise spike instantaneously forcing a loop from its null at point C. For a $\Delta\theta_e$ displacement, we can write

$$\frac{d\theta_e'}{d\theta_e} \times \Delta\theta_e \approx \Delta\theta_e' \qquad 4\text{-}6$$

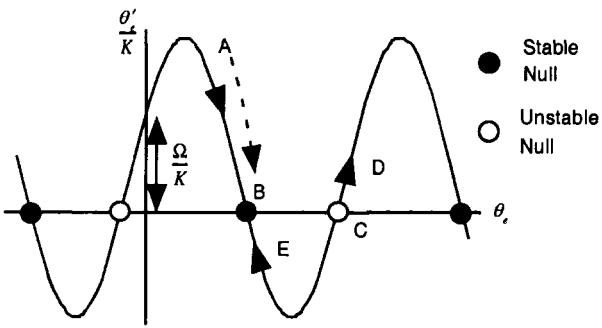


*Figure 4.2* Phase Plane Trajectory for First Order Loop

If noise creates a small phase error, corresponding to $\Delta\theta_e$, we have a positive $\Delta\theta_e'$ at the unstable nulls. As shown in Figure 4.2, this will drive the loop away from the null.

For those familiar with second order loops, it is somewhat surprising that a first order loop does not cycle slip in acquiring a signal. Cycle slipping occurs when the PLL makes a zero-crossing more than twice in the phase plane portrait of Figure 4.2 without locking. (A more formal definition is when the phase exceeds $2\pi$.) In frequency acquisition, a first order loop behaves in a binary fashion. It either acquires phase without cycle slipping, or it never does.

Equation 4-2 also shows if the input frequency, $\frac{\theta_i'(t)}{2\pi} - 2\pi f_v > \frac{\sqrt{2P}\,K_o K_f K_d}{2\pi}$, then there is no solution, implying the loop cannot acquire the input signal. (The Sin(.) function has a maximum

value of unity.) From this observation, the frequency pull-in limit for the first order phase-locked loop is written as

$$f_p \leq \frac{\sqrt{2P}K_o K_f K_d}{2\pi} \qquad 4\text{-}7$$

Equation 4-5 can be solved to yield the acquisition time, but a singularity can prevent a finite solution. Viterbi [1] notes this is physically correct, as the time to reach steady state is indeed infinite.

The acquisition time for a first order loop is was first explored by Richman [3] for color television receivers. Tausworth [4] developed an estimate of the acquisition of the first order loop as

$$t_{acq} \approx \frac{2}{\sqrt{2\ P\ K_o\ K_d \cos(\varepsilon_{ss})}} \log_e\left(\frac{2}{\gamma_{lock}}\right)$$

where $\varepsilon_{ss}$ is the steady state phase error from Equation 2-18 4-8

$\gamma_{lock}$ is the specified deviation from the steady state error

For most engineering design and analysis, Gardner [2] provides the rule-of-thumb acquisition time for a first order loop as

$$t_{acq} \approx \frac{3}{\sqrt{2P}K_o K_f K_d}\text{sec} \qquad 4\text{-}9$$

This equation is only applicable if the offset frequency is less than the pull-in limit of Equation 4-7. In fact, the first order loop will only acquire if the condition of Equation 4-7 is true. Figure 4.3 shows a first order loop attempting to acquire a frequency offset just greater than $f_p$. It appears to track the input signal for a while, and then suffers a cycle slip where the error voltage (output of the phase detector) changes sign almost instantaneously.

## 4.2 Second Order Loop Acquisition

If we were to integrate the error waveform of Figure 4.3, we would obtain a non-zero value, because the waveform is not symmetric [2]. This

integrated error voltage could be used to provide a DC offset term to the VCO, which would subsequently assist acquisition. This integral of the error waveform is actually used in a second order loop.

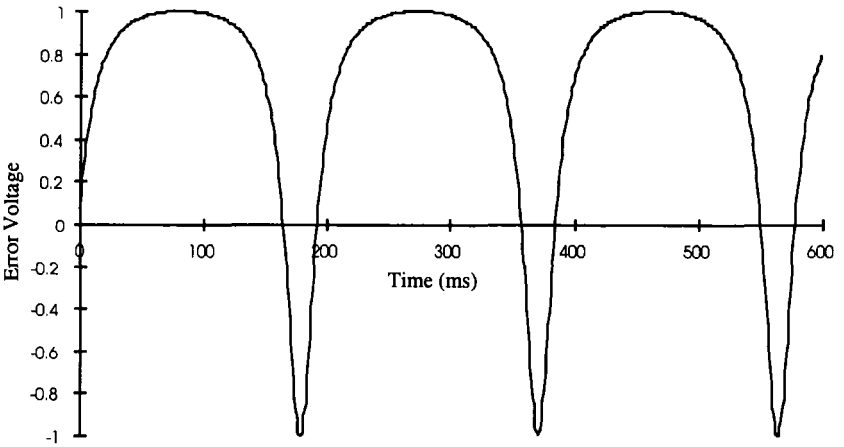


Figure 4.3 First Order Loop With Frequency Offset

Because of the advantages of the active filter for the second order loop, we will only derive the acquisition equations for this configuration. The other second order derivations are saved for the problems. Figure 4.4 shows the block diagram of the second order phase-locked loop during acquisition. As with the first order loop, we have included the Sin[.] function within the phase detector. If not for this non-linearity, the phase-locked loop acquisition would be identical to classical control loop theory, which was the linearized development in Chapter 2. The filter in Figure 4.4 is the time domain representation of the active filter's s-domain transfer function of $F(s)=\frac{\tau_2 s+1}{\tau_1 s}$. (Discussed in Chapter 2.)

The output of the loop filter can be written as

$$\gamma(t)=\frac{\tau_2}{\tau_1}\sqrt{2P}K_d\,Sin[\theta_e(t)]+\frac{\sqrt{2P}K_d}{\tau_1}\int Sin[\theta_e(t)]dt \qquad 4\text{-}10$$

The VCO has a nominal center frequency (output frequency with zero volts input) of $f_v$. The output of the VCO is

$$\theta_o(t) = K_o \int \gamma(t) dt + 2\pi f_v t \qquad 4\text{-}11$$

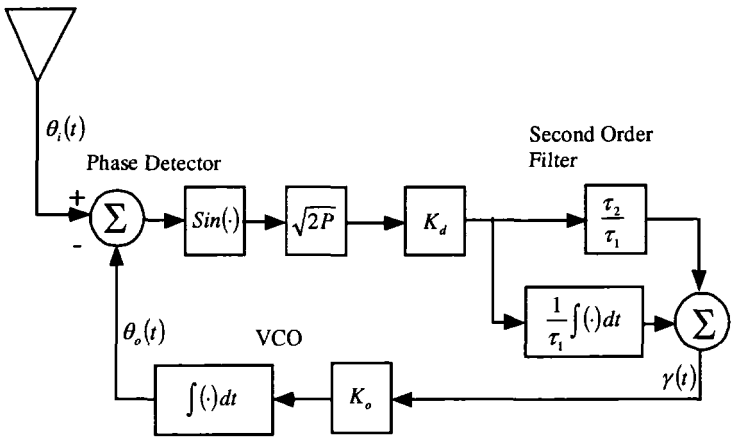


Figure 4.4 Non-Linear Representation of the Second Order Loop

From the observation that $\theta_e(t) = \theta_i(t) - \theta_0(t)$, and then using the results of Equations 4-10 and 4-11, we can write the non-linear equation for $\theta_e(t)$,

$$\theta_e(t) = \theta_i(t) - K_o \int \left\{ \begin{array}{l} \frac{\tau_2}{\tau_1}\sqrt{2P}K_d\, Sin[\theta_e(t)] \\ + \frac{\sqrt{2P}K_d}{\tau_1}\int Sin[\theta_e(\tau)]d\tau \end{array} \right\} dt - 2\pi f_v t \qquad 4\text{-}12$$

This result for $\theta_e(t)$ must be differentiated twice in order to remove both integrals on the right-hand side of Equation 4-12. As we perform this differentiation, we assume that the input signal $\theta_i(t)$ is at most a constant frequency with static phase offset. In other words, the second derivative of $\theta_i(t)$ is zero. Also, the second derivative of $2\pi f_v t$ is zero, which eliminates these two terms.

$$\theta_e''(t) + K_o \frac{\tau_2 \sqrt{2P} K_d}{\tau_1} Cos[\theta_e(t)]\theta_e'(t) + \frac{K_o \sqrt{2P} K_d}{\tau_1} Sin[\theta_e(\tau)] = 0 \qquad 4\text{-}13$$

Equation 4-13 can be rewritten with traditional servomechanism terminology as [1]

$$\theta_e''(t) + 2\zeta w_n Cos[\theta_e(t)]\theta_e'(t) + w_n^2 Sin[\theta_e(\tau)] = 0 \qquad 4\text{-}14$$

In Equation 4-14, we have made the following substitutions:

$$w_n^2 = \frac{K_o K_d \sqrt{2P}}{\tau_1} \qquad 4\text{-}15$$

$$\zeta = \sqrt{\frac{\tau_2^2 K_o K_d \sqrt{2P}}{4\tau_1}} \qquad 4\text{-}16$$

Viterbi [1] defines $\tau = 2\zeta w_n t$, which normalizes the differential equation for graphing. With this substitution, Equation 4-14 is rewritten as

$$4\zeta^2 w_n^2 \theta_e''(\tau) + 4\zeta^2 w_n^2 Cos[\theta_e(\tau)]\theta_e'(\tau) + w_n^2 Sin[\theta_e(\tau)] = 0 \qquad 4\text{-}17$$

(Note in Equation 4-17 that the variable t has been replaced with $\tau$.) Division of the coefficient for $\theta_e''(\tau)$, $4\zeta^2 w_n^2$ simplifies Equation 4-17, and we obtain

$$\ddot{\theta}_e(\tau) + \dot{\theta}_e(\tau) Cos[\theta_e(\tau)] + \frac{1}{4\zeta^2} Sin[\theta_e(\tau)] = 0 \qquad 4\text{-}18$$

Equation 4-18 is a second order non-linear differential equation, and must solved with numerical techniques. Recall to solve a second order differential equation such as Equation 4-18, two initial parameters are necessary to specify a particular solution [10]. In Figure 4.5, we graph both $\theta_e(\tau)$ and $\dot{\theta}_e(\tau)$ as functions of $\tau$ for the specific set of initial conditions, $\theta_e(0) = 0.5$

and $\dot{\theta}_e(0) = 0$. In Figure 4.5, both $\theta_e(\tau)$ and $\dot{\theta}_e(\tau)$ begin at the specified initial conditions, and eventually find a stable null with both variables equal to zero. This phase trajectory corresponds to the normal acquisition of a phase-locked loop.

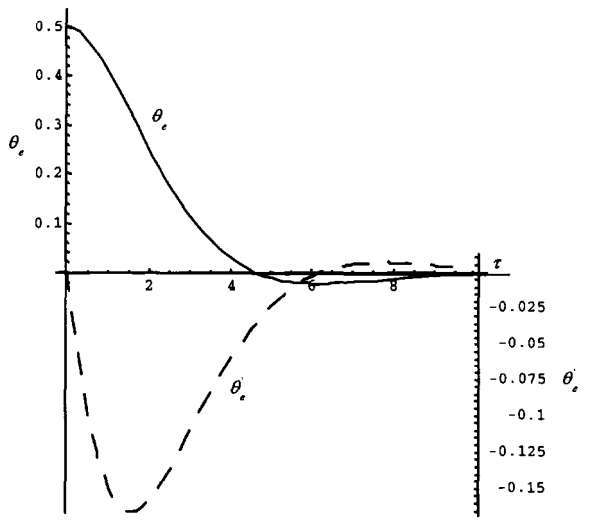


Figure 4.5 State Variables in Acquisition for Second Order Loop

Figure 4.6 is a parametric plot with coordinates, $(\dot{\theta}_e(\tau), \theta_e(\tau))$. (Again, this plot is for a specific phase acquisition with the specific initial conditions of Figure 4.5.)

The parametric plot of Figure 4.6 allows insight as to how the phase-locked loop simultaneously acquires frequency and phase. (Recall $\dot{\theta}_e(\tau)$ represents the frequency error of the loop.) The trajectory for this particular graph begins at the coordinate pair, $(\theta_e(0) = 3.14, \dot{\theta}_e(0) = 0)$, and completes at $(\theta_e(0) = 0, \dot{\theta}_e(0) = 0)$. It is tempting to think the trajectory is from left-to-right, but in Figure 4.6, it moves from right-to-left.

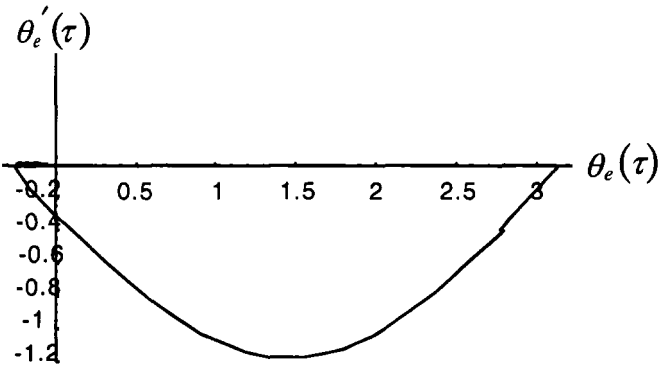


Figure 4.6 Second Order PLL Acquisition of Frequency and Phase

Figures 4.5 and 4.6 represent the nonlinear acquisition process for a specific set of initial conditions. By combining a set of plots similar to Figure 4.6, we obtain the phase plane plots shown in Figures 4.7-4.8. These are for two different loop damping factors. For additional phase plane plots, consult Viterbi [1].

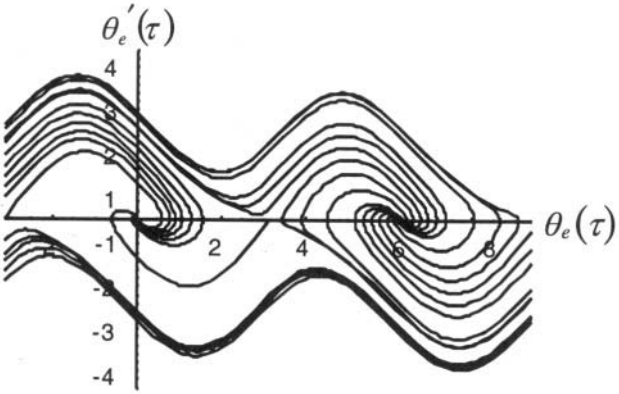


Figure 4.7 Second Order Phase Plane with $\zeta = 0.707$

Typically the phase plane plots are not used in detailed design of phase-locked loops. They are more useful philosophically in understanding the acquisition process. However, the phase plane plots can provide insight to the operation of the phase-locked loop with an initial frequency offset. (Usually, the initial conditions are random variables from acquisition to acquisition, so almost any phase plane trajectory is possible on any given

acquisition.) The single phase plane trajectory of Figure 4.6 illustrates that the instantaneous frequency error may actually increase as the loop decreases the static phase error.

Gardner and Viterbi [1,2,5] state higher order loops have the same lock-in range for acquisition without cycle slips. A second order loop can theoretically acquire any frequency offset if saturation does not occur in the loop components. Gardner gives the frequency acquisition time of a second order loop as

$$T_p \approx \frac{4.2(\Delta f)^2}{B_L^{\ 3}} \qquad 4\text{-}19$$

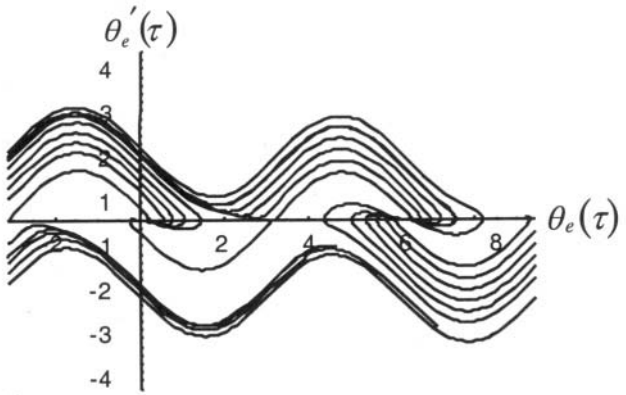


Figure 4.8 Second Order Phase Plane with $\zeta = 1.414$

Figure 4.9 shows a second order loop acquiring the same frequency offset as the first order phase-locked loop in Figure 4.3. The loop noise bandwidths and other parameters are the same with the exception of the second order loop filter's integrator. The information contained in the non-symmetric waveform allows the second order loop to acquire a frequency offset that the first order cannot.

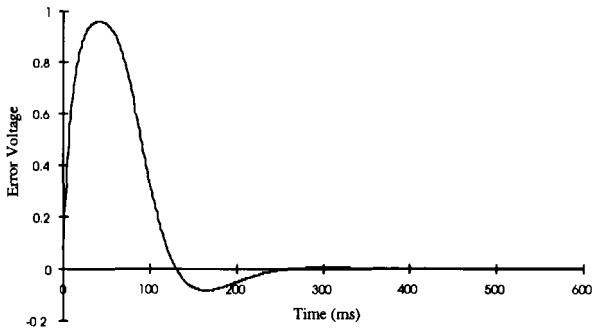


Figure 4.9 Second Order Loop Acquiring With a Frequency Offset

As a verification of Equation 4-19, the frequency offset for Figure 4.9 was 12 Hz, with a loop bandwidth of 17 Hz. Equation 4-19 suggests a frequency acquisition time of 123 ms, which is consistent with Figure 4.19. The frequency acquisition time is the time that the loop requires to eliminate the frequency offset. A phase acquisition time is then incurred as the loop adjusts phase for a phase-locked condition.

## *Example 4.1*

We want to design a PLL with a specification on acquisition time. Compute the necessary filter coefficients for an active second order filter with the following parameters and specifications:

VCO: $K_O$ = 10 MHz/Volt, Phase Detector: Kd = 1/2 Volt/Radian, Input Power: 20 dBm (1mW), Total Acquisition Time 70 ms ,Damping Factor (Specified) 0.707

Review the phase step acquisition graphs of the second order phase-locked loop in Figure 2.6. For this design, we assume that the normalized time, $w_n t_{phase} = 4.0$ will provide sufficient phase accuracy to declare phase-lock. (We want to emphasize this definition is arbitrary. In this case, it corresponds to the error less than 10%. Depending on the application, it may be necessary to increase or decrease the accuracy requirement, which then changes the acquisition time.

We can write an equation for the total acquisition time based upon this assumption [8]

$$t_{phase} + t_{freq} = \frac{4.0}{w_n} + \frac{4.2 \quad (\Delta f)^2}{B_L^3} \qquad 4\text{-}20$$

This is not sufficient, because we need to express the noise bandwidth in terms of the natural frequency, $w_n$. Using the noise bandwidth table of Figure 3.23,we substitute in the noise bandwidth for the active second order loop into Equation 4-20.

$$t_{phase} + t_{freq} = \frac{4.0}{w_n} + \frac{4.2 \ (\Delta f)^2}{\left\{\frac{w_n}{2}\left(\zeta + \frac{1}{4\ \zeta}\right)\right\}^3} \qquad 4\text{-}21$$

With the appropriate substitutions for the loop gains and damping factor, we obtain

$$t_{phase} + t_{freq} = \frac{4.0}{w_n} + \frac{4.2 \ \left(100\times10^3\right)^2}{\left\{\frac{w_n}{2}\left(\frac{1}{\sqrt{2}} + \frac{\sqrt{2}}{4}\right)\right\}^3} = 70 \ \ ms \qquad 4\text{-}22$$

Solving for $w_n$, we obtain $w_n = 15923.8$ rad/sec. After obtaining$w_n$, we can obtain the active filter coefficients in a similar procedure to Example 2.1. Our active filter transfer function is

$$F(s) = \frac{8.888\times10^{-5}s + 1}{0.392s} \qquad 4\text{-}23$$

The simulated performance of the phase-locked loop is shown in Figure 4.10. Because of the long acquisition time, we have only shown the last 4 msec of the simulation. The acquisition time of the simulation matches well with the designed performance.

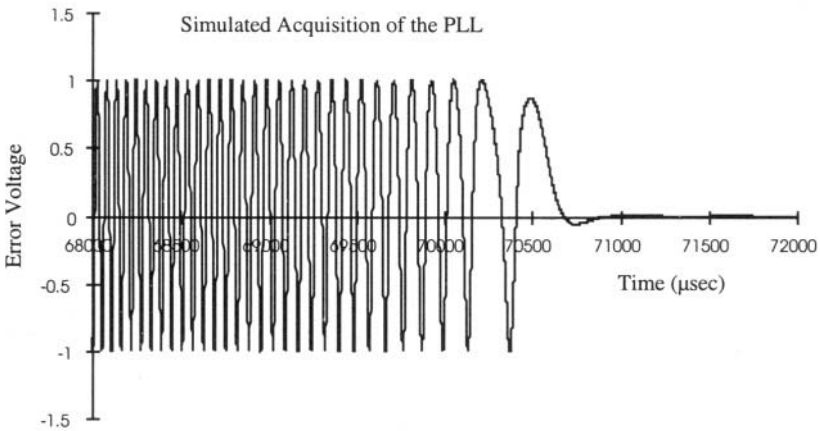


Figure 4.10 Phase-Locked Loop Acquisition of Example 4.1

## 4.3 Acquisition in Noise

In Chapter 3, we defined the noise bandwidths of the different analog phase-locked loops. These were based upon linear assumption, $\sigma^2_{n\theta_o} = \int_{-\infty}^{\infty} S_{n\theta_e}(f)|H(f)|^2 \, df$. At low signal-to-noise ratios, this is a poor approximation, and we wish to provide some analysis that will better describe loop performance.

Fundamental to understanding the stochastic process of acquisition with noise, is the probability density function of the output phase error. Using Fokker-Planck Techniques, Viterbi derived the probability density function of the first order loop as [5]

$$f_\phi(\phi) = \frac{\exp(\rho Cos[\phi])}{2\pi I_0(\rho)}, |\phi| \le \pi \qquad 4\text{-}24$$

In Equation 4-24, $\rho$ is the signal-to-noise ratio within the PLL. $I_0$, of course, is the first-order Bessel function. (Viterbi credits Tikhonov [6] for the first derivation of Equation 4-24.) From Chapter 3,

$$SNR_i \equiv \rho = \frac{P}{N_o B_L} \qquad 4\text{-}25$$

The derivation of the probability density function for the active second order loop has not been obtained. However, Viterbi shows [5] if

$$\frac{1}{\tau_2} << \frac{\tau_2}{\tau_1} K_o K_d \sqrt{2P} \qquad 4\text{-}26$$

Then the probability density function for the second order loop can be approximated by Equation 4-24. At large signal-to-noise ratios, the probability density function approaches a $N\sim(0, \sigma_\phi^2)$ Gaussian density function, which provides some insight to the operation of the phase-locked loop in noise. (The approach of Chapter 3, with the white noise and bandpass filters is thus justified.)

Using Equation 4-24, the variance of the loop's phase error may be computed as [5]

$$\sigma_\phi^2 = \int \phi^2 f_\phi(\phi) d\phi \qquad 4\text{-}27$$

$$\sigma_\phi^2 = \frac{\pi^2}{3} + 4\sum_{n=1}^{\infty} \frac{(-1)^n I_n(\rho)}{n^2 I_0(\rho)} \qquad 4\text{-}28$$

For large signal-to-noise ratios, Equation 4-27 can be approximated by

$$\sigma_\phi^2 \approx \frac{1}{\rho}, \rho >> 1 \qquad 4\text{-}29$$

Figure 4.11 shows the theoretical (Equation 4-28) phase error variance of the first order loop. The linear approximation is also shown. The phase variance of digital simulations for first order and second order loops are also graphed in Figure 4.11. We find that Figure 4.11, Equation 4-29 suggests that the loop performance should be better than it actually is. In order to develop Equation 4-24, and ultimately, Equation 4-28, the phase error $\phi$ is defined **modulo-2π**. (This is done to provide statistical stationarity.) At low signal-to-noise ratios, bursts of cycle slips may be occurring, and $\phi$ is actually increasing much more than indicated by the **modulo-2π** representation.

Early in phase-locked loop analysis, it was believed there was a signal-to-noise threshold below which acquisition or tracking could not take place. Subsequent analysis and experimentation has shown this to be inaccurate, as well-designed loops can acquire with $\rho = 0\ dB$ [2]. Most phase detectors are limited to $\pm\pi/2$, so we can visualize problems arising in PLLs when the probability of phase error becomes significant for $\phi \geq \pi/2$.

By integrating the probability density function in Equation 4-24, we can compute the probability that the phase error, $|\phi| \geq \pi/2$. Figure 4.12 shows the probabilities at the different signal-to-noise ratios.

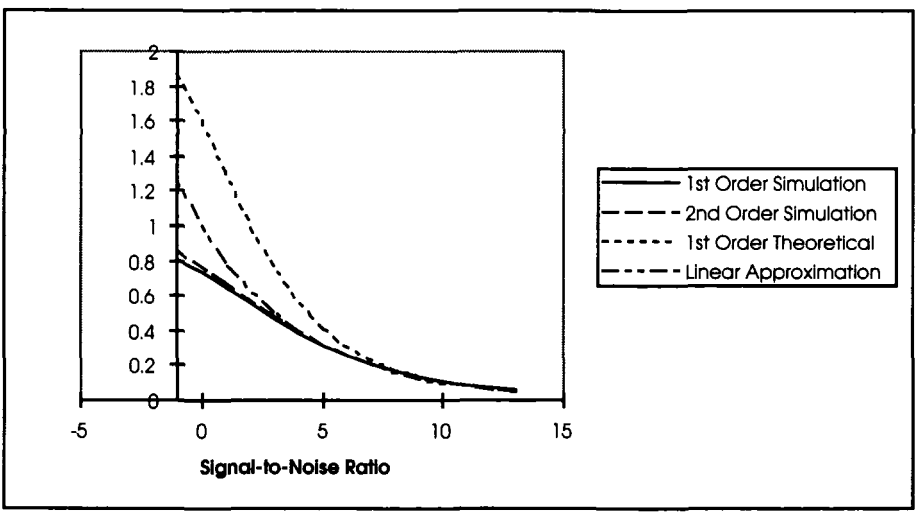


Figure 4.11 First Order PLL Phase Variance

These probabilities provide two insights. First, if the loop is under stress and the static phase error is not zero, (first order with frequency step or second order with frequency ramp), then the noise performance is going to be degraded. Second, the loop is going to have significantly reduced output phase variance for $\rho \geq 6\ dB$. (Coincidentally, the early accepted threshold for phase-locked loop acquisition and tracking was 6 dB.)

| S/N (dB) | Probability (%) |
|---|---|
| 0 | 50 |
| 1 | 21.9508 |
| 2 | 7.50469 |
| 3 | 2.37776 |
| 4 | 0.755941 |
| 5 | 0.24588 |
| 6 | 8.18E-02 |
| 7 | 2.77E-02 |
| 8 | 9.48E-03 |
| 9 | 3.28E-03 |
| 10 | 1.14E-03 |

Figure 4.12 Probability that $|\phi| \geq \pi/2$

A cycle slip is when the output phase error rotates through $2\pi$ after initially starting at zero. For a first order loop, the mean time to slip is [5]

$$T_{AV} = \frac{\pi^2 \rho I_0^2(\rho)}{2B_L} \qquad 4\text{-}30$$

Figure 4.13 graphs the normalized mean time to slip for the first order loop. Note that above a 5 dB signal-to-noise ratio, the time to cycle slip increases significantly with increasing signal-to-noise ratio. Because the output variance of Figure 4.11 is **modulo-2π,** at the low signal to noise ratios, it does not represent accurately the tracking of the loops.

Assuming an exponential probability density function, the cumulative probability function can be written as

$$P(T) = 1 - e^{-\frac{T}{T_{AV}}} \qquad 4\text{-}31$$

T is the time to slip, beginning with zero phase error. $T_{AV}$ is the mean-time-to-failure defined in Equation 4-30.

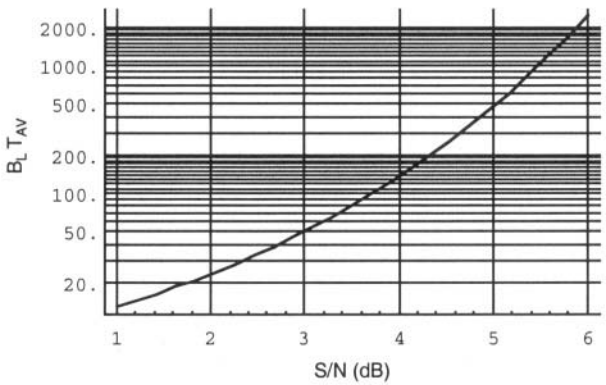


Figure 4.13 Normalized Mean-Time to Slip for First Order Loop

Asched and Meyr [9] analyze cycle slips of a second order loop using state variables. They conclude that the capacitor voltage in the second order loop filter has a primary affect on whether cycle slips occur in bursts. Higher values of damping factors produce an exponential distribution such as Equation 4-31, whereas lower damping factors deviate significantly from an exponential distribution of time between cycle slips. With an exponential distribution, the individual cycle slips are independent and thus do not appear in clusters. For $\frac{S}{N_0 B_L} \geq 0\ dB$, Equation 4-30 can be used to estimate the time between cycle slips for the second order active loop [2].

Viterbi [1] investigates third order tracking behavior similar to the second order loop. However, phase-plane techniques shown above are not applicable because there are three initial conditions corresponding to phase, frequency, and Doppler. A single three-dimensional plot could be produced similar to Figure 4.5, but extending it to include multiple initial conditions would not be practical. Viterbi concludes in moderate levels of Doppler, there is little difference between the third order and second order tracking [11].

More recently, Welti, et al. [7] have more recent research on third-order loop's mean time to lose lock. Although there are several accompanying assumptions, they conclude that higher damping factors $(\zeta > 0.9)$ significantly improve the mean time to lose lock.

## 4.4 Frequency Sweeping

As shown in Equation 4-19, the pull-in for a phase-locked loop can be very slow if $\Delta f$ is large relative to the loop bandwidth $B_L$. Frequency sweeping can improve the acquisition time, but it can degrade the loop performance in noise or other conditions, because the loop itself is under stress with a frequency ramp [13-14].

Gardner [2] suggests a method of injecting a slewing current directly into the loop filter's integrator for sweeping the phase-locked loop in acquisition. A different method is shown in Figure 4.14 [13].

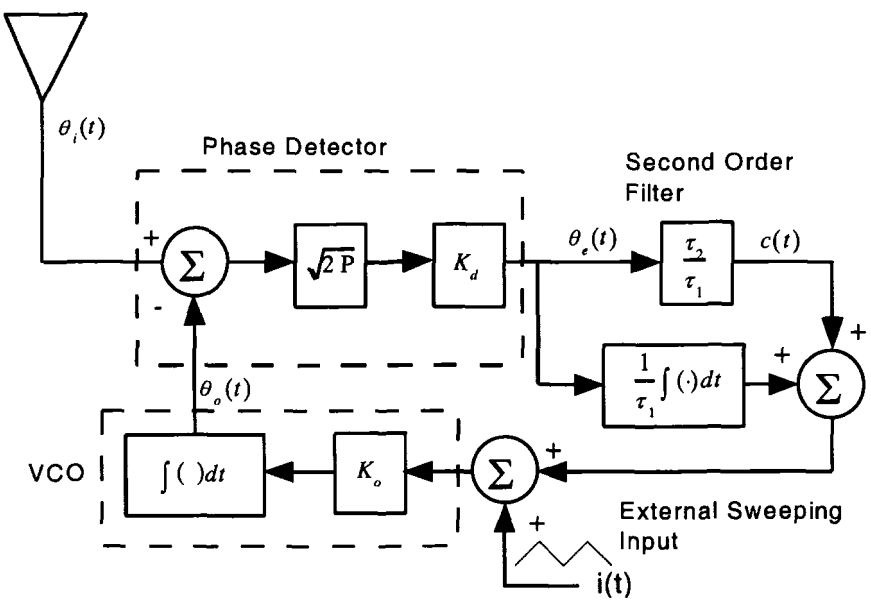


Figure 4.14 PLL With External Sweep for Acquisition

In Figure 4.14, the external sweeping input, i(t), is moving the VCO through the desired acquisition band. When the signal is acquired, the sweeping must be terminated and the sweep voltage maintained at $i(t) = i(T_L)$, where $T_L$ is the time the lock was obtained. If the sweep voltage is not terminated, the sweeping circuit will sweep the VCO right out of phase-lock. If the sweep voltage is not maintained, the VCO will lose lock immediately, because the sweep voltage has not been added to the loop filter's accumulator. Whether the sweep is implemented with the summing junction into the VCO or a charge injected into the integrator, a method of

determining lock is needed to end the external sweep input. A lock detector such as the quadrature lock detector presented in Chapter 11 provides a coherent lock detection.

The maximum sweep rate for the second order active phase-locked loop is [2]

$$\Delta\dot{\omega}_{Max} = \omega_n^2\left[1-\frac{1}{\sqrt{SNR_L}}\right] \qquad 4\text{-}32$$

In Equation 4-32, note the dependence on the signal-to-noise ratio within the loop. Frazier and Page's study [14] also shows a difference in maximum sweep rate in noise for different damping factors, $\zeta$. As an example, for 90% acquisition probability, at a $SNR_L$=9 dB, a loop with a damping ratio of 0.5 has approximately a 6% higher sweep rate than a loop with a damping ratio of 0.85. The percentage is higher at $SNR_L$=13 dB, as the loops approach the noise-less case.

## 4.5 Acquisition Summary

We conclude with a summary of the different acquisition definitions for a phase-locked loop. As discussed in [12], these definitions specify the performance of a phase-locked loop in different acquisition conditions. In general, a relationship for the definitions can be written as

$$\Delta\omega_L < \Delta\omega_{po} < \Delta\omega_p < \Delta\omega_H \qquad 4\text{-}33$$

$\Delta\omega_L$ is the frequency range in which the phase-locked loop will lock within a single cycle slip. As discussed in Equation 4-7, the frequency range is limited by the DC gain of the phase-locked loop. For the active second order filter, the lock range is

$$\Delta\omega_L \approx 2\zeta\omega_n \qquad 4\text{-}33$$

$\Delta\omega_{po}$ is defined as the maximum frequency step that can be applied to a phase-locked loop without it losing lock. (An active filter second order loop can theoretically always regain lock, but if the frequency step is larger than

$\Delta\omega_{po}$, there may be several cycle slips before the loop regains lock.) A computer simulation approximation exists [2,12],

$$\Delta\omega_{po} \approx 1.8\omega_n(\zeta + 1) \qquad 4\text{-}34$$

With such a large frequency step, the second order phase-locked loop exhibits some large transients that may be unacceptable in some applications. A more conservative approximation might be [12]

$$\Delta\omega_{po} \approx 2.0\omega_n \qquad 4\text{-}33$$

Note this parameter is important in applications that utilize frequency steps such as frequency-hopping spread spectrum receivers or CPM receivers utilizing frequency steps. Although in some instances, the phase-locked loop might rapidly recover, the resulting frequency spectrum could exhibit objectionable far-out degradation.

$\Delta\omega_p$ is the frequency range in which the phase-locked loop will eventually pull the VCO into lock. For a second order loop, this is infinite.

$\Delta\omega_H$ is the frequency range over which the phase-locked loop can maintain phase lock. For the second order loop this is theoretically infinite.

## 4.6 Summary of Analog Phase-Locked Loop Design Equations

We conclude this chapter with a summary of the different design equations. This is intended for the designer, who needs a convenient list of the pertinent design equations.

Transfer Function

$$H_o(s) = \frac{\sqrt{2P}\,K_o K_d K_f}{s + \sqrt{2P}\,K_o K_d K_f}$$

Noise Bandwidth

$$B_L = \frac{\sqrt{2P}\,K_o K_d K}{4}$$

Frequency Pull-in Limit

$$f_p \quad \frac{\sqrt{2P}\,K_o K_f K_d}{2\pi}$$

Frequency Acquisition Time

$$t_{acq} \quad \frac{3}{\sqrt{2P}\,K_o K_f K_d} \text{ sec}$$

Time Between Cycle Slips

$$T_{AV} = \frac{\pi^2 \rho I_0^2(\rho)}{2B_L}$$

Phase Step Response

$$\theta_e(t) = \sqrt{2P}\,K_d \Delta\theta\, e^{-\sqrt{2P}\,K_o K_d K_f t} u(t)$$

Frequency Step Response

$$\theta_e(t) = \frac{\sqrt{2P}\,K_d 2\pi f_\Delta}{\sqrt{2P}\,K_o K_d K_f} \left\{ - e^{-\sqrt{2P}\,K_o K_d K_f t} \right\} u(t)$$

Frequency Ramp Response

$$\theta_e(t) = \frac{\sqrt{2P}\,K_d 2d\Delta\theta}{\left(\sqrt{2P}\,K_o K_d K_f\right)^2} \left\{ \left(\sqrt{2P}\,K_o K_d K_f\right) + e^{-\sqrt{2P}\,K_o K_d K_f t} - 1 \right\} u(t)$$

Figure 4.15 Design Equations for a First Order PLL

Transfer Function

$$H_2(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2}$$

Noise Bandwidth

$$B_L = \frac{w_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

Frequency Pull-in Limit

$$f_p \le \infty \quad \text{With Cycle Slips}$$

Frequency Acquisition Time

$$T_p \approx \frac{4.2(\Delta f)^2}{B_L^3}$$

Frequency Pull-Out Limit

$$\Delta f_p \approx \frac{1.8}{2\pi}(\zeta + 1)$$

Time Between Cycle Slips

$$T_{AV} \approx \frac{\pi^2 \rho I_0^2(\rho)}{2 B_L}$$

Phase Step Response

$$\theta_e(t) = \Delta\theta\sqrt{2P}\, K_d e^{-\zeta w_n t}\left(\cos\left(w_n\sqrt{1-\zeta^2}\,t\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(w_n\sqrt{1-\zeta^2}\,t\right)\right) \quad \zeta < 1$$

$$\theta_e(t) = \Delta\theta\sqrt{2P}\, K_d e^{-\zeta w_n t}(1 - w_n t) \quad \zeta = 1$$

$$\theta_e(t) = \Delta\theta\sqrt{2P}\, K_d e^{-\zeta w_n t}\left(\cosh\left(w_n\sqrt{\zeta^2-1}\,t\right) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right)\right) \quad \zeta > 1$$

Frequency Step Response

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-\zeta w_n t}\frac{\sin\left(w_n\sqrt{1-\zeta^2}\,t\right)}{\sqrt{1-\zeta^2}} \quad \zeta < 1$$

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-w_n t}\, w_n\, t \quad \zeta = 1$$

$$\theta_e(t) = \frac{2\pi f_\Delta}{w_n} e^{-\zeta w_n t}\frac{\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right)}{\sqrt{\zeta^2-1}} \quad \zeta > 1$$

Frequency Ramp Response

$$\theta_e(t) = 2\frac{2\pi\dot{f}}{w_n^2} - 2\frac{2\pi\dot{f}}{w_n^2} e^{-\zeta w_n t}\left(\cos\left(w_n\sqrt{1-\zeta^2}\,t\right) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(w_n\sqrt{1-\zeta^2}\,t\right)\right), \zeta < 1$$

$$\theta_e(t) = 2\frac{2\pi\dot{f}}{w_n^2} - 2\frac{2\pi\dot{f}}{w_n^2} e^{-w_n t}\, w_n t, \zeta = 1$$

$$\theta_e(t) = 2\frac{2\pi\dot{f}}{w_n^2} - 2\frac{2\pi\dot{f}}{w_n^2} e^{-\zeta w_n t}\left(\cosh\left(w_n\sqrt{\zeta^2-1}\,t\right) + \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(w_n\sqrt{\zeta^2-1}\,t\right)\right), \zeta > 1$$

Figure 4.16 Design Equations for Second Order Active Filter PLL

## 4.7 References

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## 4.8 Problems

4.1 Plot the phase plane trajectory (similar to Figure 4.2) for a first-order phase-locked loop with $\sqrt{2P}K_o K_f K_d = 20$. The static frequency offset is $\Omega = \theta_i'(t) - 2\pi f_v = 8$.

4.2 Derive the nonlinear acquisition equation (Equation 4-12) for the second order phase-locked loop with a filter of the form, $F(s) = \dfrac{1+\tau_2 s}{1+\tau_1 s}$.

4.3 Design a first order loop filter that meets the following requirements: VCO: $K_O$ = 10 KHz/Volt, Phase Detector: Kd = 1/2 Volt/Radian Input Power = 200mW, error deviation = 0.01
Frequency Acquisition < 400 μ sec with a 300 Hz frequency offset

4.4 Design a second order loop filter that meets the following requirements: VCO: $K_O$ = 1000 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian Input Power = 10mW, Loop Damping Factor = 0.707
Total Acquisition < 20 msec with a frequency offset of 300 Hz. What is the noise bandwidth of the design?

4.5 Design a second order loop filter that meets the following requirements: VCO: $K_O$ = 1000 Hz/Volt, Phase Detector: Kd = 1/2 Volt/Radian Input Power = 10mW, Loop Damping Factor = 0.707
Total Acquisition < 20 msec with a frequency offset of 15 Hz. What is the noise bandwidth of the design?

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# 5

# Digital Transforms

Chapters 2-4 presented the analysis and design techniques for analog phase-locked loops. In this chapter we will review digital transform techniques so that we develop a similar analysis for digital phase-locked loops.

## 5.1 The Pulse Transform

One of the first digital phase-locked loop configurations was a sampled version of an analog phase-locked loop [1]. This architecture is still used in modems and synthesizers. Other applications include receivers for pulsed $\theta_i(t)$ signals such as radar transmissions [9]. In Figure 5.1, we have taken a conventional analog architecture and added a sampler as our first example of a digital phase-locked loop.

Figure 5.1 is an architecture common in a receiver's frequency synthesizer. The primary difference between the configuration above and the complete analog phase-locked loop in Figure 2.1 is the digital phase detector which has a sampler and zero-order hold. We have replaced the $1/s$ implicit VCO transfer function with $\mathbf{V(s)}$ because the derivations are more general if we use V(s). We will discuss the zero-order hold's transfer function, $G_{zoh}(s)$, in Example 5.1.

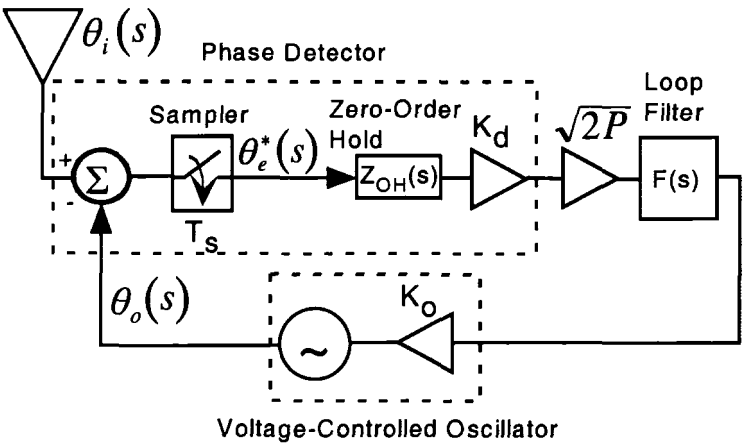


Figure 5.1 Phase-Locked Loop With Sampled Phase Detector

In Figure 5.1, there is a "star" superscript for $\theta_e^*(s)$, denoting the signal is sampled. In the communications literature, we typically assume the "star" superscript implies a complex conjugate, but the linear control literature uses this notation for a sampled function. An ideal sampler can be expressed as

$$\theta^*(t) = \sum_{k=-\infty}^{\infty} \theta(kT)\delta(t - kT_s) \qquad 5\text{-}1$$

where $T_s$ is the time interval between samples

By taking the Laplace transform of Equation 5-1, we obtain the sampled Laplace transform, sometimes called the pulse transform [2,6,8]

$$\theta^*(s) = \int_{t=0}^{\infty} \sum_{k=-\infty}^{\infty} \theta(kT_s)\delta(t - kT_s)e^{-st}\,dt \qquad 5\text{-}2$$

This is awkward and not too useful, so we simplify with the sifting property of the delta function,

$$\theta^*(s) = \sum_{k=-\infty}^{\infty} \theta(kT_s)e^{-skT_s} \qquad 5\text{-}3$$

This shows that the pulse transform is an infinite sum of the continuous transforms, with each weighted by a complex phasor. An additional property

of the impulse transform may be obtained by recognizing that $\theta(t)$ is multiplied with a periodic sequence in Equation 5-2. We can write the periodic sequence as a Fourier Series [1],

$$\sum_{k=-\infty}^{\infty}\delta(t-kT_s)=\sum_{n=-\infty}^{\infty}C_n\,\mathrm{Exp}\left(\frac{j2\pi nt}{T_s}\right)$$
$$\text{where } C_n=\frac{1}{T_s}\int_{T_s}\delta(t)\mathrm{Exp}\left(\frac{-j2\pi nt}{T_s}\right)dt, Exp(x)=e^x \qquad 5\text{-}4$$

The Fourier Series coefficients are all identical, and $C_n = 1/T$. The periodic sequence is then written as

$$\sum_{k=-\infty}^{\infty}\delta(t-kT_s)=\frac{1}{T_s}\sum_{n=-\infty}^{\infty}\mathrm{Exp}\left(\frac{j2\pi nt}{T_s}\right) \qquad 5\text{-}5$$

Substituting Equation 5-5 into Equation 5-2 yields

$$\theta^*(s)=\frac{1}{T_s}\sum_{n=-\infty}^{\infty}\int_{t=0}^{\infty}\theta(t)\,\mathrm{Exp}\left(\frac{j2\pi nt}{T_s}\right)\mathrm{Exp}(-st)\,dt \qquad 5\text{-}6$$

Combining the exponential terms simplifies the expression

$$\theta^*(s)=\frac{1}{T}\sum_{n=-\infty}^{\infty}\int_{t=0}^{\infty}\theta(t)\,\mathrm{Exp}\left(-t\left(s-\frac{j2\pi n}{T_s}\right)\right)dt \qquad 5\text{-}7$$

The integral in Equation 5-7 represents the Laplace transform of $\theta(t)$, and can be rewritten as

$$\theta^*(s)=\frac{1}{T_s}\sum_{n=-\infty}^{\infty}\theta\left(s-\frac{j2\pi n}{T_s}\right) \qquad 5\text{-}8$$

Recognizing that the inverse of the sampling period, $T_s$, is the sampling frequency, $f_s$, we can express the frequency replicas in Equation 5-8 as multiples of the sampling frequency.

$$\theta^*(s) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \theta(s - j2\pi n f_s) \qquad 5\text{-}9$$

This is a fundamental result, because it shows the ideal sampler is a harmonic generator. Each of the replicated frequency spectrums all have the same amplitude as shown mathematically by the relationship between $\theta^*(s)$ and $\theta(s)$.

A flat-top sampler which has finite pulse widths has a roll-off in the amplitudes of the harmonic replicas [2]. Although real-world samplers all have finite pulse widths, we will overlook this complicating factor in subsequent derivations.

Because the ideal sampler replicates the baseband (dc) signal at frequencies $\pm k f_s$, the baseband signal can be recovered with a bandpass rather than lowpass filter. We will use exploit this property for our IF sampling phase-locked loops to be discussed later.

Equation 5-9 also shows the importance of meeting Nyquist sampling requirements. Figure 5.2 illustrates a periodic spectrum generated by sampling a simple baseband signal as indicated with Equation 5-9. The baseband spectrum is centered at 0 Hz and has a bandwidth of $\pm$ B Hz. Equation 5-9 states that this spectrum will also appear centered at frequencies of $\pm$ $kf_s$, as demonstrated in Figure 5.2. If the sampling frequency, $f_s$, is not high enough, the periodic spectrums will overlap each other, which is termed aliasing. In terms of Figure 5.2, we can state the sampling theorem as

$$f_s \geq 2B \qquad 5\text{-}10$$

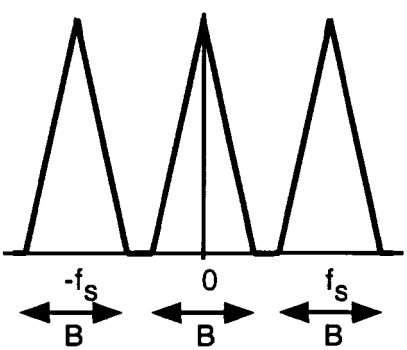


Figure 5.2 Replicated Spectrum

We have one final property of the pulse or sampled Laplace transform to discuss. Since the summation limits in Equation 5-9 are $\pm\infty$ [2], we can write the sampled signal that has already been sampled by

$$\theta^{*}(s+j2\pi m f_s)=\frac{1}{T}\sum_{n=-\infty}^{\infty}\theta(s-j2\pi n f_s-j2\pi m f) \qquad 5\text{-}11$$

| | | |
|---|---|---|
| Definition of the sampled Laplace transform | $F^{*}(s)=\sum_{k=0}^{\infty}f(kT)e^{-ksT}$ | 5-12 |
| Laplace transform, F(s) has k simple poles | $F^{*}(s)=\sum_{n=1}^{k}\frac{N(\chi_n)}{D'(\chi_n)}\frac{1}{1-e^{-T(s-\chi_n)}}$<br>$where F(\chi)=\frac{N(\chi)}{D(\chi)}$<br>$D'(\chi_n)=\left.\frac{dD(\chi)}{d\chi}\right\|_{\chi=\chi_n}$ | 5-13 |
| Laplace transform, F(s) has k poles with multiplicity mn≥1 | $F^{*}(s)=\sum_{n=1}^{k}\sum_{i=1}^{mn}\frac{-1^{mn-i}K_{ni}}{(mn-1)!}\frac{\partial^{mn-i}}{\partial s^{mn-i}}\left[\frac{1}{1-e^{-sT}}\right]\Big\|_{s=s-s_n}$<br>$where K_{ni}=\frac{1}{(i-1)!}\frac{\partial^{i-1}}{\partial s^{i-1}}\left[(s-s_n)^{mn}F(s)\right]_{s=s_n}$<br>k is the number of poles,<br>mn is the multiplicity of the nth pole<br>the residue from a single multiple pole is<br>$\frac{1}{(mn-1)!}\frac{\partial^{mn-1}}{\partial\chi^{mn-1}}\left[\frac{(\chi-\chi_n)^{mn}F(\chi)}{1-e^{-T(s-\chi)}}\right]\Big\|_{\chi=\chi_n}$ | 5-14<br><br><br><br><br>5-15 |

Figure 5.3 Pulse Transformation Table [2]

Although few systems will have redundant samplers, we will exploit this result in multi-rate sampling. More succinctly, we can write that the pulse transform of a pulse transform is unchanged

$$\theta^*(s + j2\pi m f_s) = \theta^*(s) \qquad 5\text{-}16$$

Obtaining the pulse transforms with only the identities developed above can be unwieldy. Fortunately, techniques exist to obtain the pulse transform from the ordinary Laplace transform, $\theta(s)$. Figure 5.3 provides some alternative methods of obtaining the sampled Laplace transform [2].

## *Example 5.1*

Find the pulse transform of the system in Figure 5.4.

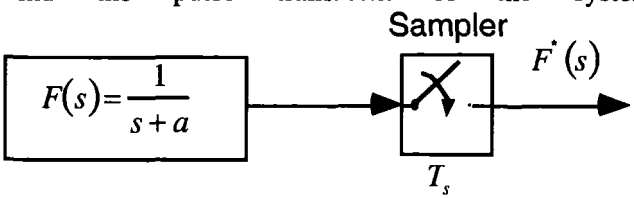


Figure 5.4 Pulse Transform of Ordinary Laplace Transform

Using Equation 5-13, we compute the intermediate functions,

$$N(\xi) = 1$$
$$D(\xi) = \xi + a$$
$$D'(-a) = 1$$

Substituting these into Equation 5-13, we obtain the pulse transfer function

$$F^*(s) = \frac{1}{1}\frac{1}{1 - e^{-T_s(s+a)}} = \frac{1}{1 - e^{-T_s(s+a)}} \qquad 5\text{-}17$$

## *Example 5.2*

Find the pulse transform of the system in Figure 5.5.

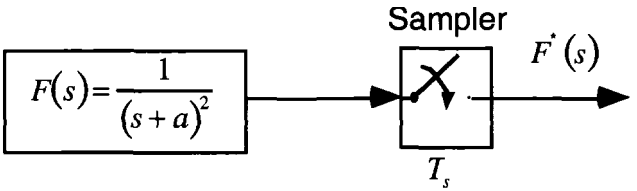


Figure 5.5 Pulse Transform of Multiple-Pole Laplace Transform

This time we utilize Equation 5-5. If the transfer function F(s) in Figure 5.5 had multiple poles instead of repeated poles, then Equation 5-14 would have been appropriate. In this example, the pole at -a is repeated twice. We make the appropriate substitutions in Equation 5-15,

$$\frac{1}{(2-1)!}\frac{\partial^{2-1}}{\partial\zeta^{2-1}}\left[(\zeta+a)^2\frac{1}{(\zeta+a)^2}\frac{1}{1-e^{-T_s(s-\zeta)}}\right]\Bigg|_{\zeta=-a} \qquad 5\text{-}18$$

Taking the derivative and simplifying, we obtain the pulse transfer function

$$F^*(s)=\frac{T_s e^{-T_s(s+a)}}{\left(1-e^{-T_s(s+a)}\right)^2} \qquad 5\text{-}19$$

## 5.2 Z Transform

A common term in Examples 5.1 and 5.2 is $e^{sT_s}$. This exponential term is a consequence of sampling the continuous-time signal. An equation with $e^{sT_s}$ is unwieldy at best. As an example, Equation 5-19 is not a ratio of polynomials, which is desirable to perform algebraic simplification. (We will need polynomial representation later to perform stability and frequency analysis of the digital transforms.)

A convenient substitution for $e^{sT_s}$ in Equation 5-19 is $z=e^{sT_s}$. With this substitution, we can express discrete-time transfer functions as a ratio of polynomials which considerably simplifies our analysis.

Performing this substitution for $e^{sT}$ in Equation 5-19 yields

$$F(z)=\frac{T_s e^{-T_s(s+a)}}{\left(1-e^{-T_s(s+a)}\right)^2}\Bigg|_{z=e^{sT_s}}$$

$$F(z)=\frac{T_s z^{-1}e^{-aT_s}}{\left(1-z^{-1}e^{-aT_s}\right)^2}=\frac{T_s z e^{-aT_s}}{\left(z-e^{-aT_s}\right)^2} \qquad 5\text{-}20$$

In Equation 5-20, we have shown that F(z) can be written as a function of $Z$ or $z^{-1}$. Even though Equation 5-20 still has the exponential, $e^{-aT_s}$, it represents a constant determined by the sampling frequency and pole location. Although F(s) corresponds to standard notation we will show it is sometimes easier to derive the filters in the Z-domain.

It is not always necessary to compute the Z-Transform by first computing the sampled Laplace Transform. A direct computation of the Z-Transform is obtained through

$$X(z)=\sum_{n=-\infty}^{\infty}x(n)z^{-n} \qquad 5\text{-}21$$

As we analyze phase-locked loops, we will often begin with a continuous transform F(s) from historical literature and find it easier to compute the Z-Transform through the sampled Laplace Transform. Kuo [2] lists several alternative expressions for the Z-Transform, X(z), which are grouped in Figure 5.6.

## *Example 5.3*

Find the Z Transform of $F(s)=\frac{1}{s+a}$.

From Example 5.1, we can substitute $z=e^{sT_s}$,

$$F(z)=F^*(s)\Big|_{z=e^{sT_s}}=\frac{1}{1-e^{-T_s(s+a)}}=\frac{1}{1-z^{-1}e^{-aT_s}} \qquad 5\text{-}22$$

| | | |
|---|---|---|
| Definition of the Z- transform | $X(z)=\sum_{}^{\infty} x(n)z^{-n}$ | 5-23 |
| F(s) has simple poles | $F(z)=\sum_{n=1}^{k}\frac{N(\chi_n)}{D'(\varphi_n)}\frac{1}{1-e^{\chi_n T}z^{-1}}$ <br> $where F(\chi)=\frac{N(\chi)}{D(\chi)}$ | 5-24 |
| F(s) has multiple-order poles with multiplicity mn | $F(z)=\sum_{n=1}^{k}\sum_{i=1}^{mn}\frac{-1^{mn-i}K_{ni}}{(mn-1)!}\left[\frac{\partial^{mn-i}}{\partial s^{mn-i}}\frac{1}{1-e^{-sT}}\right]$ <br> $\left\|s=s-s_n, z=e^{sT}\right.$ <br> $K_{ni}=\frac{1}{(i-1)!}\left[\frac{\partial^{i-1}}{\partial s^{i-1}}(s-s_n)^{mn}F(s)\right]\Big\|_{s=s_n}$ <br> k is the number of poles, <br> mn is the multiplicity of the nth pole <br> The residue for a multiple pole at $s=s_n$ may also be written as <br> $\frac{1}{(mn-1)!}\frac{\partial^{mn-1}}{\partial s^{mn-1}}\left[\frac{(s-s_n)^{mn}F(s)}{1-e^{Ts}z^{-1}}\right]\Big\|_{s=s_n}$ | 5-25 <br> 5-26 |

Figure 5.6 Methods of Obtaining the Z-Transform [2]

For an alternative solution, we can use Equation 5-26. First, the intermediate functions must be computed,

$$N(\xi_n)=1$$

$$D'(\xi_n)=1$$

Substituting these intermediate expressions of the transformation into Equation 5-25 gives

$$F(z)=\frac{1}{1-e^{-aT_s}z^{-1}} \qquad 5\text{-}27$$

Equations 5-22 and 5-27 are identical, demonstrating that both techniques are equivalent.

As a condition for the Z-Transform to exist, it is necessary for the summation in Equation 5-24 to converge [4]. Recall from the Complex Variables theory [3] that if a power series

$$\sum_{n=0}^{\infty} x(n) z^n \Big|_{z=z_1} < \infty \qquad 5\text{-}28$$

converges when $z = z_1$, it converges for every z such that $|z| < |z|_1$. By using the fact that the individual terms in the summation of Equation 5-21 are bounded, we can show that the region of convergence for the Z-Transform can be written as [4]

$$R_{x-} < |z| < R_{x+} \qquad 5\text{-}29$$

Figure 5.7 depicts the generalized region of convergence for a Z-Transform. Clearly, there are many special cases. One such case is where the sampled function x(n) is non-zero for only a finite number of terms. If the non-zero terms are bounded, then the only possible points of non-convergence are zero or infinity. There are also right-sided and left-sided sequences [3] such that the region of convergence will be a disk rather than an annulus as in Figure 5.7.

From control theory, we know a typical transfer function appears as a rational fraction with the numerator and denominator polynomials of z or s (pulse transform). Suppose the transfer function has the form shown in Equation 5-30.

$$F(z) = \frac{a_0 + a_1 z + \cdots + a_n z^n}{b_0 + b_1 z + \cdots + a_m z^m} \qquad 5\text{-}30$$

In Chapter 8, we will analyze the stability of our closed loop systems. Most of these analysis techniques examine the location of the system's poles. Recall a pole is a location of s or z that causes the denominator to vanish. A pole will force F(z) to have an infinite value at the pole location (unless cancelled by a zero).

From the definition of convergence, (Equation 5-28) it is clear that there can be no poles within the region of convergence. A zero is a value of s or z (frequency variables) that forces the transfer function to have a value of zero at that frequency, whether analog or digital frequency.

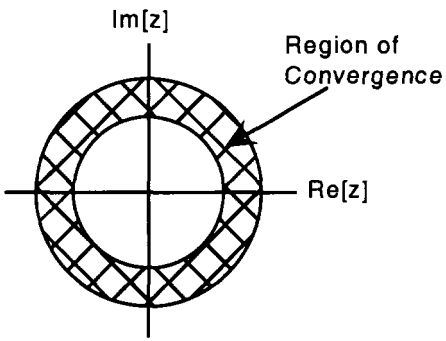


Figure 5.7 Generalized Region of Convergence for a Z-Transform

To obtain the poles or zeroes,, we note they correspond to the roots of the denominator and numerator polynomials respectively. We can write the generalized transfer function as a fraction with products of poles and zeros as shown in Equation 5-31.

$$F(z) = \frac{(z - z_1)(z - z_2)\cdots(z - z_n)}{(z - p_1)(z - p_2)\cdots(z - p_m)}$$

where $z_n$ is a root for a zero 5-31

$p_n$ is a root for a pole

## *Example 5.4*

Draw the pole-zero diagram of the transfer function $F(z) = \frac{z}{z - e^{-aT_s}}$ derived in Example 5.3. Assume a=-j1.0, and $T_s = 1.0$.

By inspection, we determine that the pole location is $z = e^{-aT_s} = e^{j1}$. The zero location is also obtained as z=0.

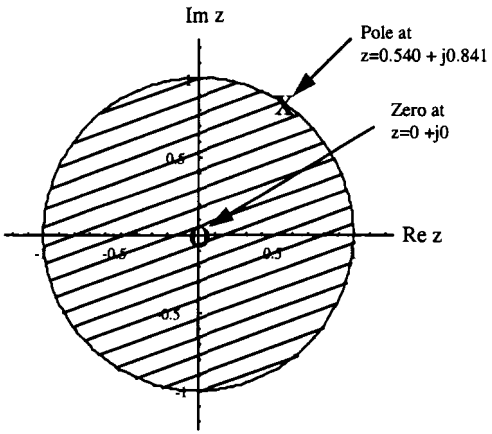


Figure 5.8 Pole-Zero Diagram of Example 5.3

## 5.3 Inverse Z-Transform

Without an inverse, the Z-Transform would be of little practical interest. As discussed earlier, our primary motivation for using the transformation is to convert complex expressions into polynomials. The inverse Z-Transform is based upon the Cauchy integral theorem [3] which states

$$\frac{1}{j2\pi}\oint_C z^{k-1}dz = \begin{cases} 1, k = 0 \\ 0, k \neq 0 \end{cases} \qquad 5\text{-}32$$

Following the approach of Oppenheim and Schafer [4] we will demonstrate how Equation 5-32 can be used with the definition of the Z-transform, Equation 5-21, to obtain the inverse Z-Transform. First, we multiply both sides of the Z transform's definition, Equation 5-21 by $z^{k-1}$. Next, we perform a contour integration where the contour of integration includes the origin and is entirely within the region of the convergence for the function X(z).

$$\frac{1}{j2\pi}\oint_C X(z)z^{k-1}dz = \frac{1}{j2\pi}\oint_C \sum_{n=-\infty}^{\infty} x(n)\, z^{k-1}\, z^{-n}dz \qquad 5\text{-}33$$

Because of the required convergence of X(z), the integration and summation on the right-hand side of Equation 5-33 can be interchanged. This yields

$$\frac{1}{j2\pi}\oint_C X(z)z^{k-1}dz = \sum_{n=-\infty}^{\infty} x(n)\frac{1}{j2\pi}\oint_C z^{-n+k-1}dz \qquad 5\text{-}34$$

Now recognize that the right-hand integral of Equation 5-34 is in the form of the Cauchy Integral Theorem, Equation 5-31. The integral is non-zero only for $k-n=0$, or $n=k$. This leaves only one term in the entire summation, x(k). This allows us to write the inverse Z-transform as

$$\frac{1}{j2\pi}\oint_C X(z)z^{k-1}dz = x(k) \qquad 5\text{-}35$$

Substituting **n=k**, and exchanging the right and left-hand sides of the equation yields the traditional form of the inverse Z-transform.

$$x(n) = \frac{1}{j2\pi}\oint_C X(z)z^{n-1}dz \qquad 5\text{-}36$$

Through this application of the Cauchy Integral Theorem, we see that the inverse Z-transform can be expressed as a sum of residues,

$$x(n) = \sum \begin{matrix}\text{residues of } X(z)z^{n-1} \text{ at the poles} \\ \text{inside the contour, C}\end{matrix} \qquad 5\text{-}37$$

The residues for multiple poles are computed as

$$\text{Res}\left[X(z)z^{n-1} \text{ at } z = z_0\right] = \frac{1}{(s-1)!}\left[\frac{d^{s-1}}{dz^{s-1}}(z-z_0)^s X(z)z^{n-1}\right] \qquad 5\text{-}38$$

## *Example 5.5*

Find the inverse Z-Transform for $F(z) = \dfrac{T_s z e^{-0.5T_s}}{\left(z - e^{-0.5T_s}\right)^2}$.

This is a more complex transformation because of the repeated poles. Utilizing Equation 5-38,

$$\text{Res}\left[\frac{T_s z e^{-0.5T_s}}{\left(z-e^{-0.5T_s}\right)^2} z^{k-1} \text{ at } z = e^{-0.5T_s}\right] = \frac{1}{(2-1)!}\left[\frac{d^{s-1}}{dz^{s-1}}\left(z-e^{-0.5T_s}\right)^2 \frac{T_s z e^{-0.5T_s}}{\left(z-e^{-0.5T_s}\right)^2} z^{k-1}\right] \quad 5\text{-}39$$

$$F(z) = k\,T_s\,z^{k-1}e^{-0.5T_s}\Big|_{z=e^{-0.5T_s}} = k\,T_s\,z^{k-1}e^{-0.5k\,T_s} \quad 5\text{-}40$$

## 5.4 Partial Fraction Expansion

Direction application of the residue Equation 5-37 can be difficult, so typically a table of inverse Z-Transforms [2-4] is used to obtain the time sequence, x(n). (Appendix B also provides a table of inverse Z-transforms.) Typically the transfer function can be separated through partial fraction expansion to obtain a sum of simpler fractions that can be identitifed in tables. To perform partial fraction expansion, we express the transfer function [2]

$$F(z) = \frac{P(z)}{Q(z)} = \sum_{k=1}^{N} \frac{A_k}{z - p_k} \quad 5\text{-}41$$

The $p_k$'s In Equation 5-41 are the poles of the transfer function as discussed earlier. The $A_k$'s correspond to the residues at the particular poles, just as we obtained earlier for the direct computation of the inverse Z-Transform in equation 5-37. We note that the order of the numerator must be less than the denominator to perform the partial fraction expansion. If this is not the case, then the ratio in Equation 5-41 must be synthetically divided to obtain a "mixed" fraction where the remaining fraction meets this criteria.

A special case of residue computation exists when a pole, $p_l$, is repeated M times in Equation 5-41. In such a situation we must modify the technique to [2]

$$F(z)=\frac{P(z)}{Q(z)}=\sum_{k=1}^{N}\frac{A_k}{z-p_k}+\sum_{m=1}^{M}\frac{c_m}{(z-p_l)^m} \qquad 5\text{-}42$$

The coefficients $c_m$, which correspond to the partial fractions with repeated roots are obtained from

$$c_m=\frac{1}{(M-m)!}\left\{\frac{d^{M-m}}{dz^{M-m}}(z-p_l)^M F(z)\right\}_{z=p_l} \qquad 5\text{-}43$$

## *Example 5.5*

Find the inverse Z-Transform of $F(z)=\dfrac{z-a}{(z+b)^2(z+c)}$.

Using partial expansion can require more effort than a direct application of the residue theorem unless some "tricks" are used. These come with experience in deriving transformations. Instead of computing the partial fraction expansion of **F(z)**, we compute the partial fraction expansion of **F(z)/z**. In the problem statement, there are three separate poles, with the pole at **z=-b** repeated twice. Applying Equation 5-42,

$$\frac{F(z)}{z}=\frac{A_1}{z}+\frac{A_2}{(z+c)}+\frac{c_1}{(z+b)}+\frac{c_2}{(z+b)^2} \qquad 5\text{-}44$$

To complete the partial fraction expansion, we must find the unknown coefficients.

$$A_1=\left.\frac{z-a}{(z+c)(z+b)^2}\right|_{z=0}=\frac{a}{cb^2} \qquad 5\text{-}45$$

$$A_2 = \frac{z-a}{z(z+b)^2}\Big|_{z=-c} = \frac{a+c}{c(b-c)^2} \qquad 5\text{-}46$$

$$c_1 = \frac{d}{dz}\frac{z-a}{z(z+c)}\Big|_{z=-b} = \frac{a+b-2a \;\; b-b \;\; c-b^2}{b^2(c-b)^2} \qquad 5\text{-}47$$

$$c_2 = \frac{z-a}{z(z+c)}\Big|_{z=-b} = \frac{a+b}{bc-b^2} \qquad 5\text{-}48$$

After finding the coefficients, the transfer function are written in the form of Equation 5-41,

$$F(z) = \frac{A_1 z}{z} + \frac{A_2 z}{z+c} + \frac{c_1 z}{z+b} + \frac{c_2 z}{(z+b)^2} \qquad 5\text{-}49$$

After all this effort, we're still not finished. The inverse Z-Transform must be computed for each individual partial fraction in Equation 5-49. Z-Transform Tables or Equation 5-34 can be used to obtain the inverse transforms for each of these partial fractions. Using the Z-Transform Table in Appendix B,

$$f(n) = A_1\delta(n) + A_2 \;\; (-c)^n + c_1(-b)^n + c_2 \;\; n \;\; (-b)^{n-1} \qquad 5\text{-}50$$

Note that Equation 5-50 could not have been obtained directly from the Z-Transform Tables if we had not first obtained the partial fraction expansion of F(z)/z. If we had computed the expansion of F(z) directly, (without the $z^{-1}$) then the individual partial fractions would have been missing a factor of z in the numerator that corresponds to the entries in the table.

## 5.5 Synthetic Division

Examination of the definition of the Z-transform, Equation 5-22, suggests yet another alternative for obtaining the inverse Z-Transform. We note that the Z-Transform is a weighted series of coefficients multiplied against the

input Z sequence. If we could obtain the coefficients of the power series, then we could obtain the resulting time sequence. Indeed, this is the case, and we can sometimes use synthetic division to obtain the inverse Z-Transform [7]. (Usually this is performed by numeric analysis routines.)

Usually, we cannot obtain a closed form expression for the inverse Z-Transform from synthetic division unless we are clever and can recognize the closed form expression for the resulting infinite series. However, this technique is useful for plotting the function for a finite number of time samples.

## *Example 5.6*

Compute and graph the first 20 time samples represented by the transfer function,

$$F(z)=\frac{z-1}{(z+0.5)(z-0.5)} \qquad 5\text{-}51$$

One method of obtaining the solution could be computing a partial fraction expansion of Equation 5-51 which would yield the inverse Z-transform of this transfer function. However for this example we want to demonstrate the use of synthetic division. Equation 5-52 shows the process of synthetic division.

$$\begin{array}{l} z^{-1}-z^{-2}+0.25z^{-3}+\cdots \\ z^2-0.25\overline{)z-1} \\ \quad \underline{z-0.25z^{-1}} \\ \quad 0-1+0.25z^{-1} \\ \quad \underline{0-1+0.25z^{-2}} \\ \quad 0-0+0.25z^{-1}-0.25^{-2} \\ \quad \underline{0-0+0.25z^{-1}-0.125z^{-3}} \\ \quad \cdots \\ \quad \cdots \\ \quad \overline{\qquad\qquad\qquad} \end{array} \qquad 5\text{-}52$$

The actual closed-form expression for f(n) is obtained from an inverse Z-Transform of Equation 5-52 and is expressed as

$$f(n) = 4\delta(n) - (0.5)^n - 3(-0.5)^n \qquad 5\text{-}53$$

The first ten samples of Equation 5-52 are graphed in Figure 5.9. The values of f(n) obtained by synthetic division are the same as those obtained from the direct inverse Z-Transform

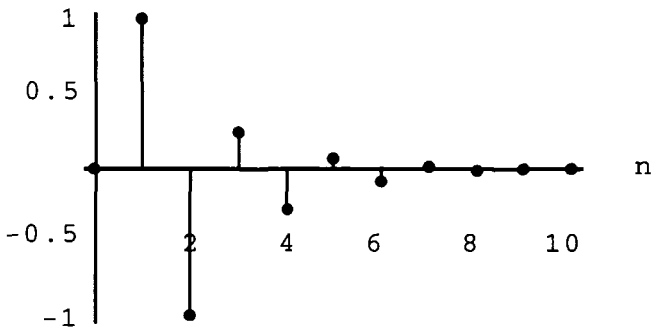


Figure 5.9 Time Samples Represented as the Inverse Transform of F(z)

There are some fundamental properties of the Z-transform that are used frequently in the analysis of phase-locked loops. These are similar to the properties of the Laplace transform that were presented in Chapter 2.

$$f(n+n_0) \leftrightarrow z^{n_0} F(z) \quad \text{Time Delay Theorem} \qquad 5\text{-}54$$

$$F(z)G(z) \leftrightarrow f(t) * g(t) \quad \text{Convolution Theorem} \qquad 5\text{-}55$$

$$\lim_{n\to 0} f(nT_s) = \lim_{z\to\infty} F(z) \quad \text{Initial Value Theorem} \qquad 5\text{-}56$$

$$\lim_{n\to\infty} f(nT_s) = \lim_{z\to 1}\left\{\frac{z-1}{z}F(z)\right\} \quad \text{Final Value Theorem} \qquad 5\text{-}57$$

## 5.6 Zero Order Hold

Discrete samples of a continuous signal can be easily produced by a sampler. Often, our system must provide a continuous output when the input is a discrete sample. In Figure 5.10, we have a zero-order hold following the sampler. A continuous-time signal is necessary for the analog filter and voltage-controlled oscillator. A simple mechanization is the zero order hold which is expressed as

$$zoh(f(t)) = f(kT),\ kT \le t < (k+1)T \qquad 5\text{-}58$$

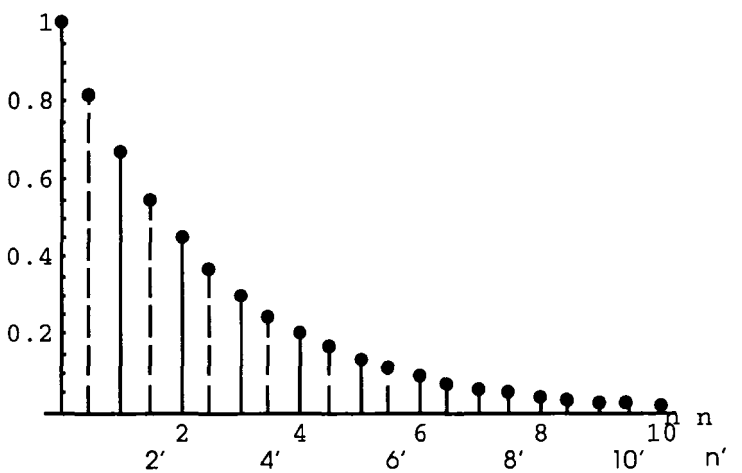


Figure 5.10 Combined Graph of Conventional and Modified Time Response

Figure 5.11 shows the output of a zero order hold for a parabolic input waveform. This depiction is similar to figures drawn for Riemann integration where the value of **f(t)** is held constant throughout the integration rectangle.

Other implementations of sample and holds are possible such as the first or second-order sample and holds [2,5]. For many applications though, it is questionable whether more complex sample and holds offer any advantages.

As an example, at high frequencies the phase lag of a first order hold exceeds that of a zero order hold, which is undesirable for control loops.

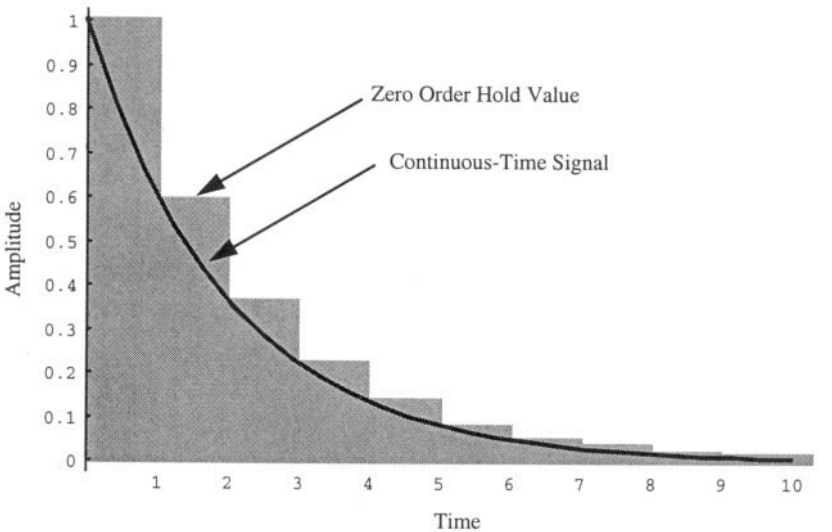


Figure 5.11 Output From a Zero Order Hold

The impulse response of the zero order hold is written as

$$g_{h0}(t) = u_s(t) - u_s(t-T) \qquad 5\text{-}59$$

Taking the Laplace Transform of Equation 5-59, we obtain [6]

$$G_{h0}(s) = \frac{1-e^{-sT}}{s} \qquad 5\text{-}60$$

The frequency response of the zero order hold is plotted in Figure 5.12. As we would expect, there is significant amplitude attenuation as the input frequency approaches the sampling frequency, $f_s$.

We note that a zero-order sample and hold preceding a transfer function G(s) has transfer function

$$G(z) = \frac{z-1}{z} Z\left[\frac{G(s)}{s}\right] \qquad 5\text{-}61$$

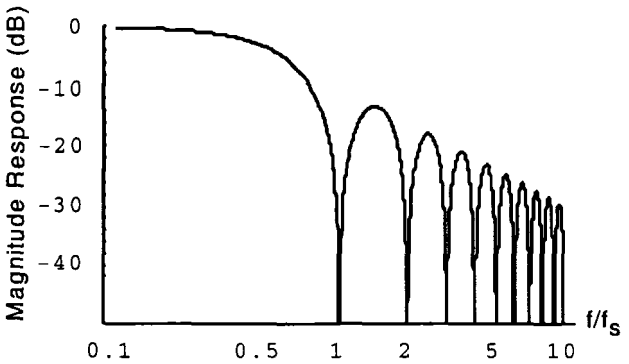


Figure 5.12 Frequency Response of the Zero Order Hold

## 5.7 References

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## 5.8 Problems

5.1 Find the pulse transform for $F(s)=\dfrac{1}{s(s+a)}$.

5.2 Compute the pulse transform for $F(s)=\dfrac{1}{s^2+2\zeta\omega_n s+\omega_n^2}$.

5.3 Compute the Z-transform for $F(s)=\dfrac{1}{s^2+2\zeta\omega_n s+\omega_n^2}$.

5.4 Compute the inverse Z-transform for $F(z)=\dfrac{1}{(z-1)^2}$.

5.5 Use partial fraction expansion to obtain the inverse Z-transform for $F(z)=\dfrac{1}{(z-\alpha)(z-\beta)}$.

5.6 Compute the modified Z-transform for $F(s)=\dfrac{1}{(s-\alpha)(s-\beta)}$.

5.7 Compute the inverse modified Z-transform for $F(z,m)=\dfrac{mT_s}{z-1}+\dfrac{T_s}{(z-1)^2}$.

5.8 Compute the Z-transform of a system with sample-and-hold prior to $H(s)=\dfrac{1}{s(s+\alpha)}$.

# 6

# Charge Pumps, Counters, and Delay-Locked Loops

In this chapter we discuss some miscellaneous topics, but very important to phase-locked loop designers. Charge pumps are the perfect match to sequential phase detectors, converting their differential outputs to a single-ended output. Aside from this useful function, we shall discuss how they offer tracking and phase noise advantages over other loop configurations.

The digital counter was originally designed for logic circuits, but was soon applied to frequency synthesizers. The phase noise performance of digital counters is discussed in Chapter 12, but in this chapter we discuss design techniques for reducing phase noise and improving the performance of digital counters. We also discuss an alternative to the conventional digital counter.

Our final topic is delay-locked loops. It is often used to describe the early-late gate synchronizer which we will discuss in Chapter 11. In this chapter, we discuss the delay-locked loop used by digital designers to align clock phases.

## 6.1 Sequential Phase Detectors

In Chapter 2, we discussed the sequential phase detector as a component of frequency synthesizers. The sequential phase detector is superior to mixer-type phase detectors in many applications. Multiplying phase detectors are preferred for data synchronization circuits, but dual detectors can also be used [1]. The sequential phase detector provides these

advantages: 1) extended phase detector range, 2) improved frequency acquisition, 3) insensitive to input signal levels.

A sequential phase detector is shown in Figure 1. This is a relatively simple implementation, as several improvements can be made to its operation [3-4]. Figure 6.1 shows a D-flip-flop implementation, but R-S flip-flop implementations are also popular. Note the "H" designates a logic high input to the data inputs of the flip-flops.

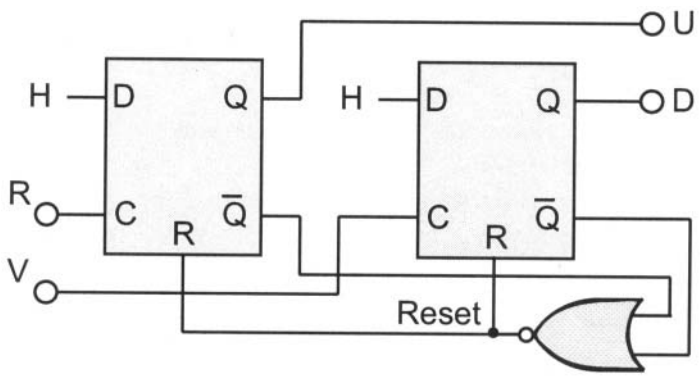


Figure 6. 1 Sequential Phase Detector

The reference frequency for the phase-locked loop (synthesizer) is applied to the "R" input in Figure 1. The VCO's output is applied to the "V" input. The phase detector generates two pulse-modulated outputs that a charge pump converts into a single-ended control voltage for the VCO. (It is also possible to use a conventional operational amplifier to convert the U and D phase detector outputs to a single output, but it doesn't provide the other advantages of a charge pump.)

The fundamental rule for the sequential phase detector of Figure 6.1 is that the Up and Down outputs can never be high at the same time. To illustrate this, assume that the inputs and outputs are all high. For this set of initial conditions, both flip-flops are set with logical high outputs. Their complementary $\overline{Q}$ outputs are both at a logical low. The NOR gate will immediately reset the flip-flops to logical lows, so the U=1, D=1, state is only transitional.

Figure 6.2 shows the trellis diagram for the sequential phase detector. The state is designated by the current U and D outputs. For example, if the sequential phase detector has U=0, D=1, the phase detector is in the middle

state of Figure 6.2. If a positive transition occurs on the V input first, $V\uparrow$, the phase detector will stay at state U=0, D=1. However, if the positive transition occurs on the R input first, $R\uparrow$, then the phase detector will change to state U=0, D=0.

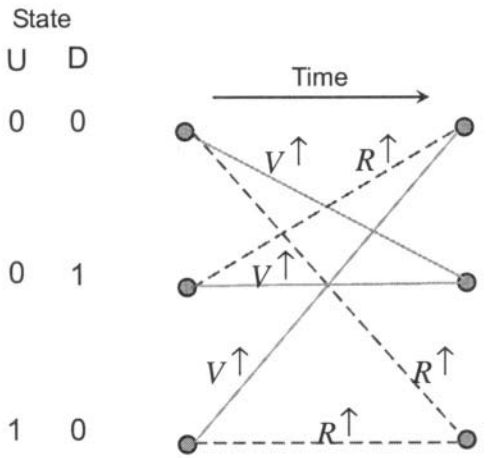


Figure 6.2 Trellis Diagram for the Sequential Phase Detector

This example also illustrates a problem with the standard phase frequency detector. As noted, when the detector was in state U=0, D=1, a transition $V\uparrow$ would keep the outputs in the current state. If a transition was missing (due to noise) on the R input, then the phase detector would erroneously have the D output high for at least one additional reference period. This would have the opportunity to drive the loop out of phase-lock.

Figure 6.3 shows the operation of the phase detector with identical reference and VCO frequencies. However, the VCO is lagging behind the reference by 180° or $\pi$ radians. Note that the Down output consists of a 50% duty cycle square wave to bring the loop into phase-lock. This allows us to determine the effective gain of this sequential phase detector,

$$K_d = 0.5 \times \frac{1V}{\pi \text{ radians}} \qquad 6\text{-}1$$

Since the input transitions occur once per reference or VCO period, the detector has a range of $\pm 2\pi$ radians. Also, the phase detector is not sensitive to the duty cycle of the input waveforms. It only requires a positive edge and a duration sufficient for the digital circuitry.

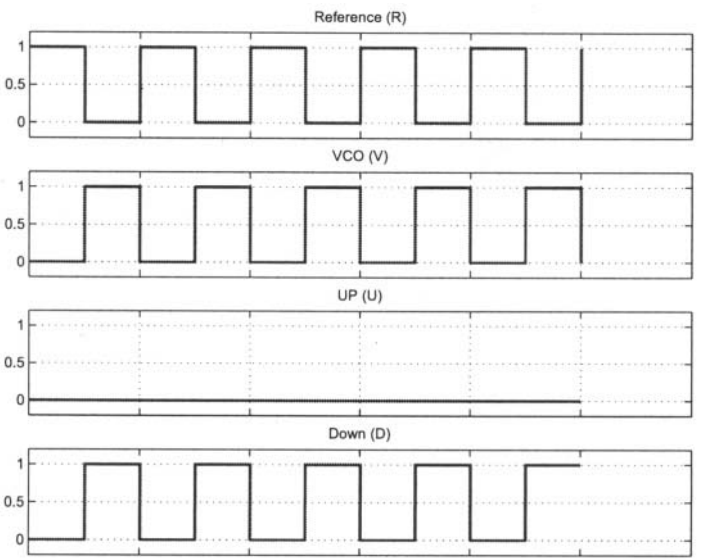


Figure 6.3 VCO Lagging Reference by 180°

Figure 6.4 shows the sequential phase detector's output when the reference frequency is greater than the VCO frequency. Under this condition, the phase detector outputs pulses on the (U) output.

Figure 6.5 shows the sequential phase detector's output when the VCO frequency is greater than the reference frequency. Under this condition, the phase detector outputs pulses on the (D) output.

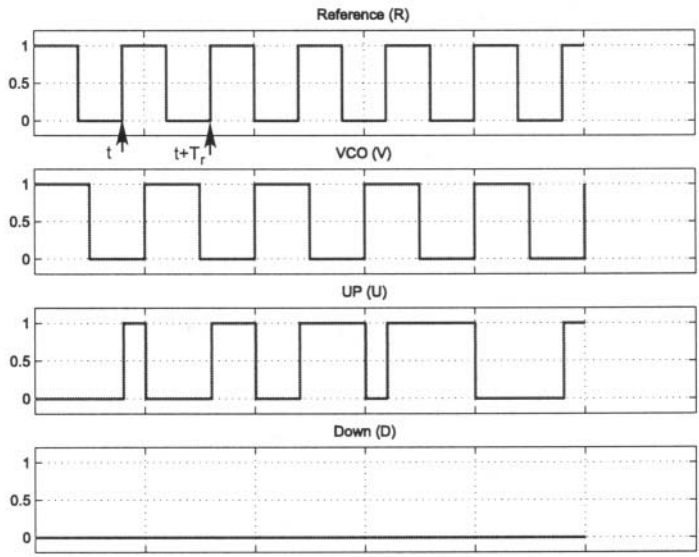


Figure 6.4 Sequential Phase Detector Output With Greater Reference Frequency

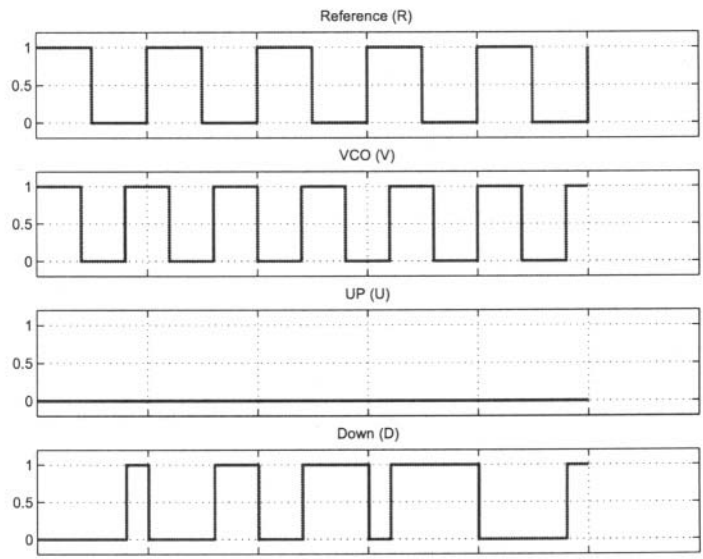


Figure 6.5 Sequential Phase Detector Output With Greater VCO Frequency

There are some design considerations for using a sequential phase detector. If either of the inputs is noisy and extra or missing transitions occur, then the outputs from the sequential phase detector will be erroneously controlling the VCO.

Another problem with sequential phase detectors is decreased gain near phase-lock. In the literature, this is described as a "dead-zone" [4-5]. A common technique to combat this effect is to produce a minimum (U) and (D) pulse on every waveform cycle [6]. Often this is implemented by placing a delay between the inputs and the flip-flops' reset input as shown in Figure 6.6. When phase-locked the minimum-duration (U) and (D) pulses are coincident. Other techniques such as precharging can also reduce the dead-zone of the sequential phase detector [3,9].

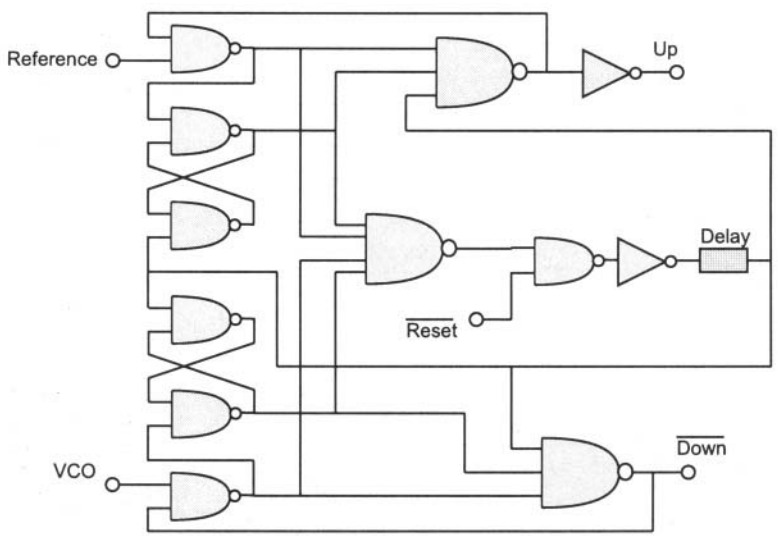


Figure 6.6 Dead Zone Elimination [3]

The low-frequency analysis of the sequential phase detector follows that of Soyuer and Meyer in [10]. If the frequencies of the VCO and Reference, designated as $f_v$ and $f_r$, respectively, are not equal, we define the ratio

$$\alpha = f_v / f_r \qquad 6\text{-}2$$

For $f_r > f_v$, $0 < \alpha < 1$. Refer back to Figure 6.4 and note the positive reference transitions $t$ and $t + T_r$. Because the reference frequency is higher, there can be at most one VCO transition in the interval $[t, t + T_r]$. Soyuer and Meyer define the probabilities of one and no VCO transitions in the interval as [10]

$$P(0) = \Pr obability\ of\ no\ VCO\ transition = 1 - \alpha \qquad 6\text{-}3$$

$$P(1) = \Pr obability\ of\ one\ VCO\ transition = \alpha \qquad 6\text{-}4$$

If there is no VCO transition in the interval $[t, t + T_r]$, the Up (U) output has a logic high level throughout the interval. If the VCO has a single transition, then the U output is at a logic high until the transition. The probabilities computed above allow us to express the expected (average) difference between the Up and Down output as [10]

$$E\{U - D\}_{r>v} = P(0) \times 1 + P(1) \times 0.5 = 1 - \alpha/2 \qquad 6\text{-}5$$

If the VCO frequency is greater than the reference, a similar derivation yields [10]

$$E\{U - D\}_{v>r} = \frac{1}{2\alpha} - 1 \qquad 6\text{-}6$$

Equations 6-5 and 6-6 represent the average difference voltage between the U and D sequential phase detector outputs when the input frequencies are not the same. As the input frequencies approach circuit limits, the duration of the reset pulse, $\Delta R$ for the flip-flops in Figures 6.1 and 6.6 begins to affect the average voltage differences. Assuming comparator times $T_r$ and $T_v$ for the reference and VCO respectively, the average voltage differences can be written as [10]

$$E\{U - D\}_{r>v} = 1 - \frac{1}{2\alpha} - \frac{\Delta R}{T_v} \quad , \quad f_r > f_v \qquad 6\text{-}7$$

$$E\{U-D\}_{v>r} = \frac{1}{2\alpha} - 1 + \frac{\Delta R}{T_r} \quad , \quad f_v > f_r \qquad 6\text{-}8$$

## 6.2 Combining Sequential Phase Detectors and Charge Pumps

Figure 6.7 shows the a sequential phase detector and charge pump combination in a phase-locked loop. The reference signal is typically a stable crystal-derived source. This phase/frequency is compared to the VCO's signal by the sequential phase detector. The phase detector generates a pair of pulse-modulated error signals that must be converted into a single voltage, $v_c$, acceptable as a control voltage by the VCO.

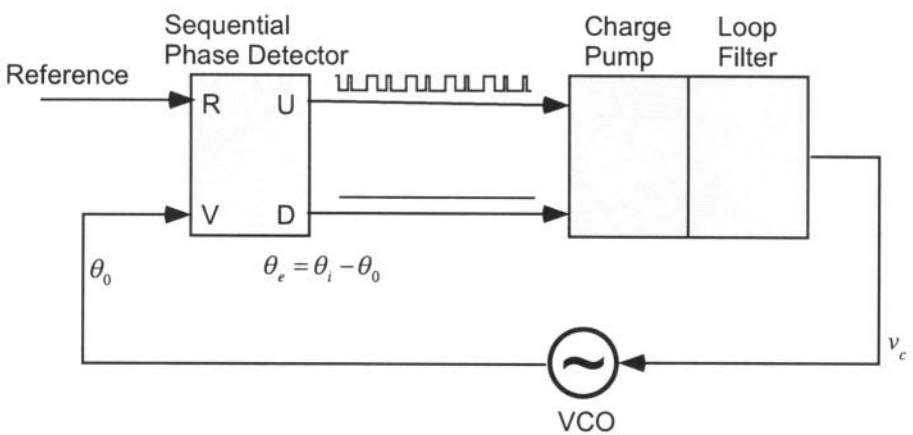


Figure 6.7 Charge-Pump Phase-Locked Loop

Gardner [7] describes the charge pump as a 3-position electronic switch that is controlled by the three states of the phase detector: a) up, b) down, and c) neutral. The loop filter can be driven by either voltage or current, and the filter itself can either be passive or active. Figure 6.8 shows various schematic permutations of the charge pump.

In Figure 6.8a, a positive current is applied for the "UP" position, a negative current is applied for the "Down" position, and an open circuit is applied for the "Neutral" position. The Neutral position corresponds to both sequential phase detector outputs in the logical low position and the others refer to the high-going pulses on either the Up or Down outputs.

It is the uniqueness of the "Neutral" position that provides much of the charge pump's advantage. When the loop is phase-locked, there is very little phase error, and both of the sequential phase detector's outputs will be low. Hence, at phase-lock, the loop filter is connected to an open circuit that does not generate noise. Recall in an analog mixer phase-locked loop, the phase error from the mixer might be zero volts, but the loop filter is still connected to noise sources which will degrade the jitter performance of the phase-locked loop.

Instead of currents, the electronic switch can supply positive or negative voltages to the load impedance as shown in Figure 6.8b. However, the current sources are the favored configuration because voltages stored in the loop filter's capacitors result in asymmetrical voltages applied to the load in Figure 6.8b. Sourcing or sinking currents as in Figure 6.8a eliminates the asymmetry which can create spurious frequency components at the phase-locked loop's output.

A typical charge pump configuration is shown in Figure 6.9. The sequential phase detector, or Phase Frequency Detector is similar to the Motorola MCH12140 (also similar to Figure 6.1) [8]. Most low-voltage implementations require differential signals throughout the circuitry to reduce susceptibility to power supply noise as shown in Figure 6.9. When neither the Up or Down phase detector outputs are active, the two current sources, ICS1 and ICS2 are shunted to an off-chip load [5]. When the phase detector outputs are modulated (pulsing), there will be a difference in the current levels $\mathbf{I_{up}}$ and $\mathbf{I_{dn}}$ which is sourced to the off-chip load (loop filter).

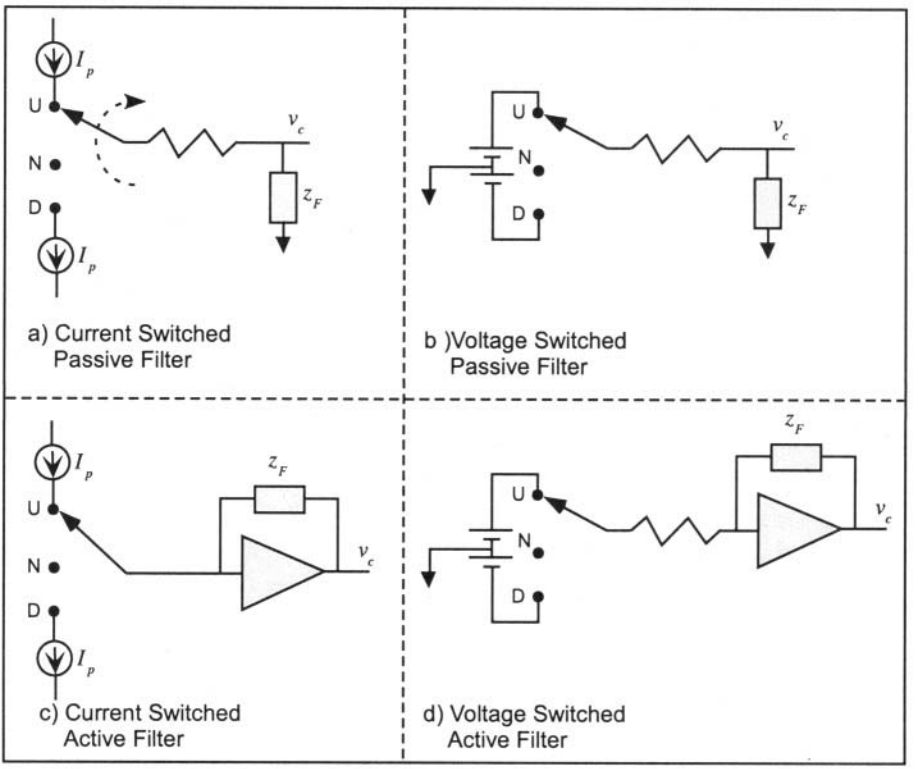


Figure 6.8 Schematic Equivalents for the Charge Pump [7]

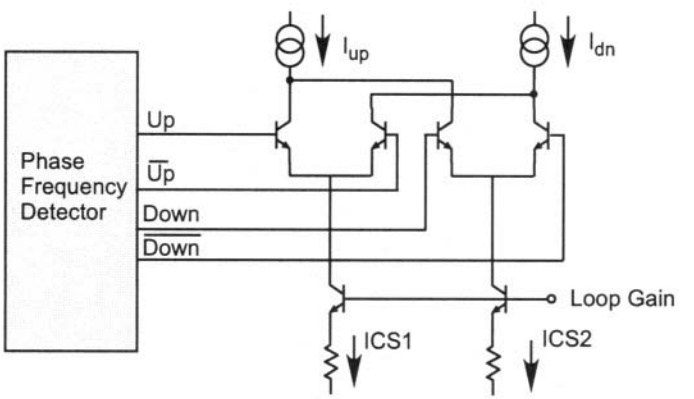


Figure 6.9 Example Charge Pump Schematic

### 6.2.1 Charge Pump Equations

Our analysis follows that of Gardner [7] and Paemel [15].

Charge pump implementations 6.8a and 6.8b use a passive filter for the load impedance whereas Figures 6.8c and 6.8d have active loop filters. Regardless of the configuration, when the loop is in the locked condition, the time period of the pulses applied to the charge pump is [7,15]

$$t_p = \frac{|\theta_e|}{2\pi f_i} \qquad 6\text{-}9$$

where $f_i$ is the input frequency, $\theta_e$ is the phase error, and "p" denotes pump. This agrees with our earlier observations of Figure 6.3 The period of the output waveform is $1/f_r$, and the duty cycle (time duration of the logic high pulse) is proportional to the phase difference between the reference and VCO inputs.

The equivalent schematics of Figure 6.8 illustrate the charge pump delivers either a pump voltage $v_p$ or pump current $I_p$ to the loop filter. Equation 6-9 is used to compute the average current for the configuration of Figure 6.8a. The load impedance $z_f$ receives a current $i = I_p \operatorname{sgn}[\theta_e]$ for $t_p$ seconds. (The sign of the current depends upon which of the two current sources in Figure 6.8a is switched.) Thus the average current provided to the loop filter's impedance is [7]

$$\langle i_d \rangle = \frac{I_p \theta_e}{2\pi} \; Amps \qquad 6\text{-}10$$

This charge pump current creates a control voltage, $v_c$, across the loop filter impedance, $z_f$. The control voltage is then used as negative feedback to adjust the VCO frequency/phase for phase-lock. The control voltage to the VCO is

$$v_c(s) = \frac{I_p z_f(s) \theta_e(s)}{2\pi} \qquad 6\text{-}11$$

The loop transfer function for the VCO is then written as

$$H_o(s) \equiv \frac{\theta_o(s)}{\theta_i(s)} = v_c(s)\frac{K_o}{s} = \frac{K_o I_p z_f(s)}{2\pi s + K_o I_p z_f(s)} \qquad 6\text{-}12$$

where $K_o$ is the transducer gain of the VCO.

Similar to Chapter 2, we can specialize the general charge pump equation for different loop filters by substituting the loop filter's impedance for $z_f$. Since the second-order phase-locked loop is used most often, we will derive the equations corresponding to the loop filter in Figure 6.10. Recall that the conventional analog loop with a passive filter such as Figure 6.10 is not able to track a frequency step without a residual phase error. Surprisingly, we will show that a second-order charge pump with a passive filter has a steady-state phase error of zero for an input frequency step.

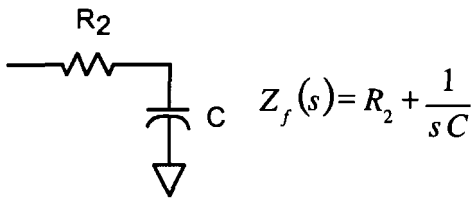


Figure 6.10 Passive Loop Filter for Second-Order Charge Pump

Substitution of the passive loop filter's impedance into the output transfer Equation 6-12 yields the second order phase-locked loop equation.

$$H_o(s) = \frac{\frac{K_o I_p}{2\pi C}(1 + R_2 C s)}{s^2 + \frac{K_o I_p}{2\pi C}(1 + R_2 C s)} \qquad 6\text{-}13$$

Recall in Chapters 2 and 3, we cast the loop equations into servo-mechanism terminology. Traditionally, the second order phase-locked loop transfer function is written as

$$H_o(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 6\text{-}14$$

Comparing Equations 6-14 and 6-13, we note that $\omega_n^2 = \frac{K_o I_p}{2\pi C}$. Thus the loop natural frequency, $\omega_n$, is written as

$$\omega_n = \sqrt{\frac{K_o I_p}{2\pi C}} \qquad 6\text{-}15$$

It results in a more compact equation for the loop damping ratio if we express the resistor-capacitor product as a time constant,

$$\tau_2 = R_2 C \qquad 6\text{-}16$$

The loop damping ratio, $\varsigma$, is also obtained by comparing Equations 6-14 and 6-13.

$$\zeta = \frac{\tau_2}{2}\sqrt{\frac{K_o I_p}{2\pi C}} \qquad 6\text{-}17$$

With these definitions, the charge pump's transfer function can be expressed in the desired servo-mechanism notation. The charge pump phase-locked loop with the filter of Figure 6.10 has the exact same dynamic response as the conventional PLL.

One final observation is the steady state phase error due to a frequency step. Recall the phase-locked loops error response to a frequency step is

$$\theta_e(s) = \frac{f_\Delta}{s} H_e(s) \qquad 6\text{-}18$$

Previously we had derived the output transfer function of the PLL relative to the VCO in Equation 6-13. To obtain the phase error response, we need the error response transfer function. It is calculated with the following relationship,

$$H_e(s) = 1 - H_o(s) = \frac{2\pi C s^2}{2\pi C s^2 + K_o I_p C R_2 s + K_o I_p} \qquad 6\text{-}19$$

Using the Laplace Transform's Final Value Theorem,

$$\theta_e(t=\infty) = Lim_{s\to 0}\, s\frac{f_\Delta}{s} H_e(s)$$
$$= Lim_{s\to 0}\, s\frac{f_\Delta}{s}\frac{2\pi\, C s^2}{2\pi\, C s^2 + K_o I_p C R_2 s + K_o I_p} = 0 \qquad 6\text{-}20$$

The final result is zero because the filter of Figure 6.10 has an infinite impedance at DC. Hence the charge pump achieves zero static error with a frequency step using only a passive loop filter.

A second-order charge pump has challenges, though as shown in Figure 6.11. The output of the charge pump filter has large steps that can exceed the VCO's tuning capability or merely provide an undesirable ripple that will cause spurious tones in the VCO output.

A rule-of-thumb is that if the loop bandwidth is less than one-tenth of the reference frequency, then the ripple is tolerable [7]. Otherwise filtering must be provided to reduce the ripple.

Besides the ripple which we will attenuate with additional filtering, the second-order charge pump is also potentially unstable. Recall in Chapter 2 that the analog second-order phase-locked loop was unconditionally stable. The charge pump phase-locked loop is really a discrete-time system and can become unstable at high gain levels. Gardner derives the discrete-time characteristic equation as [7]

$$D(z) = (z-1)^2 + (z-1)\frac{K}{f_r}\left[1 + \frac{1}{f_r \tau_2}\right] + \frac{K}{f_r^2 \tau_2} \qquad 6\text{-}21$$

where the gain is computed as $K = K_O I_p R_2 / 2\pi$.

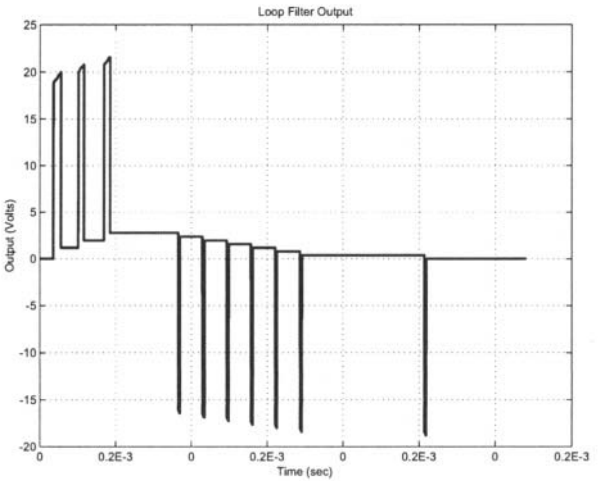


Figure 6.11 Charge Pump Filter Ripple for Second Order Loop

The characteristic equation can be examined with discrete-time analysis techniques presented in Chapter 8. The roots of the characteristic equation become real (overdamped loop) at gain values of [7]

$$K > \frac{4}{\tau_2 \left(1 + \frac{1}{f_r \tau_2}\right)^2} \qquad 6\text{-}22$$

Recall from Chapter 3 that real roots generate a loop response of the form $e^{-\alpha t}$, where $\alpha$ is real. There is no overshoot in the error response, but the loop responds much more slowly than a loop with complex roots.

The loop becomes unstable for [7]

$$K > \frac{1}{\frac{1}{2 f_r \tau_2}\left(1 + \frac{1}{2 f_r \tau_2}\right)} \qquad 6\text{-}23$$

We now return to the ripple shown in Figure 6.11. There are several difficulties presented by the ripple:

1) The voltage frequency jumps could be outside the VCO's tuning range. This condition is called overload [15]. (A special case is where the VCO is driven to negative frequency.) Clearly if the VCO cannot tune to the frequency commanded by the loop filter, the phase-locked loop operation will be non-linear and probably not meet design expectations.

2) The spectral purity becomes unacceptable.

Additional loop filtering can be provided to "smooth out" the voltage jumps commanded by the loop filter. Figure 6.12 shows example filter configurations to replace the filters of Figures 6.8a and 6.8b.

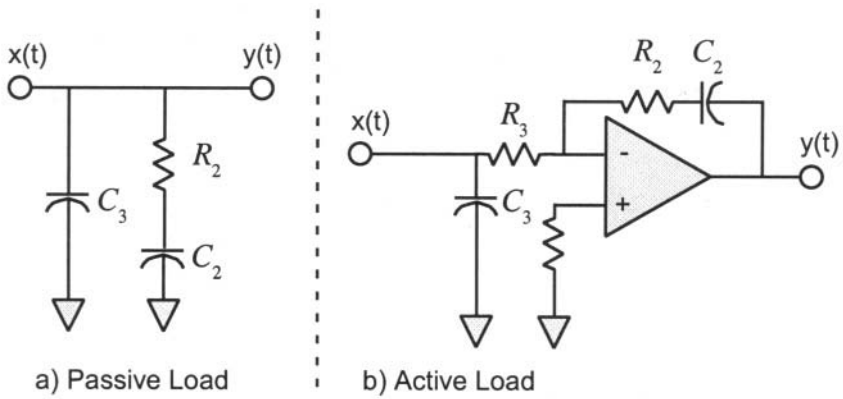


Figure 6.12 Filters for Third-Order Charge Pump Loops

The loop transfer function for Figure 6.12a can be written as

$$Z_f(s) = \frac{\frac{1}{sC_2} + R_2}{sC_3\left(\frac{1}{sC_2} + \frac{1}{sC_3} + R_2\right)} \qquad 6\text{-}24$$

For the open-loop transfer function, the filter of Figure 6.12a has provided an additional pole at $s = -\frac{1 + C_2/C_3}{R_2 C_2}$. Substituting this filter into Equation 6-12 yields the closed loop transfer function for the third-order charge pump.

$$H_O(s) = \frac{K_O I_p (1 + sC_2 R_2)}{2\pi s^2 C_3 + s C_2 (2\pi s + 2\pi s^2 C_3 R_2 + K_O I_P R_2) + K_O I_p} \quad 6\text{-}25$$

The open loop response of Equation 6-25 is a third-order, type-2 loop. The dynamic response will be similar to a second-order, type-2 loop. As a third-order loop, it is potentially unstable. However, it can provide attenuation of the ripple shown in Figure 6.11.

As an analysis aid, Gardner introduces the variable

$$b = 1 + C_2/C_3 \quad 6\text{-}26$$

For **b<1**, the loop is unstable.

## *Example 6.1*

Design a charge pump phase-locked loop with the following parameters:

$K_o = 1\times10^4\ Hz/V$, $\omega_n = 1.2\times10^4\ rad/\sec$, $I_p = 10\times10^{-3}\ A$, and $\zeta = 0.707$.

From the problem statement, we first compute the capacitor value for the second-order charge pump filter of Figure 6.10. Using Equation 6-15, we compute

$$C = \frac{K_o I_p}{2\pi\omega_N^2} = \frac{1.0\times10^4 \times 2\pi \times 10\times10^{-3}}{2\pi\times(1.2\times10^4)^2} = 6.94\times10^{-7} \quad 6\text{-}27$$

The time constant of the filter is computed next using Equation 6-17,

$$\tau_2 = 2\zeta/\omega_n = 2\times0.707\times1.2\times10^4 = 1.178\times10^{-4} \quad 6\text{-}28$$

The resistor value is now be computed from Equation 6-16,

$$R_2 = \tau_2/C = 1.178\times10^{-4}/6.94\times10^{-7} = 169.68\ \Omega \quad 6\text{-}29$$

Figure 6.13 shows the root-locus analysis for our design. It appears similar to the second-order conventional phased-lock loop designs in Chapter 3.

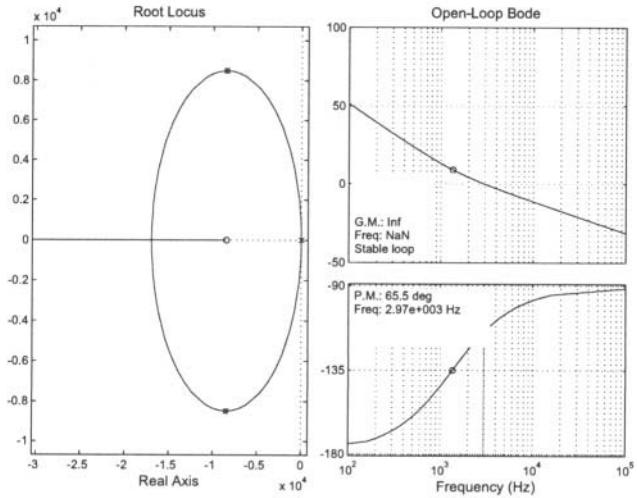


Figure 6.13 Second Order Charge Pump Root Locus

Next, we convert this to a third-order loop using Equation 6-25. The overall loop transfer function will be of the form shown in Equation 6-24. Using the previously computed values, we evaluate the root locus for **b=10.** The root locus is shown in Figure 6.14. (We caution that this transformation has different dynamics - $\zeta$ and $\omega_n$ have changed.)

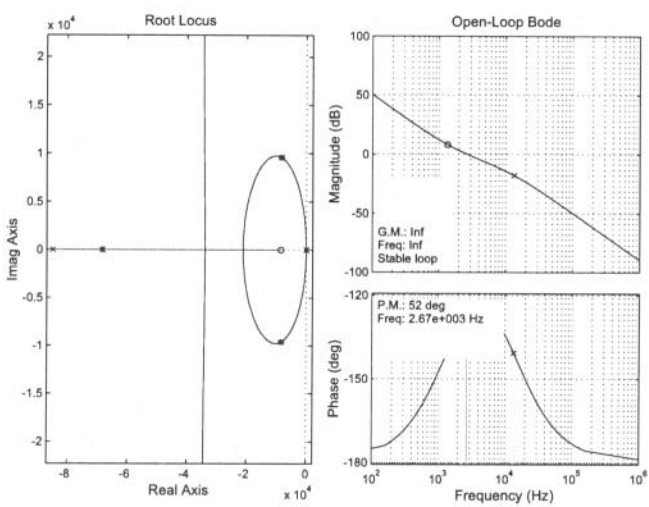


Figure 6.14 Root Locus of Third Order Charge Pump

## 6.3 Frequency Synthesizers

Digital counters are typically used to provide programmable output frequencies in synthesizer applications. Indirect synthesizers achieve selectable output frequencies through dividing the VCO and reference signals with programmable dividers before applying them to a phase detector [11]. A direct synthesizer switches offset frequencies into a mixer to achieve frequency programmability. Figure 6.15 shows a typical indirect synthesizer.

The synthesizer output frequency is computed as

$$f_{out} = \frac{f_r}{N_1} \times N_2 \qquad 6\text{-}30$$

The frequency step size of Figure 6.15's synthesizer has a limited quantization. As Equation 6-29 shows, the frequency step size is limited by the division ratios and reference frequency. As will be discussed in Chapter 13, it is generally desirable to keep the reference frequency as high as possible and division ratios small to achieve low phase noise.

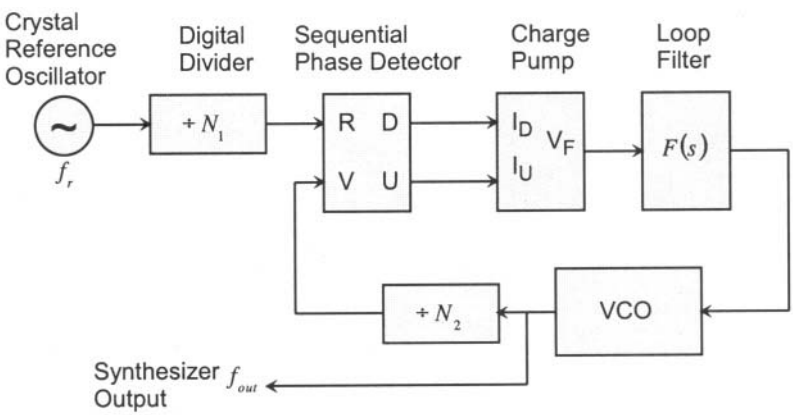


Figure 6.15 Indirect Frequency Synthesizer

The dilemma of generating fine frequency steps without a phase noise penalty is solved through the fractional-N synthesizer. The concept is to

divide the VCO by $N_1$ for a period of time, and then by the division ratio $N_2$ on a periodic basis. Figure 6.16 shows an implementation.

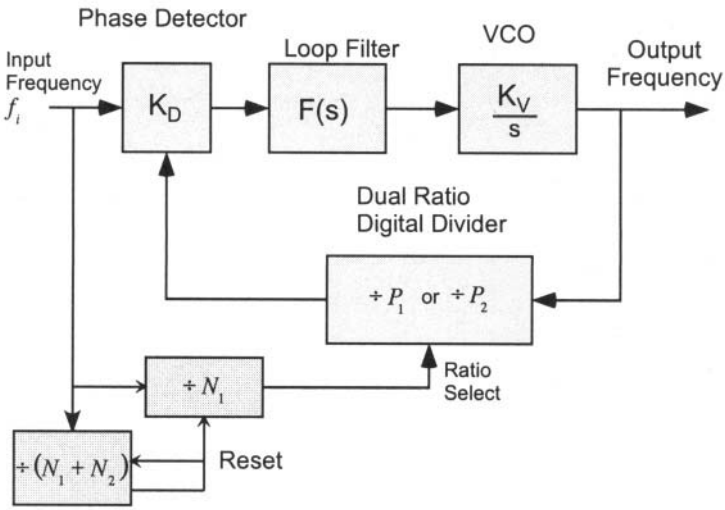


Figure 6.16 Fractional-N Synthesizer

In Figure 6.16, the digital divider divides by the division ratio $P_1$ for $N_1$ cycles of the input frequency, $f_i$. Then it divides by $P_2$ for $N_2$ cycles. Every $N_1 + N_2$ reference cycles, it resets and repeats the sequence. The output frequency of the fractional-N synthesizer in Figure 6.16 is computed as

$$f_{out} = \left( \frac{N_1}{N_1 + N_2} \times P_1 + \frac{N_2}{N_1 + N_2} \times P_2 \right) \times f_i \qquad 6\text{-}31$$

It is convenient if we rewrite the output frequency as [12]

$$f_{out} = P.frac \times f_i \qquad 6\text{-}32$$

P represents the integer portion of the divide ratio and frac represents the fractional component of the division ratio. Note that integer portion is written using $\lfloor \cdot \rfloor$ to represent the integer operation.

$$P = \left\lfloor \frac{N_1 \times P_1 + N_2 \times P_2}{N_1 + N_2} \right\rfloor \qquad 6\text{-}33$$

$$frac = \frac{N_1 \times P_1 + N_2 \times P_2}{N_1 + N_2} - P \qquad 6\text{-}34$$

In Equation 6-30, the proportion of time that the fixed counter is dividing is multiplied by the appropriate division ratio. Hence, the output frequency is the average frequency produced by the division ratios. Similar to the instantaneous adjustment pulses produced by the second-order charge pump, the fractional-N synthesizer of Figure 6.16 has large ripple on the output of the loop filter. The ripple is generated because the phase error is building up as shown in Figure 6.17

The phase error accumulation of Figure 6.17 is predictable and one technique to eliminate the ripple is to add a time-varying offset voltage or current into the loop filter. Many instrumentation-grade frequency synthesizers have corrected the ripple with an approach similar to that shown in Figure 6.18.

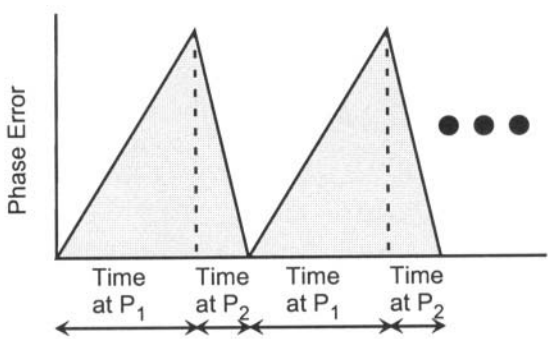


Figure 6.17 Phase Error Accumulation With Fractional-N Synthesizer

In Figure 6.18 we have replaced the two counters that previously controlled the division ratio with an accumulator. The accumulator overflow resets the accumulator and also selects the divide ratio. Because the accumulator's instantaneous value is equivalent to the phase error shown in Figure 6.17, it can also be used to provide a correction to the output of the phase detector. There are commercial components that perform all of these functions in a single device [13].

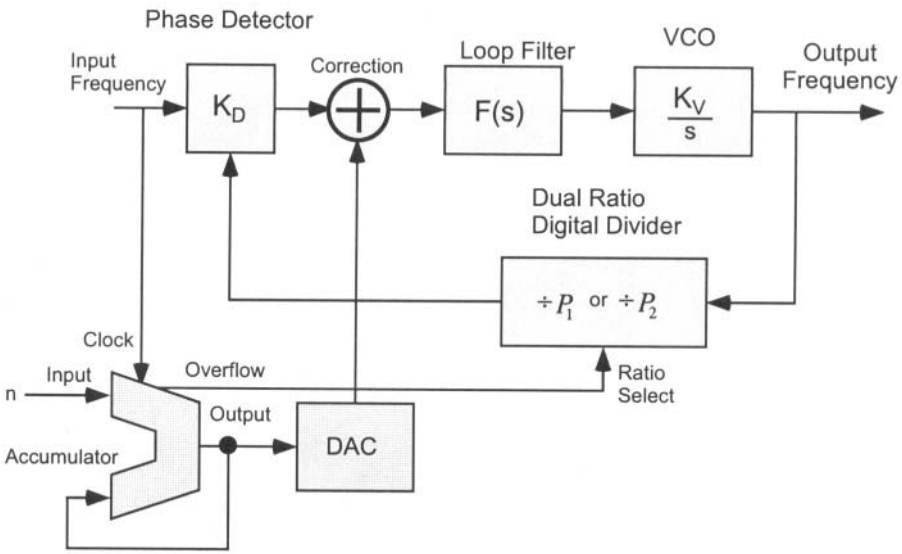


Figure 6.18 Fractional-N Synthesizer With Compensation

It has also been observed that the accumulator in Figure 6.18 can be replaced with a sigma-delta modulator to control the frequency divide ratio [12,14]. (In fact, the accumulator itself is a first-order sigma-delta modulator [14].) A delta-sigma factional-N phase-locked loop is shown in Figure 6.19.

A first-order sigma-delta modulator is known to have a high pattern noise for constant input signals such as the constant divide ratio in Figure 6.19. Higher-order sigma-delta modulators reduce the pattern noise significantly. Hence, by substituting a third-order sigma-delta modulator into Figure 6.19, we should expect much improved phase noise performance.

To understand how the sigma-delta modulator replaces the accumulator, consider the model of a divide-by (N,N+1) divider shown in Figure 6.20. By switching from a N to a N+1 division ratio, the divider is able to add

$2\pi$ radians of phase for one period of the input signal. The one-bit phase adjustment is followed by the $\div N$ divider. The input b(t) is the control signal on whether to adjust by $2\pi$.

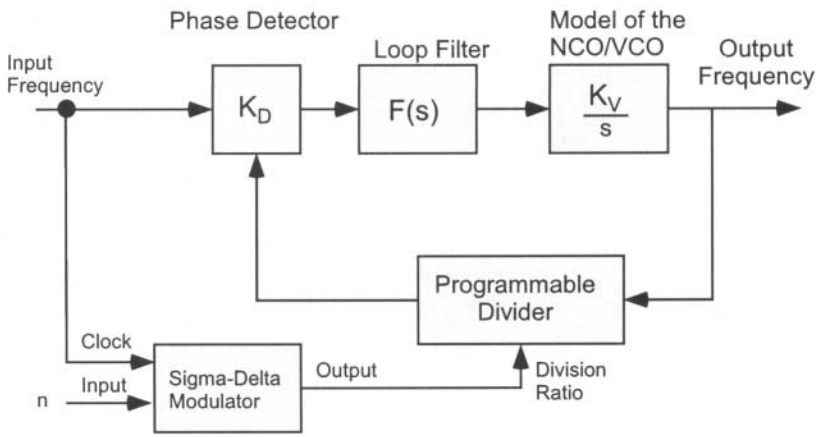


Figure 6.19 Sigma-Delta Fractional-N Synthesizer

The one-bit phase adjustment is coarse, and spectral improvements can naturally be made if we permit multi-bit phase adjustments. This is the concept of the sigma-delta fractional-N synthesizer. See [5,16] for detailed information on the design of sigma-delta modulators for fractional-n frequency synthesis.

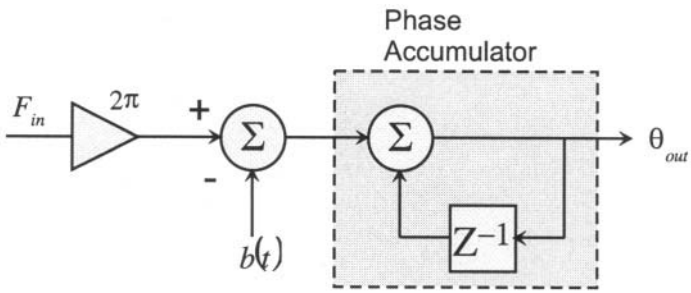


Figure 6.20 Model of Dual-Modulus Divider

## 6.4 Digital Counters

An important component of the frequency synthesizers discussed in Section 6.3 is the programmable counter. Although common digital dividers are sometimes used in frequency synthesizers, their phase noise characteristics are incompatible with system requirements. As a result, many frequency synthesizers are being developed with special low phase-noise digital counters.

There are two main categories of digital dividers: a) asynchronous and b) synchronous. In Figure 6.21a, the asynchronous counter operates by having each stage of the counter clock the succeeding stage. The advantage of this architecture is that each stage of the counter can be operated at ½ the current of the previous stage since the clock rate for succeeding stages is reduced by ½. This is an important advantage for low-power designs, but it comes at the cost of increased jitter. The jitter from one flip-flop is passed to the following flip-flop and becomes additive.

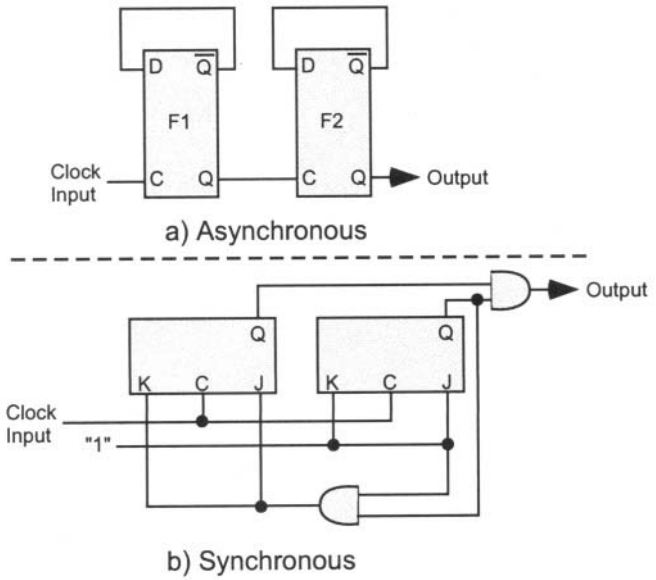


Figure 6.21 Architectural Differences for Digital Dividers

The digital divider of Figure 6.21b requires more current and components since all of the flip-flops are have the same clock. In contrast to the asynchronous design, the output jitter is not an accumulation of all the previous flip-flop stages.

Figure 6.22 shows a simple model for modeling the jitter in a flip-flop. The input clock waveform generally has some distribution amplification or buffering to all of the clock inputs. Associated with the buffer is thermal noise, which is modeled as a an additive source. The flip-flop's transition mechanism also has thermal noise which is modeled in Figure 6.22.

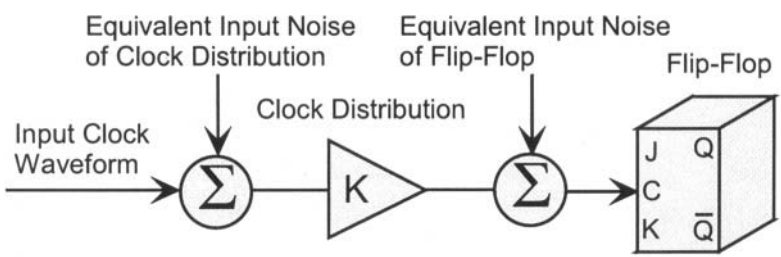


Figure 6.22 Jitter Model of a Flip-Flop

The thermal noise exists on the actual waveform used to transition the flip-flop. This could be a pre-charged gate, Schmitt trigger, etc. Regardless, the thermal noise on the clock waveform will be converted from amplitude to phase modulation. This causes jitter, or phase noise on the output of the flip-flop. Figure 6.23 illustrates the conversion of amplitude noise to timing jitter. Because the flip-flop's transition threshold is exceeded early in this diagram, the output will also change early. This causes phase noise in the output of digital counters.

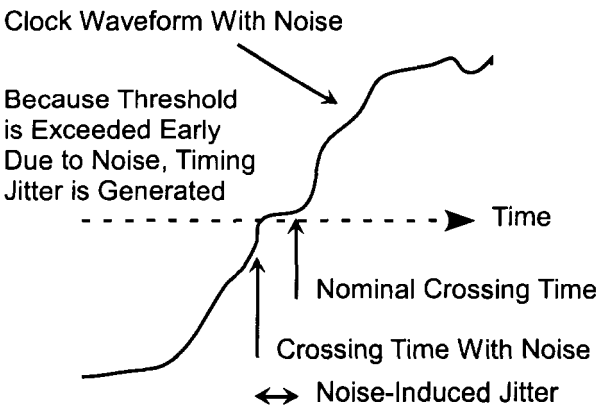


Figure 6.23 Input Clock to the Flip-Flop's Transition Mechanism

In Chapter 13, we describe the noise modeling techniques for the digital divider and provide equations for estimating the output phase noise of these components.

## 6.5 Delay-Locked Loops

Chapter 11 discusses the loops used for synchronization of data signals. Here we discuss a different application of delay-locked loops.

### 6.5.1 Introduction to Delay-Locked Loops

The fundamental design concept of the delay-locked loop is that there is no voltage-controlled oscillator in the loop. Replacing the VCO is a voltage-controlled delay line that changes the phase of the signal, but not the frequency. A common application of this phase-locked loop is to

synchronize clock edges within a digital system Figure 6.24 shows an application of delay-locked loops[17]. The idea is that ASIC 1 and ASIC 2 are allowed to drive the system bus on opposite edges of the system clock. Because the system bus is a high-speed interface, it is desirable to synchronize the output enables such that there is no contention. Bus contention, or both ASICs driving the system bus at the same time would result in large current spikes and possibly degrading the long-time reliability of the components [17].

In Figure 6.24, the time alignment of the clock edges is adjusted by error feedback from the phase detector to the voltage-controlled delay line. Recall in a conventional phase-locked loop, the VCO is adjusting frequency, but in a delay-locked loop, a VCDL adjusts phase. The Laplace transform for the VCDL is

$$VCDL(s) = K_O \frac{radians}{volt} \qquad 6\text{-}35$$

### 6.5.2 Voltage Controlled Delay Lines

There are several different approaches to the design of voltage controlled delay lines [17-20]. Some implementations use switches to select discrete phase steps, while others have continuously variable phase outputs.

Figure 6.25 shows a current-starved inverter stage [17]. The loop control voltage is applied to the current source which regulates the resistance of the inverting transistor. A large control voltage results in minimal delay because large currents are provided to the signal path's inverting stage.

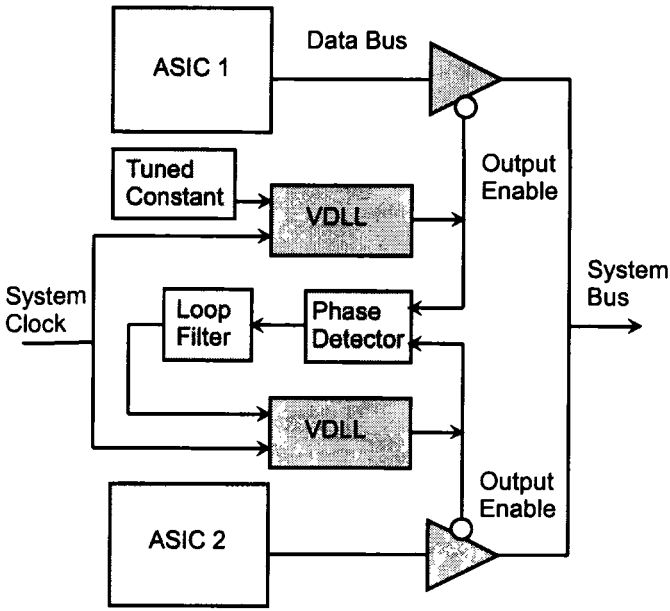


Figure 6.24 Example Application of Delay-Locked Loop

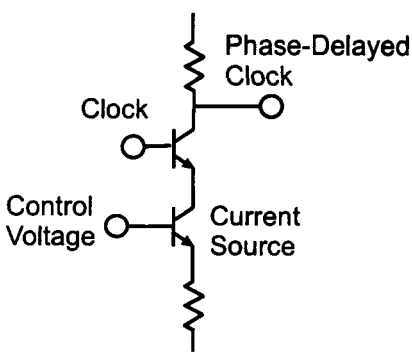


Figure 6.25 Current-Starved Inverter

Figure 6.26 shows a different VCDL. This is similar to a delay line previously used in a DRAM controller [5,17]. This circuit uses a shunt transistor to control the resistance in series with the shunt capacitance. A large control voltage will saturate the shunt transistor, resulting in a minimal resistance with the capacitor. This condition generates the maximum delay for the circuit.

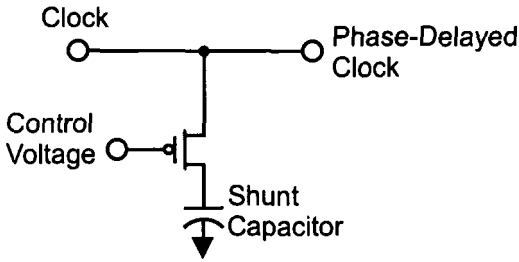


Figure 6.26 Shunt Capacitor Delay Stage

Often the delays of a single circuit are inadequate to adjust the signal by a complete 360°. To extend the range of VCDL, discrete switches can switch in fixed delays, or a continuous VCDL can be composed using a cascade of the delay stages shown Figure 6.25 or Figure 6.26. Such a cascaded phase adjustment is shown in Figure 6.27. (This is very similar to a ring oscillator where the required 180° phase shift is divided among the different stages.)

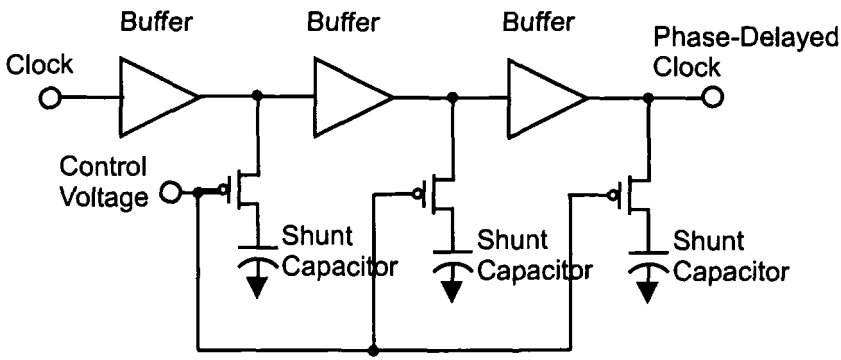


Figure 6.27 Cascade of Shunt Stages to Compose VCDL

### 6.5.3 Phase Detectors for Delay-Locked Loops

Several different phase detectors for delay-locked loops are discussed in the literature [17-20]. A very simple phase detector is the edge-triggered D-flip-flop to generate pulses interpolated by a charge pump. Figure 6.28 shows such a phase detector.

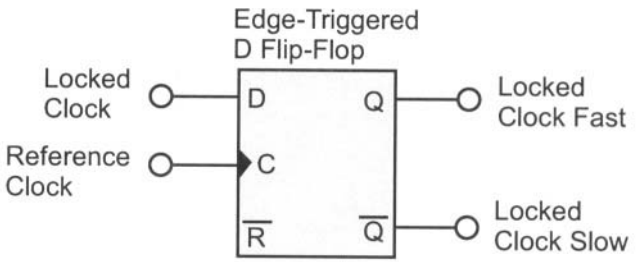


Figure 6.28 Example Phase Detector for Delay-Locked Loop [17]

Other phase detectors are possible [18-20]. In Figure 6.28, if the reference clock occurs prior to the clock we are attempting to lock, then the data input will be at a logic zero [17]. When the clock occurs, the flip-flop will have a logic zero on the "Q" output, and a logic "high" on the "Locked Clock Slow" output. Conversely if the locked clock transition occurs first, then the "Locked Clock Fast" output will have a logic "high". A charge pump can be used in cascade with this phase detector to convert the differential outputs into a single-ended VCDL drive.

The phase detector of Figure 6.28 provides only a binary indication of whether the locked clock is fast or slow. It does not provide an error signal proportional to the phase error as with a conventional phase-locked loop. As a result, the resulting loop is called a bang-bang control loop.

The residential heating/air conditioning system is a bang-bang control loop because the thermostat will turn the air conditioner either off or on. A deadband region where no temperature adjustments are made prevents constant cycling of the air conditioner.

A disadvantage of this loop is the oscillations in output error or "chatter" – continual small adjustments. The "chatter" can be reduced by increasing the deadband – error region over which no adjustments are made, but this increases the peak-to-peak output error.

## *Example 6.2 DLL Design Example*

Instead of a bang-bang control loop, design a delay-locked loop using a sequential (phase-frequency) detector with a charge pump.

$K_o = \frac{\pi}{2} radians/V$, and $I_p = 10 \times 10^{-3}\ A$. Design a first order loop that allows the loop to correct a $\pi/16$ phase step in 2 ms.

Note that since the VCDL, is really a phase adjustor expressed directly in radians rather than frequency, the Laplace Transform for the VCDL is simply $K_o$ - there is no denominator of 's' as in a conventional phase-locked loop. We can modify the charge pump Equation 6-12 to

$$H_o(s) \equiv \frac{\theta_o(s)}{\theta_i(s)} = v_c(s) K_o = \frac{K_o I_p z_f(s)}{2\pi + K_o I_p z_f(s)} \qquad 6\text{-}36$$

For this example, the charge pump filter is a series resistor and capacitor. The load impedance for the charge pump is written as

$$Z_f(s) = R + \frac{1}{sC} = \frac{RsC+1}{sC} \equiv \frac{\tau s + 1}{sC} \qquad 6\text{-}37$$

Substituting Equation 6-37 into 6-36 provides the loop response.

$$H_o(s) = \frac{K_o I_p (sRC+1)}{2\pi sC + K_o I_p (sRC+1)} \qquad 6\text{-}38$$

The time response is computed as

$$y(t) = \mathcal{L}^{-1}\left\{\frac{\theta}{s} H_o(s)\right\} \qquad 6\text{-}39$$

Performing the inverse Laplace Transform on Equation 6-38,

$$y(t) = \theta\left(1 - \frac{2\pi}{2\pi + K_o R I_p} Exp\left\{\frac{-K_o I_p t}{2\pi C + K_o R I_p C}\right\}\right) \qquad 6\text{-}40$$

A reasonable criteria for computing the phase-lock time is to compute the time required for Equation 6-40 to reach 90% of the steady-state value. Equivalently we can solve

$$0.1 = \frac{2\pi}{2\pi + K_o R I_p} Exp\left\{\frac{-K_o I_p t}{2\pi C + K_o R I_p C}\right\} \qquad 6\text{-}41$$

Solving Equation 6-40, we obtain

$$t = \frac{C\,Log\left(\left(0.0159155\left(6.28319 + K_o R I_p\right)\right)\right)\left(-6.28319 - K_o R I_p\right)}{K_o I_p} \qquad 6\text{-}42$$

Equation 6-42 suggests that the capacitor value C is the easiest variable to solve. (The variable R appears inside the Log() function.) Hence we select a resistor value R=2000 ohms, substitute the other parameters (including t) into Equation 6-42 and obtain $C = 1.63\ \mu F$. The loop's time response is shown in Figure 6.29.

Note that the phase step $\theta = \pi/16 \approx 0.196$. The loop has settled to $\theta_o \approx 0.176 = 0.9 \times \theta$ within 2 ms, achieving the design requirement.

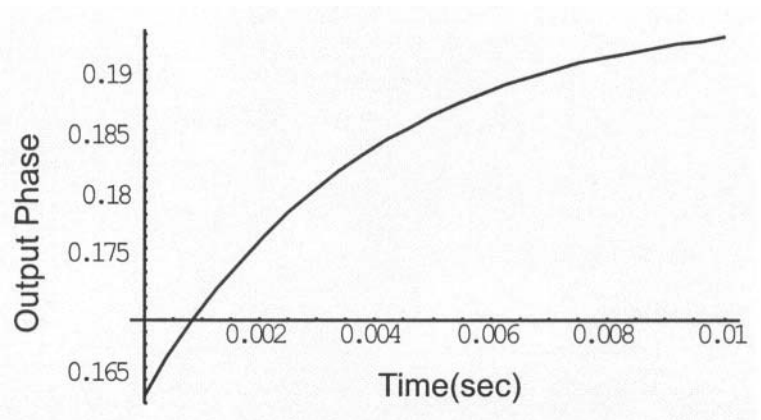


Figure 6.29 Time Response of Delay-Locked Loop Example

## 6.6 References

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# 7

# Digital Transformations of Analog PLLs

To begin our study of the digital phase-locked loop, we will begin by translating the analog loop equations of Chapters 2 and 3 to the discrete-time domain. A reader may question this approach, so we quote Oppenheim and Schafer's explanation of translating analog filters to the digital domain [1].

> 1. The art of analog filter design is highly advanced and, since useful results can be achieved, it is advantageous to utilize the design procedures already developed for analog filters.
>
> 2. Many useful analog design methods have relatively simple closed-form design formulas. Therefore, digital filter design methods based on such analog design formulas are rather simple to implement.
>
> 3. In many applications it is of interest to use a digital filter to simulate the performance of an analog linear time-invariant filter.

We believe the same statements are valid for converting analog phase-locked loop designs to the digital domain.

## 7.1 Analog Loop Transformations

We will show how the analog configurations of Chapter 2 can be transformed directly into corresponding discrete versions. There are different transformations possible, the most noteworthy being the backward difference and bilinear transformations. The time-domain equations will be emphasized similar to our development of the analog loops.

### 7.1.1. Backward Difference Transformations

Figure 7.1 reviews the block diagram of an analog phase-locked loop. The presence of the VCO's transfer function of $V(s)=\frac{K_d}{s}$ in the analog phase-locked loop yields a time-domain solution in the form of a differential equation. We repeat here the differential equation for the first-order analog phase-locked loop.

$$error'(t)+\sqrt{2P}K\,error(t)=\sqrt{2P}\theta'(t) \qquad 7\text{-}1$$

error(t) represents the phase error of the loop, and $\theta(t)$ is the input signal.

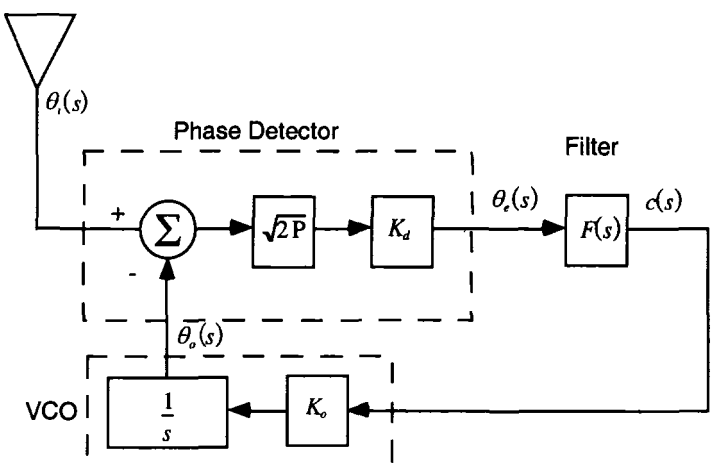


Figure 7.1 Block Diagram of the Analog Phase-Locked Loop

As a first step in converting Equation 7-1 to a discrete-time form, we replace the continuous time variable, t, with the discrete representation with nT, and approximate the derivative

$$\frac{d\,error(nT)}{dt} \approx \frac{error(nT) - error((n-1)T)}{T} \qquad 7\text{-}2$$

From elementary calculus, Equation 7-2 is the definition of a derivative in the limit as the distance, $\Delta t$ between the two points vanishes. For this application it implies that the loop's error function, error(t), is relatively smooth and the sampling instants are not too far apart. We will also approximate $\theta'(t)$ with a similar expression. Note that we are working directly with the time samples of the signals present inside the loop.

With the sampled equivalent of Equation 7-1, and substituting in Equation 7-2, we obtain

$$\frac{error(n) - error(n-1)}{T} + \sqrt{2P}\,K\,error(n) = \sqrt{2P}\,\frac{\theta(n) - \theta(n-1)}{T} \qquad 7\text{-}3$$

Note the notation of $error(n) = error(nT)$, which we adopt to reduce the physical size of the equations. Some algebraic simplification provides

$$error(n) = \frac{\sqrt{2P}\{\theta(n) - \theta(n-1)\} + error(n-1)}{1 + \sqrt{2P}\,KT} \qquad 7\text{-}4$$

Equation 7-4 is a time-domain representation of a first order digital loop which was obtained from approximating the derivative in the differential equation for an analog phase-locked loop. By inspection of Equation 7-4, we can draw the block diagram equivalent of the digital phase-locked loop. The baseband digital loop equivalent of Figure 2.2 is shown in Figure 7.2. We will draw the counterpart to Figure 2.1 after some discussion.

The symbol $Z^{-1}$ in Figure 7.2 is the customary signal processing symbol for a one-sample time delay. (Some control systems literature use the symbol T for the time delay element.) Note the $Z^{-1}$ blocks in Figure 7.1 are not both facing in the same direction. Only the $Z^{-1}$ on the right-hand side is feeding back into the loop, which is the implementation of an integrator. The first order loop of Figure 7.2 thus has only one integrator.

With the introduction of the symbol Z, it is appropriate to perform the Z-transform of Equation 7-4.

$$Error(z)\left(1+\sqrt{2P}KT-z^{-1}\right)=\theta(z)\sqrt{2P}\left(1-z^{-1}\right) \qquad 7\text{-}5$$

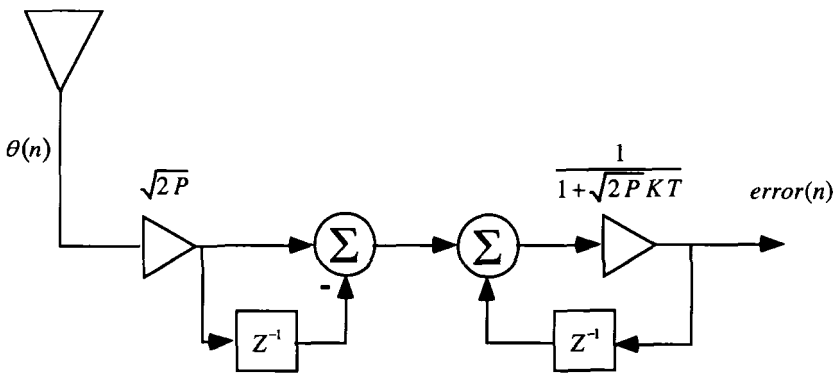


Figure 7.2 Digital First-Order Phase-locked Loop

As with the analog phase-locked loop, we compute the transfer function

$$H(z)=\frac{Error(z)}{\theta(z)}=\frac{\sqrt{2P}\left(1-z^{-1}\right)}{1+\sqrt{2P}KT-z^{-1}} \qquad 7\text{-}6$$

We simplify to remove the $z^{-1}$ terms,

$$H(z)=\frac{\sqrt{2P}}{1+\sqrt{2P}KT}\,\frac{z-1}{z-\dfrac{1}{1+\sqrt{2P}KT}} \qquad 7\text{-}7$$

To develop our architecture of Figure 7.1, we derived a difference equation, Equation 7-2. This result of this technique is called a backward difference [1,2,5]. The continuous-time transfer function of Equation 7-1 is

$$H(s) = \frac{\sqrt{2P}\,s}{s + \sqrt{2P}K} \qquad 7\text{-}8$$

Note the similarity between Equation 7-7 and Equation 7-8. In general, the backward difference equivalent of a s-domain transfer function is obtained by the substitution

$$H(z) = H(s)\Big|_{s=\frac{1-z^{-1}}{T_s}} \qquad 7\text{-}9$$

In retrospect, we should have suspected this from the digital loop representation of Figure 7.2. Recall the first order analog loop has a single integrator, which is the VCO function. In Figure 7.2, the last summation function represents an integrator. The relationship of Equation 7-9 allows us to rapidly develop a digital phase-locked loop by merely performing substitution of variables.

Equation 7-9 is based upon the backward difference approximation of a derivative (Equation 7-2). From calculus, we know it is a good approximation only if the function error(t) changes very slowly over the interval $T_s$. Heuristically, the mapping from $s \rightarrow z$ should become distorted as the sampling rate decreases because the approximation of the derivative becomes worse as the data samples become farther apart.

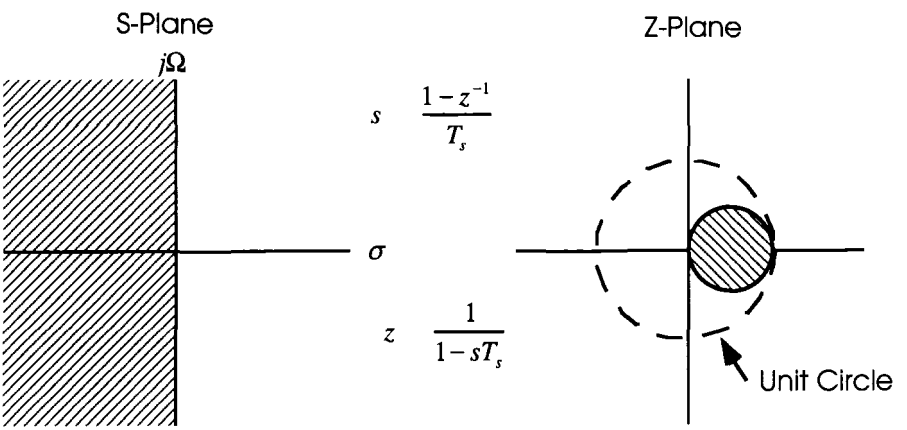


Figure 7.3 Mapping of Laplace Function to Z-Domain With Backward Difference Equation [2]

Figure 7.3 shows the mapping from s to z with the backward difference equation. Unfortunately, the backward difference mapping does not use all of the z-plane's unit circle. We note that all of the left-hand s-plane is mapped into the small circle in the right-half of the unit circle. Although we have some distortion in the mapping, any stable analog transfer function is mapped to a stable discrete-time function.

### 7.1.2. Bilinear Transformations

Once again returning to calculus theorems, we observe that the function error(t) can be represented exactly by the integral in Equation 7-10.

$$error(t) = \int_{t_0}^{t} error'(\tau)d\tau + error(t_0) \qquad 7\text{-}10$$

We can approximate the integral in Equation 7-10 with a trapezoidal approximation [3]. This approximation allows us to approximate the function, error(t) with the linear form of Equation 7-10. The interval of time between samples is denoted $T_S$.

$$error(n) = error(n-1) + \frac{T_s}{2}\{error'(n) + error'(n-1)\} \qquad 7\text{-}11$$

Equation 7-1 is rewritten to isolate the *error'*(n) on the left-hand side.

$$error'(n) = \sqrt{2\ P}\theta'(n) - \sqrt{2\ P}K error(n) \qquad 7\text{-}12$$

We substitute Equation 7-12 into the braces of Equation 7-11 which gives a new difference equation based upon the trapezoidal approximation of an integral.

$$error(n) - error(n-1) = \frac{T_S}{2}\left[\begin{array}{l}\sqrt{2P}\theta'(n) - \sqrt{2P}\ K\ error(n) \\ +\sqrt{2P}\theta'(n-1) - \sqrt{2P}\ K\ error(n-1)\end{array}\right] \qquad 7\text{-}13$$

Rearranging some terms, we isolate the derivative of the input on the right hand side of Equation 7-13.

$$error(n)\left(1+\frac{T_S}{2}\sqrt{2P}K\right)-error(n-1)\left(1-\frac{T_S}{2}\sqrt{2P}K\right) = \frac{T_S}{2}\sqrt{2P}\left[\theta'(n)+\theta'(n-1)\right] \quad 7\text{-}14$$

We recognize the $[\theta'(n)+\theta'(n-1)]$ term is similar to the trapezoidal approximation of an integral (Equation 7-11). We express the term $\frac{T_S}{2}\sqrt{2P}[\theta'(n)+\theta'(n-1)]$ in the form of Equation 7-11.

$$\frac{T_S}{2}\sqrt{2P}\left[\theta'(n)+\theta'(n-1)\right]=\sqrt{2P}\left[\theta(n)-\theta(n-1)\right] \quad 7\text{-}15$$

Equation 7-15 represents the right hand side of Equation 7-14, and is substituted to complete the difference equation. The resulting equation is now free of integrals and derivatives.

$$error(n)\left(1+\frac{T_S}{2}\sqrt{2P}K\right)-error(n-1)\left(1-\frac{T_S}{2}\sqrt{2P}K\right) = \sqrt{2P}\left[\theta(n)-\theta(n-1)\right] \quad 7\text{-}16$$

Now we take the Z-Transform of Equation 7-16,

$$Error(z)\left\{\left(1+\frac{T_S}{2}\sqrt{2P}K\right)-z^{-1}\left(1-\frac{T_S}{2}\sqrt{2P}K\right)\right\} = \sqrt{2P}\theta(z)\left[1-z^{-1}\right] \quad 7\text{-}17$$

Equation 7-17 is rearranged to provide a transfer function of the form

$$H[z]=\frac{2\sqrt{2P}}{2+T_S\sqrt{2P}K}\frac{z-1}{z+\frac{-2+T_S\sqrt{2P}K}{2+T_S\sqrt{2P}K}} \quad 7\text{-}18$$

We leave as an exercise for the reader to show that Equation 7-18 can be represented by Figure 7.2 with some minor scalar changes. More interesting however, is the conversion between the continuous-time function Equation 7-8 and the discrete time form of Equation 7-18. We find that in general, the trapezoidal rule yields a transfer function of the form

$$H(z) = H(s)\Big|_{s=\frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}}} \qquad 7\text{-}19$$

This is also known as the bilinear transformation, or in the Control Systems literature, as Tustin's Rule [5]. Recall the bilinear transfer function of Equation 7-18 was obtained by first generating a sampled version of the continuous time equation and then approximating the integrals in the differential equation with a trapezoidal approximation.

The bilinear transformation has a different mapping from the analog domain to the discrete-time and is shown in Figure 7.4. The primary advantage of the bilinear transform is that it maps the entire left-hand plane of the S-plane into the unit circle. This is the best we could hope for, because all of the stable unit circle is utilized. Any stable transform in the continuous domain is mapped to a stable Z-transform.

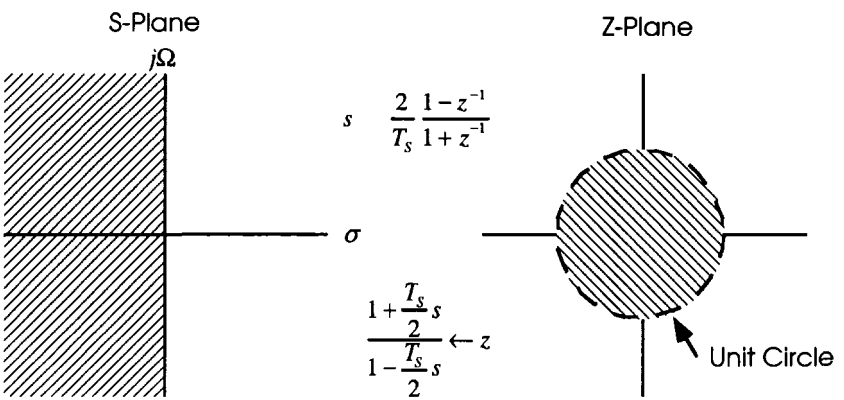


Figure 7.4 Mapping of Analog Function to Z-Domain With the Bilinear Transform [2]

Of special interest is the non-linear mapping of frequency from the continuous-time transfer function to the discrete time transfer function. Visually we see that an infinite area in the S-plane is mapped to a finite unit circle in the Z-plane. The bilinear mapping in Equation 7-19 is

$$s = \frac{2}{T_S}\frac{1-z^{-1}}{1+z^{-1}} \qquad 7\text{-}20$$

If we let $s = j\Omega$ and $z = e^{j\omega T_S}$ and substitute into Equation 7-20, we obtain the relationship between continuous frequency and discrete frequency.

$$j\Omega = \frac{2}{T_S}\frac{1-e^{-j\omega T_S}}{1+e^{-j\omega T_S}} \qquad 7\text{-}21$$

Trigonometric identities and algebraic simplification yields [7-8]

$$\Omega = \frac{2}{T_S}\tan\left(\frac{\omega T_S}{2}\right) \qquad 7\text{-}22$$

Recall that for $\theta << 1$, $\tan(\theta) \approx \theta$. Thus in Equation 7-22, as long as the product of $\omega T_S << 1$, then there is approximately linear frequency mapping between the s-plane and the z-plane. When this condition is not true, it implies the loop frequency is approaching the sampling frequency, and the consequence is nonlinear mapping. Heuristically this is reasonable, because as the time between samples increases, the trapezoidal approximation of the integral degrades.

The nonlinear mapping implies that the frequency breakpoints of filters will be different between the analog H(s) and the digital H(z). Sometimes the analog filter's transfer function is "pre-warped" [5] to obtain the desired digital frequency breakpoint. In other words, if we want the digital loop to have a cutoff frequency of $\omega_c$, then we slightly change the cutoff frequency, $\Omega_c$, of the analog filter. To pre-warp the analog system, we use the bilinear transformation with a mapping constant, C.

$$H(z) = H(s)\Big|_{s=C\frac{1-z^{-1}}{1+z^{-1}}} \qquad 7\text{-}23$$

In Equation 7-23, we have replaced the $\frac{2}{T_S}$ term with the mapping constant C, defined as

$$\frac{\Omega}{\tan\left(\frac{\omega T_S}{2}\right)} = C \qquad 7\text{-}24$$

where $\Omega$ is analog frequency (radians/sec)
$\omega$ is digital frequency (radians/sec)

By substituting the appropriate frequencies and sampling period, we can obtain the constant required for the specified frequency cutoff. The appearance of two frequency variables may appear troubling at first. However, when we discuss discrete loop filters, we will show how the analog prototype filters are usually specified with $\Omega = 1$. Equation 7-24 then provides a convenient method for rapidly obtaining a specified discrete frequency from an analog prototype.

## *Example 7.1*

We want to design a first order digital loop with a noise bandwidth of 10 Hz. Our sampling frequency is 50 Hz, the VCO and phase detector gains are unity. Assume 0 dBm input power. Design the digital loop.

From Figure 3.23, we know that $B_L = \frac{\sqrt{2P}K_o K_d K}{4}$. Solving for our analog gain, K, we obtain K= 126.49. The analog transfer function is derived from Equation 7-8. Substituting Equation 7-23 into Equation 7-8, we obtain

$$H(z) = \frac{C(z-1)}{C(z-1)+40(z+1)} \qquad 7\text{-}25$$

We are going to make the approximation that the loop cutoff frequency is related to the noise bandwidth by the relation [4] (true for a first-order Butterworth filter)

$$f_C = \frac{2}{\pi} B_L \qquad 7\text{-}26$$

Equation 7-26 allows us to obtain the cutoff frequency of our loop as $f_C = 6.3662$. Now using Equation 7-24, we solve for the pre-warping constant, C, obtaining $C = 94.6089$. We note that if we had used the true trapezoidal substitution of Equation 7-20, we would have obtained $C = 100$, which indicates that our frequency warping is minimal with the loop filter's frequency and sampling rate. Substituting $C = 94.6089$ into Equation 7-25 provides our digital phase-locked loop's transfer function.

$$H(z)_{bilinear} = \frac{94.61(z-1)}{94.61(z-1)+40(z+1)} \qquad 7\text{-}27$$

Using the backward difference equation, Equation 7-9, and the first order loop of Equation 7-8 gives a different transfer function.

$$H_{backDiff}(z) = \frac{z-1}{2001z-1} \qquad 7\text{-}28$$

We are interested in whether our digital loop response is similar to the analog loops we have previously analyzed. Suppose that the input is a step function which corresponds to $\theta(z) = \frac{z}{z-1}$, The response is $Y(z) = H(z)\theta(z)$ which we compute for the bilinear transformation of Equation 7-27 as

$$Y(z) = \frac{94.61(z-1)}{94.61(z-1)+40(z+1)} \qquad 7\text{-}29$$

The inverse Z-Transform of the step response is

$$y(n)_{step} = 0.7028 + 0.406^n u[n] \qquad 7\text{-}30$$

Although we will discuss loop performance later, we plot the step response of this first order loop using the time-domain representation of Equation 7-30 in Figure 7.5. As a reference, the corresponding analog loop response is plotted along with the digital loop response. The analog response

was obtained by performing the inverse Laplace transform of the response of the analog system with a step of phase input.

In this example, we approximated the noise bandwidth of the loop. In Chapter 8 we will show how to obtain the actual noise bandwidth of a digital loop through contour integration of the closed loop transfer function.

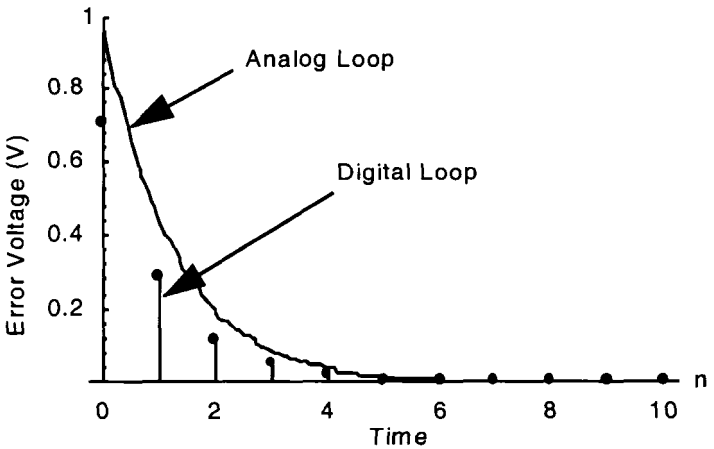


Figure 7.5 Step Response of Digital First Order Loop

## *Example 7.2*

Recall the second order analog phase-locked loop of Example 2-1. The loop specifications are:

Natural Frequency (Specified) 3 Hz, Damping Factor (Specified) 0.707 Sampling Frequency (Specified) 50 Hz

Design the digital loop using the bilinear transformation of the active filter loop's second order transform. Plot the error response of the digital loop to an input step in phase.

The second order loop's transform is repeated below for convenience.

$$H_2(s) = \frac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2} \qquad 7\text{-}31$$

We will compute the bilinear transform of Equation 7-31, but we caution that this is not the error response. It represents the transfer function of $\frac{\theta_o(s)}{\theta_i(s)}$, not $\frac{\theta_e(s)}{\theta_i(s)}$, which is required for computing the error response. We perform the bilinear transformation of Equation 7-31 with Equation 7-23.

$$H(z) = \frac{\omega_n^2 + 2\omega_n^2 z - 2C\omega_n\zeta + z^2(\omega_n^2 + 2C\omega_n\zeta)}{C^2 + \omega_n^2 + z(2\omega_n^2 - 2C^2) - 2C\omega_n\zeta + z^2(C^2 + \omega_n^2 + 2C\omega_n\zeta)} \qquad 7\text{-}32$$

We choose to let $C = 2/T_S$, which corresponds to the true bilinear transformation. Substituting in the specific design parameters yields

$$H(z) = \frac{-2310 + 710.6z + 3021z^2}{7690 - 19290z + 13020z^2} \qquad 7\text{-}33$$

To plot the error response, recall that $H_e(z) \equiv 1 - H(z)$. We multiply $H_e(z)$ with the step transform, $\frac{z}{z-1}$, to obtain

$$Y(z) = \frac{z}{z-1}H_E(z) = \frac{-z + z^2}{1 - 2.532z + 1.675z^2} \qquad 7\text{-}34$$

The inverse Z-Transform of Equation 7-34 is shown in Equation 7-35 and plotted in Figure 7.6. The digital loop obtained through the bilinear transformation is compared against the analog loop designed in Example 2.1. The continuous time loop is shown as a continuous line and the digital loop is shown with discrete "lollipops".

$$\begin{aligned} y(n) &= (0.298474 - j0.4575)(0.7561 - j0.1592)^n u[n] \\ &+ (0.298474 + j0.4575)(0.7561 + j0.1592)^n u[n] \end{aligned} \qquad 7\text{-}35$$

It is interesting to compare the second order digital loop to the analog prototype. The step response of the corresponding analog transfer function is

shown in Figure 7.6. For a loop with $\zeta = 0.7$, we note from Figure 2.8, that the peak undershoot occurs at $\omega_n T \approx 2.4$. In Figure 7.6, note that the peak undershoot occurs just prior to **n=6,** which corresponds to $T = \frac{6}{50}$. (The time between samples is $\frac{1}{50}$, obtained from the sampling frequency of 50 Hz.)

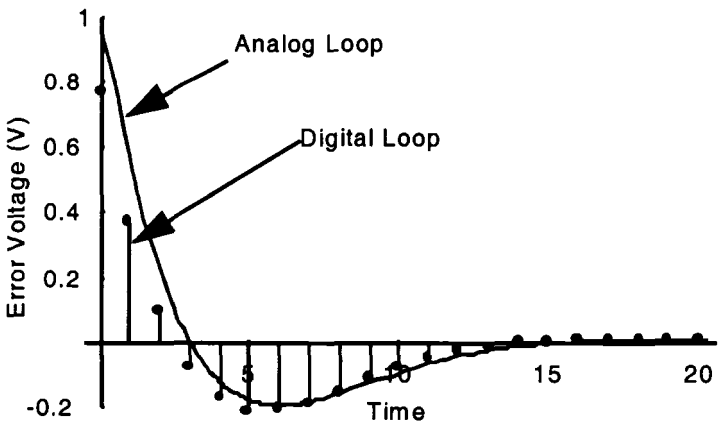


Figure 7.6 Error Response of Second Order Digital Loop

From the digital loop response, we compute $\omega_n T = 2.3$. This compares favorably to the original analog design. Visually, the two different loops appear very similar. In this situation, the digital loop can be modeled by the analog equations of Chapter 2. However, these are benign conditions with a high sampling rate. Instead of approximating the performance with analog loop equations, we encourage using the digital analysis presented later in this text to more accurately predict the performance of the digital loops.

As with Example 7.1, we can obtain a backward difference transformation of the second order analog phase-locked loop. Although we leave the actual development for the problems, we provide the corresponding transfer functions

$$H(z)=\frac{-2T_S\omega_n\zeta z+z^2\left(T_S{}^2\omega_n{}^2+2T_S\omega_n\zeta\right)}{1+z\left(-2-2T_S\omega_n\zeta\right)+z^2\left(1+T_S{}^2\omega_n{}^2+2T_S\omega_n\zeta\right)} \qquad 7\text{-}36$$

$$H_E(z)=\frac{1-2z+z^2}{1+z\left(-2-2\,T_S\omega_n\zeta\right)+z^2\left(1+T_S{}^2\omega_n{}^2+2\,T_S\omega_n\zeta\right)} \qquad 7\text{-}37$$

## 7.2 All Digital Loops With Block Elements

We have just developed transfer functions for phase-locked loops using the backward difference and bilinear transformations. Sometimes the resulting transfer functions can be implemented in a system, but often we need individual components. As an example, recall the mixer in our first configuration of Figure 2.1. The mixer is necessary to remove the frequency difference between the local oscillator and the input signal. In the linearization of Figure 2.2, we replaced the mixer with a summation element. As we discussed, this is appropriate for analysis, but it doesn't provide the insight as to how we can actually build a digital phase-locked loop. Figure 7.7 shows an analog loop with block components that we must convert to a digital form.

In Chapter 4, we showed how the delays incurred by a simple sample-and-hold can alter the performance and stability of the phase-locked loop. Therefore, it is important that we be able to analyze the actual loop that we construct. Of course, when we use the verb construct, it is implicit that the construction can merely be lines of computer code, or actual physical hardware.

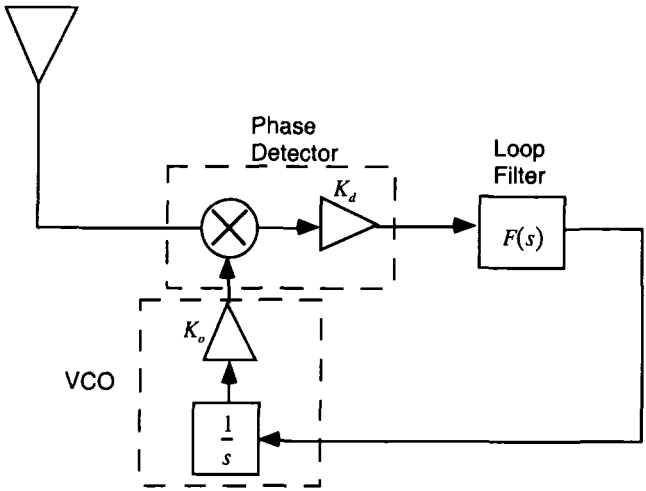


Figure 7.7 Analog Loop With Block Components

### 7.2.1 Phase Detector

There are many different configurations for phase detectors. We will discuss particular configurations in Chapter 8 and data synchronizers in Chapter 11. For our preliminary analysis in this chapter, we merely consider the phase detector multiplies the input and reference signals. The input has the form

$$s(n) = \sqrt{2P}\sin\left(2\pi f_c n T_S\right) \qquad 7\text{-}38$$

The VCO has an output of the form

$$v(n) = 2\cos\left(2\pi f_c n T_S + \theta(n)\right) \qquad 7\text{-}39$$

The product of the input and VCO is

$$e(n) = -\sqrt{2P}\sin\left(\theta(n)\right) + \sqrt{2P}\sin\left(4\pi f_c n T_S + \theta(n)\right) \qquad 7\text{-}40$$

Note the phase detector output of Equation 7-40 includes the actual error term, $\theta(n)$, as well as a double frequency term. If the double frequency

term, $4\pi f_c$ , is within the loop bandwidth, then a lowpass filter is necessary to eliminate interference for loop operation.

## 7.3 Loop Filter Transformations

The quotation from Oppenheim and Schafer [1] at the beginning of this chapter should be repeated here. There are many, many, different digital filter configurations possible. Decades of research and analysis for analog phase-locked loops have provided a legacy of analog filters that are optimized for phase-locked loops. Our approach is to perform transformations of the analog filters.

### 7.3.1. First Order Loop Filters

The first order loop filters are simply gain stages. Like their analog counterparts, there is no frequency selectivity to the digital first order filters. (There is also no delay.) Consequently, we represent these filters as a scalar gain, $K_f$

### 7.3.2. Second Order Loop Filters

Because the active second-order loop filter is superior to the passive implementation, we will analyze it only. The passive loop filter analysis is left for the problems. (Note there are some applications which can benefit from the "leaky integrator" form of the passive loop filter.)

From Chapter 2, the second order active loop filter has the form

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s} \qquad 7\text{-}41$$

(An operational amplifier implementation will yield a minus sign in front of Equation 7-41, which must be accounted for in an actual digital loop.) The backward difference transformation of this filter is derived from Equations 7-41 and 7-9.

$$F_{back}(z) = \frac{-\tau_2 + z(T_S + \tau_2)}{\tau_1 (z-1)} \qquad 7\text{-}42$$

Using Equation 7-19, we compute the bilinear transformation of the filter as

$$F_{bilinear}(z) = \frac{(1-\tau_2 C)z^{-1} + 1 + \tau_2 C}{\tau_1 C(1-z^{-1})} = \frac{1-\tau_2 C + z(1+\tau_2 C)}{\tau_1 C(z-1)} \qquad 7\text{-}43$$

This form of the filter uses the variable $z^{-1}$, instead of **z**. This form permits filter construction by inspection, which we will demonstrate in Example 7.3. The latter form is typically used for the complete transfer function of the phase-locked loop.

It is difficult to directly compare the two filter implementations of Equations 7-42 and 7-43. There are four variables in the two equations, and each transformation has a unique variable. As Oppenheim and Schafer note [1], a high sampling rate is required for an accurate approximation of the analog filter with the backward difference transformation.

The bilinear transformation of the filter can be expressed directly in terms of the loop parameters as

$$F_{bilinear}(z) = \frac{16 B_L^{\,2} \zeta^2 \left( 2(z+1) + f_s (z-1) \sqrt{\dfrac{(1+4\zeta^2)^2}{B_L^{\,2}}} \right)}{f_s K_d K_o \sqrt{2P}\,(z-1)(1+4\zeta^2)^2} \qquad 7\text{-}44$$

Where $B_L$ is the loop bandwidth defined in Chapter 4, and $f_s$ is the sampling rate for the digital phase-locked loop.

### 7.3.3 Impulse Invariance Design

An alternative to the bilinear transformation of an analog filter is impulse invariance design. Figure 7.8 shows the concept. We compute the impulse response of the prototype analog filter and then design the digital filter to match that response.

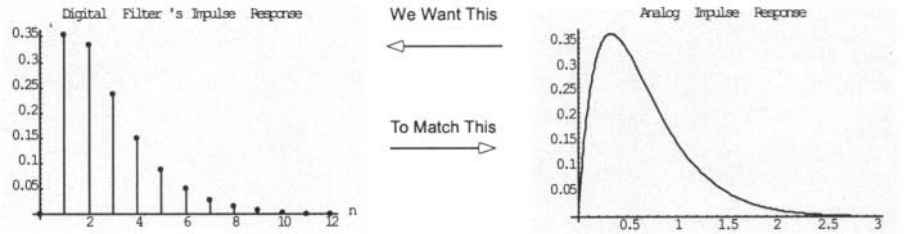


Figure 7.8 Impulse Invariance Design

If $F(s)$ is the analog loop filter's S-Transform, we obtain the impulse response from the inverse Laplace transform,

$$f(t) = \mathcal{L}^{-1}[F(s)] \qquad 7\text{-}45$$

The desired digital filter transfer function is [3]

$$F(z) = T\,\mathcal{Z}(f(t)) \qquad 7\text{-}46$$

---

## *Example 7.3*

Compute the digital loop filter using the impulse invariance design of $F(s) = \dfrac{1}{\tau_1 s + 1}$.

We compute the impulse response of the analog prototype as

$$f(t) = L^{-1}\left[\frac{1}{\tau_1 s + 1}\right] = \frac{1}{\tau_1} e^{-t/\tau_1} \qquad 7\text{-}47$$

We apply the Z-Transform to Equation 7-47,

$$F(z) = T\,\mathcal{Z}\left(\frac{1}{\tau_1} e^{-t/\tau_1}\right) = T\,\frac{1}{\tau_1}\,\frac{z}{z - e^{-nT/\tau_1}} \qquad 7\text{-}48$$

---

### 7.3.4 Step Invariance Design

Rather than matching the filter's impulse response, we can match the step response. The concept is similar to the impulse invariance design. The digital filter is computed as [3]

$$F(z) = \frac{z-1}{z} Z\left( L^{-1}\left[ \frac{F(s)}{s} \right] \right) \qquad 7\text{-}49$$

## *Example 7.4*

Compute the digital loop filter using the step invariance design of $F(s) = \dfrac{\tau_2 s + 1}{\tau_1 s}$.

First we compute the intermediate argument,

$$L^{-1}\left[ \frac{F(s)}{s} \right] = L^{-1}\left[ \frac{1}{s} \frac{\tau_2 s + 1}{\tau_1 s} \right] = \frac{t + \tau_2}{\tau_1} \qquad 7\text{-}50$$

The Z-Transform of Equation 7-50 is computed as

$$Z\left( \frac{t + \tau_2}{\tau_1} \right) = \frac{z\left(T + \tau_2 (z-1)\right)}{\tau_1 (z-1)^2} \qquad 7\text{-}51$$

The digital filter design is completed with

$$F(z) = \frac{z-1}{z} \frac{z\left(T + \tau_2 (z-1)\right)}{\tau_1 (z-1)^2} = \frac{T + \tau_2 (z-1)}{\tau_1 (z-1)} \qquad 7\text{-}52$$

Suppose we let $\tau_1 = 0.01$, $\tau_2 = 0.002$, $T = 0.001$. The step response of the analog and digital filters is graphed in Figure 7.9.

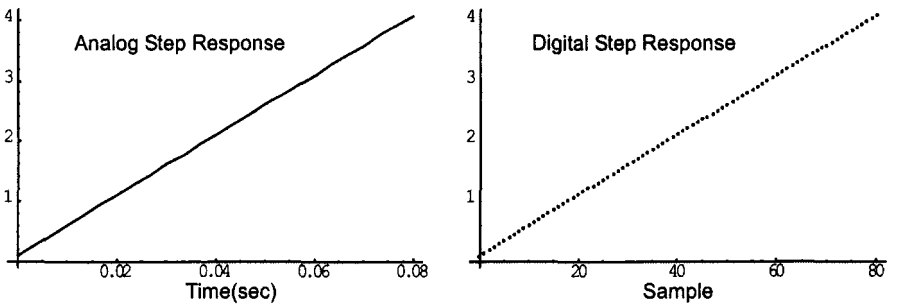


Figure 7.9 Step Responses of Step Invariance Design

## 7.4. VCOs

The VCO in the digital loop is more appropriately called an NCO (Numerically Controlled Oscillator) when it has discrete inputs and outputs. The fundamental element within the VCO in Figure 7.7 is the integrator.

Suppose that we are integrating phase with our NCO, such that every sample we are going to increment the phase accumulator by the value of error(t). A simple algorithm for this NCO could be represented by

$$\text{accumulator}(n) = \text{accumulator}(n-1) + T_S\,\text{error}(n) \qquad 7\text{-}53$$

$$v(n) = Cos[Mod\{\text{accumulator}(n)\}_{2\pi}] \qquad 7\text{-}54$$

Note the accumulator value is maintained separately from the transcendental Cos[.] function. Depending on the application, the Cos[.] function is generated from a lookup table, dedicated hardware, or a floating point CPU. Because we are using the Cos[ ] function, we want to limit our input to the range $\{0,2\pi\}$ or $\{-\pi,\pi\}$. To accomplish this, we use the Mod function which we define for the range space as

$$\text{If } (\text{accumulator}(n) \geq 2\pi)$$
$$\text{Then accumulator}(n) = \text{accumulator}(n) - 2\pi$$

An important consideration of the NCO equation is the gain of the NCO. The NCO in Equation 7-53 has a gain of $\frac{1\,\text{radian}}{T_S\ \text{seconds}}$. This implies that the sample frequency, $F_S = 1/T_S$, has a direct impact on the gain of the loop. (Designers often forget this scalar and are surprised when their PLL is unstable because they have excessive gain in the loop.)

Note $Cos[3\pi] = Cos[\pi]$, so the nonlinear Mod[.] function is really for implementation convenience, rather than disturbing the mathematical form of accumulator(n). Thus, we can take the Z-Transform of Equation 7-53 and ignore the nonlinear affects of Equation 7-54. Performing the transformation, and placing it in the form of a transfer function gives

$$H[z] = \frac{\text{Accumulator}[z]}{\text{Error}(z)} = \frac{T_S z}{z-1} \qquad 7\text{-}55$$

This integration method is termed Backward Euler by Jeruchim [2]. It is absolutely stable . If we use a previous value for error(n) in Equation 7-53, we have

$$\text{accumulator}(n) = \text{accumulator}(n-1) + T_S\,\text{error}(n-1) \qquad 7\text{-}56$$

$$H[z] = \frac{\text{Accumulator}[z]}{\text{Error}(z)} = \frac{T_S}{z-1} \qquad 7\text{-}57$$

The Forward Euler integrator represented by Equations 7-56 and 7-57 is not absolutely stable [2]. Intuitively this makes sense, because Equation 7-56 introduces a time delay in our function's response. From our study of analog loops, we know that time delays can change a stable transfer function into one that is unstable. Unfortunately, this is the most common form of the integrator because of the required processing delay to produce error(n).

Note the first loop configuration in Figure 7.10. This is really not possible, because in order to generate $\theta_e(n)$, the loop must have already computed $\theta_o(n)$, which obviously depends on $\theta_e(n)$. In order to solve this dilemma, a delay is inserted in right-hand phase-locked loop. The error voltage, $\theta_e(n)$, can now be computed because the feedback is $\theta_o(n-1)$

which is not dependent upon $\theta_e(n)$. However, the inclusion of the delay with the integrator of Equation 7-55 is the same effect as using the Forward Euler integrator. The delay can be modeled as a $z^{-1}$ term for the loop filter, but the result is the same for the loop's forward gain.

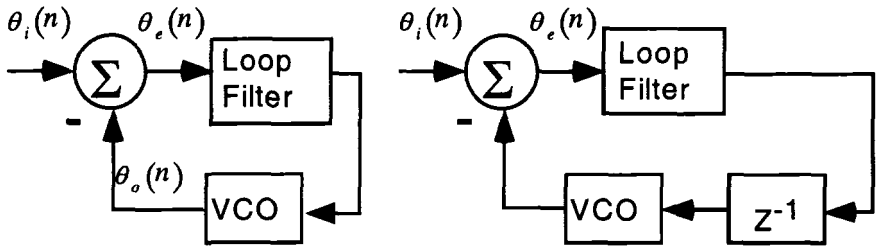


Figure 7.10 Processing Delays in a Digital Phase-Locked Loop

There are many different integrators available in the literature, and a common integrator is represented by

$$\text{accumulator(n)} = \text{accumulator(n - 1)} + \frac{T_S}{2}\{\text{error(n)} + \text{error(n - 1)}\} \qquad 7\text{-}58$$

$$H[z] = \frac{\text{Accumulator[z]}}{\text{Error(z)}} = \frac{T_S}{2}\frac{z+1}{z-1} \qquad 7\text{-}59$$

Note the similarity to our bilinear transformation development of Equation 7-11. As might be expected, this is called a trapezoidal integrator because it performs a trapezoidal approximation to the function's integral. Like the Backward Euler, it is absolutely stable [2].

Modulator/Demodulators (Modems) often require the generation of complex sinusoids where $s(n) = Cos[2\pi f_c nT] + j\,Sin[2\pi f_c nT]$. The basic idea is to compute the coordinates of samples on the unit circle as shown in Figure 7.11. The value of z on the unit circle represents the complex value of $e^{j\frac{2\pi}{N}}$. Most implementations utilize a combination of arithmetic and table lookup instead of recursion. A combination of table look-up and interpolation can significantly reduce the size of the required table [7].

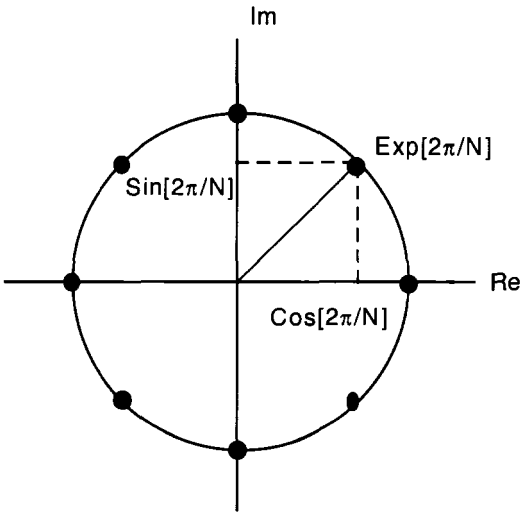


Figure 7.11 Generation of Complex Sinusoids [7]

## 7.5. Complete Digital PLL Equations

Although it is primarily useful only for analysis and not design, a complete digital phase-locked loop equation can be generated. Equation 7-60 is the closed loop transfer function for a second-order loop with a bilinear transformation of the active second order filter. The NCO has an implicit delay, corresponding to Equation 7-57.

$$H_C(z)=\frac{16B_L^{\,2}\zeta^2\left(2(z+1)+f_s(z-1)\sqrt{\frac{\left(1+4\zeta^2\right)^2}{B_L^{\,2}}}\right)}{\left(\begin{array}{l}32B_L^{\,2}(z+1)\zeta^2+f_s^{\,2}(z-1)^2\left(1+4\zeta^2\right)^2\\+16B_L^{\,2}f_s(z-1)\zeta^2\sqrt{\frac{\left(1+4\zeta^2\right)^2}{B_L^{\,2}}}\end{array}\right)} \qquad 7\text{-}60$$

A similar equation can be computed for the first order phase-locked loop. Similar to Equation 7-60, this equation represents the transformation of a prototype analog loop to the digital domain. The noise bandwidth, $B_L$, is the prototype's analog noise bandwidth, and not the resulting digital noise bandwidth. The latter must be computed with the residue technique.

$$H_C(z) = \frac{4B_L T_s}{z - 1 + 4B_L T_s} \qquad 7\text{-}61$$

A common error in developing the transformations of the analog loops (such as Equation 7-60 or 7-61) is to improperly equate the NCO's implicit gain of $T_s$ as the $K_o$ gain which is used in the analog bandwidth equations. However, $T_s$ is not in the analog prototype, so as an example for the first order loop, $B_L = \frac{4}{\sqrt{2P}\, K_0\, K_d\, K_F}$, and not $B_L = \frac{4}{\sqrt{2P}\, T_s\, K_d\, K_F}$

## *Example 7.5*

Recall the analog phase-locked loop of Example 2-1 and the digital transformation of Example 7-2. The loop specifications are: Natural Frequency (Specified) 3 Hz, Damping Factor (Specified) 0.707 Sampling Frequency (Specified) 50 Hz. Design the digital loop using the block elements discussed above. Provide a block diagram of the resulting loop. Plot the error response of the digital loop to an input step in phase.

### 7.5.1 Filter

The design technique will be to assume that the phase detector and NCO have unity gains. We begin with Equation 2-73, which gives us the parameters for the loop filter.

$$\tau_1 = \frac{\sqrt{2P}K_o K_d}{w_n^2} \qquad 7\text{-}62$$

Substituting in the design parameters of the loop into Equation 7-62, allows us to find the analog filter parameter, $\tau_1$.

$$\tau_1 = \frac{\sqrt{2\ \times 1 \times 10^{-3} \times 50}}{1}\left(\frac{1\ \text{rad}}{V \times \text{sec}}\right)\left(\frac{1V}{\text{rad}}\right)\left(\frac{\text{sec}^2}{(3 \times 2\pi)^2}\right) = 890 \times 10^{-6} \qquad 7\text{-}63$$

After finding the filter parameter $\tau_1$, the filter's other parameter, $\tau_2$ must be determined. Using the definition of the damping factor, $\zeta$, in Equation 2-74, $\tau_2$ is obtained through

$$\tau_2 = \sqrt{\frac{\zeta^2 4\tau_1}{\sqrt{2P}K_o K_d}} = 0.075015 \qquad 7\text{-}64$$

These two filter parameters, along with the constant C, define the second order filter in Equation 7-42. For this example, we choose the true bilinear transformation with $C = 2/T_S$ instead of pre-warping the breakpoint frequency. From the problem definition, the sample time, $T_S = 1/50\,\text{sec}$. Substituting all the parameters into Equation 7-44 provides

$$F_{bilinear}(z) = \frac{95.52 - 73.05z^{-1}}{z^{-1} - 1} \qquad 7\text{-}65$$

Note we express Equation 7-65 as a function of $z^{-1}$. This permits us to write the difference equation by inspection.

$$y(n) = y(n-1) + 95.52x(n) - 73.05x(n-1) \qquad 7\text{-}66$$

The equivalent block diagram for the filter is shown in Figure 7.12. This filter's topology is called a Direct 1 Form [3]. It has two different delay elements which may or may not be cost effective for a particular implementation. An advantage of this configuration is the previous value of y(n-l), which represents the integrator's previous value is readily available. Specialized techniques such as limiting or truncation can easily be performed on the integrator's contents. These might be performed to limit a phase-locked loop's acquisition range, to keep the modem or receiver from attempting to acquire a signal out-of-band.

An alternative realization of the filter is obtained by writing [3]

$$F_{bilinear}(z) = \frac{N(z)}{D(z)} \qquad 7\text{-}67$$

Where $N(z)$ and $D(z)$ are the numerator and denominator of the transfer function, respectively. We define an intermediate transfer function, $W(z)$ as

$$W(z) = \frac{X(z)}{D(z)} \qquad 7\text{-}68$$

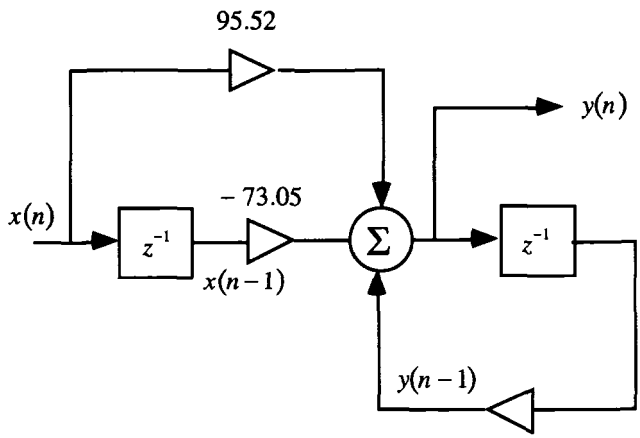


Figure 7.12 Direct 1 Form Realization of Loop Filter

$X(z)$ is the input to the filter and $D(z)$ is the denominator of the filter's transfer function previously defined in Equation 7-67. The filter's output is written using the intermediate transfer function as

$$Y(z) = N(z)W(z) \qquad 7\text{-}69$$

Specifically, for the phase-locked loop filter's transfer function,

$$W(z) = \frac{X(z)}{z^{-1} - 1} \qquad 7\text{-}70$$

$$w(n) = w(n-1) + x(n) \qquad 7\text{-}71$$

The output of the filter can be written as

$$Y(z) = \left(95.52 - 73.05z^{-1}\right)W(z) \qquad 7\text{-}72$$

The time domain representation is

$$y(n) = 95.52w(n) - 73.05w(n-1) \qquad 7\text{-}73$$

Using Equations 7-73 and 7-71, we construct the Direct Form 2 representation of the filter which is shown in Figure 7.13. Note the simpler architecture and the single time delay. The disadvantage of this configuration is that the accumulator value, $w(n-1)$, does not directly represent the previous output. In some applications this may be inappropriate, and a Direct Form 1 realization is superior for that application.

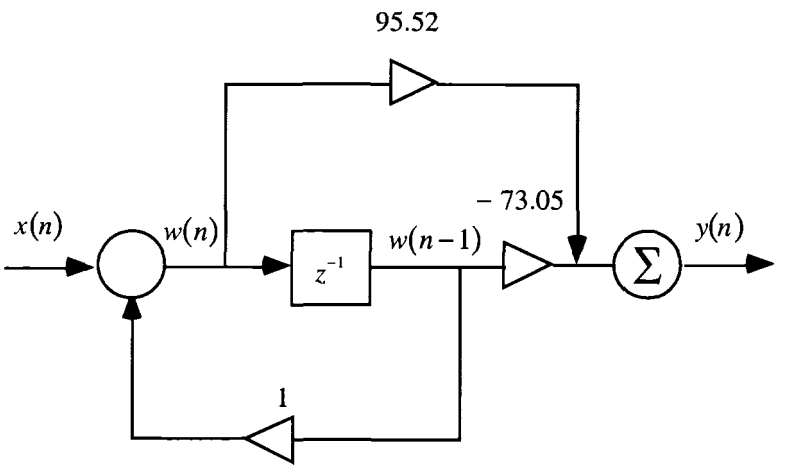


Figure 7.13 Direct Form 2 Realization of Loop Filter

## 7.5.2. NCO

The NCO will be represented by $NCO(z) = \dfrac{T_S z^{-1}}{1 - z^{-1}}$. As was discussed previously, an NCO has an implicit gain of the update rate, or $\dfrac{1}{F_S}$. Recall the loop filter was designed with the assumption that the gains of the NCO and phase detector were unity. To compensate, we multiply the input of the NCO with the inverse of this implicit gain. Figure 7.14 shows the block diagram of the NCO. Note this is a linearized representation that permits

linear analysis of the loop. The actual implementation (with the appropriate gain correction) would use Equations 7-53 and 7-54.

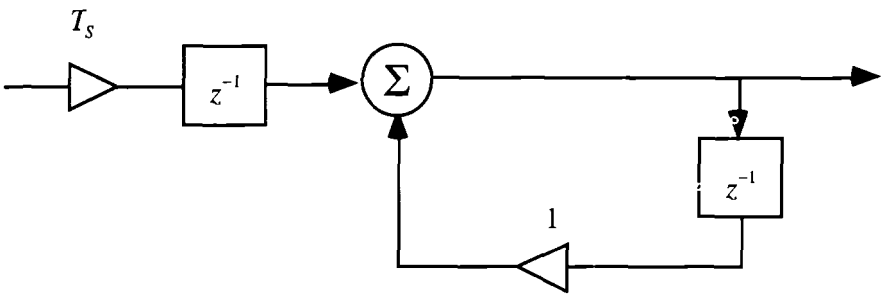


Figure 7.14 Linearized Representation of the NCO

Because we have a finite processing time to compute the NCO's output, we need to model the input delay of the backward Euler integrator. (We cannot compute y(n) when it is dependent upon e(n)=y(n)*x(n).) From Equation 7-57, the NCO transfer function is

$$NCO(z) = \frac{T_S z^{-1}}{1 - z^{-1}} \qquad 7\text{-}74$$

### 7.5.3. Phase Detector

The purpose of our block diagram is to obtain an overall transfer function that permits analysis. The actual implementation of the phase detector is a multiplier, mixing the input and the output of the NCO together. (We caution the reader to account for the gain of the phase detector when deriving the loop filter coefficients.) For the linearized representation, however, the phase detector will be a simple adder with unity gain.

### 7.5.4. Complete Loop Representations

The complete transfer function for the phase-locked loop may be obtained from the block elements previously defined. The forward gain of the loop is

$$\text{ForwardGain}(z) = \sqrt{2P}\, F_{bilinear}(z)\text{NCO}(z) = \frac{-0.4620 + 0.6041z}{1 - 2z + z^2} \qquad 7\text{-}75$$

Recall the closed loop gain of our system is $\text{ClosedLoop}(z) = \frac{\text{ForwardGain}(z)}{1 + \text{ForwardGain}(z)}$. Substituting in Equation 7-75, and manipulating the algebra yields

$$H_C(z) = \frac{-0.462 + 0.604z}{0.538 - 1.396z + z^2} \qquad 7\text{-}76$$

The complete block diagram of our loop is shown in Figure 7.15. We have selected the direct form 1 representation of the loop filter. As noted previously, this allows better monitoring and control of the loop. Again, we want to stress the NCO and phase detector have been linearized. To actually implement the loop, the nonlinear numeric functions would be replace those shown in Figure 7.15.

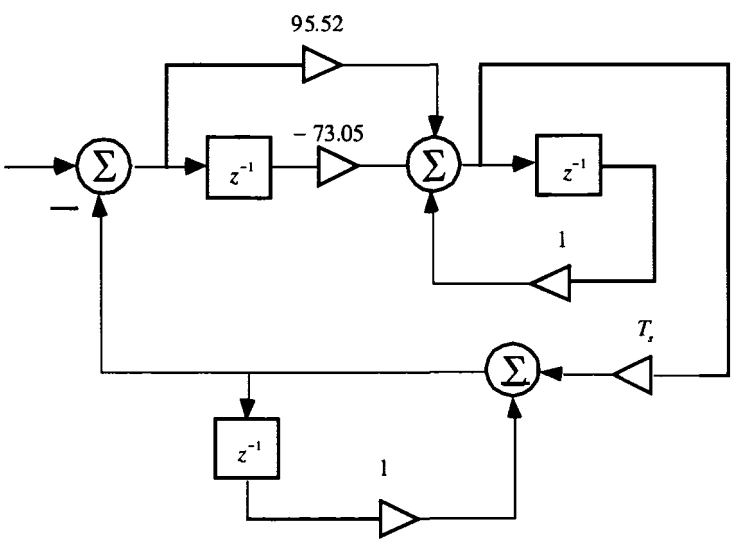


Figure 7.15 Complete Block Diagram of Digital Loop

### 7.5.5. Response to Phase Step Input

A good metric for time domain performance is the response of the loop to a phase step. To determine the step response, we must first derive the error response function, $H_e(z) = 1 - H_C(z)$. Substituting in Equation 7-76, we obtain

$$H_e(z) = \frac{1 - 2z + z^2}{0.538 - 1.396z + z^2} \qquad 7\text{-}77$$

To compare the step response of this block-constructed loop with the previous transformation design in Example 7-2, we compute the error response to a step input. We compute $Y(z) = \frac{z}{z-1} H_e(z)$

$$Y(z) = \frac{z(z-1)}{0.538 - 1.396z + z^2} \qquad 7\text{-}78$$

The inverse Z-transform of Equation 7-78 gives the time domain response to the phase step input.

$$y(n) = \left( \begin{array}{l} (0.5 - j0.670)(0.698 - j0.226)^n + \\ (0.5 + j0.670)(0.698 - j0.226)^n \end{array} \right) u(n) \qquad 7\text{-}79$$

The time domain response is plotted in Figure 7.16. As a reference, the analog loop we designed earlier in Example 2.1 is shown as a continuous line. The response of the digital phase-locked loop is shown as discrete "lollipops" corresponding to the sample values. Note how well the digital loop matches the analog design. Comparing Figures 7.16 and 7.5 (bilinear transformation of the second order loop) shows a difference between the two implementations. This is primarily due to the delay produced by the backward Euler integrator.

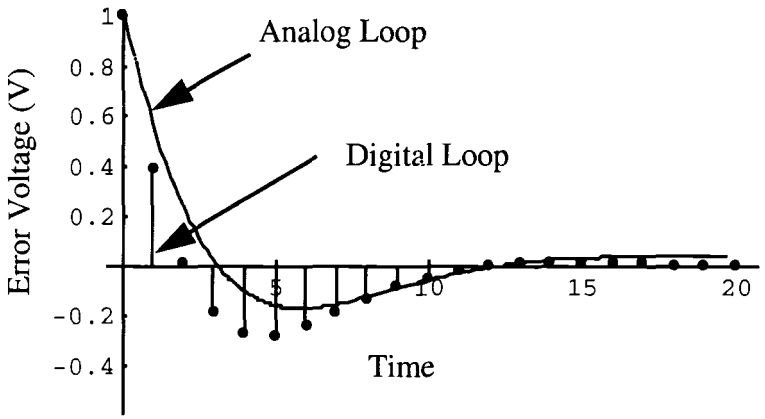


Figure 7.16 Comparison of Analog Loop With Digital Block Element Loop

## 7.6. References

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[2] Jeruchin, M.C., Balaban, P., Shanmugan, K.S., *Simulation of Communication Systems*, Plenum Press, NY, NY, 1992.

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[6] Vaidyanathan, P.P., *Multirate Systems and Filter Banks*, Englewood Cliffs, NJ, Prentice Hall, 1993.

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## 7.7. Problems

7.1 Compute the backward difference form of a first-order Butterworth filter, $F(s) = \dfrac{\alpha}{s+\alpha}$. Draw a block diagram of the filter, using multipliers, adders, and delays. Graph the magnitude response for the digital filter with $\alpha = 0.1, T_s = 0.001\text{sec}$. What is the region of stability for the filter?

7.2 Compute the backward difference form of a second-order filter, $F(s) = \dfrac{1}{s^2 + \sqrt{2}\,s + 1}$ Draw a block diagram of the filter. Graph the magnitude response for the digital filter with $T_s = 0.1\ \text{sec}$. What is the region of stability for the filter?

7.3 Compute the bilinear transformation of a first-order Butterworth filter, $F(s) = \dfrac{\alpha}{s+\alpha}$. Draw a block diagram of the filter, using multipliers, adders, and delays. Graph the magnitude response for the digital filter with $\alpha = 0.1, T_s = 1/60\ \text{sec}$. What is the region of stability for the filter?

7.4 Compute the bilinear transformation of a second-order Butterworth filter, $F(s) = \dfrac{1}{s^2 + \sqrt{2}\,s + 1}$. Draw a block diagram of the filter, using multipliers, adders, and delays. Graph the magnitude response for the digital filter with $T_s = 1/33\ \text{sec}$. What is the region of stability for the filter?

7.5 FIR filters are used frequently in digital signal processing. They offer linear phase which is highly desirable in processing communication signals. Let the loop filter for the phase-locked loop of Figure 7.15 be $F(z) = 0.0298955 + \dfrac{0.257246}{z} + \dfrac{0.257246}{z^2}$ Compute the transfer function for the phase-locked loop. Compute

the step impulse response for the phase-locked loop. Compute the response to a ramp in phase. $T_s = 0.01$, $K_o = 200$.

7.6 FIR filters are used frequently in digital signal processing. Let the loop filter for the phase-locked loop of Figure 7.17 be

$$F(z) = 0.00137575 + \frac{0.0421946}{z} + \frac{0.170413}{z^2} + \frac{0.170413}{z^3} + \frac{0.0421946}{z^2}$$

Compute the transfer function for the phase-locked loop. Compute the step impulse response for the phase-locked loop. Compute the response to a ramp in phase. $T_s = 0.01$, $K_o = 50$.

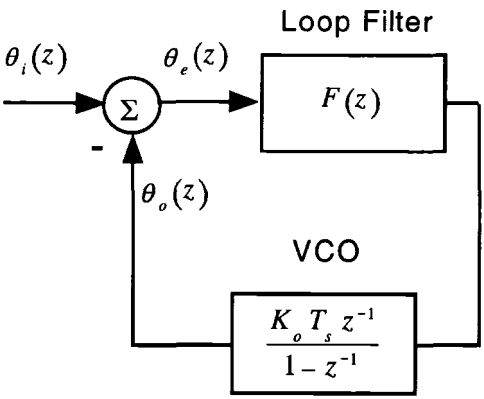


Figure 7.17 Simple Digital Phase-Locked Loop

7.7 Suppose the sampling rate for an NCO is 100 Hz. We want to produce 10 Hz with an accuracy of 1.0 Hz. How many table coefficients are required for the NCO? Produce an output sequence using the table and perform an FFT of the output.

7.8 Suppose the sampling rate for an NCO is 60 Hz. We want to produce 5 Hz with an accuracy of 0.5 Hz. How many table coefficients are required for the NCO? Produce an output sequence using the table and perform an FFT of the output.

# 8

# Stability and Frequency Response of Digital Loops

In this chapter, we want to develop stability and frequency analysis tools for digital phase-locked loops similar to those developed for analog loops in Chapter 3. As with the analog loops, we will show the root locus is invaluable in determining stability.

## 8.1. Stability

In Figure 8.1, we have a system function labeled a phase-locked loop, although for the purposes of this discussion it could be any digital system with the system impulse function, h(n).

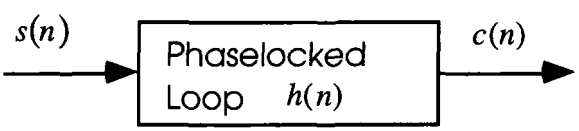


Figure 8.1 Digital System for Stability Analysis

The output, c(n), for Figure 8.1 is obtained by the convolution theorem,

$$c(n) = \sum_{k=-\infty}^{\infty} s(k)h(n-k) \qquad 8\text{-}1$$

For Bounded Input-Bounded Output (BIBO) stability, the system of Figure 8.1 must have a bounded impulse function [1]

$$\sum_{k=-\infty}^{\infty} |h(k)| < \infty \qquad 8\text{-}2$$

This is similar to the requirement for continuous systems, $\int_0^{\infty} |h(t)| dt < \infty$ [8] . If the condition of Equation 8-2 is true, then the output, c(n), of Figure 8.1 is bounded. As an example, suppose we have a closed loop transfer function of the form,

$$H(z) = \frac{z}{az^2 + bz + c} \qquad 8\text{-}3$$

A partial fraction expansion of Equation 8-3 yields

$$H(z) = \frac{c_1 z}{z - r_1} + \frac{c_2 z}{z - r_2} \qquad 8\text{-}4$$

Hint: When performing a partial fraction expansion of an equation similar to Equation 8-3, it is best to divide out a "z" first, and then perform the partial fraction expansion on the quotient. After obtaining the partial fraction, then multiply it by z to obtain a form with a z in the numerators as in Equation 8-4. This places the intermediate results of the transformation into the form most often found in Z-Transform tables.

Using Z-Transform table, Appendix B, (or direct derivation) for Equation 8-4, we obtain

$$h(n) = c_1 r_1^n + c_2 r_2^n, n > 0 \qquad 8\text{-}5$$

Equation 8-5 is bounded if $|r_1|, |r_2| < 1$. This suggests that we can determine the stability of a system by examining the position of all the poles in the closed loop transfer function. If all the poles are contained within the unit circle as shown in Figure 8.2, then the system is stable. (This corresponds to the terms $r_i^n \to 0$ as $n \to \infty$.)

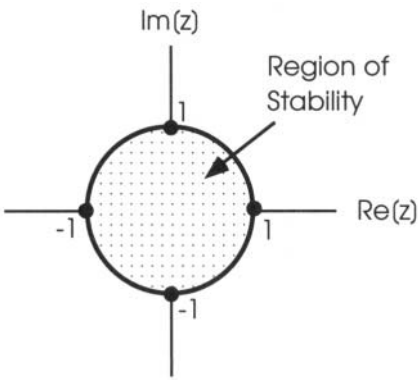


Figure 8.2 Region of Stability for System Poles

### 8.1.1. Root Locus

Similar to the continuous systems of Chapter 3, the root locus plot can be used for evaluating the stability and sensitivity of the digital phase-locked loop. The concept is the same. We compose our open loop transfer function, $H_o(z)$, and multiply by a gain constant, K. Then we find the roots of the characteristic equation (also the denominator of the closed loop transfer function) and plot them as a function of gain. The next example will illustrate the technique.

---

## *Example 8.1 Computation of Root Locus*

In Example 7.3, we computed the forward gain of a second order, active filter digital phase-locked loop as

$$\text{ForwardGain}(z) = \sqrt{2P}\, F_{bilinear}(z)\text{NCO}(z)$$
$$= \frac{-0.4620 + 0.6041z}{1 - 2z + z^2} \qquad 8\text{-}6$$

Compute the root locus of this phase-locked loop.

We rewrite the gain as

$$\text{ForwardGain}(z) = K\frac{-0.4620+0.6041z}{1-2z+z^2} \qquad 8\text{-}7$$

The characteristic equation has the form, $1+\text{ForwardGain}(z)$. Recalling that $H_c(z)=\dfrac{\text{ForwardGain}(z)}{1+\text{ForwardGain}(z)}$, we note that the characteristic equation is simply the denominator of the closed loop transfer function. Although we could compute the characteristic equation by inspection, we proceed to calculate the closed loop transfer function substituting into

$$\text{rootLocus}(z)=\frac{\text{ForwardGain}(z)}{1+\text{ForwardGain}(z)}$$

$$rootLocus(K)=\frac{K(-0.4620+0.6041z)}{K(-0.4620+0.6041z)+1-2z+z^2} \qquad 8\text{-}8$$

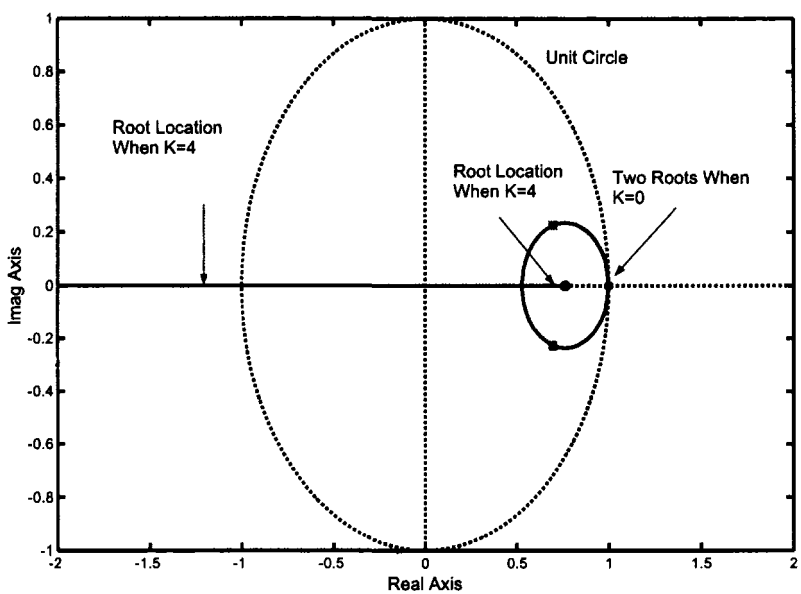


Figure 8.3 Root Locus of Example 8.1

To compute the root locus, we compute the roots of the denominator $(1 + \text{ForwardGain}(z) = 0)$, and plot them as a function of the gain term, K.

As discussed in Chapter 3, the roots of the closed loop function at **K=0** are the poles of the open loop transfer function. At $K = \infty$, the roots of the closed loop function are the zeros of the open loop transfer function. This is shown in the root locus plot of Figure 8.3.

At **K=0**, the two poles are the same as the poles of the open loop function, Equation 8-7. (A double pole at **z=1**.) At **K=4**, one pole is moving toward the only open loop zero of **z=0.76**. The other pole is moving toward the $-\infty$ real axis. Recall that poles on the negative real axis create oscillatory responses, even if they are inside the unit circle. Inside the unit circle, the negative root is exponentially weighted by the time index n, and it will be exponentially damped. However, the initial oscillation may be objectionable in some applications.

---

As Kuo [2] notes, the best method of determining stability of a digital loop is to directly compute the roots of the characteristic equation if the coefficients are known. Recall for the analog loops, we found that the Bode plot provided stability information as well as an indication of the stability.

In constructing a Bode plot for an analog loop, we have several approximations that permit the rapid construction of a Bode plot. Most of these approximations are based upon the log-frequency relationships of the analog transfer functions. Unfortunately, these approximations are not directly applicable to sampled data systems. The first problem is the sampled data systems have an inherent wrap around the Nyquist sampling frequency. The second complication is the frequency warping because the Z-Transform is mapping the entire $j\omega$ analog frequency axis into the unit circle.

There is a w-transformation [3] that allows the simple analog techniques to construct the Bode Plot for sampled data systems. However, with the availability of computer-aided analysis, the utility of such a transformation is questionable. Instead, the simple gain-phase plot of the open loop transfer function can provide relative and absolute stability measures. While this plot does not permit the easy construction of the Bode Plot, it provides the traditional gain and phase margins of control system analysis.

As with the s-domain plots, the gain margin is measured at the -180° phase crossing and the phase margin is measured at the unity gain frequency.

The reader is cautioned that this method requires special consideration when the forward gain function has poles outside the unit circle. In such cases, consult Kuo [2] for utilization of the Nyquist criteria with the gain-phase plot. Since the method is similar to the analog technique, we will demonstrate with an example.

## *Example 8.2 Gain-Phase Plot Example*

Using the gain-phase plot method, compute the gain and phase margins of the digital phase-locked loop of Example 7.3.

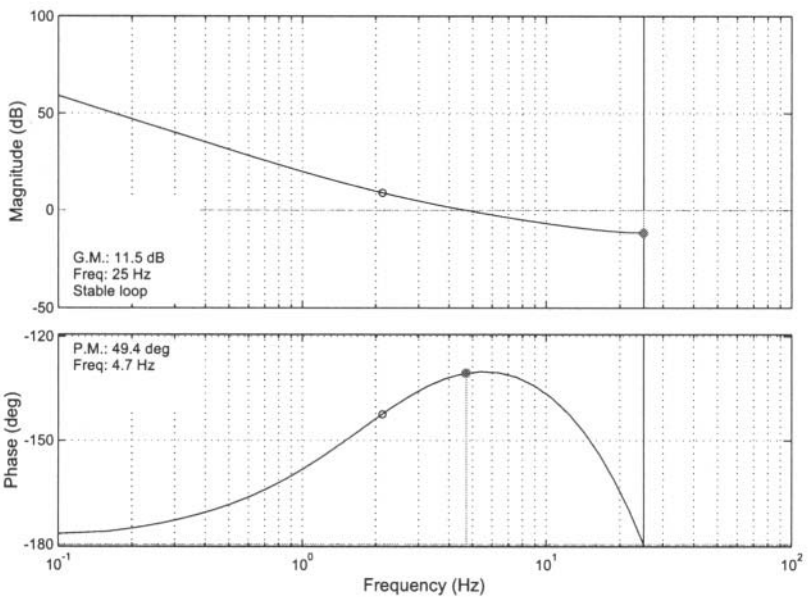


Figure 8.4 Gain-Phase Plot of Example 8.2

The forward gain of the loop is $\text{ForwardGain}(z) = \dfrac{-0.4620 + 0.6041z}{(z-1)^2}$.
This forward loop does not have a pole outside the unit circle, so the computation is straight-forward. We make the substitution $z = e^{j2\pi f T_s}$ into the forward gain equation and graph the amplitude and phase. The unity gain crossover is approximately 4.7 Hz and the phase at f=4.7 Hz is 130.6°. The phase margin is computed as 180°-130.6°=49°

---

The interpretation of a Gain-Phase plot becomes more difficult if there is a pole outside the unit circle in the forward gain transfer function. (Recall we can have a stable loop if the forward gain function has a pole outside the unit circle, but if the closed loop function has a pole outside the unit circle, then it is unstable.)

## 8.2. Noise Bandwidth of Digital Phase-Locked Loops

In Chapter 4, we presented the phase variance of an analog phase-locked loop with Equation 4-28. A fundamental parameter for Equation 4-28 is the noise bandwidth (recall the signal to noise ratio, $\rho = \dfrac{S}{N_0 B_L}$). In order to predict the performance of digital phase-locked loops, we need equivalent equations for the noise bandwidth and output noise power.

To not introduce further confusion, we carefully define the noise and corresponding bandwidths. Figure 8.5 shows a phase-locked loop with a bandpass filter preceding the input. A sinusoidal input is assumed which corresponds to the power spectral frequency terms, $\dfrac{P}{2}\delta(f + f_0)$ and $\dfrac{P}{2}\delta(f - f_0)$ shown in Figure 8.5. The bandpass filter has a bandwidth defined as $B_i$. This input bandwidth, $B_i$, is graphically defined and we specifically avoid calling it single or double-sided to avoid additional confusion in the literature.

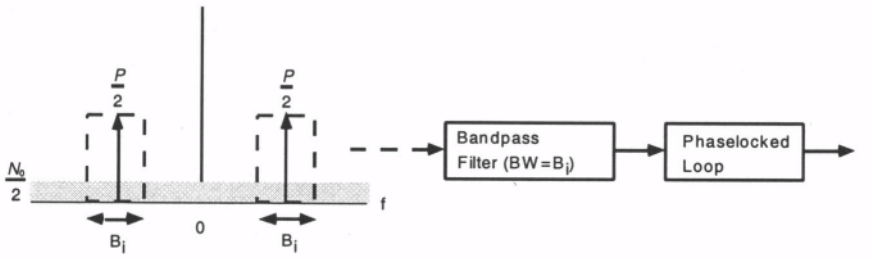


Figure 8.5 Bandpass Noise Into a Digital Phase-Locked Loop

As we know from our study of the analog phase-locked loops, white noise is represented with a constant power spectral density of $S_{nn}(f) = \frac{N_0}{2}, -\infty < f < \infty$. With infinite bandwidth, it is impossible to define a sampling frequency, $f_s$, sufficient to meet the Nyquist sampling requirements. Because of this, we consider bandwidth limited noise, which corresponds to any real system. (Parasitic capacitances, nonlinear effects, etc, all impose a finite bandwidth limit on a real system.) The total noise power into the phase-locked loop is $B_i N_0$, with the total signal power of P. The input signal-to-noise ratio into the loop is then

$$\rho = \frac{P}{B_i N_0} \qquad 8\text{-}9$$

The phase-locked loop itself has a loop filter which will further reduce the noise, assuming the sampling frequency is above the Nyquist frequency. This also explains why digital phase-locked loop signal-to-noise ratios are dependent upon the input filter's bandwidth.

When the continuous bandlimited noise process n(t), is sampled, discrete noise samples n(k) are obtained. The covariance and autocorrelation of the noise samples are identical because we assume a zero mean. The covariance is written as the statistical expectation

$$r_{nn}(m) = E[n(k)n(k+m)] \qquad 8\text{-}10$$

Because the white noise has zero mean, the Z-Transform of Equation 8-10 exists, and is defined as power spectrum of the sampled white noise sequence, n(k).

$$S_{n_s n_s}(z) = Z\{r_{nn}(m)\} \qquad 8\text{-}11$$

The total power in the white noise process, $S_{n_s n_s}(z)$, is obtained from the relationship, [1]

$$\sigma_n^2 = \frac{1}{j2\pi}\oint S_{n_s n_s}[z] z^{-1} dz \qquad 8\text{-}12$$

We can write Equation 8-12 in an equivalent form for the contour $|z| = 1$, substituting $z = e^{jw}$

$$\sigma_n^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} S_{n_s n_s}\left[e^{jw}\right]\, dw \qquad 8\text{-}13$$

In this text, the phase-locked loops have been defined with a closed loop transfer function $H_c(z)$. Recall that the output power spectrum of a linear time-invariant system is $S_Y(z) = S_{n_s n_s}[z]|H_c(z)|^2$. We can substitute this relationship into Equation 8-13 to obtain the output noise power of the phase-locked loop as

$$\sigma_\theta^2 = \frac{1}{j2\pi}\oint H_C[z] H_C[z^{-1}] S_{n_s n_s}[z] z^{-1} dz \qquad 8\text{-}14$$

Figure 8.6 shows a noise model of the digital phase-locked loop. In our closed representation, we include the scalar $\sqrt{2P}$, which represents the input signal level. This is useful for remembering the input signal level directly affects the loop performance, but the sampled white Gaussian noise samples do not have this factor of $\sqrt{2P}$. We could re-derive our closed loop equations without the gain factor, or alternatively, we can consider that the power spectrum of the noise applied to the loop is

$$S_{ll}[z] = \frac{S_{n_s n_s}[z]}{2P} \qquad 8\text{-}15$$

where $S_{ll}[z]$ is the effective input noise spectrum to the loop, and $S_{n_s n_s}[z]$ is the actual noise spectrum.

This allows us to write the noise variance out of the NCO as [5]

$$\sigma_\theta^{\,2} = \frac{1}{j2\pi}\oint H_C[z]H_C[z^{-1}]\frac{S_{n_s n_s}[z]}{2P}z^{-1}dz \qquad 8\text{-}16$$

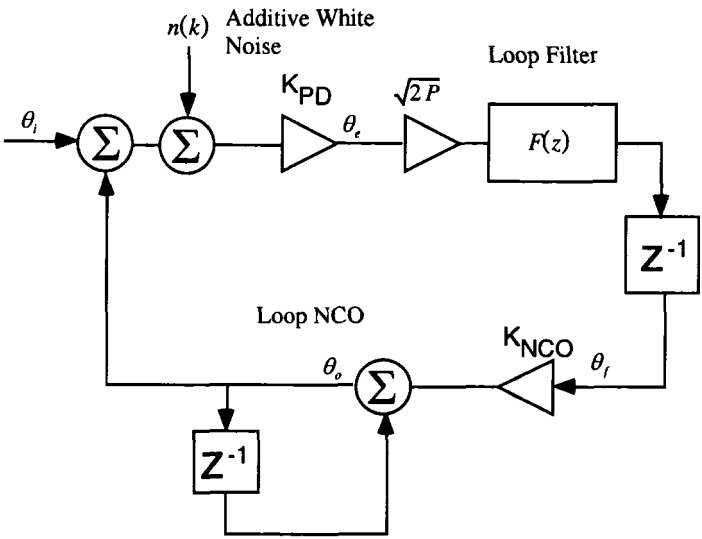


Figure 8.6 Noise Model of a Digital Phase-locked Loop.

Again, we can evaluate along the contour $|z| = 1$ and substitute $z = e^{jw}$ to obtain the equivalent form,

$$\sigma_\theta^{\,2} = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_C[e^{jw}]H_C[e^{-jw}]\frac{S_{n_s n_s}[e^{jw}]}{2P}dw \qquad 8\text{-}17$$

Actually, Equation 8-17 is more physically accurate from a perspective of spectral power density. $S_{n_s n_s}[z]$ is the Z-Transform of the covariance, $S_{n_s n_s}(z) = Z\{r_{nn}(m)\}$, whereas $S_{n_s n_s}[e^{jw}] \equiv S_{n_s n_s}[w]$ is power spectral density. We make the definition that the total noise power out of the loop,

$$\sigma_\theta^2 = B_L \frac{N_0}{P} \qquad 8\text{-}18$$

Equation 8-18 defines $B_L$ as a single-sided loop bandwidth, and makes it equivalent to the definition of noise power for the analog loop, Equation 3-64.

Lindsey and Chie [5] define the one-sided loop bandwidth $B_L$, of the loop to be

$$\frac{2B_L}{B_i} = \frac{1}{j2\pi}\oint H_C[z]H_C[z^{-1}]z^{-1}\,dz \qquad 8\text{-}19$$

Equation 8-19 is only a ratio, it does not provide an absolute noise bandwidth, $B_L$. In Equation 8-19, the variable $B_i$ represents the bandwidth of the IF filter in front of the digital phase-locked loop. (See Figure 8.5) The scalar, 2, as a multiplier for $B_L$, in Equation 8-19 may be confusing at first, but note the contour integral is the equivalent of integrating over both positive and negative frequencies. Because $B_L$ is single-sided, we need the factor of 2 in Equation 8-19.

Brute-force computation of Equation 8-19 is tedious, so typically we utilize residues or table lookups. However, caution needs to be exercised in the computation, because only poles within the region of stability should be considered. The contour of integration in Equation 8-25 is important [1], because the integration must be performed in the stable region. Direct substitution of the integrand into tables does not account for this consideration, and incorrect values can be obtained without considering the region of stability. We will demonstrate this in Example 8.6.

Beginning with Equation 8-19, we can make substitutions to obtain the output noise variance of the digital phase-locked loop.

$$\sigma_\theta^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_C\left[e^{jw}\right]H_C\left[e^{-jw}\right]\frac{S_{n_s n_s}\left[e^{jw}\right]}{2P}dw$$

$$= \frac{S_{n_s n_s}}{2P}\frac{1}{2\pi}\int_{-\pi}^{\pi} H_C\left[e^{jw}\right]H_C\left[e^{-jw}\right]dw \qquad 8\text{-}20$$

$$= \frac{S_{n_s n_s}}{2P}\frac{2B_L}{B}$$

$$= \frac{N_0 B}{2P}\frac{2B_L}{B} = \frac{N_0 B_L}{P}$$

## *Example 8.3 Computation of Noise Bandwidth*

Given a second order phase-locked loop with $H_c[z] = \dfrac{-2.607 + 2.726z}{30z^2 - 57.3z + 27.4}$, compute the noise bandwidth. An analog 1.0 Hz filter design was converted with a bilinear transform and a sampling rate of 30 Hz.

Substituting the given $H_C[z]$ into Equation 8-25 we compute the loop bandwidth integral as

$$\frac{2B_L}{B_i} = \frac{1}{j2\pi}\oint \frac{0.00865(1.0455 - z)(-0.9565 + z)}{(1.095 - 2.091z + z^2)(0.913 - 1.909z + z^2)}dz \qquad 8\text{-}21$$

As mentioned previously, direct substitution of the integrand into Z-Transform tables or improper use of residues can lead to an incorrect answer. Figure 8.7 shows the pole-zero plot of the integrand.

Note in Figure 8.7 that two poles are outside the unit circle. We want to choose a contour inside the region of stability and still include the other two poles. The unit circle is chosen in this case.

Representing the integrand of Equation 8-21 by $I(z)$, we express the integrand as products of the form

$I(z) = \frac{a_1 z + b_1}{z - p_1} \frac{a_2 z + b_2}{z - p_2} \frac{a_3 z + b_3}{z - p_3} \frac{a_4 z + b_4}{z - p_4}$. Most of the $a_i$ and $b_i$ terms will be zero, although we expressed it as the general form.

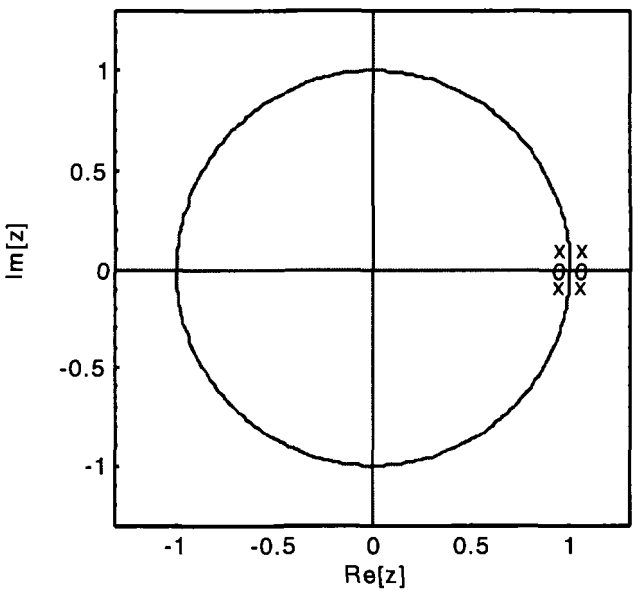


Figure 8.7 Pole-Zero Plot of Noise Bandwidth Integrand

To obtain the integrand as a product of rational fractions, it is easiest to write the functions $H_c[z]$ and $z^{-1}H_c[z^{-1}]$ as individual products.

We begin with the problem statement's $H_c[z]$ and find the roots of the denominator to write the fraction as

$$H_c[z] = \frac{0.0468(-1.856 + 1.94z)}{(-0.955 - j0.0434 + z)(-0.955 + j0.0434 + z)} \qquad 8\text{-}22$$

Each of the two poles can be separated easily in Equation 8-22, which allows us to compute the integral by residues quickly. We find the roots of the function $z^{-1} H_c[z^{-1}]$ and write it as

$$z^{-1} H_c[z^{-1}] = \frac{0.0513(1.94 - 1.856z)}{(-1.045 - j0.0476 + z)(-1.045 + j0.0476 + z)} \qquad 8\text{-}23$$

The complete integrand is then written as

$$I[z] = \frac{0.0468(-1.856 + 1.94z)}{(-0.955 - j0.0434 + z)(-0.955 + j0.0434 + z)} \times \frac{0.0513(1.94 - 1.856z)}{(-1.045 - j0.0476 + z)(-1.045 + j0.0476 + z)} \qquad 8\text{-}24$$

Equation 8-24 is consistent with the pole-zero diagram of Figure 8.7. By inspection, we see that the poles corresponding to $z^{-1} H_c[z^{-1}]$ are outside the unit circle. This indicates that we only need to compute the residues of I[z] for the poles of $H_c[z]$

$$\text{Residue } I[z]\big|_{z=0.955+j0.0434} = 0.0351 + j0.0124 \qquad 8\text{-}25$$

$$\text{Residue } I[z]\big|_{z=0.955-j0.0434} = 0.0351 - j0.0124 \qquad 8\text{-}26$$

The integral of Equation 8-21 is completed as

$$\frac{2B_L}{B_i} = \sum \text{Residues } I[z] \qquad 8\text{-}27$$

$$= 0.0351 - j0.0124 + 0.0351 + j0.0124 = 0.0703$$

Because Equation 8-27 is a ratio, it is interesting to obtain an absolute number which we can compare to analog loops. Suppose the input bandwidth is $\frac{f_s}{2}$, which just meets the Nyquist sampling frequency. To convert the fraction in Equation 8-27 to an absolute bandwidth, we multiply by the sampling frequency to obtain

$$B_L = \sum \text{Residues } I[z] \times \frac{f_s}{2} \qquad 8\text{-}28$$
$$= 1.05 \text{ Hz}$$

The loop bandwidth for the analog design was 1 Hz, so the digital design matches well at this sampling rate.

---

## 8.3. Sampling Rate Effect Upon Loop Bandwidth

From our study of the Z-Transform in Chapter 5, we would expect the loop performance to be effected by the sampling rate. Heuristically, as the sampling rate increases, the loop becomes much more like an analog loop. Figure 8.8 shows the normalized loop bandwidth of a second order phase-locked loop as a function of the normalized sampling rate. Jeruchin, et.al. suggests a sampling rate of 4 to 16 times the simulation bandwidth [6]. Figure 8.8 shows that for sampling rates less than 7 times the loop bandwidth, the resulting digital loop has excessive noise bandwidth.

To obtain Figure 8.8, we designed an analog phase-locked loop with a bandwidth of 3.5 Hz. We applied Equation 8-25 to all of the designs at the different sampling rates and graphed them after normalization.

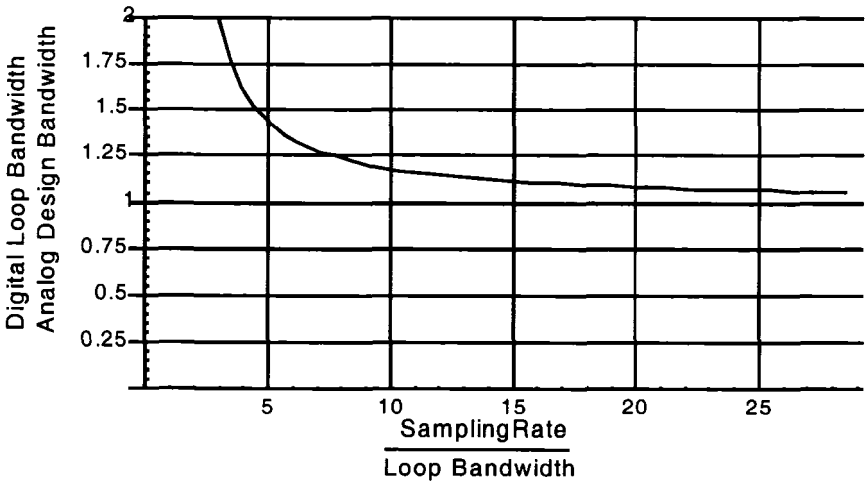


Figure 8.8 Sampling Rate Effect Upon Loop Bandwidth

## 8.4. References

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[7] Chie, C.M., Analysis of Digital Phase-Locked Loops, Ph.D. Dissertation, University of Southern California, January, 1977.

[8] Kuo, B.C., Automatic Control Systems, Englewood Cliffs, NJ, Prentice-Hall, Inc., 1982.

## 8.5. Problems

8.1 Compute the Root Locus plot for a first order phase-locked loop with a transfer function of $F(z) = \dfrac{0.265165}{z-1}$. Plot the Root Locus for 0<K<4.

8.2 Compute the Root Locus plot for a first order phase-locked loop with a transfer function of $F(z) = \dfrac{0.53033}{z-1}$. Plot the Root Locus for 0<K<4.

8.3 The open loop transfer function for the phase-locked loop is $H_C(z) = \dfrac{-0.305519 + 0.36108\,z}{(z-1)^2}$. Plot the root locus for 0.1<k<10.

8.4 Let the open loop transfer function for the phase-locked loop be $H_C(z) = \dfrac{-0.533458 + 0.551863\,z}{(z-1)^2}$

Plot the root locus for the root locus from gains of k=0.1 to k=4.

8.5 Consider the sampling frequency to be 160 Hz. Let the open loop transfer function for the phase-locked loop be $H_o(z) = \dfrac{-0.387137 + 0.662812\,z}{(z-1)^2}$. Compute the gain phase plot for 0<f<80 Hz. What are the gain and phase margins?

8.6 Let the open loop transfer function for the phase-locked loop be $H_o(z) = \dfrac{-0.472803 + 1.06074\,z}{(z-1)^2}$. Consider the sampling frequency to be 313 Hz. Compute the gain phase plot for 0<f<140 Hz. What are the gain and phase margins?

8.7 A digital loop was designed from an analog loop with a 100 Hz loop bandwidth. The sampling frequency is 1200 Hz. The closed loop transfer function is $H_C(z) = \dfrac{-0.209853 + 0.24547\,z}{0.790147 - 1.7645\,z + z^2}$. Compute the digital loop bandwidth using residues.

8.8 A digital loop was designed from an analog loop with a 33 Hz loop bandwidth. The sampling frequency is 126 Hz. The closed loop transfer function is $H_C(z) = \dfrac{-0.576385 + 0.8203\,z}{0.423615 - 1.1797\,z + z^2}$. Compute the digital loop bandwidth using residues.

8.9 Using Equation 7-53, compute the noise bandwidths of a 250 Hz phase-locked loop, $\zeta$=0.707 at sampling rates of 600 Hz, 800 Hz, and 2400 Hz.

8.10 Using Equation 7-53, compute the noise bandwidths of a 411 Hz phase- locked loop, $\zeta$=0.707 at sampling rates of 1000 Hz, 2000 Hz, and 4000 Hz.

# 9 All-Digital Phase-Locked Loops

In this chapter, we are going to extend our survey to loops that have do not have analog prototypes. Lindsey and Chie [1] performed a 1981 survey of digital PLLs that is recommended to the reader desiring additional architectures.

## 9.1. Non-Uniform Sampling

For all-digital phase-locked loops, there are alternatives to the sine and cosine based NCO as presented in Chapter 7. By utilizing sampling theory, it is possible to construct a phase-locked loop with a numerically controlled clock. Before discussing the architecture of a digital clock, we want to show the advantages of the concept. Figure 9.1 shows a phase-locked loop with a digital clock. Our derivation follows that of Chie in [2], which is similar to Weinberg and Liu [8]. (See also McCain, [3]).

In Figure 9.1, the sampler takes a sample of the bandpass signal at time $t_k$. The time interval between samples is expressed as

$$T_k = t_k - t_{k-1} \qquad 9\text{-}1$$

The digital clock has a nominal clock period, $T_*$, which is adjusted by the control input, $e_{k-1}$, according to the equation

$$T_k = T_* - e_{k-1} \qquad 9\text{-}2$$

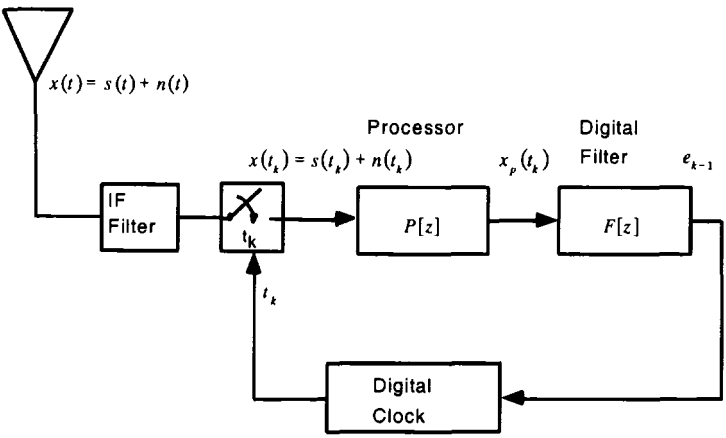


Figure 9.1 Digital Clock in a Phase-Locked Loop [3]

The control input, $e_{k-1}$, to the digital clock in Figure 9.1 has an implicit delay. (It is physically impossible to have a discrete input dependent upon that input.) This is similar to the delay included for the NCO in Chapter 7. How the digital clock actually implements Equation 9-2 is deferred for later discussion in this chapter.

In order to generate the control voltage to the digital clock, a processor [3] is symbolically included in Figure 9.1. The processor, P[z], develops the error term, $x_p(t_k)$ necessary to adjust the digital clock. The processor can be nonlinear or linear and is dependent upon the application. As an example, a data-aided data tracking loop for a modem has a processor to compute the correlation of the data and the most likely received waveform. In some applications, it is simply an implicit quantizer. For convenience, we write the output of the processor as

$$x_p(k) = P[x(k)] \qquad 9\text{-}3$$

Equations 9-1 and 9-2 allow us to develop the following recursive relationship for the clock sample times,

$$
\begin{aligned}
t_1 &= T_* - e_0 \\
t_2 &= t_1 + T_* - e_1 = 2T_* - e_0 - e_1 \\
&\vdots \\
t_k &= kT_* - \sum_{i=1}^{k} e_{k-1}
\end{aligned}
\qquad 9\text{-}4
$$

Let the sampled analog signal be written as

$$x(t_k) = \sqrt{2P}\,Sin[2\pi f_0 t_k + \theta_k] + n_k \qquad 9\text{-}5$$

Substituting the recursive expression for $t_k$ into Equation 9-5 yields

$$x(t_k) = \sqrt{2P}\,Sin\left[2\pi f_0\left(kT_* - \sum_{i=1}^{k} e_{k-1}\right) + \theta_k\right] + n_k \qquad 9\text{-}6$$

For reasons that will be apparent shortly, we define the nominal period of the digital clock as

$$T_* = N/f_0 \qquad 9\text{-}7$$

In Equation 9-7, we select a convenient integer, N, for the specific implementation. Substitution of the nominal period into the equation for the output of the sampler, Equation 9-6, yields

$$
\begin{aligned}
x(t_k) &= \sqrt{2P}\,Sin\left[2\pi f_0\left(k\frac{N}{f_{0*}} - \sum_{i=1}^{k} e_{k-1}\right) + \theta_k\right] + n_k \\
&= \sqrt{2P}\,Sin\left[\theta_k - 2\pi f_0 \sum_{i=1}^{k} e_{k-1}\right] + n_k
\end{aligned}
\qquad 9\text{-}8
$$

Note that the sampled signal represented by Equation 9-8 is now baseband instead of bandpass. The carrier frequency, $f_0$, has been removed from the signal to be processed by the phase-locked loop. If the sum of the error signals $2\pi f_0 \sum_{i=1}^{k} e_{k-1}$ is equal to the incoming phase $\theta_k$, then the PLL loop has synchronized to the input carrier frequency, $f_0$. For this reason, the loop configuration of Figure 9.1 is often called a carrier synchronizer.

The IF sampling technique of the digital clock allows direct down conversion of the input signal without requiring an actual mixer or sine-cosine NCO. Of course, the design is constrained by the requirement to select the nominal clock period. (This becomes difficult in some modems that provide bit rates adjustable in 1 Hz increments.)

Examination of Equation 9-8 suggests that the phase error between the input and the sampled output can be defined as

$$\begin{aligned}\phi(k) &= \theta(k) - \hat{\theta}(k) \\ &= \theta(k) - 2\pi f_0 \sum_{i=1}^{k} e_{k-1}\end{aligned} \qquad 9\text{-}9$$

Note in equation 9-9, $\phi(k)$ represents the phase error, it is not the equivalent of $\theta_o$ of the analog and transformed analog loops! (Recall in these loops, $\theta_o$ was the output phase to the phase detector or mixer, not the phase detector error.) The phase error estimate, $\hat{\theta}(k)$, is an accumulation of the control voltages to the digital clock. We can obtain a recursive equation for the phase error by expressing the phase error at times **k+1** and k, and then subtracting the last equation from the first.

$$\phi(k+1) = \theta(k+1) - 2\pi f_0 \sum_{i=1}^{k+1} e_{k-1}$$

$$\phi(k) = \theta(k) - 2\pi f_0 \sum_{i=1}^{k} e_{k-1} \qquad 9\text{-}10$$

$$\Rightarrow \phi(k+1) - \phi(k) = \theta(k+1) - \theta(k) - 2\pi f_0 e_k$$

To proceed further, we must define the filter F(z), and the processed output $x_p(t_k)$, from the processor in Figure 9.1. (This will define $e_k$.) The digital filter for phase-locked loops has the general form

$$F(z) = \sum_{m=1}^{N} G_m \left(1 - z^{-1}\right)^{-m+1} \qquad 9\text{-}11$$

Where $G_m$ is the filter coefficient of the m$^{th}$ filter stage. N is the number of filter stages. The quantity (N-l) also determines the highest order of

integrator in the filter. (Recall the order for the complete phase-locked loop = N). The block diagram for first and second order filters are shown in Figure 9.2.

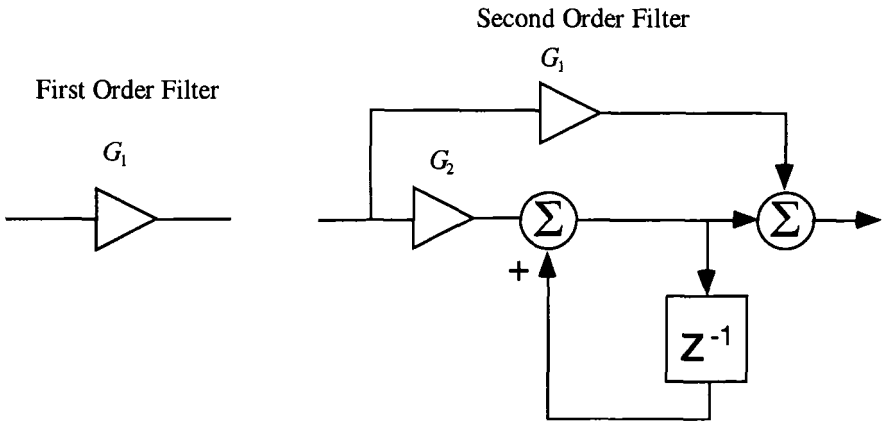


Figure 9.2 Modified Loop Filters

### 9.1.1. Second Order Digital Phase-Locked Loop Equations

From Figure 9.2, it is apparent that higher order filters can be synthesized from Equation 9-11 and cascading elements. We note that the second order filter above can be made equivalent to the bilinear transform of the active second order filter. The equivalence is

$$G_1 + \frac{G_2}{1-z^{-1}} \Rightarrow F_{bilinear}(z) = \frac{1-\tau_2 C + z(1+\tau_2 C)}{\tau_1 C(z-1)}$$

$$\text{Where } G_1 = \frac{1-\tau_2 C}{\tau_1 C}, G_2 = \frac{2}{\tau_1 C}, C = \frac{2}{T_s} \qquad 9\text{-}12$$

$$\text{and } F(s) = \frac{\tau_2 s + 1}{\tau_1 s}$$

Equation 9-12 is not the only design method for specifying the digital filter, F(z). Later, we will show how the impulse response of the closed loop

transfer function can be made into a sampled version of the traditional active second order loop.

Although the proof comes later, a digital phase-locked loop with **N=nN** can track an input of the form $\theta(t) = a + bt + ct^2 + \cdots + mt^{nN}$

Earlier, the phase error, $\phi(k)$, had been defined as $\phi(k) = \theta(k) - 2\pi f_0 \sum_{i=1}^{k} e_{k-1}$ . From Equation 9-8, this is the phase argument of a sine function, and allows the input to be written as

$$x(t_k) = \sqrt{2P}\,Sin[\phi(k)] + n_k \qquad 9\text{-}13$$

Similar to the linearized analysis of the analog phase-locked loops in Chapter 2, we approximate $Sin[\phi(k)] \approx \phi(k)$ when $\phi(k) << 1$. This is certainly true when the loop is accurately tracking the input. Acquisition analysis needs to include the nonlinearity, which we will consider later.

To further simplify the analysis, we assume the processor is linear, with a gain, $G_p$. The processor also filters the noise samples such that the output noise is represented by $n'_k$. (This is similar to modem design where we are concerned only with representing the information accurately.) [4]

$$P[x_k + n_k] = G_p x_k + G_p n'_k \qquad 9\text{-}14$$

The linear assumption for phase error, $Sin[\phi(k)] \approx \phi(k)$, and the linear processor of Equation 9-14, allows the recursive Equation 9-10 to be rewritten

$$\phi(k+1) - \phi(k) =$$
$$\theta(k+1) - \theta(k) - 2\pi f_0 \sum_{m=0}^{\infty} f(m-k)\left(\sqrt{2P}G_p\phi(k) + G_p n'(k)\right) \qquad 9\text{-}15$$

We have represented the filtering action of the loop filter in Figure 9.1 by the convolution of f(k) with the signal-plus-noise term of $\sqrt{2P}G_p x(k) + G_p n'(k)$.The digital filter's impulse function is represented by f(k) in Equation 9-15. The cumbersome convolution is removed by taking the Z-Transform of Equation 9-15.

$$\phi(z)(1-z^{-1}) = \theta(z)(1-z^{-1}) - 2\pi f_0 \sqrt{2P} G_p F(z) z^{-1}\left(\phi(z) + \frac{N'(z)}{\sqrt{2P}}\right) \quad 9\text{-}16$$

Simplification of Equation 9-16 yields

$$\phi(z)\left(1 + \frac{2\pi f_0 \sqrt{2P} G_p F(z)}{z-1}\right) = \theta(z) - \frac{2\pi f_0 \sqrt{2P} G_p F(z) N'(z)}{z-1 \qquad \sqrt{2P}} \quad 9\text{-}17$$

Recall that $\phi(k)$ represents the phase error, and not the loop output. Typically phase-locked loop transfer functions are defined to provide the loop output, and not the error term. We work around this by defining the closed loop *output* transfer function, $H_c(z)$ as

$$H_c(z) = \frac{2\pi f_0 \sqrt{2P} G_p F(z)}{(z-1) + 2\pi f_0 \sqrt{2P} G_p F(z)} \quad 9\text{-}18$$

$H_c(z)$ is the equivalent of the closed loop transfer function for the analog phase-locked loops. This permits Equation 9-17 to be written as

$$\phi(z) = [1 - H_c(z)]\theta(z) - H_c(z)\frac{N'(z)}{\sqrt{2P}} \quad 9\text{-}19$$

As with the analog phase-locked loops, the transfer function for the error response, $H_e(z) = 1 - H_c(z)$. This is consistent because substitution in Equation 9-19 for zero noise has. $\frac{\phi(z)}{\theta(z)} = H_e(z)$

To proceed further with Equation 9-18, we must specify F(z). The first order filter has $F(z) = G_1$, and the second order filter has

$F(z) = G_1 + \frac{G_2}{1 - z^{-1}}$. We can substitute the second order filter's equation into Equation 9-18, and set $G_2 = 0$ for a first order loop equation.

$$H_c[z] = \frac{\sqrt{2P}2\pi f_0 G_p (G_1(z-1) + G_2 z)}{(z-1)^2 + \sqrt{2P}2\pi f_0 G_p (G_1(z-1) + G_2 z)} \qquad 9\text{-}20$$

We can convert the closed loop transfer function of Equation 9-20 into the transfer function for the error response by the relationship, $H_e(z) = 1 - H_c(z)$

$$H_e[z] = \frac{(z-1)^2}{(z-1)^2 + \sqrt{2P}2\pi f_0 G_p (G_1(z-1) + G_2 z)} \qquad 9\text{-}21$$

This is simplified with normalized parameters as

$$H_e[z] = \frac{(z-1)^2}{(z-\alpha)^2 + \beta^2} \qquad 9\text{-}22$$

The normalized closed loop transfer function is

$$H_c[z] = \frac{\alpha^2 + \beta^2 - 1 - 2z(\alpha - 1)}{z^2 - 2\alpha z + \beta^2} \qquad 9\text{-}23$$

With the normalized error transfer function of Equation 9-22, the difference equation of Equation 9-15 with no noise can be written as

$$\phi(k) - 2\alpha\phi(k-1) + (\alpha^2 + \beta^2)\phi(k-2) = \theta(k) - 2\theta(k-1) + \theta(k-2) \qquad 9\text{-}24$$

with initial conditions of $\phi(-2) = \phi(-1) = 0$ if the phase-locked loop starts at time t=0 with zero initial states.

By defining the normalized parameters of the digital phase-locked loop with

$$\alpha = e^{-\zeta w_n T} Cos\left[w_n T\sqrt{1-\zeta^2}\right]$$
$$\beta = e^{-\zeta w_n T} Sin\left[w_n T\sqrt{1-\zeta^2}\right] \qquad 9\text{-}25$$

then the closed loop transfer function, $H_c[z]$, has the equivalent impulse transfer function of the analog loop, $H_c[s] = \dfrac{2\zeta w_n s + w_n^2}{s^2 + 2\zeta w_n s + w_n^2}$, with the normalized natural frequency, $w_n$, and damping ratio $\zeta$ [3]. Substitution of Equation 9-25 into the normalized transfer function, Equation 9-23, yields

$$H_c[z] = \frac{1 + e^{2\zeta w_n T}(-1+2z) - 2e^{\zeta w_n T} z Cos\left[w_n T\sqrt{1-\zeta^2}\right]}{e^{2\zeta w_n T} z^2 - 2e^{\zeta w_n T} z Cos\left[w_n T\sqrt{1-\zeta^2}\right] + 1} \qquad 9\text{-}26$$

The corresponding transfer function for the error response is

$$H_e[z] = \frac{e^{2\zeta w_n T}(-1+z)^2}{e^{2\zeta w_n T} z^2 - 2e^{\zeta w_n T} z Cos\left[w_n T\sqrt{1-\zeta^2}\right] + 1} \qquad 9\text{-}27$$

Equations 9-26 and 9-27 are formidable because of the transcendental functions, but the phase-locked loop transfer function is usually analyzed in the form of Equation 9-22. To provide the design coefficients for the desired performance from the specified loop natural frequency, $w_n$, and damping ratio, $\zeta$, we provide the following [3]

$$\sqrt{2P} G_p G_1 = \frac{1 - e^{-2\zeta w_n T}}{2\pi f_0}$$
$$\sqrt{2P} G_p G_2 = \frac{1 + e^{-2\zeta w_n T} - 2e^{-\zeta w_n T} Cos\left[w_n T\sqrt{1-\zeta^2}\right]}{2\pi f_0} \qquad 9\text{-}28$$

### 9.1.2. First Order Loop Equations

For those interested, substituting $G_2 = 0$ into Equation 9-20 yields the closed loop transfer function for the first order digital loop. Simplification after the substitution provides

$$H_c(z) = \frac{2\pi f_0 \sqrt{2P} G_p G_1}{(z-1) + 2\pi f_0 \sqrt{2P} G_p G_1} \qquad 9\text{-}29$$

$$H_e(z) = \frac{-1+z}{(z-1) + 2\pi f_0 \sqrt{2P} G_p G_1} \qquad 9\text{-}30$$

## 9.2. Noise Analysis of the Second Order Loop

Before discussing the second order loop responses to various inputs as in Chapter 2, we want to consider the noise performance. As with the noiseless derivation, we return to Equation 9-19.

Recall the definition of noise variance for the digital phase-locked loops, Equation 8-22, $\sigma_\theta^2 = \frac{1}{j2\pi} \oint H_C[z] H_C[z^{-1}] \frac{S_{n_s n_s}[z]}{2P} z^{-1} dz$. This result is directly applicable to this all-digital phase-locked loop. The one-sided noise bandwidth is also defined as

$$\frac{2B_L}{B_i} = \frac{1}{j2\pi} \oint H_C[z] H_C[z^{-1}] z^{-1} dz \qquad 9\text{-}31$$

where $S_{n'n'}[z]$ is the power spectral density of the noise. Substitution of the error response transfer function (Equation 9-22) into the noise bandwidth ratio equation, Equation 9-31 yields

$$\frac{2B_L}{B_i} = \frac{4}{(1+\alpha)^3 + (1+\alpha)\beta^2} + \frac{2(-1+\alpha)}{(1+\alpha) + (-1+\alpha^2+\beta^2)} - 1 \qquad 9\text{-}32$$

The noise bandwidth ratio of Equation 9-32 can be expressed with the natural loop frequency, $w_n$ and damping ratio, $\zeta$ parameters as

$$\frac{2B_L}{B_i} = \frac{1 - 2e^{2\zeta\omega_n T} + 5e^{4\zeta\omega_n T} + \left(2e^{\zeta\omega_n T} - 6e^{3\zeta\omega_n T}\right)Cos\left[\omega_n T\sqrt{1-\zeta^2}\right]}{\left(e^{2\zeta\omega_n T} - 1\right)\left(1 + e^{2\zeta\omega_n T} + 2e^{\zeta\omega_n T}Cos\left[\omega_n T\sqrt{1-\zeta^2}\right]\right)} \qquad 9\text{-}33$$

Consequently the techniques developed in Chapter 8 are directly applicable to computing the noise bandwidth of these digital phase-locked loops. (Recall the approach is use residues and compute only those that are within the unit circle.)

---

## *Example 9.1*

Design a digital sampling phase-locked loop with the following parameters:

Loop Sampling Frequency = 100 Hz, Carrier Frequency = 200 Hz, Processing Gain = 1.0, $\zeta = 0.707$, and $2B_L/B_i = 0.05$

(See 2-81 for computing $\sqrt{2P}$. Must include the 50 ohm resistor.)

We begin with Equation 9-33, because we need to determine the required $\omega_n$. This is a nonlinear equation and $\omega_n$ can be found by iterating Equation 9-33 with successive "guesses". Alternatively, a numerical analysis tool can provide the solution. Using such a tool (Mathematica), we find

$$\frac{2B_L}{B_i} = 0.05\Big|_{\zeta=0.707, T=\frac{1}{100}} \Rightarrow \omega_n = 4.61 \qquad 9\text{-}34$$

We would expect the digital loop to approach the behavior of the analog loop, since the closed loop gain Equation 9-21 was specified to have the

equivalent analog impulse response. Recall from Chapter 3, $\omega_n = \dfrac{2B_L}{\zeta + \dfrac{1}{4\zeta}}$ for a second order loop. Substituting $B_i = f_s$ into the problem statement, we obtain $B_L = 2.5$ Hz. Placing the noise bandwidth ratio into the expression for $\omega_n$, yields a loop natural frequency, $\omega_n = 4.71$, which is a close agreement to our analog design.

Noting that the processing gain, $G_p$, is unity, Equations 9-28 allow $G_1$ and $G_2$ to obtained by substitution.

$$G_1 = \frac{1 - e^{-2\zeta w_n T}}{2\pi f_0 \sqrt{2P} G_p} = 0.000159 \qquad 9\text{-}35$$

$$G_2 = \frac{1 + e^{-2\zeta w_n T} - 2e^{-\zeta w_n T} Cos\left[w_n T\sqrt{1-\zeta^2}\right]}{2\pi f_0 \sqrt{2P} G_p} = 5.183 \times 10^{-6} \qquad 9\text{-}36$$

The complete error response transfer function is

$$H_e[z] = \frac{(z-1)^2}{9.96699 \times 10^{-4} + (z - 0.967398)^2} \qquad 9\text{-}37$$

The block diagram of the phase-locked loop design can now be constructed. Figure 9.3 shows the phase-locked loop with the digital filter coefficients computed in Equations 9-34 and 9-35. We show the frequency $f_s = 100Hz$ input to the digital clock.

As discussed previously, if the sampling frequency is an integer multiple of the carrier frequency, then the phase-locked loop demodulates the carrier on the incoming signal without requiring a downconversion mixer. Again though, this requires the loop's sampling frequency to be an integer multiple of the analog IF signal's frequency.

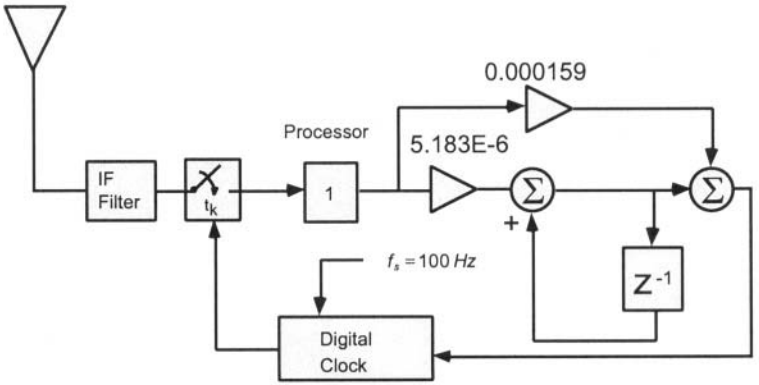


Figure 9.3 Block Diagram of Example 9.1 Phase-Locked Loop Design

The stability of the loop is verified with a pole-zero plot of the error response function in Figure 9.4. As shown in the figure, the poles are close to the unit circle, although the loop is stable. This suggests that a root locus should be computed to determine the stability sensitivity to gain and coefficient quantization.

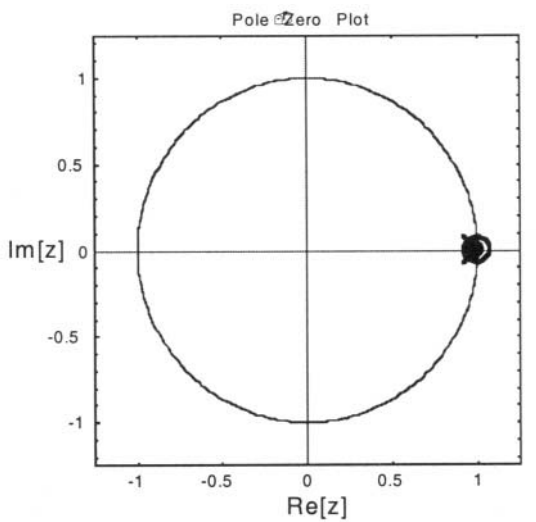


Figure 9.4 Pole-Zero Plot of the Phase-Locked Loop Design

Because the phase-locked loop was designed to approximate the analog phase-locked loop response, it is of interest to graph the step response. First,

the inverse Z-Transform of the loop's error step response, $H_{eStep}[z] = \frac{z}{z-1} \frac{(z-1)^2}{9.96699 \times 10^{-4} + (z-0.967398)^2}$ is computed.

$$h_{eStep}[n] = ((0.5 - j0.516336)(0.967398 - j0.0315705)^n + (0.5 + j0.516336)(0.967398 + j0.0315705)^n)u(n) \quad \text{9-38}$$

The error step response is graphed in Figure 9.5. Recall from the study of second order analog loops, we expect the peak undershoot to occur at $\omega_n t = 2.3$. The peak undershoot of Figure 9.5 is approximately n=47. This permits $\omega_n t$ to be computed as

$$\omega_n t = 4.61 \frac{47}{100} = 2.16 \quad \text{9-39}$$

This normalized value for the peak overshoot shows the digital loop's time response is a reasonable approximation to the performance of the analog loop.

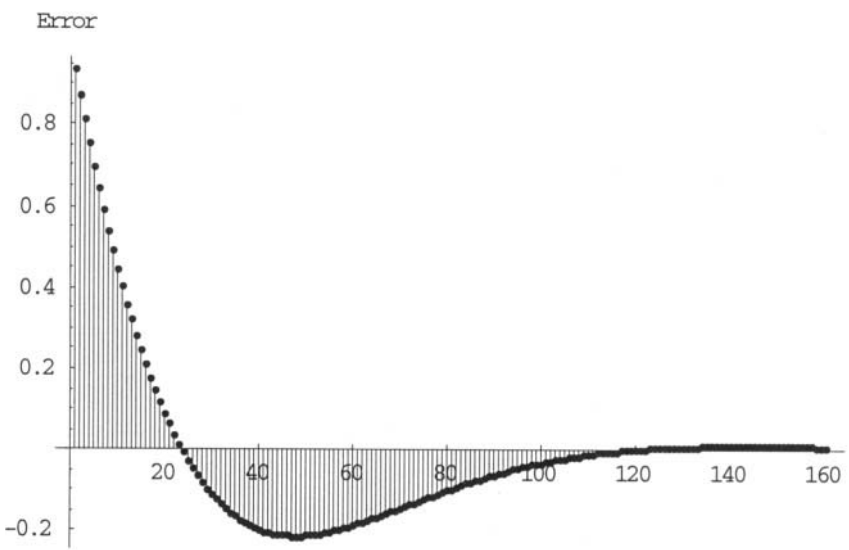


Figure 9.5 Step Error Response of the Phase-Locked Loop Design

## 9.3. Noise Bandwidth of First Order Loops

As before, we find the noise bandwidth from the relationship, $\frac{2B_L}{B} = \frac{1}{j2\pi}\oint H_C[z]H_C[z^{-1}]z^{-1}dz$. $H_C$ for the first order loop is obtained from Equation 9-29. Then the contour integral is computed by using the residue theorem. The integral is represented as

$$I = \frac{1}{j2\pi}\oint \frac{2\pi f_0\sqrt{2P}G_pG_1 \qquad 2\pi f_0\sqrt{2P}G_pG_1}{(z-1)+2\pi f_0\sqrt{2P}G_pG_1(1-z)+2\pi f_0\sqrt{2P}G_pG_1}dz \qquad 9\text{-}40$$

From the residue theorem, we compute the integral as

$$I = \left.\frac{2\pi f_0\sqrt{2P}G_pG_1 \qquad 2\pi f_0\sqrt{2P}G_pG_1}{1 \qquad (1-z)+2\pi f_0\sqrt{2P}G_pG_1}\right|_{z=1-2\pi f_0\sqrt{2P}G_pG_1} \qquad 9\text{-}41$$

The step between Equation 9-40 and 9-41 is made assuming that the integration is along the closed contour $|z|=1$. In order for $H_c[z]$ to be stable, its pole must be within the unit circle. That implies that the pole for $H_c[z^{-1}]z^{-1}$ is outside the unit circle. Recall the residue theorem states that we only consider poles within the unit circle, so we disregard the pole for $H_c[z^{-1}]z^{-1}$ in the computation of Equation 9-41. Completing the algebra of Equation 9-41, we obtain the noise bandwidth of the first order loop.

$$\frac{2B_L}{B_i} = \frac{1}{1-2\pi f_0\sqrt{2P}G_pG_1} - 1 \qquad 9\text{-}42$$

***Example 9.2***

Design a first order digital sampling phase-locked loop with the following parameters:

Loop Sampling Frequency = 100 Hz, Carrier Frequency = 200 Hz,
Processing Gain = 1.0, and $2B_L/B_i = 0.05$

(See 2-81 for computing $\sqrt{2P}$. Must include the 50 ohm resistor.)

Substituting in the problem statement parameters into Equation 9-42, we obtain

$$G_1 = 0.00012 \qquad 9\text{-}43$$

Substituting the gain of Equation 9-43, and the problem statement parameters into the first order Equations 9-29 and 9-30, yields

$$H_c[z] = \frac{0.0476}{z - 0.952} \qquad 9\text{-}44$$

$$H_e[z] = \frac{z - 1}{z - 0.952} \qquad 9\text{-}45$$

By inspection, this first order loop is unconditionally stable. (The single pole is at $z = 0.952$, inside the unit circle.) The inverse Z-Transform of the error response, Equation 9-45, is

$$h_{e,step} = 0.952^n u(n) \qquad 9\text{-}46$$

For comparison, we plot the error response of the first order loop in Figure 9.6. Note that the first order loop does not exhibit the overshoot like the second order loop of Figure 9.5.

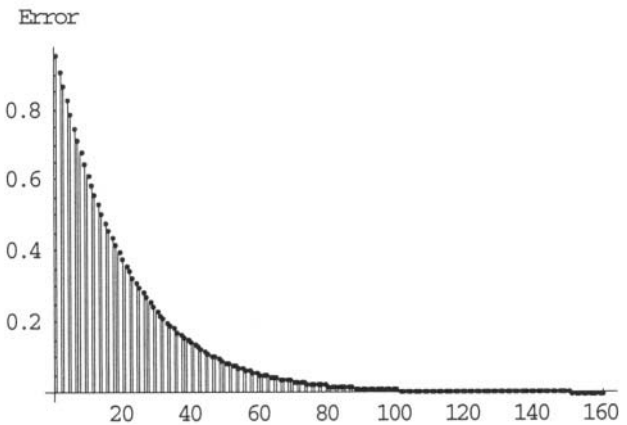


Figure 9.6 Step Error Response of the First Order Loop

## 9.4. Components of Digital Phase-Locked Loops

So far in this chapter, we have shown the advantages and theory of the phase-locked loop with the non-uniform sampling. After this analysis, we can begin the discussion of how to actually construct such a phase-locked loop. Figure 9.7 shows a block diagram of a digital clock derived from a simple preset counter.

The most important idea of Figure 9.7 is the digital filter is generating a digital word (multiple bits) to the comparator. The timer counts down from the counter's preset register contents (represented by the digital value of M) until it is preset by the comparator. The comparator is continually comparing the digital word represented by the counter's state and the digital error word from the filter.

The master clock has a clock period of $T_M$. Suppose that the error word, $d_{k-1}$, is less than M. Then the next clock period is

$$\begin{aligned} T_k &= (M - d_{k-1})T_M \\ &= M T_M - d_{k-1} T_M \end{aligned} \qquad 9\text{-}47$$

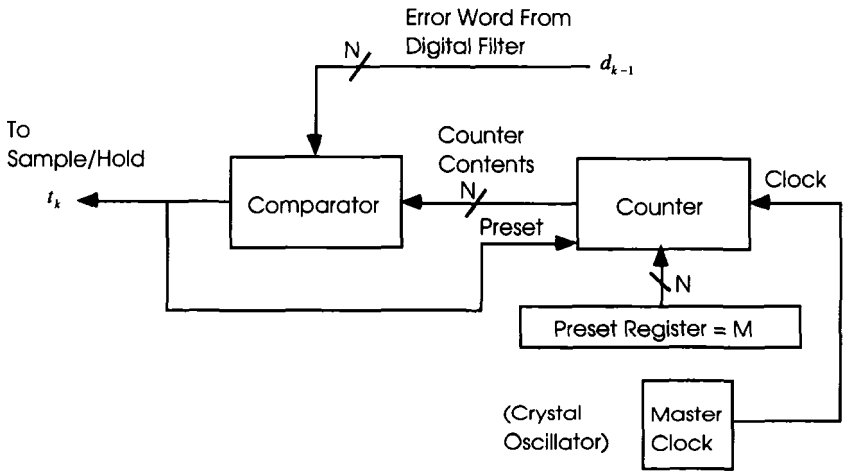


Figure 9.7 Timer-Based Digital Clock [2]

If we select the master clock period and preset value such that $MT_M = T_* = N/f_0$, and define $e_{k-1} = d_{k-1}T_M$, then our digital clock period has the equation

$$T_k = T_* - e_{k-1} \qquad 9\text{-}48$$

This is identical to Equation 9-2, which was used to demonstrate the implicit downconversion of Figure 9.1. Next, we return to Equation 9-10, and define our phase estimate, $\hat{\theta}_k$, as

$$\hat{\theta}_k = 2\pi f_0 \sum_{i=1}^{k} e_{k-1} \qquad 9\text{-}49$$

We use Equation 9-10 to discover the relationship

$$\hat{\theta}_k = 2\pi f_0 \sum_{i=1}^{k} e_{k-1}$$

$$\hat{\theta}_1 = 2\pi f_0 e_0$$

$$\hat{\theta}_2 = 2\pi f_0 e_0 + 2\pi f_0 e_1 = \hat{\theta}_1 + 2\pi f_0 e_1 \qquad 9\text{-}50$$

$$\vdots$$

$$\hat{\theta}_k = 2\pi f_0 e_{k-1} + \hat{\theta}_{k-1}, k > 1$$

By taking the Z-Transform of the final result of Equation 9-50, we obtain

$$\hat{\theta}(z) = \frac{2\pi f_0 z^{-1} e(z)}{1 - z^{-1}} \qquad 9\text{-}51$$

With some algebraic operations on Equation 9-51, we can obtain the transfer function of the digital clock.

$$H(z) = \frac{\hat{\theta}(z)}{e(z)} = \frac{2\pi f_0 z^{-1}}{1 - z^{-1}} \equiv \frac{K_0 z^{-1}}{1 - z^{-1}} \qquad 9\text{-}52$$

Equation 9-51 is the same as the sine-cosine NCO of Equation 7-47, although we have a completely different architecture. This NCO has the same backward Euler integrator configuration. (Recall because of the delay, this NCO is conditionally stable [7].)

An alternative configuration often used in processor-based phase-locked loops is shown in Figure 9.8. This architecture uses a timer with a preset to implement a digital clock.

The fundamental idea of Figure 9.8 is that the digital filter is providing a digital word (multiple bits) to the preset register. The timer counts down from the register contents until it reaches zero, and the terminal count pulse is generated. The terminal count pulse then causes the next preset register contents to be loaded into the counter and it begins counting down on the next clock pulse from the crystal oscillator. When the digital clock generates the terminal count from the countdown timer, the terminal count is used as a timing pulse, usually to cause a sample and hold to sample the analog input.

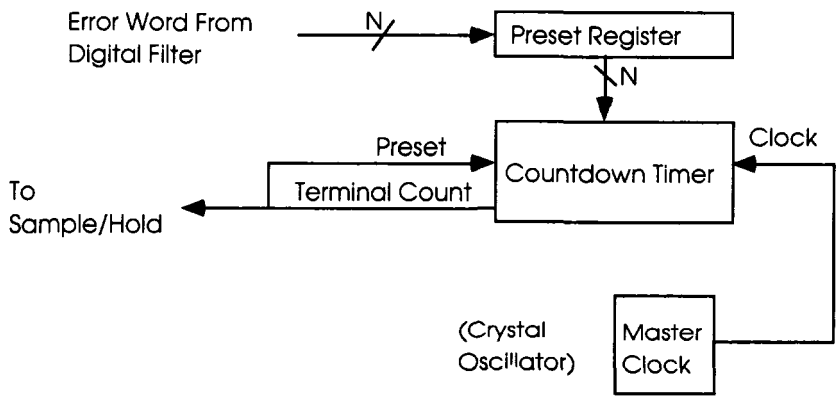


Figure 9.8 Timer-Based Digital Clock

Mathematically we represent this NCO having a clock period, $T_*$, as

$$T_* = P\,T_C \qquad 9\text{-}53$$

where

$P$ = Counter Preset Word (Digital Filter Output)

$T_C$ = Master Clock Period

We can define the control word, P, as containing a nominal integer (offset frequency) and an error term as

$$P = M - d_{k-1} \qquad 9\text{-}54$$

Substitution of Equation 9-54 into 9-53 yields the exact same digital clock equation as the digital clock of Figure 9.7 ( $T_* = (M - d_{k-1})T_C$ )

## 9.5. Phase Detectors

In Chapter 7, we considered a multiplying phase detector (which we linearized for analysis), that is appropriate for phase-locked loops at lower sampling frequencies. In higher speed applications, we often find a phase

detector based on a zero-crossing detector. The zero-crossing detector generates a pulse that is begun by the zero-crossing detector and terminated at the zero-crossing of the reference. Figure 9.9 shows the block diagram for such a phase detector.

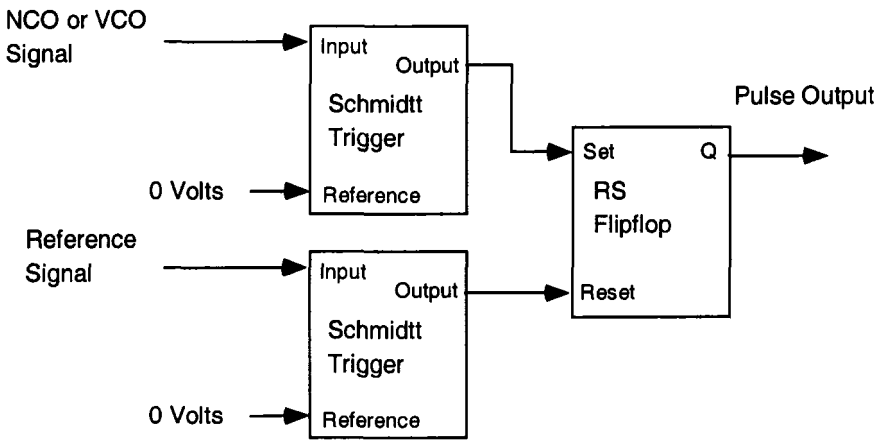


Figure 9.9 Zero-Crossing Phase Detector

In Figure 9.9, the Schmidtt Trigger is a zero-crossing detector with hysteresis, with the transfer characteristic illustrated in Figure 9.10.

In Figure 9.10, once the input to the Schmidtt Trigger has exceeded 1.2 volts and the output pulse has been generated, then the input must go below 0.8 volts before another output pulse can be generated. This helps to prevent noise from creating excessive jitter on the output. It also constrains the component to generate pulses only on positive zero-crossings.

A timing diagram for the zero-crossing phase detector is shown in Figure 9.11. The pulse begins on the rising edge of the VCO's input and ends on the rising edge of the reference signal. In this particular example, the two signals have different frequencies, which explains why the phase detector output does not have a constant width.

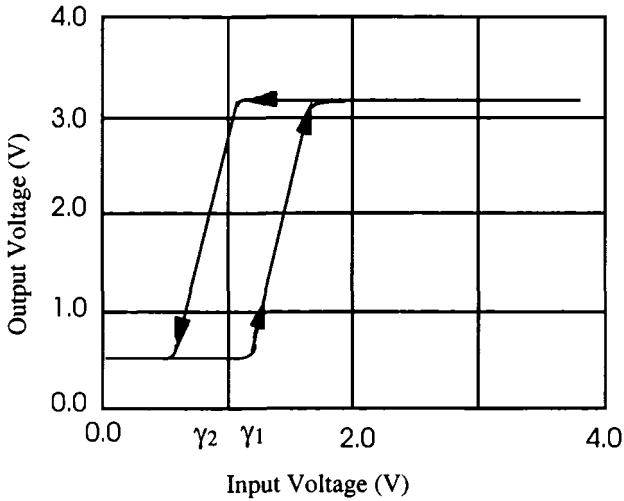


Figure 9.10 Transfer Characteristic of a Schmitt-Trigger

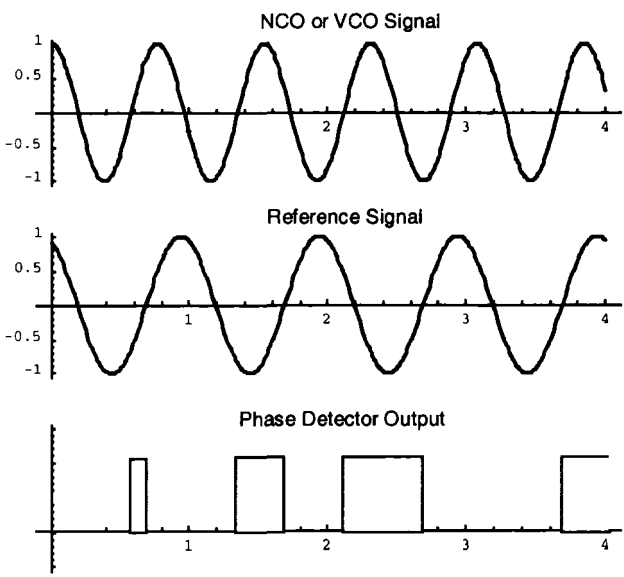


Figure 9.11 Output for Zero-Crossing Phase Detector

Figure 9.11 shows that the output of the phase detector in Figure 9.9 is pulse duration-modulated. When the two signals are aligned exactly in phase and frequency, then the output of the phase detector will be zero. A phase plane analysis of the phase detector will show this is not a stable null, because if noise causes it to shift just slightly, then a complete cycle slip will result.

A better loop configuration results if a DC voltage representing 1/2 of the pulse amplitude is subtracted from the output. This results in a symmetrical phase detector characteristic, and a zero-seeking loop will yield a $\pi$ phase difference between the reference and input signals.

There are other circuit variations of Figure 9.9, such as Figure 9.12, which reduces the severe quantization error of the zero crossing phase detector. The clock for the phase detector of Figure 9.12 is operating at a much higher frequency than either the reference or input signals. This allows the synchronous counter to count up to a digital word, N, before being reset. The numeric size (integer) of N represents the phase error.

A similar phase detector uses a sample-and-hold to produce an analog voltage instead of the digital error word shown in Figure 9.12. A capacitor is charged with current controlled by an analog switch. The input signal initiates a charge and the reference signal terminates it [9]. This type of phase detector produces a sawtooth for a phase error transfer function.

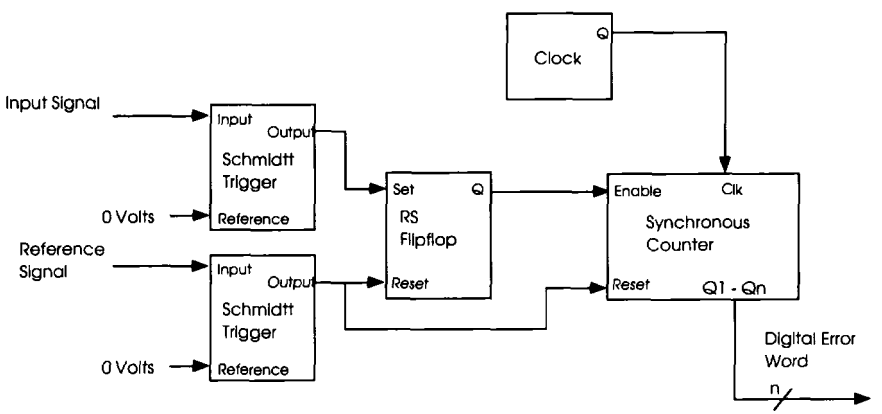


Figure 9.12 Zero Crossing Phase Detector With Word Output

### 9.5.1. Sequential Phase Detector

A popular phase detector for hardware implementations is called the lead-lag sequential phase detector [5,9]. In connection with charge pumps, it was discussed in Chapter 6.

### 9.5.2. Hilbert Transform Phase Detector

A popular phase detector for software-based phase detectors is shown in Figure 9.13 [9]. Fundamental to the implementation is the complex sinusoid (Sine and Cosine) generated by the NCO. [11]

### 9.5.3. Timing Phase Detector

A popular phase detector for timing synchronization is the early-late gate phase detector shown in Figure 9.14. This particular phase detector is often used in spread spectrum code tracking loops and in modems to synchronize the symbol timing. It is called an early-late gate because one path of the loop is advanced with respect to the main signal. The later path is delayed with respect to the main signal. For a modem, the main signal would correspond to the optimum symbol sampling time.

In Figure 9.14, a complete tracking loop is shown, because of the need to generate two reference waveforms. One waveform is ahead (early) of the other, which is late. The two waveforms are each a fraction of the clock period apart. Conceptually, the idea is that the loop will center the incoming waveform exactly $\Delta/2$ apart from either reference waveform. The phase detector then has a discriminator output shown in Figure 9.15 for $\Delta = 2$ (Note this means one reference waveform is delayed by 1/2 clock period and the other waveform is time advanced by 1/2 clock period.)

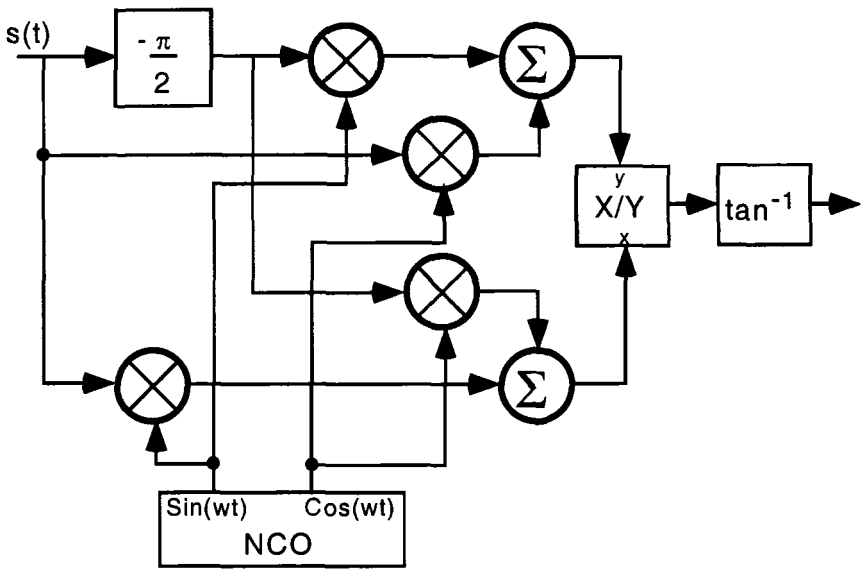


Figure 9.13 Hilbert Transform Phase Detector [9]

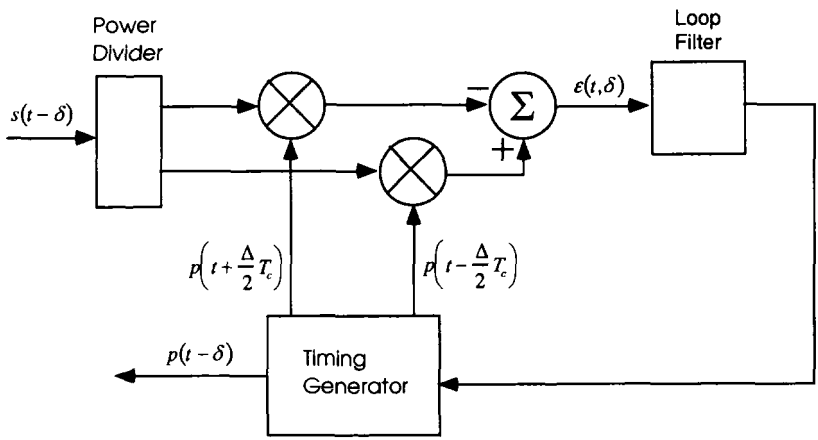


Figure 9.14 Early-Late Tracking Loop [4]

The input to the loop filter is the actual output from the phase detector and represented in Figure 9.15. Besides generating the early and late reference waveform, the timing generator also generates the desired signal, $p(t-\delta)$, which is time-aligned with the input signal. The early-late tracking loop will be discussed in greater detail in Chapter 11.

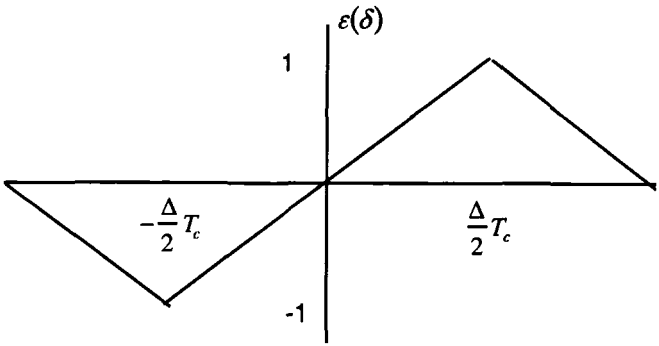


Figure 9.15 Early-Late Phase Detector Characteristic

## 9.6. References

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## 9.7. Problems

9.1 The digital loop has a transfer function of

$$\phi(k+1)-\phi(k)=\theta(k+1)-\theta(k)$$
$$-2\pi f_0\sum_{m=0}^{\infty} f(m-k)\left(\sqrt{2P}G_p\phi(k)+G_p n'(k)\right)$$

Plot the recursive relationship for $\phi(k)$, assuming a first order phase-locked loop with the following parameters: $f(k)=\delta(k)$ $\theta(0)=\phi(0)=0$, $\theta(k)=1$, $k\neq 0$ and $\sqrt{2P}=1$. Plot $\phi(k)$ for $0\le k\le 10$, with a) $G_p=10^{-3}$, b) $G_p=10^{-4}$, and c) $G_p=10^{-5}$

9.2 The digital loop has a transfer function of

$$\phi(k+1)-\phi(k)=\theta(k+1)-\theta(k)$$
$$-2\pi f_0\sum_{m=0}^{\infty} f(m-k)\left(\sqrt{2P}G_p\phi(k)+G_p n'(k)\right).$$

Plot the recursive relationship for $\phi(k)$, assuming a first order phase-locked loop with the following parameters: $f(k)=\delta(k)$, $\theta(0)=1$, $\theta(k)=4$, $k\neq 0$, $\phi(0)=3$ and $\sqrt{2P}=1$. Plot $\phi(k)$ for $0\le k\le 10$, with a) $G_p=10^{-2}$, b) $G_p=10^{-3}$, and c) $G_p=10^{-4}$

9.3 Design a second-order carrier synchronizer loop (Figure 9.1) with $2B_L/B_i=0.25$, carrier frequency = 125 Hz, loop sampling frequency of 3 KHz, damping factor = 0.707, input power =

$10^{-3}\,W$, and processing gain = 1.0. Sketch the loop's block diagram.

9.4 Design a second-order carrier synchronizer loop (Figure 9.1) with $2B_L/B_i = 0.45$, carrier frequency = 35 Hz, loop sampling frequency = 200 Hz, damping factor = 0.707, input power = $10^{-3}\,W$, and processing gain = 1.0. Sketch the loop's block diagram.

9.5 Design a first-order carrier synchronizer loop (Figure 9.1) with $2B_L/B_i = 0.17$, carrier frequency = 180 Hz, loop sampling frequency = 10 KHz, damping factor = 0.707, input power = $3\times10^{-3}\,W$, and processing gain = 1.0. Sketch the loop's block diagram. Sketch the loop's block diagram.

9.6 Design a first-order carrier synchronizer loop (Figure 9.1) with $2B_L/B_i = 0.27$, carrier frequency = 3.7 Hz, loop sampling frequency = 60 Hz, damping factor = 0.707, input power = $10\times10^{-3}\,W$, and processing gain = 1.0. Sketch the loop's block diagram.

9.7 Sketch out an algorithm to implement the sequential phase detector in software.

9.8 Sketch a multiplicative phase detector's transfer characteristic for a square wave reference input with an asymmetrical signal input. Consider the signal having a waveform that has only a 10% logic high with 90% logic low.Sketch the multiplicative phase detector's transfer characteristic with the following two input signals: a) $Cos(\omega t + \phi)$
b) $Cos(\omega t) + Cos(2\omega t)$

9.9 Sketch out an algorithm to implement the Hilbert Transform phase detector in software.

# 10

# Digital PLL Responses and Acquisition

In this chapter, we will evaluate the digital phase-locked loops for phase inputs similar to the analysis of analog phase-locked loops in Chapter 4. This analysis will be on linearized transfer functions, and applies to the complete digital loops of Chapter 9 as well as the analog/digital phase-locked loops of Chapter 8.

After the linear analysis, we will examine the nonlinear response of the complete digital phase-locked loops. This provides information about acquisition, probability of acquisition, and probability of cycle slip. The phase noise of digital phase-locked loops is also of concern, and we perform an analysis of the phase error variance.

## 10.1. Linearized Input Responses

Using the linearized transfer functions of $H_c(z)$ and $H_e(z) = 1 - H_c(z)$, the error response, $\phi(z)$ of the digital phase-locked loop to the inputs, $\theta(z)$ and $\frac{N(z)}{\sqrt{2P}}$, is

$$\phi(z) = H_e(z)\theta(z) + H_c(z)\frac{N(z)}{\sqrt{2P}} \qquad \text{10-1}$$

In Equation 10-1, recall the divisor of $\sqrt{2P}$ for *N(z)* compensates for the input signal's amplitude being included within $H_c(z)$ and $H_e(z)$. In subsequent analysis in this section, we assume noiseless operation, $N(z) \equiv 0$, for the different inputs.

Figure 10.1 tabulates the different phase step, frequency step, and frequency ramp inputs for a digital phase-locked loop. A phase step input has a forcing function of $\frac{\Delta\theta z}{z-1}$, where $\Delta\theta$ is the step size.

| Input Phase | Time Function, $\theta(t)$ | Z-Domain, $\theta(z)$ |
|---|---|---|
| Phase Step | $\Delta\theta u(t)$ | $\frac{\Delta\theta z}{z-1}$ |
| Frequency Step | $\Omega t u(t)$ | $\frac{\Omega z T}{(z-1)^2}$ |
| Frequency Ramp | $\frac{\Omega t^2}{2}u(t)$ | $\frac{\Omega T^2}{2}\frac{z(z+1)}{(z-1)^3}$ |
| Phase Modulation | $\Delta\theta Sin[\omega_m t]$ | $\Delta\theta\frac{zSin[\omega_m T]}{z^2-2zCos[\omega_m T]+1}$ |
| Frequency Modulation | $\frac{\Delta\omega}{\omega_m}Cos[\omega_m t]$ | $\frac{\Delta\omega}{\omega_m}\frac{z(z-Cos[\omega_m T])}{z^2-2zCos[\omega_m T]+1}$ |

Figure 10.1 Typical Input Functions for the Digital Phase-Locked Loop [1]

A frequency step has a forcing function of $\frac{\Omega z T}{(z-1)^2}$, where $\Omega$ is the constant offset frequency. A frequency ramp, also called a jerk [11], (because it often results from a mobile platform acceleration) is $\frac{\Omega T^2}{2}\frac{z(z+1)}{(z-1)^3}$ where $\Omega T$ is the frequency ramp in radians. Also included in Figure 10.1 are the inputs of sinusoidal phase and frequency modulation. The phase-modulated input has the form $\Delta\theta Sin[\omega_m t]$ where $\omega_m$ represents the modulating frequency and $\Delta\theta$ represents the maximum phase step. Frequency modulation has the form $\Delta\omega/\omega_m Cos[\omega_m t]$, where the term $\Delta\omega$

represents the instantaneous frequency deviation. $\omega_m$ represents the modulation frequency.

### 10.1.1. First Order Loop Responses

The error response function for a first order digital phase-locked loop is

$$H_e(z) = \frac{z-1}{(z-1)+K_1} \text{ where } K_1 = 2\pi f_0 \sqrt{2P} G_1 G_p \qquad 10\text{-}2$$

The error response transfer function for an analog/digital phase-locked loop would not have the term $2\pi f_0$ in $K_1$, but would have additional multiplicative scalars for the phase detector and NCO/VCO gains. In the Z-domain, the error response to a phase step is

$$H_{e,Step} = \frac{\Delta\theta z \quad z-1}{z-1(z-1)+K_1} \qquad 10\text{-}3$$

The corresponding time domain response is obtained with an inverse Z-Transform,

$$h_{e,Step}(n) = \Delta\theta(1-K_1)^n u(n) \qquad 10\text{-}4$$

Figure 10.2 summarizes the response of a first order digital phase-locked loop to the inputs of Figure 10.1 These are tabulated for the error response, $h_e(n)$, and not the closed loop response, $h_c(n)$, found in some references. Note for the analog/digital loops of Chapter 7, the constant $K_1$ is

$$K_1 = \sqrt{2P} K_{p.d.} K_{NCO} K_{Filter} \qquad 10\text{-}5$$

where $K_{p.d.}$ is the phase detector gain, $K_{NCO}$ is the NCO's gain constant, and $K_{Filter}$ is the scalar gain of the loop filter.

Figures 10.3 and 10.4 show the first order error responses to phase and frequency steps, respectively. The constant $K_1$ for the first order loop establishes the bandwidth of the loop, and so it is not surprising in both Figures 10.3 and 10.4 that the higher value of $K_1$ results in faster response. Besides providing the faster input response, a higher value of $K_1$ also results

in a smaller residual error due to a frequency step, as shown in Figure 10.3. This comes at the cost of higher noise sensitivity, because the first order loop has only one degree of freedom available to the designer. A second order loop can simultaneously provide minimum frequency step error and low noise bandwidth.

| Input Type | Error Response |
|---|---|
| Phase Step | $\Delta\theta(1-K_1)^n u(n)$ |
| Frequency Step | $\dfrac{\left(1-(1-K_1)^n\right)T\,\Omega\,u(n-1)}{K_1}$ |
| Frequency Ramp | $\dfrac{\left(2-2(1-K_1)^n+K_1\left(-1+(1-K_1)^n-2n\right)\right)T_s^2\,\Omega u(n-1)}{2K_1^2}$ |
| Phase Modulation | $\dfrac{\left(-K_1u(n-2)Sin[(n-1)T\omega_m]+u(n-1)\times\left(\left(-K_1(1-K_1)^n Sin[T\omega_m]+\right.\right.\right.}{\left.\left.\left.(2-K_1-2(1-K_1)Cos[T\omega_m])Sin[nT\omega_m]\right)\right)\right.}{(2+K_1(K_1-2)+2(K_1-1)Cos[T\omega_m])}$ |
| Frequency Modulation | $\dfrac{\left(\Delta\omega\,(1-K_1)^n K_1(-1+K_1+Cos[T\omega_m])u[n]+\left(\begin{matrix}-(K_1+2Cos[T\omega_m])u[n-1]Sin[T\omega_m]\\-(K_1-2)u[n]Sin[(n+1)T\omega_m]\end{matrix}\right)Tan\left[\dfrac{T\omega_m}{2}\right]\right)}{\omega_m(2+(K_1-2)K_1+2(K_1-1)Cos[T\omega_m])}$ |

Figure 10.2 First Order Digital Phase-Locked Loop Response

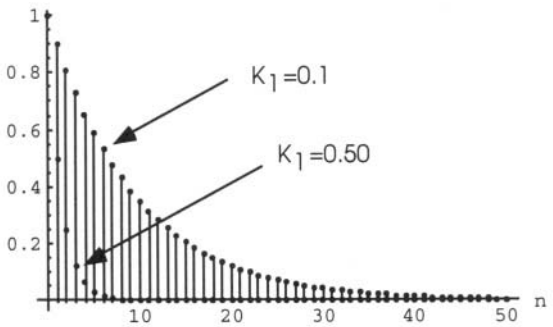


Figure 10.3 First Order Phase Step Response

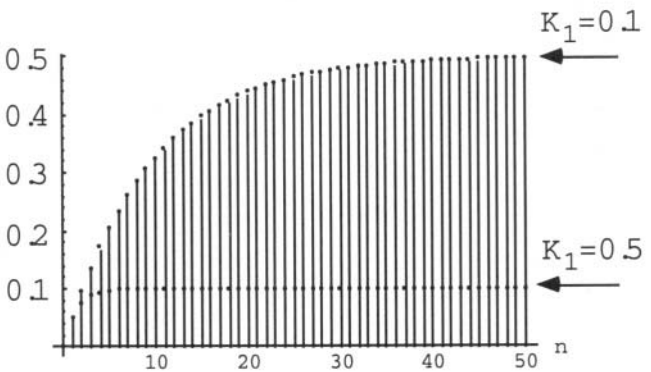


Figure 10.4 First Order Frequency Step Response

### 10.1.2. Second Order Loop Responses

The second order phase-locked loop has an error response transfer function of [4]

$$H_e[z] = \frac{(z-1)^2}{(z-\alpha)^2 + \beta^2} \qquad 10\text{-}6$$

Similar to analysis for the first order transfer function, the loop error responses may be obtained for the inputs of Figure 10.1. Recall from Chapter 9, $\alpha = e^{-\zeta w_n T} Cos\left[w_n T\sqrt{1-\zeta^2}\right]$ and $\beta = e^{-\zeta w_n T} Sin\left[w_n T\sqrt{1-\zeta^2}\right]$

for the all-digital loop. Consideration must be made for the three subsets of the loop damping factor, $\zeta$. The term, $\sqrt{1-\zeta^2}$ is real, zero, or imaginary, if $\zeta$ is $\{\zeta<1, \zeta=1, \zeta>1\}$, respectively. This can present transformation difficulties if not handled properly. Figures 10.5 -10.8 summarize the loop responses for the second order loop.

| Input Type | Error Response |
|---|---|
| Phase Step | $\frac{\Delta\theta}{2}\left(e^{-2\zeta\omega_n T}\right)^n Csch[\Psi]\left(\begin{array}{l}\left(e^{\Psi+\zeta\omega_n T}\right)^n\left(e^{\Psi}-e^{\zeta\omega_n T}\right)\\ +\left(e^{-\Psi}-e^{\zeta\omega_n T}\right)^n\end{array}\right)$ $\times\left(e^{\zeta\omega_n T}-Cosh[\Psi]+Sinh[\Psi]\right),$ $\zeta>1, \quad \Psi=\mathrm{Im}\left[\omega_n T\sqrt{1-\zeta^2}\right]$ |
| Frequency Step | $\frac{\Omega T}{2}e^{\zeta\omega_n T}\left(-\left(e^{-\Psi-\zeta\omega_n T}\right)^n+\left(e^{\Psi-\zeta\omega_n T}\right)^n\right)$ $\times Csch[\Psi]u(n-1), \quad \zeta>1, \quad \Psi=\mathrm{Im}\left[\omega_n T\sqrt{1-\zeta^2}\right]$ |
| Frequency Ramp | $\frac{\left(\begin{array}{l}-2e^{T_s\xi\omega_n}\left(-2+\left(e^{-\psi-T_s\xi\omega_n}\right)^n+\left(e^{\psi-T_s\xi\omega_n}\right)^n\right)\\ +\left(-1+e^{2T_s\xi\omega_n}\right)\left(\begin{array}{l}\left(e^{-\psi-T_s\xi\omega_n}\right)^n\\ -\left(e^{\psi-T_s\xi\omega_n}\right)^n\end{array}\right)Csch[\psi]\end{array}\right)}{4\left(1+e^{2T_s\xi\omega_n}-2e^{T_s\xi\omega_n}Cosh[\psi]\right)}$ $e^{T_s\xi\omega_n}T_s^2\Delta\Omega u[n-2]$ $\zeta>1, \quad \Psi=\mathrm{Im}\left[\omega_n T\sqrt{1-\zeta^2}\right]$ |

Figure 10.5 Second Order Loop Responses for $\zeta>1$

| Input | Error Response |
|---|---|
| Phase Step | $-\Delta\theta\left(\left(e^{\zeta\omega_n T}-1\right)n-1\right)\left(e^{-\zeta\omega_n T}\right)^n$ |
| Frequency Step | $\Omega nT\left(e^{-2\zeta\omega_n T}\right)^n\left(e^{\zeta\omega_n T}\right)^n u(n-1)$ |
| Frequency Ramp | $-\frac{T^2\Omega u(n-1)}{2\left(e^{\zeta\omega_n T-1}\right)^2}\left(\begin{array}{l}\left(e^{-2\zeta\omega_n T}\right)^n\left(e^{\zeta\omega_n T}\right)^{n+1} \\ \left(-2e^{\zeta\omega_n T}\left(\left(e^{\zeta\omega_n T}\right)^n-1\right)+\left(e^{2\zeta\omega_n T}-1\right)n\right)\end{array}\right)$ |

Figure 10.6 Second Order Loop Responses for $\zeta = 1$

| Input | Error Response |
|---|---|
| Phase Step | $-j\frac{\Delta\theta}{2}\left(\begin{array}{l}\left(e^{j\Psi-\zeta\omega_n T}\right)^n\left(e^{j\Psi-\zeta\omega_n T}\right)+\left(e^{-j\Psi-\zeta\omega_n T}\right)^n \\ \left(-e^{-j\Psi}+e^{\zeta\omega_n T}\right)\end{array}\right)$ $\times Csc[\Psi]u(n-1), \quad \zeta<1, \quad \Psi=\omega_n T\sqrt{1-\zeta^2}$ |
| Frequency Step | $\frac{j\Omega T}{2}e^{\zeta\omega_n T}\left(\left(e^{-j\Psi-\zeta\omega_n T}\right)^n-\left(e^{j\Psi-\zeta\omega_n T}\right)^n\right)$ $\times Csch[\Psi]u(n-1) \quad , \quad \zeta<1\,,\ \Psi=\omega_n T\sqrt{1-\zeta^2}$ |
| Frequency Ramp | $\left(\begin{array}{l}-2e^{\zeta\omega_n T}\left(-2+\left(e^{-\zeta\omega_n T}\right)^n\left(\left(e^{-j\Psi}\right)^n+\left(e^{j\Psi}\right)^n\right)\right) \\ -j\left(e^{-\zeta\omega_n T}\right)^n\left(-1+e^{2\zeta\omega_n T}\right)\left(\left(e^{-j\Psi}\right)^n-\left(e^{j\Psi}\right)^n\right) \\ Csch[\Psi]\end{array}\right)$ $\frac{e^{\zeta\omega_n T}T^2\Omega\,u(n-2)}{4\left(1+e^{2\zeta\omega_n T}-2e^{\zeta\omega_n T}Cos[\Psi]\right)}$ $\zeta<1, \quad \Psi=\omega_n T\sqrt{1-\zeta^2}$ |

Figure 10.7 Second Order Loop Responses for $\zeta < 1$

Figure 10.8 shows the second order step responses. The loop responses are actually discrete "lollipops" as in Figure 10.4, but it becomes difficult to plot multiple discrete responses on the same graph. For this reason, we plot Figures 10.8 - 10.9 with continuous lines, although it is understood that only discrete signal points exist at integer values of n.

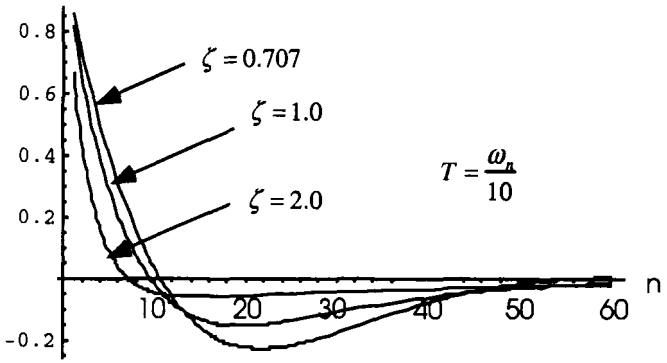


Figure 10.8 Second Order Loop Phase Step Responses

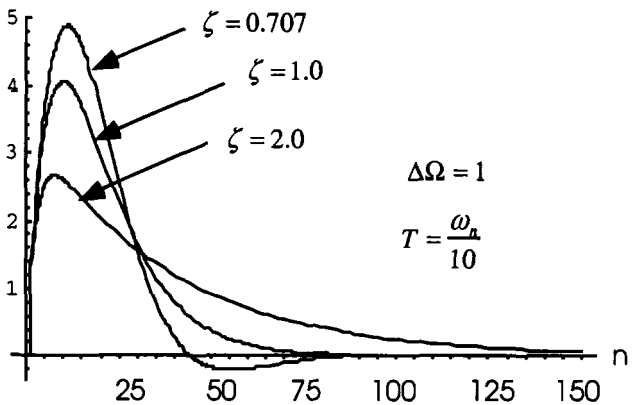


Figure 10.9 Second Order Loop Frequency Step Responses

The response of the second order loop to the phase and frequency modulation can be obtained by evaluating Equation 10-6 with the phase and frequency modulation waveforms shown in Figure 10.1. Typically, we are more interested in the frequency response of these waveforms instead of the time domain response. By substituting $z = e^{jwT}$ into the expression for the error response, $H_e(z)$, we obtain

$$\phi_{Phase}\left(e^{j\omega T}\right) = \frac{e^{j\omega T}\left(e^{j\omega T}-1\right)^2 \Delta\theta Sin[\omega_m T]}{\left(\left(e^{j\omega T}-\alpha\right)^2+\beta^2\right)\left(1+e^{j2\omega T}-2e^{j2\omega T}Cos[\omega_m T]\right)} \qquad 10\text{-}7$$

$$\phi_{Freq}\left(e^{j\omega T}\right)=\frac{e^{j\omega T}\left(e^{j\omega T}-1\right)^2\Delta\omega\left(e^{j\omega T}-Cos[\omega_m T]\right)}{\left(\left(e^{j\omega T}-\alpha\right)^2+\beta^2\right)\omega_m\left(1+e^{j2\omega T}-2e^{j2\omega T}Cos[\omega_m T]\right)} \qquad 10\text{-}8$$

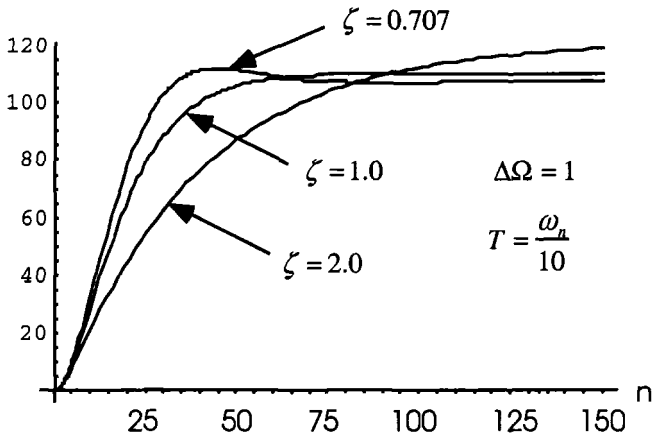


Figure 10.10 Second Order Frequency Ramp Responses

## 10.2. Nonlinear Analysis

The nonlinear operation of a second order digital phase-locked loop is difficult to analyze, requiring two dimensional Markov processes and four dimensional Fourier series [2]. Fortunately, the analysis of a first order loop is much easier, and it allows insight to the operation of higher order loops. Figure 10.11 shows a block diagram of the first order loop.

The block diagram of Figure 10.11 includes an implicit sine function. The down-sampled signal represents the sine of the differences between the signal phase and the phase-locked loop's output phase, and this is represented by the nonlinear sine function in Figure 10.11. (See Equation 9-8.) Following the approach of McCain [4], Figure 10.11 includes a gain $G_p$ for the processor which is common in modem applications.

At first glance, it is appealing to use the general transfer functions $H_e(z)$ and $H_c(z)$ to analyze the loop, but these are linearized representations of the loop and do not include the nonlinear sine function. Instead, we return to the fundamental time domain equations of the phase-locked loop. Our approach

follows that of Chie [2] and Weinberg [3] which considers the non-uniform sampling phase-locked loops of Chapter 9. The approach however, is extensible to digital phase-locked loops which utilize a mixer to remove the carrier and offset frequencies.

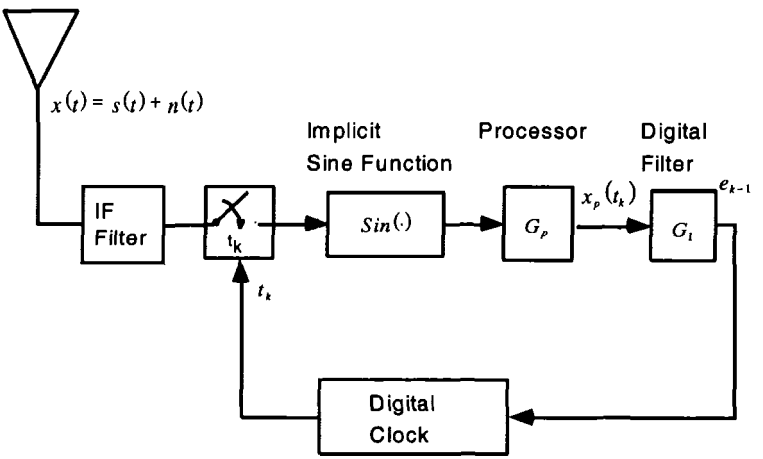


Figure 10.11 First Order Digital Phase-Locked Loop

The sampled input to the phase-locked loop is of the form

$$x(t_k) = \sqrt{2P}\,Sin[2\pi f_0 t_k + \theta_k] + n_k \qquad 10\text{-}9$$

To proceed further, we must specify the input, $\theta(t)$, or its discrete equivalent, $\theta_k$. Weinberg [3] considers both phase and frequency step inputs for $\theta_k$. However in this text, we will consider only the frequency step because it is the most stressful input that the first order loop can track. For such an input, $\theta(t) = 2\pi f_s t + \theta_0$, or $\theta_k = 2\pi f_s t_k + \theta_0$. Note that we use the term, $f_s$, to represent the step frequency input. This is not the same as the sampling frequency, $F_s$, for a digital PLL or filter. Substituting this $\theta_k$ into Equation 10-9 yields

$$x(t_k) = \sqrt{2P}\,Sin[2\pi (f_0 + f_s) t_k + \theta_0] + n_k \qquad 10\text{-}10$$

In Chapter 9, the non-uniform sampling time, $t_k$, for the loop was derived as $t_k = kT_* - \sum_{i=1}^{k} e_{k-1}$. Similar to the previous development, the nominal sampling interval, $T_*$, is selected such that $T_* = \frac{N}{f_0 + f_s}$. This selection removes the carrier and offset frequencies from the actual input signal, leaving only

$$x(t_k) = \sqrt{2P}\,Sin\left[\theta_0 - 2\pi(f_0 + f_s)\sum_{i=1}^{k} e_{k-1}\right] + n_k \qquad 10\text{-}11$$

The argument of the sine function in Equation 10-11 represents the phase error, $\varphi_k = \theta_0 - 2\pi(f_0 + f_s)\sum_{i=1}^{k} e_{k-1}$. This allows the loop's sampled input to be written as $x(t_k) = \sqrt{2P}\,Sin[\varphi_k] + n_k$. Repeating the differencing operations of Chapter 9 and using this representation of $\varphi_k$, we subtract $\varphi_k$ from $\varphi_{k+1}$ to obtain

$$\varphi_{k+1} - \varphi_k = 2\pi(f_0 + f_s)e_k \qquad 10\text{-}12$$

The error term, $e_k$, is obtained after signal processing by the processor and digital loop filter in Figure 10.3 In other words, $e_k$ is obtained after successive operations of the processor and loop filter on the sampled and down-converted $x(t_k)$. For the first order loop, the filter is the scalar $G_1$, which allows $e_k$ to be expressed as

$$e_k = \sqrt{2P}G_p G_1\left(Sin(\phi_k) + \frac{n_k}{\sqrt{2P}}\right) \qquad 10\text{-}13$$

Substitution of the phase error represented by Equation 10-13 into Equation 10-12 allows the complete nonlinear time domain representation of the first order phase-locked loop to be written as

$$\phi_{k+1} - \phi_k = (\theta_{k+1} - \theta_k) - 2\pi(f_0 + f_s)\sqrt{2P}G_p G_1\left(Sin(\phi_k) + \frac{n_k}{\sqrt{2P}}\right) \quad 10\text{-}14$$

However, for the selected input, $\theta_k = 2\pi f_s t_k + \theta_0$. This allows the $\theta_{k+1} - \theta_k$ term in Equation 10-11 to be simplified to $2\pi f_s T_*$. This term represents the phase offset of the first order loop when tracking a frequency step. (Note that the first order frequency step response in Figure 10.4 does not have a steady state of zero.) The complete time domain equation for the loop is

$$\phi_{k+1} - \phi_k = 2\pi f_s T_* - 2\pi(f_0 + f_s)\sqrt{2P}G_p G_1\left(Sin(\phi_k) + \frac{n_k}{\sqrt{2P}}\right) \quad 10\text{-}15$$

This is further simplified with Chie's notation [2],

$$\phi_{k+1} - \phi_k = -K_1 Sin(\phi_k) - K_n n_k + \Lambda_0 \quad 10\text{-}16$$

where

$$K_1 = 2\pi(f_0 + f_s)\sqrt{2P}G_p G_1$$
$$K_n = \frac{K_1}{\sqrt{2P}} \quad 10\text{-}17$$
$$\Lambda_0 = 2\pi f_s T_*$$

---

## *Example 10.1*

Derive the discrete time equations for an analog digital phase-locked loop.

Figure 10.12 shows a representative block diagram of a first order analog digital phase-locked loop. An analog signal is received by the phase-locked loop, with $\theta(t)$ representing the phase information to be tracked by the loop. The input signal is sampled with a first order sampler, and then demodulated by the mixer (multiplier), providing phase-only information to the loop. In a sense, this is more representative of a task required of a second order loop,

because a first order loop could be significantly stressed by the carrier offset frequency, $f_0$. However, if the first order loop's NCO has an offset frequency equivalent to the carrier, then the resulting loop performance will be as if the carrier was not present.

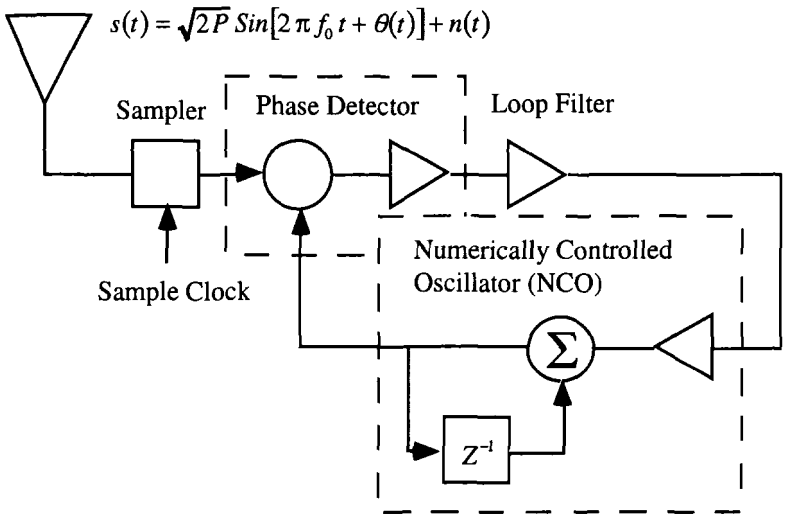


Figure 10.12 Block Diagram of First Order Analog/Digital PLL

By making some assumptions about the elements of Figure 10.12, we can draw the simplified model shown in Figure 10.13. For example, we assume the phase detector and NCO frequency offset remove the carrier's offset frequency, $f_0$, and any double frequency terms resulting from the multiplication is lowpass filtered so that it does not enter the loop. The nonlinearity of the phase detector is represented by the $\mathbf{Sin}(\cdot)$ element in Figure 10.13.

As with the analog loops of Chapter 2, the amplitude of the received signal, $\sqrt{2P}$ is moved into the feedback loop. This requires us to modify the noise component, $n_k$, to account for this additional loop gain. $K_d$ and $K_o$ are the scalar gains for the phase detector and NCO, respectively. The first order loop gain is represented by. $K_f$

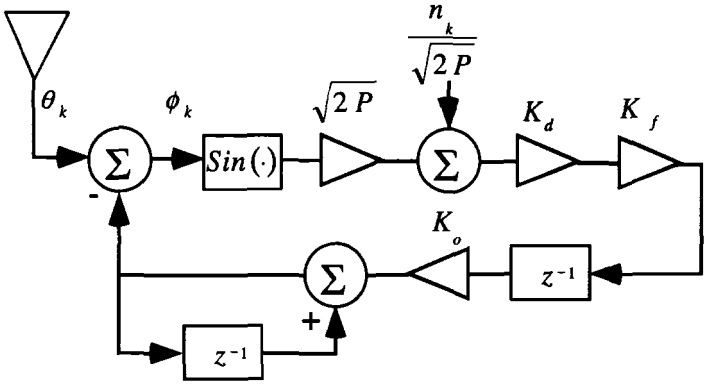


Figure 10.13 Simplified First Order Block Diagram

In Chapter 2, we represented the output of the VCO as $\theta_o$, but we have changed the symbol representation in Figure 10.13 because of the subscript, k, used to denote the time sample. The output of the NCO is $\psi_k$, which is used to obtain the phase difference, $\phi_k$. This can be written as

$$\phi_k = \theta_k - \psi_k \qquad 10\text{-}18$$

From Equation 10-18, we can also write

$$\phi_k - \phi_{k-1} = \theta_k - \theta_{k-1} - ( \psi_k - \psi_{k-1} ) \qquad 10\text{-}19$$

The NCO output, $\psi_k$, can be computed by cascading the gains and transfer functions following the input loop summing element.

$$\psi_k = \sqrt{2P} K_d K_f K_o Sin[\phi_k ] \frac{z^{-1}}{1-z^{-1}} + K_d K_f K_o n_k \frac{z^{-1}}{1-z^{-1}} \qquad 10\text{-}20$$

This can be rewritten to obtain

$$\psi_k - \psi_{k-1} = \sqrt{2P} K_d K_f K_o Sin[\phi_k ] + K_d K_f K_o n_k \qquad 10\text{-}21$$

Substituting Equation 10-21 into Equation 10-19, and using Chie's notation [2],

$$\phi_k - \phi_{k-1} = \theta_k - \theta_{k-1} - K_1 Sin[\phi_k \quad] + K_n n_k \qquad 10\text{-}22$$

where

$$K_1 = \sqrt{2P} K_d K_f K_o$$
$$K_n = \frac{K_1}{\sqrt{2P}} \qquad 10\text{-}23$$

## 10.3. Phase Plane Analysis

Equation 10-16 can be used to visualize the acquisition process if we rewrite it as $\phi_{k+1} = \phi_k - K_1 Sin(\phi_k) - K_n \frac{n_k}{\sqrt{2P}} + \Lambda_0$. Suppose that the loop is operating with no noise, $n_k \equiv 0$, and the frequency offset, $\Lambda_0 \equiv 0$. Under these conditions, a simple graph can be composed of the phase acquisition process [15]. Starting at some initial phase, $\phi_0$, the phase error on the next sampling interval, $\phi_1$ is computed by recursively applying Equation 10-13. As an example, let $K_1 = 0.1$ and $\phi_0 \equiv 2.94524$. The first few recursions of Equation 10-16 are

$$\begin{aligned}
&\phi_{k+1} = \phi_k - 0.1 Sin(\phi_k) \\
&\phi_0 \equiv 2.94524 \\
&\phi_1 = 2.94524 - 0.1 Sin(2.94524) = 2.92573 \qquad 10\text{-}24 \\
&\phi_2 = 2.92573 - 0.1 Sin(2.92573) = 2.90432 \\
&\vdots
\end{aligned}$$

Figure 10.14 shows this example of phase acquisition, with the resulting phase error for every time step. Note that the phase error is monotonically decreasing for every time step of the digital phase-locked loop.

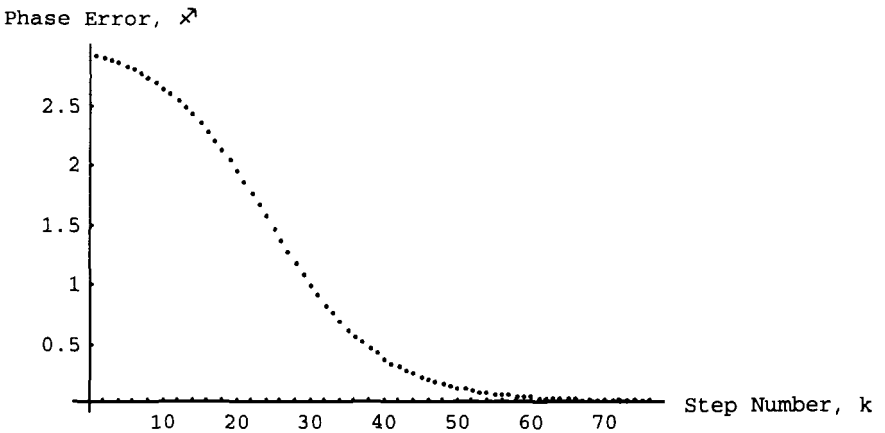


Figure 10.14 Phase Error Steps During Acquisition

Figure 10.15 shows the example acquisition trajectory, beginning with the initial phase error of $\phi = 15/16\,\pi$, and converging to the steady state phase error of $\phi_{ss} = 0$. (Recall that $\phi_{ss}$ is a function of $\Lambda_0$, described by Equation 10-16. If the offset frequency, $f_s$, is not zero, then $\phi_{ss} \neq 0$.) Figure 10.15 is a phase plane trajectory similar to Figure 4.2. Figure 10.15 differs from Figure 10.14 because the phase error is graphed as coordinates $(\phi_{K+1}, \phi_k)$, that represent the acquisition trajectory for the loop.

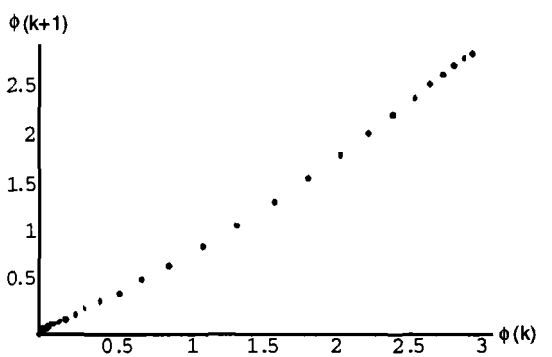


Figure 10.15 Phase Plane Trajectory of Digital Phase-Locked Loop

Examination of Equation 10-16 shows that the first order loop cannot track a signal if the offset frequency, $\Lambda_0$, is greater than $K_1 Sin(\phi_k)$. In steady state, $\phi_{k+1} = \phi_k$, and the maximum value for $Sin(\phi_k)$ is unity. The maximum offset frequency for the first order loop can then be written as

$$f_s < \frac{K_1}{2\pi T_*} \qquad 10\text{-}25$$

## 10.4. Phase Error Variance

The variance, $\sigma_\phi^2$, of the phase error is important in many phase-locked loop applications. By taking the expected value of Equation 10-16, we obtain

$$E\{\phi_{k+1}\} - E\{\phi_k\} = -K_1 E\{Sin(\phi_k)\} + \Lambda_0 \qquad 10\text{-}26$$

Taking the limit of Equation 10-26 as $k \to \infty$, we have a steady state phase error, $\varphi_{ss}$ (which is a function of the offset frequency, $\Lambda_0$). Since the $E\{\phi_{k+1}\} = E\{\phi_k\}$ as $k \to \infty$, Equation 10-20 becomes

$$E\{Sin(\phi_k)\} = \Lambda_0 / K_1 \qquad 10\text{-}27$$

As was discussed previously, the term $\Lambda_0 / K_1$ represents the first order loop's stress due to the frequency step. Following the approach of Chie [2], we square Equation 10-16, take the limits as $k \to \infty$, and perform expectations as done for Equation 10-26, to obtain

$$K_n^2 \sigma_\varphi^2 = 2K_1 E\{\varphi Sin(\varphi)\} - K_1^2 E\{Sin(\varphi)^2\} - 2\Lambda_0 E\{\varphi\} + \Lambda_0^2 \qquad 10\text{-}28$$

When the loop is tracking (otherwise the phase error variance is meaningless), the phase error is near $\varphi_{ss}$, $Sin(\varphi)$ can be approximated by a Taylor Series about the steady state phase error, $\varphi_{ss}$. Substitution of $\varphi_{ss}$ and Equation 10-20 into Equation 10-28, yields

$$\sigma_{\varphi}^2 \approx \frac{K_n^2 \sigma_n^2}{K_1 Cos[\varphi_{ss}](2 - K_1 Cos[\varphi_{ss}])} \qquad 10\text{-}29$$

With $\varphi_{ss} = 0$ and $\Lambda_0 = 0$, the linear approximation for the phase variance is identical to the analog phase-locked loop,

$$\sigma_{\varphi}^2 \approx 1/\rho \qquad 10\text{-}30$$

where the linearized signal-to-noise in the loop is defined as

$$\rho \equiv \frac{2 - K_1}{K_1} \frac{2P}{\sigma_n^2} \qquad 10\text{-}31$$

In other words, the phase error variance is approximately the inverse of the loop's signal-to-noise ratio. The first order approximation is not nearly as accurate as the second order approximation derived by Chie [2], which approximates $Sin[\phi_k] \approx \phi_{ss} + (\phi_k - \phi_{ss})Cos[\phi_{ss}]$. (Weinberg [3] uses $Sin[\phi_k] \approx \phi_k + \phi_k{}^3/3!$ which also results in a reasonable approximation.) Because of the second order nature, there are two possible roots,

$$\sigma_{\varphi}^2 \approx \begin{cases} \dfrac{2P(K_1 - 2) - \sqrt{P\left(4(K_1 - 2)^2 P + 8(K_1 - 1)K_1 \sigma_n^2\right)}}{4P(K_1 - 1)} \\ \dfrac{2P(K_1 - 2) + \sqrt{P\left(4(K_1 - 2)^2 P + 8(K_1 - 1)K_1 \sigma_n^2\right)}}{4P(K_1 - 1)} \end{cases} \qquad 10\text{-}32$$

The most rigorous phase error variance analysis uses the Chapman Kolmogorov equation, $f(x_1|x_3) = \int_{-\infty}^{\infty} f(x_1|x_2, x_3) f(x_2|x_3) dx_2$, which allows a probability density function to be a function of other probability density functions [4]. For the first order loop, the Chapman Kolmogorov equation can be written as [2,3]

$$p_{k+1}(\varphi|\varphi_0) = \int_{-\infty}^{\infty} q_k(\varphi|u)\, p_k(u|\varphi_0)\, du \qquad 10\text{-}33$$

where $q_k(\varphi|u)$ is the transition probability density function. $p_k(u|\varphi_0)$ is the conditional probability density function of $u$ given $\varphi_0$. Note the recursive nature of this probability density function. In order to have the probability density function at time k+1, we need to have the density function at time k to include within the integral of Equation 10-21. The variable $\varphi \in \{-\infty, \infty\}$ in Equation 10-27, which presents difficulties. Instead, we consider the variable $\phi = \varphi \bmod 2\pi$, as we did for the first and second order approximations.

Following the development of Weinberg [3], the transition probability density function, $q_k(\varphi|u)$, has a Gaussian distribution. The mean value and variance of $\varphi_k|z$ are

$$\begin{aligned} E\{\varphi_{k+1}|z\} &= z - K_1 Sin[z] + \Lambda_0 \\ \sigma^2_{\varphi_{k+1}|z} &= K_n^2 \sigma_n^2 \end{aligned} \qquad 10\text{-}34$$

Because the two moments are sufficient to specify the Gaussian probability density functions, we can write $q_k(\varphi|u)$ by inspection

$$q_k(\varphi|z) = \frac{1}{\sqrt{2\pi\sigma^2_{\varphi|z}}} Exp\left[ -\frac{(\varphi - u + K_1 Sin[z] - \Lambda_0)^2}{2\sigma^2_{\varphi|z}} \right] \qquad 10\text{-}35$$

Equation 10-35 can be used to provide the modulo $2\pi$ phase error, $\phi$, by the infinite sum,

$$q_k(\phi|u) = \sum_{n=-\infty}^{\infty} q_k(\varphi + 2n\pi|z) \qquad 10\text{-}36$$

The final probability density function is written as an integral equation,

$$p(\phi) = \int_{-\pi}^{\pi} q(\phi|z)p(z)dz \qquad 10\text{-}37$$

Equation 10-37 can be solved through numerical techniques. As discussed in [2-3], one method is to solve the recursive equation

$$p_{k+1}(\phi_i) = \sum_{j=1}^{N} q(\phi_i|z_j)p_k(z_j) \quad i = 1,2,\ldots,N \qquad 10\text{-}38$$

where the $\phi_i$ and $z_i$ are selected uniformly on the interval $[-\pi,\pi]$. The recursive algorithm is to begin with $p_0(\phi_i) = \phi_i$, for each bin in the interval $[-\pi,\pi]$. Using Equation 10-38, the transition probability can be computed for each conditional $z_j$. All N $p_{k+1}(\phi_i)$ values are then computed to be used recursively for the k+2 values. The recursion stops when the change from $p_{k+1}$ and $p_k$ is less than some small epsilon, $\varepsilon$. The infinite sum in Equation 10-36 is troublesome, but it converges quickly. Weinberg [3] notes that summations for $-3 \le n \le 3$ provide accurate representations of the infinite summation.

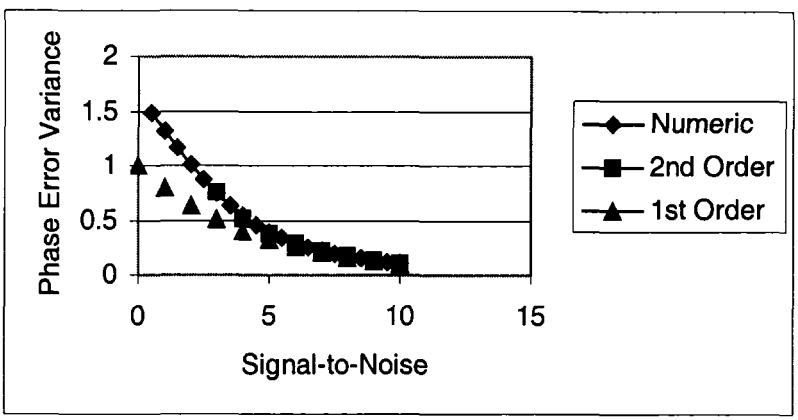


Figure 10.16 Comparison of Phase Error Variance Computations

Figure 10.16 shows the different phase error approximations for Equations 10-30, 10-32, and 10-38 for the first order digital phase-locked loop. For signal-to-noise ratios less than 8 dB, the linear approximation has significant error. However, the second order approximation, Equation 10-32,

is adequate for signal-to-noise ratios down to almost 4 dB. The second order approximation is shown only to 3 dB for this particular graph because Equation 10-32 develops an imaginary component for lower signal-to-noise ratios. The signal-to-noise ratio of the loop was defined in Equation 10-31.

Because of the accuracy, the Chapman Kolmogorov is of most interest. Figure 10.17 shows the phase error variance of the first order loop with different values of $K_1$. The recursive Chapman Kolmogorov Equation 10-38 was used exclusively to compute the values of Figure 10.17.

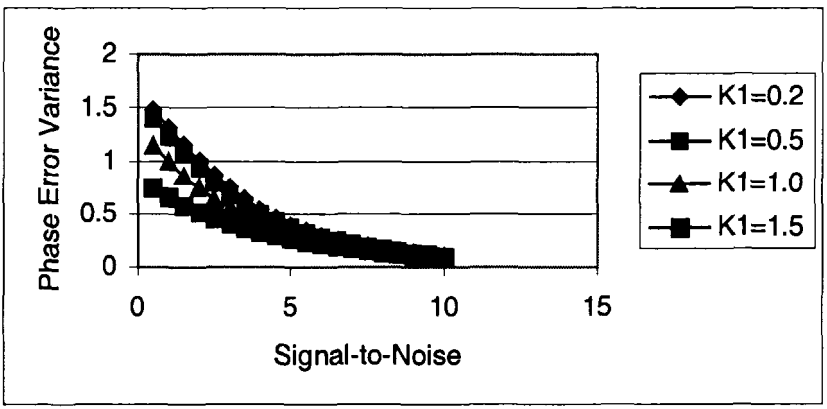


Figure 10.17 Phase Error Variances for the First Order Digital Phase-locked Loop

## 10.5. Probability of Acquisition

Weinberg [4] defines the threshold for the first order loop as the signal-to-noise ratio at which the linear approximation, Equation 10-30 has excessive error. From Figure 10.16, the threshold is in the vicinity of $\rho = 6$ dB. This is not the signal-to-noise required for initial acquisition of the signal. Charles and Lindsey explored this for analog phase-locked loops [10].

To analyze the probability of acquisition for a first order loop, we again use the Chapman Kolmogorov expression for the phase error variance, Equation 10-37. However, we note that if the loop's error, $|\phi_k| < |\phi_l| + \varepsilon$

where $\phi_l$ is the steady state tracking error ( $\Lambda_0$ might be something other than zero), then the acquisition process is complete [2-3].

In particular we define the Chapman Kolmogorov equation for acquisition as

$$p_{A,k+1}(\phi) = \begin{cases} 0, & |\phi_k| < |\phi_l| + \varepsilon \\ p(\phi) = \int_{-\pi}^{\pi} q(\phi|z)p(z)dz, & \text{otherwise} \end{cases} \qquad 10\text{-}39$$

This is equivalent to the first passage time problem [5]. Effectively we have placed a well in the probability density function as shown in Figure 10.18. Once the condition $|\phi_k| < |\phi_l| + \varepsilon$ occurs, $\phi_k$ is trapped and cannot escape.

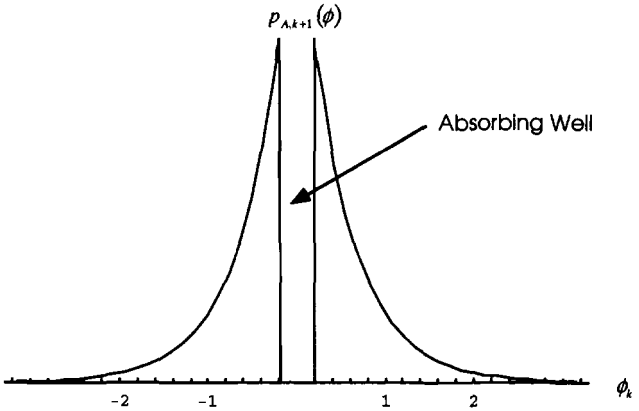


Figure 10.18 Acquisition Probability Density Function With Absorbing Well [2]

The probability of acquisition at time $t = k+1$ is [2]

$$P_{acq}(k+1) = \int_{-\pi}^{\pi} [p_{A,k}(\phi) - p_{A,k+1}(\phi)] d\phi \qquad 10\text{-}40$$

An initial uniform distribution can be assumed for $\phi$ This allows Equation 10-40 to be initialized with

$p_{A,0}(\phi) = \begin{cases} 0, |\phi_k| < |\phi_l| + \varepsilon \\ \dfrac{1}{2\pi}, \text{otherwise} \end{cases}$. By inspection, the initial probability of acquisition is $P_{acq}(1) = \varepsilon/\pi$. Equation 10-34 can be solved numerically, similar to the method used for Equation 10-38. A numeric solution for Equation 10-40 is graphed in Figure 10.19. Note the stress placed by a non-zero offset frequency, $\Lambda_0$, on a first order loop affects the probability of acquisition.

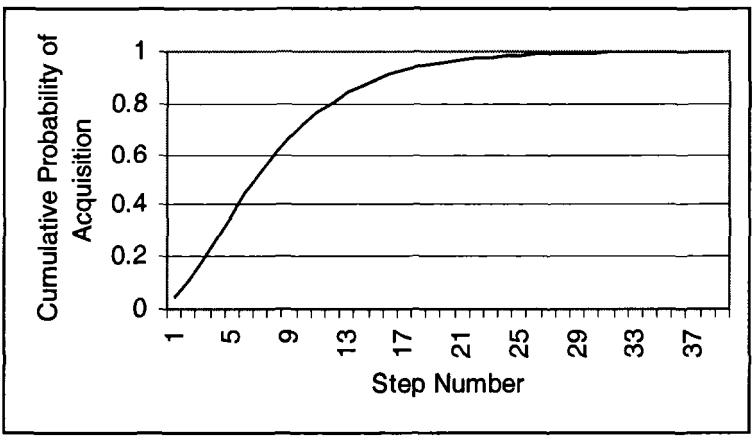


Figure 10.19 Cumulative Probability of Acquisition for First Order Loop (K1=0.5, $\rho = 6dB$)

The expected number of states to acquisition is

$$N_{acq} = \sum_{k=1}^{\infty} k P_{acq}(k+1) \qquad 10\text{-}41$$

## 10.6. Probability of Cycle Slip

In modem applications, the mean time to cycle slip is of extreme importance. Whenever the phase-locked loop loses lock in a modem, it can mean that hundreds of bits of data will be lost before the modem can regain synchronization. The probability of cycle slip is computed in a method similar to the probability of acquisition. We assume the phase-locked loop is

tracking the signal, such that $\phi_k = \phi_{ss}$ as $k \to \infty$. When a cycle slip occurs, the instantaneous phase jumps by $\pm\pi$. The probability of such an event can be computed from the transition probability function previously described.

In order to capture the cycle slip event, we place absorbing wells in the probability density function so that once a cycle slip event occurs, the phase $\phi_k$ cannot return to the normal operating range. In other words, we define the probability density function as [4]

$$p_{slip,k+1}(\phi) = \left\{ \begin{array}{c} 0,\ \phi_{ss} - 2\pi < \phi_k \\ 0,\ \phi_{ss} + 2\pi > \phi_k \\ p(\phi) = \int_{-\pi}^{\pi} q(\phi|z)p(z)dz, \text{otherwise} \end{array} \right\} \qquad 10\text{-}42$$

The probability that k cycles are required for cycle slip is

$$\Pr\{\text{k cycles for cycle slip}\} = \int_{\phi_{ss}-2\pi}^{\phi_{ss}+2\pi} p_{slip,k-1}(\phi) - p_{slip,k}(\phi)d\phi \qquad 10\text{-}43$$

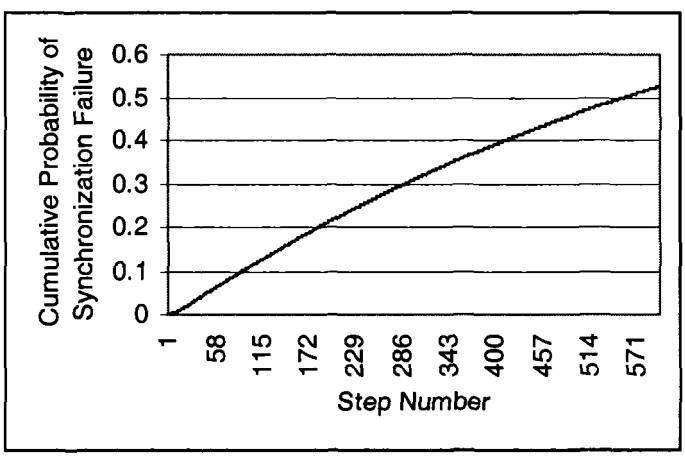


Figure 10.20 Cumulative Property of Synchronization Failure for a First Order Loop ( K1=0.5, $\rho = 3dB$ )

Figure 10.20 shows the cumulative probability of cycle slip obtained from numerically evaluating Equation 10-43. It should be noted that this

numerical evaluation requires a fine granularity of phase steps to obtain accurate results. The mean time to cycle slip is obtained by taking the expected value of the probability of cycle slip [4]

$$\sum_{k=1}^{\infty} \mathrm{k\ Pr}\{\mathrm{k\ cycles\ for\ cycle\ slip}\} \qquad 10\text{-}44$$

## 10.7. Nonlinear Analysis of Second Order Loops

The second order phase-locked loop has a loop filter of the form $F(z) = G_1 + \frac{G_2}{1 - z^{-1}}$. The general time domain representation is

$$\begin{aligned}&\phi_k - 2\phi_{k-1} + \phi_{k-2} = \theta_k - 2\theta_{k-1} + \theta_{k-2} - 2\pi f_0 G_1 n_{k-1} + 2\pi f_0 G_1 n_{k-2} \\ &- 2\pi f_0 \sqrt{2P} G_2 n_{k-1} - 2\pi f_0 \sqrt{2P} G_1 Sin[\phi_{k-1}] + 2\pi f_0 \sqrt{2P} G_1 Sin[\phi_{k-2}] \\ &- 2\pi f_0 \sqrt{2P} G_2 Sin[\phi_{k-1}]\end{aligned} \qquad 10\text{-}45$$

The first three terms on the right-hand side of Equation 10-45 are interesting, $\theta_k - 2\theta_{k-1} + \theta_{k-2}$. If $\theta_k$ is a constant, then these three terms cancel each other out, which is the expected response for a second order phase-locked loop. For the frequency step input, Equation 10-45 becomes [2]

$$\phi_{k+1} - 2\phi_k + \phi_{k-1} = K_1 Sin(\phi_{k-1}) + K_n n_{k-1} - r\{K_1 Sin(\phi_k) + K_n n_k\} \qquad 10\text{-}46$$

where

$$K_i = \omega G_i \sqrt{2P_c}, i \in \{1,2\}$$

$$K_n = \omega G_1 = \frac{K_1}{\sqrt{2P_c}} \qquad 10\text{-}47a$$

$$\omega = 2\pi f_0 + \Omega_0$$

$$r \equiv 1 + \frac{G_2}{G_1} = 1 + \frac{K_2}{K_1} \qquad 10\text{-}47b$$

Equation 10-46 is non-Markovian, but an auxiliary variable can be introduced to obtain a two-dimensional Markov process [3]. Once that is accomplished, analysis similar to the first order loop can produce expressions for probability of acquisition, mean time to acquisition, etc.. Unfortunately the expressions are unwieldy and not particularly insightful. As with the first order phase-locked loop, the linear approximation for the phase variance phase error is

$$\sigma_\varphi^2 = 1/\rho \qquad 10\text{-}48$$

where $\rho = \dfrac{2P(r+1)}{2(4-K_1(r+1)-r-1)}$ 10-49

The loop bandwidth from the linear approximation is [2]

$$W_L = \frac{2}{\frac{4}{r+1} - K_1} - 1 \qquad 10\text{-}50$$

## *Example 10.2*

In Example 7.3, we designed a second order phase-locked loop with $T_s = 50\text{Hertz}$, $\omega_n = 3\text{Hertz}$, and $\zeta = 0.707$. The complete block diagram is duplicated in Figure 10.21 for convenience. Compute the discrete time nonlinear equations for the loop and perform a simulation to estimate the phase error variance.

Figure 10.21 includes the implicit *Sin*[·] function which results from the mixer at the front of the phase-locked loop in Example 7.3. The effective noise source is shown as an additive process into the loop with $n_k$. Because the loop filter includes the gain, $\sqrt{2P}$, of the input signal, the additive noise term must be compensated as $\dfrac{n_k}{\sqrt{2P}}$. To ease the development of nonlinear difference equations, the block diagram is simplified with Figure 10.22.

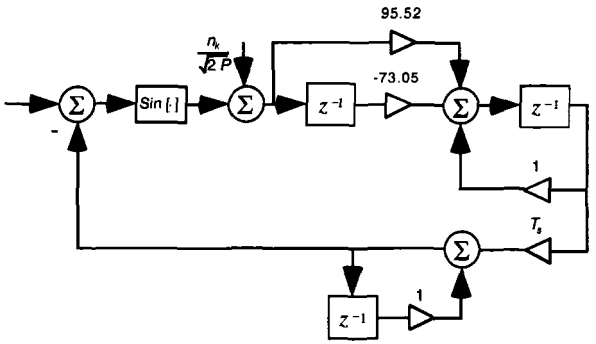


Figure 10.21 Block Diagram of Second Order Phase-locked Loop

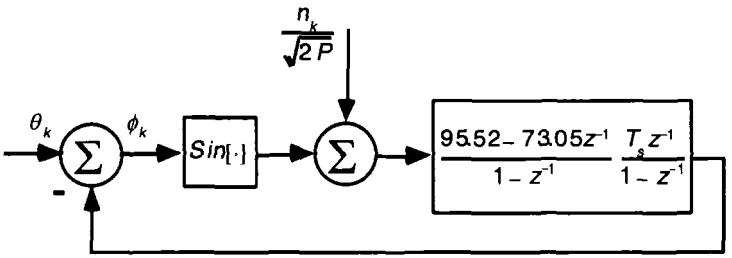


Figure 10.22 Simplified Block Diagram of Second Order Loop

To begin the development of the difference equations, the $z^{-1}$ term in the numerator of the transfer function is critical. As discussed previously, the digital loop cannot have an input dependent upon the output during the same sampling instant. The presence of this $z^{-1}$ term allows us to write by inspection,

$$\phi_k = \theta_k - \left( Sin[\phi_{k-1}] + \frac{n_{k-1}}{\sqrt{2P}} \right) \left\{ \frac{95.52 - 73.05z^{-1}}{1-z^{-1}} \frac{T_s}{1-z^{-1}} \right\} \qquad 10\text{-}51$$

Simplifying Equation 10-51, we obtain the desired difference equation,

$$\phi_k = 2\phi_{k-1} - \phi_{k-2} + \theta_k - 2\theta_{k-1} + \theta_{k-2} - 95.52T_s Sin[\phi_{k-1}]$$
$$+ 73.05T_s Sin[\phi_{k-2}] - 95.52T_s \frac{n_{k-1}}{\sqrt{2P}} + 73.05T_s \frac{n_{k-2}}{\sqrt{2P}} \qquad 10\text{-}52$$

Equation 10-52 can now be programmed or entered into a spreadsheet. Before presenting the phase error variance plot, we digress to discuss the generation of the noise samples, $n_k$.

Almost any Gaussian noise generator requires a uniform random number generator to produce random variables that are then processed to obtain the Gaussian density function. A relatively simple uniform generator that has been tested for multiple moments is the Whichman-Hill algorithm [7]. Many random number generators have good correlation qualities between $x_k x_{k-1}$, but can exhibit large correlations between other samples such as $x_k x_{k-2}$ [8]. For this reason, it is important to understand the quality of the uniform random number generator before using it as an input to a Gaussian number generator.

The 32-bit version of the Whichman-Hill algorithm is

$$\begin{aligned} iX_k &= Mod[\ 171 \times iX_{k-1}, 30269\ ] \\ iY_k &= Mod[\ 172 \times iY_{k-1}, 30307\ ] \\ iZ_k &= Mod[\ 170 \times iZ_{k-1}, 30323\ ] \\ \text{random}_k &= FMod\left\{\frac{iX_k}{30269.0} + \frac{iY_k}{30307.0} + \frac{iZ_k}{30323.0}, 1.0\right\} \end{aligned} \qquad 10\text{-}53$$

The algorithm begins with arbitrary seed values for $\{iX_{-1}, iY_{-1}, iZ_{-1}\}$ Using the appropriate modulus function for the programming language, (for C, Mod is simply the % operator), and floating point modulation function (in C, FMod is modf), a uniform random generator is obtained. The Whichman-Hill algorithm generates a random number uniformly distributed between 0.0 and 1.0.

To generate random numbers with a Gaussian distribution, the Box-Muller algorithm is suggested [9].

$$\begin{aligned} X_k &= \sqrt{-2Log[randomA_k]}\,Cos[2\pi randomB_k] \\ Y_k &= \sqrt{-2Log[randomA_k]}\,Sin[2\pi randomB_k] \end{aligned} \qquad 10\text{-}54$$

In Equation 10-54, $randomA_k$ and $randomB_k$ are two uniform random numbers such as could be obtained from the Whichman-Hill algorithm. The

uncorrelated pair of Gaussian numbers generated by Equation 10-54 have a mean of zero and a variance of 1.0. Scaling and translation can provide the desired statistics [5].

The phase-locked loop from Example 7.3 was designed with a specific signal level input. To vary the signal-to-noise in the simulation, the variance of the noise samples will be varied. From Example 7.3, the closed loop transfer function for this phase-locked loop is

$$H_C(z) = \frac{-0.462 + 0.604z}{0.538 - 1.396z + z^2} \qquad 10\text{-}55$$

From Chapter 8, the loop bandwidth is calculated as $\frac{2B_L}{B} = \frac{1}{j2\pi}\oint H_C[z]H_C[z^{-1}]z^{-1}dz$. Applying the residue theorem, we obtain $\frac{2B_L}{B} = 0.572842$

---

## 10.8. Acquisition for Non-Uniform Sampling Phase-Locked Loops

Sarkar and Chattopadhyay [12] performed an analysis on the acquisition properties of the digital phase-locked loop of Figure 10.23. ($K = \sqrt{2P}$) This is a second order non-uniform sampling phase-locked loop discussed in this chapter as well as Chapter 9. Using the notation previously introduced, the recursive loop equation is [12]

$$\phi_{k+1} = 2\pi(\varepsilon - 1) + \phi_k - \varepsilon(K_1 + K_2)Sin(\phi_k) - SUM(k)$$

*where*

$$\varepsilon = \frac{f_s}{f_0},\ K_1 = G_1 2\pi f_0 \sqrt{2P},\ K_2 = G_2 2\pi f_0 \sqrt{2P} \qquad 10\text{-}56$$

$$SUM(k) = \sum_{i=0}^{k-1} Sin(\phi_i)$$

In Equation 10-56, the cumulative value of the loop filter's accumulator is represented by the term, SUM(k). The value of SUM(k) is critical to the loop's acquisition response to a frequency step. In some instances, the loop may not be able to acquire the frequency step with a non-zero initial value of SUM(k). One implementation strategy is to always zero the accumulator prior to re-acquisition such as a burst-mode modem [12].

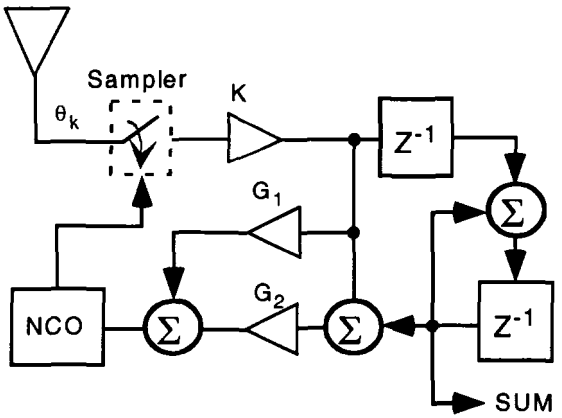


Figure 10.23 Block Diagram of DPLL for Acquisition Analysis [12]

Because the phase-locked loop of Figure 10.23 has a center frequency of $f_0$, the loop has lower and upper frequency acquisition ranges relative to $f_0$. Although earlier literature had reported [13] that the lower frequency acquisition range was unbounded, later literature show definite lower and upper bounds for frequency acquisition [14].

In [12], the authors suggest that a reasonable Frequency Acquisition Range (FAR) is

$$0.5 \le f_s / f_0 \le 1.5 \qquad 10\text{-}57$$

where $f_s$ is the frequency step or shift, as introduced earlier.

Equation 10-57 is only valid for no memory in the loop filter's accumulator. The presence of non-zero values can prevent the loop from acquiring at all.

## 10.9. References

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## 10.10. Problems

10.1 For a transformation of a first order loop prototype, the error response is $H_e(z) = \dfrac{z-1}{z-1+4B_L T_s}$. Compute the error response to a phase step.

10.2 For a transformation of a first order loop prototype, the error response is $H_e(z) = \dfrac{z-1}{z-1+4B_L T_s}$. Compute the error response to a frequency step.

10.3 For a transformation of a first order loop prototype, the error response is $H_e(z) = \dfrac{z-1}{z-1+4B_L T_s}$. Compute the error response to a frequency ramp.

10.4 Compute the noise bandwidth for the first order non-uniform sampling phase-locked loop.

10.5 Compute the noise bandwidth for a second-order non-uniform sampling phase-locked loop. Consider only the case for $\xi = 1$.

10.6 Plot the phase plane trajectory for a first-order non-uniform sampling DPLL with : $K_1 = 1.2$, $\Lambda_0 = 0.25$, $\phi_0 = 0.40$.

10.7 Plot the phase plane trajectory for a first-order non-uniform sampling DPLL with : $K_1 = 0.4$, $\Lambda_0 = 0.05$, $\phi_0 = 0.90$.

10.8 Graph the frequency response of the non-uniform DPLL to phase modulation with: $\zeta = 0.707$, $\omega_n = 30.0$, $T_s = 0.01$, $\Delta\theta = 1$, and $\omega_m = 12.0$.

10.9 Graph the frequency response of the non-uniform DPLL to frequency modulation with: $\zeta = 0.707$, $\omega_n = 30.0$, $T_s = 0.01$, $\Delta\omega = 10.0$, and $\omega_m = 12.0$.

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# 11

# Synchronizers for Digital Communications

Synchronization of digital waveforms is an area of active research. For the latest information, the reader is encouraged to review the latest issues of IEEE Transactions on Communications. Several references exist that can provide a larger theoretical foundation than provided in this chapter [1-5]. Today's demand for wireless services promises to exceed the available frequency spectrum, necessitating more efficient modulation techniques. Waveforms such as Continuous Phase Modulation (CPM) or Trellis Coded Modulation (TCM) provide more efficient spectral usage, but synchronization is significantly more difficult than traditional Phase Shift Keying (PSK) or Frequency Shift Keying (FSK).

In this chapter, we will begin with an explanation of the synchronization problem. Traditional methods of synchronizing BPSK will be presented. Because of the current research in combined modulation and coding, it is inevitable that today's advanced synchronization will soon be inadequate for the new waveforms. Because of this, our primary emphasis is to develop the general principles of synchronization so the reader can apply them to new waveforms as they are developed.

## 11.1. The Synchronization Problem

Figure 11.1 begins the problem definition with the transmitter sending a signal, $\alpha(t_1)e^{j\phi(t_1)}$, and the receiver attempting to remove the information

from the signal after it has passed through the noisy channel. Typically the receiver and transmitter are not geographically co-located, so there is an inherent problem in time synchronization. In some instances a nanosecond of timing ambiguity between timing references $t_1$ and $t_2$ may prevent the receiver from recovering the transmitted information.

Figure 11.1 assumes some form of digital modulation. It is implied that the baseband information has been translated to a higher frequency for transmission through the channel media, whether it is an optical fiber, free-space transmission, or even coaxial cable. The physical transmission media will cause a change in the phase of the signal, $\theta$, (physical distance will also impose a modulo $2\pi$ effect) which the receiver must compensate to demodulate the transmitted information.

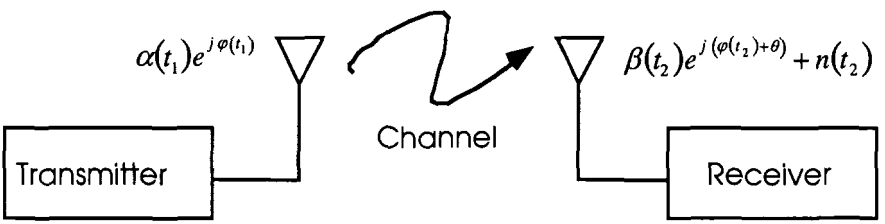


Figure 11.1 Synchronization of Receiver With Transmitter

As can be inferred from Figure 11.1, the synchronization of a receiver is a multi-dimensional problem. A simple modulation format known as Binary Shift Keying (BPSK) [1,31] is shown in Equation 11-1.

$$s(t) = \mathrm{Re}\left\{\sum_{k=-\infty}^{\infty} a_k u(t - kT - \tau) e^{j\theta} e^{j2\pi f_0 (t-\tau)}\right\} \qquad 11\text{-}1$$

where

$a_k \in \{-1,1\}$ , the actual data values
$f_0$ is the modulation (carrier) frequency
$\theta$ is the transmitted phase
$\tau$ is the transmitted timing offset

There may be absolute phase and timing references for a communications network in which the transmitter itself has synchronization ambiguities. (The transmitter must synchronize to the network's epoch.) For

this reason, we assign the phase and timing offsets $\theta$ and $\tau$ to Equation 11-1. The basic principle of BPSK is to change the phase of the modulation frequency by $\pm 180°$, dependent upon the data. To generate the data bit value $a_k$ of Equation 11-1, we map the binary values $\{0,1\} \rightarrow \{-1,1\}$

In order for the receiver to determine the transmitted data bit $a_k$, the receiver must solve for the unknown variables, $f_0$, $\theta$, and $\tau$. Suppose the receiver knew exactly the variables $f_0$ and $\tau$, but had an error of $\pi/4$ for the estimate of $\theta$. In such a situation, the receiver has the signal voltage reduced by $1/\sqrt{2}$, for a loss of 3 dB in signal power.

The receiver's local variable estimates are conventionally denoted $\hat{f}_0$, $\hat{\theta}$, and $\hat{\tau}$. In many applications, the receiver must solve for other parameters as well. (In multi-h CPM, the receiver must solve for superbaud timing[2], or the receiver may need to estimate the channel fading [19].) The data message from the transmitter may have different packet components which must identified before the actual data can be recovered. Usually, these are handled by higher level layers of the Open Systems Interconnection (OSI) hierarchy [3]. In this section, we shall confine our discussion to the synchronization needed for the physical layer of the communication model.

Figure 11.2 shows a block diagram of a digital modem. The input data s(t), is assumed to be baseband analog data that will be sampled by the modem's sample-and-hold. The sample-and-hold's timing is controlled by the timing loop. The timing loop is often a phase-locked loop as will be discussed shortly. A dashed line from the actual data detection shows that sometimes the data decision is used as information for the timing loop, as well as the carrier recovery loop.

The carrier recovery loop is required to stabilize the input frequency and phase so that efficient coherent demodulation can be performed on the resulting data. As with the timing loop, the carrier recovery loop is usually a phase-locked loop although it may be implemented with nonlinearities to remove the effect of data upon the loop.

The data detection filter may be a simple integrate-and-dump, or it may be a sophisticated Viterbi decoder. The Viterbi decoder is preferred for

implementing a maximum likelihood sequence estimator necessary for advanced waveforms. This block diagram does not show the functionality necessary for forward error coding. Figure 11.2 shows the physical layer rather than the link layer which typically incorporates error detection and correction.

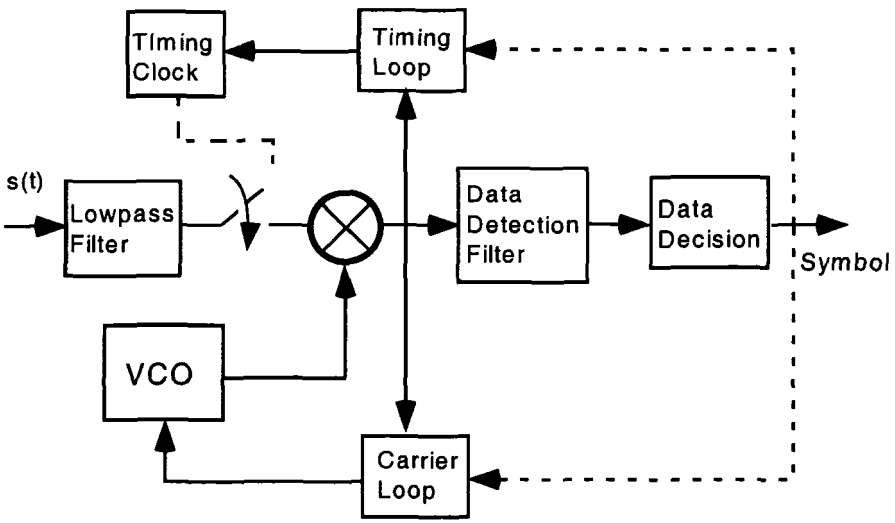


Figure 11.2 Block Diagram of Digital Modem

Because of implementation errors, platform movement, or channel disturbances, the receiver must continually adjust the variables $\hat{f}_0$, $\hat{\theta}$, and $\hat{\tau}$. Because of noise, these estimates are statistical processes. The uncertainty or remaining error in the synchronization variables will cause a degradation in a receiver's performance. Typically the degradation is characterized as a reduction in the effective signal-to-noise ratio of the receiver. Figures 11.3 and 11.4 show the effect of carrier and clock synchronization jitter upon a BPSK receiver.

A first order phase-locked loop is assumed for both the phase and timing synchronizers. As discussed in previous chapters, a phase-locked loop has a noise bandwidth, $B_L$, and an associated signal-to-noise ratio, $\frac{S}{N_0 B_L}$,

within the loop. The noise within the loop generates jitter on the loop output which we have previously designated $\sigma_\theta^2$.

From sample to sample, $\hat{\theta}$ and $\hat{\tau}$ will vary according to their respective statistical properties, $\sigma_{\hat{\theta}}^2$, and $\sigma_{\hat{t}}^2$. The variance of the estimates is a function of the signal-to-noise within the loop. In Figures 11.3 and 11.4, the probability of bit error is computed for different values of $\frac{S}{N_0 B_L}$ within the synchronization loops. A $\frac{S}{N_0 B_L} = \infty$ corresponds to perfect synchronization.

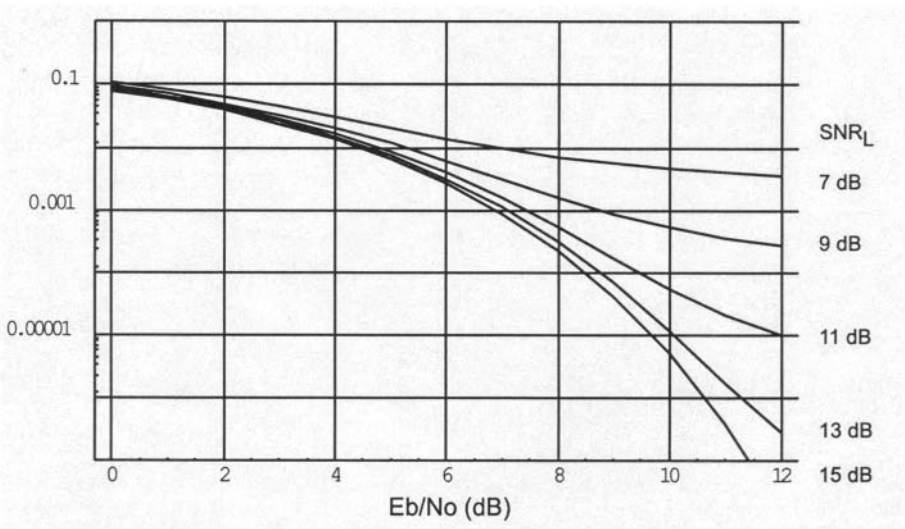


Figure 11.3 BPSK Bit Error Performance With Carrier Phase Synchronization Noise

To compute Figure 11.3, we assumed a first order phase-locked loop with a phase error probability density of the form [4]

$$f_\phi(\phi) = \frac{e^{\alpha Cos[\phi]}}{2\pi I_0[\alpha]}, \quad -\pi \le \phi \le \phi \qquad 11\text{-}2$$

$\alpha$ is the signal - to - noise ratio in the first order phaselocked loop

$I_0$ is the Bessel Function of Order 0

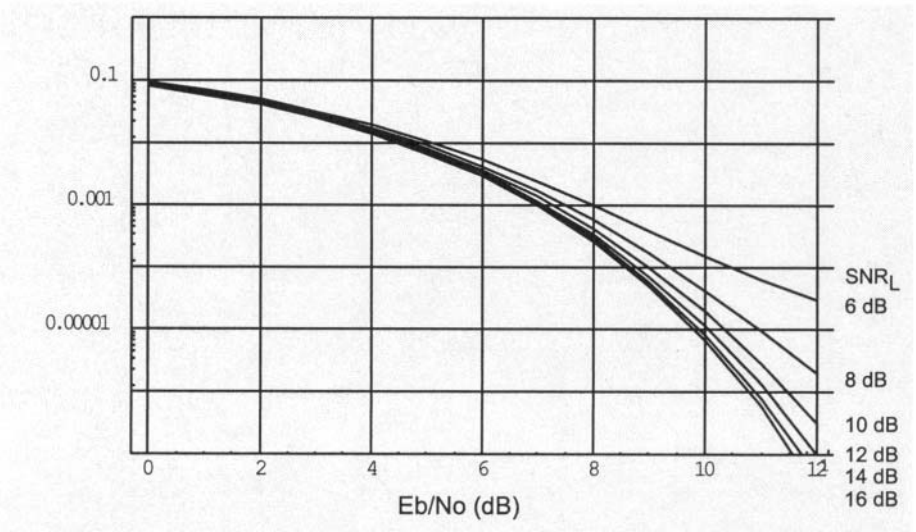


Figure 11.4 BPSK Bit Error Performance With Timing Synchronization Noise

The bit error probability of BPSK with a synchronization phase error, $\phi$, is [1,4]

$$P_E(\rho) = \frac{1}{2} Erfc\left[\sqrt{\rho}\, Cos[\phi]\right] \qquad 11\text{-}3$$

where

$\rho$ is the received $\frac{E_b}{N_0}$ ratio

$\phi$ is the demodulator's phase error

To compute the performance curves in Figure 11.3, we compute the expected value of Equation 11-3, with the probability density function from Equation 11-2.

$$P_{E,\text{Synchronizer Phase}}(\rho) = \int_{-\pi}^{\pi} \frac{1}{2} Erfc\left[\sqrt{\rho}\ \ Cos[\phi]\right] \frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}\, d\phi \qquad 11\text{-}4$$

To compute the bit error probabilities with timing error, $\tau$, we again assume a first order phase-locked loop with the probability density function

previously defined. However, we assume the random variable transformation

$$\tau = T/2\pi \qquad 11\text{-}5$$

Performing the transformation of random variables [1] for the probability density function we obtain

$$f_\tau(\tau) = \frac{e^{\alpha\, Cos\left[\frac{2\pi}{T}\tau\right]}}{2\pi I_0[\alpha]}\frac{2\pi}{T} \quad , \quad \frac{-T}{2} \le \tau \le \frac{T}{2} \qquad 11\text{-}6$$

The bit error probability of BPSK with timing error is slightly more complex than for phase error because of intersymbol interference. If the adjacent bits are the same value as the current data bit, then there is no error due to timing. If they are different values, then the signal voltages will subtract from one another. With a timing error of $T/2$ and opposite data bits, the voltage out of an integrate-and-dump detector is zero volts. At this extreme, the receiver has a bit error probability of 1/2. (It can only make a random 0 or 1 decision about the transmitted symbol because all information has been lost.) The intersymbol interference is computed by the autocorrelation, $R(\tau)$, between adjacent pulses.

$$R(\tau) = \int_0^T p(t)p(t+\tau)dt$$

where 11-7

$p(t)$ is the baseband pulse shape

T is the symbol interval

With this definition that accounts for intersymbol interference due to timing error, the bit error probability with a first order timing synchronizer is obtained by taking the expected value with the transformed probability density function.

$$P_{\text{E,Synchronizer Timing}}(\rho) =$$

$$\frac{1}{2}\int_{-\tau}^{\tau}\frac{1}{2}\left\{\begin{array}{l} Erfc\left[\sqrt{\rho}\,\dfrac{R(\tau)+R(T-\tau)}{R(0)}\right] \\ +\,Erfc\left[\sqrt{\rho}\,\dfrac{R(\tau)-R(T-\tau)}{R(0)}\right]\end{array}\right\}\frac{e^{\alpha Cos\left[\frac{2\pi}{T}\tau\right]}}{2\pi I_0[\alpha]}\frac{2\pi}{T}d\tau \qquad 11\text{-}8$$

## 11.2. BPSK and QPSK Synchronization

So far we have discussed the requirement of the receiver to make estimates for $f_0$, $\theta$, and $\tau$. We have also shown some receiver degradation effects of poor estimates. Equation 11-9 expresses the BPSK modulation in a different form.

$$s(t) = \sum_{k=-\infty}^{\infty} a_k Cos[2\pi f_0(t+\tau)+\theta] \qquad 11\text{-}9$$

Suppose the receiver estimates $f_0$, $\theta$, and $\tau$ without error, which we denote as $\hat{f}_0$, $\hat{\theta}$, and $\hat{\tau}$. With the exact estimates, the receiver might demodulate the signal with the architecture shown in Figure 11.5. With perfect frequency and phase synchronization, the modulated signal is translated to baseband, where the integrate and dump is synchronized to the symbol intervals established by the timing parameter, $\hat{\tau}$.

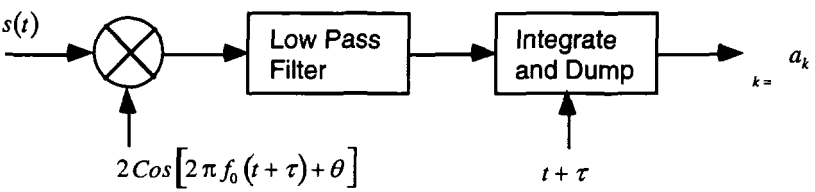


Figure 11.5 Demodulation With Perfect Synchronization

As an excursion from this perfect synchronization, consider when there is an error in the receiver's estimate, $\hat{f}_0$. (Note that if $\hat{f}_0 \neq f_0$, then generally, the phase estimate of $\theta$ cannot be computed.) The output from the receiver would be

$$y(t) = \sum_{k=-\infty}^{\infty} a_k \, Cos[2\pi f_e T k + \theta] \qquad 11\text{-}10$$

$f_e$ is the frequency error

T is the symbol timing interval

$a_k$ is the data symbol

If a training sequence of bits with $a_k = 1$ were first transmitted to the receiver, then the output of the receiver might appear as shown in Figure 11.6a. The structure of the error frequency can be easily determined in Figure 11.6a. (Another advantage of $a_k = 1$ is that the timing estimate is not needed, since all of the symbols have same data value.) By removing two of the unknown parameters, the synchronization problem is simplified. This is the general idea or concept of a preamble for TDMA networks. Because the modem must quickly acquire the signal to demodulate a short packet, the transmitter transmits a preamble which reduces the complexity of synchronization for the receiver.

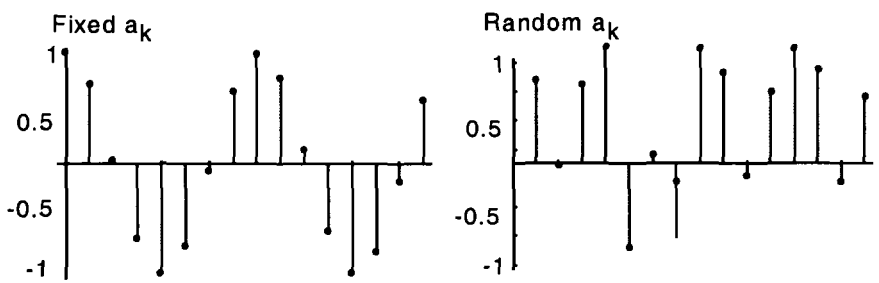


Figure 11.6 Receiver Outputs With Known and Unknown Data Patterns

The random data sequence in Figure 11.6 does not have an information structure to permit easy estimation of the frequency error. The comparison of the two receiver outputs suggests a fundamental strategy of synchronization: remove or de-couple estimate parameters. A Costas or squaring loop does exactly that: it removes the dependence upon the data values. A squaring loop receiver is shown in Figure 11.7.

The concept of the squaring loop is to remove the data modulation with the nonlinear operator, $(\cdot)^2$. As we will discuss shortly, other synchronizer

architectures substitute alternative nonlinear operators such as the absolute value, $|\cdot|^2$.

To analyze the squaring loop of Figure 11.7, let

$$s(t) = \sum_{k=-\infty}^{\infty} \sqrt{2P}\, a_k \, Cos[\, 2\pi f_0 (t+\tau) + \theta \,] + n(t) \qquad 11\text{-}11$$

The output from the nonlinear $(\cdot)^2$ operator is

$$s^2(t) = \sum_{k=-\infty}^{\infty} Pa_k^2 \left(1 + Cos[\, 4\pi f_0 (t+\tau) + 2\theta \,]\right) + n^2(t) + 4Pa_k \, Cos[\, 2\pi f_0 (t+\tau) + \theta \,] n(t) \qquad 11\text{-}12$$

Although the squaring operator removes the troublesome $\pm 1$ data values, there is a cost for the simplification. The noise term, $n(t)$, has also been squared. For additive white Gaussian noise, this effectively increases the noise in loop by 3 dB. Because of the decreased signal-to-noise, the squaring loop is not always the best choice for a synchronizer that must operate in low signal-to-noise conditions.

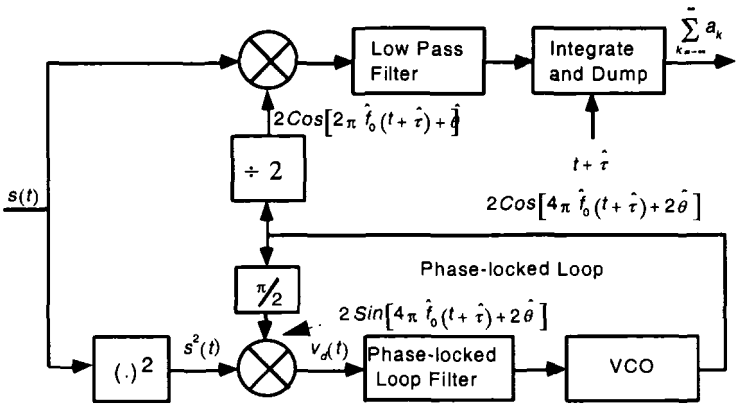


Figure 11.7 Squaring Loop for BPSK

From Figure 11-7, the VCO is assumed to have an output of the form

$$y(t) = 2\,Sin\left[4\pi \hat{f}_0(t+\hat{\tau}) + 2\hat{\theta}\right] \qquad 11\text{-}13$$

To simplify the following analysis, we are going to assume perfect symbol synchronization with $\tau = \hat{\tau} = 0$. Under these conditions, the lowpass output from the phase detector for the phase-locked loop is

$$\begin{aligned} v_d(t) &= -n_c(t)n_s(t)Cos\left[2\hat{\theta}\right] - \sqrt{2P}a_k n_s(t)Cos\left[\theta - 2\hat{\theta}\right] \\ &- \sqrt{2P}a_k n_c(t)Sin\left[\theta - 2\hat{\theta}\right] - Pa_k^2 Sin\left[2\left(\theta - \hat{\theta}\right)\right] + \frac{\left(n_c^2(t) - n_s^2(t)\right)}{2}Sin\left[2\hat{\theta}\right] \end{aligned} \qquad 11\text{-}14$$

In Equation 11-14, we have neglected all of the high order modulation terms. Most of the remaining terms are not a function of signal only. Many have a multiplicative noise term. Following the approach of Gardner [6], the phase detector output is written as a signal term with a corresponding noise term.

$$v_d(t) = -Pa_k^2 Sin\left[2\left(\theta - \hat{\theta}\right)\right] + n'(t) \qquad 11\text{-}15$$

It can be shown [6] that the equivalent phase jitter of the squaring loop is

$$\overline{\left(2\hat{\theta}\right)^2} = 4\frac{B_L N_0}{P}\frac{\frac{2P}{N_0 B_i} + 1}{\frac{2P}{N_0 B_i}}$$

$B_L$ is the loop bandwidth

$B_i$ is the input filter bandwidth 11-16

$N_0$ is the single - sided noise density

P is the input signal power

It is important to note that Equation 11-16 specifies the noise variance for the VCO in Figure 11.7 which is operating at twice the frequency as the actual data detector. In Chapter 12, we will discuss phase noise of digital divider [7] which states the output phase noise of a digital divider reduces

the input phase noise by a factor of $1/N^2$. (N is the division ratio of the divider.) In Figure 11.7, $N^2 = 4$, which allows us to approximate the noise variance for the data detector as

$$\overline{(\hat{\theta})^2} \approx \frac{B_L N_0}{P} \frac{\frac{2P}{N_0 B_i} + 1}{\frac{2P}{N_0 B_i}} \qquad 11\text{-}17$$

Recall from Chapter 4 the output variance of the analog phase-locked loop is $\sigma^2_{n\theta_o} = \frac{2N_o}{2P} B_L$, which is the inverse of the first term of Equation 11-17. The only difference in output phase variance to the data detector is the squaring loss, $\left( \frac{2P}{N_0 B_i} + 1 \right) \frac{N_0 B_i}{2P}$. At moderate signal-to-noise ratios, this term approaches unity, which would seem to imply little degradation due to the squaring loop. However, the phase-locked loop is still operating at twice the frequency, meaning it must perform acquisition and tracking according to the statistics of $\overline{(2\hat{\theta})^2}$, and not $\overline{(\hat{\theta})^2}$.

As a general estimate, a simple phase-locked loop will lose lock at $P/B_L N_0 \approx 3dB$ [6,32]. With the squaring loop, there is a nonlinear operator, $(\cdot)^N$, where N=2, that processes the input signal prior to the phase-locked loop. The squaring loop's acquisition/tracking threshold is degraded by approximately $20Log_{10}[N]$, which implies it will lose lock at approximately 9dB [6]. (We suggest the reader use comparisons of $P/B_L N_0$, instead of $SNR_L$ which varies in the literature.) A QPSK phase tracking loop that uses a N=4 nonlinearity, would be degraded by 12 dB.

Another disadvantage of squaring loops is that the output phase has a $\pi$ ambiguity. Because the squaring loop is operating at $2f_0$, it cannot

distinguish between an input phase error of $\pi$ or $2\pi$. Because of this, the output phase to the data detector could be in error by $\pi$ radians, which for BPSK would invert the sign of the data. This ambiguity can be solved by utilizing differential coding [10], or a training sequence/preamble. With a known input sequence, the demodulator can adjust its output polarity with the a priori data.

Figures 11.8 and 11.9 show the performance of a digital squaring loop. At $P/B_L N_0 = 6dB$ levels, or even $P/B_L N_0 = 12dB$, the output phase error into the phase-locked loop's filter is very noisy due to the amplitude noise on the signal. The loop could be locked, but the observer wouldn't be able to distinguish discern a difference due to the amplitude noise. With a digital simulation however, we have replicas of the signal without noise that we can demodulate with the VCO. Hence, the notation, "Error Detector With No Amplitude Noise". (The only noise is caused by the errors in the phase estimate, $\hat{\theta}$.)

A difficult problem in synchronization is determining when the synchronizer has achieved "lock". Generally, a mixer with a 90° phase shift in the local oscillator is used as a phase-lock indicator. Gardner terms this a quadrature detector [7]. In Figures 11.8 and 11.9, we consider a quadrature detector with the noiseless input signal. As with the error signal, the output of a quadrature detector is very noisy at these signal levels without filtering.

These error and lock detector outputs for a squaring loop show a cost for the simplicity of a squaring loop. As discussed earlier, the synchronization loop loses 6 dB of *S/N* performance. In some applications, the input $E_b/N_o$ and accompanying data rate may be sufficient to allow a squaring loop implementation. In others, a linear implementation may be necessary.

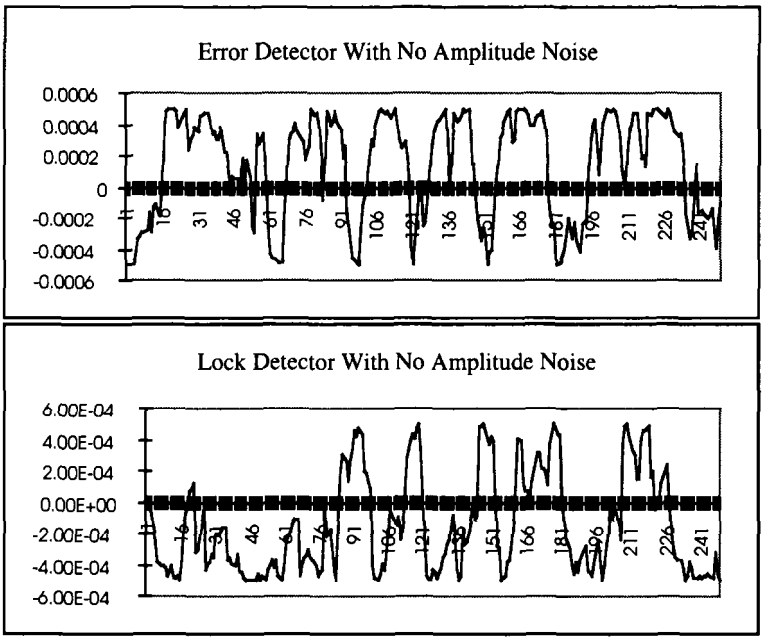


Figure 11.8 Squaring Loop Performance at $P/N_0 B_L = 6dB$

Fast acquisition and low loop jitter are opposing goals. Frequently modem designers will utilize "gear-shifting" of the phase-locked loop's bandwidth [34]. During initial acquisition of a TDMA frame, the loop bandwidth may be large to accommodate a larger Doppler offset. After frame acquisition, the loop bandwidth may be slowly stepped down to provide the low phase error variance desired for Eb/No performance.

### 11.2.1 QPSK Detection Degradation Due to Carrier Recovery Jitter

To remove the data modulation from 4-PSK (QPSK) modulation, a $4^{th}$ power nonlinearity is required. This is typically described as a quadrupling loop or an extended Costas Loop. The probability of error for QPSK demodulation with carrier phase jitter is written as [4]

$$P_{\text{E,Synchronizer Phase,QPSK}}(\rho) =$$

$$\frac{1}{2}\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\ (Cos[\phi]+Sin[\phi])\right]\frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}\,d\phi \qquad 11\text{-}18$$

$$+\frac{1}{2}\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\ (Cos[\phi]-Sin[\phi])\right]\frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}\,d\phi$$

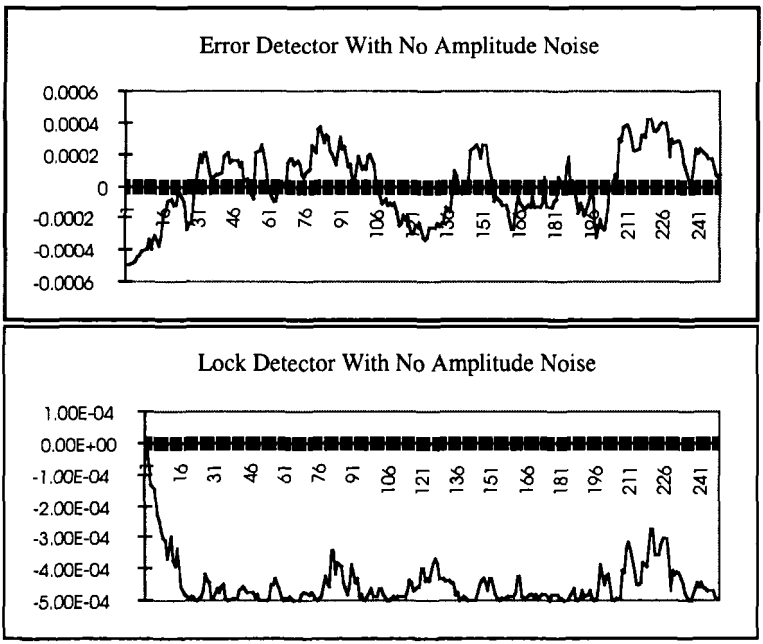


Figure 11.9 Squaring Loop Performance at $P/N_0B_L = 12dB$

Offset QPSK (OQPSK) has two quadrature bit streams as in QPSK, but the bit intervals are offset by half a bit period. (The advantage of this complexity is a waveform that is closer to constant-envelope.) Because the I and Q channels are not permitted to have transitions at the same time, the maximum phase transition at any one time is $\pi/2$. This reduces the spectrum degradation when transmitted through a bandlimited nonlinear channel. The BER degradation for OQPSK is the average of the degradation of BPSK and QPSK, as shown in Equation 11-19 [4].

$$P_{\text{E,Synchronizer Phase,OQPSK}}(\rho) = \frac{1}{2}\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\ Cos[\phi]\right]\frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}d\phi$$
$$+\frac{1}{4}\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\ (Cos[\phi]+Sin[\phi])\right]\frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}d\phi \qquad 11\text{-}19$$
$$+\frac{1}{4}\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\ (Cos[\phi]-Sin[\phi])\right]\frac{e^{\alpha\, Cos[\phi]}}{2\pi I_0[\alpha]}d\phi$$

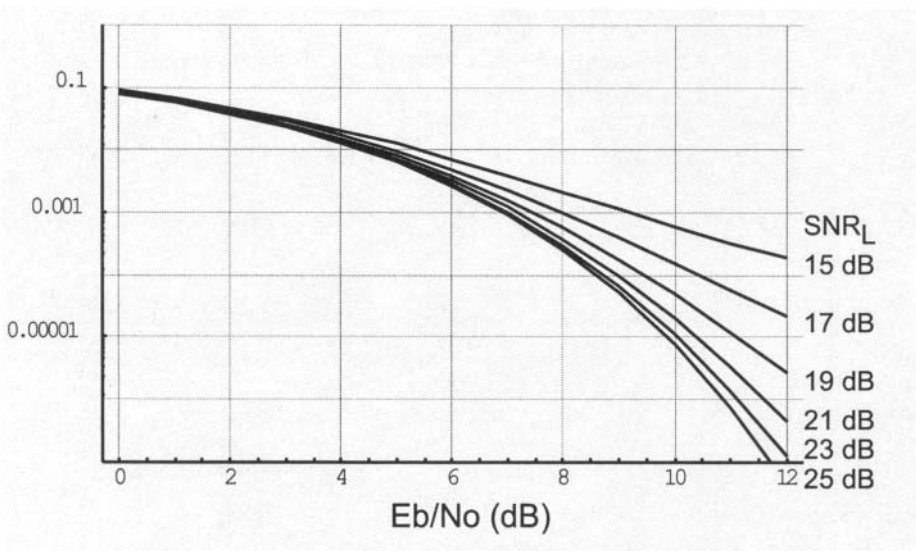


Figure 11.10 BER Performance for QPSK With Carrier Phase Jitter

The signal-to-noise ratio for the data bit, $\rho$, and the signal-to-noise ratio for the phase-locked loop, $\alpha$, were previously defined for Equation 11-4. Figures 11.10 and 11.11 graph the BER performance for QPSK and OQPSK modulations, respectively.

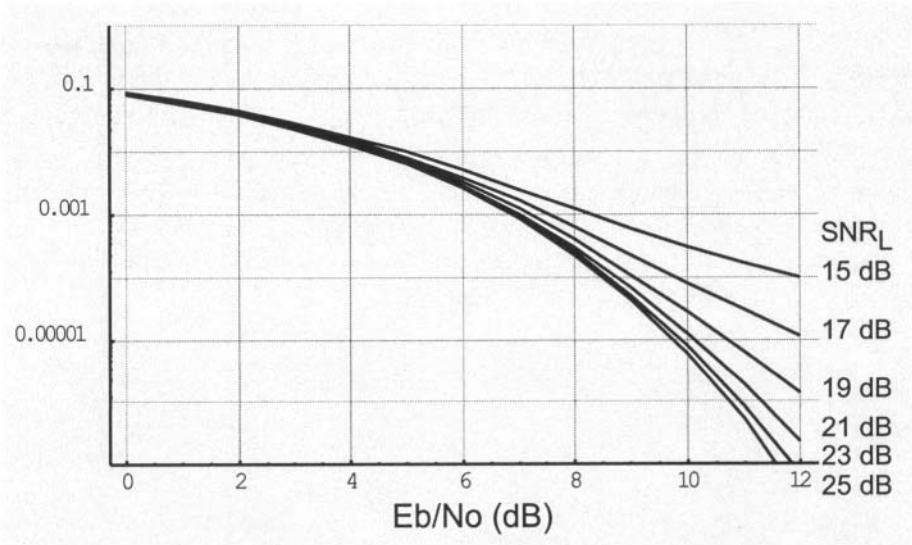


Figure 11.11 BER Performance for OQPSK With Carrier Phase Jitter

## 11.3. Lock Detectors

The quadrature lock detector was mentioned briefly in a preceding paragraph. Figure 11.12 shows the functional block diagram of a combination phase detector and quadrature detector.

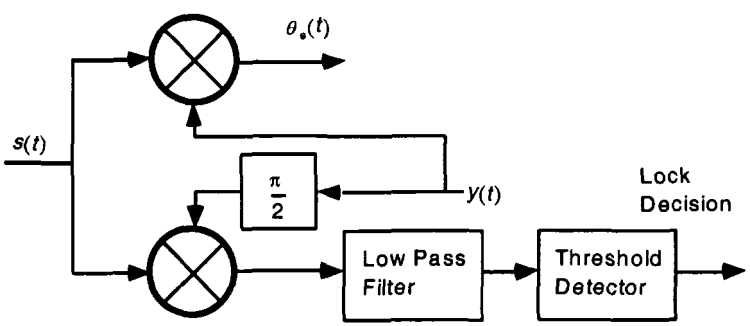


Figure 11.12 Combination Phase Detector and Lock Detector

The upper mixer element represents the traditional phase detector, producing the phase error, $\theta_e(t)$. The designation quadrature detector becomes evident in the bottom mixer element, because it is operated with a

quadrature (90°) shifted local oscillator, $y(t)$. As discussed earlier, the output of the quadrature mixer is much too noisy to be used directly at low $S/N$ levels. A lowpass filter removes enough of the noise such that a threshold detector can make a reliable lock decision. Obviously, any filtering in the lowpass filter will add to the acquisition decision time, because of the filter delay. (Typically the filter is specified in terms of delay, rather than in bandwidth. Depending on the application, the filter might be designed for a 90% rise time in 5-10 data symbols.)

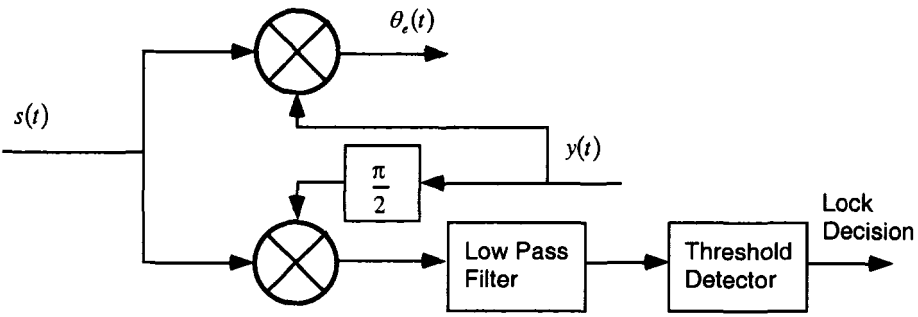


Figure 11.13 Combination Phase Detector and Lock Detector

## *Example 11.1*

Design a phase-locked loop to perform the phase synchronization for a BPSK receiver using a squaring loop. Assume the following parameters: Carrier Frequency - 2 MHz, Bit rate - 4,800 bits /sec, Input power to Phase Detector - 0 dBm, VCO Tuning Constant 10 KHz/Volt (Centered at 2 MHz), Phase Detector 1V/radian, Initial Frequency Offset -1 KHz , less than 0.2 dB degradation at $E_b/N_0 = 9.6dB$

Using Equation 11-17, we assume the squaring loss, $\left(\frac{2P}{N_0 B_i}+1\right)\left(\frac{N_0 B_i}{2P}\right)$ is negligible. (Recall this is accomplished by reducing the bandwidth of the arm filters.) With this assumption, the output phase variance of the squaring loop can be represented by $\overline{(\hat{\theta})^2} \approx B_L N_0/P$, which is the same as the first order phase-locked loop. The bit error probability for BPSK with phase jitter is specified with Equation 11-4. At

$E_b/N_0 = 9.6dB$, the bit error probability of BPSK is $9.7\times10^{-6}$. However, we are permitting 0.2 dB degradation due to the squaring loop, which implies the effective $E_b/N_0$ to the detector is 9.4 dB, yielding a bit error probability of $1.5\times10^{-5}$. (Use Equation 11-3 with $\phi = 0$.)

Numerically solving Equation 11-4 with the degraded bit error probability,

$$1.5\times10^{-5} = \int_{-\pi}^{\pi} \frac{1}{2} Erfc\left[\sqrt{\rho\, Cos[\phi]}\right] \frac{e^{\alpha Cos[\phi]}}{2\pi I_0[\alpha]} d\phi \Bigg|_{\rho=9.6\,dB} \qquad 11\text{-}20$$

for the signal-to-noise ratio, $\alpha$, within the phase-locked loop, we obtain $\alpha = 12dB$. This is the fundamental parameter, because the signal-to-noise ratio is defined as $\alpha = P/N_0 B_L$. Recall for the digital waveform, $P = E_b \times \text{Bit Rate}$. Substitution yields

$$\alpha = \frac{E_b \times \text{Bit Rate}}{N_0 B_L} \qquad 11\text{-}21$$

With the problem statement parameters and $\alpha = 12dB$, we obtain the necessary loop bandwidth for the phase-locked (squaring) loop.

$$B_L = \frac{E_b}{N_0} \frac{\text{Bit Rate}}{\alpha}$$
$$= 9.12 \frac{4800}{15.8} = 2{,}771\text{Hz} \qquad 11\text{-}22$$

As discussed earlier, the acquisition threshold for a squaring loop is somewhere around a 9 dB loop signal-to-noise ratio (implementations vary as well as the definition of threshold). Usually we would want a much smaller loop bandwidth, but recall the acquisition time of the phase-locked loop is a function of the loop bandwidth. In this example, we have an initial frequency offset of 1 KHz, which allows us to use Equation 4-20, (assuming a second order loop filter)

$$t_{phase} + t_{freq} = \frac{4.0}{w_n} + \frac{4.2}{B_L^3}(\Delta f)^2$$

$$= \frac{\frac{0.5}{\zeta} + 2\zeta}{B_L} + \frac{4.2}{B_L^3}(\Delta f)^2 \qquad 11\text{-}23$$

Assuming $\zeta = 0.707$, and substituting the other parameters, we obtain a total acquisition time, $t_{phase} + t_{freq} = 1.6\text{msec}$. (Note that the squaring loop requires $2 \times \Delta f$ for acquisition because the input frequencies are doubled.) This loop bandwidth thus requires 7.5 bit periods to obtain phase and frequency synchronization. Actually, this is best case, because in an actual squaring loop, a lock detector is required, which will required additional time to make the decision of phase-lock.

With the loop bandwidth and acquisition time established, the design of the phase-locked loop is identical to the design examples in Chapter 2. The remaining design details are left for the chapter problems.

## 11.4. Costas Loops

The Costas loop shown in Figure 11.13 [8] is similar in appearance to the squaring loop previously analyzed. In performance, it is mathematically identical to the squaring loop, but offers some reduction in complexity for BPSK demodulators. The upper arm of the Costas Loop, sometimes called the I arm, produces the demodulated data symbol.

Without modulation, the quadrature arm is producing an error voltage similar to a simple phase-locked loop. (Note that without data modulation, the output of the I arm will be zero.) When a $\pm\pi$ phase change occurs, corresponding to the data modulation, the output of the Q arm will reverse sign. However, the I arm is demodulating the data symbol, so that it corrects the sign of the Q arm's error voltage. This allows the Costas loop to be invariant to the BPSK modulation. In a sense, the Costas loop is decision-directed, because a hard decision is made on the present data symbol and that decision is used to adjust the phase tracking of the carrier.

The lowpass arm filters are usually selected to minimize the squaring loss. However, if the filter bandwidth is too small, it produces distortion of the data symbols and leads to false lock [22,23,24]. A compromise for a one-pole RC filter seems to be $B = 1/T_s$, where $T_s$ is the symbol period [29]. If timing information is known, the lowpass arm filters in Figure 11.11 can be replaced with symbol integrate-and-dump detectors.

Shown in dashed lines is the lock detector that can be included with the Costas loop. See [22,23,24] for further analysis.

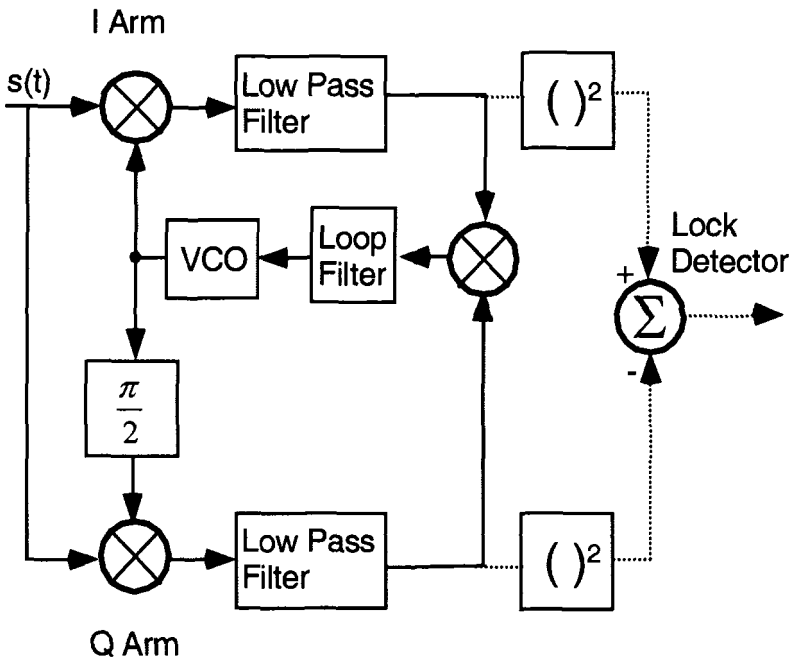


Figure 11.14 Costas Loop for BPSK

Although more complex because of the multiple symbol possibilities, an extended Costas loop [6,8,20,25] can be used to synchronize QPSK modulation. Figure 11.14 shows a Costas loop for QPSK. Because of the 4th power implementation, the QPSK Costas loop has a phase ambiguity of $\pi/2$ radians. (Generally this is accommodated by a preamble prior to the actual data transmission.) As mentioned earlier, the Costas QPSK phase tracking loop has a N=4 nonlinearity, which degrades the acquisition performance of a simple PLL by 12 dB.

The Costas Loop can exhibit a false-lock phenomena [22] where the loop is locked improperly. The false-locks are attributed to arm filter distortion of the data (the lowpass filters in Figures 11.13 and 11.14). False lock in a Costas Loop is most likely to occur when the signal's carrier frequency and the loop's VCO frequency differ by $nR_s/2$, $n \in \{1,2,\ldots\}$ where $R_s$ is the data symbol rate [22,23].

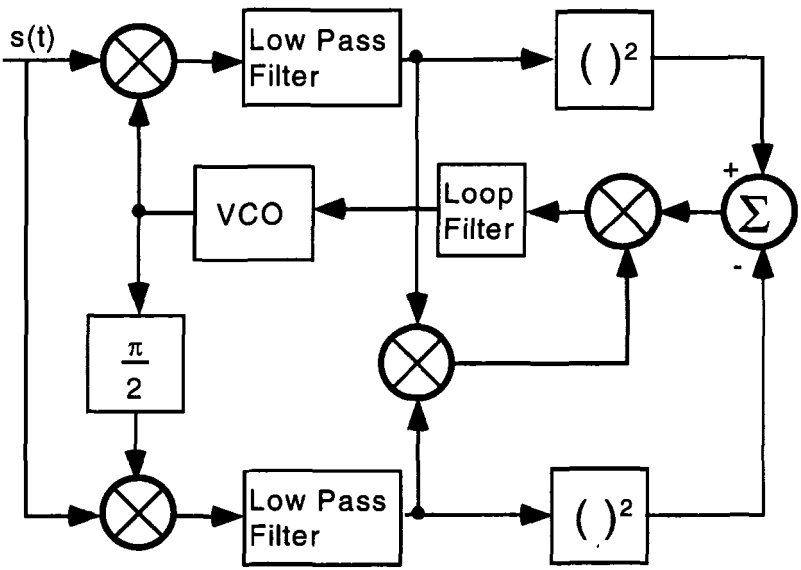


Figure 11.15 Costas Loop for QPSK Carrier Recovery

## 11.5. Timing Synchronizers

The squaring loop defined in Figure 11.6, or the Costa Loop in Figure 11.12 do not have any provision for adjusting the symbol timing estimate, $\hat{\tau}$. In a paper by Mueller and Muller [16], they describe approaches to timing recovery. They categorize three different types of timing synchronization: a) Threshold Crossings, b) Signal Derivatives, c) Spectral lines. Since that time, other approaches have been developed. One such technique is maximum likelihood which will be discussed shortly.

If the waveform has distinct reference levels, the waveform can be examined on when it crosses a threshold. For example, BPSK transitions which switch the baseband signal between $\pm$ 1. A zero crossing detector would provide timing information because the symbol transitions occur at the

zero crossing. More complex thresholds have to be defined for higher order PSK modulations.

Gardner [5,26-28] developed a timing error detector for BPSK and QPSK receivers that is based on threshold crossing. Although some algorithms can use a single sample per symbol, this algorithm utilizes two samples. The algorithm is written as [28]

$$u_n = x^i_{n-\frac{1}{2}}\left(x^i_n - x^i_{n-1}\right) + x^q_{n-\frac{1}{2}}\left(x^q_n - x^q_{n-1}\right) \qquad 11\text{-}24$$

$x^i$ is the inphase "I" symbol sample

$x^q$ is the quadrature "Q" symbol sample

$x_{n-\frac{1}{2}}$ is the sample between symbol $x_{n-1}$ and $x_n$

For BPSK operation with prior carrier recovery, the quadrature terms in Equation 11-24 are zeroed to reduce jitter [28].

An alternative detector utilizes the signal derivative at the sampling points for the waveform. This can be used to provide control information such as the Gitlin and Salz phase detector [17]. A technique previously used extensively with analog modems was a frequency detector with a narrow band filter to distinguish the symbol frequency. With balanced modulation, the spectral lines do not appear in the modulator's spectrum. Placing the received signal through a nonlinear element can generate the spectral lines that can be used to control a narrowband phase-locked loop. (This is exploiting the cyclostationary properties of the waveform.) With advanced modulation waveforms, the tone amplitude may have insufficient signal-to-noise ratio for operation at low signal levels [9].

For the BPSK timing synchronizer, we introduce the early-late gate which is shown in Figure 11.16. Similar to carrier phase synchronization, the timing synchronizer must compensate for the sign of the transmitted data symbol. As shown in Figure 11.16, the timing synchronizer is more complex than the phase synchronizer. An implementation with squaring elements such as the carrier recovery squaring loop will not produce the correct error voltages. (Note that a zero-crossing detector can provide timing information without the increased complexity of the early-late gate synchronizer. This disadvantage of this synchronizer is poorer signal-to-noise performance.)

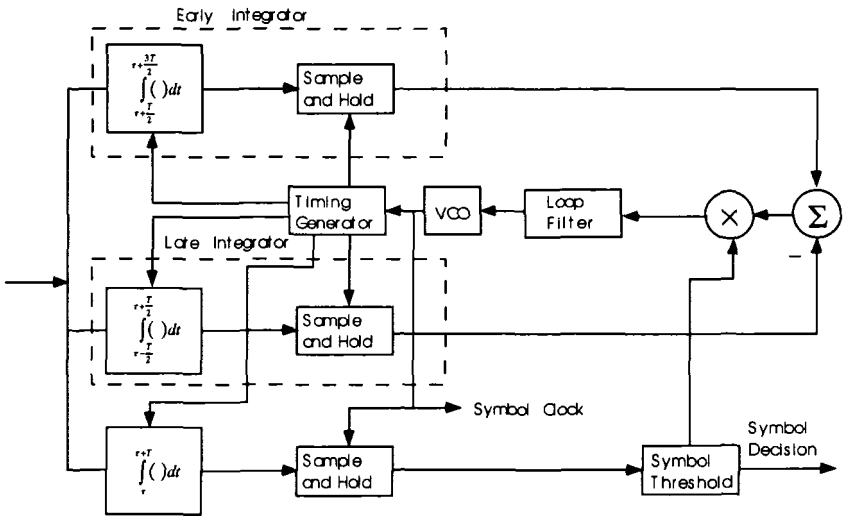


Figure 11.16 Early-Late Gate Symbol Synchronizer [6]

The most appropriate perspective of the early-late gate synchronizer is that it is approximating the derivative of the sampled waveform with respect to the unknown timing parameter, $\tau$. (An actual derivative processor is the mathematically optimum synchronizer.) A matched filter receiver must compute the term,

$$V(T,\tau) = \int_{\tau+0}^{\tau+T} s(t)h(t)dt \qquad 11\text{-}25$$

Indeed, in Figure 11.16, the lower block is a matched filter receiver implementation. Note for BPSK, the transfer function, h(t)=l because the baseband data is a simple pulse. For other modulation formats, the actual h(t) would be required in the integrator. In order to synchronize the modem's output of Equation 11-24, the receiver must accurately estimate the timing offset, $\tau$. The derivative of Equation 11-25 with respect to $\tau$ can be approximated as

$$\frac{\partial V(T,\tau)}{\partial \tau} = \frac{1}{T}\left( \int_{\tau+\frac{T}{2}}^{\tau+\frac{3T}{2}} s(t)\, h(t)\, dt - \int_{\tau-\frac{T}{2}}^{\tau+\frac{T}{2}} s(t)\, h(t)\, dt \right) \qquad 11\text{-}26$$

To maximize the symbol voltage with respect to the timing offset, $\tau$, the derivative approximation, Equation 11-26, is placed in a phase-locked loop which attempts to adjust $\tau$ so that the derivative is zero. This is the concept of the early-late synchronizer shown in Figure 11.16.

There is a complication, however, because the data values, s(t) of $\pm 1$ will not provide a consistent error detection. For example, the phase-locked loop expects that a timing error of +x volts would imply the timing needs to be advanced. However, if Equation 11-26 is implemented with an implicit h(t)=l, then the timing error will change polarity due to the data as well as the timing offset. To correct this ambiguity, the early-late synchronizer of Figure 11.16 uses the $\pm 1$ symbol value to multiply the timing offset derivative. This provides a consistent sign or direction for the phase-locked loop.

Generally the timing synchronizer has strong nonlinearities in the VCO/timing generator blocks of Figure 11.16. These nonlinearities can be a result of timer quantization, interpolators, etc. As a consequence, a synchronizer loop is more difficult to implement. In most applications though, the loop bandwidths of the symbol synchronizer loop are much lower than the carrier phase loop, and this relieves some of the implementation difficulty.

Figure 11.17 shows the synchronization acquisition of an early-late synchronizer. This synchronizer utilizes an interpolator for the timing generator, which will be discussed later in this chapter. When the synchronizer has acquired, the symbol voltage is the $\pm 1$ volts, as expected for BPSK. The data pattern to the synchronizer was 01010101..., which is desirable for acquiring BPSK because of a symbol changing value on every epoch. The symbol voltage shows a slight overshoot suggestive of a phase-locked loop at symbol 10. The control voltage however, is very nonlinear, which corresponds to the nonlinear timing generator.

The early-late synchronizer of Figure 11.16 is actually a data-aided synchronization loop. The symbol decision which is generated by the lower integrator, $\int_{\tau}^{\tau+T}(\,)dt$ is aiding the early-late synchronizer by providing the polarity of the data. As was discussed, this is necessary to generate an unambiguous error voltage from the derivative's approximation. The squaring loop of Figure 11.7 is a non-data-aided synchronization loop. It uses the nonlinear squaring function instead of relying on a data estimate.

The non-data-aided loop has a 6 dB degradation in acquisition as was discussed earlier. The data-aided loop is a conventional phase-locked loop and does not suffer this degradation. However, the data-aided loop does require accurate symbol decisions, or the synchronization loop can become "confused".

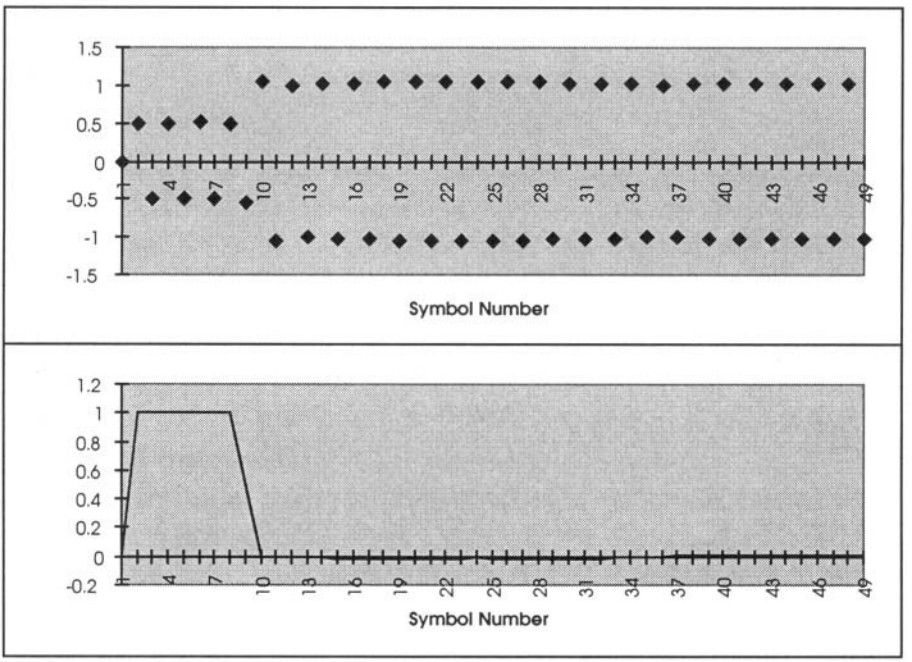


Figure 11.17 Acquisition of the Early-Late Synchronizer

As a general estimate, a data-aided loop requires a symbol error rate, $SER \leq 5 \times 10^{-2}$. Note that the symbol error rate is important, rather than the bit error rate, BER. (For BPSK, they are the same.) Also, the SER is the physical layer's error rate before forward error coding. It is the rate at which incorrect decisions are provided to the differentiator in Figure 11.16 that determines the synchronizer performance.

To design the phase-locked loop of the synthesizer, it is necessary to define the phase detector's gain for the phase-locked loop equations defined earlier in this text. The phase detector itself is the approximation of the derivative multiplied by the sign of the symbol. (Other phase detectors can be designed, but most of these tend to be ad hoc and their performance is largely unpredictable.)

Figure 11.18 shows the phase detector characteristic of the early-late synchronizer. The phase detector is monotonic between the limits of its operation. (This is extremely important for a synchronizer's phase detector because otherwise the synchronization loop becomes locked at a local minimum.)

The slope of the phase detector can be altered by changing the delay between the early and late symbols. The integration in Equation 11-25 is 1/2 symbol before and after the actual symbol integration. This can be varied to modify the phase detector characteristic.

For example, the derivative for the phase detector's transfer function can be approximated by $\frac{\partial V(T,\tau)}{\partial \tau} = \frac{1}{T}\left( \int_{\tau+\frac{T}{4}}^{\tau+\frac{5T}{4}} s(t)\, h(t)\, dt - \int_{\tau-\frac{T}{4}}^{\tau+\frac{3T}{4}} s(t)\, h(t)\, dt \right)$ which corresponds to a 1/4 symbol delay. This phase detector is shown in Figure 11.19. It has increased gain, but note that the valid input range is $-T/4 \le \tau \le T/4$

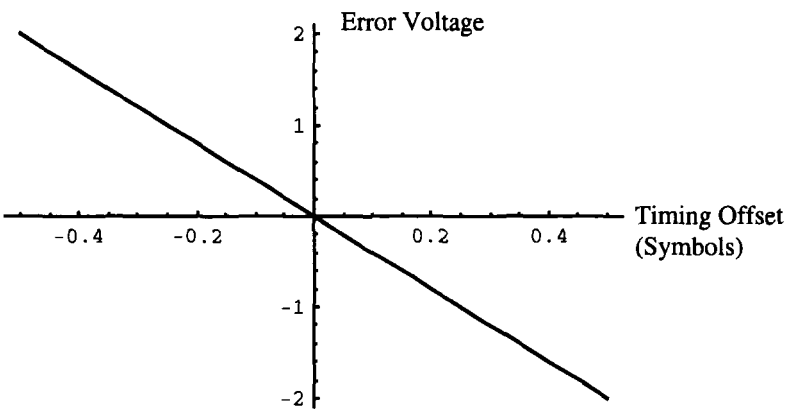


Figure 11.18 Error Voltage for Early-Late Phase Detector (Delay = $1/2$)

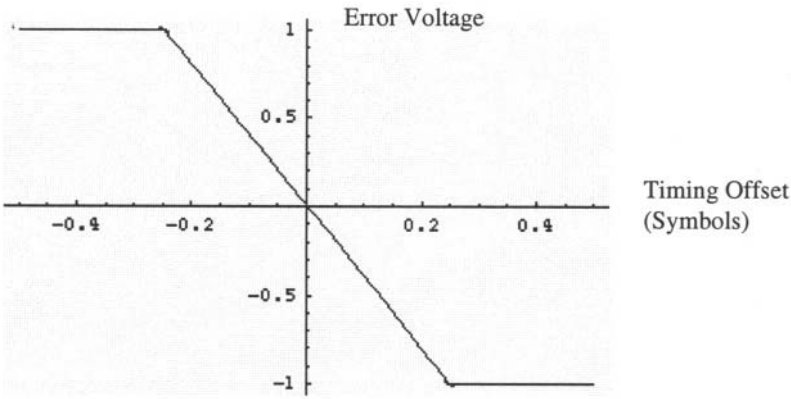


Figure 11.19 Early-Late Phase Detector With Delay = 1/4

### 11.5.1. Maximum Likelihood Synchronization

The 6 dB acquisition advantage of the simple phase-locked loop over the squaring loop suggests that communication theory can provide insight into the optimum synchronizer design. A maximum likelihood architecture provides significant improvement over ad hoc approaches to synchronization. Our development follows that of Ziemer and Peterson [10].

Suppose we represent the received signal simply as

$$y(t) = p(t) + n(t) \qquad 11\text{-}27$$

p(t) is the transmitted symbol and n(t) is additive white Gaussian noise. A set of orthogonal basis functions can be found to represent p(t) and n(t),

$$p(t) = \sum_{k=0}^{N} p_k \varphi_k(t) \quad where\ p_k = \int_0^T p(t)\varphi_k^*(t) \qquad 11\text{-}28$$

$$n'(t) = \sum_{k=0}^{N} n_k \varphi_k(t) \quad where\ n_k(t) = \int_0^T n(t)\varphi_k^*(t) \qquad 11\text{-}29$$

$$y_k = p_k + n_k \qquad 11\text{-}30$$

Recall the Fourier Series is an example of an orthogonal basis function. In this derivation, we are not concerned with defining an actual set, because we will soon discard them. The noise n(t) is not exactly represented by $n'(t)$. The basis functions were selected to reproduce the information, p(t), and we will accept distortion in the noise component, n(t).

Because $\int_0^T \varphi_k(t)\,\varphi_l^*(t) = 0$ , $k \neq l$, the individual components of $y_k$ are independent, Gaussian variables. The joint probability density function can be written as

$$\Pr(y(t)) = \prod_{k=0}^{N} \Pr(y_k(t)) \qquad 11\text{-}31$$

Because each of the $y_k(t)$ are independent and Gaussian, the joint probability can be written as

$$\Pr(y(t)) = \prod_{k=0}^{N} \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-(y_k - p_k)^2}{2\sigma^2}} \qquad 11\text{-}32$$

Because of the exponential properties, the product in Equation 11-32 can be converted to a summation with the exponent, simplifying to

$$\Pr(y(t)) = \left(2\pi\sigma^2\right)^{\frac{N}{2}} \exp\left\{ \sum_{k=0}^{N} \frac{-(y_k - p_k)^2}{2\sigma^2} \right\} \qquad 11\text{-}33$$

The log likelihood function is obtained by taking the natural logarithm of Equation 11-33, which eliminates the exponentiation. Because log() is monotonic function, maximizing Equation 11-34 is the same as maximizing Equation 11-33

$$\Lambda \approx K + \sum_{k=0}^{N} (y_k - p_k)^2 \qquad 11\text{-}34$$

From Parseval's Theorem [10], the orthogonal basis functions can be discarded, leaving,

$$\Lambda \approx K + \int_0^T \left(y(t) - p(t)\right)^2 \qquad 11\text{-}35$$

Note the binomial in the exponent can be expanded into $y^2(t) + p^2(t) - 2y(t)p(t)$. For a constant envelope waveform such as CPM, the first two terms are constant, leaving

$$\Lambda \approx \int_0^T y(t)\, p(t) \qquad 11\text{-}36$$

In an infinite bandwidth channel, BPSK and QPSK can be considered to be constant envelope, since they are phase-only modulation. However, in a non-linear, bandlimited channel, their envelope does exhibit time dependence. The approximation of Equation 11-36 may be invalid in such a communications channel [35]. Many of the spectrally efficient waveforms such as Quadrature Amplitude Modulation (QAM) do not meet this criteria of a constant envelope. (The constant envelope waveforms are highly desirable in nonlinear channels to avoid spectral regrowth [35-37].)

Equation 11-36 represents a correlation receiver [10,31,35]. As indicated by the integral, the receiver simply correlates the received signal against every possible received waveform, p(t), and selects the largest correlation. (Equivalent to the most likely received waveform.) Aside from the optimality of the symbol decision, the synchronization properties are very desirable. We rewrite Equation 11-35, showing the dependence of the likelihood function on the synchronization parameters, $\theta$ and $\tau$ [11].

$$\Lambda(\theta,\tau) \approx \int_0^T y(t)p(t,\theta,\tau)dt \qquad 11\text{-}37$$

In Equation 11-37, the phase and timing offsets are attributed to the local estimate, p(t), rather than the received signal, y(t). Recall from calculus to maximize the function with respect to a variable, we take the derivative and set it equal to zero. So to maximize the log likelihood function with respect to the timing offset, we take the partial derivative of Equation 11-36 with respect to $\tau$ and adjust $\tau$ until the partial derivative is zero. This exactly what the early-late synchronizer of Equation 11-25 performs.

$$\frac{\partial \int_0^T y(t)\, p(t,\theta,\tau)dt}{\partial \tau} = 0 \qquad 11\text{-}38$$

The same operation can be performed on the log likelihood function to optimize the estimate of carrier phase, $\theta$. The partial derivative is formed,

$$\frac{\partial \int_0^T y(t)\, p(t,\theta,\tau)dt}{\partial \theta} = 0 \qquad 11\text{-}39$$

Symbolically, this implies that if the received signal is of the form $s(t,\theta) = Cos[\varphi(t) + \theta]$, then the maximum likelihood phase detector should be

$$\varepsilon(\theta) = -\int_0^T Cos[\varphi(t) + \theta] Sin[\hat{\varphi}(t) + \hat{\theta}]dt \qquad 11\text{-}40$$

where

$\hat{\varphi}(t)$ is the estimated phase modulation (data symbol)

$\hat{\theta}$ is the estimated carrier phase offset

The phase detector of Equation 11-40 can be used with a simple phase-locked loop instead of the squaring loop configuration of Figure 11.7 to obtain a 6 dB signal-to-noise advantage in acquisition. The estimated symbol modulation, $\hat{\varphi}(t)$ is equivalent to the data-aided feedback of the early-late synchronizer of Figure 11.15.

The implementation details of maximum likelihood synchronizers are dependent upon the data modulation. If the data modulation includes coding such as trellis-coded CPM or multi-h CPM, the data symbol estimation can be obtained by following the correlators with a Viterbi algorithm [10,31]. The Viterbi algorithm can be shown [11] to be an optimum maximum likelihood estimate for the encoded symbol.

Similar to the false-lock phenomena of Costas loops, decision directed loops also are subject to false lock [23]. With decision directed or mod-

remod loops, the false locks are attributed to either the loop delay time or the modulation frequency. A delay element will cause a false lock at the offset frequencies $\Delta f_k = \frac{4k-1}{4\tau}, k \in \{1,2,\ldots\}$, where $\tau$ is the delay time, provided there is sufficient loop gain [23]. False locks can also occur at frequency offset of $\Delta f = \frac{m}{n} f_m$, where $\frac{m}{n}$ is a simple fraction and $f_m$ is the data modulation frequency. This latter false lock phenomena suggests the capture range of the PLL be limited to avoid some possible false acquisitions.

An alternative to the BPSK decision-directed maximum likelihood receiver is to square the input signal first, removing the data modulation [10]. Because this squares the input noise as well as introducing a noise x signal component, it is suboptimum. It does possess the advantage however, that a feedback decision is not necessary. The development of the corresponding maximum likelihood equations is left to the problems.

### 11.5.2. Joint Carrier and Clock Estimation

Often the carrier phase and timing synchronizers in a modem will be in conflict, because each is attempting an independent solution. However, the carrier phase detector can produce an error voltage due to a timing offset, and the carrier phase loop will attempt to adjust the carrier loop to compensate for the timing offset. If on the same symbol, the timing loop is already attempting to compensate for the timing offset, then the two loops will be competing with each other. To make the problem worse, the timing loop error detector can sometimes produce an error due to carrier phase error, and the two synchronization loops are never ever able to achieve the optimum synchronization.

In practice, modem designers are sometimes able to limit the conflict between the synchronization loops by having the timing loop bandwidth to be much less than the carrier phase loop. (A 10:1 ratio is common.) In some situations this may not be possible, or the modulation may implicitly have this phase-timing conflict. To limit the synchronizer conflict, it is possible to jointly estimate the phase and timing offsets with simultaneous equations.

Our derivation follows that of Meyers and Franks [11]. The log-likelihood Equation 11-37 can be approximated with a first-order Taylor series of two variable as [11].

$$\Lambda(\theta,\tau) \approx \int_0^T y(t)\, p(t,\theta,\tau)dt\Big|_{\hat{\theta},\hat{\tau}} + \left(\theta-\hat{\theta}\right)\frac{\partial}{\partial\theta}\int_0^T y(t)\, p(t,\theta,\tau)dt + \left(\tau-\hat{\tau}\right)\frac{\partial}{\partial\tau}\int_0^T y(t)\, p(t,\theta,\tau)dt \qquad 11\text{-}41$$

Note the last two terms are essentially the phase detector terms for the maximum likelihood synchronizer. As with the maximum likelihood derivation above, we take the partial derivative of the three-term approximation with the synchronization variables to obtain [11]

$$\frac{\partial}{\partial\theta}\Lambda(\theta,\tau) = \frac{\partial}{\partial\theta}\int_0^T y(t)\, p(t,\theta,\tau)dt\Big|_{\hat{\theta},\hat{\tau}} + \frac{\partial}{\partial\theta}\left(\theta-\hat{\theta}\right)\int_0^T y(t)\, p(t,\theta,\tau)dt + \frac{\partial}{\partial\theta}\left(\tau-\hat{\tau}\right)\int_0^T y(t)\, p(t,\theta,\tau)dt \qquad 11\text{-}42$$

$$\frac{\partial}{\partial\tau}\Lambda(\theta,\tau) = \frac{\partial}{\partial\tau}\int_0^T y(t)\, p(t,\theta,\tau)dt\Big|_{\hat{\theta},\hat{\tau}} + \frac{\partial}{\partial\tau}\left(\theta-\hat{\theta}\right)\int_0^T y(t)\, p(t,\theta,\tau)dt + \frac{\partial}{\partial\tau}\left(\tau-\hat{\tau}\right)\int_0^T y(t)\, p(t,\theta,\tau)dt \qquad 11\text{-}43$$

In the shorthand notation of Meyers and Franks [11], these synchronization equations can be written as

$$\Lambda_\theta(\theta,\tau) = \Lambda_\theta\left(\hat{\theta},\hat{\tau}\right) + \Lambda_{\theta\theta}\left(\hat{\theta},\hat{\tau}\right)\left(\theta-\hat{\theta}\right) + \Lambda_{\theta\tau}\left(\hat{\theta},\hat{\tau}\right)\left(\tau-\hat{\tau}\right) = 0 \qquad 11\text{-}44$$

$$\Lambda_\tau(\theta,\tau) = \Lambda_\tau\left(\hat{\theta},\hat{\tau}\right) + \Lambda_{\tau\theta}\left(\hat{\theta},\hat{\tau}\right)\left(\theta-\hat{\theta}\right) + \Lambda_{\tau\tau}\left(\hat{\theta},\hat{\tau}\right)\left(\tau-\hat{\tau}\right) = 0 \qquad 11\text{-}45$$

In the synchronization equations above, we have set them equal to zero, because that corresponds to the maximum of the likelihood function, $\Lambda(\theta,\tau)$. The two simultaneous equations can be written in matrix form as

$$\begin{bmatrix} \Lambda_\theta(\theta,\tau) \\ \Lambda_\tau(\theta,\tau) \end{bmatrix} = \begin{bmatrix} \Lambda_{\theta\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\theta\tau}\left(\hat{\theta},\hat{\tau}\right) \\ \Lambda_{\tau\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\tau\tau}\left(\hat{\theta},\hat{\tau}\right) \end{bmatrix} \begin{bmatrix} \theta-\hat{\theta} \\ \tau-\hat{\tau} \end{bmatrix} \qquad 11\text{-}46$$

The modem must solve for a new estimate of θ and τ, which are recursively represented by $\theta-\hat{\theta}$ and $\tau-\hat{\tau}$. (Based on the previous estimates, we composed new values which adjusted according to the differences of Equation 11-45.) The actual solution requires the inversion of the matrix,

$$\begin{bmatrix} \theta-\hat{\theta} \\ \tau-\hat{\tau} \end{bmatrix} = \begin{bmatrix} \Lambda_{\theta\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\theta\tau}\left(\hat{\theta},\hat{\tau}\right) \\ \Lambda_{\tau\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\tau\tau}\left(\hat{\theta},\hat{\tau}\right) \end{bmatrix}^{-1} \begin{bmatrix} \Lambda_\theta(\theta,\tau) \\ \Lambda_\tau(\theta,\tau) \end{bmatrix} \qquad 11\text{-}47$$

The right-most term of Equation 11-47 corresponds to the partial derivatives of the log likelihood function, which would are required for synchronization even if we do not attempt a simultaneous solution. Heuristically, the matrix can be visualized as correcting for the correlation between symbol timing and carrier phase synchronization. Mathematically, Equation 11-46 can be solved at every symbol, and provide a new estimate of θ and τ to the respective VCOs. Meyers and Franks [11] note that the matrix is computed with channel noise and may present some numerical stability concerns.

They derive a tracking loop implementation that is based upon a linearized small-jitter estimation of Equation 11-47, [11]

$$\begin{bmatrix} \hat{\theta}_{m+1}-\hat{\theta}_m \\ \hat{\tau}_{m+1}-\hat{\tau}_m \end{bmatrix} - \left( I - \frac{1}{K_0} M \begin{bmatrix} \Lambda_{\theta\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\theta\tau}\left(\hat{\theta},\hat{\tau}\right) \\ \Lambda_{\tau\theta}\left(\hat{\theta},\hat{\tau}\right) & \Lambda_{\tau\tau}\left(\hat{\theta},\hat{\tau}\right) \end{bmatrix} \right) \begin{bmatrix} \Lambda_\theta(\theta,\tau) \\ \Lambda_\tau(\theta,\tau) \end{bmatrix} = M \begin{bmatrix} \delta_m \\ \sigma_m \end{bmatrix} \qquad 11\text{-}48$$

M is a 2 x 2 matrix that accounts for the step size and coupling in the carrier phase and symbol timing VCOs.

I is the 2 x 2 identity matrix

$K_0$ is the number of symbols used in the estimate

$\delta_m$ and $\sigma_m$ are zero-mean noise terms for $\Lambda_\theta(\theta,\tau)$ and $\Lambda_\tau(\theta,\tau)$

In order to de-couple the dynamics of the timing and carrier phase, it is desirable to choose the step size and other representation of M so that the

term, $I - \frac{1}{K_0} MJ$, (J represents the 2 x 2 matrix in Equation 11-48) is diagonal. It will correct for the correlation of the two estimates, but not couple the tracking dynamics. A block diagram of Meyers and Franks' tracking loop implementation is shown in Figure 11.19.

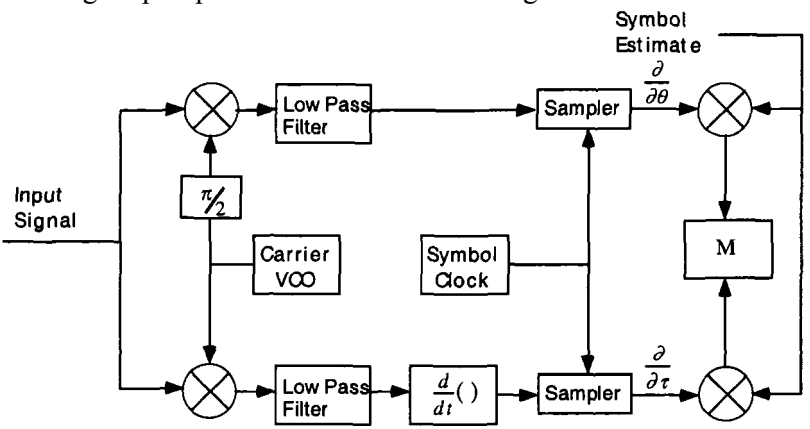


Figure 11.20 Joint Estimation Tracking Loop [11]

There are some practical problems with the joint estimation tracking loop. It is difficult to define loop bandwidths for the tracking loop in Figure 11.20. It is even more difficult to set independent loop bandwidths for the carrier and clock synchronization loops. (Which is typical requirement of SATCOM modems.) Also, the performance of Figure 11.20 may be disappointing. In one application, the author has found that independent carrier and clock loops out-performed the joint estimation loop. (Probably because of a local minima problem due to the approximations.)

Figure 11.21 shows the log likelihood surface of a CPM waveform. This surface is instantaneously dependent upon the data symbol and adjacent symbols, causing it to be data-dependent. For the surface in Figure 11.21, there is a well-defined maxima and the synchronization loops should be able to incrementally adjust the synchronization for optimum performance. However, some likelihood surfaces have the problem of local minima [12,18]. With such a likelihood surface, the synchronization variables will become "trapped" in a local minima. Because the phase-locked loop is a sequential estimate, seeking to minimize the first partial derivatives of Equation 11-47, the synchronizers can never escape a local minima in the multi-dimensional likelihood surface.

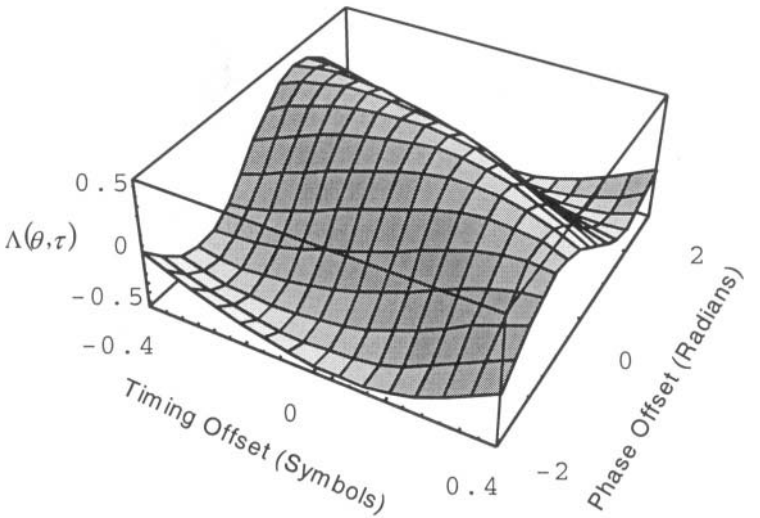


Figure 11.21 Multi-Dimensional Likelihood Surface

## 11.6. Interpolators

In some modem applications, the analog-to-digital converter may be operating independently of the modem, and the modem is required to "piece together" the appropriate A/D samples to perform symbol processing. Figure 11.22 shows a block diagram where a digital interpolator is used to provide symbol-referenced samples to the modem's processor. The modem's symbol timing synchronizer provides control to the interpolator, but the A/D and its implicit sampler is operating asynchronously with respect to the modem. The digital interpolator in Figure 11.22 can be providing more than one sample per symbol to the symbol processor. However, all of the samples are aligned to a symbol interval.

The basic problem in Figure 11.22 is how to obtain a fractional unit delay so that the symbol processor can perform optimum signal processing. A general primer on designing fractional unit delay filters is found in [33].

Gardner [14-15] has shown the interpolator can be analyzed as the hybrid configuration in Figure 11.23. The first A/D is operating asynchronously and produces digital samples, $x(mT_s)$ which are converted back to the analog domain with a digital-to-analog converter. Following the analog filter is another A/D which samples the data at a different rate, $T_i$, which in this case controlled by the modem. The second stage of Figure 11.22, (D/A -

Analog Filter - A/D) is not really necessary, because it can be performed with digital signal processing instead of the separate analog/digital steps shown.

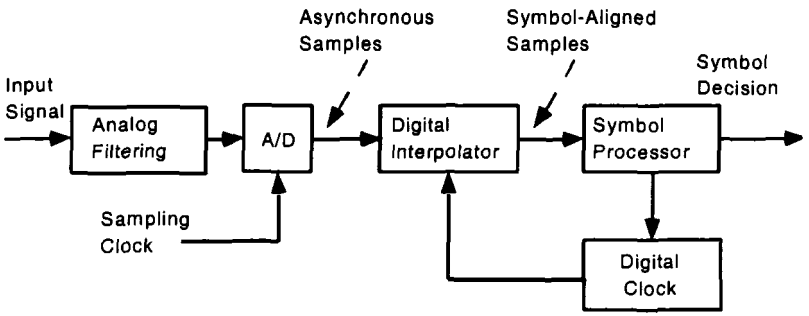


Figure 11.22 Interpolator in a Digital Modem

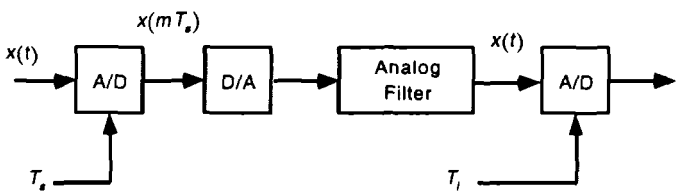


Figure 11.23 Analysis Concept of Interpolator [14]

The output, x(t), from the analog filter in Figure 11.23 is

$$x(t) = \sum_m x(m)h(t - mT_s) \qquad 11\text{-}49$$

where $h(t)$ is the analog filter's impulse response

The interpolants, $x(kT_i)$, can be obtained from the filter's time response function,

$$x(kT_i) = \sum_m x(mT_s)h(kT_i - mT_s) \qquad 11\text{-}50$$

By defining

$$m_k = \text{int}\left[\frac{kT_i}{T_s}\right]$$
$$\mu_k = \frac{kT_i}{T_s} - m_k \qquad 11\text{-}51$$

the output of the interpolator can be rewritten as [14]

$$x(kT_i) = \sum_{i=I_1}^{I_2} x[(m_k - i)T_s]h[(i + \mu_k)T_i] \qquad 11\text{-}52$$

The term $m_k$ represents a basepoint index, or the samples from the input A/D that are used by the interpolator to compute the output sample. The term $\mu_k$ represents a fractional input sample interval for the filter. The interpolator Equation 11-52, then represents a method for computing the re-sampled signal by using data samples from the input A/D, and offsetting the filter's impulse response with the fractional $\mu_k$.

The complete interpolator with control loop is shown in Figure 11.24. Note the loop error detector is generating one error correction per symbol, yet the digital interpolator may be operating at a much higher sampling rate. To analyze this loop for stability, it may be necessary to use the multi-rate sampling techniques developed in Chapter 6.

Gardner [14] developed an elegant control algorithm for the interpolator. The digital clock's difference equation is

$$\eta\ (m) = \{\eta\ (m-1) - W(m-1)\}_{\text{mod1}} \qquad 11\text{-}53$$

The control voltage from the loop filter $W(m)$, is nominally $W(m) \approx \frac{T_s}{T_i}$. The fractional interval is computed as

$$\mu_k = \frac{\eta\ (m_k)}{W(m_k)} \qquad 11\text{-}54$$

The interpolator filter is the most difficult aspect of the design. It is desirable to have a filter that does not require complex calculation of

coefficients for every $\mu_k$. As the modulation waveforms become more complex, it is desirable to minimize distortion which would degrade the modem's symbol estimation. Schafer and Rabiner published an early paper on digital interpolation [13], but their interpolation filters generally require too many computations for each new $\mu_k$.

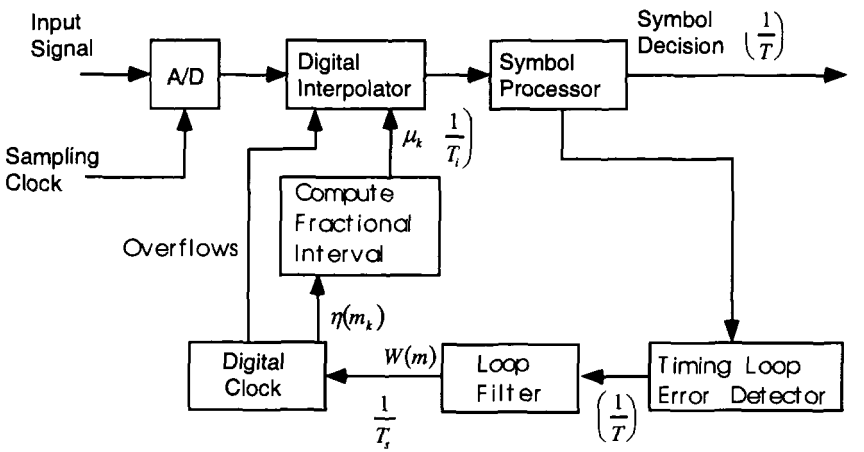


Figure 11.24 Interpolator With Control Loop [14]

Erup, et al., have analyzed several filters that require few computations for a new data sample [15]. From their research, a cubic polynomial filter is shown in Figure 11.25. This filter works best if it is used as a downsampler, otherwise the first sample after a symbol transition tends to have objectionable overshoot. The timing synchronization performance of Figure 11.17 was obtained with the cubic polynomial filter and the interpolator control algorithms of Equations 11-53 and 11-54.

The performance of digital interpolators in Rician-Fading channels was studied in [30]. For 0-2$^{nd}$ order interpolators, the BER degradation (dB) is approximately proportional with the 2$^{nd}$, 4$^{th}$, and 7.5$^{th}$ power of $T/T_s$. At sampling rates of $T/T_s > 4$, the BER degradation is less than 0.1 dB in AWG noise.

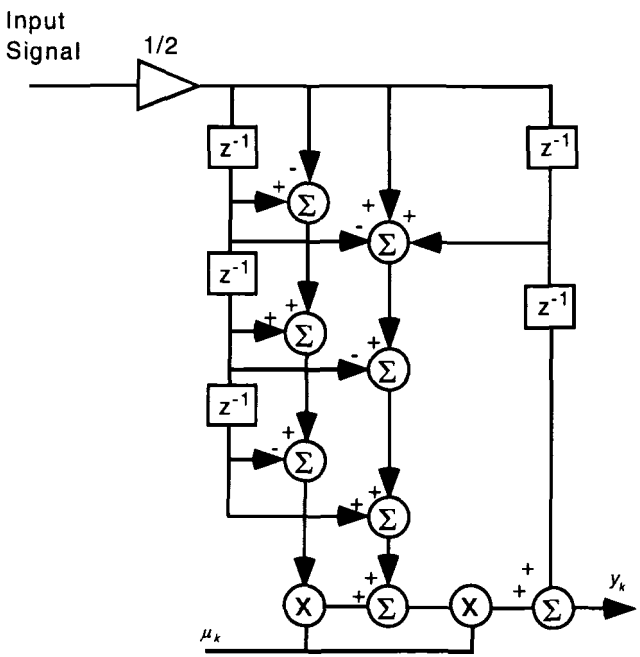


Figure 11.25 Cubic Farrow Interpolator [15]

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## 11.8. Problems

11.1 Graph the autocorrelation term, $R(\tau)$, for BPSK. (Equation 11-7). Consider the two cases of a) 11 and b) 10.

11.2 Design a Costas loop to perform the phase synchronization for a BPSK receiver. Assume the following parameters: Carrier Frequency= 200 MHz, Bit rate = 9,600 bits /sec, Input power to Phase Detector = $10^{-3}$ W, $K_{vco}$ =10 KHz/Volt, $K_d$ =lV/radian, Initial Frequency Offset =250 Hz, < 0.25 dB degradation at a BER = $10^{-6}$.

11.3 Design a Costas loop to perform the phase synchronization for a QPSK receiver. Assume the following parameters: Carrier Frequency= 200 MHz, Bit rate = 9,600 bits /sec, Input power to Phase Detector = $10^{-3}$ W, $\mathbf{K}_{vco}$ =10 KHz/Volt , $\mathbf{K}_d$ =1V/radian, Initial Frequency Offset =1200 Hz, < 0.5 dB degradation at a BER = $10^{-5}$

11.4 The data input to a phase detector using Gardner's timing algorithm is { 0.309017-j 0.951057 , 1, -0.309017 + j 0.951057, -1, 0.309017 –j 0.951057, 1, 1, 1, -0.309017 + j 0.951057, -1, -1, -1, 0.309017- j 0.951057, 1, -0.309017 +j 0.951057, -1, 0.309017 -j 0.951057, 1, 1, 1, -0.309017 +j 0.951057 , -1, -1, -1, -1, -1, -1, -1, -1, -1, 0.309017 -j 0.951057}. Graph the output of the detector. (Often the I and Q data are written in the complex form, $I + jQ$.)

11.5 Compute the squaring loss for a BPSK Costas loop for $0\,dB \le P/N_0\,B_i \le 15\,dB$.

11.6 A receiver is attempting to synchronize to a signal of the form, $s(t,\tau,\beta,\theta) = \beta\,Cos[2\pi f_0(t+\tau)+\theta]$. Assuming a decision-directed, maximum likelihood receiver, compute the estimator for $\beta$.

11.7 Design a BPSK timing synchronizer assuming the phase detector of Figure 11.17. The bit rate is 600 bps, and an input $E_b/N_0 = 9\,dB$. Specify the loop bandwidth such that the implementation loss for the synchronizer loop is less than 0.25 dB.

11.8 Assume the maximum likelihood detector for s(t) is obtained by taking the derivative of s(t) with respect to the parameter.

$$\text{Let } s(t) = \begin{cases} Cos\left[\dfrac{\pi(t+\tau)}{T}+\theta\right], & t+\tau \le \dfrac{T}{2} \\ Cos[\pi+\theta], & \dfrac{T}{2} \le t+\tau \le T \end{cases}$$

Plot the carrier phase detector's output at time t=0 for $-\pi/2 \le \theta \le \pi/2$ at: a) $\tau = 0$, b) $\tau = 0.25T$, c) $\tau = 0.50T$.

11.9 Plot the false lock frequency for a BPSK decision-aided carrier tracking loop operating a 1200 bps and a loop bandwidth of 10 KHz.

11.10 Graph the frequency response for the Cubic Farrow filter (Figure 11.21) for: a) $\mu_k = 0$, b) $\mu_k = 0.5$, and c) $\mu_k = 1.0$

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# 12

# Optical Phase-Locked Loops

## 12.1 The Applications of Optical Phase-Locked Loops

The laser was invented in 1960 [1], and since that time, different modulation techniques have been used to place information on the optical signal. Early optical transport layers used direct detection [2-3] in which the optical receiver simply determined whether a pulse was present. As technology has developed, modulation techniques have developed that allow much more of the optical fiber's 20 THz capacity to be used. Wavelength Division Multiplexing (WDM) [4] is one such technique that multiplexes multiple optical signals onto a single fiber.

Other techniques are possible such as heterodyne or homodyne detection of BPSK modulated signals [5]. In most of these advanced optical modulations, the phase noise of the laser's signal is critical and can limit capacity [6]. Many of the high-capacity systems now use optical phase-locked loops to control the line widths of the modulated (or unmodulated) laser lights.

In general, the optical phase-locked loop allows

- More optical signals on a single fiber (dense wavelength division multiplexing).

- Longer distances between repeaters in a long-haul cable.
- Higher data rates.

A different application of optical phase-locked loops is in optical beam forming networks for microwave antennas [20]. Precision amplitude and phase-controlled signals are applied to each individual element of a phase-array antenna to synthesize the desired antenna pattern. As the number of elements increases, it becomes physically impossible to provide coaxial cables to every element in the antenna. Coherent optical signals can be transmitted over fiber optics to the active antenna elements where they are converted to microwave signals.

## 12.2 A Simple Optical Phase-Locked Loop

Figure 12.1 shows a block diagram of a simple optical phase-locked loop. The reader soon concludes there is little difference between the analog phase-locked loops previously discussed and optical implementations. There are some differences as the lasers are typically modulated by a piezoelectric device, and the phase detector consists of an optical coupler and balanced photodiodes. These will be discussed shortly.

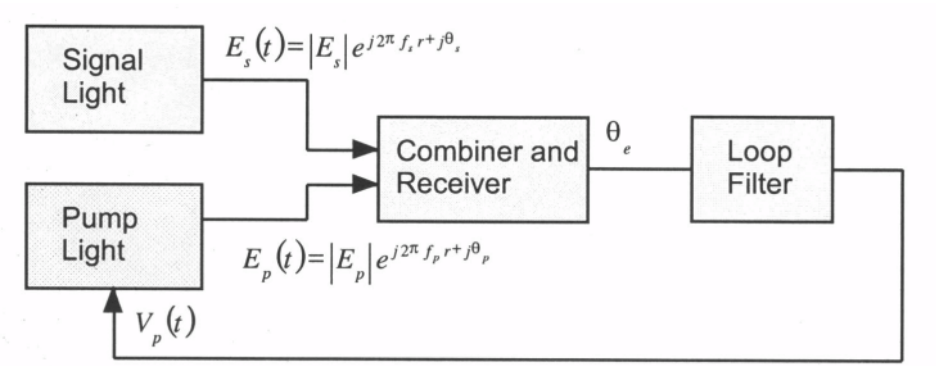


Figure 12.1 Simple Optical Phase-Locked Loop

Assuming we have optical source with phases $\theta_s$ and $\theta_p$ as shown in Figure 5.1, the phase difference between the two sources is expressed as:

$$\theta_e = \theta_p - \theta_s \qquad 12\text{-}1$$

## 12.3 Photodetectors

The fundamental principle for the operation of photodetectors and lasers is the change from one energy state to another. Recall Bohr's frequency relation [17]

$$E_2 - E_1 = h\nu_{21} \qquad 12\text{-}2$$

The atomic system is originally at energy state $E_2$ and transitions to energy state $E_1$ while emitting a photon of frequency $v$. In Equation 12-2, $h = 6.626 \times 10^{-34}$ $Js$ , Planck's constant, . The converse of Equation 12-2 describes the operation of a photodetector. A photon of the proper frequency will cause the atomic system to increase its energy state.

Figure 12.2 is a simple review of the p-n junction. We have two semiconductor materials such as phosphorus and boron forming a p-n junction. The phosphorus has an excess of electrons and is termed an n-type material. The boron has an excess of holes and is termed a p-type material. The n-type material will donate electrons and the p-type material will accept electrons.

The electrons near the junction will diffuse to the p-type material where they combine with a p-type hole, resulting in a negative charge for the accepting atom. This leaves the donor atom as a positive charge. (The electrons of the n-type material are called the majority carriers.)

At the same time, a p-type hole will likewise migrate across the junction and combine with an electron on the n-type material side, causing the acceptor atom to have a negative charge. The accumulation of charges generates a potential across the junction. This potential will now repels both the holes and electrons away from the boundary.

When the p-n junction is forward-biased, (positive terminal to the p-type material and negative terminal to the n-type material), electrons are forced into the n-type material and holes are forced into the p-type material. The presence of these additional electrons and holes neutralize the fixed charges and the junction potential decreases. This allows current to flow across the interface (junction).

Conversely, when the p-n junction is reverse-biased, (negative terminal to the p-type material), electrons are extracted from the n-type material and likewise holes are extracted from the p-type material. This effectively increases the charge distribution and increases the depletion region which

also increases the potential across the interface. No current due to the majority carriers can flow across the junction.

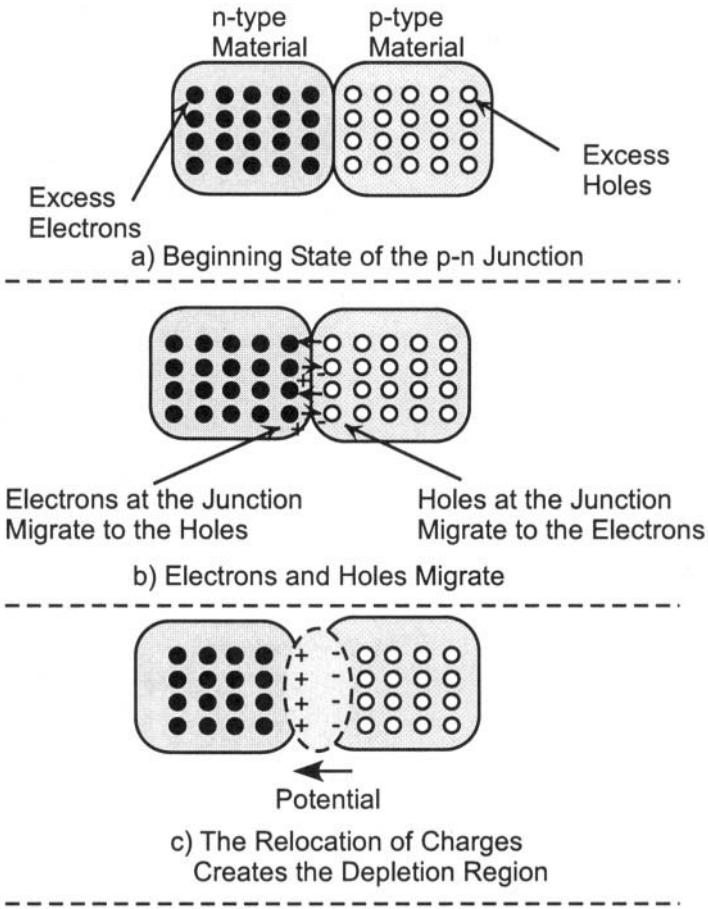


Figure 12.2 Simple p-n Junction

Figure 12.3 shows the operation of a photodetector. The photodetector has its p-n junction reverse-biased. If a photon with the energy *hv* corresponding to the band-gap energy of the p-n junction strikes the depletion region, an electron-hole pair is generated. The electron and hole will drift in opposite directions, creating a current equivalent to an electron charge, q. Because the p-n junction is reverse-biased, the current is created

external to the photodetector. The process of the depletion region converting a photon to an electron-hole pair is called absorption .

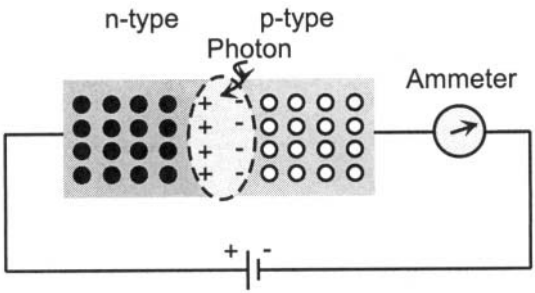


Figure 12.3 p-n Photodetector

A light source emits on average, [28]

$$\lambda_p \equiv \frac{P_s}{h\nu} \quad \text{photons/sec} \qquad 12\text{-}3$$

Where $P_s$ is the power of the light source. The photons arrive with a Poisson probability rather than a continuous distribution. Because of this random arrival, communication designers are interested in the probability of a specific number of photons arriving within a time interval. The number of photons is directly proportional to the current produced by the photodetector. The probability of N photons arriving in interval T is [28]

$$P_r(n = N) = \frac{(\lambda_p T)^N \; e^{-\lambda_p T}}{N!} \qquad 12\text{-}4$$

(As an aside, optical communication designers often specify the sensitivity of the system in units of photons/bit, just as non-optic modems are specified in Eb/No. Yamashita and Okoshi [29] provide a table of photons/bit to achieve a $10^{-9}$ BER for various modulation methods. They report 10 and 40 photons/bit required for homodyne PSK and ASK, respectively.)

The p-n junction may be slow to respond to a photon because many of the photons strike either the n-type or p-type material directly instead of the depletion region. These electron-hole pairs must subsequently diffuse to the depletion region. Higher speed photodetectors are created by placing an intrinsic layer between the n-type and p-type material at the interface. This allows more of the photons to directly strike the depletion region directly.

These photodetectors with an intrinsic layer are known as p-i-n detectors and are typically used for fast detector/receiver systems. Yet another variation is to sandwich another layer in the interface that effectively multiplies the number of electron-hole pairs created for every photon received. These are called avalanche photodetectors. Although they generate more current than a p-i-n photodetector, they also create more noise [19]. Typical multiplication ratios are 30-100 [28].

The photodetector previously described has a sensitivity determined by the absorption coefficient, $\alpha$, of the device material. (The absorption length, $1/\alpha$, is the thickness required to reduce the incident light intensity by $1/e$.) The absorption length of most detectors is a function of wavelength, so it is necessary to match the absorption length to a particular wavelength. For example, Silicon has an absorption length of approximately $14\ \mu m$ at the important GaAs laser wavelength of 850 nm. At the other common laser wavelength of 1300 nm, Germanium is the material of choice with an absorption length of approximately $1.2\ \mu m$.

The electron-hole pairs generated during absorption will recombine even in the absence of an electric field. The carriers generated in the electric field will be collected as a photocurrent [14]. Assuming that the substrate is the dominant source of diffusive transport, the photocurrent in the detector is computed as [14]

$$i = P_{inc}\,\rho \qquad 12\text{-}5$$

$$\rho = \frac{\eta e}{h\nu}(1-R)\left[1-\frac{e^{-\alpha W}}{1+\alpha L_n}\right] \qquad 12\text{-}6$$

where $1-e^{-\alpha W}$ is the fractional light intensity absorbed in the detectors' junction with depletion width W, $R$ is the reflection coefficient, $L_n$ is the

minority carrier diffusion length for electrons in the p-substrate, $hv$ is the photon energy, and $\eta$ is the internal quantum efficiency. The minority carrier diffusion length is expressed as $L_n = \sqrt{D_n \tau_n}$ where $\tau_n$ is the minority carrier lifetime and $D_n$ is the diffusion constant.

As an example, assuming 100% absorption and 0% reflectivity, the detector sensitivity is 0.69 A/W at 850 nm, while at 1550 nm, the detector sensitivity can be 1.25 A/W [14]. (This is one reason why long-haul transmission is preferred at the longer laser wavelengths.)

## 12.4 Mixing With Photodetectors

### 12.4.1 The Homodyne Advantage

Equation 12-5 showed that the photodetector's output current is directly proportional to the incident light power. If two signals are simultaneously incident upon the photodetector, then the sum and difference signals will be detected and converted to an electronic current.

To introduce the concept of photo-mixing, consider the block diagram of Figure 12.4. Our discussion will follow that of Oliver in [16]. There are two light sources that are ½ reflected, ½ transmitted through the beam splitting mirror. The reflection and transmission coefficients are assumed to be $\frac{1}{\sqrt{2}} e^{j\frac{\pi}{4}}$ and $\frac{1}{\sqrt{2}} e^{-j\frac{\pi}{4}}$, respectively. Suppose that the phase offsets of the two lights are such that the instantaneous powers can be written as

$$P_s = \left\{A_s \, Cos\left(2\pi f_s t + \tfrac{\pi}{4}\right)\right\}^2 \qquad 12\text{-}7$$

$$P_o = \left\{A_o \, Cos\left(2\pi f_s t - \tfrac{\pi}{4}\right)\right\}^2 \qquad 12\text{-}8$$

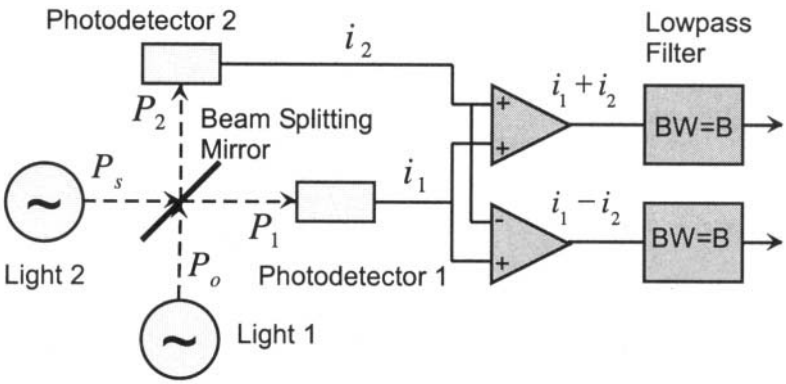


Figure 12.4 Photo-Mixing Example

Similar to electronic mixing, the signals incident upon the photodetectors can be computed as

$$P_1 = \frac{1}{2}\left(A_O\, Cos(2\pi f_O t) + A_s\, Cos(2\pi f_s t)\right)^2 \qquad 12\text{-}9$$

$$P_2 = \frac{1}{2}\left(A_O\, Sin(2\pi f_O t) - A_s\, Sin(2\pi f_s t)\right)^2 \qquad 12\text{-}10$$

From Equations 12-5 the currents from the photodetectors are written as

$$i_i = \frac{\eta q}{h\nu} P_i \qquad 12\text{-}11$$

If we assume the sum frequencies of $f_O$ and $f_s$ are either filtered out optically or beyond the bandwidth of the photodetectors, then the output current sum signal of Figure 12.4 is computed as

$$i_\Sigma \equiv i_1 + i_2 = \frac{\eta q}{2h\nu}\left(A_O^2 + A_s^2\right) \qquad 12\text{-}12$$

An actual optical mixer would not use the current sum above, but we compute it in anticipation of needing it later to compute the signal-to-noise. Our real term of interest is the difference signal which is computed as

$$i_\Delta \equiv i_1 - i_2 = \frac{\eta q}{h\nu} A_O \, A_s \, Cos\left(2\pi\left(f_s - f_O\right)t\right) \qquad 12\text{-}13$$

The mean square value of Equation (12-13) is proportional to the actual signal power.

$$\bar{i}_\Delta^2 = \left(\frac{\eta q}{h\nu}\right)^2 \frac{A_O^2 \, A_s^2}{2} \qquad 12\text{-}14$$

After the filters with noise bandwidth $B$, the shot noise is computed as

$$\bar{i}_n^2 = 2qBi_\Sigma = \frac{\eta q^2 B}{h\nu}\left(A_O^2 + A_s^2\right) \qquad 12\text{-}15$$

The ratio of the two previous equations yields the signal-to-noise ratio for the optically downconverted signal.

$$SNR = \frac{\eta}{h\nu B} \frac{A_O^2 \, A_s^2}{A_O^2 + A_s^2} \qquad 12\text{-}16$$

The SNR of the downconverted signal is a function of the receiver's noise bandwidth B, which we would anticipate. Note however, that it is also a function of the local oscillator's input power, $A_O^2$. If we assume an unlimited local oscillator power and take the limit of Equation (12-16), we obtain the maximum signal-to-noise ratio [17].

$$SNR_{\max} = \underset{A_O \to \infty}{Limit} \quad \frac{\eta}{2h\nu B} \frac{A_O^2 \, A_s^2}{A_O^2 + A_s^2} = \frac{\eta}{h\nu B} \frac{A_s^2}{2} \qquad 12\text{-}17$$

The last term, $A_s^2/2$, represents the incident optical signal power. Suppose that we have homodyne conversion, where the frequencies of the

input and local oscillator are exactly the same, i.e., $f_s = f_O$. In this case, the term in Equation (12-13), $Cos(2\pi(f_s - f_O)t) \rightarrow 1$. As a consequence, the mean square power of Equation 12-14 increases by a factor of 2. (Recall $\{A\,Cos(\theta)\}^2 = 1/2 + Cos(2\theta)$). For homodyne conversion,

$$SNR_{\max,\text{homodyne}} = \frac{\eta A_s^2}{h\nu B} \qquad 12\text{-}18$$

Equation 12-18 demonstrates that optical homodyne detection is better than heterodyne detection (where the frequencies of the input and local oscillator are not the same) by 3 dB. This is true where the local laser intensity noise is negligible. If not, then the sensitivity can be significantly reduced [39].

This result is different from the phase-locked loops we have discussed previously where the noise enters with the signal and the additional conversion gain does not affect the SNR. One insight is that in microwave signals, the noise is added prior to mixing, whereas the noise is added after the mixer in optical mixing. See [28] for additional discussion on why microwave signals do not incur a heterodyne penalty, in contrast to optical mixing.

### 12.4.2 The Dual Detector Advantage

Although we did not discuss it earlier, the dual detector configuration of Figure 12.4 has been empirically observed to provide up to 6 dB of improved receiver sensitivity [19]. The dual detector, also called a balanced receiver suppresses the local oscillator intensity noise.

Our approach will be similar to [21]. We convert Figure 12.4 into the flow graph shown in Figure 12.5. The transmission and reflection coefficients are exactly the same – we simply show them as phase shifts in the flow diagram. We assign unknown phases $\phi_s$ and $\phi_O$ to the signal and local oscillator lights, respectively.

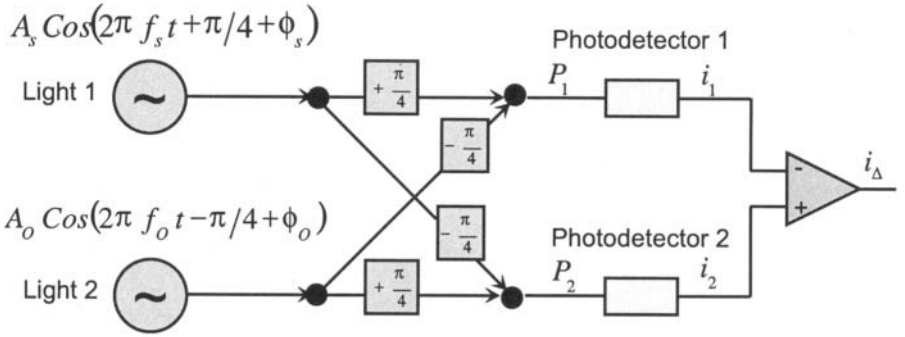


Figure 12.5 Flow Diagram of the Dual Optical Detector

From Figure 12.5, we can write the powers at the photodetectors as

$$P_1(t)=\frac{A_O^2}{2}Cos(4\pi f_O t+2\phi_O)-\frac{A_s^2}{2}Cos(4\pi f_s t+2\phi_s)$$
$$+A_O A_s Sin(2\pi t(f_O-f_s)+\phi_O-\phi_s) \qquad 12\text{-}19$$
$$-A_O A_s Sin(2\pi t(f_O+f_s)+\phi_O+\phi_s)+\frac{A_O^2+A_s^2}{2}$$

$$P_2(t)=-\frac{A_O^2}{2}Cos(4\pi f_O t+2\phi_O)+\frac{A_s^2}{2}Cos(4\pi f_s t+2\phi_s)$$
$$-A_O A_s Sin(2\pi t(f_O-f_s)+\phi_O-\phi_s) \qquad 12\text{-}20$$
$$-A_O A_s Sin(2\pi t(f_O+f_s)+\phi_O+\phi_s)+\frac{A_O^2+A_s^2}{2}$$

Recall from Equation 12-5 that the induced photocurrent, $i \propto P$. Then the single-ended equations, 12-19 and 12-20, are susceptible to variations in the incident light power. Specifically the term, $(A_O^2+A_s^2)/2$, will affect the photodetector's output current. When we compute the difference current, we eliminate the susceptibility to the intensity fluctuations.

$$i \propto -A_O^2\,Cos(4\pi f_O t+2\phi_O)+A_s^2\,Cos(4\pi f_s t+2\phi_s)$$
$$-2\,A_O A_s Sin(2\pi t(f_O-f_s)+\phi_O-\phi_s) \qquad 12\text{-}21$$

There are multiple techniques to implement the dual detector [31]. The differential amplifier can be used as shown in Figure 12.5. Another

technique is 0°-180° microwave hybrid driving a conventional single-ended amplifier. Still another approach is biasing the photodetectors between opposite polarity voltages and again driving a single-ended amplifier.

A similar analysis can be performed for multiple signals in the channel [40]. The cross-channel interference currents at the photodetectors can generate harmful interference and it concluded that single-detector receivers should not be used for homodyne detection [40].

## 12.5 Photoreceivers

Receiver sensitivity is determined by the equivalent noise current at the circuit input. It can be expressed as [11]

$$\overline{P} = \frac{1}{\eta}\frac{h\nu}{q} Q\sqrt{i_n^2} \qquad 12\text{-}21$$

where $\eta$ is the photodiode external quantum efficiency, $h$ is Planck's constant, $\nu$ is the incident light frequency, $Q$ is the signal-to-noise ratio, $i_n^2$ is the receiver's equivalent mean-square noise current, and $q$ is the electronic charge constant.

The equivalent input noise current is dependent upon both the fabrication process and the circuit topology [14]. An example MOS transimpedance amplifier has a noise current of [11]

$$i_n^2 = \frac{4kT}{R_f} I_2 B_r + \frac{4kT}{g_m} (2\pi C_T)^2 I_3 B_r^3 \qquad 12\text{-}22$$

where $k$ is Boltzmann's constant, $T$ is the device temperature, $R_f$ is the amplifier's feedback resistor, $I_2$ is a normalized noise-bandwidth integral, $B_r$ is the bit rate, $g_m$ is the amplifier's transconductance, $\Gamma$ is the FET's channel noise factor, $C_T$ is the total input capacitance, $I_3$ is a normalized noise-bandwidth integral.

Figure 12.6 shows a block diagram of a typical photoreceiver amplifier. The inductor after the photodiode peaks the bandwidth and signal-to-noise of the photodetector. Instead of the single photodiode detector shown in Figure

12.6, the dual-detector balanced optical receiver is preferred for coherent detection.

Somewhat surprising to electronic PLL designers is the concept of signal-to-noise ratios in photoelectric mixing. The total noise power spectral density of an amplifier can be written as [16]

$$S_n(\nu) = \frac{h\nu}{Exp\left(\frac{h\nu}{kT}\right) - 1} + h\nu \qquad 12\text{-}23$$

where $h$ is Planck's constant, $\nu$ is the incident light frequency, $k$ is Boltzmann's constant, and $T$ is the device temperature.

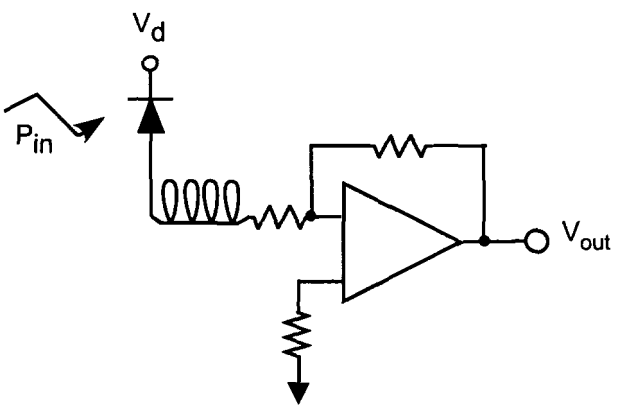


Figure 12.6 Schematic of Photodetector Amplifier[12]

The first term in Equation (12-23) is due to thermal noise (black body radiation) whereas the second term is from quantum effects. At optical frequencies, $h\nu >> kT$, which causes the thermal noise term to vanish, and $S_n \rightarrow h\nu$. For an optical signal of power $P_s$, and passband of bandwidth B, we can compute the signal-to-noise ratio as [16]

$$\frac{S}{N} = \frac{P_s}{\int_{\nu-B/2}^{\nu+B/2} S_n(\varsigma)\,d\varsigma} = \frac{P_s}{h\nu B} \qquad 12\text{-}24$$

Commercial opto-electronic integrated circuits (OEIC) are fundamental to the success of lightwave systems. A key component in OPLLs is a monolithic photoreceiver incorporating a photodiode and a low noise preamplifier. The process technology for photoreceivers is advancing rapidly and a detailed discussion of a component would soon be obsolete. The reader is referred to papers such as [9-14] for fabrication details.

## 12.6 Lasers

Equation 12-2 was used for describing how photodetectors convert a photon into electrical current. A laser operates by pumping the energy of the atomic system to a higher state, and when the system transitions to the lower level, a photon corresponding to the particular energy change is released. Additional photons are released in a positive-feedback manner because as they strike other atoms, additional photons are released. Hence, the acronym, Stimulated Emission of Radiation, LASER.

Besides Equation 12-2, another important relation for a laser is the Boltzmann ratio,

$$\frac{N_2}{N_1} = \exp\left(\frac{-(E_2 - E_1)}{kT}\right) \qquad 12\text{-}25$$

$N_2$ and $N_1$ are the numbers of atoms at atomic energy states $E_2$ and $E_1$, respectively. $k$ is Boltzmann's constant, $1.381\times10^{-23}\ J/°K$, and T is the temperature of the material in $°K$.

The energy gap, $(E_2 - E_1)$ corresponds to the photon energy, $h\upsilon$, from Equation 12-2. If the energy gap is much greater than $kT$, then at thermal equilibrium, there are very few atoms at energy level $E_2$. The selection of

materials and physical construction of the laser is required to invert this ratio, $N_2/N_1$, such that amplification of photons is possible. (In actuality, lasers use several energy levels – see [22].)

The early lasers utilized a semiconductor rod with polished mirrors on each end. One of the mirrors was 20-30% transmissive, and allowed the laser light to be emitted. The material (at first, ruby) was pumped to a higher energy level by flashtubes wrapped around the laser rod. The resonating cavity for the laser was adjusted with piezo mirrors as discussed in Chapter 1 and depicted in Figure 1.4.

The basic laser design for optical communications is the Fabry-Perot. Similar to the p-i-n diode, it consists of three layers as shown in Figure 12.7.

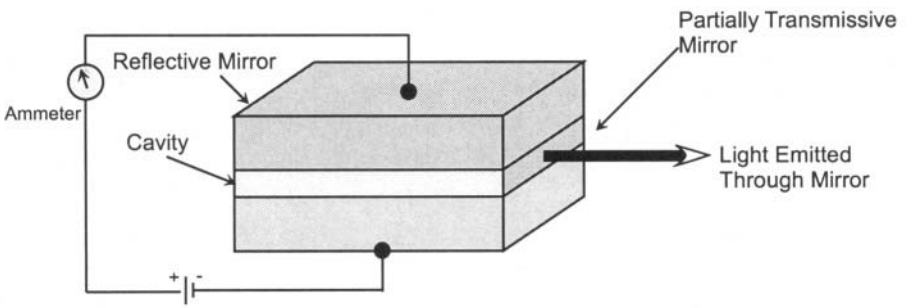


Figure 12.7 Fabry-Perot Laser

In Figure 12.7, the outer layers are special semiconductors such as InGaAs and InP, with a center or active layer of InGaAsP [23]. When current is flowed between the outer layers, light is emitted in the active layer. Light will propagate along the inner layer until it reflects against the mirror and passes through the center layer again. Because the laser is an inverted population state, the photons will strike other atoms, releasing even more photons. One of the end mirrors is semi-transmissive and allows some of the laser light out of the diode, while reflecting the majority of the light back into the active layer.

The Fabry-Perot laser is considered to be a single wavelength laser, but there is actually quite a spread in the optical frequency output. For this

reason, distributed feedback lasers are a preferred modification of the Fabry-Perot laser.

Figure 12.8 shows the modification to the Fabry-Perot laser. A corrugated layer is placed above the laser's active layer. By selecting the refractive index of the corrugate layer and spacing for a particular wavelength, it is the only optical frequency that will be reflected back into the active channel. The other optical frequencies will pass through the corrugated layer and not stimulate the emission of additional photons.

Because the output frequency is determined by the refractive index and physical fabrication, the distributed feedback laser is much less sensitive to temperature variations. The laser of [24] was measured to have a temperature sensitivity of $0.05 nm/°C$. To place this in perspective for electronic phase-locked loop designers, at the nominal 650 nm operating wavelength, this is about 35.5 GHz/°C. (A Fabry-Perot laser has about 3× greater temperature sensitivity.)

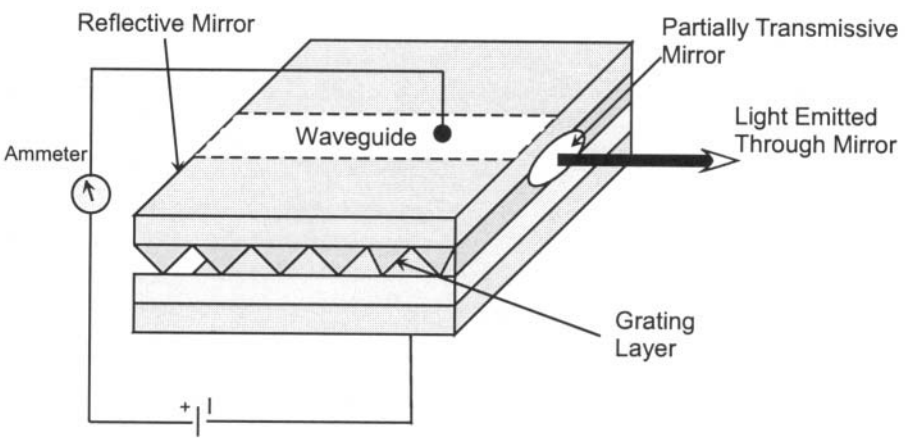


Figure 12.8 Distributed Feedback Laser

For optical phase-locked loops, the ring laser offers a much reduced temperature dependency. The ring laser of [7] has a temperature sensitivity 50 times less than a typical distributed feedback laser. Figure 12.9 shows the configuration of a semiconductor ring laser.

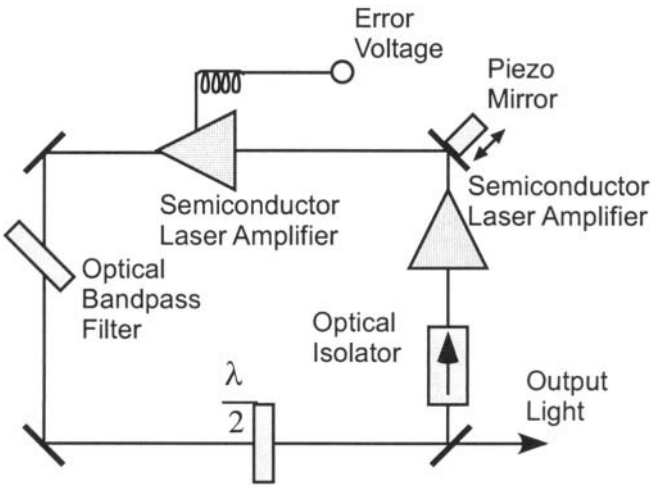


Figure 12.9 Semiconductor Ring Laser

The semiconductor laser amplifiers in Figure 12.9 are very similar to a laser itself – the fundamental difference is the absence of resonating cavity. (Actually that isn't quite true. One type of amplifier called the traveling wave amplifier does have a cavity, but the mirror transmits most of the light rather than reflecting it as in a laser.) With the applied current, the atomic systems have a inverted population (Equation 12-25) that will cause the release of additional photons when a photon enters the amplifier.

The optical bandpass filter is used to perform coarse tuning adjustments of the laser's output frequency. The piezo-mirror and the current into the upper laser amplifier provide the fine tuning adjustment.

## 12.7 Optical Phase-Locked Loops

### 12.7.1 Homodyne Loops

The homodyne loop is the most conceptually simple optical phase-locked loop. (However because of the temperature sensitivity discussed in Section 12.4, a homodyne loop is very difficult to implement.) In Figure 12.10, the OPLL generates negative feedback currents or voltages to adjust the local laser to exactly the same frequency as the input laser. This block diagram is similar to those presented earlier for electronic phase-locked loops except for the loop delay element.

In Figure 12.10, we have designated specific transfer functions for the local laser and photodetector. The local laser can have a modulation transfer function similar to a lowpass filter, or surprisingly, a bandpass response.

In our example, we will assume that the photodetector's transfer function is a simple scaler, but like the electronic phase-locked loops, it will be a linear approximation of the actual sinusoidal characteristic.

Although we discussed modeling of time delays for conventional phase-locked loops (See 3.2 Propagation Delays in PLLs), most of our analysis and examples neglected such a delay. Due to the higher frequencies and bandwidths of OPLLs, however, the loop propagation delay becomes important and must be considered. Several papers in the literature are concerned principally with the integration and fabrication of the various loop components in order to reduce the loop propagation delay. In the literature, a value such as 5 ns is typical [15].

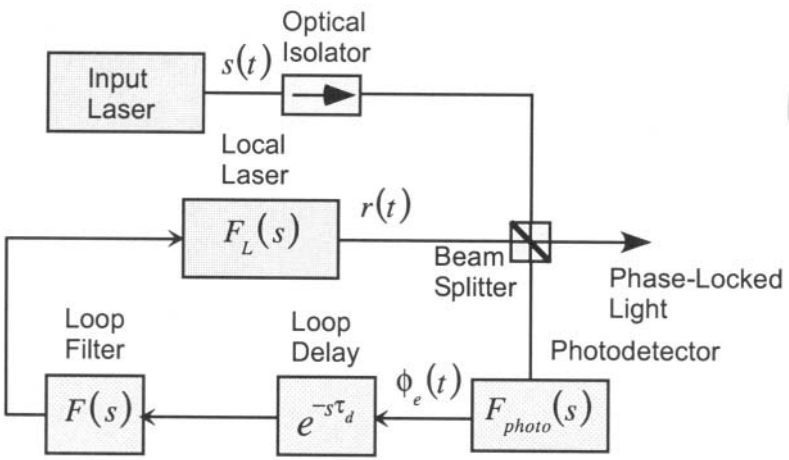


Figure 12.10 Diagram of Homodyne Optical PLL

In our analysis, we assume that the input and local laser outputs can be represented as

$$s(t) = Cos(2\pi f_s t + \phi_s(t)) \qquad 12\text{-}26$$

$$r(t) = Sin(2\pi f_r t + \phi_r(t)) \qquad 12\text{-}27$$

We let the error detected by the photodetector be represented as

$$\phi_e(t) = \phi_s(t) - \phi_r(t) \qquad 12\text{-}28$$

From Figure 12.8 and Equations (26-28), we can express the loop's transfer function as

$$H_O(s) \equiv \frac{\phi_s(s)}{\phi_r(s)} = \frac{F_{photo}(s) \times e^{-s\,t_d} \times F(s) \times F_r(s)}{1 + F_{photo}(s) \times e^{-s\,t_d} \times F(s) \times F_r(s)} \qquad 12\text{-}29$$

If we substitute $F_r(s) = K_o / s$ and $F_{photo}(s) = K_d$, the loop transfer function appears very similar to our previous developments.

$$H_O(s) = \frac{K_O\, K_d \times e^{-s\,t_d} \times F(s)}{s + K_O\, K_d \times e^{-s\,t_d} \times F(s)} \qquad 12\text{-}30$$

The condition for unconditional stability can be solved as [30]

$$\omega_n \tau_d < \frac{PV\left\{2\zeta \tan^{-1}\left(\zeta^2 \left(1 + \left(1 + (4\zeta)^{-4}\right)^{1/2}\right)^{1/2}\right)\right\}}{\zeta^2 \left(1 + \left(1 + (4\zeta)^{-4}\right)^{1/2}\right)^{1/2}} \qquad 12\text{-}31$$

In Equation 12-31, PV represents the Principal Value of the function.

For the common case of $\zeta = 0.707$, [30]

$$\omega_n \tau_d < 0.736 \qquad 12\text{-}32$$

## *Example 12.1 OPLL*

Design an optical phase-locked loop with a laser (VCO) tuning gain of 520 *KHz/V*, and a modulation bandwidth of 500 *KHz*. The received signal power is 0.06 $\mu W$, and the local oscillator power is 1 mW. The responsivity of the detectors is 0.7 A/W. Design for a loop natural frequency of 9 kHz, with a damping factor of 0.707.

| Symbol | Description | Value |
|---|---|---|
| $K_O$ | Piezo-electric Tuning Constant | $520\ KHz/V$ |
| R | Receiver Load Impedance | $2.2K\ \Omega$ |
| $\beta$ | Photodetector Responsivity | $0.7\ A/W$ |
| $P_s$ | Received Light Power | $0.06\ \mu W$ |
| $P_{LO}$ | Local Oscillator Power | $1\ mW$ |
| G | Instrumentation Amplifier Gain | 40 dB |

Design the passive lead-lag filter for this homodyne system. We desire a filter of the form, $F(s)=\dfrac{\tau_2 s+1}{\tau_1 s+1}$. Our solution follows that of [25].

The total phase detector gain is computed as

$$K_d = 2\times R\times\beta\times\sqrt{P_s\,P_{LO}}\quad V/rad \tag{12-33}$$

$$\begin{aligned} K_d &= 2\times 2200\times 0.7\times\sqrt{6\times10^{-8}\times1\times10^{-3}} \\ &= 0.0239\ V/rad \end{aligned} \tag{12-34}$$

$$K_{dc} = 2\pi\times K_O\times K_d\times G \tag{12-35}$$

$$\begin{aligned} K_{dc} &= 2\pi\times520\times10^3\times0.0239\times10^{40/20} \\ &= 1.7005\times10^7 \end{aligned} \tag{12-36}$$

To compute the passive loop filter, we modify Equation 2-66. Recall the scalar $\sqrt{2P}$ was included for multiplicative-type phase detectors or where the power was not implicitly included in the phase detector's gain. In this example, we included the optical incident power in the computation of Equation 12-33.

The first loop filter coefficient is obtained from a modification of Equation 2-66,

$$\tau_1 = \frac{K_{dc}}{\omega_n^2} = \frac{1.7005\times10^7}{\left(2\pi\times9\times10^3\right)^2} = 0.0024 \qquad 12\text{-}37$$

The second loop filter coefficient is obtained from a similar modification to Equation 2-66,

$$\tau_2 = \frac{2\xi\sqrt{K_{dc}\,\tau_1} - 1}{K_{dc}} = \frac{2\times0.707\times\sqrt{1.7005\times10^7\times0.0024} - 1}{1.7005\times10^7} \qquad 12\text{-}38$$

$$= 2.488\times10^{-5}$$

Figure 12.11 shows the root locus and Bode analysis of our design. It has over 65 degrees of phase margin, which should provide good performance. It is relatively insensitive to loop delay, as values of 40 ns contribute little change to the analysis shown in Figure 12.11.

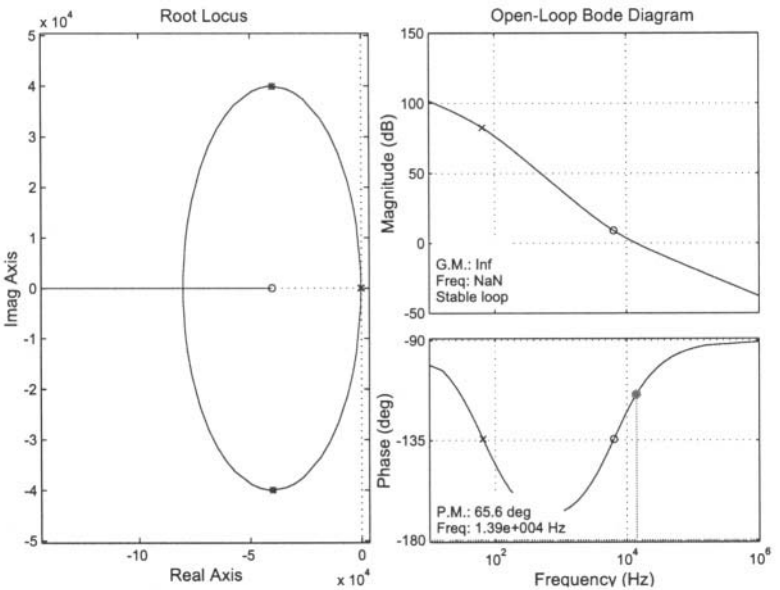


Figure 12.11 Root Locus and Bode Analysis of the OPLL

### 12.7.2 Heterodyne Loops

The large laser temperature sensitivities make homodyne loops extremely challenging. Heterodyne architectures allow the use of Automatic Frequency Control (AFC) loops which are less sensitive to the laser frequency drift. Figure 12.12 shows one configuration of heterodyne optical loops. The received optical signal has some form of digital data modulation such as ASK, BPSK, FSK, etc.

The local laser and received signal are not tuned to the same frequency as in a homodyne loop. In a heterodyne loop, the lasers are tuned to provide a difference frequency when mixed together. The photodetector/receiver is a wide bandwidth device, because the Intermediate Frequency (IF) frequency is typically several GHz. In general, the IF center frequency and bandwidth must be at least double the data modulation's bit rate [26].

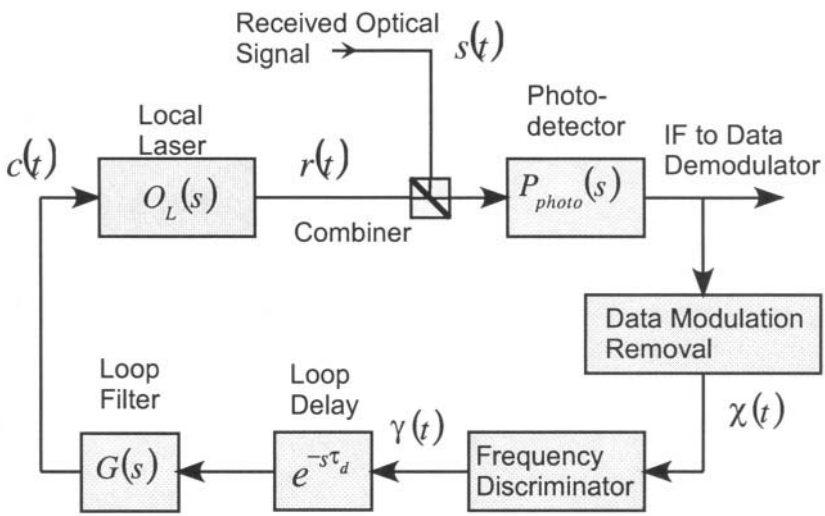


Figure 12.12 Optical Heterodyne Loop

Figure 12.12 is identical in principle to the modulation-remodulation (mod-remod) loops discussed in Chapter 11. Recall the carrier and symbol synchronization loops required the data modulation to be removed so that conventional phase-locked loops could adjust the synchronization error to zero. The same concept applies to the optical heterodyne loop. A squaring

or Costas circuit is used to remove the instantaneous phase modulation imposed by BPSK [38].

It is certainly possible to implement a heterodyne loop such as Figure 12.12 with a phase-locked loop despite the large increase in complexity. The frequency discriminator would be replaced with a phase detector. The analysis of such a loop would follow that shown earlier for the homodyne loop. In the analysis that follows, we assume the heterodyne loop is concerned only with Automatic Frequency Control (AFC), and the loop is adjusting the local laser's frequency to maintain a constant frequency separation with the incoming signal.

A frequency discriminator is used instead of a phase detector for frequency controlled loops [35-37]. The frequency discriminator can have several different topologies. Although the IF frequency is several GHz, traditional filter-type discriminators have been developed for optical communications [27]. Designed for a specific center frequency, $f_0$, the discriminator generates an output referenced to the center frequency of the discriminator.

Figure 12.13 shows an example frequency discriminator characteristic. At the discriminator's center frequency, the output voltage is zero. The monotonic segment between input frequencies $[f_0 - \nu, f_0 + \nu]$ is used control the laser. The scalar $K_d$ accounts for the gain of the specific discriminator, and $\nu$ represents the maximum input frequency offset for a monotonic output. The output voltage of the discriminator can be written as [35]

$$e(t) = \frac{K_d (f - f_0)}{1 + \left( \frac{f - f_0}{\nu} \right)^2} \qquad \text{12-39}$$

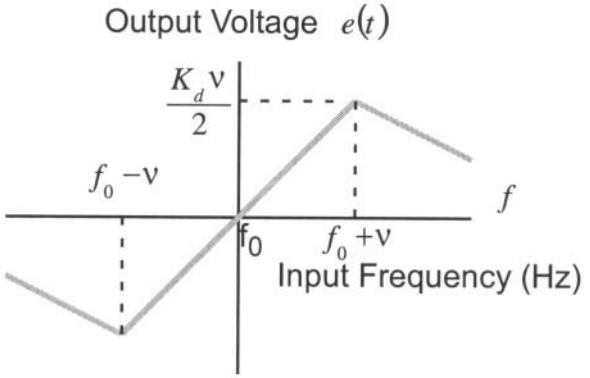


Figure 12.13 Frequency Discriminator Characteristic

To simplify our analysis, assume that we have a local laser controlled by the frequency discriminator as shown in Figure 12.14. The laser's output frequency is referenced to the discriminator's center frequency, $f_0$. If the local laser's frequency is different than the discriminator's $f_0$, then an error voltage $e(t)$ is generated. The error voltage is processed by the loop filter before applying it to the laser's control input.

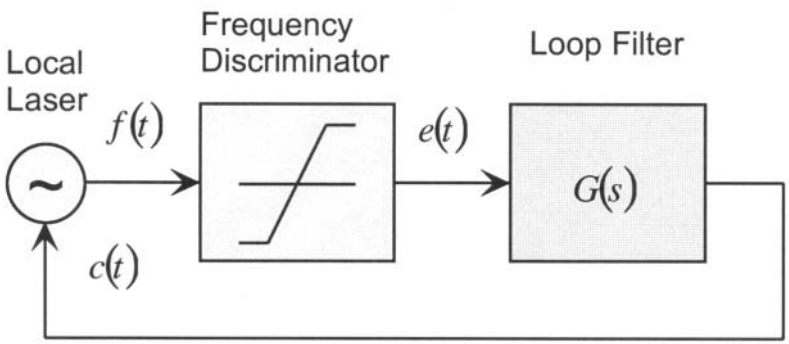


Figure 12.14 Simple AFC Loop

The laser's control equation is written as

$$c(t) = e(t) * g(t) \qquad 12\text{-}40$$

By substituting in the frequency discriminator's characteristic, we obtain

$$c(t) = \frac{K_d\,(f(t) - f_0)}{1 + \left( f(t) - f_0 \big/ \nu \right)^2} * g(t) \qquad 12\text{-}41$$

As with phase-locked loops, the simplest filter is a constant gain, $K_f$. If we include the laser's tuning constant, $K_o$, we can write the laser's output frequency for the gain-only loop filter as

$$f(t) = f_0 + K_o\, c(t) = f_0 + \frac{K_o\, K_f K_d\,(f(t) - f_0)}{1 + \left( f(t) - f_0 \big/ \nu \right)^2} * g(t) \qquad 12\text{-}42$$

It can be shown for this simple loop that stable frequency control is available only over the range [35]

$$\nu\left(1 + \frac{K_d\, K_f}{2}\right) \geq |f - f_0| \geq 2\nu\sqrt{K_d\, K_f - 3} \qquad 12\text{-}43$$

In general, the dynamic loop transfer function of the loop in Figure 12.12 is written as

$$H(f) = \frac{K_o\, K_d(f) G(f)}{1 + K_o\, K_d(f) G(f)} \qquad 12\text{-}44$$

where $K_d(f)$ represents the actual discriminator function. The 3-dB bandwidth of Equation 12-44 is defined as the closed-loop bandwidth.

This simple analysis does not consider the noise transformed by the frequency discriminator. Our more detailed analysis is similar to that of Bononi, et.al., [32]. Refer to Figure 12.15 for the position of the various signals to be computed.

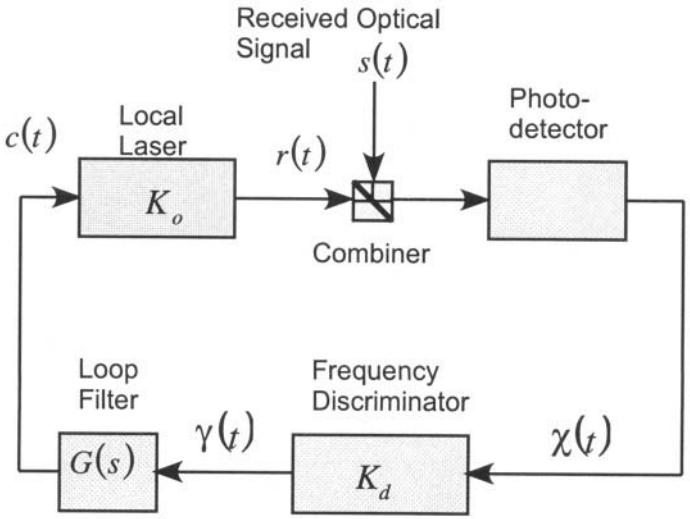


Figure 12.15 AFC Loop for Noise Analysis

Similar to the homodyne loop analysis, we model the signal and local oscillator laser signals respectively as

$$s(t) = \sqrt{2P_s}\, Cos(2\pi f_s t + \phi_s(t)) \qquad 12\text{-}45$$

$$r(t) = \sqrt{2P_r}\, Sin(2\pi f_r t + \phi_r(t) + \phi_c(t)) \qquad 12\text{-}46$$

In the equations above, $P_s$ and $P_r$ represent the optical powers of the two signals. Likewise, the phase of these optical signals is represented by $\varphi_s(t)$ and $\phi_r(t)$. The local oscillator signal, $r(t)$, is represented with the additional time-varying control phase, $\phi_c(t)$. As with the first phase-locked loops we examined in Chapter 2, the control signal adjusts the local laser's phase. Recall that $\phi_c(t) = K_o \int_0^t c(\tau)d\tau$.

Assuming the dual-detector mixer discussed previously, the IF signal to the frequency discriminator can be written as [32]

$$\chi(t) = A\,Sin(2\pi f_{if} t + \theta_{if}(t) - \phi_c(t)) + n(t) \qquad 12\text{-}47$$

The amplitude $A$, is a function of the photodetector's response and the input power of the two signals (see Equation 12-30). Clearly the IF frequency is the difference, $f_{if} = f_s - f_r$. The double frequency mixing terms are either filtered or out-of-band. The difference between the instantaneous phases of the two optical signals is represented as $\theta_{if}(t) = \theta_s(t) - \theta_r(t)$. The last term of Equation 12-47; $n(t)$, represents the shot noise generated by the photodetectors.

When the dual detector's output is applied to the frequency discriminator, we obtain,

$$\gamma(t) = K_d \left( \frac{1}{2\pi} \frac{\partial \theta_{if}(t)}{\partial t} + f_{if}(t) + N(t) - f_0 \right) \qquad 12\text{-}48$$

As before, $K_d$ represents the frequency discriminator's transducer gain, and $N(t)$ is the transformed shot noise $n(t)$. Note the discriminator's output is not a directly dependent upon the input power from the photodetector.

The discriminator has performed an amplitude-to-frequency transformation of the shot noise. The derivative in Equation 12-45 represents the phase noise of the two optical sources. (Recall $f = \frac{1}{2\pi} \frac{d\,\varphi(t)}{dt}$.) We assume that the discriminator's characteristic is centered at frequency $f = f_0$.

Bononi et al. represent the phase noise in the frequency domain as

$$\eta_{if}(t) \equiv \frac{1}{2\pi} \frac{\partial \theta_{if}(t)}{\partial t} \qquad 12\text{-}49$$

From Figure 12.13, we define the closed loop frequency error as [32]

$$e(t) = \eta_{if}(t) - K_o\, c(t) \qquad 12\text{-}50$$

When the AFC loop is in track, the nominal output frequency will be $f_0$, the center frequency of the discriminator, plus a frequency error term due to

the phase noise $\eta_{if}(t)$ and the transformed shot noise, $N(t)$. We can write the discriminator output as

$$\gamma(t) = K_d\left(e(t) + N(t)\right) \qquad 12\text{-}51$$

Because the discriminator's voltage is filtered with the function $g(t)$ prior to being applied to the laser as control voltage $c(t)$, the frequency error can also be written as

$$\begin{aligned} e(t) &= \eta_{if}(t) - K_o\, c(t) \\ &= \eta_{if}(t) - K_o\, K_d\left(e(t) + N(t)\right) * g(t) \end{aligned} \qquad 12\text{-}52$$

Equation 12-52 represents the closed loop control equation. Computing the power spectral density of both sides provides [32]

$$S_e(f) = \left|\frac{1}{1 + K_o\, K_d\, G(f)}\right|^2 S_{\eta_{if}}(f) + \left|\frac{K_o\, K_d\, G(f)}{1 + K_o\, K_d\, G(f)}\right|^2 S_N(f) \qquad 12\text{-}53$$

Assuming that the loop filter $G(f)$ is a lowpass filter, the first term of Equation 12-53 is a highpass function. Hence, the high frequency components of the phase noise appear in the frequency error. The second component however, is a lowpass function. Thus only the low frequency components of the transformed shot noise appear in the frequency error.

## 12.8 Injection Locking

Adler [33] first described the injection locking of a vacuum tube oscillator. The concept of injection locking is fairly simple. An oscillator depends upon some nonlinear mechanism to control its oscillation frequency and the introduction of another signal into the oscillator causes the nonlinear mechanism to shift the operating frequency. (After all, if the oscillator were linear, the introduction of another signal within the oscillator would yield two independent and undisturbed signals at the output.)

An application of injection locking is shown in Figure 12.16. Instead of using a phase-locked loop to generate a local oscillator for homodyne

detection of the optical modulation, an injection-locked laser generates the necessary reference signal. There are tradeoffs however. The injection-locked laser requires a substantial amount of optical power that is inserted directly (usually some form of focusing is required) into the local laser. This power is no longer available for data detection, in contrast to a homodyne phase-locked loop where the same photodetectors are used for data detection and phase-locking.

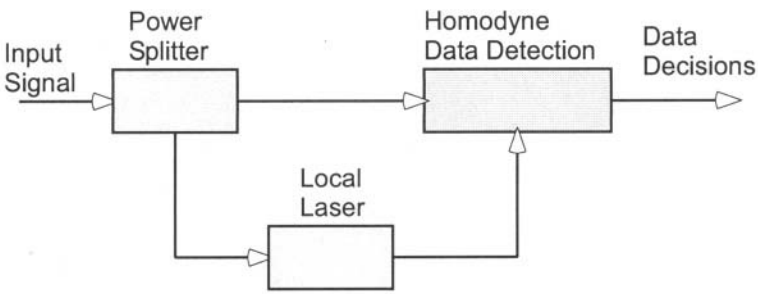


Figure 12.16 Application of Injection Locking

A block diagram of an injection-locked system is shown in Figure 12.17. We split part of the incoming optical power and inject it into a pump laser as shown in the graphic. The input light source is first optically isolated so that reflections do not produce reciprocal coupling. The injection locked laser's cavity length is precisely controlled by adjusting the piezo mirror. (The laser's output frequency is a function of the cavity length, hence the piezo mirror adjusts the lasing frequency.)

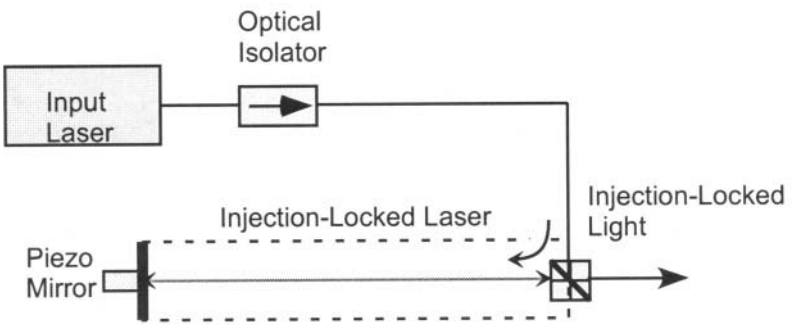


Figure 12.17 Injection-Locked Laser

There are three fundamental equations for injection locking a semiconductor laser [34].

$$\dot{P} = \left( G - \frac{1}{\tau_{pl}} + \frac{c}{n_g L}\sqrt{\frac{P_i}{P}}\,Cos(\theta) \right) P \qquad 12\text{-}54$$

$$\dot{\phi} = \left( \omega_{mo} - \omega_o + \frac{c}{2 n_g L}\sqrt{\frac{P_i}{P}}\,Sin(\theta) + \frac{\alpha}{2}\left( G - \frac{1}{\tau_{pl}} \right) \right) \qquad 12\text{-}55$$

$$\dot{N} = \frac{I}{q} - G P - \frac{N}{\tau_e} \qquad 12\text{-}56$$

P is the total photon number, G is the optical laser gain, $\tau_{pl}$ is the photon lifetime, $L$ represents the locked oscillator's cavity length, $n_g$ is the group index, c is the velocity of light, $\alpha$ accounts for the coupling of amplitude and phase in the laser's electric field, $\theta = \phi_i - \phi$ is the phase difference between the input laser and the injection-locked laser. N is the carrier number, $\omega_o$ is the input frequency, $\omega_{mo}$ is the pre-injection resonant frequency of the laser cavity, I is the injection current, q is the electron charge, and finally $\tau_e$ is spontaneous electron lifetime [34].

The three injection-locking equations must have a simultaneous solution of $P$, $N$ , $\theta$ in order for injection-locking to take place. (This is similar to the simultaneous solution of frequency and phase in the Foker-Plank equations of Chapter 4.) If we denote the difference between two laser frequencies as $\omega_{mo}$, then injection locking bandwidth can be computed as [34]

$$\Delta\omega = \frac{c}{2 n_g L}\sqrt{\frac{P_i}{P}}\,\left( Sin(\theta) - \alpha\, Cos(\theta) \right) \qquad 12\text{-}57$$

When the input laser's frequency is above the locking range, the free-running frequency is modulated by the input frequency. As the input frequency is brought closer into the locking region, the output power will increase until it reaches a maximum when the laser is locked. At input frequencies below the locking region, the operation is unstable and multiple output frequencies may exist [34].

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# 13

# Phase Noise Analysis

## 13.1 Introduction to Phase Noise

A frequency synthesizer or signal source is expected to provide a pure spectral signal. There should be no unwanted amplitude or frequency/phase modulation in the output spectrum. As we will discuss shortly, undesired phase modulation on the local oscillator in communications receivers, can reduce the channel selectivity and degrade the bit error rate of the receiver. It can also degrade the performance of coherent radars [14].

A simplified digital synthesizer is shown in Figure 13.1. In instrumentation-grade synthesizers, the crystal reference oscillator typically provides a reference frequency of 10 MHz or 5 MHz. The voltage-controlled oscillator generally operates at a much higher frequency than the crystal reference. For example, a microwave synthesizer would have a VCO operating at frequencies above 9 GHz. Similar to all of the phase-locked loop discussions in this text, the VCO's output frequency is controlled by an error signal from the loop filter.

In Figure 13.1, the VCO's output frequency is divided by a ratio N in the digital counter. This can be a fixed integer N, or it can be changed to tune the VCO to different frequencies. As in all the PLLs, the phase detector generates an error voltage corresponding to the phase difference between the digital counter output and the reference oscillator (generally a stable crystal oscillator). Often the reference oscillator is thermally and physically isolated from the environment. Even in moderate mobile environments, platform-

induced vibration of the reference oscillator can produce undesired spectral modulation.

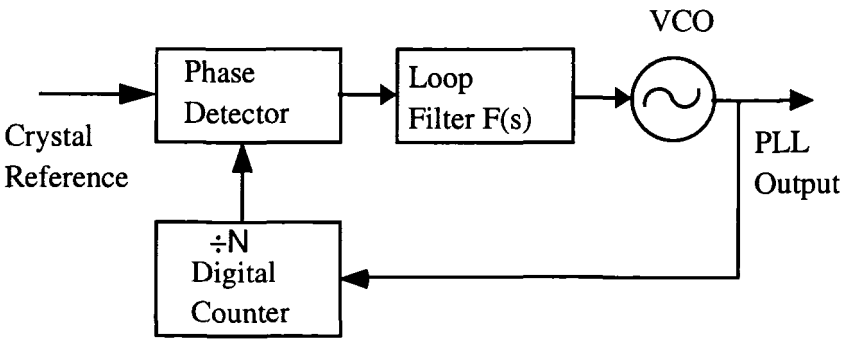



Figure 13.1 Block Diagram of Frequency Synthesizer

Neglecting amplitude noise, a sinusoidal signal source can be mathematically modeled as

$$v(t) = \sqrt{2P}\,Cos[2\pi f_0 t + \phi(t)] \qquad 13\text{-}1$$

In Equation 13-1, $\phi(t)$ is a random process representing the random phase shifts in the signal source. The instantaneous frequency for the sinusoidal source of Equation 13-1 is defined as

$$f(t) = \frac{1}{2\pi}\frac{d}{dt}(2\pi f_0 t + \phi(t)) \qquad 13\text{-}2$$

$$f(t) \equiv f_0 + \Delta f \qquad 13\text{-}3$$

For a quality signal source, the desired frequency should be much greater than the random frequency, or, $f_0 >> |\Delta f|$. Recall the Fourier Transform pair, $\frac{d}{dt}f(t) \leftrightarrow j\omega F(\omega)$. This can be used to derive a relationship between $S_\phi(f)$ and $S_{\Delta f}$. Since $\Delta f = \frac{1}{2\pi}\frac{d\phi(t)}{dt}$, and if the power spectrum $S_{\Delta f}$ exists, we can use the Fourier Transform's differentiation theorem to obtain

$$S_{\Delta f} = f^2 S_\phi(f) \qquad 13\text{-}4$$

This can be used as a figure of merit for the oscillator. As Equation 13-4 indicates, there is a simple relationship between spectrums, $S_{\Delta f}(f)$ and $S_\phi(f)$. (It also suggests a scheme for measuring $S_\phi(f)$.)

The laboratory instrument most commonly used to examine signal sources is the spectrum analyzer. It measures the spectrum of the complete signal, v(t). Assuming f(t) and f´(t) (previously defined in Equation 13-2) have Gaussian distributions, and f´(t) is also stationary, the two-sided RF spectrum for v(t) may be written as [1],

$$S_V(f) = \frac{A^2}{4} e^{-\bar{\phi}^2} \left\{ \begin{array}{l} \delta(f-f_0) + S_\phi(f-f_0) + \sum_{n=2}^{\infty} \frac{1}{n!} \left[ S_\phi(f) \otimes S_\phi(f) \right]_{f_0} \\ + \delta(f+f_0) + S_\phi(f+f_0) + \sum_{n=2}^{\infty} \frac{1}{n!} \left[ S_\phi(f) \otimes S_\phi(f) \right]_{-f_0} \end{array} \right\} \qquad 13\text{-}5$$

where $\overline{\phi^2} = E\left[\phi^2(t)\right]$ and $\otimes$ represents n-1 convolutions of $S_\phi(f)$ with itself, frequency translated to the carrier frequency. Besides the difficult convolution operations, Rutman notes that $S_\phi(f)$ must be known for all frequencies, although estimates can be made for a only finite set [1].

Fortunately for researchers in the field, an approximation exists, based upon the narrowband FM approximation. Because of the sinusoidal waveform, Equation 13-1 may be written as [2]

$$v(t) = \mathrm{Re}\left\{ \sqrt{2P}\, e^{j2\pi f_0 t} e^{j\phi(t)} \right\} \qquad 13\text{-}6$$

Assuming $\phi(t)$ is small, ($<<1$ radian), the exponential phasor $e^{j\phi(t)}$ may be approximated with a truncated power series. Performing this approximation, we obtain [2]

$$v(t) \approx \sqrt{2P}\, Cos\left[2\pi f_0 t\right] - \sqrt{2P}\, \phi(t) Sin\left[2\pi f_0 t\right] \qquad 13\text{-}7$$

By taking the Fourier transform of Equation 13-7, the approximate RF spectrum is obtained [1],

$$S_V(f) \approx \frac{2P}{4}\{\delta(f - f_0) + S_\phi(f - f_0) + \delta(f + f_0) + S_\phi(f + f_0)\} \qquad 13\text{-}8$$

The National Institute of Standards and Technology (NIST) has defined Single-Sideband Phase Noise Referenced to Carrier, **£(f),** as the normalized power in a single sideband of the RF spectrum within a 1 Hz bandwidth. Mathematically it is expressed as

$$£(f) = \frac{\int_{f_0+f-\frac{1}{2}}^{f_0+f+\frac{1}{2}} s_v(f')df'}{\text{Carrier Power}} \qquad 13\text{-}9$$

A graphical depiction of Equation 13-9 is shown in Figure 13.2. Note that a continuous wave signal source such as the frequency synthesizer in Figure 13.1 does not a produce a discrete spectral line, but a defined spectral "smear". (In order to see the spectral broadening, it is necessary to reduce the measurement bandwidth and frequency span.) Some observers describe the close-in phase noise of a signal source similar to a "Christmas Tree". Figure 13.2 is a typical measurement of a signal on a spectrum analyzer with narrow bandwidths.

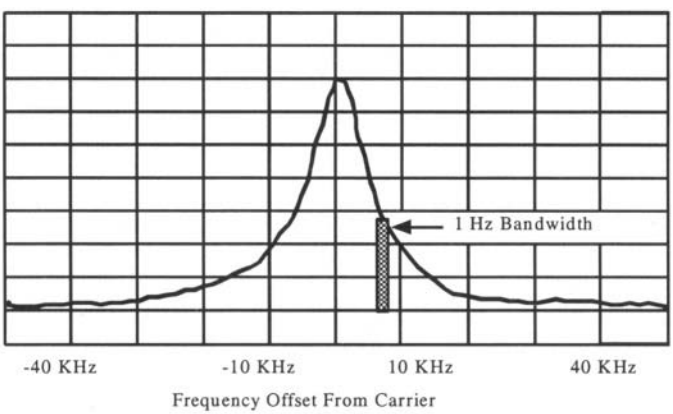



Figure 13.2 Spectral Representation for £(f)

In a strict sense, £(f) defines the spectral purity of the signal. However, using Equations 13-8 and 13-9, £(f) for the sinusoidal source may be expressed as

$$£(f) \approx \frac{1}{2} S_{\phi}(f) \qquad 13\text{-}10$$

## 13.2 Phase Noise in Phase-Locked Loops

As seen in Equation 13-10, there is a relationship between the phase modulation term $\phi(t)$ and the spectral purity £(f). The latter is the industry accepted format for phase-noise measurements. Equation 13-10 is noteworthy because most phase-noise measurements are $S_{\phi}(f)$ instead of £(f).

Because the VCO changes an error voltage to frequency modulation, amplitude modulated (AM) noise present in the loop after the phase detector will undergo a conversion to phase modulation (PM). This can occur at any point in the phase-locked loop.

At the input to a digital counter in a frequency synthesizer, AM noise is also converted to phase modulation. This causes the output transitions of the digital counter to have time jitter (phase modulation). This phase modulation is transferred through the phase detector and subsequently appears on the output waveform of the VCO. A model of phase noise sources for a frequency synthesizer is shown in Figure 13.3 [13,15,19].

In Figure 13.3, several additive phase noise sources have been included in the block diagram. Beginning at the crystal reference, the reference oscillator for the frequency synthesizer has a phase noise, $\varphi_r(f)$, associated with its output, which will be discussed in greater detail. If the phase-locked loop is implemented in hardware, the loop filter usually has an amplifier that generates amplitude noise which will subsequently be converted to phase modulation, $\varphi_l(f)$. The VCO itself generates phase instabilities which are represented by the term, $\varphi_v(f)$. Finally, the divider used by the frequency

synthesizer, also exhibits jitter which is modeled as phase noise by the term, $\varphi_d(f)$.

Recall the output power spectrum of a linear system is expressed as

$$S_y(f) = S_x(f)\left|H(f)^2\right| \qquad 13\text{-}11$$

where

$S_x(f)$ is the input power spectrum

$H(f)$ is the linear system's transfer function

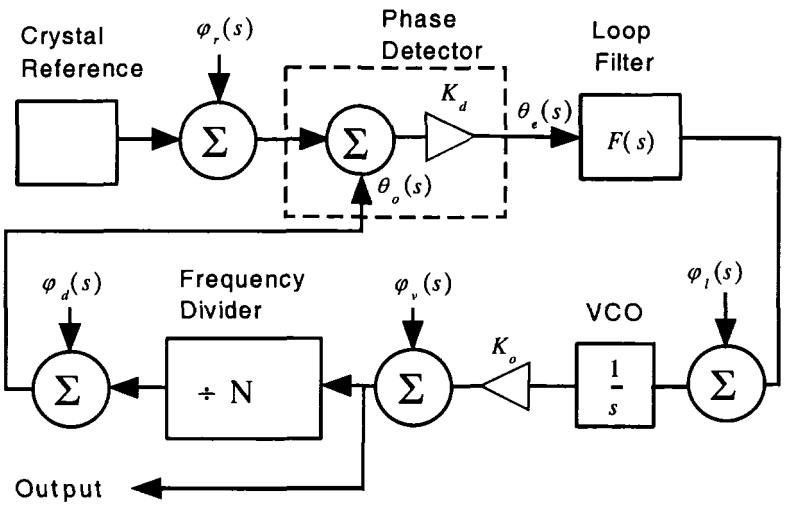



Figure 13.3 Phase Noise Model for Frequency Synthesizer

By computing the forward gain from the additive noise sources to the output and dividing by (1 + closed loop gain), the output power spectrum for Figure 13.3 can be obtained using Equation 13-12 [3].

$$S_\phi(f)=\varphi_r(f)\left|\frac{\frac{K_dK_oF(s)}{s}}{1+\frac{K_dK_oF(s)}{Ns}}\right|^2_{s=j2\pi f}+\varphi_l(f)\left|\frac{\frac{K_o}{s}}{1+\frac{K_dK_oF(s)}{Ns}}\right|^2_{s=j2\pi f}$$
$$+\varphi_v(f)\left|\frac{1}{1+\frac{K_dK_oF(s)}{Ns}}\right|^2_{s=j2\pi f}+\varphi_d(f)\left|\frac{\frac{K_dK_oF(s)}{s}}{1+\frac{K_dK_oF(s)}{Ns}}\right|^2_{s=j2\pi f} \quad 13\text{-}12$$

Because of the relationship between variance and the power spectrum, the output noise variance of the frequency synthesizer can be computed as

$$\sigma_\phi^2=\int_0^\infty S_\phi(f)df \quad 13\text{-}13$$

We can gain more insight into the phase noise of the frequency synthesizer if we replace the term, $\frac{K_dK_oF(s)}{Ns}$, by $G_{OL}(s)$. Although the synthesizer's output frequency does not include the division factor, N, $G_{OL}(s)$ represents the gain of the closed loop. It is the complete gain $G_{OL}(s)$ that determines the loop bandwidth. With this substitution, Equation 13-12 becomes

$$S_\phi(f)=\varphi_r(f)N^2\left|\frac{G_{OL}(s)}{1+G_{OL}(s)}\right|^2_{s=j2\pi f}+\varphi_l(f)N^2\left|\frac{\frac{K_o}{s}}{1+G_{OL}(s)}\right|^2_{s=j2\pi f}$$
$$+\varphi_v(f)N^2\left|\frac{1}{1+G_{OL}(s)}\right|^2_{s=j2\pi f}+\varphi_d(f)N^2\left|\frac{G_{OL}(s)}{1+G_{OL}(s)}\right|^2_{s=j2\pi f} \quad 13\text{-}14$$

Observation of Equation 13-14 shows that the power spectrums are multiplied by the square of the counter's division ratio, N. Note that the

counter and crystal reference are the only significant contributors within the bandwidth of the phase-locked loop. At offset frequencies greater than the PLL bandwidth, the phase noise of the synthesizer is approximately that of the VCO.

## *Example 13.1*

For this example, assume that the phase noise contributions due to the divider and loop filter in Figure 13.3 are negligible. With the tabulated phase noise spectrums of the VCO and crystal reference below, compute the composite phase-locked loop performance. Assume the second order, type-2, phase-locked loop has a loop bandwidth of 1000 Hz, with a damping factor of 0.707. Analysis of Equation 13-14 shows that the VCO's gain constant is a direct contributor to the VCO's phase noise contribution. For this example, let $K_o = \frac{1\,KHz}{Volt}$ and N=100.

| Offset Frequency (Hz) | $\varphi_r(f)$ (dBm) | $\varphi_v(f)$ (dBm) |
|---|---|---|
| 100 | -120 | -40 |
| 1000 | -120 | -73 |
| 10,000 | -120 | -107 |
| 100,000 | -120 | -117 |
| 1,000,000 | -120 | -117 |

Figure 13.4 Phase Noise Specifications for Example 13.1

The specification of a loop bandwidth of 1 KHz implies that $\omega_n = 1.88 \times 10^3$. Recall $\left( \omega_n = \frac{8B_L\zeta}{1+4\zeta^2} \right)$. Assuming $K_d = 1.0$, and using the specifications of N=100, $K_0 = 2.0\pi 10^3$ radians/Volt, the loop filter is computed as

$$F(s) = 56594.1\left(1 + 7.49810^{-4}s\right)/s \qquad 13\text{-}15$$

The open loop transfer function is

$$G_{OL}(s) = 3.556 \times 10^{6}\left(1 + 7.498 \times 10^{-4} s\right)/s^{2} \qquad 13\text{-}16$$

The composite synthesizer phase noise characteristic is plotted in Figure 13.5, using Equation 13-14. (The divider and loop filter noise are assigned as zero.) Along with the composite performance, the individual components for the VCO and crystal reference are also plotted. For this example, the loop bandwidth was chosen arbitrarily, and does not represent the best choice for minimizing the phase noise of the synthesizer.

This example does show that inside the loop bandwidth however, the multiplication factor of $N^2$ has tremendous consequences for microwave synthesizers. In Figure 13.5, the crystal's reference phase noise is increased by 20 Log( 100 ) = 40 dB.

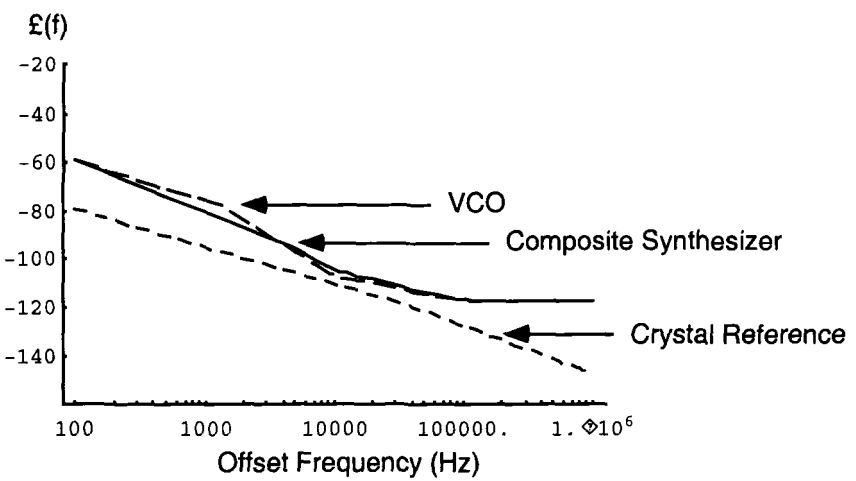



Figure 13.5 Phase Noise Curves for Example 13.1

## 13.3 Phase Noise of Oscillators

Equation 13-4 indicates the phase noise of an oscillator can be measured by either $S_{\phi}(f)$ or $S_{\Delta f}$. An oscillator's phase noise is a complex interaction of variables, ranging from its atomic composition to the physical

environment of the oscillator. Fortunately, a piecewise polynomial representation of an oscillator's phase noise exists and is shown in Equation 13-17 [1].

$$S_\phi(f) = \sum_{\alpha=-2}^{2} h_{\alpha-2} f^{\alpha-2} \qquad 13\text{-}17$$

Traditionally the polynomial representation of oscillator phase noise is characterized for $S_{\Delta f}$ instead of $S_\phi(f)$. and this explains the somewhat unwieldy $\alpha-2$ subscripts and exponents. Not all oscillators will have constants $h_{\alpha-2} \neq 0, \forall\ \alpha-2$ . In other words, the oscillator might have only one, two, three, etc, non-zero polynomial components. Figure 13.6 shows the power-law model for spectral densities [1].

Equation 13-17 indicates that an oscillator's phase noise consists of several additive components. As modeled, they can be represented by physical mechanisms which are listed in Figure 13-6. Random walk frequency noise [4] is due to the oscillator's physical environment (temperature, vibration, shocks, etc.). This phase noise contribution can be significant for a moving platform, and presents design difficulties since laboratory measurements are necessary when the synthesizer is under vibration. Usually great attention is directed to the mounting of the synthesizer's crystal oscillator in these environments.

| $S_\phi(f)$ | Designation |
|---|---|
| $f_0^2 h_{-2} f^{-4}$ | Random walk frequency noise |
| $f_0^2 h_{-1} f^{-3}$ | Flicker frequency noise |
| $f_0^2 h_0 f^{-2}$ | White frequency noise |
| $f_0^2 h_1 f^{-1}$ | Flicker phase noise |
| $f_0^2 h_2$ | White phase noise |

Figure 13.6 Power Law Model for Oscillator Phase Noise [1]

White frequency noise originates from additive white thermal noise sources inside the oscillator's feedback loop [1]. Flicker phase noise generally is produced by amplifiers [1], and the white phase noise is caused by additive white noise sources outside the oscillator's feedback loop.

Figure 13.7 is a graphical representation of the different oscillator phase noise contributors. $1/f$ noise is a particular problem for designers. The

power in a frequency decade is constant, even though the frequency span is increasing [20]. For example, the power contained in the frequency span {0.1,1} is the same as {l,10}. The source of $1/f$ noise in semiconductors continues to be debated [21,22].

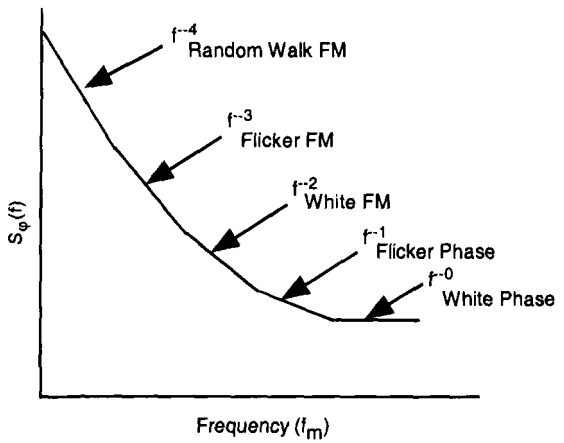



Figure 13.7 Graphical Representation of an Oscillator's Phase Noise Contributors

In his 1966 paper, Leeson describes a heuristic phase noise model for a feedback oscillator [5]. Figure 13.8 shows Leeson's model for the feedback oscillator. The oscillator is composed of a noisy amplifier and a resonator in the feedback loop. The amplifier has a noise figure, F, and the resonator has a loaded quality factor, $Q_{\text{loaded}}$

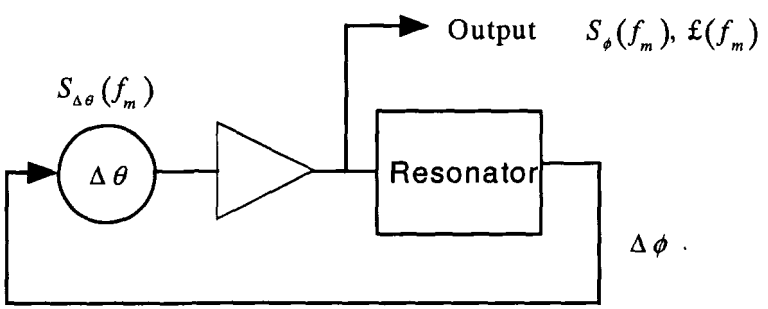



Figure 13.8 Leeson's Model of a Feedback Oscillator [6]

The phase noise of the oscillator can be written as [6]

$$\pounds(f) = \frac{1}{2}\left[1 + \frac{1}{f^2}\left(\frac{f_0}{2Q_{\text{loaded}}}\right)^2\right] S_{\Delta\theta}(f) \qquad 13\text{-}18$$

where

$$S_{\Delta\theta}(f) = \frac{FkT}{P_{\text{s Available}}}\left(1 + \frac{f_c}{f}\right) \qquad 13\text{-}19$$

It is not always possible to model the oscillator with this model. Razavi [16] also notes that a two integrator oscillator "does indeed oscillate" although the definition of Q is not applicable for this oscillator.

The power supply is critical for an oscillator, since power supply noise can enter the feedback loop at many different points. Often linear voltage regulators are used to filter the power supply voltage into the oscillator. However, some linear voltage regulators can add significant phase noise to the oscillator and the designer needs to empirically determine the phase noise contribution of the power supply.

Another caution concerns the control input of the oscillator. Typically low-noise operational amplifiers are used to provide the drive voltage or current. Often the control input is quite capacitive, such as a varactor diode. Some operational amplifiers have difficulty driving capacitive loads over large voltage swings, and this can also degrade the spurious/phase noise performance of the oscillator. Because the VCO changes an error voltage to frequency, amplitude modulated (AM) noise present in the loop after the phase detector will undergo a conversion to phase modulation (PM).

## 13.4 Phase Noise of Dividers

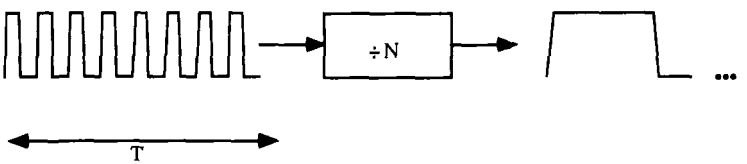
At the input to the digital divider, AM noise also undergoes an AM-to-PM conversion. This causes the output transitions of the digital counter to have time jitter (phase modulation). This phase modulation is transferred through the phase detector and subsequently appears on the output waveform of the VCO.

To analyze a digital counter, Blachman and Mayerhofer [7] observed the divide-by-N counter could be analyzed by differentiating the waveform, and

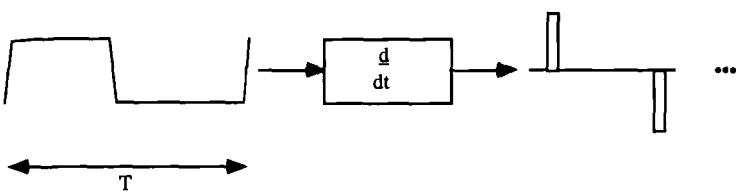
then computing the power spectrum of the resulting waveform. The digital waveform and it's derivative are shown in Figure 13.9.

Recall the power spectrum relationship between a signal and its derivative,

$$S_Y(f) = \frac{1}{4\pi^2 f^2} S_{\dot{Y}}(f) \qquad 13\text{-}20$$




a. Operation of the Divide-By-N Counter




b. Derivative of the Counter Output

Figure 13.9 Digital Divider Waveforms

Using Equation 13-20, it is possible to obtain the power spectrum of the waveform from its derivative. Blachman and Mayerhofer's power spectrum for the digital divider is [7]

$$S(f) = \frac{\dfrac{1-\left\{e^{-\pi^2 f^2 \sigma^2}\right\}^4}{4\pi f^2 T}}{\left(1-\left\{e^{-\pi^2 f^2 \sigma^2}\right\}^2\right)^2 + \left(2\left\{e^{-\pi^2 f^2 \sigma^2}\right\}Cos[\pi f T]\right)^2} \qquad 13\text{-}21$$

In general, the digital divider reduces the input phase noise by the factor

$$\pounds_Y(f) = \pounds_X(f) - 20Log_{10}(N) \qquad 13\text{-}22$$

In Equation 13-22, N is the division ratio, $\pounds_X(f)$ is the input phase noise to the divider, and $\pounds_Y(f)$ is the divider's output phase noise. Equation 13-22 is not completely represent the divider's phase noise, because a digital divider has a minimum noise floor, as shown with the phase noise plot of TTL flipflop in Figure 13.10. This noise floor is often the dominant phase noise contributor to a frequency synthesizer.

A simple representation of a digital divider's input clock is shown in Figure 13.11. The input clock has a finite rise time and is corrupted with internal and external noise. The counter will switch its output when the threshold is exceeded, and Figure 13.11 demonstrates how the clock period is modulated by additive noise. (The additive noise can originate from a number of different sources.) As with the VCO, amplitude noise is converted to phase modulation.

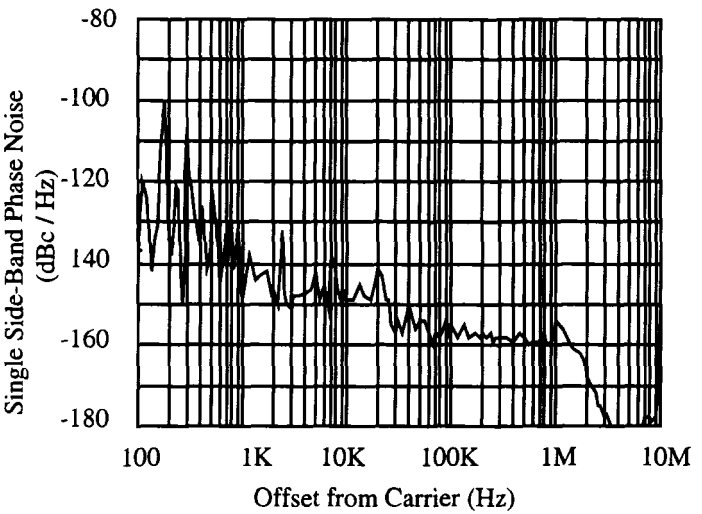



Figure 13.10 Phase Noise Measurement of TTL Flipflop [6]

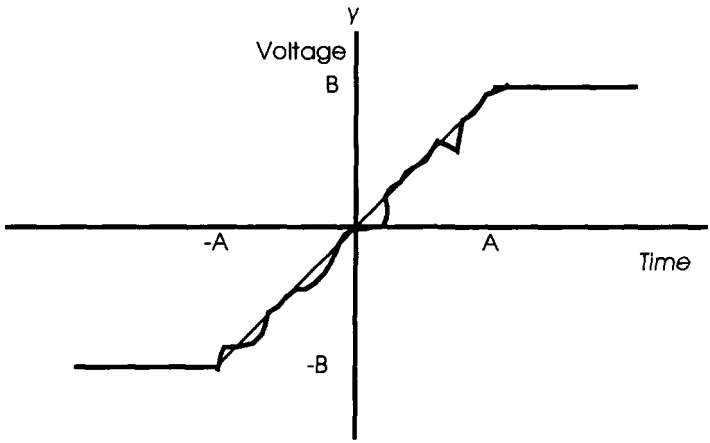



Figure 13.11 Digital Divider's Output Period Modulated by Amplitude Noise

By modeling the digital divider, the equivalent amplitude noise can be determined. Figure 13.12 shows an example analysis of a digital divider schematic. The idea is to compute the equivalent amplitude noise that can modulate the output transition point as in Figure 13.11.

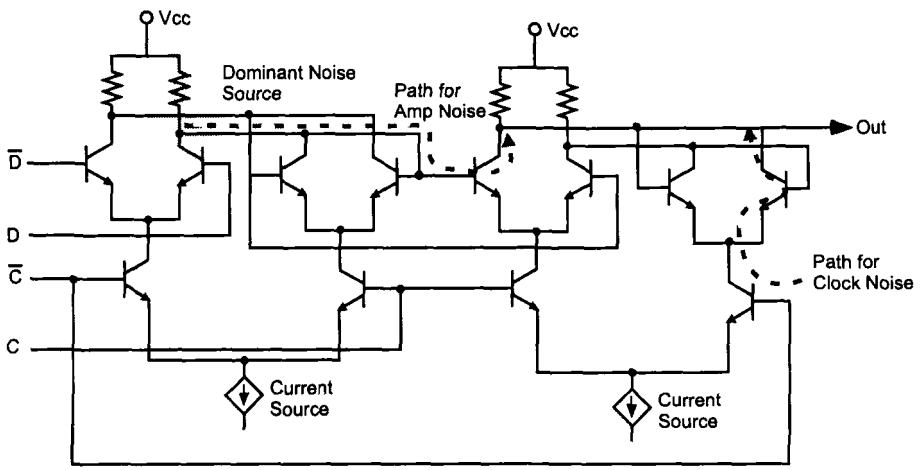



Figure 13.12 Example Divider Schematic

After the noise has been modeled, the phase noise can be estimated by Equation 13-23 below [8].

$$\pounds(f,N)=\frac{\dfrac{2\left(t_r\,Sinc[f t_r]\right)^2\left(1-e^{-(2\pi f\sigma)^2}\right)}{4\pi^2 f^2 N T_0}}{2\left(\dfrac{Q}{NT_0}\right)^2\left(t_r\,Sinc\left[\dfrac{f t_r}{NT_0}\right]\right)^2 e^{-\left(\frac{2\pi\sigma}{NT_0}\right)^2} Sinc^2\left[\dfrac{\pi Q}{NT_0}\right]} \qquad 13\text{-}23$$

where $t_r$ is the divider's input rise time, $\sigma$ is the timing jitter variance, $T_0$ is the period of the input pulse, and $Q = T_0/2$.

## 13.5 Consequences of Phase Noise

A heuristic explanation of phase noise degradation in a receiver can be shown by the graphical representation of the receiver's demodulation process in Figure 13.13. The local oscillator without phase noise is able to demodulate the input signal without distortion. However, the local oscillator with phase noise introduces signal distortion. This describes how a receiver's selectivity (ability to demodulate a single signal in a crowded electromagnetic spectrum) is degraded by phase noise. Yet, degradation of receiver selectivity is not the only degradation caused by phase noise.

In a coherent receiver, a noisy phase reference will introduce implementation losses as discussed in Chapter 11. Recall the degradation for a phase error in a BPSK receiver is

$$P_{\text{E,Synchronizer Phase}}(\rho)=\int_{-\pi}^{\pi}\frac{1}{2}Erfc\left[\sqrt{\rho}\;Cos[\phi]\right]\frac{e^{\alpha\,Cos[\phi]}}{2\pi I_0[\alpha]}d\phi \text{ (Equation 11-4).}$$

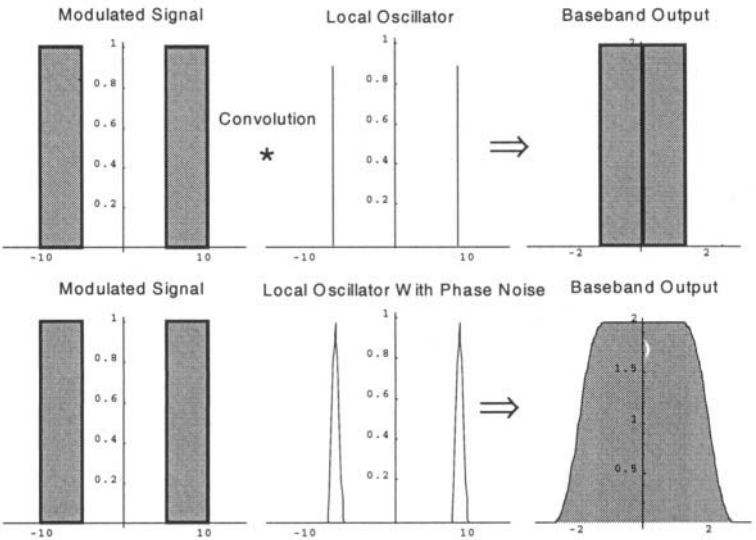



Figure 13.13 Heuristic Depiction of Phase Noise

We can approximate the effect of phase noise in a receiver by modifying $\alpha$ such that

$$\alpha^2 = \left( \frac{S}{N_0 B_L} \right)^{-1} + \sigma_{\Delta\phi}^2 \qquad 13\text{-}24$$

In Equation 13-24, note that the variance of the carrier loop is the summation of the inverse signal-to-noise ratio of the loop, plus the variance of integrated phase noise. For the phase noise only, Figure 13.13 shows the BER of BPSK.

Higher order modulation techniques such as CPM and m-ary PSK are much more susceptible to phase noise than BPSK. Intuitively this would be reasonable, since those modulations have a much smaller signal space than BPSK.

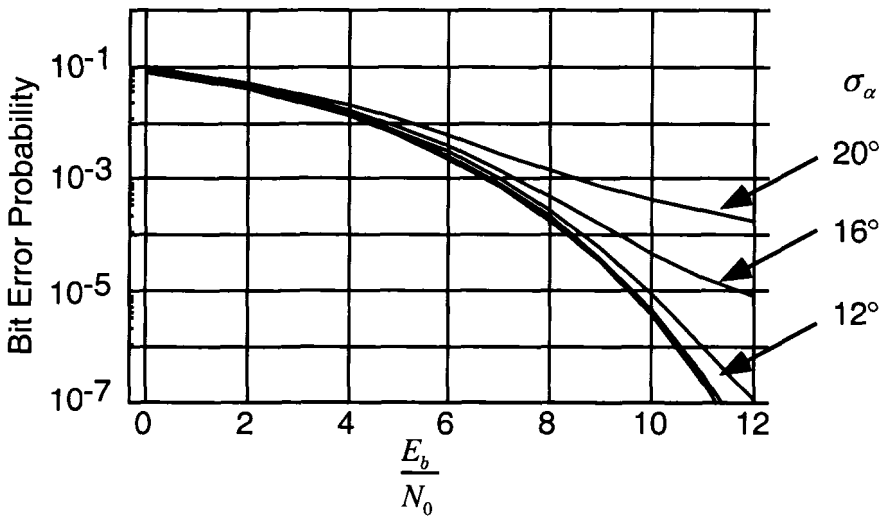



Figure 13.14 BPSK BER With Phase Noise

## 13.6 Phase Noise Measurements

There are several different methods of measuring phase noise and each has its own individual merits. The required instrumentation and expected phase noise of the test devices also provide additional selection criteria. Although the following list is not exhaustive, it discusses some of the techniques suitable for the phase-noise measurements of frequency synthesizers.

1. Direct spectrum measurement. The output of the Device Under Test (DUT) is observed directly with a spectrum analyzer. It is a simple RF spectrum measurement, but is limited by the dynamic range and phase-noise characteristics of the spectrum analyzer. With present microwave spectrum analyzers, this limits sensitivity to about –90 dBc.
2. Time-domain measurements. The duality of frequency and time permits an interval timer to measure the time jitter of the source. This is typically limited for low frequency offsets from the carrier because of the difficulty in gating high frequency waveforms. Often the counter is used measure a related parameter, the Allan variance [17,18].

3. Golden-source measurements. The device under test is demodulated with a comparable frequency source having phase-noise characteristics much better than the DUT itself. The down- converted signal is then measured on a low-frequency spectrum analyzer. In some measurement systems the reference is phase-locked to the DUT and the output of the phase-locked loop is used as the demodulated phase noise. The primary difficulty is obtaining low phase-noise references.
4. Frequency Discriminator. This technique is very versatile and requires little instrumentation. The output power of the DUT is divided between a delay-line and the local oscillator input of a double balanced mixer. The output of the delay line drives the RF input of the mixer and the demodulated (baseband) phase noise appears at the mixer's IF output. Although it removes the requirement for a golden source, it is severely limited in sensitivity by the delay line characteristics.

The sensitivity of a delay line is shown in Equation 13-25 [11]. This sensitivity exhibits a sinusoidal response, with peaks and nulls as a function of the offset frequency. Generally, industry practice is to limit measurements to offset frequencies much less than $1/\tau_d$, where $\tau_d$ is the time delay of the delay line [11]. The constant $k_\phi$ is limited by the same mixer output levels available for the phase detector method.

$$\Delta V(f_m) = \left\{ k_\phi \, 2\pi \tau_d \, \frac{Sin[\pi f_m \tau_d]}{\pi f_m \tau_d} \right\} \Delta f(f_m) \qquad 13\text{-}25$$

where

$\Delta V$ is the differential output voltage

$k_\phi$ is the phase detector gain

$\tau_d$ is the time delay of the discriminator

$f_m$ is the offset from the carrier frequency.

5. Two source measurements. This is similar to the golden-source measurement, but instead of a nearly ideal reference, two identical devices are demodulated with a mixer. Assuming roughly equal phase noise from each device, the measured phase noise is 3-dB greater than the individual device. This technique can be improved by using more than two devices, and measuring the output phase noise in different combinations.

## 13.7 References

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## 13.8 Problems

13.1 If the measured $S_{\Delta f}(f)$ of an oscillator is $S_{\Delta f}(f) = A^2\ Sinc^2(f - f_o) - A^2\ Sinc^2(f + f_o)$, calculate $S_{\varphi}(f)$.

13.2 Obtain V(t) using a second-order approximation of Equation 13-6. What is the approximate RF spectrum?

13.3 With the tabulated phase noise spectrums of the VCO and crystal reference below, compute the composite phase-locked loop performance. Assume the second order, type-2, phase-locked loop has a loop bandwidth of 100 Hz, with a damping factor of 0.707. For this problem, let $K_o = \frac{1\,KHz}{Volt}$ and N=78.

| Offset Frequency (Hz) | $\varphi_r(f)$ (dBm) | $\varphi_v(f)$ (dBm) |
|---|---|---|
| 100 | -110 | -30 |
| 1000 | -120 | -73 |
| 10,000 | -120 | -107 |
| 100,000 | -120 | -117 |
| 1,000,000 | -120 | -117 |

13.4 With the tabulated phase noise spectrums of the VCO , crystal reference, and divider below, compute the composite phase-locked loop performance. Assume the second order, type-2, phase-locked loop has a loop bandwidth of 10000 Hz, with a damping factor of 0.707. For this problem, let $K_o = \frac{1\,KHz}{Volt}$ and N=1000.

| Offset Frequency (Hz) | $\varphi_r(f)$ (dBm) | $\varphi_d(f)$ | $\varphi_v(f)$ (dBm) |
|---|---|---|---|
| 100 | -120 | -110 | -40 |
| 1000 | -120 | -120 | -73 |
| 10,000 | -120 | -130 | -107 |
| 100,000 | -120 | -150 | -117 |
| 1,000,000 | -120 | -160 | -117 |

13.5 Derive a phase noise degradation equation for QPSK similar to Equation 11-4 and 13-23.

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# APPENDIX A LAPLACE TRANSFORMS

| $x(t)$ | $X(s)$ |
|---|---|
| $\delta(t)$ | $1$ |
| $u(t)$ | $1/s$ |
| $t$ | $1/s^2$ |
| $t^2/2$ | $1/s^3$ |
| $t^{k-1}$ | $\dfrac{(k-1)!}{s^k}$ |
| $e^{\alpha t}$ | $(s+\alpha)^{-1}$ |
| $t^k\, e^{-\alpha t}$ | $\dfrac{(k-1)!}{(s+\alpha)^k}$ |
| $\dfrac{1}{\alpha}\left(e^{\alpha t}-1\right)$ | $\dfrac{1}{s(s-\alpha)}$ |
| $\dfrac{1}{\alpha}\left(1-e^{\alpha t}\right)$ | $\dfrac{1}{s(s+\alpha)}$ |
| $\dfrac{1}{\alpha}Sin(\omega t)$ | $\dfrac{1}{s^2+\omega^2}$ |
| $Cos(\omega t)$ | $\dfrac{s}{s^2+\omega^2}$ |
| $\dfrac{e^{\beta t}-e^{\alpha t}}{\beta-\alpha}$ | $\dfrac{1}{(s-\alpha)(s-\beta)}$ |
| $\dfrac{\beta e^{\beta t}-\alpha e^{\alpha t}}{\beta-\alpha}$ | $\dfrac{s}{(s-\alpha)(s-\beta)}$ |
| $\dfrac{\beta e^{\beta t}-\alpha e^{\alpha t}}{\beta(\alpha-\beta)}+\dfrac{1}{\alpha\beta}$ | $\dfrac{s}{s\,(s-\alpha)(s-\beta)}$ |
| $\dfrac{e^{-\xi\omega_n t}\,Sin\left(\sqrt{1-\xi^2}\,\omega_n t\right.}{\sqrt{1-\xi^2}\,\omega_n}$ | $\dfrac{1}{s^2+2s\xi\omega_n+\omega_n^2}$ |

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# APPENDIX B Z TRANSFORMS

| $x(n)$ | $X(z)$ |
|---|---|
| $\delta(n)$ | $1$ |
| $u(n)$ | $\frac{z}{z-1}$ |
| $nT$ | $\frac{Tz}{(z-1)^2}$ |
| $(nT)^2$ | $\frac{T^2 z(z+1)}{(z-1)^3}$ |
| $\alpha^n$ | $\frac{z}{z-\alpha}$ |
| $e^{-\alpha nT}$ | $\frac{z}{z-e^{-\alpha T}}$ |
| $nTe^{-\alpha nT}$ | $\frac{Tze^{-\alpha T}}{\left(z-e^{-\alpha T}\right)^2}$ |
| $1-e^{\alpha nT}$ | $\frac{z\left(1-e^{-\alpha T}\right)}{(z-1)\left(z-e^{-\alpha T}\right)}$ |
| $Sin(\omega nT)$ | $\frac{zSin[\omega T]}{z^2-2zCos[\omega T]+1}$ |
| $Cos(\omega nT)$ | $\frac{z(z-Cos[\omega T])}{z^2-2zCos[\omega T]+1}$ |

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