Some Design Aspects on RF CMOS LNAs and Mixers

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Abstract

This thesis deal with two parts of a radio receiver. The low noise amplifier (LNA) and the mixer.

A tuned RF front-end amplifier in CMOS with an operating frequency around 1.8 to 2GHz has been investigated. A symmetric design has been used to improve linearity with preserved power consumption. In this case it has been a parallel connection of complementary devices. The symmetric solution allows the use of inductor pairs in transformer configuration to improve the gain of the circuit.

The input impedance has been controlled by an inductive series feedback of a transconductance. An extended investigation has been made to determine the effect of the capacitive shunt feedback, traditionally ignored, as well as the effects of other internal parasitics. Simulation results shows that for a required input resistance and operating frequency a maximum transconductance of the transistor can be found. A new approximation of the input resistance where found, valid for low frequencies and for small transconductances.

The most important part of the amplifier is the first stage (the inverter) as it will affect both input impedance and noise. Analysis of the optimum noise figure both with the capacitive shunt feedback excluded and included are made to show that it is possible to repeat the calculations in the same manner both times and thereby being able to compare the results.

The major conclusion of this paper is that the shunt feedback can not be ignored and that good design methods therefore require a more extended analysis.

Imbalances in quadrature demodulators, based on a passive CMOS mixer with capacitive load, has been studied with respect to process spread.

A mathematical model of the mixer has been presented which explains the statistical spread in the mixer. The mixer transfer function has been divided into a multiplier, an amplifier and a time-variant filter, where the statistical spread will affect the filtering part of the mixer.

The filter is time-invariant if the time constant is large enough compared with the local oscillator frequency. A first approximation of the mixer filter is therefore that it is time-invariant which simplifies the statistical analysis. The model does not require time-consuming transient analysis, as it possible to use the time average of the transfer function, enabling the use of AC simulation instead.

The time-invariant model gives a maximum of the minimum image rejection. The time-variance increases the spread and reduces the image rejection.

The main conclusion of the investigation is that the time average of the transfer function can be used as the small signal model for the mixer. The model can be used to analyse and simulate the statistical spread and thereby the imbalance and minimum image rejection of a quadrature demodulator.

Preface

This thesis begins with an introduction of why it is interesting to find circuit solutions in a standard CMOS process for RF transceivers. This is followed by a description of the LNA and the analysis of its gain, noise and impedance matching. The last chapter is about the mismatch in mixers and its effect on I/Q-receivers.

I have published two conference papers on the LNA:

- I Anna-Karin Stenman and Lars Sundström, A 2-GHz Tuned Linear CMOS Amplifier, Midwest Symposium on Circuits and Systems, MWSCAS '99
- II Anna-Karin Stenman and Lars Sundström, Extended Analysis of Input Impedance Control of an NMOS-Transistor with an Inductive Series Feedback, International Conference on Electronics, Circuits and Systems, ICECS '99, pp. 307-310

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Contents

1	Introduction	1
2	Low Noise Amplifier	3
	2.1 Background	3
	2.2 Basic Amplifier Configuration	3
	2.2.1 Selection of Amplifier Configuration	3
	2.2.2 Differential Stage or Inverter	4
	2.2.3 Linearity	5
	2.2.4 Using Coupled Inductors	8
	2.2.5 Effects of Transistor Dimensions	9
	2.3 Noise Analysis of MOS Transistor	. 10
	2.3.1 Noise Sources	. 10
	2.3.1.1 Drain Current Thermal Noise	. 10
	2.3.1.2 Gate Noise	. 14
	2.3.1.3 Substrate Noise	. 15
	2.3.1.4 Flicker Noise	. 15
	2.3.2 Transistor Noise Model	. 16
	2.3.3 Equivalent Noise Model	. 18
	2.3.3.1 Two-Port Model for a MOS-Transistor	. 18
	2.3.3.2 Two-Port Model for an Inverter	. 19
	2.5.5.5 Noise Comparison	. 20
	2.4 Transadmittance Ampinier	. 22
	2.4.1 Input Impedance	. 22
	2.4.1.1 Calculation Using Complete MOS Model	. 23
	2.4.1.2 Calculation Using New Simplified MOS Model	. 23
	2.4.1.5 Calculation Using New Simplified WOS Woder	27
	2.4.2.1 Calculation Using Simplified MOS Model	. 28
	2.4.2.2 Calculation Using New Simplified MOS Model	. 28
	2.4.3 Noise Factor	. 30
	2.4.3.1 Noise Factor of Simplified MOS Model	. 30
	2.4.3.2 Noise Factor of New Simplified MOS Model	. 32
	2.5 Transresistance Amplifier	. 36
	2.5.1 Input Impedance	. 36
	2.5.2 Gain of Transresistance Amplifier	. 37
	2.6 Voltage Follower	. 37
	2.6.1 Input Impedance	. 37
	2.6.2 Output Impedance	. 38
	2.6.3 Gain of Voltage Follower	. 39
	2.7 Overall Amplifier Performance	. 39
	2.7.1 Overall Gain	. 39

	2.7.2 Simulating Gain and Linearity	40
	2.7.3 Calculating the Noise Figure	42
	2.8 Conclusion	44
3	Analysis of Conversion Gain Spread in Mixers	45
	3.1 Background	45
	3.2 An Image-Reject Mixer and the Effect of I/Q-Imbalance	47
	3.2.1 Mixing	47
	3.2.2 Imbalance	49
	3.3 Conversion Gain	51
	3.3.1 Ideal Mixer	51
	3.3.2 Passive CMOS Mixer	52
	3.3.3 Numerical Calculation of the Time-Variant Filter	55
	3.3.4 Conversion Gain and the Dependency on the Conductance	58
	3.4 Modelling and Statistical Properties of Mixer Image Rejection	58
	3.4.1 Channel Conductance	58
	3.4.2 Mixer Conductance	59
	3.4.3 Image Rejection	
	3.5 Simulation	61
	3.5.1 Simulation Setup	61
	3.5.2 Channel Conductance	
	3.5.3 Image Rejection	
	3.5.4 Additional simulations	
	3.5.4.1 Changing the IF	
	5.5.4.2 Varying the LO signal	

Appendix

A	Input Impedance of the Common Source Amplifier	73					
	A.1 Blackman's Formula	73					
	A.2 Complete Small Signal Model	74					
	A.3 New Simplified Small Signal Model						
B	Gain of Various Stages	77					
	B.1 Superposition Model	77					
	B.2 Transconductance Amplifier	77					
	B.2.1 Schematic	78					
	B.2.2 Gate Drain Capacitance Excluded	79					
	B.2.3 Gate Drain Capacitance Included	80					
	B.3 Current Follower	81					
	B.4 Voltage Follower	83					
С	Noise	85					
	C.1 Schematic	85					
	C.2 Calculating the Equivalent Noise Sources	85					
	C.2.1 Output Noise as a Function of Equivalent Input Noise						
	C.2.1.1 Open Circuit	85					
	C.2.1.2 Short Circuit	89 80					
	C.2.2.1 Open Circuit	89					
	C.2.2.2 Short Circuit	92					
	C.2.3 Equivalent Noise as a Function of Transistor Noise	94					
	C.2.3.1 Open Circuit						
	C 3 Total Equivalent Input Noise Voltage	95 96					
	C 3.1 Gate Drain Capacitance is Zero	96					
	C.3.2 Gate Drain Capacitance is not Zero	96					
D	Gaussian Approximation	99					
Е	Conductance Model						
	E.1 Transistor Parameters with Mismatch						
	E.2 Conductance	101					
	E.2.1 Effective Transistor Width and Length	102					
	E.2.2 Threshold Voltage	102					
	E.2.3 Effective Electron Mobility	103					
	E.2.4 Oxide Capacitance	103					
	E.2.5 Effect of Drain and Source Kesistance	103					
F	Additional Simulation Results	105					

Chapter 1

Introduction

The number of wireless applications is increasing rapidly in todays society of information technology, as it is not only the phone that is mobile but the computer as well, e.g. lap-top or a hand-held PDA (Personal Digital Assistant). Basically there are two types of wireless connections. The mobile phone systems, such as GSM, that can handle roaming of an object on the move, and short range stationary wireless systems, e.g. Bluetooth and W-LAN (Wireless Local Area Network), that connects two or more devices within a short distance. Wireless connections are thereby used by mobile units and their equipment, by stationary computers and surrounding devices (e.g. printers), as well as the mobile phone and the computer, etc. In short: anything should be able to be connected with everything by them selves or via another unit. Wirelessly.

As many units are, if not mobile, at least portable and battery-powered, the radio transceiver has to decrease power consumption to increase battery life-time. The use of smaller transistor dimensions in digital integrated circuits (IC) drives the power supply towards lower voltages, which also decreases the power consumption in digital circuits. The analog transceiver should therefore also be able to operate at low voltage, to be able to use the same power supply. Size is important for mobile units, as customers want nifty light weight gadgets, as a consequence the chips should be few and small. Finally it is impossible not to stress the importance of low cost, as the number of units produced can be counted in millions and customers are very price sensitive.

The radio transceiver consists of analog, mixed-mode and digital circuits. Traditionally these circuits are manufactured in different processes. The necessity of reducing cost is driving production towards cheap processes where CMOS (Complementary-Metal-Oxide-Semiconductor) holds a strong position. If radio frequency (RF) solutions can be found for a standard CMOS process, it is possible to integrate analog and digital parts on the same IC. This would reduce the number of capsules, as well as the need for external components, which reduces circuit board area and the cost of mounting. The problem remains, however, that the performance of the transistor, concerning gain, current consumption, noise and high frequency behaviour in general, is better for a bipolar transistor than for a CMOS transistor.

RF CMOS has been a strong field of research since the early nineties. As time has passed manufacturers have been able to implement smaller structures for semiconducting devices, which has improved the performance of the CMOS transistor in RF analog circuits. Even though the performance has become better, there is still a large potential to improve existing circuit solutions and find new circuits that can compete with bipolar circuits, and by thorough theoretical analysis find the benefits and drawbacks of each solution.

This licentiate thesis deals with some design aspects for two circuit blocks in an RF receiver, the low noise amplifier (LNA) and the mixer. The circuits has been analysed mathematically to make it possible to control and improve circuit performance.

As for the LNA, the objective was to investigate a partly new CMOS amplifier topology, with matched input impedance, suitable for low voltage applications. The circuit is a symmetrical version of a traditional receiver amplifier with an inductive series feedback, making the circuit more linear due to the symmetry. It was found that the first order model of the circuit did not apply and that the introduction of an adjusted model was necessary to get the correct input resistance. The noise figure calculations were also affected, showing an optimum transconductance slightly different from what was first expected. The noise figure equation looks very similar to the original equation, after the addition of only a few terms. Unfortunately the noise performance got worse due to the lower transition frequency in the inverter.

Regarding the mixer the work has been focused on spread in the conversion gain of mixers. This gives an opportunity to study the mismatch in an I/Q-receiver due to the mixers. The mixer used has been a traditional passive voltage driven CMOS mixer with a capacitive load, which is the assumed input impedance of an IF buffer.

The mixer is a time-variant linear element that usually needs to be simulated with transient analysis with very short time steps over a long time period. This renders a huge amount of data that has to be Fourier-transformed to find the frequency information of interest. Adding statistical variation increases the amount of data to the limit where the computer/program might not be able to handle it. A new way of modelling has therefore been developed where the statistical spread can be analysed in the frequency domain directly using the time average small signal model of the transfer function. In this way simulation time and data can be reduced.

The mixer is modelled as a multiplier, an amplifier and a time-variant filter, where the statistical spread will affect the filtering part of the mixer. The filter becomes time-invariant if the time-constant is large enough compared with the local oscillator frequency, which enables the use of AC simulation. The AC simulation gives the maximum image rejection possible while the time-variance increases the spread, which reduces the image rejection.

The time-variant filter contains of the Thevenin equivalent conductance of the mixer, given by the transistors channel conductance, and the capacitive load. The Thevenin conductance is dependant on the LO signal, which gives that the conductance is time-variant, unless the LO signal is a perfect square-wave, then the conductance is constant and AC simulations of the filter will equal transient simulations.

Finally it is found that the image rejection is dependant on the transistor width (conductance), capacitive load, IF and LO frequency.

Chapter 2

Low Noise Amplifier

2.1 Background

For low noise amplifiers (LNA) in receiving systems, it is important to have a low reflection coefficient at the input port, so that the energy of the received signal is totally absorbed and not reflected back causing an inefficient reception. The performance of the antenna filter may also be dependent on a well defined termination. Thereby it is important to present a well-defined resistance to the antenna or antenna filter. The CMOS common source input port is capacitive and therefore an input resistance of for example 50Ω has to be achieved by other means.

The transistor is a nonlinear element. To improve linearity it is possible to introduce symmetric solutions that compensates the nonlinearity. There are two ways of doing this: either an anti-series connection of identical elements (a differential stage) or a parallel connection of complementary devices (an inverter). Another way to increase the linearity is to apply feedback.

The work on LNAs has been focused on the analysis of the different stages of the LNA. But there still are some common requirements for all calculations and simulations. The circuit should be designed in such a way that it should be able to operate at low voltage, to be able to use the same power supply as digital IC's. The supply voltage is set to 2.5-3V, which is a relaxed requirement. The operating frequency is around 1.8-2GHz. The input resistance is supposed to be 50Ω The load is assumed to be a capacitive input of a CMOS mixer.

2.2 Basic Amplifier Configuration

2.2.1 Selection of Amplifier Configuration

The first stage in an amplifier is the most important part as it will have a large influence on the noise figure. The inductively degenerated transconductance is quite often found in articles [3-6] as a useful LNA. The circuit provides high gain while it still gives a good control of the input impedance.

Another benefit of the inductive series feedback is that the noise (v.s. power and gain) can be kept lower than with other solutions to control the input impedance, such as resistive termination, common gate stage and shunt-series feedback [4].

One way of increasing the gain is to use a cascode with a resonant tank at the output [4,7]. The current is transformed into a voltage in a resonant tank containing an inductor and a capacitance. Instead of using a lumped capacitance, it is possible to use the input capacitance of a voltage follower. The voltage follower improves the driving of the next stage (in this case a mixer). In figure 2.1 the different stages of the amplifier are shown, first the common source transconductance with an inductive degeneration, then the common gate current follower, with a resonant tank as a load, and finally the common drain voltage follower.

2.2.2 Differential Stage or Inverter

The cascode in figure 2.1 can be replaced with a differential stage and a differential current follower on top of the transconductance. The problem is that an extra transistor is needed as a current source at the bottom of the circuit, which makes the circuit less suitable for low voltage applications, as three transistors are stacked on top of each other.

In the differential amplifier there are two inductors in the transconductance as well as at the output of the current follower. Connecting them in a transformer structure, using them as coupled inductors, increases the Q-value, which is important as lossy inductors can contribute quite a lot to the noise. The circuit is working in a push-pull manner (usually considered a great benefit), giving that the individual inductors has to turn clockwise in one branch and counter-clockwise, in the other branch. It is possible to use the inductors in a symmetric transformer structure, but the metal wires are crossing each other, which means that the enhanced Q-value can only be obtained at the cost of larger loss in the individual inductor, due to the necessary vias when changing metal layer and the increased capacitance towards the substrate.

Instead of using a differential stage as a transconductance it is possible to use an inverter. The inverter is used by Karanicolas [3] to drive a mixer connected/stacked directly between the two drain outputs. The reason for this was to half the current consumption, while the noise of the inverter could be kept almost constant. Just as in a differential stage the linearity is increased due to the symmetry of the inverter. It is possible connect the inductors in a transformer layout as source degeneration. The circuit is working in a push-push manner, giving that both the individual inductors are turning either clock-wise ore counter-clock-wise.

In figure 2.2 the inverter is shown with coupled inductors as source degeneration. The current follower can also be designed in a symmetric manner (with coupled inductors in the resonant tanks), as well as the voltage follower. As all circuits in the amplifier are parallel connections they can be analysed as single transistor circuits from a small signal point of view, see figure 2.9, 2.16 and 2.17.

The fact that only two transistors are stacked in each stage makes it useful for low voltage operation and as the first stage is the most important circuit in a low noise amplifier, most of this part of the thesis will be focused on the inverter structure.



Figure 2.1: A traditional nonsymmetric amplifier.



Figure 2.2: The symmetric amplifier.

2.2.3 Linearity

The nonlinearity is defined as the difference between the expected output level, given by the gain at the operating point, and the actual output level for a given input signal level [20]. It is dependent on the excursion from the operation point and therefore the differential gain or differential error is defined as

$$\varepsilon(x_i, x_o) = \frac{A(x_i, x_o) - A_q}{A_q}$$
(2.1)

where x_i and x_o is the input and output signal excursion from the operating point, respectively, A_q is the gain at the operating point and $A(x_i, x_o)$ is the actual gain for the given signal excursion.

The second and third order intermodulation (IM) products can be estimated from the differential error, if the signal level is small, i.e. weak non-linearity.

$$IM_2 \approx \left| \frac{\varepsilon_+ - \varepsilon_-}{4} \right| \tag{2.2}$$

$$IM_3 \approx \left| \frac{\varepsilon_+ + \varepsilon_-}{8} \right| \tag{2.3}$$

 ε_+ and ε_- are the differential errors at signal excursions of x_i and $-x_i$, respectively, from the operating point.

From equation 2.2 it is seen that IM_2 will be small if the alteration of the gain is symmetric around the operating point. This can be achieved by using symmetric configuration. IM_3 , on the other hand, gives that the differential error should be of equal size but opposite sign to be cancelled. This can be achieved by applying feedback. Both intermodulations can then be reduced by designing a symmetric circuit with feedback.

Example 1 DC Simulation of Linearity

The purpose of this simulation is to show the DC output signal excursion, gain and differential error as a function of the input signal excursion from the operating point, for the nonsymmetric amplifier in figure 2.1 and the symmetric amplifier in figure 2.2. The differential error and the intermodulation products can then be calculated from equations 2.1 to 2.3, where the DC gain was calculated from the simulation as

$$A(v_l, v_g) = \frac{\partial v_l}{\partial v_g}$$

In the nonsymmetric circuit the width of the NMOS-transistors is twice that of the NMOS transistors in the symmetric circuit. An inverter consumes half the current compared with a single transistor amplifier, for the same transconductance. On the other hand it is not possible to stack the complementary current follower and the inverter, as in the case of a single MOS transistor, which means that it is placed in series after the inverter, with its own bias current of approximately the same size as the inverter.

The PMOS and NMOS transistors are not a perfectly complementary pair as they have slightly different large signal behaviour and parasitic capacitances. The large signal behaviour of the inverter can to some extent be compensated by individual biasing of the transistors. And the difference between the parasitic capacitance between the nodes can simply be compensated by adding external capacitors where it is necessary.

The coils has no effect, as it is a DC simulation. The gain of the two circuits are different as r_c is of the same size in both circuits, resulting in that the DC gain of the symmetric amplifier is smaller as the small signal output load of the current follower is $r_c/2$, which reduces the gain. r_s provides only a very small feedback in the transconductance stage and has a very small influence on the gain.

For an input signal excursion of $\pm 0.2V$, the intermodulation products are found to be 39.8 $\cdot 10^{-3}$ and 4.78 $\cdot 10^{-3}$ for IM_2 and IM_3 , respectively, for the nonsymmetric amplifier, while they are $0.95 \cdot 10^{-3}$ and 5.33 $\cdot 10^{-3}$ for the symmetric amplifier. IM_2 of the symmetric amplifier is thereby 42 times smaller than IM_2 of the nonsymmetric amplifier and IM_3 is about the same size for both circuits.





Figure 2.3: Simulation of DC a) output signal excursion, b) gain and c) differential error, for nonsymmetric (solid) and symmetric (dotted) amplifier.

The simulated results in example 1 are shown in figure 2.3. The output signal excursion in figure 2.3a) does not reveal the difference in linearity between the two circuits, only the difference in gain. Figure 2.3b) shows the DC gain as a function of the signal excursion. It is clear that the gain of the symmetric circuit is symmetric around the operating point and that for small signal excursions the second order intermodulation will be small, as the differential errors for positive and negative signal excursion are almost equal, see figure 2.3c). The difference in IM_3 is not seen in the figure but it is slightly larger in the symmetric amplifier than the nonsymmetric amplifier, see example 1.

In example 1 the symmetric amplifier has the same transconductance for the same current consumption, as the nonsymmetric amplifier, but with increased linearity in the circuit, at least regarding the second order harmonic.

2.2.4 Using Coupled Inductors

One of the main differences between a non-symmetric configuration and a symmetric one is the possibility of using coupled inductors in the symmetric transadmittance and at the output of the current follower.

The individual inductance L_I in one of the branches will be increased, due to the coupling. On the other hand the symmetric circuit is a parallel connection which will reduce the inductance by two, giving a resulting coupled inductance L_{CI} of

$$L_{CI} = \frac{l+k}{2} L_I \le L_I \tag{2.4}$$

where k is the coupling coefficient. Thanks to the coupling it is thereby not necessary to double the inductance in the individual coils in the symmetric configuration.

The advantage of coupled inductors is the increased Q-value, as the resistance r_I is also reduced by a factor of two due to the symmetry of the circuit, giving

$$Q_{CI} = \frac{\omega(1+k)L_I/2}{r_I/2} = (1+k)\frac{\omega L_I}{r_I} = (1+k)Q_I$$
(2.5)

As the Q-value is generally low in a semiconductor process, every chance of increasing the Q-value is welcome. For the input stage this means that the influence of the inductor series resistance r_I on the input resistance is reduced as well as its influence on the noise. For the current follower with a resonance tank it means that the equivalent parallel resistance R_I of the inductor will increase. The gain of the stage is R_I , as a first approximation, and the gain will increase as

$$\frac{R_I|_{CI}}{R_I|_I} = \frac{\frac{r_I}{2}(1+Q_{CI}^2)}{r_I(1+Q_I^2)} \approx \frac{1}{2}(1+k)^2 \le 2$$
(2.6)

due to the increased Q-value in the coupled inductors.

Example 2 Inductance, Coupling Factor and Q-value

There are many ways of trying to estimate/calculate the inductance of a spiral inductor and its parasitics [10,30,31]. The problem is that the model of a metal structure residing on a lossy conductive substrate is complicated and not fully known yet. A CAD tool called ASITIC [32] can provide a π model for the coupled inductor, where the individual inductance is modelled as in figure 2.4. In the process used for simulation the substrate resistivity is 10 Ω -cm and the metal sheet resistance is 18.7 Ω



Figure 2.4: Inductance model

Small coupled inductor

One individual coil with 16 sides, 3 turns, radius of 108µm width 10µm and a spacing of 14µm between the turns (will give a spacing of 2µm between the interlaced inductors) has an inductance L_I of 1.33nH and a series resistance r_I of 4.91 Ω . For an operating frequency of 1.8GHz the Q-value is 3.0 for one of the coils. The parasitic capacitance C_s and resistance R_s to the ground is about 80fF and 800 Ω , respectively. The coupling factor k is 0.72, giving that the Q-value of the coupled inductor is 5.3 and the coupled inductance is 1.14nH.

Large coupled inductor

One individual coil with 16 sides, 4 turns, radius of 165 μ m width 10 μ m and a spacing of 14 μ m between the turns (will give a spacing of 2 μ m between the interlaced inductors) has an inductance of 4.3nH and a series resistance of 10.3 Ω . For an operating frequency of 1.8GHz the Q-value is 4.7 for one of the coils. The parasitic capacitance and resistance to the ground is about 165fF and 650 Ω , respectively. The coupling factor k is 0.82, giving that the Q-value of the coupled inductor is 8.6 and the coupled inductance is 3.9nH.

2.2.5 Effects of Transistor Dimensions

It is possible to use the fact that everything is almost equally scaled with the dimension of the transistor once the transistor is biased. In this case it is the width of the transistor that changes X times, as it is supposed to be of minimum length. The analysis of the circuit is simplified when the internal relation between the elements in the transistor then can be considered constant, giving the parameters as a function of the nominal value of the biased circuit.

$$W = X \cdot W_{nom} \qquad C_{bs} \approx X \cdot C_{bsnom}$$

$$g_m \approx X \cdot g_{mnom} \qquad C_{gb} \approx X \cdot C_{gbnom} \qquad (2.7)$$

$$C_{gs} \approx X \cdot C_{gsnom} \qquad I_d \approx X \cdot I_{dnom}$$

$$C_{gd} \approx X \cdot C_{gdnom} \qquad r_d \approx r_{dnom} / X$$



Figure 2.5: Cross section of MOS transistor.

2.3 Noise Analysis of MOS Transistor

This section deals with a brief presentation of the noise sources known today. If there is no or little risk for confusion, the same name and index is used as in the original book or article, which means they can vary a little trough out this part of the report. A cross section of the MOS-transistor is shown in figure 2.5 and the complete transistor noise model is shown in figure 2.6.

2.3.1 Noise Sources

The noise sources dealt with in this section are the drain current thermal noise generated in the channel, the induced gate noise (which is partly correlated with the channel thermal noise) as well as the gate resistance thermal noise, the substrate noise and the flicker noise.

2.3.1.1 Drain Current Thermal Noise

When defining long channel and short channel devices from a noise point of view, it is not the actual length that is in question but the strength of the electric field, where high electric fields will cause velocity saturation and electron heating. As transistor geometries are shrinking, high-field effects are becoming important even at moderate biasing voltages.

Long Channel Devices

There are two expressions generally used for the thermal noise generated in the channel, and these are

$$\overline{i_d^2} = 4kT_{\overline{3}}^2 g_m \Delta f \tag{2.8}$$

and

$$i_d^2 = 4kT\gamma g_{d0}\Delta f \tag{2.9}$$

One way of retrieving equation 2.8 is presented by Tsividis [12], where the expression for the drain current is

$$I_{D} = -\mu W Q_{I}'(V_{CB}(x)) \frac{dV_{CB}(x)}{dx}$$
(2.10)

where Q_I ' is the inversion layer charge per unit area, x is the position along the channel and V_{CB} is the effective reverse bias in that point. An expression for the channel resistance ΔR in a small distance Δx is found to be, by using the fact that $\Delta V = I_D \Delta R$

$$\Delta R = \frac{\Delta x}{-\mu W Q_I'(V_{CB}(x))}$$
(2.11)

The noise voltage is then expressed as

$$\overline{\left(\Delta v_{t}\right)^{2}} = 4kT\Delta R\Delta f \qquad (2.12)$$

This noise voltage in the channel will affect the drain current of the transistor and by using the approximate strong inversion model and assuming saturation it is found that the drain noise current can be expressed as

$$\bar{i}_{d}^{2} = 4kT_{3}^{2}\mu C_{ox}(V_{GS} - V_{T})\Delta f = 4kT_{3}^{2}g_{m}\Delta f \qquad (2.13)$$

This is the most commonly used expression in simulator models and in literature [9,12,14].

van der Ziel [11] has a slightly different approach and gets equation 2.9 as a result. He expresses the drain current as

$$I_D = g(V_0) \frac{dV_0}{dx}$$
(2.14)

where the dc differential voltage $V_0 = V(x)$ and the unit length conductance $g(V_0) = g(x)$ appears at a distance x from the source.

At zero drain bias the conductance $g(V_0)=g_0$ all along the channel, so that

$$g_d = g_{d0} = \frac{g_0}{L}$$
(2.15)

Assuming there is a noise source h(x,t) in the channel, equation 2.14 must be replaced with

$$I_D + \Delta I_D(t) = g(V) \frac{dV}{dx} + h(x, t)$$
 (2.16)

where $V=V_0+\Delta V$ and $\Delta V(x,t)$ is caused by h(x,t). He then finds that the thermal noise of the conductance for a unit length is

$$\Delta S_{I_D}(f) = \frac{4kTg(x)}{\Delta x} \tag{2.17}$$

and that for the entire channel length (using equation 2.14 for variable substitution) it is

$$S_{I_D}(f) = \frac{1}{L^2} \int_0^L 4kTg(x)dx = \frac{4kT}{L^2} \int_0^L g^2(V_0)dV_0 = 4kT\gamma g_{d0}$$
(2.18)

where

$$\gamma = \frac{1}{g_0 L I_D} \int_0^L g^2(V_0) dV_0$$
 (2.19)

Equation 2.18 is valid up to reasonably high frequencies (no figure or relation given).

For a long channel in strong inversion γ is usually assumed to be 2/3 in saturation and one for V_{DS} equal to zero [10,4,16]. As far as noise concerned, van der Ziel claims that equation 2.19 can be expressed as

$$\gamma = \frac{1 - v + \frac{1}{3}v^2}{1 - \frac{1}{2}v}$$
(2.20)

where

$$v = \frac{V_D}{V_g - V_{g0}} \tag{2.21}$$

giving the claimed γ above. v is assumed to remain unity in saturation.

Tedja [16] has shown that g_{d0} can be measured as

$$g_{s} = \frac{\partial I_{D}}{\partial V_{s}} \bigg|_{V_{GB} = \text{ constant and } V_{D} \ge V_{Dsat}} = -g_{d0}$$
(2.22)

which means that the noise and g_{d0} can be measured for the same operating point.

As a first order approximation g_{d0} equals g_m in saturation. According to [10] the relation between g_m and g_{d0} is

$$\alpha = \frac{g_m}{g_{d0}} = \frac{1 + \rho/2}{(1 + \rho)^2}$$
(2.23)

where

$$\rho = \frac{V_{GS} - V_T}{L \cdot E_{sat}} \tag{2.24}$$

where E_{sat} is the velocity saturation electric field.

Short Channel Devices

There is no straight forward answer to what happens with the noise in short channel devices. For high field strengths, though, the mobility decreases as

$$\mu = \frac{\mu_0}{1 + \frac{E}{E_0}}$$
(2.25)

In addition the electron temperature increases. One assumption for this effect [11] is

$$\frac{T_e(x)}{T} = \left(1 + \frac{E}{E_c}\right)^n , n = 2, 1 \text{ or } 0$$
(2.26)

The noise can then be expressed as

$$S_{I_D}(f) = \frac{4kT}{L^2 I_{D_0}} \int_0^L \frac{T_e(x)}{T} g^2(V_0) dV_0 = 4kT\gamma g_{d_0}$$
(2.27)

which shows that it is γ that is affected.

Triantis [17] uses two different models for the electron heating. Below the critical field E_c it is

$$\frac{T_e(x)}{T_0} = 1 + \delta \left(\frac{E(x)}{E_c}\right)^2 , \quad \delta = 5 - 20$$
(2.28)

and above it is

$$\frac{T_e(x)}{T_o} = 2e^{\lambda \frac{E(x)}{E_c}} , \lambda = 1 - 2$$
(2.29)

None of the final expressions [11,15,17] for the thermal noise are simple or simplified enough for hand calculations. They are expressions useful for simulation models. One can assume though that γ is in the vicinity of 2 to 4 for short channel devices [10,13] when used in equation 2.27. The short channel effects are smaller for PMOS devices compared with the NMOS at the same operating point.

2.3.1.2 Gate Noise

Induced Gate Noise

Fluctuating channel potentials couples capacitively into the gate terminal, giving that the FET gate channel structure must be considered a distributed RC network, where the capacitive coupling represents the distributed capacitance and the channel the distributed resistance. The gate admittance, excluding high order terms, can the be expressed as

$$Y_{g} = j\omega C_{g} + g_{g} = j\omega C_{g} + \frac{1}{5} \frac{\omega^{2} C_{g}^{2}}{g_{d0}} \qquad , C_{g} = \frac{2}{3} C_{ox} wL \qquad (2.30)$$

In saturation and for a long channel device the thermal noise of g_g may be written as

$$\overline{i_g^2} = 4kT\delta g_g \Delta f \qquad , \delta = \frac{4}{3}$$
(2.31)

The gate noise and drain noise share a common origin, it is therefore important to know the auto correlations $\overline{i_d i_d}^*$ and $\overline{i_g i_g}^*$ and the crosscorrelation $\overline{i_g i_d}^*$ at higher frequencies. If we only use the first order terms [11] the result, for the long channel device, becomes

$$\overline{i_d i_d^*} = \overline{i_d^2} = \frac{2}{3} \cdot 4kTg_{d0}\Delta f \qquad (2.32)$$

$$\overline{i_g i_g^*} = \overline{i_g^2} = \frac{4}{3} \cdot 4kTg_g\Delta f$$
(2.33)

$$\overline{i_g i_d^*} = \frac{1}{6} \cdot j \omega C_g 4 k T \Delta f$$
(2.34)

and the crosscorrelation coefficient

$$c = \frac{i_{g}i_{d}^{*}}{\sqrt{\overline{i_{g}i_{g}^{*}} \cdot \overline{i_{d}i_{d}^{*}}}} = j0.395$$
(2.35)

The final expression [4] for the gate noise is

$$\overline{i_g^2} = \overline{i_{g,u}^2} + \overline{i_{g,c}^2} = \underbrace{4kT\delta g_g(1 - |c|^2)\Delta f}_{uncorrelated} + \underbrace{4kT\delta g_g|c|^2\Delta f}_{correlated}$$
(2.36)

Manku [13] has simulated and plotted the real and imaginary part of the crosscorrelation coefficient as a function of frequency. The correlation is about 0.4 for lower frequencies but it decreases slightly as it gets closer to f_t (c≈j0.3). The real part is almost zero for all frequencies.

The precise behaviour of the gate noise for short channels are not known, but a crude approximation is that $\delta = 2\gamma$ also in the short channel domain [10].

Gate Resistance Thermal Noise

The noise contribution from the gate connection itself arises from its distributed resistance. This noise source can be modelled as a series resistance in the gate circuit.

$$\overline{v_g^2} = 4kTr_g\Delta f \tag{2.37}$$

The equivalent gate noise resistance (connected at one end) is given by [4,13,18,19] as

$$r_g = \frac{R_{\Box}W}{3n^2L} \tag{2.38}$$

where R_{\Box} is the sheet resistance and *n* is the number of gate fingers. If the gate is connected at both ends, r_g is reduced by a factor of 4. The factor arises from the distributed analysis of the gate. The gate noise is reduced by a large number of gate fingers.

2.3.1.3 Substrate Noise

The thermal noise voltage across the distributed substrate resistance induces a fluctuating substrate potential. The effect of the substrate noise, due to the bulk resistance R_b , can be defined in two different ways. The fluctuating substrate potential is coupled to the channel and the contribution to the drain current from the substrate can be defined as [14,16,21]

$$\overline{i_{db}^2} = 4kTR_b g_{mb}^2 \Delta f \tag{2.39}$$

The substrate voltage noise v_u can also be defined as a current directly injected to the gate through the gate-bulk capacitance[22]

$$\overline{i_u^2} = \frac{4kT}{R_b} \left| \frac{j\omega C_{gb} R_b}{1 + j\omega C_{gb} R_b} \right|^2 \Delta f$$
(2.40)

The bulk resistance can be approximated from one end of the device layout to the other as

$$R_b = \frac{\rho \cdot L_{trans}}{W_{trans} \cdot T}$$
(2.41)

where L_{trans} is the device layout length and W_{trans} is the device layout width. No analysis of the distributed nature of the bulk resistance have been found or made, as it is beyond the scope of this thesis. To use a lot of gate fingers increases L_{trans} and reduces W_{trans} and thereby increase the bulk resistance.

2.3.1.4 Flicker Noise

Flicker noise is prominent in devices that are sensitive to the surface phenomenon, giving that it is a bigger problem in CMOS than in bipolar transistors.

The precise mechanisms involved in 1/f noise is not known. The flicker noise may be expressed as [10,12]

$$\overline{i}_{f}^{2} = \frac{K}{f} \cdot \frac{g_{m}^{2}}{WLC_{ax}^{2}} \Delta f$$
(2.42)

It shows that a large area and a thin dielectric gives a small noise. A crude estimate [10] of $K\approx 10^{-28}$ C²/m² in a PMOS transistor and it is about 50 times larger in an NMOS transistor. The parameter varies between processes and even among batches of the same process.

As the flicker noise increases with decreasing frequency, there will be a corner frequency where the flicker noise has the same power as the sum of the other noise sources, all referred to the same port. Flicker noise is usually not a problem for an LNA in the RF domain.

2.3.2 Transistor Noise Model

The final noise model for a MOS transistor, with the different noise sources described in section 2.3.1.1 to 2.3.1.4, is shown in figure 2.6. Two different models for the substrate noise were introduced insection 2.3.1.3 and depending on the model chosen either figure 2.6a) or b) should be used.

Example 3 Comparing noise sources

The purpose is to show the difference between the noise sources in the NMOS and PMOS transistors, as well as finding the sources that are the main contributors to the noise.

Data from the symmetric amplifier (PMOS/NMOS) is found in table 2.1

<i>f</i> =1.8GHz	$R_{\Box} = 15\Omega/\text{square}$	α=1 δ	5=4/3 γ=	2/3
W _{trans} =9.6µm/	$23.3\mu m$ $L_{trans}=3^{\circ}$	7.7μm <i>T</i> =7	7.24e-04m	$ ho_{epi}$ =11.8 Ω *cm
C_{ox} =4.6fF/µm	² <i>k</i> =1.38e-23	Temp=300K	<i>R_b</i> =64	0Ω/1.86kΩ
is the ratio betv	veen g_m and g_{d0} , se e	equation 2.23, a	nd as γ=2/3 i	t is assumed that equation

 α is the ratio between g_m and g_{d0} , se equation 2.23, and as $\gamma=2/3$ it is assumed that equation 2.8 is valid for the drain current thermal noise. The result is tabulated in table 2.2.

From table 2.2 it is seen that the noise sources i_u , which is the Norton equivalent of v_u , and i_f is much smaller than i_d and i_g . i_{db} on the other hand could be very important but is a very uncertain figure. Using equation 2.44 to translate i_d to an equivalent voltage noise source at the input reveals that it is much larger than the noise voltage v_g . Its equivalent current noise source at the input is larger than i_g (about 2.5 times) but not much larger, therefore i_d and i_g are the two most important noise sources.

Comparing i_f with i_d reveals that the corner frequency for the flicker noise is about 88kHz for the PMOS transistor, while it is 11MHz for the NMOS transistor.



a)



b)

Figure 2.6: Noise model for an MOS transistor where either a) eq. 2.39 or b) eq. 2.40 is valid.

Table 2.1: Small signal parameters for the inverter with *L*=0.35µm and 24 gate fingers.

SSP	<i>g_m</i> (mS)	<i>g_{mb}</i> (mS)	c _{gs} (fF)	c _{gd} (fF)	c _{gb} (fF)	Width (µm)
NMOS	12.7	3.29	127	13.1	0.78	67.2
PMOS	12.5	2.06	230	47.6	1.16	174

 Table 2.2: Noise sources for an NMOS and a PMOS transistor.

Source	$\overline{v_g^2}$	$\overline{i_{db}^2}$	$\overline{i_u^2}$	$\overline{i_f^2}$	$\overline{i_g^2}$	$\overline{i_d^2}$
PMOS	17.9e-21	45e-24	825e-30	31.2e-30	2.38e-24	138e-24
NMOS	6.91e-21	335e-24	5.30e-27	4.13e-27	718e-27	140e-24



Figure 2.7: a) ABCD-matrix. b) Simple MOS model with equivalent input noise sources.

2.3.3 Equivalent Noise Model

An equivalent noise model is used to calculate the overall noise figure of the circuit. The noise sources therefore has to be translated to the input port of the circuit. C_{gd} in figure 2.6 is considered as a part of the feedback and will not be included in the analysis.

An analysis is made to ensure that the noise of the inverter does not ruin the overall noise figure of the amplifier compared with a single transistor stage. First an equivalent noise model is given for the single MOS transistor. Then the equivalent noise model for the inverter is developed and finally the noise performance of the circuits are compared.

2.3.3.1 Two-Port Model for a MOS-Transistor

The transmission parameters [20], see figure 2.7a), of a two-port is

$$v_i = Av_o + Bi_o$$

$$i_i = Cv_o + Di_o$$
(2.43)

and if C_{gd} is considered to be part of the feedback, a simple model for a MOS-transistor, as shown in figure 2.7b), gives the following transmission parameters

$$A = \frac{v_i}{v_o}\Big|_{i_o = 0} = 0 \qquad B = \frac{v_i}{i_o}\Big|_{v_o = 0} = -\frac{1}{g_m}$$

$$C = \frac{i_i}{v_o}\Big|_{i_o = 0} = 0 \qquad D = \frac{i_i}{i_o}\Big|_{v_o = 0} = -\frac{sC_{gs}}{g_m}$$
(2.44)

The reciprocal value of the transmission parameters are known as: voltage gain (1/A), transconductance (1/B), transresistance (1/C) and current gain (1/D).

The noise sources considered most important are i_d and i_g , therefore only these two will be included in the analysis and the rest are ignored. The equivalent transistor input noise sources, see figure 2.7b), will then be

$$i_{ia} = i_d \cdot \frac{j\omega C_{gs}}{g_m} + i_{g,c} + i_{g,u}$$

$$v_{ia} = i_d \cdot \frac{1}{g_m}$$
(2.45)

Observe that some of the sources are correlated, which will be important when the power of the total equivalent noise voltage is calculated. They are random sources with a power value and not signal sources with a given amplitude and phase, giving that the sources can only be added as power values. For simplicity and visibility the sources are expressed as complex voltage and current sources, which is true for the instant values and as long as the noise sources i_d and i_g are treated separately.

2.3.3.2 Two-Port Model for an Inverter

As the inverter is a parallel connection of two complementary devices, it is necessary to calculate the transmission parameters for the inverter as well. It is assumed that the two transistors can be biased in such a way that the parameters becomes identical.

From figure 2.8a) a new transmission matrix for the inverter is found as

$$v_{i} = v_{i1} = v_{i2} = Av_{o1} + Bi_{o1} = Av_{o2} + Bi_{o2}$$

$$i_{i} = i_{i1} + i_{i2} = Cv_{o1} + Di_{o1} + Cv_{o2} + Di_{o2}$$
(2.46)

and if

$$i_o = i_{o1} + i_{o2}$$
 $i_{o1} = i_{o2}$ $v_o = v_{o1} = v_{o2}$ (2.47)

the new transmission parameters reduces to

$$v_i = Av_o + \frac{B}{2}i_o$$

$$i_i = 2Cv_o + Di_o$$
(2.48)

This means that the new transconductance and the new input capacitance is twice that of the individual transistors in the inverter.

$$A = 0 \qquad B = -\frac{1}{2 \cdot g_m}$$

$$C = 0 \qquad D = -\frac{sC_{gs}}{g_m} = -\frac{2 \cdot sC_{gs}}{2 \cdot g_m}$$
(2.49)

As the transistors are in parallel the equivalent noise sources will be affected as well. The current sources are simply added together as they already are in parallel. The noise source may be conveniently transformed to currents using the transmission matrix. The transmission matrix including the noise voltage source is

$$v_i - v_{ia} = Av_o + Bi_o$$

$$i_i = Cv_o + Di_o$$
(2.50)

By moving the noise voltage source to the right-hand side of the equation it can be expressed as a part of the output current

$$v_i = Av_o + B\left(i_o + \frac{v_{ia}}{B}\right)$$

$$i_i = Cv_o + Di_o$$
(2.51)

The total output current should be the same in the both equations, giving

$$v_{i} = Av_{o} + B\left(i_{o} + \frac{v_{ia}}{B}\right)$$

$$i_{i} + D\frac{v_{ia}}{B} = Cv_{o} + D\left(i_{o} + \frac{v_{ia}}{B}\right)$$
(2.52)

From figure 2.8b)-d) it is then seen that the new equivalent noise sources and the noise spectrum, S, of the symmetric inverter becomes

$$i_{ias} = i_{ia1} + i_{ia2} \qquad S(i_{ias}) = 2S(i_{ia}) v_{ias} = v_{ia1}/2 + v_{ia2}/2 \qquad S(v_{ias}) = S(v_{ia})/2$$
(2.53)

where $i_{ia} = i_{ia1} = i_{ia2}$ and $v_{ia} = v_{ia1} = v_{ia2}$.

2.3.3.3 Noise Comparison

To see if we have improved the noise performance or not by using an inverter, we should compare it with a single transistor of twice the width of one of the transistors in the inverter, e.g. the NMOS transistor. This gives us the same g_m but with twice the current consumption. It is assumed, for the moment, that C_{gs} is of the same size as well for both transistors. The equivalent noise spectrum of the single large transistor are denoted $S(i_{ia2w})$ and $S(v_{ia2w})$.

It is assumed the two noise sources of importance are the drain current thermal noise, i_d , and the induced gate noise, i_g , see chapter 2.3. This means that the current noise spectrums are proportional to transistor size, with $g_m = \alpha \cdot g_{d0}$, as

$$S(i_d) \sim g_{d0}$$
 $S(i_g) \sim \frac{C_{gs}^2}{g_{d0}}$ (2.54)





Figure 2.8: a) Parallel connection of complementary devices. b) Noise transformation for one device. c) Connecting devices in parallel and d) final transmission matrix.

see equation 2.9 and equations 2.30 and 2.31, respectively. The equivalent current noise spectrum of one of the transistors in the inverter, compared with the single transistor, then is

$$S(i_{ia}) = \frac{1}{2}S(i_{ia2w})$$
(2.55)

as g_{d0} and C_{gs} is half of that in the single large transistor, giving that the total noise current of the inverter is equal to that of the single large transistor, see equations 2.53.

The equivalent voltage noise spectrum is

$$S(v_{ia}) \sim \frac{g_{d0}}{g_m^2}$$
 (2.56)

giving that the noise power of one of the transistors in the inverter, compared with the single transistor, is

$$S(v_{ia}) = 2S(v_{ia2w})$$
 (2.57)

Once again the total noise of the inverter is equal to that of the single large transistor.

What we gain by using an inverter instead of one large transistor is a reduction of current consumption and increased linearity, see section 2.2.3. The error made by assuming that C_{gs} is the same for both devices in the inverter, is the difference in the gate induced noise, which is smaller in an NMOS transistor due to the smaller capacitance.

2.4 Transadmittance Amplifier

In a high frequency receiver it is important to keep the reflection coefficient as small as possible. Reflection can occur when the distance between two components is large enough for the connecting wire to become a transmission line. To avoid reflection the loading impedance should be matched to the impedance seen from the transmission line. It is therefore important to be able to control the input impedance of the LNA.

The inductive degeneration in the inverter gives a capacitive part in input impedance as well as a resistive part. The capacitive part can be cancelled with the input inductance L_g to give a completely resistive input impedance. This will affect the gain of the circuit, which will be investigated.

To minimize the noise in a receiver chain the first stage should have a high gain, to reduce the influence of the following stages, and still contribute very little to noise itself. The noise factor is analysed both with the gate drain capacitance C_{gd} excluded and included, as well as excluding and including the gate induced noise i_g .

2.4.1 Input Impedance

In the most simple model for the feedback of the transistor circuit, only the inductive source degeneration is included, neglecting the gate drain shunt capacitance. The simple model in figure 2.9 will be analysed first to explain the principle to retrieve a resistive part in the input impedance. As reality is a little bit more complex the more complicated model in figure 2.10 is analysed to retrieve a useful model.



Figure 2.9: A simple model of the MOS-transistor with an inductive series feedback.

2.4.1.1 Calculation Using Simplified MOS Model

In the simple model all small signal components are excluded, except the gate source capacitance. The simplified model of the MOS-transistor with inductive feedback is shown in figure 2.9 and analysis shows that the input impedance becomes

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{L_s \cdot g_m}{C_{gs}}$$
(2.58)

As g_m/C_{gs} remains fairly constant with size of the transistor (once it is biased), the resistive part of the input impedance is finally set by the inductance L_s in equation 2.58.

All that is needed now is to connect an inductance L_g in series with the input, see figure 2.2, so that the input impedance will be purely resistive at the desired frequency, giving that

$$\omega_0^2 C_{gs} (L_s + L_g) = 1 \tag{2.59}$$

The basic necessity for equation 2.58 to hold is that the influence of all other small signal parameters in the transistor are negligible.

2.4.1.2 Calculation Using Complete MOS Model

In figure 2.10 it is seen that the calculation of the impedance can be divided into two parts. First Z_f is calculated with Blackman's formula, see appendix A.1, for the part of the input impedance affected by feedback and then the final impedance Z_{in} as

$$Z_{in} = X_{gb} \parallel Z_f \tag{2.60}$$

The input impedance of the feedback part becomes

$$Z_{f} = \frac{(X_{gs} + X_{bs} \| Z_{s}) \cdot \left(1 + \frac{R_{l} \| X_{db}}{X_{gd}} + \frac{R_{l} \| X_{db}}{r_{d}}\right) + X_{gs} \cdot X_{bs} \| Z_{s} \cdot \left(g_{m} + \frac{1}{r_{d}}\right) \cdot \left(1 + \frac{R_{l} \| X_{db}}{X_{gd}}\right)}{1 + (X_{bs} \| Z_{s} + R_{l} \| X_{db}) \cdot \left(\frac{1}{r_{d}} + \frac{1}{X_{gd}}\right) + \frac{X_{gs}}{X_{gd}} \cdot \left(1 + \frac{X_{bs} \| Z_{s}}{r_{d}} + \frac{R_{l} \| X_{db}}{r_{d}} + (X_{gs} + X_{bs} \| Z_{s}) \cdot g_{m}\right)}$$
(2.61)

which is a complex expression. It is therefore necessary to introduce some conditions, to be able to simplify the expression.



Figure 2.10: The complete small signal model of a MOS-transistor with inductive series feedback.

The circuit should operate as a transconductance with an inductive feedback. Therefore the load should be regarded as small giving that

$$R_l \parallel X_{db} \approx R_l \qquad r_d \gg R_l \tag{2.62}$$

so that the output current i_d goes through the load. For the feedback to be inductive the requirements are

$$X_{bs} \parallel Z_s \approx Z_s \qquad Q_{ind} \ge 3 \tag{2.63}$$

The operating point of the transistor should give that

$$r_d \gg r_s \qquad g_m \gg \frac{1}{r_d}$$
 (2.64)

By applying these conditions and calculating the input impedance from equation 2.60 and 2.61 it still becomes a huge expression with numerous frequency dependent terms (some of them of resonant nature). By identifying the major contributions to the input resistance it is found to be

$$Re(Z_{in}) \approx \frac{\frac{L_s}{C_{gs}}g_m \left(1 + \frac{C_{gd}}{C_{gs}}g_m R_L (1 - \omega^2 L_s (C_{gd} + C_{gb}))\right) + r_s \left(1 + \frac{C_{gd}}{C_{gs}}g_m R_L \left(1 + \frac{C_{gd}}{C_{gs}}(2 + g_m (R_L + r_s))\right)\right)}{\left(1 + \frac{C_{gd}}{C_{gs}}g_m R_L + \frac{C_{gd} + C_{gb}}{C_{gs}}(1 + g_m r_s) - \omega^2 L_s (C_{gd} + C_{gb})\right)^2 + \left(\omega C_{gd} \left(\left(r_s + \frac{L_s}{C_{gs}}g_m\right)\left(1 + \frac{C_{gb}}{C_{gd}}\right) + R_L (1 - \omega^2 L_s C_{gb}) + \frac{L_s}{C_{gd} r_d}\right)\right)^2}$$

$$(2.65)$$

As seen in the equation the terms are collected in groups (depending on e.g. $L_s g_m / C_{gs}$) and subgroups making it possible to make sensible comparisons to facilitate further simplifications.
g_m	g _{ds}	c _{bd}	c_{bs}	c_{gs}	c_{gd}	c_{gb}	g_m/I_d
23e-3	630e-6	44e-15	115e-15	235e-15	95e-15	30e-15	3.1

Table 2.3: Data for the nominal NMOS transistor ($0.6\mu m$ process), with X=1.

Example 4 Simulation of Input Impedance

The purpose is to show how the input resistance of an NMOS transistor is dependant on the inductive source degeneration, the size of the transistor and the operating frequency. The desired operating frequency is 2GHz and the desired input resistance is 50Ω . The evaluation is made both in Matlab and Cadence.

Equation 2.65 is used in Matlab to find the input resistance as a function of the inductance, L_s , for a fixed operating frequency of 2GHz. This was repeated for four different scalings, X, of the nominal width of the transistor shown in table 2.3 and plot in figure 2.11, where the desired input resistance of 50 Ω also is shown.

The simulations of the input impedance were repeated in the Spectre circuit simulator in Cadence and the scattering parameter S_{II} is plotted in figure 2.12a) and b). The operating frequency of 2GHz is indicated with an additional marker for each curve. In figure 2.12a) the inductance is kept constant and the transistor size is varied around a nominal value. In figure 2.12b) the inductance is increased from a nominal value when trying to compensate for the lower resistance of the largest transistor.

The simulations in example 4 shows that for small sizes of the transistor and small values of the inductance the resistance is linearly dependent on the inductance value and independent of the transistor size. This is seen in figure 2.11, as the resistance for *X* equal to 0.5 and 1 are almost equal up to an inductance of 2nH, and in figure 2.12a) are both the 2GHz markers on the 50 Ω circle.

The transistor size for X equal to 2 renders a slightly lower resistance for the constant inductance value in figure 2.12a) but as seen in figure 2.11 this can be compensated with a larger inductance value. But when the transistor has become too large it is not possible to compensate with a large inductance any more. In figure 2.11 and figure 2.12b) this is demonstrated by the fact that the input resistance of the largest transistor can not reach the desired 50 Ω , regardless of the size of the inductance. The result indicates that terms dependent on g_m (size) and frequency becomes to large and reduces the input resistance. The difference in resistance between figure 2.11 and figure 2.12b) is due to the fact that equation 2.65 is a less complex model and therefore a little bit optimistic about how large the resistance can be for large inductance values and large transistor widths.

To be able to control the input resistance as well as the gain and the noise of the circuit there is a maximum available transistor size, dependent on operating frequency and resistance.



Figure 2.11: R_{in} as a function of L_s according to equation 2.65



Figure 2.12: Smith charts of S_{II} for a) constant inductance and four different transistor sizes and for b) the largest transistor with three different inductor sizes.

2.4.1.3 Calculation Using New Simplified MOS Model

When scaling the transistor to a small size, giving a small conductance, and operating the transistor at a low frequency, equation 2.65 reduces to

$$Re(Z_{in}) \approx \frac{\frac{L_s}{C_{gs}}g_m + r_s}{\left(1 + \frac{C_{gd} + C_{gb}}{C_{gs}}\right)^2}$$
(2.66)

The capacitors in the small signal model of a MOS-transistor [12] consist of an intrinsic part (a change of gate and depletion charges) and of an extrinsic part (the gate overlap, gate-wiring and junction capacitances). The intrinsic capacitances of C_{gd} and C_{gs} are of equal size when the transistor is operated in nonsaturation, and C_{gd} becomes much smaller than C_{gs} in saturation. The extrinsic capacitances though are of the same size and remains the same independent of operating point.

As silicon dimensions of the silicon process is reduced, the relation between the intrinsic and extrinsic part of the capacitance may change. Unfortunately this will increase the influence of the extrinsic capacitance, giving that C_{gd} can be as much as 1/5 or 1/7 of C_{gs} instead of 1/15 or smaller. This means that the input resistance can become up to 30% smaller than expected, only due to the increased gate drain capacitance.

The input impedance of a reduced model, only containing C_{gd} , C_{gs} and g_m , has been calculated in appendix A.3. A rough estimate of the input impedance for this model is

$$Z_{in} \approx \frac{j\omega L_s + \frac{1}{j\omega C_{gs}}}{1 + \frac{C_{gd}}{C_{gs}}} + \frac{\frac{L_s}{C_{gs}}g_m}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^2}$$
(2.67)

Comparing with the simplified expression for the input impedance given by equation 2.58 it is seen that C_{gd} now has an influence on both the reactance and the resistance.

2.4.2 Gain of Transadmittance

To calculate the overall gain A_g of the circuit the tuning inductor L_g and the source resistance R_g have to be included, as shown in figure 2.13. The small signal model has been reduced to only contain C_{gd} , C_{gs} and g_m . First an analysis is made where C_{gd} is excluded as well, to be able to compare the gain with the gain when it is present. Expressions for the different gain at resonance have been derived in appendix B.2.

2.4.2.1 Calculation Using Simplified MOS Model

It has been recognized before [26] that the input circuit consists of a series-resonant network. An equivalent circuit of the input circuit in figure 2.13 is shown in figure 2.14, where the feedback circuit has been replaced with its input impedance from equation 2.58, where

$$R_g = \frac{g_m}{C_{gs}} L_s \tag{2.68}$$

This reveals that the overall transconductance A_g at resonance is dependent on the Q-value of the equivalent circuit, i.e.

$$A_{g} = \frac{i_{l}}{v_{g}} = \frac{-g_{m}}{j\omega_{0}C_{gs}R_{g} + j\omega_{0}L_{s}g_{m}} = \frac{-g_{m}}{j\omega_{0}C_{gs}\left(R_{g} + \frac{g_{m}}{C_{gs}}L_{s}\right)} = jg_{m}Q_{in} = \frac{-\omega_{T}}{2j\omega_{0}R_{g}}(2.69)$$

What is seen is that the overall gain is independent on the width of the transistor. For a reduced size g_m will decrease and the Q-value increase, giving that the gain is only dependent on transition frequency f_T , operating frequency f_0 and the generator resistance R_g .

2.4.2.2 Calculation Using New Simplified MOS Model

As C_{gd} is included in the model it represents a second feedback path and thereby gives a more complicated expression for the input impedance of the amplifier. From equation 2.67, which is the input impedance of the reduced model, the new equivalent circuit of figure 2.13 becomes as in figure 2.15, where

$$R_g = \frac{\frac{L_s g_m}{C_{gs}}}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^2}$$
(2.70)

The overall transconductance A_g at resonance then becomes

$$A_{g} \approx \frac{-g_{m}}{j\omega_{0}(C_{gs} + C_{gd})R_{g} + j\omega_{0}L_{s}g_{m}} = \frac{-g_{m}}{j\omega_{0}C_{gs}\left(1 + \frac{C_{gd}}{C_{gs}}\right)R_{g} + \frac{j\omega_{0}L_{s}g_{m}}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)}\left(1 + \frac{C_{gd}}{C_{gs}}\right)}$$
$$= \frac{-g_{m}}{\frac{j}{2Q_{in}} + \frac{j}{2Q_{in}}\left(1 + \frac{C_{gd}}{C_{gs}}\right)} = j\frac{2Q_{in}g_{m}}{2 + \frac{C_{gd}}{C_{gs}}} = \frac{1}{2 + \frac{C_{gd}}{C_{gs}}} \cdot \frac{-g_{m}}{j\omega_{0}(C_{gs} + C_{gd})R_{g}} = \frac{-\omega_{T}}{\left(2 + \frac{C_{gd}}{C_{gs}}\right)j\omega_{0}R_{g}}$$



Figure 2.13: Reduced small signal model for the first stage of the LNA.



Figure 2.14: Equivalent input circuit with C_{gd} neglected.



Figure 2.15: Equivalent input circuit with C_{gd} included.

where

$$\omega_T' = \frac{g_m}{C_{gs} + C_{gd}} \tag{2.72}$$

Equation 2.71 is still independent on transistor width. Due to the gate drain capacitance the overall gain is reduced both as $\omega_T' < \omega_T$ and $(2 + C_{gd}/C_{gs}) > 2$.

2.4.3 Noise Factor

In the previous sections the input impedance and the gain of the input stage is treated. There it is found that the gate drain capacitance, C_{gd} , affects the gain and the input impedance. Therefore its effects on the noise will be investigated as well. But first an analysis is given of the simplified circuit, see figures 2.9 and 2.14, as most articles and books deals with the noise when the effect of C_{gd} is neglected. e.g.[4,26]. Then the analysis is repeated but with C_{gd} included, see figures 2.13 and 2.15.

The analysis of the total equivalent noise voltage is made in appendix C and the current thermal noise i_d in the channel and the induced gate noise i_g are considered the most important noise sources, see section 2.3.2.

2.4.3.1 Noise Factor of Simplified MOS Model

From a noise point of view the inductance L_s is going to appear in the input circuit, see figure 2.14, and affect the equivalent noise sources, as the total equivalent noise voltage of the feedback circuit with zero gate drain capacitance is (from equation C.76)

$$v_{eT} = v_{ia} + (R_g + j\omega_0 (L_g + L_s))i_{ia}$$
(2.73)

where i_{ia} and v_{ia} is given by equation 2.45. The noise current i_{ia} can be expressed as a noise voltage independent of the inductances.

$$v_{iia} = (R_g + j\omega_0(L_s + L_g))i_{ia} = R_g \left(1 + j\frac{1}{\omega_0 C_{gs} R_g}\right)i_{ia}$$
(2.74)

In equation 2.74 it is the Q-value of the input circuit that is used to remove the dependency on the inductors at resonance.

The total equivalent input noise voltage is then

$$v_{eT} = v_{ia} + v_{iia} = \frac{j\omega_0 C_{gs} R_g}{g_m} i_d + R_g \left(1 + j\frac{1}{\omega_0 C_{gs} R_g}\right) (i_{g,c} + i_{g,u})$$
(2.75)

where i_d and $i_{g,c}$ are correlated.

Noise Factor with i_g Neglected

If i_g is negligible then the noise voltage power becomes

$$\overline{v_{eT}^2} = \left(\frac{\omega_0 C_{gs} R_g}{g_m}\right)^2 \cdot 4kT\gamma g_{d0}\Delta f$$
(2.76)

Defining the generator noise voltage power as

$$\overline{v_g^2} = 4kTR_g\Delta f \tag{2.77}$$

(Observe that this is *not* the thermal noise of the gate resistance this time, but the noise voltage of the generator resistance.)

If ρ remains constant with the scaling of the transistor, then α remains constant as well and it is possible to exchange g_{d0} with g_m , see equation 2.23. Then the noise factor becomes [4,26] (with $\omega_T = g_m / C_{gs}$)

$$F = 1 + \frac{v_{eT}^2}{\overline{v_g}^2} = 1 + R_g \frac{\gamma}{\alpha} g_m \left(\frac{\omega_0}{\omega_T}\right)^2$$
(2.78)

This result implies that the transistor transconductance should be as small as possible. The generator resistance, and thereby the input resistance, should also be as small as possible.

Noise Factor with i_g Included

In the case when the gate noise is included the noise voltage power becomes (using equation 2.30 and 2.36)

$$\overline{v_{eT}^{2}} = \left| \frac{j\omega_{0}C_{gs}R_{g}}{g_{m}} \sqrt{4kT\gamma g_{d0}} + \left(1 + j\frac{1}{\omega_{0}C_{gs}R_{g}}\right)R_{g}\sqrt{\delta 4kTg_{g}|c|^{2}} \right|^{2}\Delta f + \left| \left(1 + j\frac{1}{\omega_{0}C_{gs}R_{g}}\right)R_{g}\sqrt{\delta 4kTg_{g}(1 + |c|^{2})} \right|^{2}\Delta f \\
= 4kT\left(\left(\frac{\omega_{0}C_{gs}R_{g}}{g_{m}}\right)^{2}\gamma g_{d0} + 2|c|\frac{\omega_{0}C_{gs}R_{g}}{g_{m}}\sqrt{\frac{\gamma\delta}{5}} + \frac{\delta}{5g_{d0}} + \left(\omega_{0}C_{gs}R_{g}\right)^{2}\frac{\delta}{5g_{d0}}\right)\Delta f$$
(2.79)

Assuming that ρ and α , in equation 2.23, remains constant with the scaling of the transistor. The total noise voltage power can then be written as (with $\omega_T = g_m / C_{gs}$)

$$\overline{v_{nT}^{2}} = 4kT \left(R_{g} + \frac{\omega_{0}^{2}}{\omega_{T}^{2}} R_{g}^{2} \left(\frac{\gamma}{\alpha} + \frac{\delta\alpha}{5} \right) g_{m} + \frac{\delta\alpha}{5} \frac{1}{g_{m}} + 2|c| \frac{\omega_{0}}{\omega_{T}} R_{g} \sqrt{\frac{\gamma\delta}{5}} \right) \Delta f$$
(2.80)

The noise factor contains terms that are proportional both to g_m and l/g_m

$$F = 1 + \frac{\omega_0^2}{\omega_T^2} R_g \left(\frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\right) g_m + \frac{\delta\alpha}{5R_g} \frac{1}{g_m} + 2|c| \frac{\omega_0}{\omega_T} \sqrt{\frac{\gamma\delta}{5}}$$
(2.81)

By differentiating equation 2.81 with respect to g_m the optimum transconductance g_{mopt} is found to be

$$g_{mopt} = \frac{\omega_T}{\omega_0 R_g \sqrt{1 + \frac{5\gamma}{\delta \alpha^2}}}$$
(2.82)

The minimum noise factor is then given by (see also $[4]^1$)

$$F_{min} = 1 + 2\frac{\omega_0}{\omega_T} \sqrt{\frac{\gamma \delta}{5}} \left(\sqrt{1 + \frac{\delta \alpha^2}{5\gamma}} + |c| \right)$$
(2.83)

It is seen from equation 2.83 that the minimum noise is increased with frequency. The noise factor increases with high electric fields as, γ and δ will increase. A small α will reduce the noise factor, but γ and δ has a stronger influence. The noise figure is low when the transistor is working as a long channel device at low frequencies.

2.4.3.2 Noise Factor of New Simplified MOS Model

The gate drain capacitance changes the equivalent input capacitance and inductance of the circuit, figure 2.15, which in turn will affect the equivalent noise voltage source v_{iia} in equation 2.74. Once again it is important that the final noise figure is independent of the inductors, to be able to do the same transformation as in equation 2.74. To be able to do this it is necessary to make some assumptions, see appendix C.3, and one of them are that the input impedance is matched, giving

$$R_g = \frac{\frac{L_s}{C_{gs}}g_m}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^2}$$
(2.84)

The total equivalent noise voltage then is (from equation C.85)

$$v_{eT} = v_{ia} + \left(R_g + j\omega_0 \left(L_g + \frac{L_s}{1 + \frac{C_{gd}}{C_{gs}}} \right) \right) i_{ia}$$
(2.85)

¹[4,26] has also made an extended analysis with different optimizations. Fixed amplifier transadmittance and fixed power consumption.

2.4 Transadmittance Amplifier

and the noise current i_{ia} can then be transformed into a noise voltage independent of the inductances as

$$v_{iia} = \left(R_g + j\omega_0 \left(L_g + \frac{L_s}{1 + \frac{C_{gd}}{C_{gs}}} \right) \right) i_{ia} = R_g \left(1 + j \frac{1}{\omega_0 (C_{gs} + C_{gd}) R_g} \right) i_{ia}$$
(2.86)

In equation 2.86 the Q-value of the input circuit in figure 2.15 is used to remove the dependency on the inductors at resonance.

The total equivalent input noise voltage is then

$$v_{eT} = v_{ia} + v_{iia}$$

$$= \left(\frac{1}{g_m} \frac{C_{gd}}{C_{gs} + C_{gd}} + \frac{j\omega_0 C_{gs} R_g}{g_m}\right) i_d + R_g \left(1 + j \frac{1}{\omega_0 (C_{gs} + C_{gd}) R_g}\right) (i_{g,c} + i_{g,u})$$
(2.87)

where i_d and $i_{g,c}$ are correlated.

Noise Factor with i_g Neglected

If i_g is negligible then the total noise voltage power becomes

$$\overline{v_{nT}^2} = 4kT \left(R_g + \left(\left(\frac{1}{g_m} \frac{C_{gd}}{C_{gs} + C_{gd}} \right)^2 + \left(\frac{\omega_0 C_{gs} R_g}{g_m} \right)^2 \right) \cdot \gamma g_{d0} \right) \Delta f$$
(2.88)

Assuming that ρ and α , in equation 2.23, remains constant with the scaling of the transistor. The new noise factor can then be written as (with $\omega_T = g_m / C_{gs}$)

$$F = 1 + \frac{1}{R_g} \frac{\gamma}{\alpha} \frac{1}{g_m} \left(\frac{C_{gd}}{C_{gs} + C_{gd}} \right)^2 + R_g \frac{\gamma}{\alpha} g_m \left(\frac{\omega_0}{\omega_T} \right)^2$$
(2.89)

The noise factor in the equation above is different compared with equation 2.78, as the new noise factor is going to have a minimum dependent on the size of the transistor. There will also be a minimum versus the generator resistance.

Once again it is possible to use the scalability of the transistor, see section 2.2.5, to find the optimum size for a given operating point. Observe though that it is necessary to know the operating parameters for one transistor size and scale from that transistor.

Assuming the generator resistance is fixed the differentiation of the noise factor can be expressed as

$$\frac{dF}{dg_m} = 0 - \frac{1}{R_g} \frac{1}{g_m^2} \left(\frac{C_{gd}}{C_{gs} + C_{gd}} \right)^2 + R_g \left(\frac{\omega_0}{\omega_T} \right)^2 = 0$$
(2.90)

where

$$\frac{1}{R_g} \left(\frac{C_{gd}}{C_{gs} + C_{gd}} \right)^2 \tag{2.91}$$

remains constant with the change of size.

The optimum transconductance is then

$$g_{mopt} = \frac{\omega_T C_{gd}}{R_g \omega_0 (C_{gs} + C_{gd})}$$
(2.92)

and the minimum noise factor becomes

$$F_{min} = 1 + 2\frac{\omega_0}{\omega_T} \frac{\gamma}{\alpha} \frac{C_{gd}}{C_{gs} + C_{gd}}$$
(2.93)

In equation 2.78 the transconductance should be as small as possible for a low noise factor. This is also the result of equations 2.92 and 2.93, as the minimum noise figure will be 0dB and the optimum transconductance 0mS, if $C_{gd}=0$. The result in equation 2.93 is probably not that close to the truth either, regarding the result given equation 2.83.

Noise Factor with i_g Included

In the case when the gate noise is included the equivalent noise voltage power becomes (using equation 2.30 and 2.36)

$$\overline{v_{eT}^{2}} = \left| \left(\frac{1}{g_{m}} \frac{C_{gd}}{C_{gs} + C_{gd}} + \frac{j\omega_{0}C_{gs}R_{g}}{g_{m}} \right) \sqrt{4kT\gamma g_{d0}} + \left(1 + j\frac{1}{\omega_{0}(C_{gs} + C_{gd})R_{g}} \right) R_{g} \sqrt{\delta 4kTg_{g}|c|^{2}} \right|^{2} \Delta f + (2.94) + \left| \left(1 + j\frac{1}{\omega_{0}(C_{gs} + C_{gd})R_{g}} \right) R_{g} \sqrt{\delta 4kTg_{g}(1 + |c|^{2})} \right|^{2} \Delta f \\
= 4kT \left(\left(\frac{\omega_{0}C_{gs}R_{g}}{g_{m}} \right)^{2} \gamma g_{d0} + \frac{1}{g_{m}^{2}} \left(\frac{C_{gd}}{C_{gs} + C_{gd}} \right)^{2} \gamma g_{d0} + 2|c| \frac{\omega_{0}C_{gs}R_{g}}{g_{m}} \sqrt{\frac{1}{5}} + \frac{\delta}{5g_{d0}} \left(\frac{C_{gs}}{C_{gs} + C_{gd}} \right)^{2} + (\omega_{0}C_{gs}R_{g})^{2} \frac{\delta}{5g_{d0}} \right) \Delta f$$

Compared with equation one new term is added and another term is multiplied with a ratio, due to C_{gd} .

Assuming that ρ and α , in equation 2.23, remains constant with the scaling of the transistor. The new total noise voltage power can then be written as (with $\omega_T = g_m / C_{gs}$)

$$\overline{v_{nT}^{2}} = 4kT \left(R_{g} + \frac{\omega_{0}^{2}}{\omega_{T}^{2}} R_{g}^{2} \left(\frac{\gamma}{\alpha} + \frac{\delta\alpha}{5} \right) g_{m} + \frac{\left(C_{gs}^{2} + C_{gd}^{2} \frac{5\gamma}{\delta\alpha^{2}} \right)}{\left(C_{gs} + C_{gd} \right)^{2}} \frac{\delta\alpha}{5} \frac{1}{g_{m}} + 2|c| \frac{\omega_{0}}{\omega_{T}} R_{g} \sqrt{\frac{\gamma\delta}{5}} \right) \Delta f$$

$$(2.95)$$

2.4 Transadmittance Amplifier

with the noise factor

$$F = 1 + \frac{\omega_0^2}{\omega_T^2} R_g \left(\frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\right) g_m + \frac{\left(C_{gs}^2 + C_{gd}^2 \frac{5\gamma}{\delta\alpha^2}\right)}{\left(C_{gs} + C_{gd}\right)^2} \frac{\delta\alpha}{5R_g} \frac{1}{g_m} + 2|c| \frac{\omega_0}{\omega_T} \sqrt{\frac{\gamma\delta}{5}}$$
(2.96)

The difference between the equation above and equation 2.81 is the factor added to the third term. Notice that

$$\frac{C_{gs}^2 \frac{\delta \alpha}{5} + C_{gd}^2 \frac{\gamma}{\alpha}}{\left(C_{gs} + C_{gd}\right)^2}$$
(2.97)

remains constant with the scaling of the transistor. It is therefore still possible to get the optimum transconductance by differentiating F with respect to g_m .

$$g_{mopt} = \frac{\omega_T}{\omega_0 R_g \sqrt{1 + \frac{5\gamma}{\delta\alpha^2}}} \cdot \frac{\sqrt{\frac{C_{gs}^2}{C_{gd}^2} + \frac{5\gamma}{\delta\alpha^2}}}{\left(\frac{C_{gs}}{C_{gd}} + 1\right)}$$
(2.98)

The ratio between the equation above and equation 2.82 can be expressed as

$$M = \frac{1}{K+1} \sqrt{K^2 + \frac{5\gamma}{\delta\alpha^2}}$$
(2.99)

where $K = C_{gs}/C_{gd}$. For all K's larger than one and smaller than infinite, M will be smaller than one. By differentiating equation 2.99 with respect to K a minimum is found for

$$K_{opt} = \frac{5\gamma}{\delta\alpha^2}$$
(2.100)

and

$$M_{min} = \frac{1}{\sqrt{1 + \frac{\delta \alpha^2}{5\gamma^2}}}$$
(2.101)

which reveals that the optimum transconductance is reduced with the introduction of the gate drain capacitance in the model.

The minimum noise factor is found to be

$$F_{min} = 1 + 2\frac{\omega_0}{\omega_T} \sqrt{\frac{\gamma \delta}{5}} \left(\sqrt{\left(1 + \frac{\delta \alpha^2}{5\gamma}\right)} M + |c| \right)$$
(2.102)

2 Low Noise Amplifier



Figure 2.16: Simplified small signal model of a current follower with an LC-tank.

The difference between the equation above and equation 2.83 is the factor M, which will be smaller than one. In the process used for simulations, see section 2.7, C_{gd} is fairly large resulting in a smaller noise factor, for a smaller optimum transconductance.

2.5 Transresistance Amplifier

The small signal equivalent of a current follower (common gate amplifier) with a resonant tank is shown in figure 2.16, including the input admittance of the source voltage follower. The input admittance of the follower is included as it will have an influence on the resonance frequency and the Q-value of the tank. The current follower is going to be a load to the inverter stage and transform the input current to a voltage output signal in the resonant tank. At resonance the load is equal to

$$(j\omega L_c + r_c) \parallel \frac{1}{j\omega C_2} \parallel \frac{1}{g_f} = [\omega = \omega_0] = R_{pc}$$
 (2.103)

The capacitances are

$$C_1 = C_{gsc} + C_{bsc} \text{ and } C_2 = C_{gdc} + C_{bdc} + C_f$$
 (2.104)

where C_f is the input capacitance of the source voltage follower.

2.5.1 Input Impedance

Traditionally the input impedance of a common gate amplifier is considered to be $1/g_{mc}$, which is true in an ideal situation, where r_{dc} is infinite and the input capacitance C_1 is zero. The real input impedance is

$$Z_{c} = \frac{1}{j\omega C_{I}} \| \frac{r_{dc} + \frac{1}{j\omega C_{2}} \| (j\omega L_{c} + r_{c}) \| \frac{1}{g_{f}}}{1 + r_{dc}g_{mc}} = [\omega = \omega_{0}]$$
(2.105)
$$= \frac{1}{j\omega_{0}C_{I}} \| \frac{r_{dc} + R_{pc}}{1 + r_{dc}g_{mc}} \approx \frac{1}{j\omega_{0}C_{I}} \| \frac{1}{g_{mc}} \left(1 + \frac{R_{pc}}{r_{dc}} \right)$$

The input impedance of the current follower, in figure 2.16, is affected by the resonant tank, giving an increase of the input resistance. This is not good as a larger load will jeopardise the assumptions in equation 2.62, that the load must be much smaller than the output impedance of the transconductance, to ensure the performance of the transconductance.

2.5.2 Gain of Transresistance Amplifier

At resonance the load to the currant follower, with a gain of A_i , simply is the parallel resistance R_{pc} , which ideally transforms the output current, see appendix B.3, into a voltage. Therefore the total gain A_r of the circuit is

$$A_{r} = \frac{v_{l}}{i_{g}} = A_{i} \cdot R_{pc} = [\omega = \omega_{0}] = \frac{1}{1 + \frac{r_{dc} + R_{pc}}{\frac{1}{j\omega_{0}C_{I}}(1 + r_{dc}g_{mc})}} \cdot R_{pc}$$
(2.106)

Assuming that $r_{dc}g_{mc} \gg 1$ the denominator can be written as

$$I + \frac{j\omega_0 C_I}{g_{mc}} + \frac{j\omega_0 C_I R_{pc}}{r_{dc} g_{mc}}$$
(2.107)

The biasing of the circuit determines how large $j\omega_0 C_{p'}g_{mc}$ is, which should be much smaller than one if the common gate is supposed to operate as an ideal current follower, and $R_{pc} \ll r_{dc}$ to ensure that the gain of the current follower is as close to unity as possible.

There is an upper limit of the gain as R_{pc} affects both the numerator and the denominator.

2.6 Voltage Follower

The small signal equivalent circuit of the voltage follower is a common drain amplifier, see figure 2.17. The purpose of the circuit is to shift the DC component of the signal, increase the driving capability of the next stage, as well as applying negative resistance to the resonant tank of the common gate stage to increase the Q-value. The reactance of the loading capacitance is assumed to be small enough to be able to ignore the channel conductance of the follower.

2.6.1 Input Impedance

Due to the capacitive load, C_L , the resistive part of the input impedance is going to be negative, which gives an opportunity to increase the Q-value of the resonant tank of the current follower. The input impedance is

$$Z_f = \left(\frac{1}{j\omega C_{gsf}} + \frac{1}{j\omega C_L} - \frac{g_{mf}}{\omega^2 C_{gsf} C_L}\right) \parallel \frac{1}{j\omega C_{gdf}}$$
(2.108)

The input admittance is thereby going to be dependent on the Q-value of the input impedance. As an ideal voltage follower has unity gain, the transistor needs to be large to have

2 Low Noise Amplifier



Figure 2.17: Simplified model of a voltage follower with capacitive load.

large transconductance to retrieve unity gain, see equation 2.113. If the transistor is large, the Q-value of the input impedance will be low, giving that the input admittance can be expressed as

$$Y_f \approx -\frac{\omega^2 C_{gsf} C_L}{g_{mf}} + j\omega \left(\omega^2 \frac{C_{gsf} C_L (C_{gsf} + C_L)}{g_{mf}^2} + C_{gdf} \right)$$
(2.109)

The negative conductance is controlled by the capacitive load, as transition frequency is almost constant with the change of transistor width, giving

$$g_f = -\frac{\omega^2 C_L}{\omega_{Tf}}$$
(2.110)

The capacitance of equation 2.109 is dominated by C_{gdf} , but the influence of C_L is increased with its size, as C_f can be expressed as

$$C_f = \frac{\omega^2}{\omega_{Tf}^2} C_L + \frac{\omega^2}{\omega_{Tf}} \frac{C_L^2}{g_{mf}} + C_{gdf}$$
(2.111)

2.6.2 Output Impedance

Ideally the output impedance is $1/g_{mf}$ but the inductance and the capacitances on the input of the common drain is a large impedance, Z_c , loading the input of the circuit, giving that the output impedance is

$$Z_{out} = \frac{\frac{1}{j\omega C_{gs}} + Z_c}{1 + \frac{1}{j\omega C_{gs}} g_{mf}} \approx \frac{1}{g_{mf}} + j\frac{Z_c}{\omega_{Tf}/\omega}$$
(2.112)

and therefore the output impedance is increased, which might reduce the capability of driving the next stage.

2.6.3 Gain of Voltage Follower

The gain of the voltage follower should ideally be one, but as C_L is the input capacitance of the next stage it could be rather large. A large capacitive load then requires a large transconductance to be able to drive the loading circuit, which in turn gives a large gate source capacitance making the voltage gain more ideal, as the voltage gain A_v is

$$A_{v} = \frac{v_{l}}{v_{g}} = \frac{1}{1 + \frac{j\omega C_{L}}{j\omega C_{gsf} + g_{mf}}} = \frac{1}{1 + \frac{C_{L}}{C_{gsf}} \frac{1}{1 + \omega_{Tf}/j\omega}}$$
(2.113)

2.7 Overall Amplifier Performance

2.7.1 Overall Gain

To optimize the overall gain of the entire amplifier is a fairly complicated procedure as the stages affect each other significantly. If there is no signal mismatch between the stages, the gain is

$$A_{tot} = A_{g}A_{r}A_{v} \tag{2.114}$$

The gain A_g of the transadmittance, the inverter, is dependent on the transition frequency of the inverter, the operating frequency and the desired matching resistance. The amplifier gain A_g is independent of the transconductance g_m of the inverter. But this is true only as long as the model of the input resistance holds. The inverter also requires that the loading of the current follower is small.

The output current of the current follower, with a current of gain A_i , is converted into a voltage by the parallel resistance R_{pc} of the resonant tank, giving the total transresistance gain A_r . Three parameters controls the parallel resistance. The size of the inductor, the Q-value and the negative input conductance of the voltage follower. The parallel resistance can be made very large but an extremely large parallel resistance also renders a very large input impedance of the current follower and a signal mismatch between the inverter and the current follower arises and the overall gain is reduced. The input matching of the inverter can also be altered.

The voltage follower has a gain of A_v and controls the gain A_r by affecting the resonant tank in two ways. The capacitive input determines the inductance value, for a given resonance frequency, and large transistors has a larger input capacitance, resulting in a smaller inductance and a lower gain. The negative conductance increases the value of the parallel resistance and is proportional to the capacitance loading the voltage follower, if the transistors in the follower is large enough. Small transistor gives a small gain in the follower itself.

The Q-value of the coupled inductors has a small dependency versus the inductor reactance, see example 2 in page 8, if the operating frequency is not in the vicinity of the self resonance of the inductor. This implies that small coupled inductors will have a smaller parallel resistance and a larger coupled inductors a large parallel resistance. The fact that coupled

inductors are used, instead of separate inductors, improves the Q-value and thereby the gain of A_r .

2.7.2 Simulating Gain and Linearity

The difference in performance between one symmetric amplifier and two nonsymmetric amplifiers has been simulated in a 0.35 μ m CMOS process. The corresponding stages in the amplifiers were design for equal transconductance and current consumption. The amplifiers have a resonance peak at 1.8GHz and a resistive part of the input impedance of 50 Ω .

The difference in capacitance between a PMOS and an NMOS transistor has to be compensated in the symmetric amplifier (AMP1) by using external capacitances, see example 1 in page 6. The nonsymmetric circuit is therefore simulated both with (AMP2) and without (AMP3) extra capacitances, that are naturally present in the symmetric circuit, see figure 2.18. The total capacitance will thereby be given as

$$C_{ab} = C_{abint} + C'_{ab} \tag{2.115}$$

The reason for using external capacitances in the nonsymmetric circuit is to show by how much the linearity of the symmetric circuit is improved. It is also interesting to see that the gain of all stages are the same, except for the increased gain A_r in the symmetric circuit due to the higher Q-value.

The input resistance will be affected by the source degeneration inductance L_s and the gate source and gate drain capacitances, C_{gs} and C_{gd} respectively, as the input resistance R_{in} is given as

$$R_{in} \approx \frac{\frac{L_s}{C_{gs}}g_m}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^2}$$
(2.116)

 L_s , C_{gs} , C_{gd} and g_m are equal in AMP1 and AMP2 in figure 2.18a) and b). Observe that the coupled inductance L_s of the symmetric circuit is (1+k)/2 smaller than the individual inductances in the circuit. AMP3, in figure 2.18c), has much smaller gate source and gate drain capacitance and therefore the inductance has to be much smaller to provide the same input resistance.

The gain A_g of the first stage is dependent on the transition frequency, operating frequency and generator resistance, see equation 2.90 (here repeated for convenience)

$$A_g \approx \frac{-\omega_T'}{\left(2 + \frac{C_{gd}}{C_{gs}}\right)j\omega R_g}$$
(2.117)

where $\omega_T' = g_m / (C_{gs} + C_{gd})$. As the capacitances in AMP3 are much smaller, the transition frequency, and thereby A_g , is going to be much larger than in AMP1. The gain is about 6dB better for the process used and the given bias. The gain of the current and volt-



Figure 2.18: Transconductance stage in the a) symmetric amplifier (AMP1)b) nonsymmetric amplifier with external capacitance (AMP2) and c) nonsymmetric amplifier without external capacitance (AMP3).

age followers are also better in AMP3, due to the smaller capacitances, see equations 2.106 and 2.113, improving the gain by about 2dB.

Large inductances have lower self resonance frequency, therefore the inductances in the resonant tank of the transresistance amplifiers were made as large as possible and equal in all circuits. This means that the gain A_r of the common gate stage in AMP1 should be about 6dB better, as the parallel resistance in the resonant tank with coupled inductances is about twice the size in a symmetric circuit than in a nonsymmetric circuit with a single inductance.

As seen in table 2.4 the expected overall gain of AMP1 is 28.8dB, which is higher than the overall gain of AMP2, which is 22.9dB. The difference between them is about 6dB, due to the higher A_r in AMP1. The expected overall gain of AMP3 is 30.5dB, which is about 2dB higher than the gain of AMP1, due to the higher gain in the current and voltage followers in AMP3. The larger R_{pc} in AMP1 and the higher A_g in AMP3 both improve the overall gain by 6dB, compared with the gain of the different stages in AMP2.

The simulated gain, see table 2.4, of AMP1 was 28.4dB. The main reason for the lower gain is that the parallel resistance R_{pc} in the amplifier becomes too big and the input impedance of the current follower increases resulting in a loading mismatch between the inverter and the current follower. The gain of AMP2 was simulated to be 22.9dB, as expected. There were no loading mismatch in the cascode as R_{pc} is smaller. In AMP3 the simulated gain was about 1.5dB lower than the expected 30.5dB, due to the fact that g_{mbs} has an influence in the transistors of the followers which has been ignored so far.

The substrate transconductance g_{mbs} is adding current to the output in the current follower, while it is subtracting current from the output in the voltage follower, thereby the gain is increased in the current follower and decreased in the voltage follower. In AMP1 and AMP2, where there are the same amount of capacitance in both circuits, the effects cancel each other. The current gain is much higher in AMP3, compared with the other two, and is not

Circuit	Symmetric (AMP1)	Nonsymmetric with capacitances (AMP2)	Nonsymmetric without capacitances (AMP3)
Predicted A_{tot} (dBV)	28.8	22.9	30.5
Simulated A_{tot} (dBV)	28.4	22.9	29.0
CP1 (dBm)	-21.8	-20.0	-27.0
IP3 (dBm)	-18.7	-15.9	-20.0
IP2 (dBm)	14.7	2.5	-0.3

Table 2.4: Simulated Results for a 0.35µm CMOS process.

changed very much by the substrate transconductance, g_{mbs} , but the gain of the voltage follower is still lowered due to g_{mbs} .

The overall difference in the simulated gain becomes +5.5dB between AMP1 and AMP2 and -0.6dB between AMP1 and AMP3.

The smallest compression point (CP1) is found in AMP3, which is quite natural as the gain is much higher in the first stage of this amplifier compared with the other two. CP1 of AMP1 is slightly lower than in AMP2, but it was expected as the gain in the second stage is larger in this circuit. The third order intermodulation, here given as third order intercept point (IP3), is about the same in all circuits and the intermodulation is not affected by the symmetry of the circuit. On the other hand the second order intercept point (IP2) is greatly improved with symmetry in AMP1 by +15dB compared with AMP3. As is seen from table 2.4 the main differences between AMP1 and AMP3 is CP1 and IP2.

2.7.3 Calculating the Noise Figure

The inverter model in table 2.1 is used for the noise calculations, with a compensation for the difference in gate source capacitance between the NMOS and PMOS transistor. The large NMOS transistor is simply two times the NMOS transistor in the inverter. The resulting circuit parameters are tabulated in table 2.5.

The operating frequency is 1.8GHz and the circuit is matched to 50 Ω , which is the value of the generator resistance R_g . The electric field in the channel is assumed to be small enough such that the transistors can be considered as long channel devices, giving that $\gamma=2/3$, $\delta=4/3$ and $\alpha=1$. c=j0.4.

The result in table 2.6 is presented as the minimum noise figure (NF_{min}) at the optimum transconductance (g_{mopt}) and the noise figure given by the operating transconductance in table 2.5. From table 2.6 it is seen that the gate induced noise can not be excluded from the noise figure calculation, because it will give a far to optimistic result. If C_{ed} is included in

circuit	$g_m / (\mathrm{mS})$	c_{gs} / (fF)	$c_{gd}/(\mathrm{fF})$	$\omega_T / (\text{Grad/s})$
inverter	25.2	460	60.7	58.6
NMOS	25.4	254	26.2	100

Table 2.5: Transadmittance amplifier in a 0.35µm CMOS process.

Table 2.6:	Comparing	transconductance and	l noise figure	for a 0.35	µm CMOS	process.

C_{gd}		No		Yes	
ig		No	Yes	No	Yes
inverter	g _{mopt} (mS)	N/A	51.8	11.3	46.7
	NF _{min} (dB)	N/A	1.06	0.14	0.99
	NF (dB)	0.15	1.24	0.18	1.11
large NMOS	g _{mopt} (mS)	N/A	94.5	16.5	86.8
	NF _{min} (dB)	N/A	0.61	0.06	0.58
	NF (dB)	0.05	1.02	0.07	0.90
difference	NF _{min} (dB)	N/A	0.45	0.08	0.41
	NF (dB)	0.1	0.22	0.11	0.21

the model both the optimum transconductance and the noise figure is lowered. It is not a large change but it shows that the noise figure will not suffer from the introduction of C_{gd} .

The difference in noise figure between the symmetric inverter and the nonsymmetric large NMOS transistor is at the most 0.45dB. For the transconductances used in the previous simulations, see table 2.4, the difference is about 0.2dB. The main reason for the lower noise in the large NMOS transistor is the higher transition frequency, see table 2.5.

In example 4 in page 25 there was a maximum size of the transistor, and thereby the transconductance, to be able to mach the input resistance to the wanted value. Repeating the simulation for the inverter and the large NMOS transistor shows that the optimum transconductances calculated should be feasible.

Some approximations were made in appendix C.3.2 to get equation 2.86. Therefore the output current of the inverter transadmittance was both simulated and calculated to be able to compare the difference. The input current source i_{ia} is shown in figure C.1b) and figure 2.7b). The amplitude difference was less than 1% and the phase difference was less than 3°. The approximations made should therefore hold and the noise factor given by equation 2.96 is correct.

2.8 Conclusion

There are a number of wireless applications, both long range systems for objects on the move and short range stationary systems, resulting in a great interest in transceivers that are cheap, small and have low power consumption. The digital IC's drives the power supply towards lower voltages, which also decreases the power consumption in digital circuits. The analog transceiver should therefore also be able to operate at low voltage, to be able to use the same power supply. The need for low cost gives that the chips should be few and small and drives production towards cheap processes where CMOS holds a strong position. The problem remains, however, that the performance of the transistor, concerning gain, current consumption, noise and high frequency behaviour in general, is better for a bipolar transistor than for a CMOS transistor. By implementing smaller structures for semiconducting devices the manufacturers have been able to improved the performance of the CMOS transistor in RF analog circuits. Even though the performance has become better, there is still a large potential to improve existing circuit solutions and find new circuits that can compete with bipolar circuits, and by thorough theoretical analysis find the benefits and drawbacks of each solution.

The objective was to investigate a new CMOS amplifier topology, with matched input impedance, suitable for low voltage applications. The circuit is a symmetric amplifier, which makes it more linear. The first stage of the amplifier is an inverter (as it is more suitable for low voltage applications than a differential stage) with an inductive series feedback, where the Q-value of the inductances were in creased by connecting them in a transformer structure. It was found that the first order model of the transistor, where only the transconductance and the gate source capacitance were present, did not apply and that the introduction of an adjusted model, including the gate drain capacitance as well, was necessary to get the correct input resistance. The gain of the transadmittance amplifier, with both the original and the modified transconductance model, was only dependent of the transition frequency of the inverter, the operating frequency and the generator resistance. The gain was found to be lower for the modified model as the gate drain capacitance has a significant influence on the transition frequency. The noise figure was slightly decreased for an optimum transconductance lower than would first be expected from the simplified model of the transistor. The different noise sources in a transistor were analysed, giving that the thermal current noise in the channel and the gate induced noise were the most important sources. The second stage is a symmetric current follower were the output current is converted into a voltage by a parallel resistance R_{pc} of a resonant tank. Three parameters controls the parallel resistance. The size of the inductor, the Q-value and the negative input conductance of the third stage, the voltage follower. The Q-value is increased by using coupled inductors, giving about twice as high gain. The third stage is a voltage follower that improves the driving of the following stage, which is assumed to be a capacitive input of a mixer. It is the capacitive load that gives the negative input conductance of the follower that improves the Q-value in the resonant tank.

Comparing a symmetric amplifier with a nonsymmetric amplifier, the gain is about the same size, while the compression point and second order intercept point is much higher in the symmetric circuit. The major difference in compression point is due to the fact that the gain of the first stage is lower in the symmetric amplifier, while the higher second order intercept point in is due to the symmetry of the circuit.

Chapter 3

Analysis of Conversion Gain Spread in Mixers

3.1 Background

In a radio transmitter-receiver system it is important that the transmitter does not generate unwanted signals[23] outside the wanted frequency-band that can interfere with other transmitted signals, as well as it is important for the receiver to reject unwanted signals. The selectivity of the receiver can either be controlled by a tunable filter or a superheterodyne[10] receiver, see figure 3.1. The benefit with the superhet over the tunable filter is that the demodulation can take place at a lower fixed frequency and that it is hard to make a simple tunable high-frequency filter.



Figure 3.1: Superheterodyne receiver.

The single mixer receiver converts both the desired radio frequency (RF) and the image frequency to the intermediate frequency (IF), see figure 3.2. The suppression of the image RF can be done with an RF filter in front of the RF amplifier or between the RF amplifier and the mixer, but then the IF need to be high enough for the image RF to be outside the receiver frequency band. It is also possible to exchange the single mixer with an image-reject mixer architecture[24]. This mixer architecture enables the use of a very low IF.

3 Analysis of Conversion Gain Spread in Mixers



Figure 3.2: Wanted and image frequency at the intermediate frequency.

By integrating the receiver mixer on a chip, including the LO quadrature decomposition, it is common to retrieve 30-35dB of image rejection. It is possible to find articles [29] reporting minimum image rejection lower than 50dB, waiving some of the requirements. Still, a high image rejection is feasible. The degree of image rejection relies on how well the inphase (I) and quadrature-phase (Q) branches are matched in terms of gain and phase. The major errors arise from the quadrature decomposition of the local oscillator (LO) and the IF phase-shift, but to retrieve a really high image rejection the mixer imbalance becomes equally important.

The purpose of this work is to study the imbalance between mixers due to statistical spread in the semiconductor process. The major random variations in a semiconductor process are observed from one batch to another, but even within a batch there are some small variations between the components, usually termed mismatch.

The transfer function of the mixer is time-variant and therefore it is usually simulated with a transient simulation where the output data is Fourier-transformed to get the frequency information of interest. The goal of this part of the thesis is to show that it is possible to use a time-invariant approximation, and thereby be able to evaluate the statistical spread in the frequency domain directly.

The configuration considered [10,26], as an example, is a passive CMOS mixer, see figure 3.3, as it is suitable for low-voltage applications, see chapter 1. The procedure can be repeated for active mixers such as the Gilbert-cell.

The load on the IF side of the mixer will play an important role. It will be the capacitive input load of a buffer, which will affect the transfer function. While it would be beneficial to have large transistor devices in the mixer, to minimize the influence of device mismatch, this also comes at a cost in terms of increased power consumption, as the LO buffer circuitry must drive a larger capacitive load. For that reason the size of the mixer transistors should not be larger than necessary. Obviously, for a given level of matching there exists an optimal transistor size.

The imbalance of the receiver path can be studied as a function of a large number of parameters, e.g. intermediate frequency, capacitive and/or resistive load, transistor width and/or length, non-ideal signal generators (both radio frequency and local oscillator) and LO waveform. The most interesting parameters are the transistor width and the capacitive load, simulated with a sine-wave LO signal driving the mixers, for the following reasons:



Figure 3.3: Double-balanced passive CMOS mixer.

- Increasing the transistor width reduces the loss whereas the length should be kept as small as possible to minimize loss.
- The most plausible input load of a CMOS voltage IF buffer will be capacitive and not resistive.
- The result for one IF will be scalable to another.
- The signal from the LO buffer is sine-wave-like at high frequencies rather than squarewave-like.

3.2 An Image-Reject Mixer and the Effect of I/Q-Imbalance

3.2.1 Mixing

The simplest passive commutating CMOS mixer consists of four transistor switches in a bridge configuration, see figure 3.3. The switches are driven by a local oscillator v_{lo} in antiphase, so that only one diagonal pair is conducting at any given time, making v_{if} periodically equal to v_{rf} and $-v_{rf}$ with the period of the oscillator. This way a multiplication is achieved in the time-domain.

The radio signal of interest can be either RF_1 or RF_2 in figure 3.2. If RF_1 is the wanted signal then RF_2 is the image and vice versa. In this case the radio signal is simply defined as

$$v_{rf}(t) = b\cos\omega_{rf}t \tag{3.1}$$

The LO is a sine-wave, with a phase offset φ , defined as

$$v_{lo}(t) = a\cos(\omega_{lo}t + \varphi)$$
(3.2)

The product becomes

$$a\cos(\omega_{lo}t + \varphi) \cdot b\cos\omega_{rf}t = \frac{1}{2}ab(\cos(\omega_{lo}t + \varphi + \omega_{rf}t) + \cos(\omega_{lo}t + \varphi - \omega_{rf}t))(3.3)$$

resulting in a sum frequency and a difference frequency, where the latter is the intermediate frequency of interest. Neglecting the amplitude of the radio and local oscillator signal for the moment, gives that the intermediate frequency equals

$$v_{if}(t) = \frac{1}{2}\cos(\omega_{lo}t + \varphi - \omega_{rf}t) = \frac{1}{2}\cos(\pm \omega_{if}t + \varphi)$$
(3.4)

where the intermediate frequency, ω_{if} , is defined as $|\omega_{lo} - \omega_{rf}|$. The phase offset φ will be positive if the LO frequency is higher than the radio signal, in this case RF_l , giving

$$v_{if}(t)\Big|_{RF_{I}} = \frac{1}{2}\cos(\omega_{if}t + \varphi)$$
(3.5)

 RF_2 will thereby render a negative phase, as v_{if} can be rewritten as

$$v_{if}(t)\Big|_{RF_2} = \frac{1}{2}\cos(\omega_{if}t - \varphi)$$
(3.6)

For $\varphi=0$ both signals will have the same phase but if $\varphi\neq0$ there will be a phase difference of 2φ between the signals. This means that it is possible to distinguish between the wanted and the image frequency. The principle is to use two mixers and to multiply the RF signal with an LO frequency that is split up into two signals with a $\pi/2$ phase difference. The resulting phase of the IF signal is demonstrated in figure 3.4, where the I-path, with $\varphi=0$, the phase is

$$I = \frac{1}{2}\cos\omega_{if}t \tag{3.7}$$

for RF_1 and RF_2 . The phase for RF_1 in the Q-path, with $\varphi = \pi/2$, is

$$Q = \frac{1}{2}\cos\left(\omega_{if}t + \frac{\pi}{2}\right) \tag{3.8}$$

and for RF_2 it is

$$Q = \frac{1}{2}\cos\left(\omega_{if}t - \frac{\pi}{2}\right) \tag{3.9}$$

By phase-shifting another $\pi/2$ (using an all-pass filter) in e.g. the Q-path one of the incoming frequencies are going to be in phase and the other in anti-phase. It is now possible to add the two paths together, see figure 3.5, and the wanted frequency component comes through as

$$v_{if}(t)\Big|_{wanted} = \cos\omega_{if}t \tag{3.10}$$

in the ideal case and the image as

$$v_{if}(t)\Big|_{image} = 0 \tag{3.11}$$



Figure 3.4: The resulting phases of the IF signals after mixing RF_1 and RF_2 with an LO signal with a zero phase offset (black) and a $\pi/2$ phase offset (grey).



Figure 3.5: Image reject mixer.

3.2.2 Imbalance

So far it has been assumed that the output signals of the mixers have identical amplitude and a perfect $\pi/2$ phase offset. In reality there is a difference in amplitude and a phase offset different from the desired $\pi/2$, even if the LO signals are in perfect quadrature of equal amplitude. The reason is that the transistors in the mixer are not identical, giving that the transfer function (the mixing) of two mixers will not be identical either.

From a statistical point of view the transfer function contains a mean value, E(x), and a standard deviation, D(x). The main part of the standard deviation is going to be correlated with other mixers, while a small part will remain uncorrelated, the mismatch. The correlated standard deviation arises from variations between batches while the mismatch is the difference between components in the same batch.

In figure 3.6 is one statistical outcome of the I an Q signals demonstrated as a vector diagram. The I and Q signals are drawn with separate vectors for the mean value, *m*, the correlated part of the standard deviation, σ_{corr} , and the noncorrelated mismatch, σ_{mm} . It is seen that the wanted signal, in figure 3.6c), is going to be mainly influenced by the correlated



Figure 3.6: a) One statistical outcome of the *I* and *Q* signal of RF_1 after the mixer. b) $+\pi/2$ phase shift and subtraction. c) $-\pi/2$ phase shift and addition.

spread in the process, while the amplitude of the image frequency, in figure 3.6b), will not be zero due to the mismatch between the mixers.

The overall image reject ratio (IRR) is the ratio of the wanted to the image signal given as

$$IRR = \frac{|A_{wanted}|}{|A_{image}|} \tag{3.12}$$

The spread of the desired signal magnitude is only a few percentages while the image frequency can vary several orders of magnitudes, therefore it is realised that it is the mismatch in the process that will set the limit to what level of image rejection that can be obtained.



Figure 3.7: A theoretical model of a passive switching mixer.



Figure 3.8: An ideal mixer with a low pass filter.

3.3 Conversion Gain

3.3.1 Ideal Mixer

The mixer itself is assumed to use ideal switches, see figure 3.7. This way the LO signal produces a mixing function m and the amplitude level of the LO signal itself is not important. The mixing function is a unit-amplitude square-wave signal, given by its Fourier-series as

$$m(t) = \frac{4}{\pi} \left(\cos \omega_{lo} t - \frac{1}{3} \cos 3 \omega_{lo} t + \frac{1}{5} \cos 5 \omega_{lo} t - \frac{1}{7} \cos 7 \omega_{lo} t + \dots \right)$$
(3.13)

The ideal mixer path for one single mixer can then be described as in figure 3.8. The radio signal v_{rf} is multiplied by the mixing function *m*, resulting in the signal *w*, where the higher frequencies have to be attenuated to finally obtain the IF signal v_{if} of interest.

The radio signal is defined as before as

$$v_{rf}(t) = b\cos\omega_{rf}t \tag{3.14}$$

The product of the fundamental frequency of the LO and the RF signal then becomes

$$w(t) = \frac{4}{\pi} \cos \omega_{lo} t \cdot b \cos \omega_{rf} t = \frac{1}{2} \frac{4}{\pi} b (\cos(\omega_{lo} + \omega_{rf})t + \cos(\omega_{lo} - \omega_{rf})t) \quad (3.15)$$

The convolution of the input signal w(t) and the filter impulse response h(t) gives the intermediate signal as

$$v_{if}(t) = h(t) * w(t) = h(t) * [m(t) \cdot v_{rf}(t)] \approx \frac{4b}{\pi^2} \cos \omega_{if} t$$
 (3.16)

By using a square-wave LO signal, the transistors will behave as close as possible to ideal switches. The output signal will also be $4/\pi$ times larger, due to the fundamental of the mixing function, than if the mixing function only was a sine-wave. But this is only an ideal mathematical model, which do not consider that, beside the mixing function *m*, the mixer is a circuit with a transfer function, containing components with nonlinear characteristics, losses and loading effects.

3.3.2 Passive CMOS Mixer

In a real mixer the transistors will not operate as perfect switches, and the LO signal may very well be close to a sine-wave, rather than a square-wave. The switch will have a conductance g_i dependent on v_{lo} , making the amplitude level important. The mixer circuit may therefore be modelled as in figure 3.9a), where it to begin with is assumed that all conductances are of equal size. The Thevenin equivalent circuit, in figure 3.9b), looks like an ordinary low-pass RC-network, with the difference that the resistance is expressed as a timevariant conductance instead of being fixed. The mixer should therefore be looked upon as a time-variant linear system, rather than an ideal multiplication of two signals. This analysis has been performed by Shaeffer and Lee [26], and in this thesis the analysis is extended to include the effect of spread in the transistor conductance.

The conductance of one switch, g(t), is of course dependent on the LO-signal, as shown in figure 3.10, and the Thevenin equivalent voltage can then be calculated as

$$v_T(t) = \frac{g(t) - g(t - \frac{T}{2})}{g(t) + g(t - \frac{T}{2})} v_{rf}(t) = m(t) v_{rf}(t)$$
(3.17)

where m(t) is the mixing function. The Thevenin conductance is calculated as

$$g_T(t) = \frac{g(t) + g(t - \frac{T}{2})}{2}$$
 (3.18)

The state equation can be found by using Kirchhoffs voltage law, giving

$$v_T(t) = \frac{1}{g_T(t)}i(t) + v_{if}(t) = \frac{C_L}{g_T(t)}\frac{dv_{if}(t)}{dt} + v_{if}(t)$$
(3.19)

which gives

$$\frac{dv_{if}(t)}{dt} = -\frac{g_T(t)}{C_L}v_{if}(t) + \frac{g_T(t)}{C_L}v_T(t)$$
(3.20)

The differential equation is then solved as

$$v_{if}(t) = v_{if}(t_0)e^{t_0} + \int_{t_0}^{t} \frac{g_T(s)}{C_L}ds + \int_{t_0}^{t} \frac{g_T(\tau)}{C_L}e^{-\int_{\tau}^{t} \frac{g_T(s)}{C_L}ds} v_T(\tau)d\tau$$
(3.21)

with t_0 as the initial time and $v_{if}(t_0)$ as the initial state. The corresponding impulse response becomes, as the system is causal,

$$h(t, \tau) = \frac{g_T(\tau)}{C_L} e^{-\int_{\tau}^{t} \frac{g_T(s)}{C_L} ds} \Theta(t-\tau)$$
(3.22)

where $\theta(t)$ is the unit step function.



Figure 3.9: The passive switching mixer modelled by a) time-varying conductances and b) the thevenin equivalent.



Figure 3.10: Transistor conductance g, mixing function m and Thevenin conductance g_T .

A second look on figure 3.10 shows that the conductance $g_T(t)$ can be expressed as a sum of frequencies with the fundamental period T/2, as in equation 3.23, where T is the period of the LO-signal.

$$g_T(t) = \frac{\hat{g}}{2} \left(a_0 + \sum_n a_n \cos 2n \omega_{lo} t \right)$$
(3.23)

The average value a_0 equals 1 for the square-wave and $2/\pi$ for the sine-wave. If the maximum and the average conductances are defined as $\hat{g}_T = \hat{g}/2$ and $\overline{g}_T = \hat{g}_T a_0$, respectively, and assuming that the transient response has decayed ($t_0 = -\infty$), then the superposition integral¹ in equation 3.21 becomes

$$v_{if}(t) = \int_{-\infty}^{t} \frac{\overline{g_T}}{C_L} e^{-\frac{g_T}{C_L}(t-\tau) - \frac{g_T}{a_0 C_L 2 \omega_{lo}} \sum_n \frac{a_n}{n} (\sin 2n\omega_{lo}t - \sin 2n\omega_{lo}\tau)} \hat{g_T} \frac{g_T(\tau)}{\overline{g_T}} m(\tau) v_{rf}(\tau) d\tau$$
(3.24)

The result is time-variant as the impulse response is not independent of τ , i.e.

$$h(t, \tau) \neq h(t - \tau, 0) \tag{3.25}$$

The new mixer path can then be looked upon as in figure 3.11, where it is the mixer itself and the loading capacitor that causes the filtering.

From equation 3.24 it is seen that the effective gain of the function can be expressed as

$$A = \hat{g_T} / \bar{g_T} = 1/a_0$$
 (3.26)

and the modified mixing function, for the square-wave and sine-wave LO signal, respectively, as

$$m'(t) = \frac{g_T(t)}{\hat{g}_T}m(t) = \begin{cases} \frac{4}{\pi} \left(\cos\omega_{lo}t - \frac{1}{3}\cos 3\omega_{lo}t + \dots\right) \\ \cos\omega_{lo}t \end{cases}$$
(3.27)

The input signal to the time-variant filter can then be defined as

$$w(t) = Am'(t)v_{rf}(t)$$
 (3.28)

and the new impulse response of the filter as

$$h(t, \tau) = \frac{\overline{g_T}}{C_L} e^{-\frac{\overline{g_T}}{C_L}(t-\tau)} \cdot e^{-\frac{\overline{g_T}}{a_0 C_L 2 \omega_{lo}} \sum_n \frac{a_n}{n} (\sin 2n \omega_{lo} t - \sin 2n \omega_{lo} \tau)} \cdot \theta(t-\tau)$$
(3.29)

¹In the time-invariant case it reduces to the convolution integral [28].



Figure 3.11: A time-variant low pass mixing filter.

giving that

$$v_{if}(t) = h(t) * w(t) = h(t) * [A \cdot m'(t) \cdot v_{rf}(t)]$$
(3.30)

The impulse response has one time-invariant and one time-variant part. If the time-variant part of the filter remains close to unity, then the filter reduces to a first order low pass filter with the time-constant $C_L / \overline{g_T}$ and a low frequency unity gain. Observe that the amplitude of the LO-signal affects the time constant of the filter.

The modified mixing function, m', is a unit amplitude signal, just as the mixing function m in section 3.3.1, where the amplitude of the fundamental signal is $A_{m'}$. For the square-wave $A_{m'}$ equals $4/\pi$, which is the same as in the ideal case in equation 3.16, but the effective gain A is going to vary with the type of LO-signal used as well. The total conversion gain, excluding the filter, will be

$$A_{tot} = \frac{A_{m'} \cdot A}{2} \tag{3.31}$$

For a sine-wave the total gain will be $\pi/4$ and for a square-wave $2/\pi$, which means that the gain for a sine-wave is $\pi^2/8$ larger. This is the opposite result compared with section 3.3.1 and shows that the conversion gain of the mixer is more dependent on the actual circuitry than just the mixing function.

3.3.3 Numerical Calculation of the Time-Variant Filter

As the impulse response is time-variant, it is not easy (if possible) to find an analytical and explicit expression for the transfer function. If the output signal is periodic, though, it is possible to apply a Fast Fourier Transform (FFT) to find a numerical representation of the transfer function for the filter.

The effect of time-variance in the LP-filter can be simulated by applying an input signal w(t), which simply could be the IF signal only or the result of the mixing in equation 3.28. With a time-discrete approximation of the filter, and if the time steps are small enough, $v_{if sample}$ will correspond well with v_{if} , see equation 3.30, as

$$v_{if_sample}(t) = \sum_{k} h_{\Delta_k}(t, \tau_k) w(\tau_k) \Delta_k \tau \to v_{if}(t) = \int_{-\infty}^{\infty} h(t, \tau) w(\tau) d\tau \qquad \Delta_k \tau \to 0 \quad (3.32)$$

In this case *v*_{*if_sample*} can be expressed as

$$v_{if_sample}(t_i) = \underline{H}(t_i, \tau_j) \cdot w(\tau_j) \Delta \tau$$
(3.33)

where

$$\underline{H} \cdot w = \begin{bmatrix}
h(t_0, \tau_0) & 0 & 0 & \dots & 0 \\
h(t_1, \tau_0) & h(t_1, \tau_1) & 0 & \dots & 0 \\
h(t_2, \tau_0) & h(t_2, \tau_1) & h(t_2, \tau_2) & \dots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
h(t_N, \tau_0) & h(t_N, \tau_1) & h(t_N, \tau_2) & \dots & h(t_N, \tau_N)
\end{bmatrix} \begin{bmatrix}
w(\tau_0) \\
w(\tau_1) \\
w(\tau_2) \\
\vdots \\
w(\tau_N)
\end{bmatrix}$$
(3.34)

If the system is time-invariant then

$$h(t_i, \tau_j) = h(t_{i+1}, \tau_{j+1}) \qquad \forall i \text{ and } j$$
(3.35)

Example 5 Impulse Response and Output Signal

The purpose of the simulation is to show the impulse response of the filter and the size of the timevariant part in the response as well as the final output signal for two different time-constants. The time-variant part of the filter is given as

$$h_{tv}(t,\tau) = e^{-\frac{\overline{g_T}}{a_0 C_L 2 \omega_{lo}} \sum_n \frac{a_n}{n} (\sin 2n \omega_{lo} t - \sin 2n \omega_{lo} \tau)}$$

The simulation is made for:

 $g_d=246\mu S$ $C_L=25fF$ and 250fF $w(t)=sin(2\pi 100e6^*t)$ LO=2GHz

Figures 3.12 and 3.13 shows the simulated impulse response in matrix $H(t, \tau)$ (equation 3.34), where the time-constant is 10 times shorter in figure 3.12 than in figure 3.13. It seen that even if there is a time-variance in the impulse response is still dominated by the behaviour of the time-invariant part and that the time-variant influence is reduced with a large timeconstant. The fact that the time-variant part is inversely proportional to the LO frequency, which the time-constant is as well, gives that the higher the frequency the smaller the influence.

Figure 3.14 shows the output signal of equation 3.33 and its Fourier-transform for a single input frequency of 100MHz for both a small and a large time constant. The time-variance of the filter gives additional frequencies of $2n\omega_{lo}$, where only the first frequency at 4GHz is shown.

As demonstrated in example 5 it is possible, as a first order approximation, to describe the filter as an ordinary first order low pass filter with the transfer function

$$H(\omega) = \frac{1}{1 + j\omega(C_L/\overline{g_T})}$$
(3.36)



Figure 3.12: C_L is small a) $H(t, \tau)$. b) The time-variant part of $H(t, \tau)$ is varying around unity.



Figure 3.13: C_L is large a) $H(t, \tau)$. b) The time-variant part of $H(t, \tau)$ is very close to unity.



Figure 3.14: a) y(t) with an IF of 100MHz for both time-constants. b) FFT of y(t) in e.

3.3.4 Conversion Gain and the Dependency on the Conductance

The gain A, in equation 3.26, is only dependent on the average value a_0 in equation 3.23 giving that the gain is independent on the conductance. m' in equation 3.27, is the modified mixing function and it is independent of the conductance if the mixing function m is independent of the conductance. m can be recalculated as

$$m(t) = \frac{v_T(t)}{v_{rf}(t)} = \frac{g_I(t)}{g_I(t) + g_2(t - \frac{T}{2})} - \frac{g_3(t - \frac{T}{2})}{g_4(t) + g_3(t - \frac{T}{2})} = \begin{cases} 1 & 0 < t < \frac{T}{2} \\ -1 & \frac{T}{2} < t < T \end{cases}$$
(3.37)

which shows that it is independent of the conductance, if the conductance in the off-state is much smaller then the conductance in the on-state.

It is the statistical spread in the transfer function of the Thevenin equivalent of the mixer, see figure 3.9b), that produces the I/Q-imbalance in an image-reject mixer, as the dependency on the conductance is only present in equation 3.36.



Figure 3.15: The biasing of one mixer transistor.

3.4 Modelling and Statistical Properties of Mixer Image Rejection

3.4.1 Channel Conductance

In figure 3.9 the mixer was modelled as four conductances, g_i , dependent on the LO voltage, which could be simplified to a Thevenin equivalent conductance, g_T . The conductance in this case is the channel conductance, g_d , of the transistor. As the biasing of the MOS transistor, see figure 3.15, in the mixer has a V_{DS} that is virtually zero, a simple DC-model for the channel conductance is given by [12]

$$g_{d0} = \frac{W_{eff}}{L_{eff}} \mu_{eff} C'_{ox} (V_{GS} - V_{TH})$$
(3.38)

If the drain source resistance factor, R_{ds} , is included the channel conductance becomes

$$g_d = \frac{g_{d0}}{I + R_{ds}g_{d0}}$$
(3.39)

In the process used, mismatch was modelled as being dependent on the threshold voltage for a zero biased substrate, the oxide thickness and variations in the transistor width and length. Each of the mismatches are uncorrelated with all the others and they are all Gaussian. By studying the BSIMv3.3 model, one realizes that even if the individual mismatch effects are Gaussian and uncorrelated, the final result of the parameters in equations 3.38 and 3.39, giving g_d , does not have to be Gaussian and certainly not uncorrelated. The description of the parameters and their effect on g_d is found in appendix E and a simulated result of the conductance is found in section 3.5.2, showing that g_d agrees well with Gaussian distribution.

3.4.2 Mixer Conductance

The final mixer conductance is defined by the Thevenin equivalent conductance, g_T , in equation 3.18, but this equation assumes that all conductances, g_i , are equal. Therefore g_T has to be recalculated to include the statistical spread. If the standard deviation for a stochastic variable X is small and the mean value is sufficiently displaced from zero then it is possible to calculate a Gaussian approximation [27] of f(X), see appendix D.

Observe that there are two different averages. The time average over several periods, given as $\overline{g}_T = a_0 \hat{g}/2$, and a conductance average, $E(g_T(t))$ for every *t*, due to mismatch. The shape of the wave in equation 3.23 will not change with statistical variations only the peak value. The mean value and the standard deviation of the statistical spread in \overline{g}_T can then be calculated from \overline{g} .

Assuming that every g_i in figure 3.9a) has its own Gaussian statistical variation with a mean value of m_i and a standard deviation of σ_i , then g_T in equation 3.18 can be rewritten as

$$g_{T}(t) = \frac{\left(g_{1}(t) + g_{2}(t - \frac{T}{2})\right) \cdot \left(g_{4}(t) + g_{3}(t - \frac{T}{2})\right)}{g_{1}(t) + g_{2}(t - \frac{T}{2}) + g_{4}(t) + g_{3}(t - \frac{T}{2})} = \begin{cases} \frac{g_{1} \cdot g_{4}}{g_{1} + g_{4}} & 0 < t < \frac{T}{2} \\ \frac{g_{2} \cdot g_{3}}{g_{2} + g_{3}} & \frac{T}{2} < t < T \end{cases}$$
(3.40)

The mean value of g_T for every *t* will then be (here calculated for g_1 and g_4 in the time interval from zero to T/2 but equally valid for g_2 and g_3)

$$E(g_T) = \frac{m_1 \cdot m_4}{m_1 + m_4} = [m_i = m] = \frac{m}{2} \qquad 0 < t < \frac{T}{2}$$
(3.41)

which is the same result as in equation 3.18. The time average of the Thevenin conductance can thereby be calculated from the average transistor conductance as before.

3 Analysis of Conversion Gain Spread in Mixers

The variance becomes

$$V(g_T) = \sigma_I^2 \left(\frac{m_4}{m_1 + m_4} - \frac{m_1 \cdot m_4}{(m_1 + m_4)^2} \right)^2 + \sigma_4^2 \left(\frac{m_1}{m_1 + m_4} - \frac{m_1 \cdot m_4}{(m_1 + m_4)^2} \right)^2$$
(3.42)
= $[m_i = m, \sigma_i = \sigma] = 2\sigma^2 \left(\frac{m}{2m} - \frac{m^2}{4m^2} \right)^2 = \frac{\sigma^2}{8}$

which is independent of the conductance value. The standard deviation for the mixer conductance is then

$$D(g_T) = \frac{\sigma}{\sqrt{8}}$$
(3.43)

which also is the standard deviation for $\overline{g_T}$, in equations 3.23 and 3.36.

It is seen from equation 3.41 and 3.43 that the relative standard deviation of the mixer conductance is reduced by $l/\sqrt{2}$ compared to the standard deviation of the transistor conductance.

3.4.3 Image Rejection

The image rejection was only found to be dependent on the filtering part of the mixer, see section 3.3.4 and equation 3.36. In an image reject receiver there are two mixers, one in the I-path, $H_i(\omega)$, and one in the Q-path, $H_q(\omega)$. Assuming that the output signal of the Q-mixer is phase-shifted by $\pi/2$, the image rejection of the system at the summation point should be calculated as

$$IRR = 20 \log \frac{|H_i(\omega) + H_q(\omega)|}{|H_i(\omega) - H_q(\omega)|}$$
(3.44)

Unfortunately the average value of $H_i(\omega) - H_q(\omega)$ is equal to zero and therefore it is impossible to use a Gaussian approximation to calculate the image rejection. It has to be simulated which is done in section 3.5.3.

To guarantee the needed level of image rejection, it is interesting to find the worst case, which is

$$IRR_{wc} = min(IRR) \tag{3.45}$$

Two simulators are most likely going to use different spreading sequence generators, and as the results should be comparable, it is preferred to simulate the image rejection without being dependent on a specific random sequence. The level of image rejection is therefore defined as ± 3 standard deviations of spread instead of finding a specific minimum value, as this expression will be close to the minimum value.


Figure 3.16: Simulation setup of a) the receiver path and b) the mixer.

3.5 Simulation

3.5.1 Simulation Setup

To verify if the simple time-invariant mixer model is valid, it will be compared with a more complex time-variant model in a circuit simulator. Basically this means that we are going to compare AC simulations with transient simulations of the mixer regarding the image rejection and gain.

The circuit simulator used is Cadence Spectre, with Monte Carlo analysis. Statistical parameters for the CMOS transistors are provided by the vendor. For the transient analysis the DFT function is used to get the magnitude of the IF signal in equations 3.46 and 3.48. The AC simulation made in Cadence uses the IF as the input signal instead of the RF, as it is the filtering function from w to v_{if} that is examined. The mixer should have the average conductance $\overline{g_T}$, and therefore the LO is set to the proper DC level giving that conductance. The arithmetic computations are made in Matlab and are simply based on the equations for the mixer filter and channel conductance, with the IF as the input signal. The results from circuit simulations and calculations will finally be compared and plotted in Matlab.

The difference between the mixer signals, in the transient simulation, are very small and are therefore simulated under similar conditions (no phase offset between the mixers) to minimize the numerical errors, making mismatch the only difference between them. Hence the signals can be added and subtracted directly without phase-shifting.

The simulated receiver path is illustrated in figure 3.16a). It shows a common RF input and two mixers with a common LO input signal. The capacitive loading of the mixer is modelled by a lumped capacitor. The statistical spread is only applied to the transistors in the mixers in figure 3.16b).

3 Analysis of Conversion Gain Spread in Mixers



Figure 3.17: a) Three LO waveforms. b) The absolute amplitude of the LO waveforms having the same time average value.

The most likely shape of the LO signal at high frequency is a sine-wave (due to filtering effects) but it is interesting to make additional simulations with two-tone² and square-wave signals to see the impact of a more ideal LO signal. During the simulations the average of the absolute amplitude was kept constant for all LO signal shapes as illustrated by figure 3.17, to be able to compare the image rejection and gain.

The simulations need to be done for a rather high intermediate frequency to reduce the transient simulation time, but the scalability of the results will be verified by reducing the IF frequency 10 times.

First, though, it will be necessary to verify the spread in the conductance model. Tables for the simulated results are found in appendix F.

3.5.2 Channel Conductance

It is difficult to calculate the spread in the channel conductance, due to the fact that even if the mismatches are Gaussian and uncorrelated, the final result of the parameters giving g_d does not have to be Gaussian and certainly not uncorrelated, see section 3.4.1. To find the statistical variations of the conductance in equation 3.39, it is best to simulate the channel conductance and from the result judge if the conductance has a Gaussian variation or not, and what the average value and standard deviation is. This has been done both with mathematical analysis in Matlab and circuit simulations in Cadence to verify the effect of the mismatch in equation 3.39, due to the mismatch parameters in the transistor model. See appendix E for the equations used in Matlab.

Example 6 Simulated Conductance.

The purpose of the simulation is to see if the transistor conductance g_d has a Gaussian distribution, giving that it will be possible to use Gaussian approximation to calculate the statistical average value of $\overline{g_T}$ and its standard deviation.

²The first two frequencies in the Fourier-series of the square-wave.

 V_{GS} was set to correspond to average conductance value giving

$$V_{GS} = a_0 \cdot \hat{v_{gs}} + V_{TH}$$

Matlab calculation:

The simulation was done with 1000 tests, for five different transistor widths, with <u>one</u> statistical spread for each Gaussian mismatch. Both g_d and g_{d0} are simulated.

W=1, 2, 5, 10 and 20 μ m *L*=0.35 μ m *a*₀=0.6366 \hat{v}_{gs} =1.2V *V*_{TH}=0.68

Cadence simulation:

I

The simulation was done with 100 tests of the DC operating point, for five different transistor widths, where only the mismatch parameters were modelled.

7=1, 2, 5, 10 and 20µm	<i>L</i> =0.35µm	<i>a</i> ₀ =0.6366	$\hat{v}_{gs} = 1.2 V$	$V_{TH} = 0.77$
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The simulated result for g_d in Matlab corresponds well with Gaussian distribution. In figure 3.18 the result for a transistor width of 5µm is plotted. Both the histogram and the normal probability plot fits well with the Gaussian distribution indicated as a dash-dotted line in the normal probability plot. It is thereby possible to use Gaussian approximation to calculate the average and the standard deviation of the conductance $\overline{g_T}$. In table F.1 all the mean values and standard deviations are tabulated, as well as the relative standard deviation. It is seen that the relative standard deviation stays within 7.1% and 5.6% for g_{d0} and g_d , respectively, with a very small dependency on the transistor width. The ratio between g_{d0} and g_d is constant, as the factor $R_{ds}g_{d0}$ is independent of the width of the transistor.

The simulated result for g_d in Cadence also corresponds well with the Gaussian distribution, see figure 3.19. It is not so easily seen in the histogram, but the normal probability plot follows the Gaussian line very well and we can use it to calculate $\overline{g_T}$. In table F.2 all the



Figure 3.18: a) Histogram and b) normal probability plot for Matlab calculations.

3 Analysis of Conversion Gain Spread in Mixers



Figure 3.19: a) Histogram and b) normal probability plot for Cadence DC simulations.

mean values and standard deviations of g_d are listed. The relative standard deviation stay within 2.9%, independent of the transistor width. This basically means that the conductance model can be modelled as a statistic variable with Gaussian distribution and that the dependency on width is small enough to be ignored.

The difference in conductance and standard deviation between calculated and simulated value is due to difference in the mean value of V_{TH} . It is difficult to calculate the threshold voltage, as it is dependent on a lot of variables, which are not necessarily defined in the model but calculated from other parameters. And it is not always clear which parameter or how the variable should be calculated. The electron mobility will also differ as it is dependent on the threshold voltage.

3.5.3 Image Rejection

It is possible to simulate both the correlated and noncorrelated spread in Cadence, while it is only the noncorrelated part that has been evaluated mathematically and considered in Matlab. Looking back at figure 3.6 and equation 3.44 it is realized that it is the mismatch that is important. The correlated spread is much larger than the mismatch, which is demonstrated by the fact that the ratio between mean value and standard deviation does not change noticeably after the signals are added, even with the mismatch present. But the correlated part affects only the numerator in equation 3.44. In a worst case scenario with $\pm 3\sigma$ the image rejection could be reduced by 0.35dB and 2dB, for a small and a large time-constant, respectively. Considering that the image rejection will range from 30dB and higher, the contribution from the correlated part is considered to be insignificant.

The image reject ratio, *IRR*, is defined as the ratio of the magnitude of the wanted signal to the magnitude of the image signal, see equation 3.12. In the circuit simulations the magnitude of the wanted signal is calculated as

$$V_{sum}(\omega) = |V_{IFi}(\omega) + V_{IFq}(\omega)| \qquad (3.46)$$

and in Matlab

$$H_{sum}(\omega) = |H_i(\omega) + H_q(\omega)|$$
(3.47)

The image is calculated as

$$V_{diff}(\omega) = |V_{IFi}(\omega) - V_{IFq}(\omega)|$$
(3.48)

and

$$H_{diff}(\omega) = |H_i(\omega) - H_a(\omega)|$$
(3.49)

 $H(\omega)$ is the transfer function of the mixers with the index *i* and *q* for the two paths. $V_{IF}(\omega)$ is the output voltage amplitude of the mixers in both transient and AC simulation, at the IF frequency.

The mean value, E(X), and the standard deviation, D(X), will be considered for both the numerator and the denominator, even though the standard deviation is more important in the denominator. The worst case image rejection will be calculated as

$$IRR_{wc} \approx 20\log \frac{E(H_{sum}) - 3 \cdot D(H_{sum})}{E(H_{diff}) + 3 \cdot D(H_{diff})} = 20\log \frac{E(V_{sum}) - 3 \cdot D(V_{sum})}{E(V_{diff}) + 3 \cdot D(V_{diff})}$$
(3.50)

Example 7 Setup for Image Rejection Simulation and Calculation.

Three simulations were made to show that the small-signal time-invariant approximation of the mixer model is valid for *IRR* calculations. By varying the transistor width/conductance and the capacitive load, it will be seen that the *IRR* is only dependant of the transfer function in the Thevenin equivalent model in figure 3.9b), i.e. the time-variant filter. The Cadence transient simulation shows the full effect of both time-invariant and time-variant behaviour. In the Cadence AC simulation and in the Matlab calculation the model is reduced to contain only the time-invariant filter.

Cadence transient simulation:

In the circuit simulator the biasing, see figure 3.15, and LO sine-wave swing were set to fit within a 3V supply. Five different widths and capacitive loads were used. Transient simulations and DFTs were performed and the image rejection was calculated from V_{sum} and V_{diff} as in equation 3.50.

<i>V</i> =1V	V _{TH} =0.77V	$\hat{v}_{gs} = 1.2 \text{V}$	RF=2.1GHz	LO=2GHz	IF=100MHz
W=1, 2, 5	5, 10 and 20µm	<i>C_L</i> =25, 50, 12	5, 250 and 500fF	tests=50	

Cadence AC simulation:

The mixer were set to have the average conductance by using the average LO swing level as DC input signal to the mixer gate of the conducting transistors.

<i>V</i> =1V	$V_{TH}=0.77 \mathrm{V}$	V _{GS} =0.6366*1.2V	LO=0Hz	<i>RF=IF</i> =100MHz
<i>W</i> =1, 2, 5	, 10 and 20µm	<i>C_L</i> =25, 50, 125, 250 a	and 500fF	tests=100

Matlab calculation:

C_I=25, 50, 125, 250 and 500fF

The mathematical computations of the image rejection were made for two different test vector using equation 3.36 and 3.50. Five different average conductances with spread, as simulated in Cadence, and capacitive loads were used.

 \overline{g}_d =0.284, 0.562, 1.39, 2.78, 5.55mS $\sigma_{gd} = 2.9\%$ IF=100MHz tests=1000

The results from example 7 are plotted in figure 3.20, which shows that for small widths, small g_d 's, and large capacitances the image rejection is small, while for large widths and small capacitances the image rejections is high. Hence it is the time constant of the filter that determines the image rejection for a given distribution in the transistor. The results are also tabulated in table F.3 to F.5.

To show the differences between the simulations more clearly, the result is plotted versus C_I/W in figure 3.21. As the conductance is proportional to the width of the transistor, the result is plotted versus an approximation of the time-constant in the circuit.

There are two things that gives the major contribution to the discrepancy between the mathematical model and the actual transient circuit simulation and these are the time-variant part and the internal capacitance, Cint, in the MOS-model, which is not included in the ideal model. The internal capacitance is in parallel with the capacitive load and the influence is seen as a reduction of the IRR between the Matlab and Cadence AC simulation, at small ratios of C_I/W . The real time-constant is larger at these ratios in the AC simulation. The timevariance is large for short time-constants, as shown in figure 3.12b). It is also seen in figure 3.21, that small ratios of C_L/W reduces the image rejection further, giving that the time-variance has a negative influence on the image rejection. The time-invariant filter model corresponds best to the actual circuit model for the larger time-constants, which is not surprising as the effect of time-variance is small for the ratios where both the conductances and the internal capacitances are small.

The reason for the high image rejection at small time constants can be found in the filter functions itself. Equation 3.36 shows that the spread in each mixer is reduced, as the transfer function gets closer to unity. The choice of IF will also have an effect on the IRR. The smaller the IF the larger the IRR. It is therefore interesting to plot the IRRs versus an normalized IF frequency, ω'_{if} , which is defined as

$$\omega'_{if} = \omega_{if} \frac{C_L + C_{int}}{\overline{g_T}}$$
(3.51)

The Matlab and Cadence AC simulations in figure 3.22 corresponds very well with each other, as the internal capacitance is now included in the normalized frequency value and the width is exchanged for the average transfer conductance, $\overline{g_T}$. It is thereby possible to control the image rejection by varying the IF, the capacitive load and the conductance. The transition from the time-invariant model to the time-variant model, though, is not affected by the IF. Here it is the LO frequency and the time-constant in the time-variant part of the



Figure 3.20: Image rejection of a passive mixer receiver simulated in a) a Cadence transient simulation, b) Cadence AC simulation and in c) a Matlab calculations.

3 Analysis of Conversion Gain Spread in Mixers



Figure 3.21: Image Rejection Ratio as function of C_L/W .



Figure 3.22: Image Rejection Ration versus normalized IF frequency.

impulse response in equation 3.29 that affects the *IRR*. An increase of the LO, and thereby of the RF, will increase the image rejection for a given IF and time-constant.



Figure 3.23: The intermediate frequency is changed from 100MHz to 10MHz and the loading reactance is kept constant for the two frequencies.

3.5.4 Additional simulations

3.5.4.1 Changing the IF

If the model of the mixer is correct, i.e. that it contains a multiplier, an amplifier and a filter, then it should be possible to change the intermediate frequency and retrieve the same image rejection for the same normalized IF frequency, see equation 3.51. The point where the time-variant effects will occur will change due to the fact that the filtering of the LO signal will change.

Example 8 Varying the Intermediate Frequency.

The purpose of this simulation is to show that the *IRR* will not change with the change of the IF frequency in an AC simulation, if the normalized frequency is kept constant. The normalized frequency is kept constant by reducing the IF frequency and increasing the capacitive load with the same factor. The transient simulation should differ as the increased capacitance will attenuate the LO frequency more, giving an increase in the *IRR* as the time-variant effects are reduced, see equation 3.29.

The simulations have been repeated for three widths keeping the reactance constant, for each width respectively, as the IF frequency was changed from 100MHz to 10MHz. The internal capacitances are slightly large for the widths of 5 and 20 μ m, forcing the loading capacitance to change with more than 10 times to keep the total reactance constant. The original loading capacitance is 50fF. Both AC and transient simulations were performed in Cadence with a sine-wave LO signal.

W=1, 5 and 20µm $C_L=500$ fF, 626f and 1pF IF=10 MHz

In figure 3.23 the simulated results in example 8 are compared with previous results in example 7. It is seen in the figure that a 10 times lower IF and a 10 times large capacitance does not change the image rejection of the normalized frequency in the AC simulation. In the transient simulation the high capacitive load gives that the time-constant of the filter is large and thereby is the time-variant part of the LO signal attenuated more efficiently, giving a higher image rejection.

3.5.4.2 Varying the LO signal

As seen in figure 3.10 and equation 3.29 there will not be a time-variant part in the impulse response if the LO signal is a square-wave and should thereby agree very well with AC simulations.

Example 9 Local Oscillator Waveform.

The effect of different LO signals on the image rejection and gain was simulated. The different LO waveforms are shown in figure 3.17. The peak value of the conductance will vary as it is the average value of the LO signal, i.e. the time average of the conductance $\overline{g_T}$ is kept constant.

W=1 and $20\mu m$ IF=100MHz $C_L=50 fF$

The IRR and gain data is taken from the simulations made in example 7 and 9.

Figure 3.24a) shows that the image rejection for a square-wave signal agrees very well with an AC simulation. But even a slightly more square-wave signal, like the two-tone wave used, improves the image rejection significantly at low time-constants. For large time-constants the *IRR* is almost identical for the sine-, square- and two-tone-wave.

In section 3.3.2 the predicted gain of one mixer was $\pi/4=0.785$ and $2/\pi=0.636$, for the sinewave and square-wave LO, respectively. The difference in gain between the sine-wave and square-wave was found to be $\pi^2/8=1.23$. The maximum difference simulated between sinewave and square-wave is

0,724/0,619 = 1,170

The gain, see figure 3.24b), never reaches the maximum value, when driven by a sine-wave LO. This is due to the fact that the IF frequency chosen is quite high and therefore the time-variant part in the filter will reduce the gain for small time-constants, while the large time-constants will quite naturally reduce the gain as the frequency is higher than the cutoff frequency.

Once again it is possible to see that the time-variance of the filter is removed if the LO signal is a square-wave, as the gain becomes the expected 0.636 for small time-constants.



Figure 3.24: Varying the LO signal. a) The *IRR* compared with an AC simulation. b) Transient simulation of the gain in the mixer.

3.6 Conclusion

The image rejection ratio of an I/Q-receiver will always be reduced due to the mismatch between the two paths of the receiver given by the statistical spread in the semiconductor process. The purpose of this work was to study the imbalance between mixers, focusing on the spread in the conversion gain. The mixer used has been a traditional passive voltage driven CMOS mixer with a capacitive load, which is the assumed input impedance of an IF buffer.

The transfer function of the mixer is time-variant and therefore it is usually simulated with a transient simulation where the output data is Fourier-transformed to get the frequency information of interest. The amount of data is large due to short time steps over a long time period and adding statistical variation increases the amount of data to the limit where the computer/program might not be able to handle it.

It has been shown that the mixer (from its Thevenin equivalent) contains of a multiplying part, an amplifying part and a time-variant filter. The statistical variations in the mixer mainly affects the transistor conductance and the transfer function of the time-variant filter. It is thereby the filter that sets the limit to what image rejection ratio that can be achieved.

It is possible to use a time-invariant first order approximation of the filter to study the mismatch. The benefit of this model is that it is possible to make AC simulations of the mixer and thereby be able to evaluate the statistical spread in the frequency domain directly, instead of using time-consuming transient simulations. The AC simulation gives the maximum value of the possible minimum image rejection ratio, while the time-variance increases the spread, which reduces the image rejection. The filter becomes time-invariant if the time-constant is large enough compared with the local oscillator frequency.

The level and shape of the LO signal determines the time average channel conductance of the transistor in its on-state. It has been shown that the statistical spread of the channel conductance is Gaussian, making it possible to use Gaussian approximation to calculate the mean value and standard deviation of the conductance in the Thevenin equivalent, giving that the spread of the mixer transfer function is Gaussian.

The channel conductance is constant, if the LO signal is a perfect square-wave, giving that AC simulations of the filter will equal transient simulations, due to the fact that the time-variance in the filter is not present for a square-wave LO signal.

The overall conversion gain of the mixer is affected both by the modified mixing function and the effective gain. A sine-wave mixing function provides a higher overall gain, than a square-wave signal, as the product of the amplitude of the modified mixing function and the effective gain is larger.

Finally it is found that the image rejection is dependant on the transistor width (conductance), capacitive load, IF and LO frequency. The time-constant should be small for a high image rejection ratio, giving that the mixer transistors should be as large as possible while the input capacitance of the IF buffers should be as small as possible.

Appendix A

Input Impedance of the Common Source Amplifier

A.1 Blackman's Formula



Figure A.1: Model of a linear network

A convenient way to find the input impedance is to use Blackman's formula [8] and to simplify the entire expression retrieved. The impedance between two arbitrarily chosen nodes (a,b), see figure A.1, is calculated as

$$Z_{ab} = Z_{ab}\Big|_{A=0} \cdot \frac{1 + \beta_{sc} \cdot A}{1 + \beta_{oc} \cdot A}, \qquad (A.1)$$

where

$$-\beta_{sc} = \frac{Q_i}{Q_c}\Big|_{v_{ab}} = 0 \qquad -\beta_{oc} = \frac{Q_i}{Q_c}\Big|_{i_{ab}} = 0 \qquad (A.2)$$

 $Z_{ab}|_{A=0}$ is the impedance with the controlled generator set to zero (voltage or current). The controlled generator is treated as if it was independent when calculating β_{sc} and β_{oc} .

A.2 Complete Small Signal Model

A complete small signal model of the MOS transistor with inductive source degeneration is investigated to see the effect of all small signal parameters.

$$Z_{in} = X_{gb} \parallel Z_f \tag{A.3}$$

$$Z_f = Z_{f0} \cdot \frac{1 + \beta_{sc} \cdot g_m}{1 + \beta_{oc} \cdot g_m}$$
(A.4)

$$\frac{v_{gs}}{i_d} = -\beta_{oc} = -\frac{r_d \| (R_l \| X_{db} + X_{bs} \| Z_s) \cdot X_{gs}}{r_d \| (R_l \| X_{db} + X_{bs} \| Z_s) + X_{gd} + X_{gs}}$$
(A.5)

$$\frac{v_{gs}}{i_d} = -\beta_{sc} = -\frac{r_d \cdot X_{gs} \| X_{bs} \| Z_s}{r_d + X_{gd} \| R_l \| X_{db} + X_{gs} \| X_{bs} \| Z_s}$$
(A.6)

$$Z_{f0} = \frac{1 + \frac{X_{bs} \parallel Z_s}{X_{gs}} + \frac{X_{bs} \parallel Z_s}{r_d} - \frac{X_{bs} \parallel Z_s}{r_d} \cdot \frac{1 + \frac{X_{bs} \parallel Z_s}{X_{gs}} + \frac{X_{bs} \parallel Z_s}{r_d} + \frac{R_l \parallel X_{db}}{r_d}}{1 + \frac{X_{bs} \parallel Z_s}{r_d} + \frac{R_l \parallel X_{db}}{r_d} + \frac{R_l \parallel X_{db}}{X_{gd}}}{\frac{1}{1 + \frac{X_{bs} \parallel Z_s}{X_{gs}} + \frac{X_{bs} \parallel Z_s}{r_d} + \frac{R_l \parallel X_{db}}{r_d}}{\frac{1}{1 + \frac{X_{bs} \parallel Z_s}{X_{gs}} + \frac{X_{bs} \parallel Z_s}{r_d} + \frac{R_l \parallel X_{db}}{r_d}}{\frac{1}{1 + \frac{X_{bs} \parallel Z_s}{r_d} + \frac{R_l \parallel X_{db}}{r_d} + \frac{R_l \parallel X_{db}}{R_gd}}}$$

(A.7)

$$Z_{f} = \frac{(X_{gs} + X_{bs} \| Z_{s}) \cdot \left(1 + \frac{R_{l} \| X_{db}}{X_{gd}} + \frac{R_{l} \| X_{db}}{r_{d}}\right) + X_{gs} \cdot X_{bs} \| Z_{s} \cdot \left(g_{m} + \frac{1}{r_{d}}\right) \cdot \left(1 + \frac{R_{l} \| X_{db}}{X_{gd}}\right)}{1 + (X_{bs} \| Z_{s} + R_{l} \| X_{db}) \cdot \left(\frac{1}{r_{d}} + \frac{1}{X_{gd}}\right) + \frac{X_{gs}}{X_{gd}} \cdot \left(1 + \frac{X_{bs} \| Z_{s}}{r_{d}} + \frac{R_{l} \| X_{db}}{r_{d}} + (X_{gs} + X_{bs} \| Z_{s}) \cdot g_{m}\right)}$$
(A.8)

By identifying the major contributions at operating frequency for moderately large transistors Z_{in} is found to be

$$Z_{in} \approx \frac{\frac{1}{j\omega C_{gs}}(1+g_m r_s) + j\omega L_s \left(1 + \frac{C_{gd}}{C_{gs}} g_m R_L\right) + j\omega C_{gd} R_L r_s + \frac{L_s}{C_{gs}} g_m + r_s \left(1 + \frac{C_{gd}}{C_{gs}} g_m R_L\right) + \frac{C_{gd}}{C_{gs}} R_L (1-\omega^2 L_s C_{gs})}{1 + \frac{C_{gd}}{C_{gs}} g_m R_L + \frac{C_{gd} + C_{gb}}{C_{gs}} (1+g_m r_s) - \omega^2 L_s (C_{gd} + C_{gb}) + j\omega C_{gd} \left(\left(r_s + \frac{L_s}{C_{gs}} g_m\right) \left(1 + \frac{C_{gd}}{C_{gd}}\right) + R_L (1-\omega^2 L_s C_{gb}) + \frac{L_s}{C_{gd}} r_d\right)}$$
(A.9)

Once the transistor is bias the input resistance is mainly affected by the choice of operating frequency and transistor width, as the small signal parameters are equally scaled with the width of the transistor.



Figure A.2: Complete small signal model of a MOS transistor with inductive source degeneration.

At low frequencies the input resistance is

$$Re(Z_{in}) \approx \frac{\left(\frac{L_s}{C_{gs}}g_m + r_s\right)\left(1 + \frac{C_{gd}}{C_{gs}}g_m R_L\right)}{\left(1 + \frac{C_{gd}}{C_{gs}}g_m R_L + \frac{C_{gd} + C_{gb}}{C_{gs}}(1 + g_m r_s)\right)^2}$$
(A.10)

and for small sized transistor it is

$$Re(Z_{in}) \approx \frac{\left(\frac{L_s}{C_{gs}}g_m + r_s\right)}{\left(1 + \frac{C_{gd} + C_{gb}}{C_{gs}}\right)^2}$$
(A.11)

A.3 New Simplified Small Signal Model

The small signal model of the transistor has been simplified to only contain C_{gd} , C_{gs} and g_m . This model is used when the overall gain for the inverter is calculated.

$$Z_{in} = Z_{in0} \cdot \frac{1 + \beta_{sc} \cdot g_m}{1 + \beta_{oc} \cdot g_m}$$
(A.12)

$$\frac{v_{gs}}{i_d} = -\beta_{oc} = -\frac{X_s \cdot X_{gs}}{X_s + X_{gd} + X_{gs}}$$
(A.13)

A Input Impedance of the Common Source Amplifier

$$\frac{v_{gs}}{i_d} = -\beta_{sc} = -X_{gs} || X_s$$
 (A.14)

$$Z_{in0} = \frac{X_{gd}(X_{gs} + X_s)}{X_{gd} + X_{gs} + X_s}$$
(A.15)

$$Z_{in} = X_{gd} \frac{X_{gs} + X_s + X_{gs}X_s \cdot g_m}{X_{gd} + X_{gs} + X_s + X_{gs}X_s \cdot g_m}$$
(A.16)

$$= \frac{\frac{1}{j\omega C_{gs}} + j\omega L_{s} + \frac{L_{s}}{C_{gs}}g_{m}}{1 + \frac{C_{gd}}{C_{gs}} - \omega^{2}L_{s}C_{gd} + j\omega C_{gd}\frac{L_{s}}{C_{gs}}g_{m}}$$

=
$$\frac{\frac{1}{j\omega C_{gs}}\left(1 + \frac{C_{gd}}{C_{gs}} - \omega^{2}L_{s}C_{gd}\left(1 - \frac{L_{s}g_{m}^{2}}{C_{gs}}\right)\right) + j\omega L_{s}\left(1 + \frac{C_{gd}}{C_{gs}} - \omega^{2}L_{s}C_{gd}\right) + \frac{L_{s}}{C_{gs}}g_{m}}{\left(1 + \frac{C_{gd}}{C_{gs}} - \omega^{2}L_{s}C_{gd}\right)^{2} + \left(\omega C_{gd}\frac{L_{s}}{C_{gs}}g_{m}\right)^{2}}$$

For low frequencies and a small size of the transistor the new input impedance is given by

$$Z_{in} \approx \frac{\frac{1}{j\omega C_{gs}} + j\omega L_s}{1 + \frac{C_{gd}}{C_{gs}}} + \frac{\frac{L_s}{C_{gs}}g_m}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^2}$$
(A.17)

The input reactance is negative, giving a capacitive input. To compensate for the input capacitance the reactance of the inductance L_g in series with the input should be

$$j\omega_0 L_g = -\frac{\frac{1}{j\omega_0 C_{gs}} + j\omega_0 L_s}{1 + \frac{C_{gd}}{C_{gs}}}$$
(A.18)

at operating frequency ω_0 , giving that

$$1 - \omega_0^2 L_g C_{gs} - \omega_0^2 L_g C_{gd} - \omega_0^2 L_s C_{gs} = 0$$
 (A.19)

Appendix B

Gain of Various Stages

B.1 Superposition Model

In figure B.1a) is a model of a generic amplifier shown. Q_g is the signal from the input generator, while Q_l is the output signal across/through the load. Q_i is the input signal of the controlled generator, in the case of a MOS transistor it is v_{gs} , while Q_c is the output signal from the controlled generator, which is i_d in a MOS transistor. A is the gain of the controlled source and for a transistor it will be the transconductance g_m .

In figure B.1b) is a model of an amplifier with feedback shown. The gain A_f of the feedback circuit is given by

$$A_f = \rho + \frac{\xi v \cdot g_m}{1 + \beta \cdot g_m} \tag{B.1}$$

where ρ is the feed through, ξ and ν the input and output attenuation, respectively, while β is the feedback. All defined as

$$\frac{Q_l}{Q_g}\Big|_{Q_c = 0} = \rho \qquad \frac{Q_i}{Q_g}\Big|_{Q_c = 0} = \xi$$

$$\frac{Q_l}{Q_c}\Big|_{Q_g = 0} = \nu \qquad \frac{Q_i}{Q_c}\Big|_{Q_g = 0} = -\beta$$
(B.2)

B.2 Transconductance Amplifier

The inverter is a transconductance amplifier, where the influence of the parasitic feedback due to C_{gd} usually is ignored. As it has been found in section 2.4.1 that C_{gd} has a large influence on the input impedance the gain of the transconductance amplifier will be calculat-



Figure B.1: a) Generic amplifier. b) Signal-flow-graph of an amplifier with feedback.

ed with C_{gd} excluded, giving the traditional result, and with C_{gd} included, giving a slightly different gain.

B.2.1 Schematic

The schematic of the inverter is shown in figure 2.13 on page 29 and figure B.2.



Figure B.2: New simplified small signal model of transconductance amplifier

B.2.2 Gate Drain Capacitance Excluded

Excluding C_{gd} gives that its assumed to be zero.

$$C_{gd} = 0 \tag{B.3}$$

The feed through, input and output attenuation and the feedback becomes

$$\frac{i_l}{v_g} = \rho = 0 \tag{B.4}$$

$$\frac{v_{gs}}{v_g} = \xi = \frac{X_{gs}}{Z_g + X_{gs} + X_s}$$
 (B.5)

$$\frac{i_l}{i_d} = v = -1 \tag{B.6}$$

$$\frac{v_{gs}}{i_d} = -\beta = -\frac{X_{gs}X_s}{X_{gs} + X_s + Z_g}$$
(B.7)

The transconductance gain A_g at the operating frequency ω_0 is given as

$$A_{g} = 0 + \frac{\frac{X_{gs}}{Z_{g} + X_{gs} + X_{s}}(-1) \cdot g_{m}}{1 + \frac{X_{gs}X_{s}}{X_{gs} + X_{s} + Z_{g}} \cdot g_{m}} = -\frac{X_{gs}g_{m}}{Z_{g} + X_{gs} + X_{s} + X_{gs}X_{s} \cdot g_{m}}$$
(B.8)

$$= -\frac{g_m}{j\omega C_{gs}R_g - \omega^2 L_g C_{gs} + 1 - \omega^2 L_s C_{gs} + j\omega L_s g_m} = [\omega = \omega_0]$$

$$= -\frac{g_m}{j\omega_0 C_{gs}R_g + j\omega_0 L_s g_m}$$

where the operating frequency ω_0 is defined for

$$1 - \omega_0^2 L_g C_{gs} - \omega_0^2 L_s C_{gs} = 0$$
 (B.9)

B.2.3 Gate Drain Capacitance Included

Including C_{gd} in the model gives the feed through, input and output attenuation and the feedback as

$$\frac{i_l}{v_g} = \rho = \frac{1}{Z_g + (X_{gs} + X_s) \parallel X_{gd}} \cdot \frac{X_{gs} + X_s}{X_{gs} + X_s + X_{gd}}$$
(B.10)

$$\frac{v_{gs}}{v_g} = \xi = \frac{(X_{gs} + X_s) \parallel X_{gd}}{Z_g + (X_{gs} + X_s) \parallel X_{gd}} \cdot \frac{X_{gs}}{X_{gs} + X_s}$$
(B.11)

$$\frac{i_l}{i_d} = \mathbf{v} = -1 \tag{B.12}$$

$$\frac{v_{gs}}{i_d} = -\beta = -\frac{X_{gs}X_s}{X_{gs} + X_s + Z_g \parallel X_{gd}}$$
(B.13)

The transconductance gain A_g is given as

$$A_{g} = \frac{1}{Z_{g} + (X_{gs} + X_{s}) \parallel X_{gd}} \cdot \frac{X_{gs} + X_{s}}{X_{gs} + X_{s} + X_{gd}} + \frac{\left(\frac{(X_{gs} + X_{s}) \parallel X_{gd}}{Z_{g} + (X_{gs} + X_{s}) \parallel X_{gd}} \cdot \frac{X_{gs}}{X_{gs} + X_{s}}\right)(-1) \cdot g_{m}}{1 + \frac{X_{gs}X_{s}}{X_{gs} + X_{s} + Z_{g} \parallel X_{gd}} \cdot g_{m}}$$
(B.14)

The influence of ρ is considered negligible, giving that the transconductance gain A_g at the operating frequency ω_0 is given as

$$A_{g} \approx -\frac{\left(\frac{(X_{gs} + X_{s}) \| X_{gd}}{Z_{g} + (X_{gs} + X_{s}) \| X_{gd}} \cdot \frac{X_{gs}}{X_{gs} + X_{s}}\right)g_{m}}{1 + \frac{X_{gs}X_{s}}{X_{gs} + X_{s} + Z_{g} \| X_{gd}} \cdot g_{m}}$$

$$= -\frac{X_{gd}X_{gs}g_{m}}{(X_{gs} + X_{s})(Z_{g} + X_{gd}) + Z_{g}X_{gd} + X_{gs}X_{s}(Z_{g} + X_{gd})g_{m}}$$

$$= -\frac{g_{m}}{(X_{gs} + X_{s})(Z_{g} + X_{gd}) + Z_{g}X_{gd}} \cdot g_{m} + Z_{gs}X_{s}(Z_{g} + X_{gd})g_{m}}$$

$$(1 - \omega^2 L_s C_{gs})(1 - \omega^2 L_g C_{gd} + j\omega C_{gd} R_g) + j\omega C_{gs} R_g - \omega^2 L_g C_{gs} + j\omega L_s (1 - \omega^2 L_g C_{gd} + j\omega C_{gd} R_g) g_m$$

$$= -\frac{g_m}{1 - \omega^2 (L_g + L_s) C_{gs} - \omega^2 L_g C_{gd} (1 - \omega^2 L_g C_{gs} + R_g g_m) + j \omega (C_{gs} + C_{gd}) R_g \left(1 - \omega^2 L_s \frac{C_{gd} C_{gs}}{C_{gd} + C_{gs}}\right) + j \omega L_s g_m (1 - \omega^2 L_g C_{gd})$$
(B.15)

An approximation of the equation B.15 is

$$A_{g} \approx -\frac{g_{m}}{1 - \omega^{2}L_{g}C_{gs} - \omega^{2}L_{g}C_{gd} - \omega^{2}L_{s}C_{gs} + j\omega(C_{gs} + C_{gd})R_{g} + j\omega L_{s}g_{m}}$$
(B.16)
$$= [\omega = \omega_{0}] = -\frac{g_{m}}{j\omega_{0}(C_{gs} + C_{gd})R_{g} + j\omega_{0}L_{s}g_{m}}$$

where the operating frequency ω_0 is defined for

$$1 - \omega_0^2 L_g C_{gs} - \omega_0^2 L_g C_{gd} - \omega_0^2 L_s C_{gs} = 0$$
 (B.17)

B.3 Current Follower

The schematic is shown in figure 2.16 on page 36 and in figure B.3.



Figure B.3: The current follower with an LC-tank.

The loading impedance of the LC-tank is

$$(X_{Lc} + r_c) \parallel X_2 \parallel \frac{1}{g_f} = [\omega = \omega_0] = R_{pc}$$
(B.18)

where ω_0 is defined in equation B.17.

The feed through, input and output attenuation and the feedback becomes

$$\frac{i_l}{i_g} = \rho = \frac{X_1}{X_1 + r_{dc} + (X_{Lc} + r_c) \parallel X_2 \parallel \frac{1}{g_f}} = \frac{X_1}{X_1 + r_{dc} + R_{pc}}$$
(B.19)

$$\frac{v_{gs}}{i_g} = \xi = -\frac{r_{dc} + (X_{Lc} + r_c) \| X_2 \| \frac{1}{g_f}}{X_1 + r_{dc} + (X_{Lc} + r_c) \| X_2 \| \frac{1}{g_f}} \cdot X_1$$
(B.20)

$$= -\frac{r_{dc} + K_{pc}}{X_1 + r_{dc} + R_{pc}} \cdot X_1$$

$$\frac{i_l}{i_d} = v = -\frac{r_{dc}}{r_{dc} + (X_{Lc} + r_c) \| X_2 \| \frac{1}{g_f} + X_1} = -\frac{r_{dc}}{r_{dc} + R_{pc} + X_1}$$
(B.21)

$$\frac{v_{gs}}{i_d} = -\beta = -\frac{r_{dc}X_1}{r_{dc} + (X_{Lc} + r_c) \|X_2\| \frac{1}{g_f} + X_1} = -\frac{r_{dc}X_1}{r_{dc} + R_{pc} + X_1} \cdot X_1 \quad (B.22)$$

The current gain A_i is

$$A_{i} = \frac{i_{l}}{i_{g}} = \frac{X_{1}}{X_{1} + r_{dc} + R_{pc}} + \frac{\frac{(r_{dc} + R_{pc})X_{1}}{X_{1} + r_{dc} + R_{pc}} \frac{r_{dc}}{r_{dc} + R_{pc} + X_{1}} g_{mc}}{1 + \frac{r_{dc}X_{1}}{r_{dc} + R_{pc} + X_{1}} g_{mc}}$$
(B.23)
$$= \frac{X_{1} + \frac{r_{dc}X_{1}^{2}g_{mc}}{X_{1} + r_{dc} + R_{pc}} + \frac{(r_{dc} + R_{pc})r_{dc}X_{1}g_{mc}}{X_{1} + r_{dc} + R_{pc}}}{X_{1} + r_{dc} + R_{pc}}$$

$$= \frac{1}{1 + \frac{r_{dc} + R_{pc}}{X_1(1 + r_{dc}g_{mc})}} = \frac{1}{1 + \frac{r_{dc} + R_{pc}}{\frac{1}{j\omega_0 C_1}(1 + r_{dc}g_{mc})}}$$

B.4 Voltage Follower

The schematic is shown in figure 2.17 on page 38 and in figure B.4.

The feed through, input and output attenuation and the feedback becomes

$$\frac{v_l}{v_g} = \rho = \frac{X_L}{X_{gsf} + X_L}$$
(B.24)

$$\frac{v_{gs}}{v_g} = \xi = \frac{X_{gsf}}{X_{gsf} + X_L}$$
(B.25)

$$\frac{v_l}{i_d} = v = \frac{X_{gsf}}{X_{gsf} + X_L} \cdot X_L$$
(B.26)

$$\frac{v_{gs}}{i_d} = -\beta = -\frac{X_L}{X_{gsf} + X_L} \cdot X_{gsf}$$
(B.27)

The voltage gain A_v is

$$A_{v} = \frac{v_{l}}{v_{g}} = \frac{X_{L}}{X_{gsf} + X_{L}} + \frac{\frac{X_{gsf}}{X_{gsf} + X_{L}} \frac{X_{gsf}}{X_{gsf} + X_{L}} X_{L}g_{mf}}{1 + \frac{X_{L}}{X_{gsf} + X_{L}} X_{gsf}g_{mf}}$$
(B.28)
$$= \frac{X_{L} \left(1 + \frac{X_{L}}{X_{gsf} + X_{L}} X_{gsf}g_{mf}\right) + \frac{X_{gsf}^{2}}{X_{gsf} + X_{L}} X_{L}g_{mf}}{X_{gsf} + X_{L} + X_{L} X_{gsf}g_{mf}}$$

$$= \frac{X_L + X_L X_{gsf} g_{mf}}{X_{gsf} + X_L + X_L X_{gsf} g_{mf}} = \frac{1}{1 + \frac{j\omega C_L}{j\omega C_{gsf} + g_{mf}}}$$



Figure B.4: Voltage follower with capacitive load.

Appendix C

Noise

C.1 Schematic

To find the optimum/minimum noise for the inverter amplifier, the equivalent input noise sources, v_i and i_i , has to be calculated from the transistors input noise sources, v_{ia} and i_{ia} .

The method is to calculate the output noise current for all the sources and then compare the equivalent noise source with all the contributions from the different transistor noise sources. It is assumed that the output noise voltage is negligible due to a small load.

Figure C.1 shows the noise sources where

$$v_{ia} = v_{ia1} = v_{ia2}$$

 $i_{ia} = i_{ia1} = i_{ia2}$
(C.1)

C.2 Calculating the Equivalent Noise Sources

C.2.1 Output Noise as a Function of Equivalent Input Noise

The output current i_o is calculated from the input noise sources in figure C.1a).

C.2.1.1 Open Circuit

When the input is an open circuit the output signal i_o is only dependent on i_i .



a)



b)



c)

Figure C.1: a) The equivalent input noise sources. b) The input noise of the inverter. c) The input noise sources relocated to calculate the output noise and then comparing them with the equivalent noise sources.

The node equations are

$$i_{i} - i_{gs} - i_{gd} = 0 \qquad v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$i_{gs} + i_{d} - i_{s} = 0 \qquad v_{s} = j\omega L_{s} \cdot i_{s}$$

$$i_{gd} - i_{d} + i_{o} = 0 \qquad v_{gd} = \frac{1}{j\omega C_{gd}} \cdot i_{gd}$$

$$i_{d} = g_{m} \cdot v_{gs}$$
(C.2)

$$j\omega L_s \cdot i_s + \frac{1}{j\omega C_{gs}} \cdot i_{gs} - \frac{1}{j\omega C_{gd}} \cdot i_{gd} = 0$$
(C.3)

$$j\omega L_{s} \cdot (i_{gs} + i_{d}) + \frac{1}{j\omega C_{gs}} \cdot i_{gs} - \frac{1}{j\omega C_{gd}} \cdot (i_{d} - i_{o}) = 0$$
(C.4)

$$j\omega L_{s} \cdot \left(i_{gs} + \frac{g_{m}}{j\omega C_{gs}} \cdot i_{gs}\right) + \frac{1}{j\omega C_{gs}} \cdot i_{gs} - \frac{1}{j\omega C_{gd}} \cdot \left(\frac{g_{m}}{j\omega C_{gs}} \cdot i_{gs} - i_{o}\right) = 0 \quad (C.5)$$

$$\left(j\omega L_s + \frac{L_s g_m}{C_{gs}} + \frac{1}{j\omega C_{gs}} + \frac{g_m}{\omega^2 C_{gd} C_{gs}}\right)i_{gs} + \frac{i_o}{j\omega C_{gd}} = 0$$
(C.6)

Find an expression for i_{gs} that are dependent on i_i and/or i_o .

$$i_i - i_{gs} - (i_d - i_o) = 0$$
 (C.7)

$$\dot{i}_i - \dot{i}_{gs} - \left(\frac{g_m}{j\omega C_{gs}} \cdot \dot{i}_{gs} - \dot{i}_o\right) = 0$$
(C.8)

$$i_{gs} = \frac{i_i + i_o}{1 + \frac{g_m}{j\omega C_{gs}}}$$
(C.9)

Express i_o as a function of i_i

$$\left(j\omega L_s + \frac{L_s g_m}{C_{gs}} + \frac{1}{j\omega C_{gs}} + \frac{g_m}{\omega^2 C_{gd} C_{gs}}\right) \frac{i_i + i_o}{1 + \frac{g_m}{j\omega C_{gs}}} + \frac{i_o}{j\omega C_{gd}} = 0 \quad (C.10)$$

C Noise

$$i_{i} + i_{o} \left(1 + \frac{1 + \frac{g_{m}}{j\omega C_{gs}}}{j\omega C_{gd} \left(j\omega L_{s} + \frac{L_{s}g_{m}}{C_{gs}} + \frac{1}{j\omega C_{gs}} + \frac{g_{m}}{\omega^{2}C_{gd}C_{gs}} \right)} \right) = 0$$
(C.11)

$$i_{o} = -\frac{1}{1 + \frac{g_{m}}{j\omega C_{gs}}} i_{i} \qquad (C.12)$$

$$1 + \frac{g_{m}}{\omega^{2}L_{s}C_{gd} + j\omega L_{s}\frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}} - \frac{g_{m}}{j\omega C_{gs}}$$

$$i_{o} = -\frac{-\omega^{2}L_{s}C_{gd} + j\omega L_{s}\frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}} - \frac{g_{m}}{j\omega C_{gs}}}{-\omega^{2}L_{s}C_{gd} + j\omega L_{s}\frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}} - \frac{g_{m}}{j\omega C_{gs}}}{-\frac{g_{m}}{\omega^{2}L_{s}C_{gd}} + j\omega L_{s}\frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}}g_{m} + \frac{C_{gd}}{C_{gs}}g_{m}} i_{i}$$

$$(C.13)$$

$$i_{o} = -\frac{j\omega C_{gd}(1 - \omega^{2}L_{s}C_{gs} + j\omega L_{s}g_{m}) - g_{m}}{j\omega C_{gd}(1 - \omega^{2}L_{s}C_{gs} + j\omega L_{s}g_{m}) + j\omega C_{gs}}i_{i}$$
(C.14)

If the gate drain capacitance is zero then

$$i_o = \frac{g_m}{j\omega C_{gs}} i_i \tag{C.15}$$

C.2.1.2 Short Circuit

When the input is a short circuit the output signal i_o is only dependent on v_i . The node equations are

$$v_{i} - v_{gs} - v_{s} = 0$$

$$v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$v_{i} - v_{gd} = 0$$

$$v_{s} = j\omega L_{s} \cdot i_{s}$$

$$i_{gs} + i_{d} - i_{s} = 0$$

$$v_{gd} = \frac{1}{j\omega C_{gd}} \cdot i_{gd}$$

$$i_{d} = g_{m} \cdot v_{gs}$$

$$v_{i} - \frac{1}{j\omega C_{gd}} (i_{d} - i_{o}) = 0$$
(C.17)

C.2 Calculating the Equivalent Noise Sources

$$v_i - \frac{1}{j\omega C_{gd}} \left(\frac{g_m}{j\omega C_{gs}} i_{gs} - i_o \right) = 0$$
 (C.18)

Find an expression for i_{gs} that are dependent on v_i and/or i_o .

$$v_i - \frac{1}{j\omega C_{gs}} i_{gs} - j\omega L_s (i_{gs} + i_d) = 0$$
 (C.19)

$$v_i - i_{gs} \left(\frac{1}{j\omega C_{gs}} + j\omega L_s \left(1 + \frac{g_m}{j\omega C_{gs}} \right) \right) = 0$$
 (C.20)

$$i_{gs} = \frac{v_i}{\left(\frac{1}{j\omega C_{gs}} + j\omega L_s \left(1 + \frac{g_m}{j\omega C_{gs}}\right)\right)}$$
(C.21)

Express i_o as a function of v_i

$$v_{i} - \frac{1}{j\omega C_{gd}} \left(\frac{g_{m}}{j\omega C_{gs}} \frac{v_{i}}{\left(\frac{1}{j\omega C_{gs}} + j\omega L_{s} \left(1 + \frac{g_{m}}{j\omega C_{gs}}\right)\right)} - i_{o} \right) = 0$$
(C.22)

$$v_i \left(1 - \frac{1}{j\omega C_{gd}} \frac{g_m}{\left(1 - \omega^2 L_s C_{gs} \left(1 + \frac{g_m}{j\omega C_{gs}}\right)\right)}\right) + \frac{i_o}{j\omega C_{gd}} = 0$$
(C.23)

$$i_o = -v_i \left(j \omega C_{gd} - \frac{g_m}{1 - \omega^2 L_s C_{gs} + j \omega L_s g_m} \right)$$
(C.24)

If the gate drain capacitance is zero then

$$i_o = v_i \frac{g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m}$$
(C.25)

C.2.2 Output Noise as a Function of Transistor Input Noise

The output current i_o is calculated from the equivalent transistor noise sources in figure C.1c).

C.2.2.1 Open Circuit

When the input is an open circuit the output current i_o is dependent on i_{ia1} , i_{ia2} and v_{ia2} .

i_o as a function of i_{ia1}

The calculated result of i_i , equation C.14, and i_{ial} is the same giving

$$i_o = -\frac{j\omega C_{gd}(1 - \omega^2 L_s C_{gs} + j\omega L_s g_m) - g_m}{j\omega C_{gd}(1 - \omega^2 L_s C_{gs} + j\omega L_s g_m) + j\omega C_{gs}}i_{ia1}$$
(C.26)

If the gate drain capacitance is zero then

$$i_o = \frac{g_m}{j\omega C_{gs}} i_{ia1} \tag{C.27}$$

i_o as a function of i_{ia2}

The node equations

$$-i_{gs} - i_{gd} = 0 \qquad \qquad v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$i_{gs} - i_{ia2} + i_d - i_s = 0 \qquad \qquad v_s = j\omega L_s \cdot i_s$$

$$i_{gd} - i_d + i_o = 0 \qquad \qquad v_{gd} = \frac{1}{j\omega C_{gd}} \cdot i_{gd}$$

$$i_d = g_m \cdot v_{gs}$$
(C.28)

$$j\omega L_{s}i_{s} + \frac{1}{j\omega C_{gs}}i_{gs} + \frac{1}{j\omega C_{gd}}i_{gs} = 0$$
 (C.29)

$$i_s = -\frac{i_{gs}}{j\omega L_s} \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}} \right)$$
(C.30)

$$i_{gs} - i_{ia2} - i_{gs} + i_o + \frac{i_{gs}}{j\omega L_s} \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}} \right) = 0$$
(C.31)

$$-i_{ia2} + i_o + \frac{i_{gs}}{j\omega L_s} \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}} \right) = 0$$
(C.32)

Find an expression for i_{gs} that are dependent on i_{ia2} and/or i_o .

$$-i_{gs} - g_m v_{gs} + i_o = 0 (C.33)$$

$$i_{gs} = \frac{i_o}{1 + \frac{g_m}{j\omega C_{gs}}}$$
(C.34)

C.2 Calculating the Equivalent Noise Sources

Express i_o as a function of i_{ia2} .

$$-i_{ia2} + i_o + \frac{1}{j\omega L_s} \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}} \right) \frac{i_o}{1 + \frac{g_m}{j\omega C_{gs}}} = 0$$
(C.35)

$$-i_{ia2}\left(1+\frac{g_m}{j\omega C_{gs}}\right) + \left(1+\frac{g_m}{j\omega C_{gs}}+\frac{1}{j\omega L_s}\left(\frac{1}{j\omega C_{gs}}+\frac{1}{j\omega C_{gd}}\right)\right)i_o = 0 \qquad (C.36)$$

$$i_o = i_{ia2} \frac{1 + \frac{g_m}{j\omega C_{gs}}}{1 + \frac{g_m}{j\omega C_{gs}} + \frac{1}{j\omega L_s} \left(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}}\right)}$$
(C.37)

$$i_o = i_{ia2} \frac{-\omega^2 C_{gs} L_s + j\omega L_s g_m}{-\omega^2 C_{gs} L_s + g_m j\omega L_s + 1 + \frac{C_{gs}}{C_{gd}}}$$
(C.38)

$$i_o = i_{ia2} \frac{j\omega C_{gd}(-\omega^2 C_{gs}L_s + j\omega L_s g_m)}{j\omega C_{gd}(1 - \omega^2 C_{gs}L_s + g_m j\omega L_s) + j\omega C_{gs}}$$
(C.39)

If the gate drain capacitance is zero then

$$i_o = 0 \tag{C.40}$$

i_o as a function of v_{ia2}

The node equations

$$-i_{gs} - i_{gd} = 0 \qquad v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$i_{gs} + i_d - i_s = 0 \qquad v_s = j\omega L_s \cdot i_s$$

$$i_{gd} - i_d + i_o = 0 \qquad v_{gd} = \frac{1}{j\omega C_{gd}} \cdot i_{gd}$$

$$v_s + v_{gs} - v_{ia2} - v_{gd} = 0 \qquad i_d = g_m \cdot v_{gs}$$
(C.41)

$$j\omega L_{s}(i_{gs} + i_{d}) + \frac{1}{j\omega C_{gs}}i_{gs} - v_{ia2} + \frac{1}{j\omega C_{gd}}i_{gs} = 0$$
(C.42)

$$\left(j\omega L_{s}\left(1+\frac{g_{m}}{j\omega C_{gs}}\right)+\frac{1}{j\omega C_{gs}}+\frac{1}{j\omega C_{gd}}\right)i_{gs}-v_{ia2} = 0$$
(C.43)

Find an expression for i_{gs} that are dependent on v_{ia2} and/or i_o .

$$-i_{gs} - g_m v_{gs} + i_o = 0 (C.44)$$

$$i_{gs} = \frac{i_o}{1 + \frac{g_m}{j\omega C_{gs}}}$$
(C.45)

Express i_o as a function of v_{ia2} .

$$\left(j\omega L_{s}\left(1+\frac{g_{m}}{j\omega C_{gs}}\right)+\frac{1}{j\omega C_{gs}}+\frac{1}{j\omega C_{gd}}\right)\frac{i_{o}}{1+\frac{g_{m}}{j\omega C_{gs}}}-v_{ia2} = 0 \quad (C.46)$$

$$\left(-\omega^{2}L_{s}C_{gs} + j\omega L_{s}g_{m} + 1 + \frac{C_{gs}}{C_{gd}}\right)\frac{i_{o}}{j\omega C_{gs} + g_{m}} - v_{ia2} = 0$$
(C.47)

$$i_o = v_{ia2} \frac{j\omega C_{gd}(j\omega C_{gs} + g_m)}{j\omega C_{gd}(1 - \omega^2 C_{gs} L_s + g_m j\omega L_s) + j\omega C_{gs}}$$
(C.48)

If the gate drain capacitance is zero then

$$i_o = 0 \tag{C.49}$$

C.2.2.2 Short Circuit

When the input is a short circuit the output current i_o is given by v_{ia1} , v_{ia2} and i_{ia2} .

i_o as a function of v_{ia1}

The calculated result of v_i , in equation C.24, and v_{ial} is the same giving

$$i_o = -v_{ia1} \left(j\omega C_{gd} - \frac{g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m} \right)$$
(C.50)

If the gate drain capacitance is zero then

$$i_o = v_{ia1} \frac{g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m}$$
(C.51)

i_o as a function of v_{ia2}

The node equations are

$$-v_{gs} - v_{s} = 0$$

$$v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$-v_{ia2} - v_{gd} = 0$$

$$v_{s} = j\omega L_{s} \cdot i_{s}$$

$$i_{gs} + i_{d} - i_{s} = 0$$

$$i_{gd} - i_{d} + i_{o} = 0$$

$$v_{gd} = \frac{1}{j\omega C_{gd}} \cdot i_{gd}$$

$$i_{d} = g_{m} \cdot v_{gs}$$
(C.52)

$$-v_{ia2} - \frac{1}{j\omega C_{gd}}(i_d - i_o) = 0$$
 (C.53)

$$-v_{ia2} - \frac{1}{j\omega C_{gd}} \left(\frac{g_m}{j\omega C_{gs}} i_{gs} - i_o \right) = 0$$
(C.54)

Find an expression for i_{gs} that are dependent on v_{ia2} and/or i_o .

$$i_{gs} + \frac{1}{j\omega C_{gd}}i_{gs} + \frac{v_{gs}}{j\omega L_s} = 0$$
 (C.55)

$$i_{gs} = 0$$

$$v_{gs} = 0$$

$$i_{d} = 0$$
(C.56)

$$-v_{ia2} + \frac{1}{j\omega C_{gd}}i_o = 0$$
 (C.57)

$$i_o = j \omega C_{gd} v_{ia2} \tag{C.58}$$

If the gate drain capacitance is zero then

$$i_o = 0 \tag{C.59}$$

i_o as a function of i_{ia2}

The node equations

$$-v_{gs} - v_{s} = 0 \qquad v_{gs} = \frac{1}{j\omega C_{gs}} \cdot i_{gs}$$

$$-v_{gd} = 0 \qquad v_{s} = j\omega L_{s} \cdot i_{s}$$

$$i_{gs} - i_{ia2} + i_{d} - i_{s} = 0$$

$$i_{gd} - i_{d} + i_{o} = 0$$

$$i_{d} = g_{m} \cdot v_{gs}$$

$$(C.60)$$

$$-i_d + i_o = 0 \tag{C.61}$$

$$i_{gs} - i_{ia2} + i_o + \frac{1}{-\omega^2 L_s C_{gs}} i_{gs} = 0$$
 (C.62)

$$i_{gs} = i_o \frac{j \omega C_{gs}}{g_m} \tag{C.63}$$

$$\left(\frac{j\omega C_{gs}}{g_m} + 1 + \frac{1}{-\omega^2 L_s C_{gs}} \frac{j\omega C_{gs}}{g_m}\right) i_o - i_{ia2} = 0$$
(C.64)

$$i_o = i_{ia2} \frac{j\omega L_s g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m}$$
(C.65)

 i_o is independent of the gate drain capacitance.

C.2.3 Equivalent Noise as a Function of Transistor Noise

The input noise current i_i is calculated as a function of i_{ia} and v_{ia} , defined by equation C.1

C.2.3.1 Open Circuit

When the input is an open circuit the result is given by equations C.14, C.26, C.39 and C.48.

C.2 Calculating the Equivalent Noise Sources

$$\frac{-j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+g_{m}}{j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+j\omega C_{gs}}i_{i} = (C.66)$$

$$\frac{-j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+j\omega C_{gs}}{j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+j\omega C_{gs}}i_{ia} + \frac{j\omega C_{gd}(-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})}{j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+g_{m}j\omega L_{s})+j\omega C_{gs}}i_{ia} + \frac{j\omega C_{gd}(j\omega C_{gs}+g_{m})}{j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+g_{m}j\omega L_{s})+j\omega C_{gs}}v_{ia}$$

$$i_{i} = i_{ia} + \frac{j\omega C_{gd}(-\omega^{2}C_{gs}L_{s}+j\omega L_{s}g_{m})}{-j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+g_{m}}i_{ia} + \frac{j\omega C_{gd}(j\omega C_{gs}+g_{m})}{-j\omega C_{gd}(1-\omega^{2}L_{s}C_{gs}+j\omega L_{s}g_{m})+g_{m}}i_{ia} + \frac{j\omega C_{gd}(j\omega C_{gs}+g_{m})$$

$$i_{i} = \frac{-j\omega C_{gd} + g_{m}}{-j\omega C_{gd} (1 - \omega^{2} L_{s} C_{gs} + j\omega L_{s} g_{m}) + g_{m}} i_{ia} + \frac{j\omega C_{gd} (j\omega C_{gs} + g_{m})}{-j\omega C_{gd} (1 - \omega^{2} L_{s} C_{gs} + j\omega L_{s} g_{m}) + g_{m}} v_{ia}$$
(C.68)

If the gate drain capacitance is zero then

$$i_i = i_{ia} \tag{C.69}$$

C.2.3.2 Short Circuit

When the input is a short circuit the result is given by equations C.24, C.50, C.58 and C.65.

$$\begin{pmatrix} -j\omega C_{gd} + \frac{g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m} \end{pmatrix} v_i =$$
(C.70)
$$\begin{pmatrix} -j\omega C_{gd} + \frac{g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m} \end{pmatrix} v_{ia} + j\omega C_{gd} v_{ia} +$$
$$\frac{j\omega L_s g_m}{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m} i_{ia}$$

$$\begin{pmatrix} -j\omega C_{gd} \frac{1 - \omega^2 L_s C_{gs} + j\omega L_s g_m}{g_m} + 1 \end{pmatrix} v_i = v_{ia} + j\omega L_s i_{ia}$$
(C.71)
$$v_i = \frac{v_{ia} + j\omega L_s i_{ia}}{1 - \frac{j\omega C_{gd}}{g_m} (1 - \omega^2 L_s C_{gs}) + \omega^2 L_s C_{gd}}$$
(C.72)

If the gate drain capacitance is zero then

$$v_i = v_{ia} + j\omega L_s i_{ia} \tag{C.73}$$

C.3 Total Equivalent Input Noise Voltage

The generator impedance is

$$Z_g = R_g + j\omega L_g \tag{C.74}$$

C.3.1 Gate Drain Capacitance is Zero

$$v_{eT} = v_{ia} + j\omega L_s i_{ia} + (R_g + j\omega L_g) i_{ia}$$
(C.75)

$$v_{eT} = v_{ia} + (R_g + j\omega(L_g + L_s))i_{ia}$$
 (C.76)

C.3.2 Gate Drain Capacitance is not Zero

$$v_{eT} = \frac{v_{ia} + j\omega L_s i_{ia}}{1 - \frac{j\omega C_{gd}}{g_m} (1 - \omega^2 L_s C_{gs}) + \omega^2 L_s C_{gd}} +$$
(C.77)

$$(R_g + j\omega L_g) \left(\frac{-j\omega C_{gd} + g_m}{-j\omega C_{gd} (1 - \omega^2 L_s C_{gs} + j\omega L_s g_m) + g_m} i_{ia} + \frac{j\omega C_{gd} (j\omega C_{gs} + g_m)}{-j\omega C_{gd} (1 - \omega^2 L_s C_{gs} + j\omega L_s g_m) + g_m} v_{ia} \right)$$

The total noise can be expressed as

$$v_{eT} = \frac{v_{ia} + j\omega L_s i_{ia} + (R_g + j\omega L_g) \left(\left(-\frac{j\omega C_{gd}}{g_m} + 1 \right) i_{ia} + j\omega C_{gd} \left(\frac{j\omega C_{gs}}{g_m} + 1 \right) v_{ia} \right)}{1 - \frac{j\omega C_{gd}}{g_m} (1 - \omega^2 L_s C_{gs}) + \omega^2 L_s C_{gd}}$$
(C.78)

As usual it is necessary to make some assumptions.

For the numerator it is assumed that

$$1 - \frac{j\omega C_{gd}}{g_m} (1 - \omega^2 L_s C_{gs}) + \omega^2 L_s C_{gd} \approx 1$$
(C.79)
C.3 Total Equivalent Input Noise Voltage

and for v_{ia}

$$v_{ia} + (R_g + j\omega L_g) j\omega C_{gd} \left(\frac{j\omega C_{gs}}{g_m} + 1\right) v_{ia} \approx v_{ia}$$
(C.80)

For i_{ia} it is not this simple. To be able to make the noise factor calculation independent of the inductances one would like to find that the total equivalent input noise has a dependency on the input inductance given as

$$L_{in} = \frac{L_s}{1 + \frac{C_{gd}}{C_{gs}}}$$
(C.81)

The noise contribution from i_{ia} is

$$j\omega L_{s}i_{ia} + (R_{g} + j\omega L_{g})\left(-\frac{j\omega C_{gd}}{g_{m}} + 1\right)i_{ia} =$$

$$\left(j\omega L_{s} + R_{g} + j\omega L_{g} - R_{g}\frac{j\omega C_{gd}}{g_{m}} + \frac{\omega^{2}L_{g}C_{gd}}{g_{m}}\right)i_{ia} =$$

$$\left(R_{g} + j\omega L_{g}\left(1 - \frac{j\omega C_{gd}}{g_{m}}\right) + j\omega L_{s} - R_{g}\frac{j\omega C_{gd}}{g_{m}}\right)i_{ia}$$
(C.82)

It is possible to use the fact that

$$R_{g} = \frac{\frac{L_{s}}{C_{gs}}g_{m}}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^{2}}$$
(C.83)
$$j\omega L_{s} - R_{g}\frac{j\omega C_{gd}}{g_{m}} = j\omega L_{s}\left(1 - \frac{\frac{C_{gd}}{C_{gs}}}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^{2}}\right) = j\omega L_{s}\frac{1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_{gs}}^{2}}{\left(1 + \frac{C_{gd}}{C_{gs}}\right)^{2}} \approx \frac{j\omega L_{s}}{1 + \frac{C_{gd}}{C_{gs}}}$$
(C.84)

Assuming that $j\omega C_{gd}/g_m \ll 1$ gives an input noise of

$$v_{eT} = v_{ia} + \left(R_g + j\omega \left(L_g + \frac{L_s}{1 + \frac{C_{gd}}{C_{gs}}} \right) \right) i_{ia}$$
(C.85)

C Noise

Appendix D

Gaussian Approximation

For a stochastic variable X with Gaussian distribution, it is possible calculate a Gaussian approximation [27] of the mean value and variance for a function f(X). If the standard deviation σ of the stochastic variable X is much smaller than the mean value *m* and the mean value is separated from zero, then the mean value and variance of the function f(X) is defined as

$$E(f(X)) \approx f(E(X))$$

$$V(f(X)) \approx V(X) \cdot [f'(E(X))]^2$$
(D.1)

f(X) is then calculated, with E(X)=m, as

$$f(X) = f(m) + (X - m) \cdot f'(m) + \text{residue}$$
(D.2)

where the residue should be very small.

If there are several stochastic variables then the Gaussian approximation is calculated from

$$E(f(X_1, X_2, ..., X_n)) \approx f(m_1, m_2, ..., m_n)$$

$$V(f(X_1, X_2, ..., X_n)) \approx \sum_{i=1}^{n} V(X_i) \left(\frac{\partial f}{\partial m_i}\right)^2 + 2\sum_{i < j} C(X_i, X_j) \frac{\partial f}{\partial m_i} \frac{\partial f}{\partial m_j}$$
(D.3)

D Gaussian Approximation

Appendix E

Conductance Model

E.1 Transistor Parameters with Mismatch

In the process used, AMS $0.35\mu m$, CMOS transistors are modelled with the BSIM3v3 model, where VTH0, tox, wint and lint are the parameters with mismatch, while all others are assumed to be fixed.

E.2 Conductance

If a simple DC model is used for the transistor switch that only contains the channel conductance (R_{ds} is set to zero) then

$$g_{d0} = \frac{W_{eff}}{L_{eff}} \mu_{eff} C'_{ox} (V_{GS} - V_{TH})$$
(E.1)

when the DC source drain voltage is zero.

If the drain and source resistance is included then

$$g_d = \frac{g_{d0}}{1 + R_{ds}g_{d0}}$$
(E.2)

which is derived from

$$I_{DS} = \frac{I_{dslin0}}{1 + \frac{R_{ds}I_{dslin0}}{V_{DS}}}$$
(E.3)

where

$$I_{dslin0} = \frac{\frac{W_{eff}}{L_{eff}} \mu_{eff} C'_{os} \left(V_{GS} - V_{TH} - \frac{1}{2} A_{bulk} V_{DS} \right) V_{DS}}{1 + \frac{V_{DS}}{E_{sat} L_{eff}}}$$
(E.4)

E.2.1 Effective Transistor Width and Length

The effective transistor dimension are dependent on wint and lint and calculated as

$$W_{eff} = W_{draw} - 2$$
 wint
 $L_{eff} = L_{draw} - 2$ lint
(E.5)

E.2.2 Threshold Voltage

The threshold voltage is dependent on all the parameters: VTHO, tox, wint and lint. The equations given are those that are necessary for tracking the mismatch.

The threshold voltage is given by

$$V_{TH} = \text{VTH0} + k_1(\sqrt{phi - V_{BS}} - \sqrt{phi}) - k_2 V_{BS} - \Delta V_{TH} + V_1 + V_2 \quad (E.6)$$

with a direct dependency on VTH0 (threshold voltage with zero substrate bias), and where V_1 is dependent on lint, through L_{eff} , as

$$V_1 = k_1 \left(\sqrt{1 + \frac{NLX}{L_{eff}}} \sqrt{\frac{phi}{phi - V_{BS}}} - 1 \right) \sqrt{\phi}$$
(E.7)

 V_2 is dependent both on wint, through W_{eff} , and tox as

$$V_2 = \frac{k_3 \tan phi}{W_{eff} + w0} \tag{E.8}$$

while ΔV_{TH} is dependent on both lint and tox as

$$\Delta V_{TH} = (vbi - phi)dvt0 \left(e^{-\frac{dvt1L_{eff}}{2l_0}} + 2e^{-\frac{dvt1L_{eff}}{l_0}} \right)$$
(E.9)

where

$$l_0 = \sqrt{\frac{\varepsilon_{si} X_{dep}}{\varepsilon_{ox}}} \text{tox}$$
(E.10)

E.2.3 Effective Electron Mobility

The electron mobility is dependent on VTHO, wint and lint, through V_{TH} , and tox as

$$U_{vert} = 1 + ua \frac{V_{GS} + V_{TH}}{tox} + ub \left(\frac{V_{GS} + V_{TH}}{tox}\right)^2 + uc V_{BS}$$
(E.11)

$$\mu_{eff} = \frac{u0}{U_{vert}} \tag{E.12}$$

E.2.4 Oxide Capacitance

The oxide capacitance is only dependent on tox as

$$C'_{ox} = \frac{\varepsilon_{ox} \cdot \varepsilon_0}{\text{tox}}$$
 (E.13)

E.2.5 Effect of Drain and Source Resistance

The drain source resistance factor is dependent on wint, through W_{eff} , as

$$R_{ds} = \frac{rdsw}{W_{eff}} \tag{E.14}$$

E Conductance Model

Appendix F

Additional Simulation Results

If nothing else is stated, the LO signal is a sin-wave and IF=100MHz. The worst case image rejection ratio is defined by equation 3.50 on page 65.

Width (µm)	1	2	5	10	20
$\overline{g_{d0}}$ (mS)	0.441	0.868	2.15	4.23	8.56
σ_{gd0} (µS)	31.7	62.0	153	305	610
$\sigma_{gd0}^{/}\overline{g_{d0}^{'}}$ (%)	7.2	7.1	7.1	7.1	7.1
\overline{g}_d (mS)	0.348	0.684	1.69	3.38	6.75
$σ_{gd}$ (μS)	19.8	38.4	94.7	189	377
$\sigma_{gd}^{/}\overline{g_d} (\%)$	5.7	5.6	5.6	5.6	5.6

Table F.1: Channel conductance according to Matlab.

Table F.2: Channel conductance according to Caden	ce.
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Width (µm)	1	2	5	10	20
$\overline{g_d}$ (mS)	0.284	0.562	1.39	2.78	5.55
$σ_{gd}$ (μS)	8.38	16.2	40.0	79.9	160
$\sigma_{gd}^{/}\overline{g_d}$ (%)	3.0	2.9	2.9	2.9	2.9

Image Rejection (dB)		Capacitive load (fF)					
		25	50	125	250	500	
	1	46.4	42.6	36.7	33.4	31.8	
	2	48.5	46.6	41.4	36.9	33.6	
Width (µm)	5	50.6	48.9	46.6	42.8	38.2	
	10	53.3	50.6	48.40	46.5	42.8	
	20	55.3	53.4	49.8	48.4	46.5	

 Table F.3: Cadence transient simulation of worst case image rejection.

Table F.4: Cadence AC simulation of worst case image rejection
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Image Rejection (dB)		Capacitive load (fF)					
		25	50	125	250	500	
	1	47.4	42.1	35.4	31.8	30.1	
	2	52.6	47.6	40.6	35.7	32.2	
Width (µm)	5	58.4	54.2	47.6	42.3	37.2	
	10	61.7	58.4	52.7	47.6	42.3	
	20	64.0	61.7	57.2	52.7	47.6	

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Table E.5:	Matlah	simulation	of worst	case image	rejection
Iubic I.c.	manuo	Simulation	or worst	cuse muge	rejection.

Image Rejection (dB)		Capacitive load (fF)					
		25fF	50fF	125fF	250fF	500fF	
	1µm	48.6	42.8	35.8	32.1	30.3	
Width (µm)	2μm	54.5	48.6	40.9	35.7	32.1	
	5μm	62.4	56.4	48.5	42.6	37.2	
	10µm	68.4	62.4	54.4	48.5	42.6	
	20µm	74.4	68.4	60.4	54.4	48.5	

Table F.6: The scalability of IF for a capacitive load.

Image Rejection (dB)		Tran	sient	AC		
		IF=100MHz	IF=10MHz	IF=100MHz	IF=10MHz	
	1µm	42.6	43.8	42.1	42.6	
Width	5μm	48.9	54.0	54.2	53.1	
	20µm	53.4	56.7	61.7	62.0	

 Table F.7: Image Rejection for various LO signals.

Image	Rejection	Width		
(dB)		1µm	20µm	
	sine-wave	42.6	53.4	
LO	2-tone	42.9	56.9	
	Sqr-wave	43.2	62.6	
AC		42.1	61.7	

 Table F.8: Cadence transient simulation of the gain.

Gain		Capacitive load (fF)					
		25	50	125	250	500	
	1	0.738	0.724	0.637	0.475	0.285	
	2	0.736	0.738	0.713	0.636	0.473	
Width (µm)	5	0.720	0.734	0.739	0.725	0.670	
	10	0.701	0.720	0.737	0.739	0.725	
	20	0.685	0.701	0.725	0.737	0.739	

	ain	Width		
Gam		1µm	20µm	
LO	sine-wave	0.724	0.701	
	2-tone	0.669	0.667	
	Sqr-wave	0.619	0.636	

 Table F.9: Gain for various LO signals.

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