CHAPTER 8

INTEGRATED-CIRCUIT LOGIC FAMILIES

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OBJECTIVES

Upon completion of this chapter, you will be able to:

- Read and understand digital IC terminology as specified in manufacturers' data sheets.
- Compare the characteristics of standard TTL and the various TTL series.
- Determine the fan-out for a particular logic device.
- Use logic devices with open-collector outputs.
- Analyze circuits containing tristate devices.
- Compare the characteristics of the various CMOS series.
- Analyze circuits that use a CMOS bilateral switch to allow a digital system to control analog signals.
- Describe the major characteristics of and differences among TTL, ECL, MOS, and CMOS logic families.
- Cite and implement the various considerations that are required when interfacing digital circuits from different logic families.
- Use voltage comparators to allow a digital system to be controlled by analog signals.
- Use a logic pulser and a logic probe as digital circuit troubleshooting tools.

INTRODUCTION

As we described in Chapter 4, digital IC technology has advanced rapidly from small-scale integration (SSI), with fewer than 12 gates per chip; through medium-scale integration (MSI), with 12 to 99 equivalent gates per chip; on to large-scale and very large scale integration (LSI and VLSI, respectively), which can have tens of thousands of gates per chip; and, most recently, to ultra-large-scale integration (ULSI), with over 100,000 gates per chip, and giga-scale integration (GSI), with 1 million or more gates.

Most of the reasons that modern digital systems use integrated circuits are obvious. ICs pack a lot more circuitry in a small package, so that the overall size of almost any digital system is reduced. The cost is dramatically reduced because of the economies of mass-producing large volumes of similar devices. Some of the other advantages are not so apparent.

ICs have made digital systems more reliable by reducing the number of external interconnections from one device to another. Before we had ICs, every circuit connection was from one discrete component (transistor, diode, resistor, etc.) to another. Now most of the connections are internal to the ICs, where they are protected from poor soldering, breaks or shorts in connecting paths on a circuit board, and other physical problems. ICs have also drastically reduced the amount of electrical power needed to perform a given function because their miniature circuitry typically requires less power than their discrete counterparts. In addition to the savings in powersupply costs, this reduction in power has also meant that a system does not require as much cooling.

There are some things that ICs cannot do. They cannot handle very large currents or voltages because the heat generated in such small spaces would cause temperatures to rise beyond acceptable limits. In addition, ICs cannot easily implement certain electrical devices such as inductors, transformers, and large capacitors. For these reasons, ICs are principally used to perform low-power circuit operations that are commonly called *information processing*. The operations that require high power levels or devices that cannot be integrated are still handled by discrete components.

With the widespread use of ICs comes the necessity to know and understand the electrical characteristics of the most common IC logic families. Remember that the various logic families differ in the major components that they use in their circuitry. TTL and ECL use *bipolar* transistors as their major circuit element; PMOS, NMOS, and CMOS use unipolar *MOSFET* transistors as their principal component. In this chapter, we will present the important characteristics of each of these IC families and their subfamilies. The most important point is understanding the nature of the input circuitry and output circuitry for each logic family. Once these are understood, you will be much better prepared to do analysis, troubleshooting, and some design of digital circuits that contain any combination of IC families. We will study the inner workings of devices in each family with the simplest circuitry that conveys the critical characteristics of all members of the family.

8-1 DIGITAL IC TERMINOLOGY

Although there are many digital IC manufacturers, much of the nomenclature and terminology is fairly standardized. The most useful terms are defined and discussed below.

Current and Voltage Parameters (See Figure 8-1)

- V_{IH}(min)—High-Level Input Voltage. The minimum voltage level required for a logical 1 at an *input*. Any voltage below this level will not be accepted as a HIGH by the logic circuit.
- *V*_{IL}(max)—Low-Level Input Voltage. The maximum voltage level required for a logic 0 at an *input*. Any voltage above this level will not be accepted as a LOW by the logic circuit.
- *V*_{OH}(min)—High-Level Output Voltage. The minimum voltage level at a logic circuit *output* in the logical 1 state under defined load conditions.
- *V*_{0L}(max)—Low-Level Output Voltage. The maximum voltage level at a logic circuit *output* in the logical 0 state under defined load conditions.
- *I*_{IH}—High-Level Input Current. The current that flows into an input when a specified high-level voltage is applied to that input.
- *I*_{IL}—Low-Level Input Current. The current that flows into an input when a specified low-level voltage is applied to that input.
- I_{OH}—High-Level Output Current. The current that flows from an output in the logical 1 state under specified load conditions.

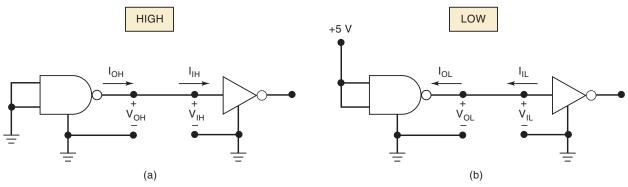


FIGURE 8-1 Currents and voltages in the two logic states.

*I*_{OL}—Low-Level Output Current. The current that flows from an output in the logical 0 state under specified load conditions.

Note: The actual current directions may be opposite to those shown in Figure 8-1, depending on the logic family. All descriptions of current flow in this text refer to conventional current flow (from higher potential to lower potential). In keeping with the conventions of most data books, current flowing into a node or device is considered positive, and current flowing out of a node or device is considered negative.

Fan-Out

In general, a logic-circuit output is required to drive several logic inputs. Sometimes all ICs in the digital system are from the same logic family, but many systems have a mix of various logic families. The **fan-out** (also called *loading factor*) is defined as the *maximum* number of logic inputs that an output can drive reliably. For example, a logic gate that is specified to have a fan-out of 10 can drive 10 logic inputs. If this number is exceeded, the output logic-level voltages cannot be guaranteed. Obviously, fan-out depends on the nature of the input devices that are connected to an output. Unless a different logic family is specified as the load device, fan-out is assumed to refer to load devices of the same family as the driving output.

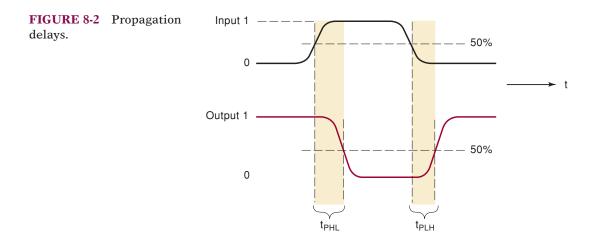
Propagation Delays

A logic signal always experiences a delay in going through a circuit. The two propagation delay times are defined as follows:

- *t*_{PLH}. Delay time in going from logical 0 to logical 1 state (LOW to HIGH)
- *t*_{PHL}. Delay time in going from logical 1 to logical 0 state (HIGH to LOW)

Figure 8-2 illustrates these propagation delays for an INVERTER. Note that $t_{\rm PHL}$ is the delay in the output's response as it goes from HIGH to LOW. It is measured between the 50 percent points on the input and output transitions. The $t_{\rm PLH}$ value is the delay in the output's response as it goes from LOW to HIGH.

In some logic circuits, t_{PHL} and t_{PLH} are not the same value, and both will vary depending on capacitive loading conditions. The values of propagation times are used as a measure of the relative speed of logic circuits. For example, a logic circuit with values of 10 ns is a faster logic circuit than one with values of 20 ns under specified load conditions.



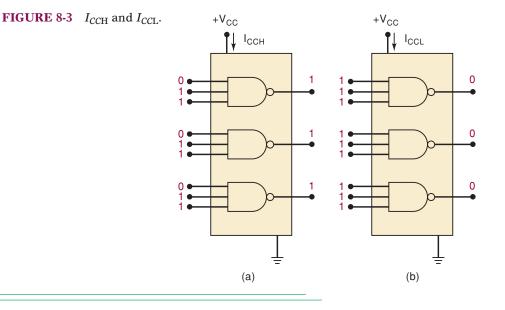
Power Requirements

Every IC requires a certain amount of electrical power to operate. This power is supplied by one or more power-supply voltages connected to the power pin(s) on the chip labeled V_{CC} (for TTL) or V_{DD} (for MOS devices).

The amount of power that an IC requires is determined by the current, I_{CC} (or I_{DD}), that it draws from the V_{CC} (or V_{DD}) supply, and the actual power is the product $I_{CC} \times V_{CC}$. For many ICs, the current drawn from the supply varies depending on the logic states of the circuits on the chip. For example, Figure 8-3(a) shows a NAND chip where *all* of the gate *outputs* are HIGH. The current drain on the V_{CC} supply for this case is called I_{CCH} . Likewise, Figure 8-3(b) shows the current when *all* of the gate *outputs* are LOW. This current is called I_{CCL} . The values are always measured with the outputs open circuit (no load) because the size of the load will also have an effect on I_{CCH} .

In some logic circuits, I_{CCH} and I_{CCL} will be different values. For these devices, the average current is computed based on the assumption that gate outputs are LOW half the time and HIGH half the time.

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$



This equation can be rewritten to calculate average power dissipated:

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$

Noise Immunity

Stray electric and magnetic fields can induce voltages on the connecting wires between logic circuits. These unwanted, spurious signals are called *noise* and can sometimes cause the voltage at the input to a logic circuit to drop below $V_{\rm IH}(\rm min)$ or rise above $V_{\rm IL}(\rm max)$, which could produce unpredictable operation. The **noise immunity** of a logic circuit refers to the circuit's ability to tolerate noise without causing spurious changes in the output voltage. A quantitative measure of noise immunity is called **noise margin** and is illustrated in Figure 8-4.

Figure 8-4(a) is a diagram showing the range of voltages that can occur at a logic-circuit output. Any voltages greater than $V_{OH}(min)$ are considered a logic 1, and any voltages lower than $V_{OL}(max)$ are considered a logic 0. Voltages in the indeterminate range should not appear at a logic circuit output under normal conditions. Figure 8-4(b) shows the voltage requirements at a logic circuit input. The logic circuit responds to any input greater than $V_{IH}(min)$ as a logic 1, and it responds to voltages lower than $V_{IL}(max)$ as a logic 0. Voltages in the indeterminate range produce an unpredictable response and should not be used.

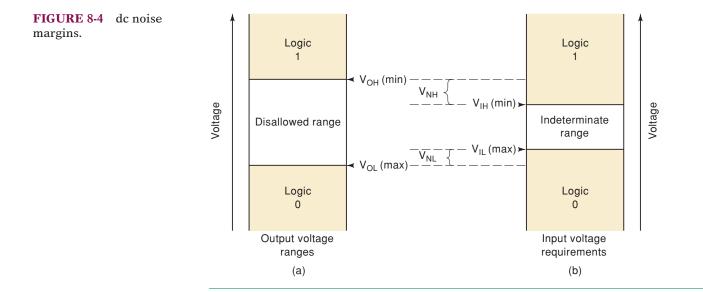
The *high-state noise margin* $V_{\rm NH}$ is defined as

$$V_{\rm NH} = V_{\rm OH}(\rm min) - V_{\rm IH}(\rm min)$$
(8-1)

and is illustrated in Figure 8-4. $V_{\rm NH}$ is the difference between the lowest possible HIGH output and the minimum input voltage required for a HIGH. When a HIGH logic output is driving a logic-circuit input, any negative noise spikes greater than $V_{\rm NH}$ appearing on the signal line can cause the voltage to drop into the indeterminate range, where unpredictable operation can occur.

The *low-state noise margin* $V_{\rm NL}$ is defined as

$$V_{\rm NL} = V_{\rm IL}(\rm max) - V_{\rm OL}(\rm max)$$
(8-2)



and it is the difference between the largest possible LOW output and the maximum input voltage required for a LOW. When a LOW logic output is driving a logic input, any positive noise spikes greater than $V_{\rm NL}$ can cause the voltage to rise into the indeterminate range.

EXAMPLE 8-1

The input/output voltage specifications for the standard TTL family are listed in Table 8-1. Use these values to determine the following.

- (a) The maximum-amplitude noise spike that can be tolerated when a HIGH output is driving an input.
- (b) The maximum-amplitude noise spike that can be tolerated when a LOW output is driving an input.

Parameter	Min (V)	Typical (V)	Max (V)
V _{OH}	2.4	3.4	
V _{OL}		0.2	0.4
V_{IH}	2.0*		
V_{IL}			0.8 [*]

^{*}Normally only the minimum V_{IH} and maximum V_{IL} values are given.

Solution

TABLE 8-1

(a) When an output is HIGH, it may be as low as $V_{OH}(min) = 2.4$ V. The minimum voltage that an input responds to as a HIGH is $V_{IH}(min) = 2.0$ V. A negative noise spike can drive the actual voltage below 2.0 V if its amplitude is greater than

$$V_{\rm NH} = V_{\rm OH}({\rm min}) - V_{\rm IH}({\rm min})$$

= 2.4 V - 2.0 V = 0.4 V

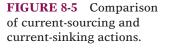
(b) When an output is LOW, it may be as high as $V_{OL}(max) = 0.4$ V. The maximum voltage that an input responds to as a LOW is $V_{IL}(max) = 0.8$ V. A positive noise spike can drive the actual voltage above the 0.8-V level if its amplitude is greater than

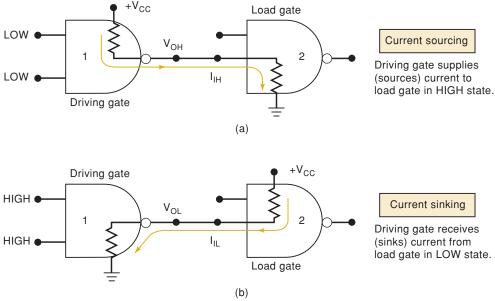
$$V_{\rm NL} = V_{\rm IL}({
m max}) - V_{\rm OL}({
m max})$$

= 0.8 V - 0.4 V = 0.4 V

Invalid Voltage Levels

For proper operation the input voltage levels to a logic circuit must be kept outside the indeterminate range shown in Figure 8-4(b); that is, they must be either lower than $V_{\rm IL}(\max)$ or higher than $V_{\rm IH}(\min)$. For the standard TTL specifications given in Example 8-1, this means that the input voltage must be less than 0.8 V or greater than 2.0 V. An input voltage between 0.8 and 2.0 V is considered an *invalid* voltage that will produce an unpredictable output response, and so must be avoided. In normal operation, a logic input voltage will not fall into the invalid region because it comes from a logic output that is within the stated specifications. However, when this logic output is malfunctioning or is being overloaded (i.e., its fan-out is being exceeded), then its voltage may be in





the invalid region. Invalid voltage levels in a digital circuit can also be caused by power-supply voltages that are outside the acceptable range. It is important to know the valid voltage ranges for the logic family being used so that invalid conditions can be recognized when testing or troubleshooting.

Current-Sourcing and Current-Sinking Action

Logic families can be described according to how current flows between the output of one logic circuit and the input of another. Figure 8-5(a) illustrates **current-sourcing** action. When the output of gate 1 is in the HIGH state, it supplies a current I_{IH} to the input of gate 2, which acts essentially as a resistance to ground. Thus, the output of gate 1 is acting as a *source* of current for the gate 2 input. We can think of it as being like a faucet that acts as a *source* of water.

Current-sinking action is illustrated in Figure 8-5(b). Here the input circuitry of gate 2 is represented as a resistance tied to $+V_{CC}$, the positive terminal of a power supply. When the gate 1 output goes to its LOW state, current will flow in the direction shown from the input circuit of gate 2 back through the output resistance of gate 1 to ground. In other words, in the LOW state, the circuit output that drives the input of gate 2 must be able to *sink* a current, $I_{\rm IL}$, coming from that input. We can think of this as acting like a *sink* into which water is flowing.

The distinction between current sourcing and current sinking is an important one, which will become more apparent as we examine the various logic families.

IC Packages

Developments and advancements in integrated circuits continue at a rapid pace. The same is true of IC packaging. There are various types of packages, which differ in physical size, the environmental and power-consumption conditions under which the device can be operated reliably, and the way in which the IC package is mounted to the circuit board. Figure 8-6 shows five representative IC packages.

The package in Figure 8-6(a) is the **DIP** (dual-in-line package), which has been around for a long time. Its pins (or leads) run down the two long sides of the rectangular package. The device shown is a 24-pin DIP. Note the presence

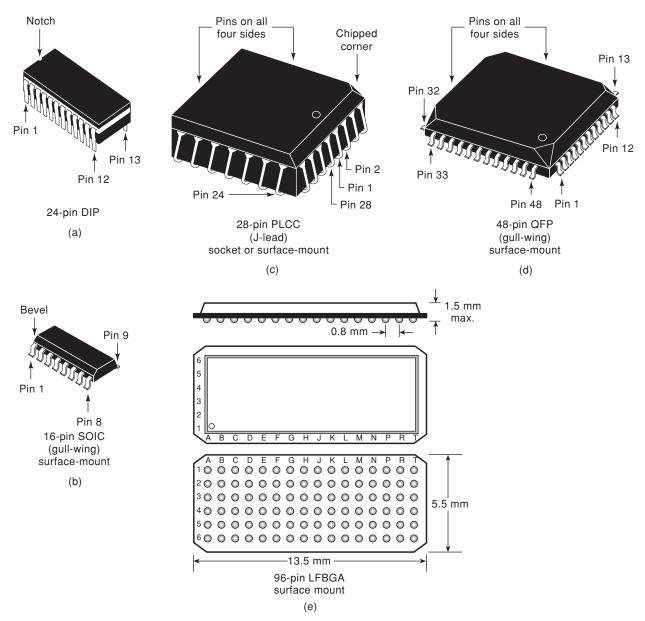


FIGURE 8-6 Common IC packages. (Courtesy of Texas Instruments)

of the notch on one end, which is used to locate pin 1. Some DIPs use a small dot on the top surface of the package to locate pin 1. The leads extend straight out of the DIP package so that the IC can be plugged into an IC socket or inserted into holes drilled through a printed circuit board. The spacing between pins (lead pitch) is typically 100 mils (a mil is a thousandth of an inch). DIP packages are still the most popular package for prototyping, breadboarding, and educational experimentation.

Nearly all new circuit boards that are produced using automated manufacturing equipment have moved away from using DIP packages whose leads are inserted through holes in the board. New manufacturing methods use **surfacemount technology**, which places an IC onto conductive pads on the surface of the board. They are held in place by a solder paste, and the entire board is heated to create a soldered connection. The precision of the placement machine allows for very tight lead spacing. The leads on these surface-mount packages are bent out from the plastic case, providing adequate surface area

Abbreviation	Package Name	Height	Lead Pitch
DIP	Dual-in-line package	200 mils (5.1 mm)	100 mils (2.54 mm)
SOIC	Small outline integrated circuit	2.65 mm	50 mils (1.27 mm)
SSOP	Shrink small outline package	2.0 mm	0.65 mm
TSSOP	Thin shrink small outline package	1.1 mm	0.65 mm
TVSOP	Thin very small outline package	1.2 mm	0.4 mm
PLCC	Plastic leaded chip carrier	4.5 mm	1.27 mm
QFP	Quad flat pack	4.5 mm	0.635 mm
TQFP	Thin quad flat pack	1.6 mm	0.5 mm
LFBGA	Low-profile fine-pitch ball grid array	1.5 mm	0.8 mm

TABLE 8-2	IC packages.
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for the solder joint. The shape of these leads has resulted in the nickname of "gull-wing" package. Many different packages are available for surface-mount devices. Some of the most common packages used for logic ICs are shown in Figure 8-6. Table 8-2 gives the definition of each abbreviation along with its dimensions.

The need for more and more connections to a complex IC has resulted in another very popular package that has pins on all four sides of the chip. The PLCC has J-shaped leads that curl under the IC, as shown in Figure 8-6(c). These devices can be surface-mounted to a circuit board but can also be placed in a special PLCC socket. This is commonly used for components that are likely to need to be replaced for repair or upgrade, such as programmable logic devices or central processing units in computers. The QFP and TQFP packages have pins on all four sides in a gull-wing surface-mount package, as shown in Figure 8-6(d). The ball grid array (BGA) shown in Figure 8-6(e) is a surface-mount package that offers even more density. The pin grid array (PGA) is a similar package that is used when components must be in a socket to allow easy removal. The PGA has a long pin instead of a contact ball (BGA) at each position in the grid.

The proliferation of small, handheld consumer equipment such as digital video cameras, cellular phones, computers (PDAs), portable audio systems, and other devices has created a need for logic circuits in very small packages. Logic gates are now available in individual surface-mount packages containing one, two, or three gates (1G, 2G, 3G, respectively). These devices may have as few as five or six pins (power, ground, two to three inputs, and an output) and take up less space than an individual letter on this page.

REVIEW QUESTIONS

- 1. Define each of the following: V_{OH} , V_{IL} , I_{OL} , I_{IH} , t_{PLH} , t_{PHL} , I_{CCL} , I_{CCH} .
- 2. True or false: If a logic circuit has a fan-out of 5, the circuit has five outputs.
- 3. *True or false:* The HIGH-stage noise margin is the difference between $V_{\text{IH}}(\text{min})$ and V_{CC} .
- 4. Describe the difference between current sinking and current sourcing.
- 5. Which IC package can be plugged into sockets?
- 6. Which package has leads bent under the IC?
- 7. How do surface-mount packages differ from DIPs?
- 8. Will a standard TTL device work with an input level of 1.7 V?

THE TTL LOGIC FAMILY 8-2

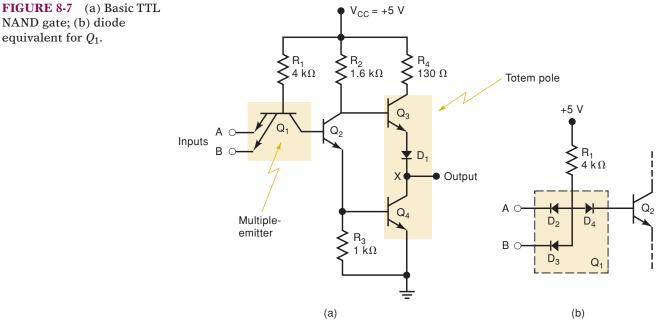
At this writing, many small- to medium-scale ICs (SSI and MSI) can still be obtained in the standard **TTL** technology series that has been available for over 30 years. This original series of devices and their descendants in the TTL family have had a tremendous influence on the characteristics of all logic devices today. TTL devices are still used as "glue" logic that connects the more complex devices in digital systems. They are also used as interface circuits to devices that require high current drive. Even though the bipolar TTL family as a whole is on the decline, we will begin our discussion of logic ICs with the devices that shaped digital technology.

The basic TTL logic circuit is the NAND gate, shown in Figure 8-7(a). Even though the standard TTL family is nearly obsolete, we can learn a great deal about the more current family members by studying the original circuitry in its simplest form. The characteristics of TTL inputs come from the multiple-emitter (diode junction) configuration of transistor Q_1 . Forward biasing either (or both) of these diode junctions will turn on Q_1 . Only when all junctions are reverse biased will the transistor be off. This multiple-emitter input transistor can have up to eight emitters for an eight-input NAND gate.

Also note that on the output side of the circuit, transistors Q_3 and Q_4 are in a totem-pole arrangement. The totem pole is made up of two transistor switches, Q_3 and Q_4 . The job of Q_3 is to connect V_{CC} to the output, making a logic HIGH. The job of Q_4 is to connect the output to ground, making a logic LOW. As we will see shortly, in normal operation, either Q_3 or Q_4 will be conducting, depending on the logic state of the output.

Circuit Operation—LOW State

Although this circuit looks extremely complex, we can simplify its analysis somewhat by using the diode equivalent of the multiple-emitter transistor Q_1 , as shown in Figure 8-7(b). Diodes D_2 and D_3 represent the two E–B junctions of Q_1 , and D_4 is the collector-base (C-B) junction. In the following analysis, we will use this representation for Q_1 .



NAND gate; (b) diode equivalent for Q_1 .

First, let's consider the case where the output is LOW. Figure 8-8(a) shows this situation with inputs A and B both at +5 V. The +5 V at the cathodes of D_2 and D_3 will turn these diodes off, and they will conduct almost no current. The +5 V supply will push current through R_1 and D_4 into the base of Q_2 , which turns on. Current from Q_2 's emitter will flow into the base of Q_4 and turn Q_4 on. At the same time, the flow of Q_2 collector current produces a voltage drop across R_2 that reduces Q_2 's collector voltage to a low value that is insufficient to turn Q_3 on.

The voltage at Q_2 's collector is shown as approximately 0.8 V. This is because Q_2 's emitter is at 0.7 V relative to ground due to Q_4 's E–B forward voltage,

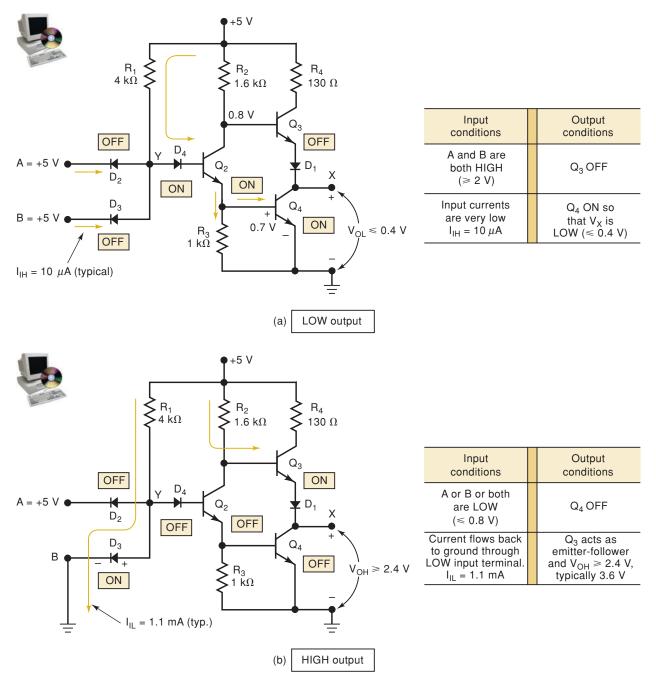


FIGURE 8-8 TTL NAND gate in its two output states.

and Q_2 's collector is at 0.1 V relative to its emitter due to $V_{CE}(\text{sat})$. This 0.8 V at Q_3 's base is not enough to forward-bias both Q_3 's E–B junction and diode D_1 . In fact, D_1 is needed to keep Q_3 off in this situation.

With Q_4 on, the output terminal, X, will be at a very low voltage because Q_4 's ON-state resistance will be low (1 to 25 Ω). Actually, the output voltage, V_{OL} , will depend on how much collector current Q_4 conducts. With Q_3 off, there is no current coming from the +5 V terminal through R_4 . As we shall see, Q_4 's collector current will come from the TTL inputs that terminal X is connected to.

It is important to note that the HIGH inputs at *A* and *B* will have to supply only a very small diode leakage current. Typically, this current I_{IH} is only around 10 μ A at room temperature.

Circuit Operation—HIGH State

Figure 8-8(b) shows the situation where the circuit output is HIGH. This situation can be produced by connecting either or both inputs LOW. Here, input B is connected to ground. This will forward-bias D_3 so that current will flow from the +5 V source terminal, through R_1 and D_3 , and through terminal B to ground. The forward voltage across D_3 will hold point Y at approximately 0.7 V. This voltage is not enough to forward-bias D_4 and the E–B junction of Q_2 sufficiently for conduction.

With Q_2 off, there is no base current for Q_4 , and it turns off. Because there is no Q_2 collector current, the voltage at Q_3 's base will be large enough to forward-bias Q_3 and D_1 , so that Q_3 will conduct. Actually, Q_3 acts as an emitter follower because output terminal X is essentially at its emitter. With no load connected from point X to ground, V_{OH} will be around 3.4 to 3.8 V because two 0.7-V diode drops (E–B of Q_3 , and D_1) subtract from the 5 V applied to Q_3 's base. This voltage will decrease under load because the load will draw emitter current from Q_3 , which draws base current through R_2 , thereby increasing the voltage drop across R_2 .

It's important to note that there is a substantial current flowing back through input terminal *B* to ground when *B* is held LOW. This current, I_{IL} , is determined by the value of resistor R_1 , which will vary from series to series. For standard TTL, it is about 1.1 mA. The LOW *B* input acts as a *sink* to ground for this current.

Current-Sinking Action

A TTL output acts as a current sink in the LOW state because it *receives* current from the input of the gate that it is driving. Figure 8-9 shows one TTL gate driving the input of another gate (the load) for both output voltage states. In the output LOW state situation depicted in Figure 8-9(a), transistor Q_4 of the driving gate is on and essentially "shorts" point X to ground. This LOW voltage at X forward-biases the emitter–base junction of Q_1 , and current flows, as shown, back through Q_4 . Thus, Q_4 is performing a current-sinking action that derives its current from the input current ($I_{\rm IL}$) of the load gate. We will often refer to Q_4 as the **current-sinking transistor** or as the **pull-down transistor** because it brings the output voltage down to its LOW state.

Current-Sourcing Action

A TTL output acts as a current source in the HIGH state. This is shown in Figure 8-9(b), where transistor Q_3 is supplying the input current, I_{IH} , required by the Q_1 transistor of the load gate. As stated above, this current is a

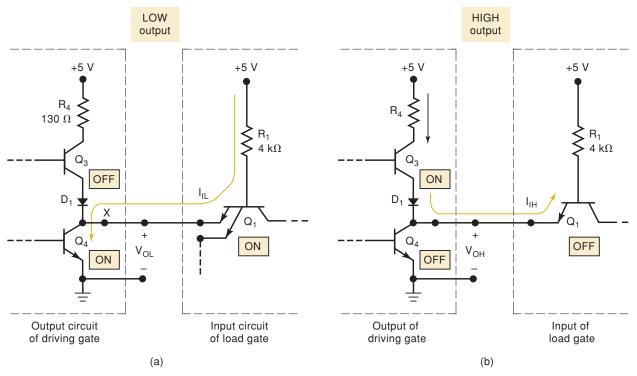


FIGURE 8-9 (a) When the TTL output is in the LOW state, Q_4 acts as a current sink, deriving its current from the load. (b) In the output HIGH state, Q_3 acts as a current source, providing current to the load gate.

small reverse-bias leakage current (typically 10 μ A). We will often refer to Q_3 as the **current-sourcing transistor** or **pull-up transistor**. In some of the more modern TTL series, the pull-up circuit is made up of two transistors, rather than a transistor and diode.

Totem-Pole Output Circuit

Several points should be mentioned concerning the totem-pole arrangement of the TTL output circuit, as shown in Figure 8-9, because it is not readily apparent why it is used. The same logic can be accomplished by eliminating Q_3 and D_1 and connecting the bottom of R_4 to the collector of Q_4 . But this arrangement would mean that Q_4 would conduct a fairly heavy current in its saturation state (5 V/130 $\Omega \approx 40$ mA). With Q_3 in the circuit, there will be no current through R_4 in the output LOW state. This is important because it keeps the circuit power dissipation down.

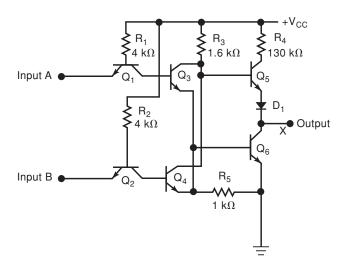
Another advantage of this arrangement occurs in the output HIGH state. Here Q_3 is acting as an emitter follower with its associated low output impedance (typically 10 Ω). This low output impedance provides a short time constant for charging up any capacitive load on the output. This action (commonly called *active pull-up*) provides very fast rise-time waveforms at TTL outputs.

A disadvantage of the totem-pole output arrangement occurs during the transition from LOW to HIGH. Unfortunately, Q_4 turns off more slowly than Q_3 turns on, and so there is a period of a few nanoseconds during which both transistors are conducting and a relatively large current (30 to 40 mA) will be drawn from the 5-V supply. This can present a problem that will be examined later.

FIGURE 8-10 TTL NOR

gate circuit.





TTL NOR Gate

Figure 8-10 shows the internal circuit for a TTL NOR gate. We will not go through a detailed analysis of this circuit, but it is important to note how it compares to the NAND circuit of Figure 8-8. On the input side, we can see that the NOR circuit *does not use a multiple-emitter* transistor; instead, each input is applied to the emitter of a separate transistor. On the output side, the NOR circuit uses the same totem-pole arrangement as the NAND circuit.

Summary

All TTL circuits have a similar structure. NAND and AND gates use multipleemitter transistor or multiple diode junction inputs; NOR and OR gates use separate input transistors. In either case, the input will be the cathode (N-region) of a P–N junction, so that a HIGH input voltage will turn off the junction and only a small leakage current ($I_{\rm IH}$) will flow. Conversely, a LOW input voltage turns on the junction, and a relatively large current ($I_{\rm IL}$) will flow back through the signal source. Most, but not all, TTL circuits will have some type of totem-pole output configuration. There are some exceptions that will be discussed later.

REVIEW QUESTIONS

- 1. True or false: A TTL output acts as a current sink in the LOW state.
- 2. In which TTL input state does the largest amount of input current flow?
- 3. State the advantages and disadvantages of a totem-pole output.
- 4. Which TTL transistor is the pull-up transistor in the NAND circuit?
- 5. Which TTL transistor is the pull-down transistor in the NOR circuit?
- 6. How does the TTL NOR circuit differ from the NAND circuit?

8-3 TTL DATA SHEETS

In 1964, Texas Instruments Corporation introduced the first line of standard TTL ICs. The 54/74 series, as it is called, has been one of the most widely used IC logic families. We will simply refer to it as the 74 series because the major difference between the 54 and 74 versions is that devices in the 54 series can operate over a wider range of temperatures and power-supply voltages. Many semiconductor manufacturers still produce TTL ICs. Fortunately, they all use

the same numbering system, so that the basic IC number is the same from one manufacturer to another. Each manufacturer, however, usually attaches its own special prefix to the IC number. For example, Texas Instruments uses the prefix SN, National Semiconductor uses DM, and Signetics uses S. Thus, depending on the manufacturer, you may see a quad NOR gate chip labeled as a DM7402, SN7402, S7402, or some other similar designation. The important part is the number 7402, which is the same for all manufacturers.

As we learned in Chapter 4, there are several series in the TTL family of logic devices (74, 74LS, 74S, etc.). The original standard series and its immediate descendants (74, 74LS, 74S) are no longer recommended by the manufacturers for use in new designs. In spite of this, enough demand in the market keeps them in production. An understanding of the characteristics that define the capabilities and limitations of any logic device is vital. This section will define those characteristics using the advanced low-power Schottky (ALS) series and help you understand a typical data sheet. Later we introduce the other TTL series and compare their characteristics.

We can find all of the information we need on any IC by consulting the manufacturer's published data sheets for that particular IC family. These data sheets can be obtained from data books, CD ROMs, or the IC manufacturer's Internet web site. Figure 8-11 is the manufacturer's data sheet for the 74ALS00 NAND gate IC showing the recommended operating conditions, electrical characteristics, and switching characteristics. Most of the quantities discussed in the following paragraphs in this section can be found on this data sheet. As we discuss each quantity, you should refer to this data sheet to see where the information came from.

Supply Voltage and Temperature Range

Both the 74ALS series and the 54ALS series use a nominal supply voltage (V_{CC}) of 5 V, but can tolerate a supply variation of 4.5 to 5.5 V. The 74ALS series is designed to operate properly in ambient temperatures ranging from 0 to 70°C, while the 54ALS series can handle -55 to +125°C. Because of its greater tolerance of voltage and temperature variations, the 54ALS series is more expensive. It is employed only in applications where reliable operation must be maintained over an extreme range of conditions. Examples are military and space applications.

Voltage Levels

The input and output logic voltage levels for the 74ALS series can be found on the data sheet of Figure 8-11. Table 8-3 presents them in summary form. The minimum and maximum values shown are for worst-case conditions of power supply, temperature, and loading conditions. Inspection of the table reveals a guaranteed maximum logical 0 output $V_{\rm OL} = 0.5$ V, which is 300 mV less than the logical 0 voltage needed at the input $V_{\rm IL} = 0.8$ V. This means that the guaranteed LOW-state dc noise margin is 300 mV. That is,

$$V_{\rm NL} = V_{\rm IL}({\rm max}) - V_{\rm OL}({\rm max}) = 0.8 \,{\rm V} - 0.5 \,{\rm V} = 0.3 \,{\rm V} = 300 \,{\rm mV}$$

Similarly, the logical 1 output $V_{\rm OH}$ is a guaranteed minimum of 2.5 V, which is 500 mV greater than the logical 1 voltage needed at the input, $V_{\rm IH} = 2.0$ V. Thus, the HIGH-state dc noise margin is 500 mV.

$$V_{\rm NH} = V_{\rm OH}({\rm min}) - V_{\rm IH}({\rm min}) = 2.5 \,{\rm V} - 2.0 \,{\rm V} = 0.5 \,{\rm V} = 500 \,{\rm mV}$$

Thus, the guaranteed worst-case dc noise margin for the 74ALS series is 300 mV.

recommended operating conditions

		SN	SN54ALS00A		SN74ALS00A				
		MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
V _{II} Low-level input voltage			0.8‡			0.8			
VIL	Low-reventingut voltage			0.7§				ľ	
юн	High-level output current			-0.4			0.4	m∧	
IOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	÷С	

[‡] Applies over temperature range – 55°C to 70°C

§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range unless otherwise noted

PARAMETER	TEST CONDITIONS		SN54ALS	SN54ALS00A			A	
PARAMETER			MIN TYPT	MAX	MIN	түр†	MAX	UNIT
VIK	$V_{CC} = 4.5 V_{c}$	= −18 mA		-1.2			-1.5	V
VoH	V_{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} -2		Vcc -2			V
Vol	Vcc = 4.5 V	I _{OL} = 4 mA	0.25	0.4		0.25	0.4	v
VOL	VCC - 4.5 V	I _{OL} = 8 mA				0.35	0.5	v
Ц	V _{CC} = 5.5 V.	V ₁ = 7 V		0.1			0.1	mΑ
Чн	V _{CC} = 5.5 V,	V1 = 2.7 V		20			20	μA
t _{IL}	V _{CC} = 5.5 V,	VI = 0.4 V		-0.1			-0.1	mΑ
IO‡	$V_{CC} = 5.5 V_{c}$	V _O = 2.25 V	-20	-112	-30		- 112	mΑ
Іссн	V _{CC} = 5.5 V,	V ₁ = 0	0.5	0.85		0.5	0.85	mΑ
ICCL	V _{CC} = 5.5 V,	V∣ = 4.5 V	1.5	3		1.5	3	mΑ

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current. IOS.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	CL RL	V_{CC} = 4.5 V to 5.5 C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§			UNIT
			SN54A	LS00A	SN74A	LSOOA	
			MIN	MAX	MIN	MAX] [
^t PLH	A or B	V	3	15	3	11	
^t PHL	AUIB	Y	2	9	2	8	ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

FIGURE 8-11 Data sheet for the 74ALS00 NAND gate IC. (Courtesy of Texas Instruments)

TABLE 8-3 74ALS seriesvoltage levels.		Minimum	Typical	Maximum
	V_{OL}	_	0.35	0.5
	V _{OH}	2.5	3.4	—
	$V_{\rm IL}$	—	—	0.8
	$V_{\rm IH}$	2.0	—	—

Maximum Voltage Ratings

The voltage values in Table 8-3 *do not include* the absolute maximum ratings beyond which the useful life of the IC may be impaired. The absolute maximum operating conditions are generally given at the top of a data sheet (not shown in Figure 8-11). The voltages applied to any input of this series IC

must never exceed +7.0 V. A voltage greater than +7.0 V applied to an input emitter can cause reverse breakdown of the E–B junction of Q_1 .

There is also a limit on the maximum *negative* voltage that can be applied to a TTL input. This limit, -0.5 V, is caused by the fact that most TTL circuits employ protective shunt diodes on each input. These diodes were purposely left out of our earlier analysis because they do not enter into the normal circuit operation. They are connected from each input to ground to limit the negative input voltage excursions that often occur when logic signals have excessive ringing. With these diodes, we should not apply more than -0.5 V to an input because the protective diodes would begin to conduct and draw substantial current, probably causing the diode to short out, resulting in a permanently faulty input.

Power Dissipation

An ALS TTL NAND gate draws an average power of 2.4 mW. This is a result of $I_{CCH} = 0.85$ mA and $I_{CCL} = 3$ mA, which produces $I_{CC}(avg) = 1.93$ mA and $P_D(avg) = 1.93$ mA × 5 V = 9.65 mW. This 9.65 mW is the total power required by all four gates on the chip. Thus, one NAND gate requires an average power of 2.4 mW.

Propagation Delays

The data sheet gives minimum and maximum propagation delays. Assuming the typical value is midway between gives a $t_{PLH} = 7$ ns and $t_{PHL} = 5$ ns. The typical *average* propagation delay $t_{pd}(avg) = 6$ ns.

EXAMPLE 8-2

Refer to the data sheet for the 74ALS00 quad two-input NAND IC in Figure 8-11. Determine the *maximum* average power dissipation and the *maximum* average propagation delay of a *single* gate.

Solution

Look under the electrical characteristics for the maximum I_{CCH} and I_{CCL} values. The values are 0.85 mA and 3 mA, respectively. The average I_{CC} is therefore 1.9 mA. The average power is obtained by multiplying by V_{CC} . The data sheet indicates that these I_{CC} values were obtained when V_{CC} was at its maximum value (5.5 V for the 74ALS series). Thus, we have

 $P_{\rm D}({\rm avg}) = 1.9 \,{\rm mA} \times 5.5 \,{\rm V} = 10.45 \,{\rm mW}$

as the power drawn by the *complete* IC. We can determine the power drain of one NAND gate by dividing this by 4:

$$P_{\rm D}({\rm avg}) = 2.6 \,{\rm mW} \,{\rm per \,gate}$$

Because this average power drain was calculated using the maximum current and voltage values, it is the maximum average power that a 74ALS00 NAND gate will draw under worst-case conditions. Designers often use worst-case values to ensure that their circuits will work under all conditions.

The maximum propagation delays for a 74ALS00 NAND gate are listed as

$$t_{\rm PLH} = 11 \, \rm ns$$
 $t_{\rm PHL} = 8 \, \rm ns$

so that the maximum average propagation delay is

$$t_{\rm pd}(\rm avg) = \frac{11+8}{2} = 9.5 \, \rm ns$$

Again, this is a worst-case maximum possible average propagation delay.

8-4 TTL SERIES CHARACTERISTICS

The standard 74 series of TTL has evolved into several other series. All of them offer a wide variety of gates and flip-flops in the small-scale integration (SSI) line, and counters, registers, multiplexers, decoders/encoders, and other logic functions in their medium scale integration (MSI) line. The following TTL series—often called "subfamilies"—provide a wide range of speed and power capabilities.

Standard TTL, 74 Series

The original standard 74 series of TTL logic was described in Section 8-2. These devices are still readily available, but in most cases they are no longer a reasonable choice for new designs because other devices are now available that perform much better at a lower cost.

Schottky TTL, 74S Series

The 7400 series operates using saturated switching in which many of the transistors, when conducting, will be in the saturated condition. This operation causes a storage-time delay, t_S , when the transistors switch from ON to OFF, and it limits the circuit's switching speed.

The 74S series reduces this storage-time delay by not allowing the transistor to go as deeply into saturation. It accomplishes this by using a Schottky barrier diode (SBD) connected between the base and the collector of each transistor, as shown in Figure 8-12(a). The SBD has a forward voltage of only 0.25 V. Thus, when the C–B junction becomes forward-biased at the onset of saturation, the SBD will conduct and divert some of the input current away from the base. This reduces the excess base current and decreases the storage-time delay at turn-off.

As shown in Figure 8-12(a), the transistor/SBD combination is given a special symbol. This symbol is used for all of the transistors in the circuit diagram for the 74S00 NAND gate shown in Figure 8-12(b). This 74S00 NAND gate has an average propagation delay of only 3 ns, which is six times as fast as the 7400. Note the presence of shunt diodes D_1 and D_2 to limit negative input voltages.

Circuits in the 74S series also use smaller resistor values to help improve switching times. This increases the circuit average power dissipation to about 20 mW, about two times greater than the 74 series. The 74S circuits also use a Darlington pair (Q_3 and Q_4) to provide a shorter output rise time when switching from ON to OFF.

Low-Power Schottky TTL, 74LS Series (LS-TTL)

The 74LS series is a lower-powered, slower-speed version of the 74S series. It uses the Schottky-clamped transistor, but with larger resistor values than the 74S series. The larger resistor values reduce the circuit power requirement, but at the expense of an increase in switching times. A NAND gate in the

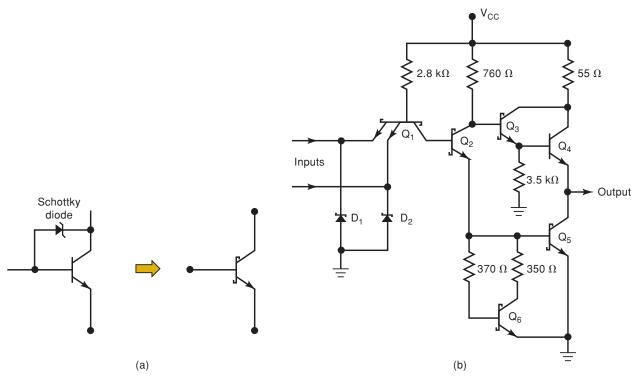


FIGURE 8-12 (a) Schottky-clamped transistor; (b) basic NAND gate in S-TTL series.

74LS series will typically have an average propagation delay of 9.5 ns and an average power dissipation of 2 mW.

Advanced Schottky TTL, 74AS Series (AS-TTL)

Innovations in integrated-circuit design led to the development of two improved TTL series: advanced Schottky (74AS) and advanced low-power Schottky (74ALS). The 74AS series provides a considerable improvement in speed over the 74S series at a much lower power requirement. The comparison is shown in Table 8-4 for a NAND gate in each series. This comparison clearly shows the advantage of the 74AS series. It is the fastest TTL series, and its power dissipation is significantly lower than that of the 74S series. The 74AS has other improvements, including lower input current requirements ($I_{\rm IL}$, $I_{\rm IH}$), that result in a greater fan-out than in the 74S series.

Advanced Low-Power Schottky TTL, 74ALS Series

This series offers an improvement over the 74LS series in both speed and power dissipation, as the numbers in Table 8-5 illustrate. The 74ALS series has the lowest gate power dissipation of all the TTL series.

TABLE 8-4

	74S	74AS
Propagation delay	3 ns	1.7 ns
Power dissipation	20 mW	8 mW

TABLE 8-5

	74LS	74ALS
Propagation delay	9.5 ns	4 ns
Power dissipation	2 mW	1.2 mW

74F—Fast TTL

This series uses a new integrated-circuit fabrication technique to reduce interdevice capacitances and thus achieve reduced propagation delays. A typical NAND gate has an average propagation delay of 3 ns and a power consumption of 6 mW. ICs in this series are designated with the letter F in their part number. For instance, the 74F04 is a hex-inverter chip.

Comparison of TTL Series Characteristics

Table 8-6 gives the typical values for some of the more important characteristics of each of the TTL series. All of the performance ratings, except for the maximum clock rate, are for a NAND gate in each series. The maximum clock rate is specified as the maximum frequency that can be used to toggle a J-K flip-flop. This gives a useful measure of the frequency range over which each IC series can be operated.

74 74S 74LS 74**A**S **74ALS** 74F Performance ratings 9 3 4 3 Propagation delay (ns) 9.5 1.7 Power dissipation (mW) 10 20 2 8 1.2 6 Max. clock rate (MHz) 35 125 45 200 70 100 Fan-out (same series) 10 20 20 40 20 33 Voltage parameters $V_{OH}(min)$ 2.7 2.5 2.5 2.5 2.4 2.7 $V_{OL}(max)$ 0.4 0.5 0.5 0.5 0.5 0.5 $V_{\rm IH}(\rm min)$ 2.0 2.0 2.0 2.0 2.0 2.0 V_{II} (max) 0.8 0.8 0.8 0.8 0.8 0.8

TABLE 8-6 Typical TTL series characteristics.

EXAMPLE 8-3

Use Table 8-6 to calculate the dc noise margins for a typical 74LS IC. How does this compare with the standard TTL noise margins?

Solution

74LS

74

 $V_{\rm NH} = V_{\rm OH}(\rm min) - V_{\rm IH}(\rm min) \qquad V_{\rm NH} = 2.4 V - 2.0 V \\ = 2.7 V - 2.0 V \qquad = 0.4 V \\ = 0.7 V \qquad V_{\rm NL} = V_{\rm IL}(\rm max) - V_{\rm OL}(\rm max) \qquad V_{\rm NL} = 0.8 V - 0.4 V \\ = 0.8 V - 0.5 V \qquad = 0.4 V \\ = 0.3 V \qquad = 0.4 V$

EXAMPLE 8-4

Which TTL series can drive the most device inputs of the same series?

Solution

The 74AS series has the highest fan-out (40), which means that a 74AS00 NAND gate can drive 40 inputs of other 74AS devices. If we want to determine

the number of inputs of a *different* TTL series that an output can drive, we will need to know the input and output currents of the two series. This will be dealt with in the next section.

REVIEW QUESTIONS

- 1. (a) Which TTL series is the best at high frequencies?
 - (b) Which TTL series has the largest HIGH-state noise margin?
 - (c) Which series has essentially become obsolete in new designs?
 - (d) Which series uses a special diode to reduce switching time?
 - (e) Which series would be best for a battery-powered circuit operating at 10 MHz?
- 2. Assuming the same cost for each, why should you choose to use a 74ALS193 counter over a 74LS193 or a 74AS193 in a circuit operating from a 40-MHz clock?
- 3. Identify the pull-up and pull-down transistors for the 74S circuit in Figure 8-12.

8-5 TTL LOADING AND FAN-OUT

It is important to understand what determines the fan-out or load drive capability of an IC output. Figure 8-13(a) shows a standard TTL output in the LOW state connected to drive several standard TTL inputs. Transistor Q_4 is on and is acting as a current sink for an amount of current I_{OL} that is the sum of the I_{IL} currents from each input. In its ON state, Q_4 's collector–emitter resistance is very small, but it is not zero, and so the current I_{OL} will produce a voltage drop V_{OL} . This voltage must not exceed the $V_{OL}(max)$ limit of the IC, which limits the maximum value of I_{OL} and thus the number of loads that can be driven.

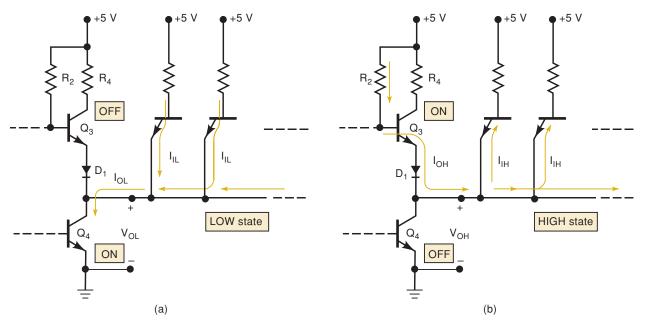


FIGURE 8-13 Currents when a TTL output is driving several inputs.

To illustrate, suppose that the ICs are in the 74 series and each $I_{\rm IL}$ is 1.6 mA. From Table 8-6, we see that the 74 series has $V_{\rm OL}(\max) = 0.4$ V and $V_{\rm IL}(\max) = 0.8$ V. Let's suppose further that Q_4 can sink up to 16 mA before its output voltage reaches $V_{\rm OL}(\max) = 0.4$ V. This means that it can sink the current from up to 16 mA/1.6 mA = 10 loads. If it is connected to more than 10 loads, its $I_{\rm OL}$ will increase and cause $V_{\rm OL}$ to increase above 0.4 V. This is usually undesirable because it reduces the noise margin at the IC inputs [remember, $V_{\rm NL} = V_{\rm IL}(\max) - V_{\rm OL}(\max)$]. In fact, if $V_{\rm OL}$ rises above $V_{\rm IL}(\max) = 0.8$ V, it will be in the indeterminate range.

A similar situation occurs in the HIGH state depicted in Figure 8-13(b). Here, Q_3 is acting as an emitter follower that is sourcing (supplying) a total current I_{OH} that is the sum of the I_{IH} currents of the different TTL inputs. If too many loads are being driven, this current I_{OH} will become large enough to cause the voltage drops across R_2 , Q_3 's emitter-base junction, and D_1 to bring V_{OH} below $V_{\text{OH}}(\text{min})$. This too is undesirable because it reduces the HIGH-state noise margin and could even cause V_{OH} to go into the indeterminate range.

What this all means is that a TTL output has a limit, $I_{OL}(max)$, on how much current it can sink in the LOW state. It also has a limit, $I_{OH}(max)$, on how much current it can source in the HIGH state. These output current limits must not be exceeded if the output voltage levels are to be maintained within their specified ranges.

Determining the Fan-Out

To determine how many different inputs an IC output can drive, you need to know the current drive capability of the output [i.e., $I_{OL}(max)$ and $I_{OH}(max)$] and the current requirements of each input (i.e., I_{IL} and I_{IH}). This information is always presented in some form on the manufacturer's IC data sheet. The following examples will illustrate one type of situation.

EXAMPLE 8-5

How many 74ALS00 NAND gate inputs can be driven by a 74ALS00 NAND gate output?

Solution

We will consider the LOW state first as depicted in Figure 8-14. Refer to the 74ALS00 data sheet in Figure 8-11 and find

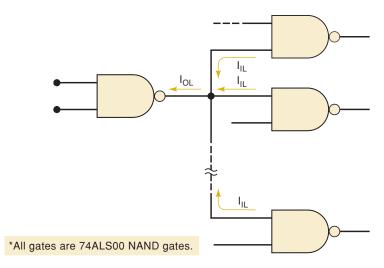
 $I_{OL}(max) = 8 mA$ $I_{IL}(max) = 0.1 mA$

This says that a 74ALS00 output can sink a maximum of 8 mA and that each 74ALS00 input will source a maximum of 0.1 mA back through the driving gate's output. Thus, the number of inputs that can be driven in the LOW state is obtained as

fan-out (LOW) =
$$\frac{I_{OL}(max)}{I_{IL}(max)}$$

= $\frac{8 \text{ mA}}{0.1 \text{ mA}}$
= 80





(*Note:* The entry for $I_{\rm IL}$ is actually -0.1 mA. The negative sign is used to indicate that this current flows *out of* the input terminal; we can ignore this sign for our purposes here.) The HIGH state is analyzed in the same manner. Refer to the data sheet to find values for $I_{\rm OH}$ and $I_{\rm IH}$, ignoring any negative signs.

 $I_{OH}(max) = 0.4 \text{ mA} = 400 \,\mu\text{A}$ $I_{IH}(max) = 20 \,\mu\text{A}$

Thus, the number of inputs that can be driven in the HIGH state is

fan-out (HIGH) = $\frac{I_{OH}(max)}{I_{IH}(max)}$ = $\frac{400 \ \mu A}{20 \ \mu A}$ = 20

If fan-out (LOW) and fan-out (HIGH) are not the same, as will sometimes occur, the fan-out is chosen as the smaller of the two. Thus, the 74ALS00 NAND gate can drive up to 20 other 74ALS00 NAND gates.

EXAMPLE 8-6

Refer to the data sheet on the TI CD ROM (or Table 8-7) and determine how many 74AS20 NAND gates can be driven by the output of another 74AS20.

Solution

The 74AS20 data sheet gives the following values:

$$\begin{split} I_{\rm OH}(\max) &= 2 \, \mathrm{mA} \\ I_{\rm OL}(\max) &= 20 \, \mathrm{mA} \\ I_{\rm IH}(\max) &= 20 \, \mu \mathrm{A} \\ I_{\rm IL}(\max) &= 0.5 \, \mathrm{mA} \end{split}$$

Considering the HIGH state first, we have

fan-out (HIGH) =
$$\frac{2 \text{ mA}}{20 \,\mu\text{A}} = 100$$

For the LOW state, we have

fan-out (LOW) =
$$\frac{20 \text{ mA}}{0.5 \text{ mA}} = 40$$

In this case, the overall fan-out is chosen to be 40 because it is the lower of the two values. Thus, one 74AS20 can drive 40 other 74AS20 inputs.

In older equipment, you will notice that most of the logic ICs were often chosen from the same logic family. In today's digital systems, there is much more likely to be a combination of various logic families. Consequently, loading and fan-out calculations are not as straightforward as they once were. A good method for determining the loading of any digital output is as follows:

- **Step 1.** Add the $I_{\rm IH}$ for all inputs connected to an output. This sum must be less than the output's $I_{\rm OH}$ specification.
- **Step 2.** Add the I_{IL} for all inputs connected to an output. This sum must be less than the output's I_{OL} specification.

Table 8-7 shows the limiting specifications for input and output currents in simple logic gates of the various TTL families. Notice that some of the current values are given as negative numbers. This convention is used to show the direction of current flow. Positive values indicate current flowing into the specified node, whether it is an input or an output. Negative values indicate current flowing out of the specified node. Consequently, all $I_{\rm OH}$ values are negative as current flows out of the output (sourcing current), and all $I_{\rm OL}$ values are positive as load current flows into the output pin on its way to ground (sinking current). Likewise, $I_{\rm IH}$ is positive, while $I_{\rm IL}$ is negative. When calculating loading and fan-out as described above, you should ignore these signs.

	Outp	Outputs		puts
TTL Series	I _{OH}	I _{OL}	I _{IH}	I _{IL}
74	-0.4 mA	16 mA	40 μA	-1.6 mA
74S	-1 mA	20 mA	50 μΑ	-2 mA
74LS	-0.4 mA	8 mA	20 μA	-0.4 mA
74AS	-2 mA	20 mA	20 µA	-0.5 mA
74ALS	-0.4 mA	8 mA	20 µA	-0.1 mA
74F	-1 mA	20 mA	20 µA	-0.6 mA

*Some devices may have different input or output current ratings. Always consult the data sheet.

TABLE 8-7Current ratingsof TTL series logic gates.*

EXAMPLE 8-7

A 74ALS00 NAND gate output is driving three 74S gate inputs and one 7406 input. Determine if there is a loading problem.

Solution

1. Add all of the $I_{\rm IH}$ values:

 $\begin{aligned} & 3 \cdot (I_{\rm IH} \text{ for } 74 \text{S}) \, + \, 1 \cdot (I_{\rm IH} \text{ for } 74) \\ & \text{Total} \, = \, 3 \cdot (50 \, \mu \text{A}) \, + \, 1 \cdot (40 \, \mu \text{A}) \, = \, 190 \, \mu \text{A} \end{aligned}$

The $I_{\rm OH}$ for the 74ALS output is 400 μ A (max), which is greater than the sum of the loads (190 μ A). This poses no problem when the output is HIGH.

2. Add all of the $I_{\rm IL}$ values:

 $3 \cdot (I_{IL} \text{ for } 74\text{S}) + 1 \cdot (I_{IL} \text{ for } 74)$ Total = $3 \cdot (2 \text{ mA}) + 1 \cdot (1.6 \text{ mA}) = 7.6 \text{ mA}$

The I_{OH} for the 74ALS output is 8 mA (max), which is greater than the sum of the loads (7.6 mA). This poses no problem when the output is LOW.

EXAMPLE 8-8

The 74ALS00 NAND gate output in Example 8-7 needs to be used to drive some 74ALS inputs in addition to the load inputs described in Example 8-7. How many additional 74ALS inputs could the output drive without being overloaded?

Solution

From the calculations of Example 8-7, only in the LOW state are we close to being overloaded. A 74ALS input has an $I_{\rm IL}$ of 0.1 mA. The maximum sink current ($I_{\rm OL}$) is 8 mA, and the load current is 7.6 mA (as calculated in Example 8-7). The additional current that the output can sink is found by

Additional current = I_{OLmax} - sum of loads (I_{IL}) = 8 mA - 7.6 mA = 0.4 mA

This output can drive up to four more 74ALS inputs that have an $I_{\rm IL}$ of 0.1 mA.

EXAMPLE 8-9

The output of a 74AS04 inverter is providing the CLEAR signal to a parallel register made up of 74AS74 D flip-flops. What is the maximum number of FF *CLR* inputs that this gate can drive?

Solution

The input specifications for flip-flop inputs are not always the same as those for a logic gate input in the same family. Refer to the 74AS74 data sheet on the TI CD ROM. The clock and *D* inputs are similar to the gate inputs in Table 8-7. However, the *PRE* and *CLR* inputs have specifications of $I_{\rm IH} = 40 \,\mu\text{A}$ and $I_{\rm IL} = 1.8 \,\text{mA}$. The 74AS04 has specifications of $I_{\rm OH} = 2 \,\text{mA}$ and $I_{\rm OL} = 20 \,\text{mA}$.

Maximum number of inputs (HIGH) = $2 \text{ mA}/40 \mu \text{A} = 50$ Maximum number of inputs (LOW) = 20 mA/1.8 mA = 11.11

We must limit the fan-out to 11 CLR inputs.

REVIEW QUESTIONS

- 1. What factors determine the $I_{OL}(max)$ rating of a device?
- 2. How many 7407 inputs can a 74AS chip drive?
- 3. What can happen if a TTL output is connected to more gate inputs than it is rated to handle?
- 4. How many 74S112 *CP* inputs can be driven by a 74LS04 output? By a 74F00 output?

8-6 OTHER TTL CHARACTERISTICS

Several other characteristics of TTL logic must be understood if one is to use TTL intelligently in a digital-system application.

Unconnected Inputs (Floating)

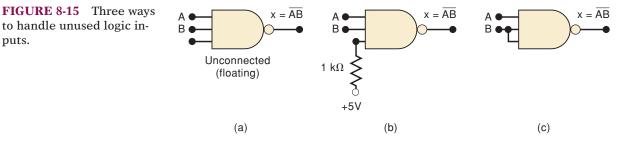
Any input to a TTL circuit that is left disconnected (open) acts exactly like a logical 1 applied to that input because in either case the emitter-base junction or diode at the input will not be forward-biased. This means that on *any* TTL IC, *all* of the inputs are 1s if they are not connected to some logic signal or to ground. When an input is left unconnected, it is said to be **floating**.

Unused Inputs

Frequently, not all of the inputs on a TTL IC are being used in a particular application. A common example is when not all the inputs to a logic gate are needed for the required logic function. For example, suppose that we needed the logic operation \overline{AB} and we were using a chip that had a three-input NAND gate. The possible ways of accomplishing this are shown in Figure 8-15.

In Figure 8-15(a), the unused input is left disconnected, which means that it acts as a logical 1. The NAND gate output is therefore $x = \overline{A \cdot B \cdot 1} = \overline{A \cdot B}$, which is the desired result. Although the logic is correct, it is highly undesirable to leave an input disconnected because it will act like an antenna, which is liable to pick up stray radiated signals that could cause the gate to operate improperly. A better technique is shown in Figure 8-15(b). Here, the unused input is connected to +5 V through a $1 \cdot k\Omega$ resistor, so that the logic level is a 1. The $1 \cdot k\Omega$ resistor is simply for current protection of the emitter-base junctions of the gate inputs in case of spikes on the power-supply line. This same technique can be used for AND gates because a 1 on an unused input will not affect the output. As many as 30 unused inputs can share the same $1 \cdot k\Omega$ resistor tied to V_{CC} .

A third possibility is shown in Figure 8-15(c), where the unused input is tied to a used input. This is satisfactory provided that the circuit driving



input *B* is not going to have its fan-out exceeded. This technique can be used for *any* type of gate. For OR gates and NOR gates, the unused inputs cannot be left disconnected or tied to +5 V because this would produce a constantoutput logic level (1 for OR, 0 for NOR) regardless of the other inputs. Instead, for these gates, the unused inputs must either be connected to ground (0 V) for a logic 0 or be tied to a used input, as in Figure 8-15(c).

Tied-Together Inputs

When two (or more) TTL inputs on the same gate are connected together to form a common input, as in Figure 8-15(c), the common input will generally represent a load that is the sum of the load current rating of each individual input. The only exception is for NAND and AND gates. For these gates, the LOW-state input load *will be the same as a single input* no matter how many inputs are tied together.

To illustrate, assume that each input of the three-input NAND gate in Figure 8-15(c) is rated at 0.5 mA for $I_{\rm IL}$ and 20 μ A for $I_{\rm IH}$. The common input *B* will therefore represent an input load of 40 μ A in the HIGH state but only 0.5 mA in the LOW state. The same would be true if this were an AND gate. If it were an OR or a NOR gate, the common *B* input would present an input load 40 μ A in the HIGH state and 1 mA in the LOW state.

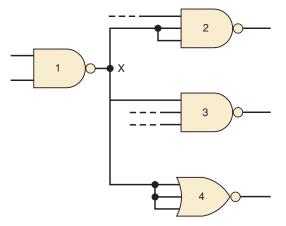
The reason for this characteristic can be found by looking back at the circuit diagram of the TTL NAND gate in Figure 8-8(b). The current I_{IL} is limited by the resistance R_1 . Even if inputs *A* and *B* were tied together and grounded, this current would not change; it would merely divide and flow through the parallel paths provided by diodes D_2 and D_3 . The situation is different for OR and NOR gates because they do not use multiple-emitter transistors but rather have a separate input transistor for each input, as we saw in Figure 8-10.

EXAMPLE 8-10

Determine the load that the X output is driving in Figure 8-16. Assume that each gate is a 74LS series device with $I_{\rm IH} = 20 \,\mu\text{A}$ and $I_{\rm IL} = 0.4 \,\text{mA}$.

Solution

The loading on the output of gate 1 is equivalent to six 74LS input loads in the HIGH state but only five 74LS input loads in the LOW state because the NAND gate represents only a single input load in the LOW state.



Loading on gate 1 output						
HIGH		LOW				
Load Current	Gate	Load Current	Gate			
40 μA	2	0.4 mA	2			
20 µA	3	0.4 mA	3			
60 µA	4	1.2 mA	4			
120 μA	Total	2.0 mA	Total			

FIGURE 8-16 Example 8-10.

Biasing TTL Inputs Low

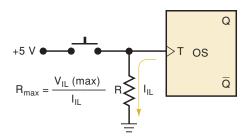
Occasionally, the situation arises where a TTL input must be held normally LOW and then caused to go HIGH by the actuation of a mechanical switch. This situation is illustrated in Figure 8-17 for the input to a one-shot. This OS triggers on a positive transition that occurs when the switch is momentarily closed. The resistor R serves to keep the T input LOW while the switch is open. Care must be taken to keep the value of R low enough so that the voltage developed across it by the current $I_{\rm IL}$ that flows out of the OS input to ground will not exceed $V_{\rm IL}(\max)$. Thus, the largest value of R is given by

$$R_{\rm max} = \frac{V_{\rm IL}({\rm max})}{I_{\rm IL}}$$

$$R_{\rm max} = \frac{V_{\rm IL}({\rm max})}{I_{\rm IL}}$$
(8-3)

R must be kept below this value to ensure that the OS input will be at an acceptable LOW level while the switch is open. The minimum value of *R* is determined by the current drain on the 5-V supply when the switch is closed. In practice, this current drain should be minimized by keeping *R* just slightly below R_{max} .

FIGURE 8-17



EXAMPLE 8-10

Determine an acceptable value for *R* if the OS is a 74LS TTL IC with an I_{IL} input rating of 0.4 mA.

Solution

The value of I_{IL} will be a maximum of 0.4 mA. This maximum value should be used to calculate R_{max} . From Table 8-6, $V_{IL}(max) = 0.8$ V for the 74LS series. Thus, we have

$$R_{\rm max} = \frac{0.8 \, \rm V}{0.4 \, \rm mA} = 2000 \, \Omega$$

A good choice here would be $R = 1.8 \text{ k}\Omega$, a standard resistor value.

Current Transients

TTL logic circuits suffer from internally generated current transients or spikes because of the totem-pole output structure. When the output is switching from the LOW state to the HIGH state (see Figure 8-18), the two output transistors are changing states: Q_3 OFF to ON, and Q_4 ON to OFF. Because Q_4 is changing from the saturated condition, it will take longer than

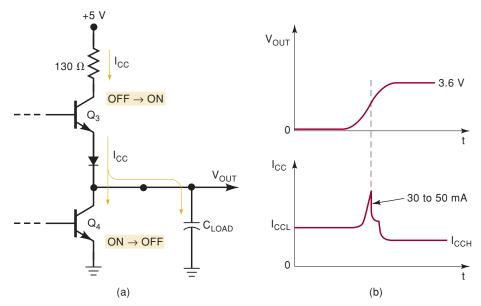


FIGURE 8-18 A large current spike is drawn from V_{CC} when a totem-pole output switches from LOW to HIGH.

 Q_3 to switch states. Thus, there is a short interval of time (about 2 ns) during the switching transition when both transistors are conducting and a relatively large surge of current (30 to 50 mA) is drawn from the +5 V supply. The duration of this current transient is extended by the effects of any load capacitance on the circuit output. This capacitance consists of stray wiring capacitance and the input capacitance of any load circuits and must be charged up to the HIGH-state output voltage. This overall effect can be summarized as follows:

Whenever a totem-pole TTL output goes from LOW to HIGH, a high-amplitude current spike is drawn from the V_{CC} supply.

In a complex digital circuit or system, there may be many TTL outputs switching states at the same time, each one drawing a narrow spike of current from the power supply. The accumulative effect of all of these current spikes will be to produce a voltage spike on the common V_{CC} line, mostly due to the distributed inductance on the supply line [remember: V = L(di/dt) for inductance, and di/dt is very large for a 2-ns current spike]. This voltage spike can cause serious malfunctions during switching transitions unless some type of filtering is used. The most common technique uses small radio-frequency capacitors connected from V_{CC} to GROUND essentially to "short out" these high-frequency spikes. This is called **power-supply decoupling**.

It is standard practice to connect a 0.01- μ F or 0.1- μ F low-inductance, ceramic disk capacitor between V_{CC} and ground near each TTL IC on a circuit board. The capacitor leads are kept very short to minimize series inductance.

In addition, it is standard practice to connect a single large capacitor (2 to $20 \ \mu\text{F}$) between V_{CC} and ground on each board to filter out relatively low-frequency variations in V_{CC} caused by the large changes in I_{CC} levels as outputs switch states.

REV	EW	QU	ESTI	ONS

- 1. What will be the logic output of a TTL NAND gate that has all of its inputs unconnected?
- 2. What are two acceptable ways to handle unused inputs to an AND gate?
- 3. Repeat question 2 for a NOR gate.
- 4. *True or false:* When NAND gate inputs are tied together, they are always treated as a single load on the signal source.
- 5. What is power-supply decoupling? Why is it used?

8-7 MOS TECHNOLOGY

MOS (metal-oxide-semiconductor) technology derives its name from the basic MOS structure of a metal electrode over an oxide insulator over a semiconductor substrate. The transistors of MOS technology are field-effect transistors called **MOSFETs**. This means that the electric *field* on the *metal* electrode side of the *oxide* insulator has an *effect* on the resistance of the substrate. Most of the MOS digital ICs are constructed entirely of MOSFETs and no other components.

The chief advantages of the MOSFET are that it is relatively simple and inexpensive to fabricate, it is small, and it consumes very little power. The fabrication of MOS ICs is approximately one-third as complex as the fabrication of bipolar ICs (TTL, ECL, etc.). In addition, MOS devices occupy much less space on a chip than do bipolar transistors. More important, MOS digital ICs normally do not use the IC resistor elements that take up so much of the chip area of bipolar ICs.

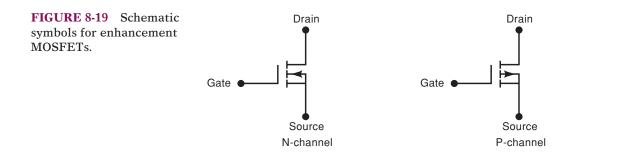
All of this means that MOS ICs can accommodate a much larger number of circuit elements on a single chip than bipolar ICs. This advantage is illustrated by the fact that MOS ICs have dominated bipolar ICs in the area of large-scale integration (LSI, VLSI). The high packing density of MOS ICs makes them especially well suited for complex ICs such as microprocessor and memory chips. Improvements in MOS IC technology have led to devices that are faster than 74, 74LS, and 74ALS TTL with comparable current drive characteristics. Consequently, MOS devices (specifically CMOS) have also become dominant in the SSI and MSI market. The 74AS TTL family is still as fast as the best CMOS devices, but at the price of much greater power dissipation.

The principal disadvantage of MOS devices is their susceptibility to static-electricity damage. Although this can be minimized by proper handling procedures, TTL is still more durable for laboratory experimentation. Consequently, you are likely to see TTL devices used in education as long as they are available.

The MOSFET

There are presently two general types of MOSFETs: *depletion* and *enhancement*. MOS digital ICs use enhancement MOSFETs exclusively, and so only this type will be considered in the following discussion. Furthermore, we will concern ourselves only with the operation of these MOSFETs as on/off switches.

Figure 8-19 shows the schematic symbols for the N-channel and P-channel enhancement MOSFETs, where the direction of the arrow indicates either

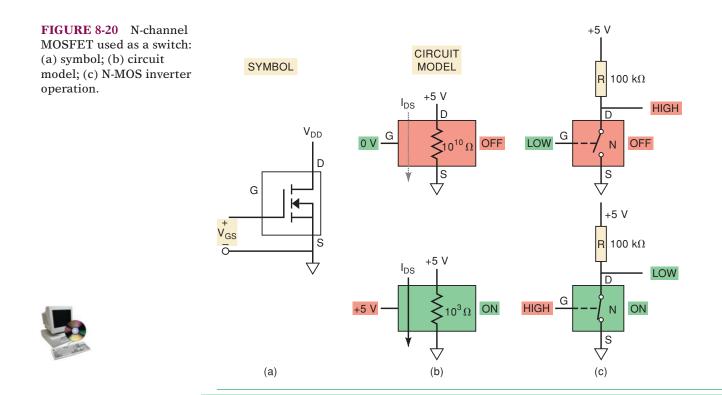


P- or N-channel. The symbols show a broken line between the *source* and the *drain* to indicate that there is *normally* no conducting channel between these electrodes. The symbol also shows a separation between the *gate* and the other terminals to indicate the very high resistance (typically around $10^{12} \Omega$) of the oxide layer between the gate and the channel, which is formed in the substrate.

Basic MOSFET Switch

Figure 8-20 shows the switching operation of an N-channel MOSFET, the basic element in a family of devices known as **N-MOS**. For the N-channel device, the drain is always biased positive relative to the source. The gate-to-source voltage V_{GS} is the input voltage, which is used to control the resistance between drain and source (i.e., the channel resistance) and therefore determines whether the device is on or off.

When $V_{GS} = 0$ V, there is no conductive channel between source and drain, and the device is off, as shown in Figure 8-20(b). Typically the channel resistance in this OFF state is $10^{10} \Omega$, which for most purposes is an *open circuit*. The MOSFET will remain off as long as V_{GS} is zero or negative. As V_{GS} is made positive (gate positive relative to source), a threshold voltage (V_T) is reached, at



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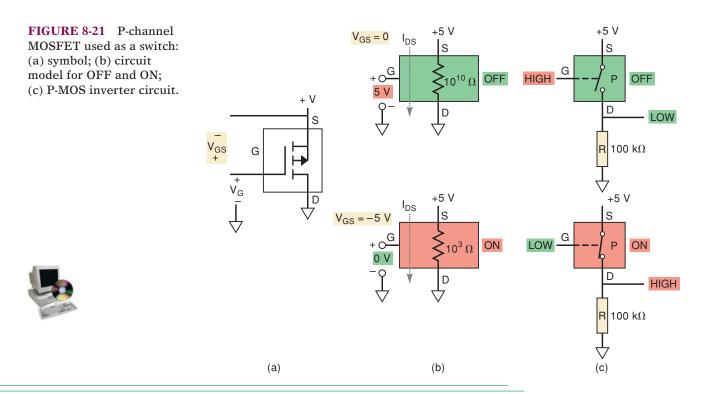
which point a conductive channel begins to form between source and drain. Typically $V_{\rm T} = +1.5$ V for an N-MOSFET, and so any $V_{GS} \ge 1.5$ V will cause the MOSFET to conduct. Generally, a value of V_{GS} much larger than $V_{\rm T}$ is used to turn on the MOSFET more completely. As shown in Figure 8-20(b), when $V_{GS} = +5$ V, the channel resistance between source and drain has dropped to a value of $R_{\rm ON} = 1000 \ \Omega$.

In essence, then, the N-MOS will switch from a very high resistance to a low resistance as the gate voltage switches from a LOW voltage to a HIGH voltage. It is helpful simply to think of the MOSFET as a switch that is either opened or closed between source and drain. Figure 8-20(c) shows how an inverter can be formed using one N-MOS transistor as a switch. The first N-MOS logic devices were built using this approach. The drawback to this circuit, as with TTL, is that when the transistor is ON, there will always be current flowing from the supply to ground, producing heat.

The P-channel MOSFET, or P-MOS, shown in Figure 8-21(a) operates in exactly the same manner as the N-channel except that it uses voltages of opposite polarity. For P-MOSFETs, the drain is connected to the lower side of the circuit so that it is biased with a more negative voltage relative to the source. To turn the P-MOSFET ON, a voltage *lower* than the source by $V_{\rm T}$ must be applied to the gate, meaning the voltage at the gate, relative to the source, must be negative.

Figure 8-21(b) shows that when the gate is at 5 V with respect to ground (the same voltage as applied to the source), the transistor is OFF and has a very high resistance from drain to source. When the gate is at 0 V (relative to ground), then the gate-to-source voltage $V_{\rm GS} = -5$ V and it turns the transistor ON, lowering its resistance from drain to source. The circuit of Figure 8-20(c) shows the switching action of an inverter using P-MOS logic.

Table 8-8 summarizes the P- and N-channel switching characteristics.



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TABLE 8-8

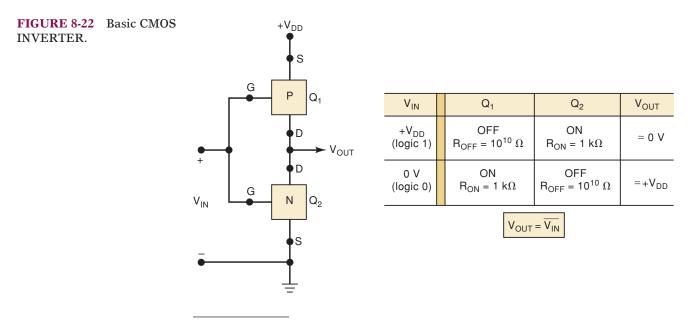
	Drain-to- Source Bias	Gate-to-Source Voltage (<i>V_{GS}</i>) Needed for Conduction	R_{ON} (Ω)	R_{OFF} (Ω)
P-channel	Negative	Typically more negative than -1.5 V	1000 (typical)	10 ¹⁰
N-channel	Positive	Typically more positive than +1.5 V	1000 (typical)	10 ¹⁰

8-8 COMPLEMENTARY MOS LOGIC

P-MOS and N-MOS logic circuits use fewer components and are much simpler to manufacture than TTL circuits. As a result, they began to dominate the LSI and VLSI markets in the 1970s and 1980s. During this era, a new technology began to emerge that used both P-MOS transistors (as high-side switches) and N-MOS transistors (as low-side switches) in the same logic circuit. This is referred to as complementary MOS, or **CMOS**, technology. CMOS logic circuits are not quite as simple and easy to manufacture as P-MOS or N-MOS, but they are faster, use much less power, and are the dominant technology in the market today.

CMOS Inverter

The circuitry for the basic CMOS INVERTER is shown in Figure 8-22. For this diagram and those that follow, the standard symbols for the MOSFETs have been replaced by blocks labeled P and N to denote a P-MOS and an N-MOS, respectively. This is done simply for convenience in analyzing the circuits. The CMOS INVERTER has two MOSFETs in series so that the P-channel device has its source connected to $+V_{DD}$ (a positive voltage), and the N-channel device has its source connected to ground.* The gates of the two devices are connected together as a common input. The drains of the two devices are connected together as the common output.



*Most manufacturers label this terminal V_{SS} .

The logic levels for CMOS are essentially $+V_{DD}$ for logical 1 and 0 V for logical 0. Consider, first, the case where $V_{IN} = +V_{DD}$. In this situation, the gate of Q_1 (P-channel) is at 0 V relative to the source of Q_1 . Thus, Q_1 will be in the OFF state with $R_{OFF} \approx 10^{10} \Omega$. The gate of Q_2 (N-channel) will be at $+V_{DD}$ relative to its source. Thus, Q_2 will be on with typically $R_{ON} = 1 \ k\Omega$. The voltage divider between Q_1 's R_{OFF} and Q_2 's R_{ON} will produce $V_{OUT} \approx 0 \ V$.

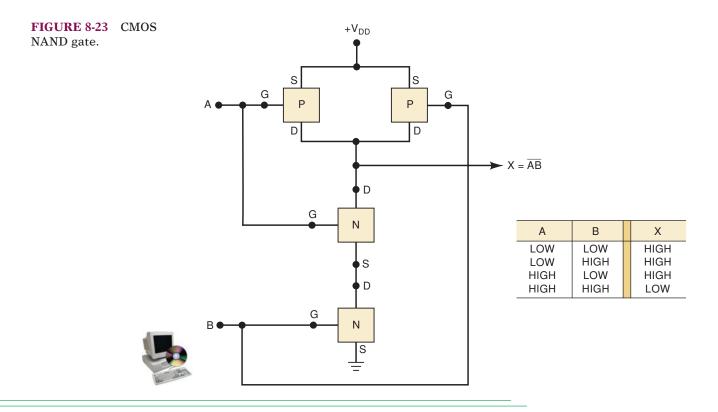
Next, consider the case where $V_{\rm IN} = 0$ V. Q_1 now has its gate at a negative potential relative to its source, while Q_2 has $V_{GS} = 0$ V. Thus, Q_1 will be on with $R_{\rm ON} = 1$ k Ω , and Q_2 will be off with $R_{\rm OFF} = 10^{10} \Omega$, producing a $V_{\rm OUT}$ of approximately $+V_{DD}$. These two operating states are summarized in the table on Figure 8-22, showing that the circuit does act as a logic INVERTER.

CMOS NAND Gate

Other logic functions can be constructed by modifying the basic INVERTER. Figure 8-23 shows a NAND gate formed by adding a parallel P-channel MOSFET and a series N-channel MOSFET to the basic INVERTER. To analyze this circuit, it helps to realize that a 0-V input turns on its corresponding P-MOS and turns off its corresponding N-MOS, and vice versa, for a $+V_{DD}$ input. Thus, you can see that the only time a LOW output will occur is when inputs *A* and *B* are both HIGH $(+V_{DD})$ to turn on both N-MOSFETs, thereby providing a low resistance from the output terminal to ground. For all other input conditions, at least one P-MOS will be on while at least one N-MOS will be off. This produces a HIGH output.

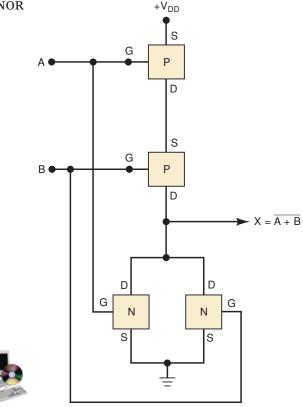
CMOS NOR Gate

A CMOS NOR gate is formed by adding a series P-MOS and a parallel N-MOS to the basic INVERTER, as shown in Figure 8-24. Once again, this circuit can be analyzed by realizing that a LOW at any input turns on its corresponding





gate.



А	В	Х
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

P-MOS and turns off its corresponding N-MOS, and vice versa, for a HIGH input. It is left to the reader to verify that this circuit operates as a NOR gate.

CMOS AND and OR gates can be formed by combining NANDs and NORs with INVERTERs.

CMOS SET-RESET FF

Two CMOS NOR gates or NAND gates can be cross-coupled to form a simple SET-RESET latch. Additional gating circuitry is used to convert the basic SET-RESET latch to clocked D and J-K flip-flops.

REVIEW QUESTIONS	1. How does CMOS internal circuitry differ from N-MOS?
	2. How many P-channel MOSFETs are in a CMOS INVERTER?
	3. How many MOSFETs are in a three-input CMOS NAND gate?

8-9 CMOS SERIES CHARACTERISTICS

CMOS ICs provide not only all of the same logic functions that are available in TTL but also several special-purpose functions not provided by TTL. Several different CMOS series have been developed over time because manufacturers have sought to improve performance characteristics. Before we look at the various CMOS series, it will be helpful to define a few terms that are used when ICs from different families or series are to be used together or as replacements for one another.

- **Pin-compatible.** Two ICs are pin-compatible when their pin configurations are the same. For example, pin 7 on both ICs is GROUND, pin 1 on both is an input to the first INVERTER, and so on.
- Functionally equivalent. Two ICs are functionally equivalent when the logic functions they perform are exactly the same. For example, both contain four two-input NAND gates, or both contain six D flip-flops with positive-edge clock triggering.
- Electrically compatible. Two ICs are electrically compatible when they can be connected directly to each other without taking any special measures to ensure proper operation.

4000/14000 Series

The oldest CMOS series is the 4000 series first introduced by RCA, and its functionally equivalent 14000 series from Motorola. Devices in the 4000/14000 series have very low power dissipation and can operate over a wide range of power-supply voltages (3 to 15 V). They are very slow compared to TTL and other CMOS series and have very low output current capabilities. They are not pin-compatible or electrically compatible with any TTL series. The 4000/14000 series devices are rarely used in new designs except when a special-purpose IC is available that is not available in other series.

74HC/HCT (High-Speed CMOS)

The 74HC series has a 10-fold increase in switching speed, comparable to that of the 74LS devices, and a much higher output current capability than the first 7400 CMOS series ICs. 74HC/HCT ICs are pin-compatible with and functionally equivalent to TTL ICs with the same device number. 74HCT devices are electrically compatible with TTL, but 74HC devices are not. This means, for example, that a 74HCT04 hex-INVERTER chip can replace a 74LS04 chip, and vice versa. It also means that a 74HCT IC can be connected directly to any TTL IC.

74AC/ACT (Advanced CMOS)

This series is often referred to as ACL for advanced CMOS logic. The series is functionally equivalent to the various TTL series but is *not* pin-compatible with TTL because the pin placements on 74AC or 74ACT chips have been chosen to improve noise immunity so that the device inputs are less sensitive to signal changes occurring on other IC pins. 74AC devices are not electrically compatible with TTL; 74ACT devices can be connected directly to TTL. ACL offers advantages over the HC series in noise immunity, propagation delay, and maximum clock speed.

Device numbering for this series differs slightly from TTL, 74C, and 74HC/HCT numbering. It uses a five-digit device number beginning with the digits 11. The following examples illustrate:

74AC11004=74HC0474ACT11293=74HCT293

This series of CMOS devices offers a natural migration path from the HC series to faster, lower-power, low-drive applications. The devices in this series are three times faster and can be used as direct replacements for HC series devices. They offer similar noise immunity to HC without the overshoot/undershoot problems often associated with higher drive characteristics required for comparable speed.

BiCMOS 5-V Logic

Several IC manufacturers have developed logic series that combine the best features of bipolar and CMOS logic—called BiCMOS logic. The low-power characteristics of CMOS and the high-speed characteristics of bipolar circuits are integrated to produce an extremely low-power, high-speed logic family. BiCMOS ICs are not available in most SSI and MSI functions, but are limited to functions that are used in microprocessor and bus interfacing applications such as latches, buffers, drivers, and transceivers. The 74BCT (BiCMOS bus-interface technology) series offers 75 percent reduction in power consumption over the 74F family while maintaining similar speed and drive characteristics. Parts in this series are pin-compatible with industry standard TTL parts and operate on standard 5-V logic levels. The 74ABT (advanced BiCMOS technology) series is the second generation of BiCMOS bus-interface devices. Details of bus interface logic will be presented Section 8-13.

Power-Supply Voltage

The 4000/14000 series and 74C series devices operate with V_{DD} values ranging from 3 to 15 V, which makes them very versatile. They can be used in low-voltage battery-operated circuits, in standard 5-V circuits, and in circuits where a higher supply voltage is used to attain the noise margins required for operation in a high-noise environment. The 74HC/HCT, 74AC/ACT, and 74AHC/AHCT series operate over a much narrower range of supply voltages, typically between 2 and 6 V.

Logic series that are designed to operate at lower voltages (e.g., 2.5 or 3.3 V) are also available. Whenever devices that use different power supply voltages are interconnected in the same digital system, special measures must be taken. The low-voltage devices and the special interfacing techniques will be covered in Section 8-10.

Logic Voltage Levels

The input and output voltage levels will be different for the different CMOS series. Table 8-9 lists these voltage values for the various CMOS series as well as those for the TTL series. The values listed in the table assume that all devices are operating from a supply voltage of 5 V and that all device outputs are driving inputs of the same logic family.

Examination of this table discloses some important points. First, note that $V_{\rm OL}$ for the CMOS devices is very close to 0 V, and $V_{\rm OH}$ is very close to 5 V. The reason why is that the CMOS outputs do not have to source or sink any significant amount of current when they are driving CMOS inputs with their extremely high input resistance ($10^{12} \Omega$). Also note that, except for 74HCT and 74ACT, the required input voltage levels are greater for CMOS than for TTL. Recall that 74HCT and 74ACT are designed to be electrically

	CMOS									TTL	
Parameter	4000B	74HC	74HCT	74AC	74 ACT	74AHC	74AHCT	74	74LS	74AS	74ALS
V _{IH} (min)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0	2.0
V _{IL} (max)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8	0.8
V _{OH} (min)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7	2.5
V _{OL} (max)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5	0.5
V _{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7	0.7
V _{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3	0.4

TABLE 8-9 Input/output voltage levels (in volts) with $V_{DD} = V_{CC} = +5$ V.

compatible with TTL, so they must be able to accept the same input voltage levels as TTL.

Noise Margins

The noise margins for each series are also given in Table 8-9. They are calculated using

 $V_{\rm NH} = V_{\rm OH}({
m min}) - V_{\rm IH}({
m min})$ $V_{\rm NL} = V_{\rm IL}({
m max}) - V_{\rm OL}({
m max})$

Note that, in general, the CMOS devices have greater noise margins than TTL. The difference would be even greater if the CMOS devices were operated at a supply voltage greater than 5 V.

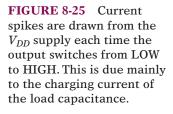
Power Dissipation

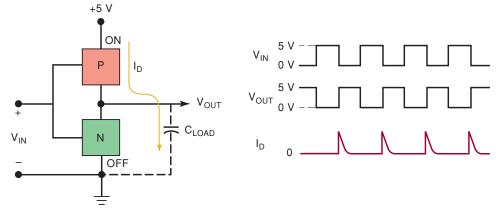
When a CMOS logic circuit is in a static state (not changing), its power dissipation is extremely low. We can see the reason by examining each of the circuits shown in Figures 8-22 to 8-24. Note that, regardless of the state of the output, there is always a very high resistance between the V_{DD} terminal and ground because there is always an off MOSFET in the current path. This results in a typical CMOS dc power dissipation of only 2.5 nW per gate when $V_{DD} = 5 \text{ V}$; even at $V_{DD} = 10 \text{ V}$, this power increases to only 10 nW. With these values for $P_{\rm D}$, it is easy to see why CMOS is ideally suited for applications using battery power or battery backup power.

P_D Increases with Frequency

The power dissipation of a CMOS IC will be very low as long as it is in a dc condition. Unfortunately, P_D will increase in proportion to the frequency at which the circuits are switching states. For example, a CMOS NAND gate that has $P_D = 10$ nW under dc conditions will have $P_D = 0.1$ mW at a frequency of 100 kpps, and 1 mW at 1 MHz. The reason for this dependence on frequency is illustrated in Figure 8-25.

Each time a CMOS output switches from LOW to HIGH, a transient charging current must be supplied to the load capacitance. This capacitance consists of the combined input capacitances of any loads being driven and the device's own output capacitance. These narrow spikes of current are



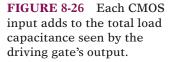


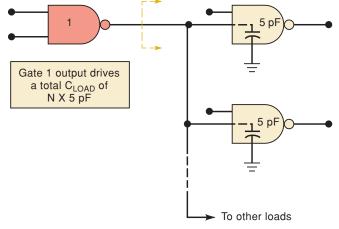
supplied by V_{DD} and can have a typical amplitude of 5 mA and a duration of 20 to 30 ns. Clearly, as the switching frequency increases, there will be more of these current spikes occurring per second, and the average current drawn from V_{DD} will increase. Even with very low capacitive loads, there is a brief point in the transition from LOW to HIGH or HIGH to LOW when the two output transistors are partially turned on. This effectively lowers the resistance from the supply to ground, causing a current spike as well.

Thus, at higher frequencies, CMOS begins to lose some of its advantage over other logic families. As a general rule, a CMOS gate will have the same average $P_{\rm D}$ as a 74LS gate at frequencies near 2 to 3 MHz. Above these frequencies, TTL power also increases with frequency because of the current required to reverse the charge on the load capacitance. For MSI chips, the situation is somewhat more complex than stated here, and a logic designer must do a detailed analysis to determine whether or not CMOS has a power-dissipation advantage at a particular frequency of operation.

Fan-Out

Like N-MOS and P-MOS, CMOS inputs have an extremely large resistance $(10^{12} \Omega)$ that draws essentially no current from the signal source. Each CMOS input, however, typically presents a 5-pF load to ground. This input capacitance limits the number of CMOS inputs that one CMOS output can drive (see Figure 8-26). The CMOS output must charge and discharge the parallel combination of all of the input capacitances, so that the output switching





time will be increased in proportion to the number of loads being driven. Typically, each CMOS load increases the driving circuit's propagation delay by 3 ns. For example, NAND gate 1 in Figure 8-26 might have a t_{PLH} of 25 ns if it were driving no loads; this would increase to 25 ns + 20(3 ns) = 85 ns if it were driving *twenty* loads.

Thus, CMOS fan-out depends on the permissible maximum propagation delay. Typically, CMOS outputs are limited to a fan-out of 50 for low-frequency operation (\leq 1 MHz). Of course, for higher-frequency operation, the fan-out would have to be less.

Switching Speed

Although CMOS, like N-MOS and P-MOS, must drive relatively large load capacitances, its switching speed is somewhat faster because of its low output resistance in each state. An N-MOS output must charge the load capacitance through a relatively large (100-k Ω) resistance. In the CMOS circuit, the output resistance in the HIGH state is the $R_{\rm ON}$ of the P-MOS-FET, which is typically 1 k Ω or less. This allows more rapid charging of load capacitance.

A 4000 series NAND gate will typically have an average t_{pd} of 50 ns at $V_{DD} = 5$ V, and 25 ns at $V_{DD} = 10$ V. The reason for the improvement in t_{pd} as V_{DD} is increased is that the R_{ON} on the MOSFETs decreases significantly at higher supply voltages. Thus, it appears that V_{DD} should be made as large as possible for operation at higher frequencies. However, the larger V_{DD} will result in increased power dissipation.

A typical NAND gate in the 74HC or 74HCT series has an average t_{pd} of around 8 ns when operated at $V_{DD} = 5$ V. A 74AC/ACT NAND gate has an average t_{pd} of around 4.7 ns. A 74AHC NAND gate has an average t_{pd} of around 4.3 ns.

Unused Inputs

CMOS inputs should never be left disconnected. All CMOS inputs must be tied either to a fixed voltage level (0 V or V_{DD}) or to another input.

This rule applies even to the inputs of extra unused logic gates on a chip. An unconnected CMOS input is susceptible to noise and static charges that could easily bias both the P-channel and the N-channel MOSFETs in the conductive state, resulting in increased power dissipation and possible overheating.

Static Sensitivity

All electronic devices, to varying degrees, are sensitive to damage by static electricity. The human body is a great storehouse of electrostatic charges. For example, when you walk across a carpet, a static charge of over 30,000 V can be built up on your body. If you then touch an electronic device, some of this sizable charge can be transferred to the device. The MOS logic families (and all MOSFETs) are especially susceptible to static-charge damage. All of this potential difference (static charge) applied across the thin oxide film overcomes the film's dielectric insulation capability. When

it breaks down, the resulting flow of current (discharge) is like a lightning strike, blowing a hole in the oxide layer and permanently damaging the device.

Electrostatic discharge (ESD) is responsible for billions of dollars of damage to electronic equipment annually, and equipment manufacturers have devoted considerable attention to developing special handling procedures for all electronic devices and circuits. Even though most modern ICs have on-chip resistor-diode networks to protect inputs and outputs from the effects of ESD, the following precautions are used by most engineering labs, production facilities, and field service departments:

- 1. Connect the chassis of all test instruments, soldering-iron tips, and your workbench (if metal) to earth ground (i.e., the round prong in the 120-VAC plug). This prevents the buildup of static charge on these devices that could be transferred to any circuit board or IC that they come in contact with.
- 2. Connect yourself to earth ground with a special wrist strap. This will allow potentially dangerous charges from your body to be discharged to ground. The wrist strap contains a 1-M Ω resistor that limits current to a nonlethal value should you accidentally touch a "live" voltage while working with the equipment.
- 3. Keep ICs (especially MOS) in conductive foam or aluminum foil. This will keep all IC pins shorted together so that no dangerous voltages can be developed between any two pins.
- 4. Avoid touching IC pins, and insert the IC into the circuit immediately after removing it from the protective carrier.
- 5. Place shorting straps across the edge connectors of PC boards when the boards are being carried or transported. Avoid touching the edge connectors. Store PC boards in conductive plastic or metallic envelopes.
- 6. Do not leave any unused IC inputs unconnected because open inputs tend to pick up stray static charges.

Latch-Up

Because of the unavoidable existence of parasitic (unwanted) PNP and NPN transistors embedded in the substrate of CMOS ICs, a condition known as latch-up can occur under certain circumstances. If these parasitic transistors on a CMOS chip are triggered into conduction, they will latchup (stay ON permanently), and a large current may flow and destroy the IC. Most modern CMOS ICs are designed with protection circuitry that helps prevent latch-up, but it can still occur when the device's maximum voltage ratings are exceeded. Latch-up can be triggered by high-voltage spikes or ringing at the device inputs and outputs. Clamping diodes can be connected externally to protect against such transients, especially when the ICs are used in industrial environments where high-voltage and/or highcurrent load switching takes place (motor controllers, relays, etc.). A wellregulated power supply will minimize spikes on the V_{DD} line; if the supply also has current limiting, it will limit current should latch-up occur. Modern CMOS fabrication techniques have greatly reduced ICs' susceptibility to latch-up.

 Which CMOS series is pin-compatible with TTL? Which CMOS series is electrically compatible with TTL? Which CMOS series is functionally equivalent to TTL? What logic family combines the best features of CMOS and bipolar logic? What factors determine CMOS fan-out? What precautions should be taken when handling CMOS ICs? Which IC family (CMOS, TTL) is best suited for battery-powered applications? True or false: (a) CMOS power drain increases with operating frequency. (b) Unused CMOS inputs can be left unconnected. (c) TTL is better suited than CMOS for operation in high-noise environments. (d) CMOS switching speed increases with operating frequency. 		
 3. Which CMOS series is functionally equivalent to TTL? 4. What logic family combines the best features of CMOS and bipolar logic? 5. What factors determine CMOS fan-out? 6. What precautions should be taken when handling CMOS ICs? 7. Which IC family (CMOS, TTL) is best suited for battery-powered applications? 8. <i>True or false:</i> (a) CMOS power drain increases with operating frequency. (b) Unused CMOS inputs can be left unconnected. (c) TTL is better suited than CMOS for operation in high-noise environments. 	TIONS	1. Which CMOS series is pin-compatible with TTL?
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(c) TTL is better suited than CMOS for operation in high-noise environ- ments.		(a) CMOS power drain increases with operating frequency.
ments.		(b) Unused CMOS inputs can be left unconnected.
(d) CMOS switching speed increases with operating frequency.		
		(d) CMOS switching speed increases with operating frequency.
(e) CMOS switching speed increases with supply voltage.		(e) CMOS switching speed increases with supply voltage.
(f) The latch-up condition is an advantage of CMOS over TTL.		(f) The latch-up condition is an advantage of CMOS over TTL.
		8-10 LOW-VOLTAGE TECHNOLOGY
8-10 LOW-VOLTAGE TECHNOLOGY		IC manufacturers are continually looking for ways to put semiconductor devices (diodes, resistors, transistors, etc.) closer together on a chip, that is, to increase the chip density. This higher density has at least two major benefits. First, it allows more circuits to be packed onto the chip; second, with the circuits closer together, the time for signals to propagate from one circuit to another will decrease, thereby improving overall circuit operating speed. There are also drawbacks to higher chip density. When circuits are placed closer together, the insulating material that isolates one circuit from another is narrow.

rower. This decreases the amount of voltage that the device can withstand before dielectric breakdown occurs. Increasing the chip density increases the overall chip power dissipation, which can raise the chip temperature above the maximum level allowed for reliable operation.

These drawbacks can be neutralized by operating the chip at lower voltage levels, thereby reducing power dissipation. Several series of logic on the market operate on 3.3 V. The newer series are optimized to run on 2.5 V. This low-voltage technology may very well signal the beginning of a gradual transition in the digital equipment field that will eventually find all digital ICs operating from a new low-voltage standard.

Low-voltage devices are currently designed for applications ranging from electronic games to engineering workstations. The newer CPUs are 2.5-V devices, and 3.3-V dynamic RAM chips are used in memory modules for personal computers.

Several low-voltage logic series are currently available. It is not possible to cover all of the families and series from all manufacturers, so we will describe those currently offered by Texas Instruments.

CMOS Family

The 74LVC (Low-Voltage CMOS) series contains the widest assortment of the familiar SSI gates and MSI functions of the 5-V families, along with many bus-interface devices such as buffers, latches, drivers, and so on. This series can handle 5-V logic levels on its inputs, so it can convert from 5-V systems to 3-V systems. As long as the current drive is kept low enough to keep the output voltage within acceptable limits, the 74LVC can also drive 5-V TTL inputs. The $V_{\rm IH}$ input requirements of 5-V CMOS parts such as the 74HC/AHC do not allow LVC devices to drive them.

- The 74ALVC (Advanced Low-Voltage CMOS) series currently offers the highest performance. The devices in this series are intended primarily for bus-interface applications that use 3.3-V logic only.
- The 74LV (Low-Voltage) series offers CMOS technology and many of the common SSI gates and MSI logic functions, along with some popular octal buffers, latches, and flip-flops. It is intended to operate only with other 3.3-V devices.
- The 74AVC (Advanced Very-Low-Voltage CMOS) series has been introduced with tomorrow's systems in mind. It is optimized for 2.5-V systems, but it can operate on supplies as low as 1.2 V or as high as 3.3 V. This broad range of supply voltage makes it useful in mixed-voltage systems. It has propagation delays of less than 2 ns, which rivals 74AS bipolar devices. It has many of the bus interface features of the BiCMOS series that will make it useful in future generations of low-voltage workstations, PCs, networks, and telecommunications equipment.
- The 74AUC (Advanced Ultra-Low-Voltage CMOS) series is optimized to operate at 1.8-V logic levels.
- The 74AUP (Advanced Ultra-low Power) series is the industries lowestpower logic series and is used in battery-operated portable applications.
- The 74CBT (Cross Bar Technology) series offers high-speed bus-interface circuits that can switch quickly when enabled and not load the bus when they are disabled.
- The 74CBTLV (Cross Bar Technology Low Voltage) is the 3.3-V complement to the 74CBT series.
- The 74GTLP (Gunning Transceiver Logic Plus) series is made for highspeed parallel backplane applications. This series will be covered in a later section.
- The 74SSTV (Stub Series Terminated Logic) is useful in the high-speed advanced-memory systems of today's computers.
- The TS Switch (TI Signal Switch) series is made for mixed-signal applications and offers some analog and digital switching and multiplexing solutions.
- The 74TVC (Translation Voltage Clamp) series is used to protect the inputs and outputs of sensitive devices from voltage overshoot on the bus lines.

BiCMOS Family

- The 74LVT (Low-Voltage BiCMOS Technology) contains BiCMOS parts that are intended for 8- and 16-bit bus-interface applications. As with the LVC series, the inputs can handle 5-V logic levels and serve as a 5-V to 3-V translator. Because the output levels $[V_{OH}(min) \text{ and } V_{OL}(max)]$ are equivalent to TTL levels, they are fully electrically compatible with TTL. Table 8-10 compares the various features.
- The 74ALVT (Advanced Low-Voltage BiCMOS Technology) series is an improvement over the LVT series. It offers 3.3-V or 2.5-V operation at 3 ns and is pin-compatible with existing ABT and LVT series. It is also intended for bus-interface applications.

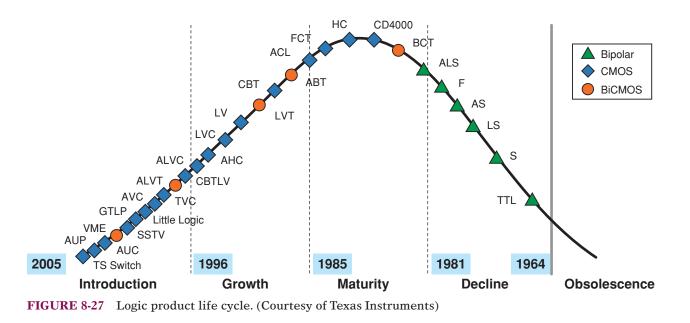
	LV	ALVC	AVC	ALVT	ALB
V _{CC} (recommended)	2.7–3.6	2.3–3.6	1.65–3.6	2.3–2.7	3–3.6
T _{PD} (ns)	18	3	1.9	3.5	2
V _{IH} (V)	2 to $V_{\rm CC}$ + 0.5	2.0 to 4.6	1.2 to 4.6	2 to 7	2.2 to 4.6
$V_{\rm IL}$ (V)	0.8	0.8	0.7	0.8	0.6
I _{OH} (mA)	6	12	8	32	25
I _{OL} (mA)	6	12	8	32	25

TABLE 8-10 Low-voltage series characteristics.

- The 74ALB (Advanced Low-Voltage BiCMOS) series is designed for 3.3-V bus-interface applications. It provides 25 mA output drive and propagation delays of only 2.2 ns.
- The 74VME (VERSA Module Eurocard) series is designed to operate with the standard VME bus technology.

Digital technicians and engineers can no longer assume that every IC in a digital circuit, system, or piece of equipment is operating at 5 V, and they must be prepared to deal with the necessary interfacing considerations in mixed-voltage systems. The interfacing skills you learn in this chapter will allow you to accomplish this, regardless of what develops as low-voltage systems become more common.

The continued development of low-voltage technology promises to bring about a complete revolution from the original 5-V system, to mixed-voltage systems, and finally to pure 3.3-V, 2.5-V, or even lower-voltage digital systems. To put all of this in perspective, Figure 8-27 shows Texas Instruments' perception of the life cycle of the various logic families.



- 1. What are the two advantages of higher-density ICs?
- 2. What are the drawbacks?
- 3. What is the minimum HIGH voltage at a 74LVT input?
- 4. Which low-voltage series can work only with other low-voltage series ICs?
- 5. Which low-voltage series is fully electrically compatible with TTL?

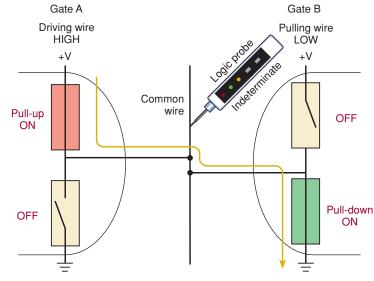
8-11 OPEN-COLLECTOR/OPEN-DRAIN OUTPUTS

Several digital devices must sometimes share the use of a single wire in order to transmit a signal to some destination device, very much like several neighbors sharing the same street. This means that several devices must have their outputs connected to the same wire, which essentially connects them all to each other. For all of the logic devices we have considered so far, this presents a problem. Each output has two states, HIGH and LOW. When one output is HIGH while the other is LOW and when they are connected together, we have a HIGH/LOW conflict. Which one will win? Just like arm wrestling, the stronger of the two wins. In this case, the transistor circuit whose output transistor has the lowest "ON" resistance will pull the output voltage in its direction.

Figure 8-28 shows a generic block diagram of two logic devices with their outputs connected to a common wire. If the two logic devices were CMOS, then the ON resistance of the pull-up circuit that outputs the HIGH would be approximately the same as the ON resistance of the pull-down circuit that outputs the LOW. The voltage on the common wire will be about half the supply voltage. This voltage is in the indeterminate range for most CMOS series and is unacceptable for driving a CMOS input. Furthermore, the current through the two conducting MOSFETs will be much greater than normal, especially at higher values of V_{DD} , and it can damage the ICs.

Conventional CMOS outputs should never be connected together.

If the two devices were TTL totem-pole outputs, as shown in Figure 8-29, a similar situation would occur but with different results because of the



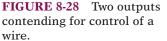
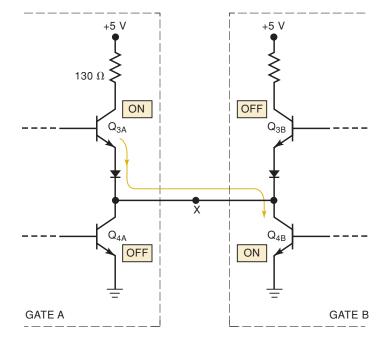


FIGURE 8-29 Totem-pole outputs tied together can produce harmful current through Q_4 .



difference in output circuitry. Suppose that gate *A* output is in the HIGH state (Q_{3A} ON, Q_{4A} OFF) and the gate *B* output is in the LOW state (Q_{3B} OFF, Q_{4B} ON). In this situation, Q_{4B} is a very low resistance load on Q_{3A} and will draw a current that is far greater than it is rated to handle. This current might not damage Q_{3A} or Q_{4B} immediately, but over a period of time it can cause overheating and deterioration in performance and eventual device failure.

Another problem caused by this relatively high current flowing through Q_{4B} is that it will produce a larger voltage drop across the transistor collector emitter, making V_{OL} of between 0.5 and 1 V. This is greater than the allowable V_{OL} (max). For these reasons:

TTL totem-pole outputs should never be tied together.

Open-Collector/Open-Drain Outputs

One solution to the problem of sharing a common wire among gates is to remove the active pull-up transistor from each gate's output circuit. In this way, none of the gates will ever try to assert a logic HIGH. TTL outputs that have been modified in this way are called **open-collector outputs**. CMOS output circuits that have been modified in this way are called open-drain outputs. The output is taken at the drain of the N-channel pull-down MOSFET, which is an open circuit (i.e., not connected to any other circuitry).

The TTL equivalent is called an open-collector output because the collector of the bottom transistor in the totem pole is connected directly to the output pin and nowhere else, as shown in Figure 8-30(a). The open-collector structure eliminates the pull-up transistors Q_3 , D_1 , and R_4 . In the output LOW state, Q_4 is ON (has base current and is essentially a short between collector and emitter); in the output HIGH state, Q_4 is OFF (has no base current and is essentially an open between collector and emitter). Because this circuit has no internal way to pull the output HIGH, the circuit designer must connect an external pull-up resistor R_P to the output, as shown in Figure 8-30(b).

When Q_4 is ON, it pulls the output voltage down to a LOW. When Q_4 is OFF, R_P pulls the output of the gate HIGH. Note that without the pull-up resistor, the output voltage would be indeterminate (floating). The value of the resistor

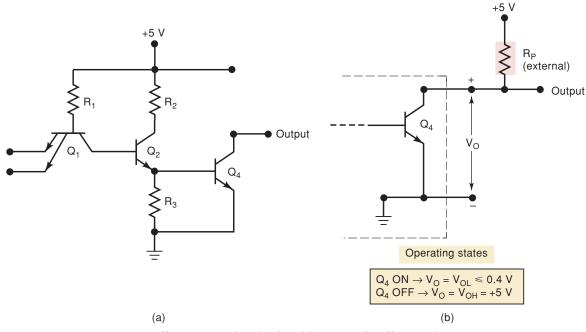
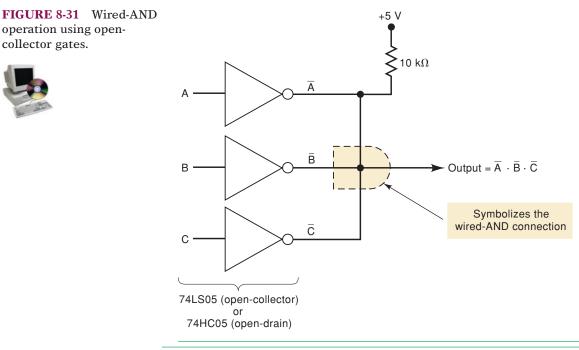


FIGURE 8-30 (a) Open-collector TTL circuit; (b) with external pull-up resistor.

 $R_{\rm P}$ is usually chosen to be 10 k Ω . This value is small enough so that, in the HIGH state, the voltage dropped across it due to load current will not lower the output voltage below the minimum $V_{\rm OH}$. It is large enough so that, in the LOW state, it will limit the current through Q_4 to a value below $I_{OL}(max)$.

When several open-collector or open-drain gates share a common connection, as shown in Figure 8-31, the common wire is HIGH by default due to the pull-up resistor. When any one (or more) of the gate outputs pulls it LOW, the 5 V are dropped across $R_{\rm P}$ and the common connection is in the LOW





state. Because the common output is HIGH only when all the outputs are in the HIGH state, connecting the outputs in this way essentially implements the logic AND function. This is called a **wired-AND** connection. This is shown symbolically by the dotted AND gate symbol. There is no actual AND gate there. A wired-AND can be implemented only with open-collector TTL and opendrain CMOS logic devices.

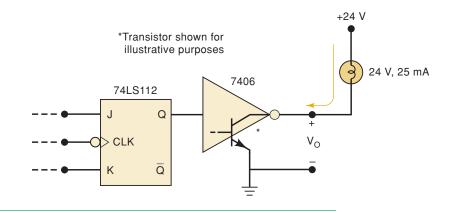
To summarize, the open-collector/open-drain circuits cannot actively make their outputs HIGH; they can only pull them LOW. This feature can be used to allow several devices to share the same wire for transmitting a logic level to another device or to combine the outputs of the devices effectively in a logic AND function. As we mentioned before, the purpose of the active pull-up transistor in the output circuit of conventional gates is to charge up the load capacitance rapidly and allow for fast switching. Open-collector and open-drain devices have a much slower switching speed from LOW to HIGH and consequently are not used in high-speed applications.

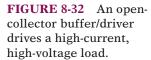
Open-Collector/Open-Drain Buffer/Drivers

The applications of open-collector/drain outputs that we have described were more prevalent in the early days of logic circuits than they are today. A more common use of these circuits now is as a **buffer/driver**. A buffer or a driver is a logic circuit that is designed to have a greater output current and/or voltage capability than an ordinary logic circuit. They allow a weaker output circuit to drive a heavy load. Open-collector/drain circuits offer some unique flexibility as buffer/drivers.

Due to their high $I_{\rm OL}$ and $V_{\rm OH}$ specifications, the 7406 and 7407 are the only standard TTL devices that are still being recommended for new designs. The 7406 is an open-collector buffer/driver IC that contains six INVERTERs with open-collector outputs that can sink up to 40 mA in the LOW state. In addition, the 7406 can handle output voltages up to 30 V in the HIGH state. This means that the output can be connected to a load that operates on a voltage greater than 5 V. This is illustrated in Figure 8-32, where a 7406 is used as a buffer between a 74LS112 flip-flop and an incandescent indicator lamp that is rated at 24 V, 25 mA. The 7406 controls the lamp's ON/OFF status to indicate the state of FF output *Q*. Note that the lamp is powered from +24 V, and it acts as the pull-up resistor for the open-collector output.

When Q = 1, the 7406 output goes LOW, its output transistor sinks the 25 mA of lamp current supplied by the 24-V source, and the lamp is on. When



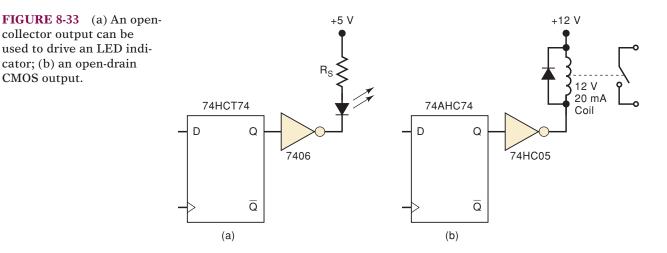


Q = 0, the 7406 output transistor turns off; there is no path for current, and the lamp turns off. In this state, the full 24 V will appear across the OFF output transistor so that $V_{\rm OH} = 24$ V, which is lower than the 7406 maximum $V_{\rm OH}$ rating.

Open-collector outputs are often used to drive indicator LEDs, as shown in Figure 8-33(a). The resistor is used to limit the current to a safe value. When the INVERTER output is LOW, its output transistor provides a lowresistance path to ground for the LED current, so that the LED is on. When the INVERTER output is HIGH, its output transistor is off, and there is no path for LED current; in this state, the LED is off.

The 7407 is an open-collector, noninverting buffer with the same voltage and current ratings as a 7406.

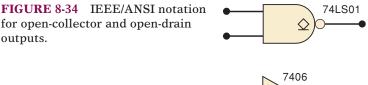
The 74HC05 is an open-drain hex inverter with 25 mA current sink capability. Figure 8-33(b) shows a way to interface a 74AHC74 D-FF to a control relay. A control relay is an electromagnetic switch. The contacts close magnetically when the rated current flows through the coil. The 74HC05 can handle the relay's relatively high voltage and current so that the 74AHC74 output can turn the relay on and off.



CMOS output.

IEEE/ANSI Symbol for Open-Collector/Drain Outputs

The new IEEE/ANSI symbology uses a distinctive notation to identify opencollector/drain outputs. Figure 8-34 shows the standard IEEE/ANSI designation for an open-collector/drain output. It is an underlined diamond. Although we will not normally use the complete IEEE/ANSI symbology in this book, we will use this underlined diamond to indicate open-collector and open-drain outputs.





REVIEW QUESTIONS	1. When does a HIGH/LOW conflict occur?
	2. Why shouldn't totem-pole outputs be tied together?
	3. How do open-collector outputs differ from totem-pole outputs?
	4. Why do open-collector outputs need a pull-up resistor?
	5. What is the logic expression for the wired-AND connection of six 7406 outputs?
	6. Why are open-collector outputs generally slower than totem-pole outputs?
	7. What is the IEEE/ANSI symbol for open-collector outputs?

8-12 TRISTATE (THREE-STATE) LOGIC OUTPUTS

The tristate configuration is a third type of output circuitry used in TTL and CMOS families. It takes advantage of the high-speed operation of the pullup/pull-down output arrangement, while allowing outputs to be connected together to share a common wire. It is called tristate because it allows three possible output states: HIGH, LOW, and high-impedance (Hi-Z). The Hi-Z state is a condition in which both the pull-up and the pull-down transistors are turned OFF so that the output terminal is a high impedance to both ground and the power supply +V. Figure 8-35 illustrates these three states for a simple inverter circuit.

Devices with tristate outputs have an *enable* input. It is often labeled E for enable or OE for output enable. When OE = 1, as shown in Figures 8-35(a) and (b), the circuit operates as a normal INVERTER because the HIGH logic level at OE enables the output. The output will be either HIGH or LOW, depending on the input level. When OE = 0, as shown in Figure 8-35(c), the circuit's output is *disabled*. It goes into its Hi-Z state with both transistors in the nonconducting state. In this state, the output terminal is essentially an open circuit (not connected to anything).

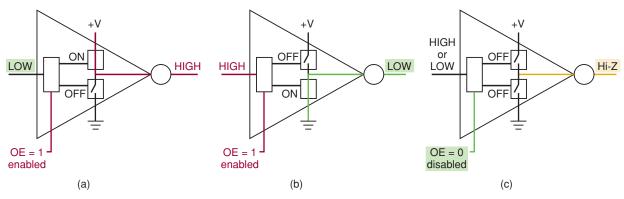


FIGURE 8-35 Three output conditions of tristate.

Advantage of Tristate

The outputs of tristate ICs can be connected together (share the use of a common wire) without sacrificing switching speed because a tristate output, when enabled, operates as a totem pole for TTL or an active pull-up/pull-down CMOS output with its associated low-impedance, high-speed characteristics. It is important to realize, however, that when tristate outputs are connected together, only one of them should be enabled at one time. Otherwise, two active outputs could fight for control of the common wire, as we discussed earlier, causing damaging currents to flow and producing invalid logic levels.

In our discussion of open-collector/open-drain and tristate circuits, we have referred to cases when the outputs of several devices must share a single wire to transmit information to another device. The shared wire is referred to as a bus wire. An entire bus is made up of several wires that are used to carry digital information between two or more devices that share the use of the bus.

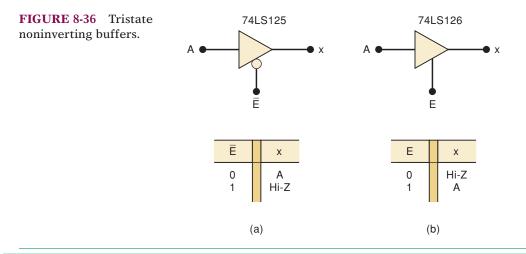
Tristate Buffers

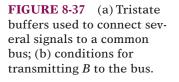
A *tristate buffer* is a circuit used to control the passage of a logic signal from input to output. Some tristate buffers also invert the signal as it goes through. The circuits in Figure 8-35 can be called *inverting tristate buffers*.

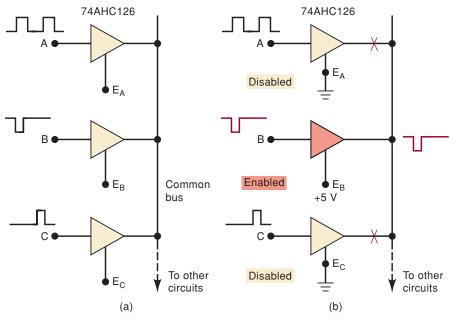
Two commonly used tristate buffer ICs are the 74LS125 and the 74LS126. Both contain four *noninverting* tristate buffers like those shown in Figure 8-36. The 74LS125 and 74LS126 differ only in the active state of their ENABLE inputs. The 74LS125 allows the input signal *A* to reach the output when $\overline{E} = 0$, while the 74LS126 passes the input when E = 1.

Tristate buffers have many applications in circuits where several signals are connected to common lines (buses). We will examine some of these applications in Chapter 9, but we can get the basic idea from Figure 8-37(a). Here, we have three logic signals *A*, *B*, and *C* connected to a common bus line through 74AHC126 tristate buffers. This arrangement permits us to transmit any one of these signals over the bus line to other circuits by enabling the appropriate buffer.

For example, consider the situation in Figure 8-37(b), where $E_B = 1$ and $E_A = E_C = 0$. This disables the upper and lower buffers so that their outputs are in the Hi-Z state and are essentially disconnected from the bus. This is symbolized by the X's on the diagram. The middle buffer is enabled so that its input, *B*, is passed through to its output and onto the bus, from which it is routed to other circuits connected to the bus. When tristate outputs are connected together as in Figure 8-37, it is important to remember that no more than one output should be enabled at one time. Otherwise, two or more active totem-pole outputs would be connected, which could



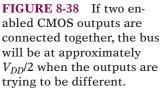


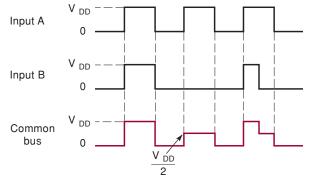


produce damaging currents. Even if damage did not occur, this situation would produce a signal on the bus that is a combination of more than one signal. This is commonly referred to as **bus contention**. Figure 8-38 shows the effect of enabling outputs *A* and *B* simultaneously. In Figure 8-37, when inputs *A* and *B* are in opposite states, they contend for control of the bus. The resulting voltage on the bus is an invalid logic state. In tristate bus systems, the designer must make sure that the enable signals do not allow bus contention to occur.

Tristate ICs

In addition to tristate buffers, many ICs are designed with tristate outputs. For example, the 74LS374 is an octal D-type FF register IC with tristate outputs. This means that it is an eight-bit register made up of D-type FFs whose outputs are connected to tristate buffers. This type of register can be connected to common bus lines along with the outputs from other, similar devices to allow efficient transfer of data over the bus. We examine this *tristate data bus* arrangement in Chapter 9. Other types of logic devices that are available with tristate outputs include decoders, multiplexers, analog-to-digital converters, memory chips, and microprocessors.

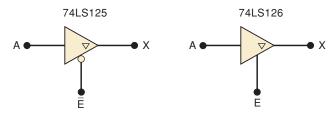




IEEE/ANSI Symbol for Tristate Outputs

The traditional logic symbology has no special notation for tristate outputs. Figure 8-39 shows the notation used in the IEEE/ANSI symbology to indicate a tristate output. It is a triangle that points downward. Although it is not part of the traditional symbology, we will use this triangle to designate tristate outputs throughout the remainder of the book.

FIGURE 8-39 IEEE/ANSI notation for tristate outputs.



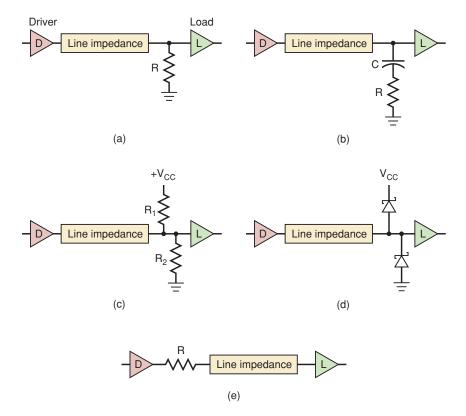
REVIEW QUESTIONS	1. What are the three possible states of a tristate output?
	2. What is the state of a tristate output when it is disabled?
	3. What is bus contention?
	4. What conditions are necessary to transmit signal <i>C</i> onto the bus in Figure 8-37?
	5. What is the IEEE/ANSI designation for tristate outputs?

8-13 HIGH-SPEED BUS INTERFACE LOGIC

Many digital systems use a shared bus to transfer digital signals and data between the various components of the system. As you can see from our discussion of CMOS technology development, systems are getting faster and faster. Many of the newer high-speed logic series are designed specifically to interface to a tristate bus system. The components in these series are primarily tristate buffers, bidirectional transceivers, latches, and high-current line drivers.

A significant distance often physically separates the components in these systems. If this distance is more than about 4 inches, the bus wires between them need to be viewed as a transmission line. Although transmission line theory could fill up a whole book and is beyond the scope of this text, the general idea is simple enough. Wires have inductance, capacitance, and resistance, which means that for changing signals (ac), they have a characteristic impedance that can affect a signal placed on one end and distort it by the time it reaches the other end. At the high speeds we are discussing, the travel time down the wire and the effects of reflected waves (like echoes) and ringing become real concerns. There are several ways to combat the problems associated with transmission lines. In order to prevent reflected pulse waves, the end of the bus must be terminated with a resistance that is equal to the line impedance (about 50 Ω), as shown in Figure 8-40(a). This method is not feasible because too much current is required to maintain logic level voltages across such a low resistance. Another technique uses a capacitor to block the dc current when the line is not changing, but effectively appears as just a resistor to the rising or falling pulse. This method is shown in Figure 8-40(b).

Using a voltage divider, as in Figure 8-40(c), with resistances larger than the line, impedance helps reduce reflections, but with hundreds of individual bus lines, it obviously makes a heavy load on the system power supply. The



diode termination shown in Figure 8-40(d) simply clips off or clamps the overshoot/undershoot of the ringing caused by the reactive LC nature of the line. Series termination at the source, as shown in Figure 8-40(e), slows down the switching speed, which reduces the frequency limits of the bus but substantially improves the reliability of the bus signals.

As you can see, none of these methods are ideal. IC manufacturers are designing new series of logic circuits that overcome many of these problems. Texas Instruments' bus interface logic series offers new output circuits that dynamically lower the output impedance during signal transition to provide fast transition times, then raises the impedance during the steady state (like a series termination) to damp any ringing and reduce reflections on the bus line. The GTLP (Gunning Transceiver Logic Plus) series of bus interface devices is specially designed to drive the relatively long buses that connect modules of a large digital system. The backplane refers to the interconnections between modules in the back of an industry standard, 19-inch rack mounting system.

Another major player in the high-speed bus-interface arena is known as **low-voltage differential signaling (LVDS)**. It uses two wires for each signal, and differential signaling means it responds to the difference between the two wires. Unwanted noise signals are usually present on both lines, and have no effect on the difference between the two. To represent the two logic states, LVDS uses a low voltage swing but switches polarity to clearly distinguish a 1 from a 0.

REVIEW QUESTIONS	1. How close together do components need to be to ignore "transmission
	line" effects?
	2. What three characteristics of real wires add up to distort signals that move through them?
	3. What is the purpose of bus terminations?

FIGURE 8-40 Bus termi-

nation techniques.

8-14 THE ECL DIGITAL IC FAMILY

The TTL family uses transistors operating in the saturated mode. As a result, their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation. Another *bipolar* logic family has been developed that prevents transistor saturation, thereby increasing overall switching speed. This logic family is called **emitter-coupled logic (ECL)**, and it operates on the principle of current switching whereby a fixed bias current less than $I_C(sat)$ is switched from one transistor's collector to another. Because of this current-mode operation, this logic form is also referred to as *current-mode logic* (CML).

Basic ECL Circuit

The basic circuit for emitter-coupled logic is essentially the differential amplifier configuration of Figure 8-41(a). The V_{EE} supply produces an essentially fixed current I_E , which remains around 3 mA during normal operation. This current is allowed to flow through either Q_1 or Q_2 , depending on the voltage level at V_{IN} . In other words, this current switches between Q_1 's collector and Q_2 's collector as V_{IN} switches between its two logic levels of -1.7 V (logical 0 for ECL) and -0.8 V (logical 1 for ECL). The table in Figure 8-41(a) shows the resulting output voltages for these two conditions at V_{IN} . Two important points should be noted: (1) V_{C1} and V_{C2} are the *complements* of each other, and (2) the output voltage levels are not the same as the input logic levels.

The second point noted above is easily taken care of by connecting V_{C1} and V_{C2} to emitter-follower stages (Q_3 and Q_4), as shown in Figure 8-41(b). The emitter followers perform two functions: (1) they subtract approximately 0.8 V from V_{C1} and V_{C2} to shift the output levels to the correct ECL logic levels; and (2) they provide a very low output impedance (typically 7 Ω), which provides for large fan-out and fast charging of load capacitance. This circuit produces two complementary outputs: V_{OUT1} , which is equal to $\overline{V_{IN}}$, and V_{OUT2} , which is equal to V_{IN} .

ECL OR/NOR Gate

The basic ECL circuit of Figure 8-41(b) can be used as an INVERTER if the output is taken at V_{OUT1} . This basic circuit can be expanded to more than one input by paralleling transistor Q_1 with other transistors for the other inputs, as in Figure 8-42(a). Here, either Q_1 or Q_3 can cause the current to be switched out of Q_2 , resulting in the two outputs V_{OUT1} and V_{OUT2} being the logical NOR and OR operations, respectively. This OR/NOR gate is symbolized in Figure 8-42(b) and is the fundamental ECL gate.

ECL Characteristics

The latest ECL series by Motorola is called ECLin PS. This stands for ECL in pico seconds. This logic series boasts a maximum gate propagation delay of 500 ps (that's half a nanosecond!) and FF toggle rates of 1.4 GHz. Some devices in this series have gate delays of only 100 ps at an average power of 5 mW. The following are the most important characteristics of the ECLin PS series of Motorola's MECL family of logic circuits:

1. The transistors never saturate, and so switching speed is very high. Typical propagation delay time is 360 ps, which makes ECL faster than any TTL or CMOS family members.

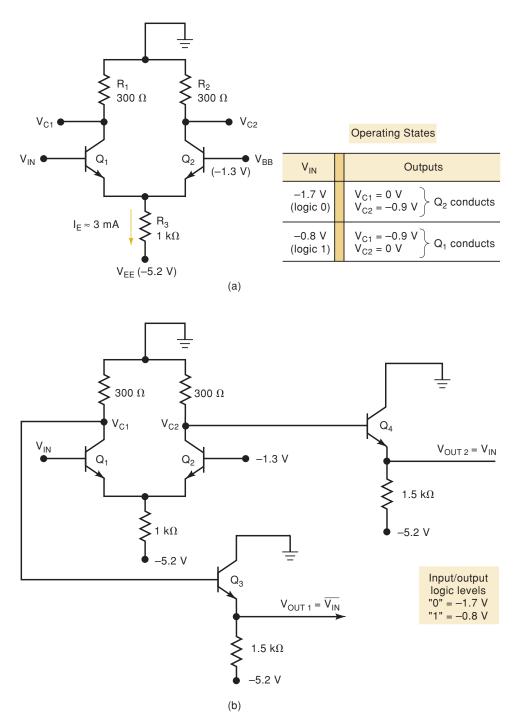


FIGURE 8-41 (a) Basic ECL circuit; (b) with addition of emitter followers.

- 2. The logic levels are nominally -0.8 V and -1.7 V for the logical 1 and 0, respectively. ECLin PS is fully voltage-compatible with former series of ECL.
- 3. Worst-case ECL noise margins are approximately 150 mV. These low noise margins make ECL somewhat unreliable for use in heavy industrial environments.
- 4. An ECL logic block usually produces an output and its complement. This eliminates the need for inverters. High current complementary drive

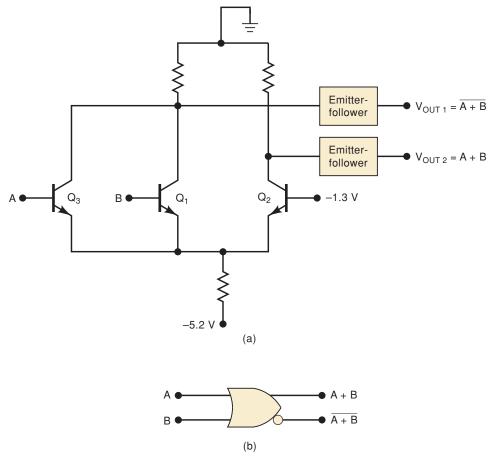


FIGURE 8-42 (a) ECL NOR/OR circuit; (b) logic symbol.

also makes ECL an excellent line driver for twisted-pair cable (such as telephone wires).

- 5. Fan-out is typically around 25, owing to the low-impedance emitter-follower outputs.
- 6. Typical power dissipation is 25 mW, somewhat higher than the 74AS series.
- 7. The total current flow in an ECL circuit remains relatively constant, regardless of its logic state. This helps to maintain an unvarying current drain on the power supply even during switching transitions. Thus, no noise spikes will be generated internally, like those produced by TTL and CMOS switching.

Table 8-11 shows how ECL compares with the important TTL logic families. The ECL family of ICs does not include a wide range of generalpurpose logic devices, as do the TTL and CMOS families. ECL does include complex, special-purpose ICs used in applications such as high-speed data transmission, high-speed memories, and high-speed arithmetic units. The relatively low noise margins and high power drain of ECL are disadvantages compared with TTL and CMOS. Another drawback is its negative powersupply voltage and logic levels, which are not compatible with those of the other logic families. This makes it difficult to use ECL devices in conjunction with TTL and/or CMOS ICs; special level-shifting circuits must be connected between ECL devices and the TTL (or CMOS) devices on both input and output.

Logic Family	t _{pd} (ns)	<i>P</i> _D (mW) <100 kHz	Worst-Case Noise Margin (mV)	Maximum Clock Rate (MHz)
74AS	1.7	8	300	200
74F	3.8	6	300	100
74AHC	3.7	0.006	550	130
74AVC	2	0.006	250	*
74ALVT	2.4	0.33	400	*
74ALB	2.2	1	400	*
ECL	0.3	25	150	1400

TADE TO 44	TT' 1 11 '	
TABLE 8-11	High-speed logic	comparison.

*Flip-flops not available in this series.

REVIEW QUESTIONS

1. *True or false:*

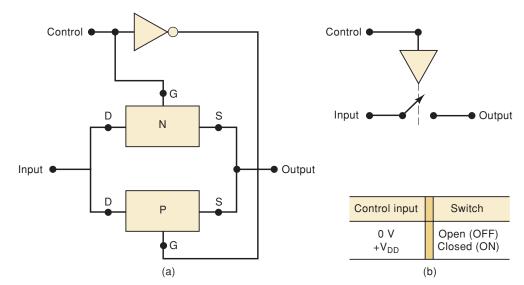
- (a) ECL obtains high-speed operation by preventing transistor saturation.
- (b) ECL circuits usually have complementary outputs.
- (c) The noise margins for ECL circuits are larger than TTL noise margins.
- (d) ECL circuits do not generate noise spikes during state transitions.
- (e) ECL devices require less power than standard TTL.
- (f) ECL can easily be used with TTL.

8-15 CMOS TRANSMISSION GATE (BILATERAL SWITCH)

A special CMOS circuit that has no TTL or ECL counterpart is the **transmission gate** or **bilateral switch**, which acts essentially as a single-pole, single-throw switch controlled by an input logic level. This transmission gate passes signals in both directions and is useful for digital and analog applications.

Figure 8-43(a) is the basic arrangement for the bilateral switch. It consists of a P-MOSFET and an N-MOSFET in parallel so that both polarities of input voltage can be switched. The CONTROL input and its inverse are used to turn the switch on (closed) and off (open). When the CONTROL is HIGH, both MOSFETs are turned on and the switch is closed. When CONTROL is LOW, both MOSFETs are turned off and the switch is open. Ideally, this circuit operates like an electromechanical relay. In practice, however, it is not a perfect short circuit when the switch is closed; the switch resistance R_{ON} is typically 200 Ω . In the open state, the switch resistance is very large, typically 10¹² Ω , which for most purposes is an open circuit. The symbol in Figure 8-43(b) is used to represent the bilateral switch.

This circuit is called a *bilateral* switch because the input and output terminals can be interchanged. The signals applied to the switch input can be either digital or analog signals, provided that they stay within the limits of 0 to V_{DD} volts.



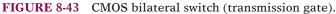
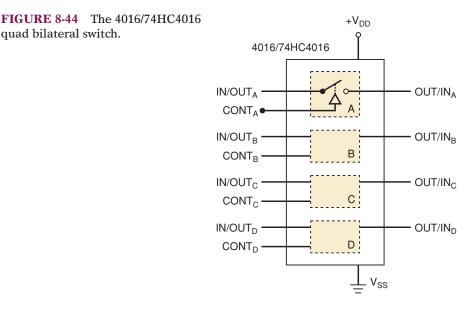


Figure 8-44(a) shows the traditional logic diagram for a 4016 quad bilateral switch IC, which is also available in the 74HC series as a 74HC4016. The IC contains four bilateral switches that operate as described above. Each switch is independently controlled by its own control input. For example, the ON/OFF status of the top switch is controlled by input $CONT_A$. Because the switches are bidirectional, either switch terminal can serve as input or output, as the labeling indicates.



EXAMPLE 8-12

Describe the operation of the circuit in Figure 8-45.

Solution

Here, two of the bilateral switches are connected so that a common analog input signal can be switched to either output X or output Y, depending on the logic state of the OUTPUT SELECT input. When OUTPUT SELECT is LOW, the upper switch is closed and the lower one is open so that V_{IN} is connected

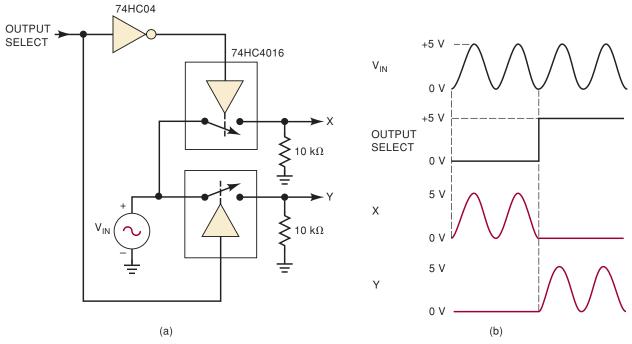


FIGURE 8-45 Example 8-12: 74HC4016 bilateral switches used to switch an analog signal to two different outputs.

to output X. When OUTPUT SELECT is HIGH, the upper switch is open and the lower one is closed so that $V_{\rm IN}$ is connected to output Y. Figure 8-45(b) shows some typical waveforms. Note that for proper operation, $V_{\rm IN}$ must be within the range 0 V to $+V_{DD}$.

The 4016/74HC4016 bilateral switch can switch only input voltages that lie between 0 V and V_{DD} , and so it could not be used for signals that were both positive and negative relative to ground. The 4316 and 74HC4316 ICs are quad bilateral switches that can switch *bipolar* analog signals. These devices have a second power-supply terminal called V_{EE} , which can be made negative with respect to ground. This permits input signals that can range from V_{EE} to V_{DD} . For example, with $V_{EE} = -5$ V and $V_{DD} = +5$ V, the analog input signal can be anywhere from -5 V to +5 V.

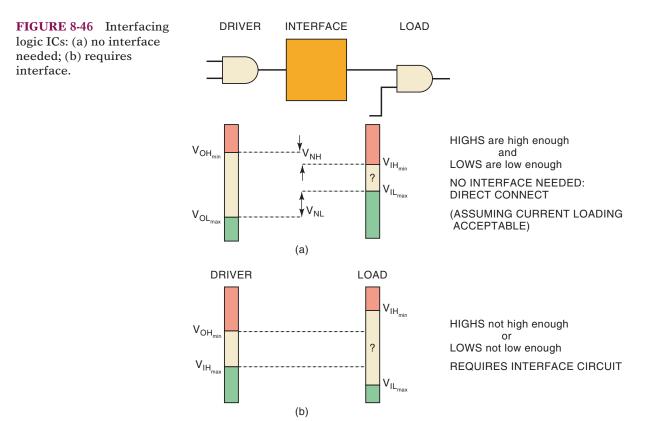
REVIEW QUESTIONS

1. Describe the operation of a CMOS bilateral switch.

2. True or false: There is no TTL bilateral switch.

8-16 IC INTERFACING

Interfacing means connecting the output(s) of one circuit or system to the input(s) of another circuit or system that has different electrical characteristics. Often a direct connection cannot be made because of the difference in the electrical characteristics of the *driver* circuit that is providing the output signal and the *load* circuit that is receiving the signal. An interface circuit is connected between the driver and the load as shown in Figure 8-46. Its function is to take the driver output signal and condition it so that it is compatible with



the requirements of the load. In digital systems this is pretty simple, because each device is either on or off. The interface must ensure that when the driver outputs a HIGH, the load receives a signal it perceives to be HIGH; *and*, when the driver outputs a LOW, the load receives a signal it perceives to be LOW.

The simplest and most desirable interface circuit between a driver and a load is a direct connection. Of course, devices that are in the same series are designed to interface directly with each other. Today, however, many systems involve mixed families, mixed voltages, and mixed series. In these systems the challenge is to make sure that the driver is able to consistently activate the load in both the LOW and HIGH states.

For any case such as shown in Figure 8-46(a), where V_{OH} of the driver is enough greater than the $V_{OH}(\min)$ of the load and V_{OL} of the driver is enough less than the $V_{IL}(\max)$ of the load, there is no need for an interface circuit other than a direct connection. "How much greater?" and "How much less?" are questions related to how much noise is expected in the system. Recall that the noise margins (V_{NH} and V_{NL}) are measures of this difference between output and input characteristics. (Refer back to Figure 8-4.) The minimum acceptable noise margin for any system is a judgment call that must be made by the system designer. Whenever the V_{NH} or V_{NL} is determined to be too small (or even negative), then an interface circuit is necessary in order to ensure that the driver and load can work together. This situation is depicted in Figure 8-46(b) To summarize this:

Driver	Load
$V_{\rm OH}({\rm min})$	$> V_{\rm IH}({ m min}) + V_{ m NH}$
$V_{\rm OL}({\rm max}) + V_{\rm NL}$	$< V_{\rm IL}({\rm max})$

We should also note that, especially when using older families, the current (as opposed to voltage) characteristics of the driver and load must also match. The $I_{\rm OH}$ of the driver must be able to source enough current to supply the necessary $I_{\rm IH}$ of the load, and the $I_{\rm OL}$ of the driver must be able to sink enough current to accommodate the $I_{\rm IL}$ from the load. This topic was covered in Section 8-5 when we discussed fan-out. Most modern logic devices have high enough output drive and low enough input current to make loading a rare problem. However, this is very important when interfacing to external input/output devices such as motors, lights, or heaters. To summarize current loading requirements:

Driver	Load
I _{OH} (max)	$> I_{\rm IH}({\rm total})$
I _{OL} (max)	$> I_{\rm IL}({\rm total})$

Table 8-12 lists some nominal values for a number of different families and series of digital devices. Within each family there will be exceptions to these listed values, and so in practice it is important that you look up the data sheet values for the specific ICs you are working with. For the sake of convenience we will use these values in the examples that follow.

Interfacing 5-V TTL and CMOS

When interfacing different types of ICs, we must check that the driving device can meet the current and voltage requirements of the load device. Examination of Table 8-12 indicates that the input current values for CMOS are extremely low compared with the output current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.

There is a problem, however, when we compare the TTL output voltages with the CMOS input voltage requirements. Table 8-9 shows that $V_{OH}(min)$ of every TTL series is too low when compared with the $V_{IH}(min)$ requirement of the 4000B, 74HC, and 74AC series. For these situations, something must be done to raise the TTL output voltage to an acceptable level for CMOS.

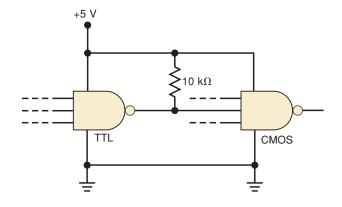
The most common solution to this interface problem is shown in Figure 8-47, where the TTL output is connected to +5 V with a pull-up resistor. The presence of the pull-up resistor causes the TTL output to rise to approximately 5 V in the HIGH state, thereby providing an adequate CMOS input voltage level. This pull-up resistor is not required if the CMOS device is a 74HCT or a 74ACT because these series are designed to accept TTL outputs directly, as Table 8-9 shows.

 TABLE 8-12
 Input/output currents for standard devices with a supply voltage of 5 V.

CMOS							TTL		
Parameter	4000B	74HC/HCT	74AC/ACT	74AHC/AHCT	74	74LS	74AS	74ALS	74F
l _{IH} (max)	1 µA	1 µA	1 µA	1 µA	40 A	20 µA	20 µA	20 µA	20 µA
l _{IL} (max)	1 μA	1 µA	1 µA	1 µA	1.6 mA	0.4 mA	0.5 mA	100 μA	0.6 mA
I _{OH} (max)	0.4 mA	4 mA	24 mA	8 mA	0.4 mA	0.4 mA	2 mA	400 mA	1.0 mA
I _{OL} (max)	0.4 mA	4 mA	24 mA	8 mA	16 mA	8 mA	20 mA	8 mA	20 mA

FIGURE 8-47 External pull-up resistor is used when TTL drives CMOS.





CMOS Driving TTL

Before we consider the problem of interfacing CMOS outputs to TTL inputs, it will be helpful to review the CMOS output characteristics for the two logic states. Figure 8-48(a) shows the equivalent output circuit in the HIGH state. The $R_{\rm ON}$ of the P-MOSFET connects the output terminal to V_{DD} (remember, the N-MOSFET is off). Thus, the CMOS output circuit acts like a V_{DD} source with a source resistance of $R_{\rm ON}$. The value of $R_{\rm ON}$ typically ranges from 100 to 1000 Ω .

Figure 8-48(b) shows the equivalent output circuit in the LOW state. The R_{ON} of the N-MOSFET connects the output terminal to ground (remember, the P-MOSFET is off). Thus, the CMOS output acts as a low resistance to ground; that is, it acts as a current sink.

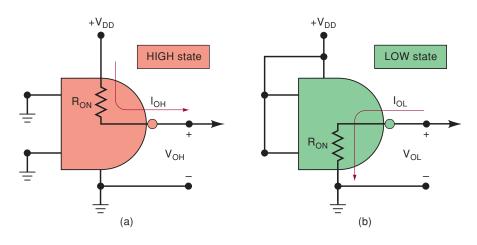


FIGURE 8-48 Equivalent CMOS output circuits for both logic states.

CMOS Driving TTL in the HIGH State

Table 8-9 shows that CMOS outputs can easily supply enough voltage ($V_{\rm OH}$) to satisfy the TTL input requirement in the HIGH state ($V_{\rm IH}$). Table 8-12 shows that CMOS outputs can supply more than enough current ($I_{\rm OH}$) to meet the TTL input current requirements ($I_{\rm IH}$). Thus, no special consideration is needed for the HIGH state.

CMOS Driving TTL in the LOW State

Table 8-12 shows that TTL inputs have a relatively high input current in the LOW state, ranging from 100 μ A to 2 mA. The 74HC and 74HCT series can sink up to 4 mA, and so they would have no trouble driving a *single* TTL load of any series. The 4000B series, however, is much more limited. Its low I_{OL} capability is not sufficient to drive even one input of the 74 or 74AS series. The 74AHC series has output drive comparable to that of the 74LS series.

74HC125

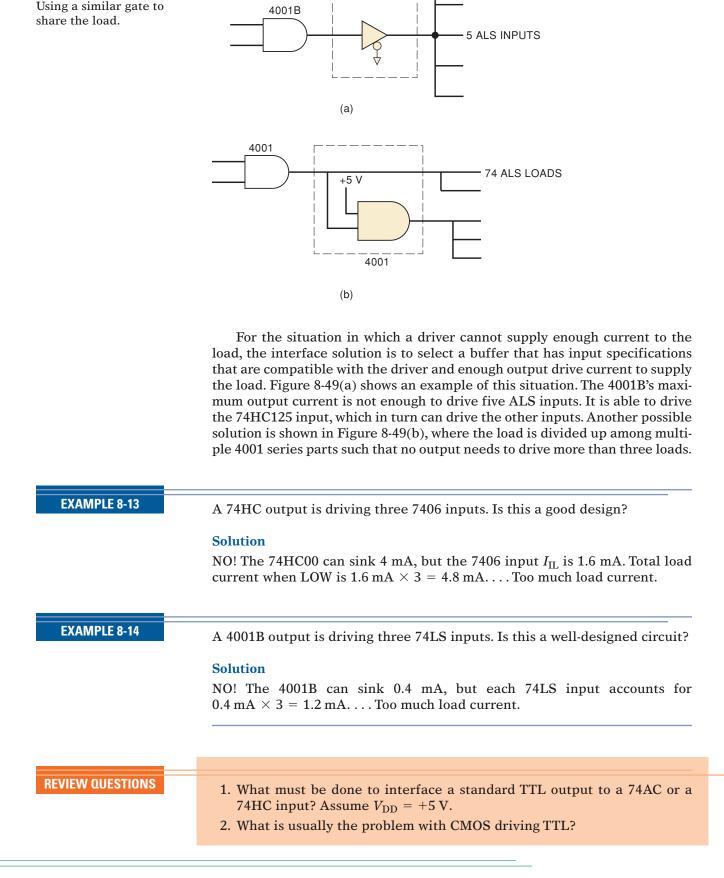


FIGURE 8-49 (a) Using an

HC series interface IC. (b)

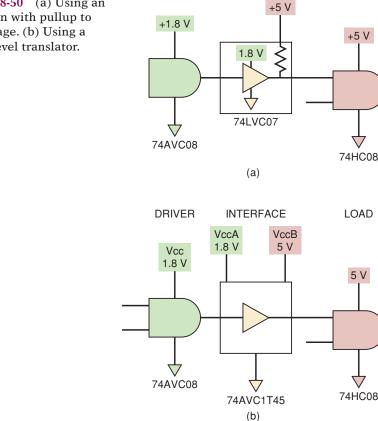
MIXED-VOLTAGE INTERFACING 8-17

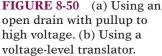
As we discussed in Section 8-10, many new logic devices operate on less than 5 V. In many situations, these devices need to communicate with each other. In this section we will look specifically at how to interface logic devices that operate on different voltage standards.

Low-Voltage Outputs Driving High-Voltage Loads

In some situations, the V_{OH} of the driver is just slightly lower than the load requires to recognize it as a HIGH. This situation was discussed when interfacing TTL outputs to 5-V CMOS inputs. The only interface component needed was a 10-k Ω pull-up resistor, which will cause the TTL output voltage to be boosted above the 3.3-V level when the output is HIGH.

When there is a need for a more substantial shift in voltage because the driver and load operate on different power supply voltages, a voltage-level translator interface circuit is required. An example of this is a low-voltage (1.8-V) CMOS device driving a 5-V CMOS input. The driver can put out a maximum of only 1.8 V as a HIGH, and the load gate requires 3.33V for a HIGH. We need an interface that can accept 1.8-V logic levels and translate them to 5-V CMOS levels. The simplest way to accomplish this is with a buffer that has an open drain, such as the 74LVC07 shown in Figure 8-50(a). Notice that the pull-up resistor is connected to the 5-V supply, while the power supply for the interface buffer is 1.8 V. Another solution is to utilize a dual-supply-level translator circuit such as the 74AVC1T45, as shown in Figure 8-50(b). This device uses two different power supply voltages, one for the inputs and the other for the outputs, and translates between the two levels.

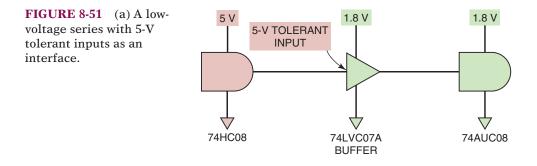




High-Voltage Outputs Driving Low-Voltage Loads

When logic circuits that operate on a higher voltage supply must drive other logic circuits that operate on a lower voltage supply, the output voltage of the driver often exceeds the safe limits that the load gate can handle. In these situations, a dual-supply-voltage-level translator can be used just as it was in Figure 8-50(b). Another common solution to this problem is to interface them using a buffer from a series that can withstand the higher input voltage. Figure 8-51 demonstrates this with a 5-V CMOS part driving a 1.8-V AUC series input. The highest voltage the AUC input (load gate) can handle is 3.6 V. However, a 74LVC07A can handle up to 5.5 V on its input without damaging it, even though it is operating on 1.8 V. Figure 8-51 shows how we can use the higher voltage tolerance of the 74LVC07A to translate a 5-V logic level down to a 1.8-V logic level.

At this point you may be wondering, "Why in the world would anyone choose to use such an assortment of incompatible parts?" The answer lies in considering larger systems and trying to balance performance and cost. In a computer system, for example, you may have a 2.5-V CPU, a 3.3-V memory module, and a 5-V hard drive controller all working on the same mother board. The low-voltage components may be necessary to obtain the desired performance, but the 5-V hard drive may be the least expensive or the only type available. The driver and load devices may not be standard logic gates at all, but may be a VLSI component in our system. Using the data sheet for those devices, we must look up the output characteristics and interface them using the techniques we have shown. As logic standards continue to evolve, it is important that we can make systems work using any of the diverse components available to us.



REVIEW QUESTIONS

- 1. What is the function of an *interface* circuit?
- 2. True or false: All CMOS outputs can drive TTL in the HIGH state.
- 3. True or false: Any CMOS output can drive any single TTL input.
- 4. Which CMOS series can TTL drive without a pull-up resistor?
- 5. How many 7400 inputs can be driven from a 74HCT00 output?

8-18 ANALOG VOLTAGE COMPARATORS

Another very useful device for interfacing to digital systems is the **analog voltage comparator**. It is especially useful in systems that contain both analog voltages as well as digital components. An analog voltage comparator

compares two voltages. If the voltage on the (+) input is greater than the voltage on the (-) input, the output is HIGH. If the voltage on the (-) input is greater than the voltage on the (+) input, the output is LOW. The inputs to a comparator can be thought of as analog inputs, but the output is digital because it will always be either HIGH or LOW. For this reason, the comparator is often referred to as a one-bit analog-to-digital (A/D) converter. We will examine A/D converters in detail in Chapter 10.

An LM339 is an analog linear IC that contains four voltage comparators. The output of each comparator is an open-collector transistor just like an open-collector TTL output. V_{CC} can range from 2 to 36 V but is usually set slightly greater than the analog input voltages that are being compared. A pull-up resistor must be connected from the output to the same supply that the digital circuits use (normally 5 V).

EXAMPLE 8-15

Suppose that an incubator must have an emergency alarm to warn if the temperature exceeds a dangerous level. The temperature-measuring device is an LM34 that puts out a voltage directly proportional to the temperature. The output voltage goes up 10 mV per degree F. The digital system alarm must sound when the temperature exceeds 100°F. Design a circuit to interface the temperature sensor to the digital circuit.

Solution

We need to compare the voltage from the sensor with a fixed threshold voltage. First, we must calculate the proper threshold voltage. We want the comparator output to go HIGH when the temperature exceeds 100°F. The voltage out of the LM34 at 100°F will be

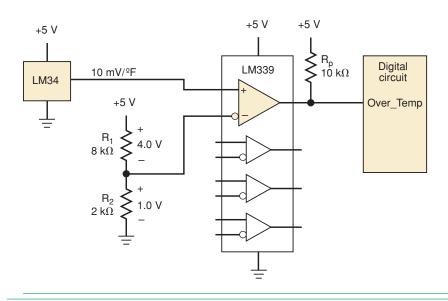
$$100^{\circ}F \cdot 10 \text{ mV/}^{\circ}F = 1.0 \text{ V}$$

This means that we must set the (-) input pin of the comparator to 1.0 V and connect the LM34 to the (+) input. In order to create a 1.0-V reference voltage, we can use a voltage-divider circuit and choose a bias current of $100 \,\mu\text{A}$. The LM339 input current will be relatively negligible because it will draw less than $1 \,\mu\text{A}$. This means that $R_1 + R_2$ must total $10 \,\text{k}\Omega$. In this example, we can operate everything from a $+5 \,\text{V}$ power supply. Figure 8-52 shows the



temperature-limit detector using an LM339 analog voltage comparator.





complete circuit. The calculations are as follows:

$$V_{R2} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$R_2 = V_{R2} \cdot (R_1 + R_2) / V_{CC}$$

= 1.0 V(10 kΩ)/5 V = 2 kΩ

$$R_1 = 10 k\Omega - R_2 = 10 k\Omega - 2 k\Omega = 8 k\Omega$$

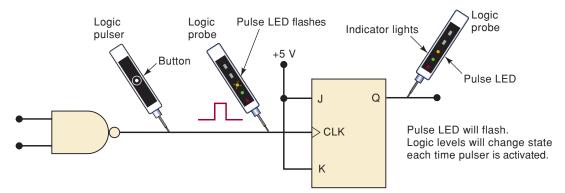
REVIEW QUESTIONS

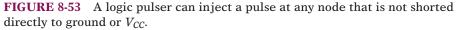
- 1. What causes the output of a comparator to go to the HIGH logic state?
- 2. What causes the output of a comparator to go to the LOW logic state?
- 3. Is an LM339 output more similar to a TTL totem-pole or an open-collector output?

8-19 TROUBLESHOOTING

A **logic pulser** is a testing and troubleshooting tool that generates a shortduration pulse when manually actuated, usually by pressing a push button. The logic pulser shown in Figure 8-53 has a needle-shaped tip that is touched to the circuit node that is to be pulsed. The logic pulser is designed so that it senses the existing voltage level at the node and produces a voltage pulse in the opposite direction. In other words, if the node is LOW, the logic pulser produces a narrow positive-going pulse; if the node is HIGH, it produces a narrow negative-going pulse.

The logic pulser is used to change the logic level at a circuit node momentarily, even though the output of another device may be connected to that same node. In Figure 8-53, the logic pulser is contacting node X, which is also connected to the output of the NAND gate. The logic pulser has a very low output impedance (typically 2 Ω or less), so that it can overcome the NAND gate's output and can change the voltage at the node. The logic pulser, however, cannot produce a voltage pulse at a node that is shorted directly to ground or V_{CC} (e.g., through a solder bridge).



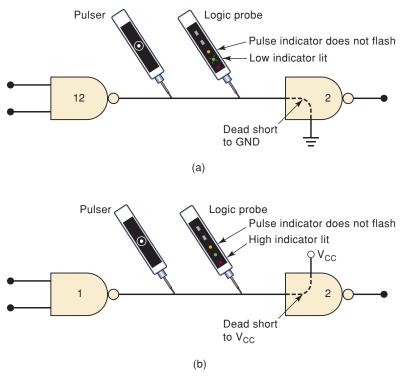


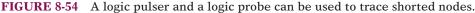
Using a Logic Pulser and Probe to Test a Circuit

A logic pulser can be used to inject a pulse or a series of pulses manually into a circuit in order to test the circuit's response. A logic probe is almost always used to monitor the circuit's response to the logic pulser. In Figure 8-53, the J-K flip-flop's toggle operation is being tested by applying pulses from the logic pulser and monitoring Q with the logic probe. This logic pulser/logic probe combination is very useful for checking the operation of a logic device while it is wired into a circuit. Note that the logic pulser is applied to the circuit node *without* disconnecting the output of the NAND gate that is driving that node. When the probe is placed on the same node as the pulser, the logic level indicators appear to remain unchanged (LOW in this example), but the yellow pulse indicator flashes once each time the pulser button is pressed. When the probe is placed on the Q output, the pulse LED flashes once (indicating a transition), and the logic level indicators change state each time the pulser button is pushed.

Finding Shorted Nodes

The logic pulser and logic probe can be used to check for nodes that are shorted directly to ground or V_{CC} , as shown in Figure 8-54. When you touch a logic pulser and a logic probe to the same node and press the logic pulser button, the logic probe should indicate the occurrence of a pulse at the node. If the probe indicates a constant LOW and the pulse LED does not flash, the node is shorted to ground, as shown in Figure 8-54(a). If the probe indicates a constant HIGH and the pulse LED does not flash, the node is shorted to V_{CC} as shown in Figure 8-54(b).





REVIEW QUESTIONS	1. What is the function of a logic pulser?
	2. <i>True or false:</i> A logic pulser will produce a voltage pulse at any node.
	3. <i>True or false:</i> A logic pulser can force a node LOW or HIGH for extended
	periods of time.

4. How does a logic probe respond to the logic pulser?

SUMMARY

- 1. All digital logic devices are similar in nature but very much different regarding the details of their characteristics. An understanding of the terms used to describe these characteristics is important and allows us to compare and contrast the performance of devices. By understanding the capabilities and limitations of each type of device, we can intelligently combine devices to take advantage of each device's strengths in building reliable digital systems.
- 2. The TTL family of logic devices has been in use for over 30 years. The circuitry uses bipolar transistors. This family offers many SSI logic gates, and MSI devices. Numerous series of similarly numbered devices have been developed because advances in technology have offered improved characteristics.
- 3. When you are connecting devices together, it is vital to know how many inputs a given output can drive without compromising reliability. This is referred to as *fan-out*.
- 4. Open-collector and open-drain outputs can be wired together to implement a wired-AND function. Tristate outputs can be wired together to allow numerous devices to share a common data path known as a *bus*. In such a case, only one device is allowed to assert a logic level on the bus (i.e., drive the bus) at any one time.
- 5. The *fastest* logic devices are from a family that uses emitter-coupled logic (ECL). This technology also uses bipolar transistors but is not as widely used as TTL due to inconvenient input/output characteristics.
- 6. MOSFET transistors can also be used to implement logic functions. The main advantage of MOS logic is lower power and greater packing density.
- 7. The use of complementary MOSFETs has produced CMOS logic families. CMOS technology has captured the market due to its very low power and competitive speed.
- 8. The ongoing need to reduce power and size has led to several new series of devices that operate on 3.3 V and 2.5 V.
- 9. Logic devices that use various technologies cannot always be directly connected together and operate reliably. The voltage and current characteristics of inputs and outputs must be considered and precautions taken to ensure proper operation.
- 10. CMOS technology allows a digital system to control analog switches called *transmission gates*. These devices can pass or block an analog signal, depending on the digital logic level that controls it.
- 11. Analog voltage comparators offer another bridge between analog signals and digital systems. These devices compare analog voltages and output a digital logic level based on which voltage is greater. They allow an analog system to control a digital system.

IMPORTANT TERMS

PROBLEMS

SECTIONS 8-1 TO 8-3

B 8-1.*Two different logic circuits have the characteristics shown in Table 8-13.

- (a) Which circuit has the best LOW-state dc noise immunity? The best HIGH-state dc noise immunity?
- (b) Which circuit can operate at higher frequencies?
- (c) Which circuit draws the most supply current?

TABLE 8-13

	Circuit A	Circuit B
V _{supply} (V)	6	5
V _{IH} (min) (V)	1.6	1.8
V _{IL} (max) (V)	0.9	0.7
V _{OH} (min) (V)	2.2	2.5
V _{OL} (max) (V)	0.4	0.3
t _{PLH} (ns)	10	18
t _{PHL} (ns)	8	14
P _D (mW)	16	10

- **B** 8-2. Look up the IC data sheets, and use *maximum* values to determine $P_{\rm D}(\text{avg})$ and $t_{\rm pd}(\text{avg})$ for one gate on each of the following TTL ICs. (See Example 8-2 in Section 8-3.)
 - (a)*7432
 (b)*74S32
 (c) 74LS20
 (d) 74ALS20
 (e) 74AS20

*Answers to problems marked with an asterisk can be found in the back of the text.

8-3. A certain logic family has the following voltage parameters:

 $V_{\rm IH}({
m min}) = 3.5 \ {
m V} \qquad V_{\rm IL}({
m max}) = 1.0 \ {
m V} \\ V_{\rm OH}({
m min}) = 4.9 \ {
m V} \qquad V_{\rm OL}({
m max}) = 0.1 \ {
m V}$

- (a)*What is the largest positive-going noise spike that can be tolerated?
- (b) What is the largest negative-going noise spike that can be tolerated?

DRILL QUESTION

- **B** 8-4.*For each statement, indicate the term or parameter being described.
 - (a) Current at an input when a logic 1 is applied to that input
 - (b) Current drawn from the V_{CC} source when all outputs are LOW
 - (c) Time required for an output to switch from the 1 to the 0 state
 - (d) The size of the voltage spike that can be tolerated on a HIGH input without causing indeterminate operation
 - (e) An IC package that does not require holes to be drilled in the printed circuit board
 - (f) When a LOW output receives current from the input of the circuit it is driving
 - (g) Number of different inputs that an output can safely drive
 - (h) Arrangement of output transistors in a standard TTL circuit
 - (i) Another term that describes pull-down transistor Q_4
 - (j) Range of V_{CC} values allowed for TTL
 - (k) $V_{OH}(min)$ and $V_{IH}(min)$ for the 74ALS series
 - (l) $V_{\rm IL}(\max)$ and $V_{\rm OL}(\max)$ for the 74ALS series
 - (m) When a HIGH output supplies current to a load

SECTION 8-4

- 8-5.*(a) From Table 8-6, determine the noise margins when a 74LS device is driving a 74ALS input.
 - (b) Repeat part (a) for a 74ALS driving a 74LS.
 - (c) What will be the overall noise margin of a logic circuit that uses 74LS and 74ALS circuits in combination?
 - (d) A certain logic circuit has $V_{IL}(max) = 450 \text{ mV}$. Which TTL series can be used with this circuit?

SECTIONS 8-5 AND 8-6

B 8-6. **DRILL QUESTION**

- (a) Define fan-out.
- (b)*In which type of gates do tied-together inputs always count as a single input load in the LOW state?
- (c)*Define "floating" inputs.
- (d) What causes current spikes in TTL? What undesirable effect can they produce? What can be done to reduce this effect?

- (e) When a TTL output drives a TTL input, where does $I_{\rm OL}$ come from? Where does $I_{\rm OH}$ go?
- 8-7. Use Table 8-12 to find the fan-out for interfacing the first logic family to drive the second.
 - (a)*74AS to 74AS
 - (b)*74F to 74F
 - (c) 74AHC to 74AS
 - (d) 74HC to 74ALS
- **B** 8-8. Refer to the data sheet for the 74LS112 J-K flip-flop.
 - (a)*Determine the HIGH and LOW load current at the J and K inputs.
 - (b) Determine the HIGH and LOW load current at the clock and clear inputs.
 - (c) How many 74LS112 clock inputs can the output of one 74LS112 drive?
- **B** 8-9.*Figure 8-55(a) shows a 74LS112 J-K flip-flop whose output is required to drive a total of eight standard TTL inputs. Because this exceeds the fan-out of the 74LS112, a buffer of some type is needed. Figure 8-55(b) shows one possibility using one of the NAND gates from the 74LS37 quad NAND buffer, which has a much higher fan-out than the 74LS112. Note that \overline{Q} is used because the NAND is acting as an INVERTER. Refer to the data sheet for the 74LS37.
 - (a) Determine its maximum fan-out to standard TTL.
 - (b) Determine its maximum sink current in the LOW state.

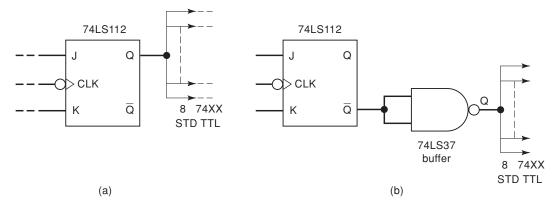


FIGURE 8-55 Problems 8-9 and 8-10.

- Buffer gates are generally more expensive than ordinary gates, and sometimes there are unused ordinary gates available that can be used to solve a loading problem such as that in Figure 8-55(a). Show how 74LS00 NAND gates can be used to solve this problem.
- B 8-11*Refer to the logic diagram of Figure 8-56, where the 74LS86 exclusive-OR output is driving several 74LS20 inputs. Determine whether the fan-out of the 74LS86 is being exceeded, and explain. Repeat using all 74AS devices. Use Table 8-7.

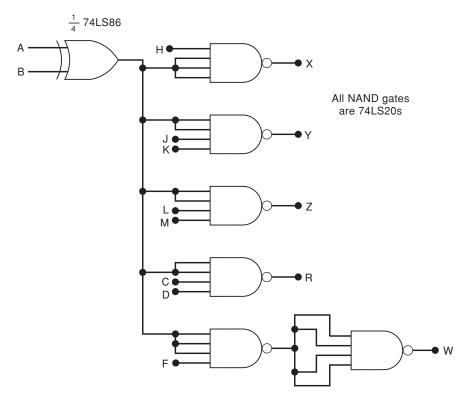
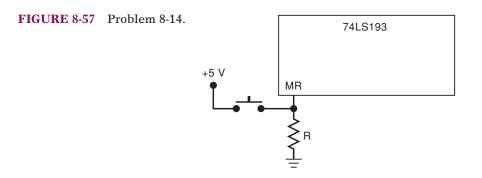
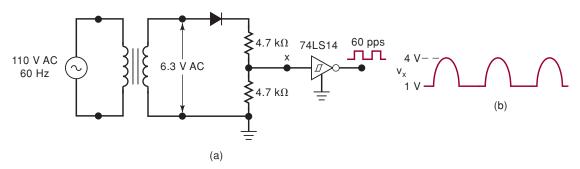


FIGURE 8-56 Problems 8-11 and 8-13.

- **B** 8-12. How long does it take for the output of a typical 74LS04 to change states in response to a positive-going transition at its input?
- C 8-13.*For the circuit of Figure 8-56, determine the longest time it will take for a change in the *A* input to be felt at output *W*. Use all worst-case conditions and maximum values of gate propagation delays. (*Hint:* Remember that NAND gates are inverting gates.) Repeat using all 74ALS devices.
 - 8-14.*(a) Figure 8-57 shows a 74LS193 counter with its active-HIGH master reset input activated by a push-button switch. Resistor R is used to hold MR LOW while the switch is open. What is the maximum value that can be used for R?
 - (b) Repeat part (a) for the 74ALS193.

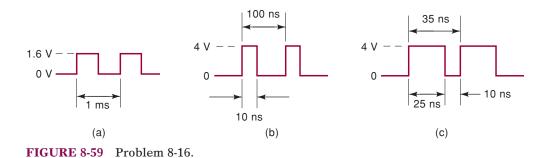


- C, T 8-15. Figure 8-58(a) shows a circuit used to convert a 60-Hz sine wave to a 60-pps signal that can reliably trigger FFs and counters. This type of circuit might be used in a digital clock.
 - (a) Explain the circuit operation.
 - (b)*A technician is testing this circuit and observes that the 74LS14 output stays LOW. He checks the waveform at the INVERTER input, and it appears as shown in Figure 8-58(b). Thinking that the INVERTER is faulty, he replaces the chip and observes the same results. What do you think is causing the problem, and how can it be fixed? (*Hint:* Examine the v_x waveform carefully.)

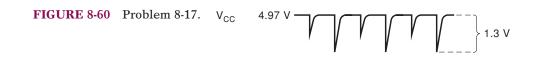




T 8-16. For each waveform in Figure 8-59, determine *why* it will *not* reliably trigger a 74LS112 flip-flop at its *CLK* input.



T 8-17. A technician breadboards a logic circuit for testing. As she tests the circuit's operation, she finds that many of the FFs and counters are triggering erratically. Like any good technician, she checks the V_{CC} line with a dc meter and reads 4.97 V, which is acceptable for TTL. She then checks all circuit wiring and replaces each IC one by one, but the problem persists. Finally she decides to observe V_{CC} on the scope and sees the waveform shown in Figure 8-60. What is the probable cause of the noise on V_{CC} ? What did the technician forget to include when she breadboarded the circuit?



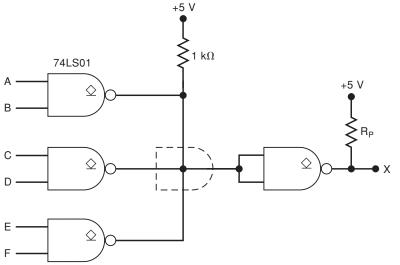
SECTIONS 8-7 TO 8-10

- **B** 8-18. Which type of MOSFET is turned on by placing
 - (a) 5 V on the gate and 0 V on the source?
 - (b) 0 V on the gate and 5 V on the source?
- **B** 8-19.* Which of the following are advantages that CMOS generally has over TTL?
 - (a) Greater packing density
 - (b) Higher speed
 - (c) Greater fan-out
 - (d) Lower output impedance
 - (e) Simpler fabrication process
 - (f) More suited for LSI
 - (g) Lower $P_{\rm D}$ (below 1 MHz)
 - (h) Transistors as only circuit element
 - (i) Lower input capacitance
 - (j) Less susceptible to ESD
 - 8-20. Which of the following operating conditions will probably result in the lowest average $P_{\rm D}$ for a CMOS logic system? Explain.
 - (a) $V_{DD} = 5$ V, switching frequency $f_{max} = 1$ MHz
 - (b) $V_{DD} = 5 \text{ V}, f_{\text{max}} = 10 \text{ kHz}$
 - (c) $V_{DD} = 10 \text{ V}, f_{\text{max}} = 10 \text{ kHz}$
- C 8-21.*The output of each INVERTER on a 74LS04 IC is driving two 74HCT08 inputs. The input to each INVERTER is LOW over 99 percent of the time. What is the maximum power that the 74LS04 chip is dissipating?
 - 8-22. Use the values from Table 8-9 to calculate the HIGH-state noise margin when a 74HC gate drives a standard 74LS input.
 - 8-23. What will cause latch-up in a CMOS IC? What might happen in this condition? What precautions should be taken to prevent latch-up?
 - 8-24. Refer to the data sheet for the 74HC20 NAND gate IC. Use maximum values to calculate $P_{\rm D}(\text{avg})$ and $t_{\rm pd}(\text{avg})$. Compare with the values calculated in Problem 8-2 for TTL.

SECTIONS 8-11 AND 8-12

- **B** 8-25. **DRILL QUESTION**
 - (a) Define wired-AND.
 - (b) What is a pull-up resistor? Why is it used?
 - (c) What types of TTL outputs can safely be tied together?
 - (d) What is bus contention?
- **D** 8-26. The 74LS09 TTL IC is a quad two-input AND with open-collector outputs. Show how 74LS09s can be used to implement the operation $x = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot M$.
- **B** 8-27.* Determine the logic expression for output *X* in Figure 8-61.





- **C** 8-28. Which of the following would be most likely to destroy a TTL totempole output while it is trying to switch from HIGH to LOW?
 - (a) Tying the output to +5 V
 - (b) Tying the output to ground
 - (c) Applying an input of 7 V
 - (d) Tying the output to another TTL totem-pole output
- **D** 8-29.*Figure 8-62(a) shows a 7406 open-collector inverting buffer used to control the ON/OFF status of an LED to indicate the state of FF output *Q*. The LED's nominal specification is $V_{\rm F} = 2.4$ V at $I_{\rm F} = 20$ mA, and $I_{\rm F}({\rm max}) = 30$ mA.
 - (a) What voltage will appear at the 7406 output when Q = 0?
 - (b) Choose an appropriate value for the series resistor for proper operation.

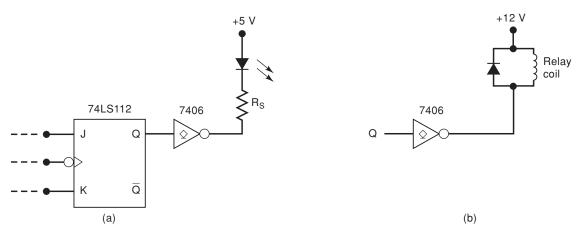
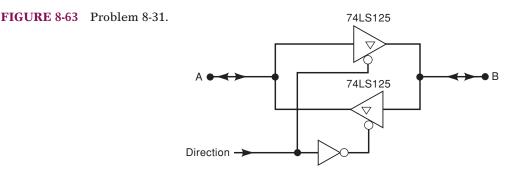


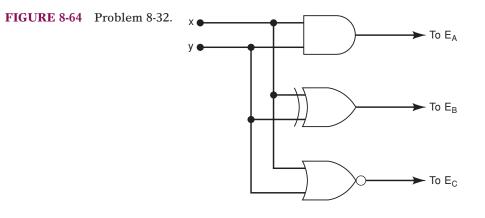
FIGURE 8-62 Problems 8-29 and 8-30.

- 8-30. In Figure 8-62(b), the 7406 output is used to switch current to a relay.
 - (a)*What voltage will be at the 7406 output when Q = 0?
 - (b)*What is the largest current relay that can be used?
 - (c) How can we modify this circuit to use a 7407?

N 8-31. Figure 8-63 shows how two tristate buffers can be used to construct a *bidirectional transceiver* that allows digital data to be transmitted in either direction (*A* to *B*, or *B* to *A*). Describe the circuit operation for the two states of the DIRECTION input.



- 8-32. The circuit of Figure 8-64 is used to provide the enable inputs for the circuit of Figure 8-37.
 - (a) Determine which of the data inputs (*A*, *B*, or *C*) will appear on the bus for each combination of inputs *x* and *y*.
 - (b) Explain why the circuit will not work if the NOR is changed to an XNOR.



8-33.* What type of counter circuit from Chapter 7 could control the enables in Figure 8-37 so that only one buffer is on at any time, and the buffers are enabled sequentially?

SECTION 8-14

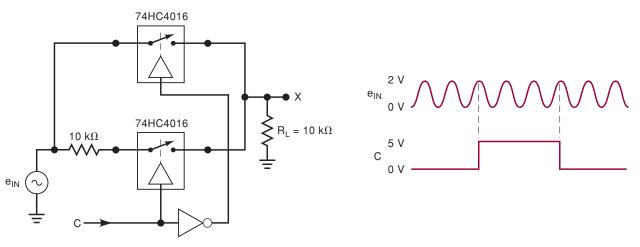
B 8-34. **DRILL QUESTIONS**

- (a) Which logic family must be used if maximum speed is of utmost importance?
- (b) Which logic family uses the most power?
- (c) Which TTL series is the fastest?
- (d) Which pure CMOS series is the fastest?
- (e) Which family has the best speed-power product?
- 8-35. Name two radical differences between ECL outputs and either TTL or CMOS outputs.

8-36.*Determine the approximate values of $V_{\rm OUT}$ for both states of the CONTROL input in Figure 8-65.

FIGURE 8-65 Problem 8-36. +5 V $68 k\Omega$ 74HC4016 V_{OUT} $22 k\Omega$

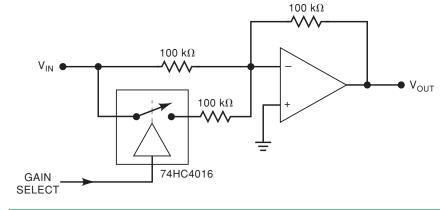
8-37.*Determine the waveform at output X in Figure 8-66 for the given input waveforms. Assume that $R_{\rm ON} \approx 200 \ \Omega$ for the bilateral switch.





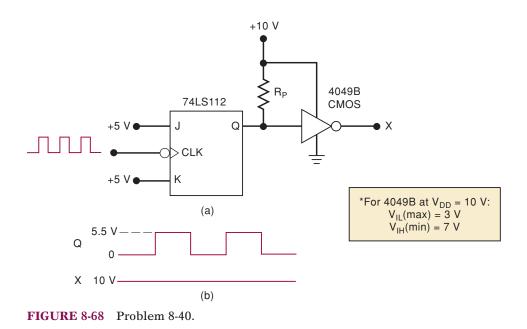
N, **D**, **C** 8-38.* Determine the gain of the op-amp circuit of Figure 8-67 for the two states of the GAIN SELECT input. This circuit shows the basic principle of digitally controlled signal amplification.

FIGURE 8-67 Problem 8-38.

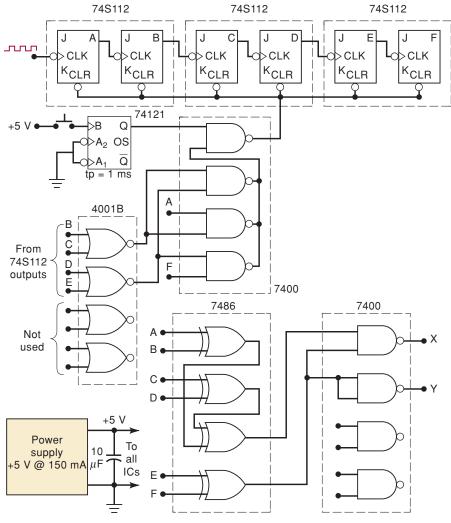


B 8-39. **DRILL QUESTION**

- (a) Which CMOS series can have its inputs driven directly from a TTL output?
- (b) What is the function of a level translator? When is it used?
- (c) Why is a buffer required between some CMOS outputs and TTL inputs?
- (d) *True or false:* Most CMOS outputs have trouble supplying the TTL HIGH-state input current.
- **T** 8-40. Refer to Figure 8-68(a), where a 74LS TTL output, Q, is driving a CMOS INVERTER operating at $V_{DD} = 10$ V. The waveforms at Q and X appear as shown in Figure 8-68(b). Which of the following is a possible reason why X stays HIGH?
 - (a) The 10-V supply is faulty.
 - (b) The pull-up resistor is too large.
 - (c) The 74LS112 output breaks down at well below 10 V and maintains a 5.5-V level in the HIGH state. This is in the indeterminate range for the CMOS input.
 - (d) The CMOS input is loading down the TTL output.

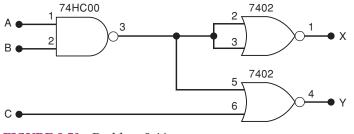


- 8-41. (a)* Use Table 8-12 to determine how many 74AS inputs can typically be driven by a 4000B output.
 - (b) Repeat part (a) for a 74HC output.
- T 8-42. Figure 8-69 is a logic circuit that was poorly designed. It contains at least eight instances where the characteristics of the ICs have not been properly taken into account. Find as many of these as you can.





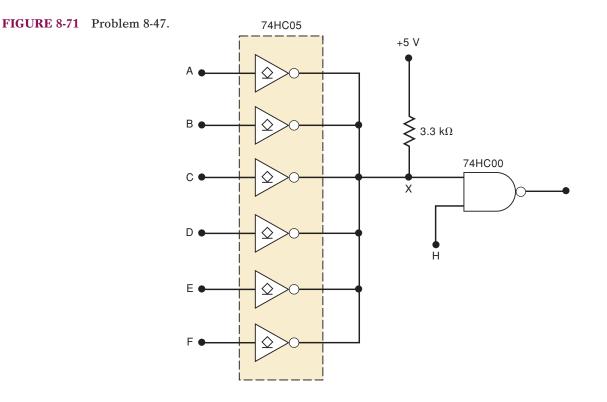
- T 8-43. Repeat Problem 8-42 with the following changes in the circuit:
 - Each TTL IC is replaced with its 74LS equivalent.
 - The 4001B is replaced with a 74HCT02.
 - 8-44.*Use Table 8-12 to explain why the circuit of Figure 8-70 will not work as it is. How can the problem be corrected?



- D 8-45. The gas tank on your car has a fuel-level sending unit that works like a potentiometer. A float moves up and down with the gasoline level, changing the variable resistor setting and producing a voltage proportional to the gas level. A full tank produces 12 V, and an empty tank produces 0 V. Design a circuit using an LM339 that turns on the "Fuel Low" indicator lamp when the voltage level from the sending unit gets below 0.5 V.
- **D** 8-46.* The over-temperature comparator circuit in Figure 8-52 is modified by replacing the LM34 temperature sensor with an LM35 that outputs 10 mV per degree Celsius. The alarm must still be activated (HIGH) when the temperature is over 100°F, which is equal to approximately 38°C. Recalculate the values of R_1 and R_2 to complete the modification.

SECTION 8-19

T 8-47. The circuit in Figure 8-71 uses a 74HC05 IC that contains six opendrain INVERTERs. The INVERTERs are connected in a wired-AND arrangement. The output of the NAND gate is always HIGH, regardless of the inputs A-H. Describe a procedure that uses a logic probe and pulser to isolate this fault.



- **T** 8-48. The circuit of Figure 8-53 has a solder bridge to ground somewhere between the output of the NAND gate and the input of the FF. Describe a procedure for a test that could be performed to indicate that the fault is on the circuit board and probably not in either the NAND or the FF ICs.
- **T** 8-49.*In Figure 8-46, a logic probe indicates that the lower end of the pullup resistor is stuck in the LOW state. Which of the following is the possible fault?
 - (a) The TTL gate's current-sourcing transistor is open.
 - (b) The TTL gate's current-sinking transistor has a collector–emitter short.
 - (c) There is a break in the connection from R_P to the CMOS gate.

MICROCOMPUTER APPLICATION

C, N 8-50*In Chapter 5, we saw how a microprocessor (MPU), under software control, transfers data to an external register. The circuit diagram is repeated in Figure 8-72. Once the data are in the register, they are stored there and used for whatever purpose they are needed. Sometimes, each individual bit in the register has a unique function. For example, in automobile computers, each bit could represent the status of a different physical variable being monitored by the MPU. One bit might indicate when the engine temperature is too high. Another bit might signal when oil pressure is too low. In other applications, the bits in the register are used to produce an analog output that can be used to drive devices requiring analog inputs that have many different voltage levels.

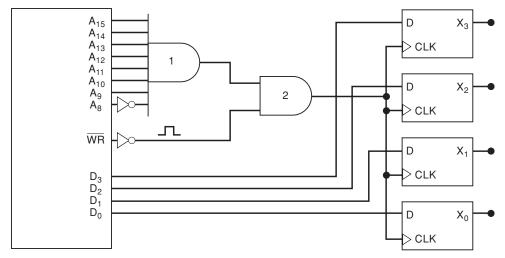


FIGURE 8-72 Problem 8-50.

Figure 8-73 shows how we can use the MPU to generate an analog voltage by taking the register data from Figure 8-72 and using them to control the inputs to a summing amplifier. Assume that the MPU is executing a program that is transferring a new set of data to the register every 10 μ s according to Table 8-14. Sketch the resulting waveform at $V_{\rm OUT}$.

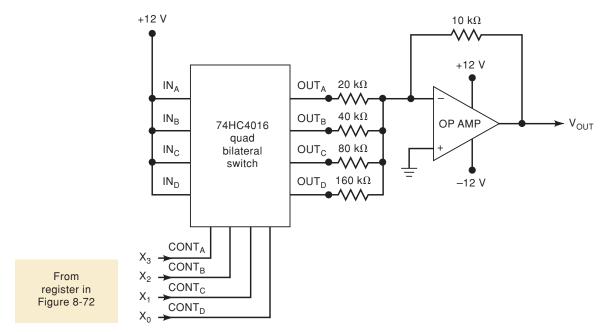


FIGURE 8-73 Problem 8-50.

	Problem 8-50.		
TABLE 8-14		Time (μ s)	MPU Data
		0	0000
		10	0010
		20	0100
		30	0111
		40	1010
		50	1110
		60	1111
		70	1111
		80	1110
		90	1100
		100	1000

ANSWERS TO SECTION REVIEW QUESTIONS

SECTION 8-1

1. See text.2. False3. False; $V_{\rm NH}$ is the difference between $V_{\rm OH}({\rm min})$ and $V_{\rm IH}({\rm min})$.4. Current sinking: an output actually receives (sinks) current fromthe input of the circuit it is driving.Current sourcing: an output supplies (sources)current to the circuit it is driving.5. DIP6. J-lead7. Its leads are bent.8. No

1. True 2. LOW 3. Fast switching times, low power dissipation; large current spike during switching from LOW to HIGH 4. Q_3 5. Q_6 6. No multipleemitter transistor

SECTION 8-4

1. (a) 74AS (b) 74S, 74LS (c) standard 74 (d) 74S, 74LS, 74AS, 74ALS (e) 74ALS 2. All three can operate at 40 MHz, but the 74ALS193 will use less power. 3. *Q*₄, *Q*₅, respectively

SECTION 8-5

1. Q_4 's ON-state resistance and $V_{OL}(max)$ 2. 123. Its output voltages may notremain in the allowed logic 0 and 1 ranges.4. Two; five

SECTION 8-6

1. LOW2. Connect to $+V_{CC}$ through a 1-k Ω resistor; connect to another used input3. Connect to ground; connect to another used input4. False; only in theLOW state5. Connecting small RF capacitors between V_{CC} and ground neareach TTL IC to filter out voltage spikes caused by rapid current changes during output transitions from LOW to HIGH

SECTION 8-8

1. CMOS uses both P- and N-channel MOSFETs. 2. One 3. Six

SECTION 8-9

1. 74C, HC, HCT, AHC, AHCT2. 74ACT, HCT, AHCT3. 74C, HC/HCT,AC/ACT, AHC/AHCT4. BiCMOS5. Maximum permissible propagation delay;input capacitance of each load6. See text.7. CMOS8. (a) True(c) False(d) False(e) True(f) False

SECTION 8-10

1. More circuits on chip; higher operating speed2. Can't handle higher voltages:increased power dissipation can overheat the chip.3. Same as standard TTL: 2.0 V4. 74ALVC, 74LV5. 74LVT

SECTION 8-11

1. When two or more circuit outputs are connected together2. Damaging cur-rent can flow; V_{OL} exceeds $V_{OL}(max)$.3. Current-sinking transistor Q_4 's collectoris unconnected (there is no Q_3).4. To produce a V_{OH} level5. $\overline{A} \ \overline{B} \ \overline{C} \ \overline{D} \ \overline{E} \ \overline{F}$ 6. No active pull-up transistor7. See Figure 8-34.

SECTION 8-12

1. HIGH, LOW, Hi-Z 2. Hi-Z 3. When two or more tristate outputs tied to a common bus are enabled at the same time 4. $E_A = E_B = 0$, $E_C = 1$ 5. See Figure 8-39.

SECTION 8-13

1. Less than 4 inches 2. Resistance, capacitance, inductance 3. To reduce reflections and reactive ringing on the line.

SECTION 8-14

1. (a) True (b) True (c) False (d) True (e) False (f) False

1. The logical level at the control input controls the open/closed status of a bidirectional switch that can pass analog signals in either direction. 2. True

SECTION 8-16

1. A pull-up resistor must be connected to +5 V at the TTL output. 2. CMOS I_{OH} or I_{OL} may be too low.

SECTION 8-17

1. It takes the output from a driver circuit and conditions it so that it is compatiblewith the input requirements of the load.2. True3. False; for example, the4000B series cannot sink $I_{\rm IL}$ of a 74 or a 74AS device.4. 74HCT and ACT5. Two

SECTION 8-18

1. $V^{(+)} > V^{(-)}$ 2. $V^{(-)} > V^{(+)}$ 3. Open-collector

SECTION 8-19

1. It injects a voltage pulse of selected polarity at a node that is not shorted to V_{CC} or ground. 2. False 3. False 4. The pulse LED flashes once each time the pulser is activated.