GLOSSARY

Access Time Time between the memory's receiving a new input address and the output data's becoming available in a read operation.

Accumulator Principal register of an arithmetic/logic unit (ALU).

Acquisition Time Time required for a sample-and-hold circuit to capture the analog value that is present on its input.

Active-HIGH (LOW) Decoder Decoder that produces a logic HIGH (LOW) at the output when detection occurs.

Active Logic Level Logic level at which a circuit is considered active. If the symbol for the circuit includes a bubble, the circuit is active-LOW. On the other hand, if it doesn't have a bubble, then the circuit is active-HIGH.

Actuator Electrically controlled device that controls a physical variable.

Addend Number to be added to another.

Adder/Subtractor An adder circuit that can subtract by complementing (negating) one of the operands. *See also* Parallel/Adder.

Address Number that uniquely identifies the location of a word in memory.

Address Bus Unidirectional lines that carry the address code from the CPU to memory and I/O devices.

Address Multiplexing Multiplexing used in dynamic RAMs to save IC pins. It involves latching the two halves of a complete address into the IC in separate steps.

Alias A digital signal that results from sampling an incoming signal at a rate less than twice the highest frequency contained in the incoming signal.

Alphanumeric Codes Codes that represent numbers, letters, punctuation marks, and special characters.

Altera Hardware Description Language (AHDL) A proprietary HDL developed by Altera Corporation for programming their programmable logic devices.

Alternate Logic Symbol A logically equivalent symbol that indicates the active level of the inputs and outputs.

Analog Representation Representation of a quantity that varies over a continuous range of values.

Analog System Combination of devices designed to manipulate physical quantities that are represented in analog form.

Analog-to-Digital Converter (ADC) Circuit that converts an analog input to a corresponding digital output.

Analog Voltage Comparator Circuit that compares two analog input voltages and produces an output that indicates which input is greater.

& When used inside an IEEE/ANSI symbol, an indication of an AND gate or AND function.

AND Gate Digital circuit that implements the AND operation. The output of this circuit is HIGH (logic level 1) only if all of its inputs are HIGH.

AND Operation Boolean algebra operation in which the symbol is used to indicate the ANDing of two or more logic variables. The result of the AND operation will be HIGH (logic level 1) only if all variables are HIGH.

Application-Specific Integrated Circuit (ASIC) An IC that has been specifically designed to meet the requirements of an application. Subcategories include PLDs, gate arrays, standard cells, and full-custom ICs.

ARCHITECTURE Keyword in VHDL used to begin a section of code that defines the operation of a circuit block (ENTITY).

Arithmetic/Logic Unit (ALU) Digital circuit used in computers to perform various arithmetic and logic operations.

ASCII Code (American Standard Code for Information Interchange) Seven-bit alphanumeric code used by most computer manufacturers.

Asserted Term used to describe the state of a logic signal; synonymous with "active."

Astable Multivibrator Digital circuit that oscillates between two unstable output states.

Asynchronous Counter Type of counter in which each flip-flop output serves as the clock input signal for the next flip-flop in the chain.

Asynchronous Inputs Flip-flop inputs that can affect the operation of the flip-flop independent of the synchronous and clock inputs.

Asynchronous Transfer Data transfer performed without the aid of the clock.

Augend Number to which an addend is added.

Auxiliary Memory The part of a computer's memory that is separate from the computer's main working memory. Generally has high density and high capacity, such as magnetic disk.

Backplane Electrical connection common to all segments of an LCD.

Barrel Shifter A shift register that can very efficiently shift a binary number left or right by any number of bit positions.

BCD Counter Binary counter that counts from 0000_2 to 1001_2 before it recycles.

BCD-to-Decimal Decoder Decoder that converts a BCD input into a single decimal output equivalence.

BCD-to-7-Segment Decoder/Driver Digital circuit that takes a four-bit BCD input and activates the required outputs to display the equivalent decimal digit on a 7-segment display.

Behavioral Level of Abstraction A technique of describing a digital circuit that focuses on how the circuit reacts to its inputs.

Bidirectional Data Line Term used when a data line functions as either an input or an output line depending on the states of the enable inputs.

Bilateral Switch CMOS circuit that acts like a single-pole, single-throw (SPST) switch controlled by an input logic level.

Binary-Coded-Decimal Code (BCD Code) Four-bit code used to represent each digit of a decimal number by its four-bit binary equivalent.

Binary Counter Group of flip-flops connected in a special arrangement in which the states of the flip-flops represent the binary number equivalent to the number of pulses that have occurred at the input of the counter.

Binary Digit Bit.

Binary Point Mark that separates the integer from the fractional portion of a binary quantity.

Binary System Number system in which there are only two possible digit values, 0 and 1.

Bipolar DAC Digital-to-analog converter that accepts signed binary numbers as input and produces the corresponding positive or negative analog output value.

Bipolar ICs Integrated digital circuits in which NPN and PNP transistors are the main circuit elements.

BIT In VHDL, the data object type representing a single binary digit (bit).

Bit Digit in the binary system.

Bit Array A way to represent a group of bits by giving it a name and assigning an element number to each bit's position. This same structure is sometimes called a bit vector.

BIT_VECTOR In VHDL, the data object type representing a bit array. *See also* Bit Array.

Boolean Algebra Algebraic process used as a tool in the design and analysis of digital systems. In Boolean algebra only two values are possible, 0 and 1.

Boolean Theorems Rules that can be applied to Boolean algebra to simplify logic expressions.

Bootstrap Program Program, stored in ROM, that a computer executes on power-up.

Bubbles Small circles on the input or output lines of logic-circuit symbols that represent inversion of a particular signal. If a bubble is present, the input or output is said to be active-LOW.

Buffer/Driver Circuit designed to have a greater output current and/or voltage capability than an ordinary logic circuit.

Buffer Register Register that holds digital data temporarily.

Buried Node A defined point in a circuit that is not accessible from outside that circuit.

Bus Group of wires that carry related bits of information.

Bus Contention Situation in which the outputs of two or more active devices are placed on the same bus line at the same time.

Bus Drivers Circuits that buffer the outputs of devices connected to a common bus; used when a large number of devices share a common bus.

Byte Group of eight bits.

Cache A high-speed memory system that can be loaded from the slower system DRAM and accessed quickly by the high-speed CPU.

Capacity Amount of storage space in a memory expressed as the number of bits or number of words.

Carry Digit or bit that is generated when two numbers are added and the result is greater than the base for the number system being used.

Carry Propagation Intrinsic circuit delay of some parallel adders that prevents the carry bit (C_{OUT}) and the result of the addition from appearing at the output simultaneously.

Carry Ripple *See* Carry Propagation.

CAS (Column Address Strobe) Signal used to latch the column address into a DRAM.

CAS-before-RAS Method for refreshing DRAMs that have built-in refresh counters. When the *CAS* input is driven LOW and held there as *RAS* is pulsed LOW, an internal refresh operation is performed at the row address given by the on-chip refresh counter.

Cascading Connecting logic circuits in a serial fashion with the output of one circuit driving the input of the next, and so on.

CASE A control structure that selects one of several options when describing a circuit's operation based on the value of a data object.

Central Processing Unit (CPU) Part of a computer that is composed of the arithmetic/logic unit (ALU) and the control unit.

Checksum Special data word stored in the last ROM location. It is derived from the addition of all other data words in the ROM, and it is used for error-checking purposes.

Chip Select Input to a digital device that controls whether or not the device will perform its function. Also called *chip enable.*

Circuit Excitation Table Table showing a circuit's possible PRESENT-to-NEXT state transitions and the required *J* and *K* levels at each flip-flop.

Circular Buffer A memory system that always contains the last *n* data values that have been written. Whenever a new data value is stored, it overwrites the oldest value in the buffer.

Circulating Shift Register Shift register in which one of the outputs of the last flip-flop is connected to the input of the first flip-flop.

CLEAR An input to a latch or FF used to make $Q = 0$.

CLEAR State The $Q = 0$ state of a flip-flop.

Clock Digital signal in the form of a rectangular pulse train or a square wave.

Clock Skew Arrival of a clock signal at the clock inputs of different flip-flops at different times as a result of propagation delays.

Clock Transition Times Minimum rise and fall times for the clock signal transitions used by a particular IC, specified by the IC manufacturer.

Clocked D Flip-Flop Type of flip-flop in which the *D* (data) input is the synchronous input.

Clocked Flip-Flops Flip-flops that have a clock input.

Clocked J-K FLip-Flop Type of flip-flop in which inputs *J* and *K* are the synchronous inputs.

Clocked S-R Flip-Flop Type of flip-flop in which the inputs SET and RESET are the synchronous inputs.

CMOS (Complementary Metal-Oxide-Semiconductor) Integrated-circuit technology that uses MOSFETs as the principal circuit element. This logic family belongs to the category of unipolar digital ICs.

Combinational Logic Circuits Circuits made up of combinations of logic gates, with no feedback from outputs to inputs.

Comments Text added to any HDL design file or computer program to describe the purpose and operation of the code in general or of individual statements in the code. Documentation regarding author, date, revision, etc., may also be contained in the comments.

Common Anode LED display that has the anodes of all of the segment LEDs tied together.

Common Cathode LED display that has the cathodes of all of the segment LEDs tied together.

Common-Control Block Symbol used by the IEEE/ANSI standard to describe when one or more inputs are common to more than one of the circuits in an IC.

Compiler A program that translates a text file written in a high-level language into a binary file that can be loaded into a programmable device such as a PLD or a computer's memory.

Complement *See* Invert.

Complex PLD (CPLD) Class of PLDs that contain an array of PAL-type blocks that can be interconnected.

COMPONENT A VHDL keyword used at the top of a design file to provide information about a library component.

Computer Word Group of binary bits that form the primary unit of information in a computer.

Concatenate A term used to describe the arrangement or linking of two or more data objects into ordered sets.

Concurrent Events that occur simultaneously (at the same time). In HDL, the circuits generated by concurrent statements are not affected by the order or sequence of the statements in the code.

Concurrent Assignment Statement A statement in AHDL or VHDL that describes a circuit that works concurrently with all other circuits that are described by concurrent statements.

Conditional Signal Assignment A VHDL concurrent construct that evaluates a series of conditions sequentially to determine the appropriate value to assign to a signal. The first true condition evaluated determines the assigned value.

Constants Symbolic names that can be used to represent fixed numeric (scalar) values.

Contact Bounce The tendency of all mechanical switches to vibrate when forced to a new position. The vibrations cause the circuit to make contact and break contact repeatedly until the vibrations settle out.

Contention Two (or more) output signals connected together trying to drive a common point to different voltage levels. *See also* Bus Contention.

Control Bus Set of signal lines that are used to synchronize the activities of the CPU and the separate μC elements.

Control Inputs Input signals synchronized with the active clock transition that determine the output state of a flip-flop.

Control Unit Part of a computer that provides decoding of program instructions and the necessary timing and control signals for the execution of such instructions.

Count Enable An input on a synchronous counter that controls whether the outputs respond to or ignore an active clock transition.

Crystal-Controlled Clock Generator Circuit that uses a quartz crystal to generate a clock signal at a precise frequency.

Current-Sinking Logic Logic family in which the output of a logic circuit sinks current from the input of the logic circuit that it is driving.

Current-Sinking Transistor Name given to the output transistor (Q_4) of a TTL circuit. This transistor is turned on when the output logic level is LOW.

Current-Sourcing Logic Logic family in which the output of a logic circuit sources, or supplies, current to the input of the logic circuit that it is driving.

Current-Sourcing Transistor Name given to the output transistor (Q_3) of most TTL circuits. This transistor is conducting when the output logic level is HIGH.

Current Transients Current spikes generated by the totem-pole output structure of a TTL circuit and caused when both transistors are simultaneously turned on.

D Flip-Flop *See* Clocked D Flip-Flop.

D Latch Circuit that contains a NAND gate latch and two steering NAND gates.

Data Binary representations of numerical values or nonnumerical information in a digital system. Data are used and often modified by a computer program.

Data Acquisition Process by which a computer acquires digitized analog data.

Data Bus Bidirectional lines that carry data between the CPU and the memory, or between the CPU and the I/O devices.

Data Distributors *See* Demultiplexer.

Data-Rate Buffer Application of FIFOs in which sequential data are written into the FIFO at one rate and read out at a different rate.

Data Selectors *See* Multiplexer.

Data Transfer *See* Parallel Data Transfer *or* Serial Data Transfer.

Decade Counter Any counter capable of going through 10 different logic states.

Decimal System Number system that uses 10 different digits or symbols to represent a quantity.

Decision Control Structures The statements and syntax that describe how to choose between two or more options in the code.

Decoder Digital circuit that converts an input binary code into a corresponding single active output.

Decoding Act of identifying a particular binary combination (code) in order to display its value or recognize its presence.

DEFAULTS An AHDL keyword used to establish a default value for a combinational signal for instances when the code does not explicitly specify a value.

DeMorgan's Theorems (1) Theorem stating that the complement of a sum (OR operation) equals the product (AND operation) of the complements, and (2) theorem stating that the complement of a product (AND operation) equals the sum (OR operation) of the complements.

Demultiplexer (DEMUX) Logic circuit that, depending on the status of its select inputs, will channel its data input to one of several data outputs.

Density A relative measure of capacity to store bits in a given amount of space.

Dependency Notation Method used to represent symbolically the relationship between inputs and outputs of logic circuits. This method employs the use of qualifying symbols embedded near the top center or geometric center of a symbol element.

Differential Inputs Method of connecting an analog signal to an analog circuit's + and − inputs, neither of which is ground, such that the analog circuit acts upon the voltage difference between the two inputs.

Digital Computer System of hardware that performs arithmetic and logic operations, manipulates data, and makes decisions.

Digital Integrated Circuits Self-contained digital circuits made by using one of several integrated-circuit fabrication technologies.

Digital One-Shot A one-shot that uses a counter and clock rather than an RC circuit as a time base.

Digital-Ramp ADC Type of analog-to-digital converter in which an internal staircase waveform is generated and utilized for the purpose of accomplishing the conversion. The conversion time for this type of analog-to-digital converter varies depending on the value of the input analog signal.

Digital Representation Representation of a quantity that varies in discrete steps over a range of values.

Digital Signal Processing (DSP) Method of performing repetitive calculations on an incoming stream of digital data words to accomplish some form of signal conditioning. The data are typically digitized samples of an analog signal.

Digital Storage Oscilloscope Instrument that samples, digitizes, stores, and displays analog voltage waveforms.

Digital System Combination of devices designed to manipulate physical quantities that are represented in digital form.

Digital-to-Analog Converter (DAC) Circuit that converts a digital input to a corresponding analog output.

Digitization Process by which an analog signal is converted to digital data.

Disable Action in which a circuit is prevented from performing its normal function, such as passing an input signal through to its output.

Divide-and-Conquer Troubleshooting technique whereby tests are performed that will eliminate half of all possible remaining causes of the malfunction.

Don't-Care Situation when a circuit's output level for a given set of input conditions can be assigned as either a 1 or a 0.

Down Counter Counter that counts from a maximum count downward to 0.

Downloading Process of transferring output files to a programming fixture.

DRAM Controller IC used to handle refresh and address multiplexing operations needed by DRAM systems.

Driver Technical term sometimes added to an IC's description to indicate that the IC's outputs can operate at higher current and/or voltage limits than a normal standard IC.

Dual-in-Line Package (DIP) A very common IC package with two parallel rows of pins intended to be inserted into a socket or through holes drilled in a printed circuit board.

Dual-Slope Analog-to-Digital Converter Type of analog-to-digital converter that linearly charges a capacitor from a current proportional to V_A for a fixed time interval and then increments a counter as the capacitor is linearly discharged to 0.

Dynamic RAM (DRAM) Type of semiconductor memory that stores data as capacitor charges that need to be refreshed periodically.

ECL Emitter-coupled logic; also referred to as *current-mode logic.*

Edge-Detector Circuit Circuit that produces a narrow positive spike that occurs coincident with the active transition of a clock input pulse.

Edge-Triggered Manner in which a flip-flop is activated by a signal transition. A flip-flop may be either a positive- or a negative-edge-triggered flip-flop.

Electrically Compatible When two ICs from different logic series can be connected directly without any special measures taken to ensure proper operation.

Electrically Erasable Programmable ROM (EEPROM) ROM that can be electrically programmed, erased, and reprogrammed.

Electrostatic Discharge (ESD) The often detrimental act of the transfer of static electricity (i.e., an electrostatic charge) from one surface to another. This impulse of current can destroy electronic devices.

ELSE A control structure used in conjunction with IF/THEN to perform an alternate action in the case that the condition is false. An IF/THEN/ELSE always performs one of two actions.

ELSIF A control structure that can be used multiple times following an IF statement to select one of several options in describing a circuit's operation based on whether the associated expressions are true or false.

Embedded Microcontroller Microcontroller that is embedded in a marketable product such as a VCR or an appliance.

Emitter-Coupled Logic *See* ECL.

Enable Action in which a circuit is allowed to perform its normal function, such as passing an input signal through to its output.

Encoder Digital circuit that produces an output code depending on which of its inputs is activated.

Encoding Use of a group of symbols to represent numbers, letters, or words.

ENTITY Keyword in VHDL used to define the basic block structure of a circuit. This word is followed by a name for the block and the definitions of its input/output ports.

Enumerated Type A VHDL user-defined type for a signal or variable.

Erasable Programmable ROM (EPROM) ROM that can be electrically programmed by the user. It can be erased (usually with ultraviolet light) and reprogrammed as often as desired.

EVENT A VHDL keyword used as an attribute attached to a signal to detect a transition of that signal. Generally, an event means a signal changed state.

Exclusive-NOR (XNOR) Circuit Two-input logic circuit that produces a HIGH output only when the inputs are equal.

Exclusive-OR (XOR) Circuit Two-input logic circuit that produces a HIGH output only when the inputs are different.

Fan-Out Maximum number of standard logic inputs that the output of a digital circuit can reliably drive.

Field Programmable Gate Array (FPGA) Class of PLDs that contain an array of more complex logic cells that can be very flexibly interconnected to implement high-level logic circuits.

Field Programmable Logic Array (FPLA) A PLD that uses both a programmable AND array and a programmable OR array.

Firmware Computer programs stored in ROM.

First-In, First-Out (FIFO) Memory Semiconductor sequential-access memory in which data words are read out in the same order in which they were written in.

555 Timer TTL-compatible IC that can be wired to operate in several different modes, such as a one-shot and an astable multivibrator.

Flash ADC Type of analog-to-digital converter that has the highest operating speed available.

Flash Memory Nonvolatile memory IC that has the high-speed access and in-circuit erasability of EEPROMs but with higher densities and lower cost.

Flip-Flop Memory device capable of storing a logic level.

Floating Bus When all outputs connected to a data bus are in the Hi-*Z* state.

Floating Input Input signal that is left disconnected in a logic circuit.

FOR Loop *See* Iterative Loop.

4-to-10 Decoder *See* BCD-to-Decimal Decoder.

Frequency The number of cycles per unit time of a periodic waveform.

Frequency Counter Circuit that can measure and display a signal's frequency.

Frequency Division The use of flip-flop circuits to produce an output waveform whose frequency is equal to the input clock frequency divided by some integer value.

Full Adder Logic circuit with three inputs and two outputs. The inputs are a carry bit (C_{IN}) from a previous stage, a bit from the augend, and a bit from the addend, respectively. The outputs are the sum bit and the carry-out bit (C_{OUT}) produced by the addition of the bit from the addend with the bit from the augend and C_{IN}.

Full-Custom An application-specific integrated circuit (ASIC) that is completely designed and fabricated from fundamental elements of electronic devices such as transistors, diodes, resistors, and capacitors.

Full-Scale Error Term used by some digital-to-analog converter manufacturers to specify the accuracy of a digital-to-analog converter. It is defined as the

maximum deviation of a digital-to-analog converter's output from its expected ideal value.

Full-Scale Output Maximum possible output value of a digital-to-analog converter.

Function Generator Circuit that produces different waveforms. It can be constructed using a ROM, a DAC, and a counter.

Function Prototype A text description that contains all the essential defining attributes of a library function or module.

Functionally Equivalent When the logic functions performed by two different ICs are exactly the same.

Fusible Link Conducting material that can be made nonconducting (i.e., open) by passing too much current through it.

Gate Array An application-specific integrated circuit (ASIC) made up of hundreds of thousands of prefabricated basic gates that can be custom interconnected in the last stages of manufacture to form the desired digital circuit.

GENERATE A VHDL keyword used with the FOR construct to iteratively define multiple similar components and to interconnect them.

Glitch Momentary, narrow, spurious, and sharply defined change in voltage.

Gray Code A code that never has more than one bit changing when going from one state to another,

GSI Giga-scale integration (1,000,000 gates or more).

Half Adder Logic circuit with two inputs and two outputs. The inputs are a bit from the augend and a bit from the addend. The outputs are the sum bit produced by the addition of the bit from the addend with the bit from the augend and the resulting carry (C_{OUT}) bit, which will be added to the next stage.

Hard Disk Rigid metal magnetic disk used for mass storage.

Hardware Description Language (HDL) A text-based method of describing digital hardware that follows a rigid syntax for representing data objects and control structures.

Hexadecimal Number System Number system that has a base of 16. Digits 0 through 9 plus letters A through F are used to express a hexadecimal number.

Hierarchical Design A method of designing a project by breaking it into constituent modules, each of which can be broken further into simpler constituent modules.

Hierarchy A group of tasks arranged in rank order of magnitude, importance, or complexity.

High-Capacity PLD (HCPLD) A PLD with thousands of logic gates and many programmable macrocell resources, along with very flexible interconnection resources.

Hold Time (t_H) Time interval immediately following the active transition of the clock signal during which the control input must be maintained at the proper level.

Hybrid System System that employs both analog and digital techniques.

IEEE/ANSI Institute of Electrical and Electronics Engineers/American National Standards Institute, both professional organizations that establish standards.

IF/THEN A control structure that evaluates a condition and performs an action if the condition is true or bypasses the action and continues on if the condition is false.

Indeterminate Of a logic voltage level, outside the required range of voltages for either logic 0 or logic 1.

Index Another name for the element number of any given bit in a bit array.

Inhibit Circuits Logic circuits that control the passage of an input signal through to the output.

Input Term Matrix Part of a programmable logic device that allows inputs to be selectively connected to or disconnected from internal logic circuitry.

Input Unit Part of a computer that facilitates the feeding of information into the computer's memory unit or ALU.

Instructions Binary codes that tell a computer what operation to perform. A program is made up of an orderly sequence of instructions.

INTEGER In VHDL, the data object type representing a numeric value.

Interfacing Joining of dissimilar devices in such a way that they are able to function in a compatible and coordinated manner; connection of the output of a system to the input of a different system with different electrical characteristics.

Interpolation Filtering Another name for oversampling. Interpolation refers to intermediate values inserted into the digital signal to smooth out the waveform.

Invert Cause a logic level to go to the opposite state.

INVERTER Also referred to as the NOT circuit; logic circuit that implements the NOT operation. An INVERTER has only one input, and its output logic level is always the opposite of this input's logic level.

Iterative Loop A control structure that implies a repetitive operation and a stated number of iterations.

Jam Transfer *See* Asynchronous Transfer.

JEDEC Joint Electronic Device Engineering Council, which established standards for IC pin assignments and PLD file format.

J-K Excitation Table Table showing the required *J* and *K* input conditions for each possible state transition for a single J-K flip-flop.

Johnson Counter Shift register in which the inverted output of the last flip-flop is connected to the input of the first flip-flop.

JTAG Joint Test Action Group, which created a standard interface that allows access to the inner workings of an IC for testing, controlling, and programming purposes.

Karnaugh Map (K Map) Two-dimensional form of a truth table used to simplify a sum-of-products expression.

Latch Type of flip-flop; also, the action by which a logic circuit output captures and holds the value of an input.

Latch-Up Condition of dangerously high current in a CMOS IC caused by high-voltage spikes or ringing at device input and output pins.

Latency The inherent delay associated with reading data from a DRAM. It is caused by the timing requirements of supplying the row and column addresses, and the time for the data outputs to settle.

LCD Liquid-crystal display.

Lead Pitch The distance between the centers of adjacent pins on an IC.

Least Significant Bit (LSB) Rightmost bit (smallest weight) of a binary expressed quantity.

Least Significant Digit (LSD) Digit that carries the least weight in a particular number.

LED Light-emitting diode.

Libraries A collection of descriptions of commonly used hardware circuits that can be used as modules in a design file.

Library of Parameterized Modules (LPM) A set of generic library functions designed to be very flexible in allowing the user to specify the number of bits, mod number, control options, etc.

Linear Buffer A first-in, first-out memory system that fills at one rate and empties at another rate. After it is full, no data can be stored until data is read from the buffer. *See also* First In, First-Out (FIFO) Memory.

Linearity Error Term used by some digital-to-analog converter manufacturers to specify the device's accuracy. It is defined as the maximum deviation in step size from the ideal step size.

Literals In VHDL, a scalar value or bit pattern that is to be assigned to a data object.

Load Operation Transfer of data into a flip-flop, a register, a counter, or a memory location.

Local Signal *See* Buried Node.

Logic Array Block (LAB) A term Altera Corporation uses to describe building blocks of their CPLDs. Each LAB is similar in complexity to an SPLD.

Logic Circuit Any circuit that behaves according to a set of logic rules.

Logic Elements A term Altera Corporation uses to describe the building blocks of their FLEX10K family of PLDs. The logic elements are programmed as a ram-based look-up table.

Logic Function Generation Implementation of a logic function directly from a truth table by means of a digital IC such as a multiplexer.

Logic Level State of a voltage variable. The states 1 (HIGH) and 0 (LOW) correspond to the two usable voltage ranges of a digital device.

Logic Primitive A circuit description of a fundamental component that is built into the MAX+PLUS II system of libraries.

Logic Probe Digital troubleshooting tool that senses and indicates the logic level at a particular point in a circuit.

Logic Pulser Testing tool that generates a short-duration pulse when actuated manually.

Look-Ahead Carry Ability of some parallel adders to predict, without having to wait for the carry to propagate through the full adders, whether or not a carry bit (C_{OUT}) will be generated as a result of the addition, thus reducing the overall propagation delays.

Look-Up Table (LUT) A way to implement a single logic function by storing the correct output logic state in a memory location that corresponds to each particular combination of input variables.

Looping Combining of adjacent squares in a Karnaugh map containing 1s for the purpose of simplification of a sum-of-products expression.

Low-Power Schottky TTL (LS-TTL) TTL subfamily that uses the identical Schottky TTL circuit but with larger resistor values.

Low-Voltage Differential Signaling (LVDS) A technology for driving high-speed data lines in low-voltage systems that uses two conductors and reverses the polarity to distinguish between HIGH and LOW.

Low-Voltage Technology New line of logic devices that operate from a nominal supply voltage of 3.3 V or less.

LSI Large-scale integration (100 to 9999 gates).

MAC An abbreviation for Multiply Accumulate Unit, the hardware section of a DSP that multiplies a sample with a coefficient and then accumulates (sums) a running total of these products.

MACHINE An AHDL keyword used to create a state machine in a design file.

Macrocell A circuit made up of a group of basic digital components such as AND gates, OR gates, registers, and tristate control circuits that can be interconnected within a PLD via a program.

Macrofunctions A term used by Altera Corporation to describe the predefined hardware descriptions in their libraries that represent standard IC parts.

Magnetic Disk Memory Mass storage memory that stores data as magnetized spots on a rotating, flat disk surface.

Magnetic Tape Memory Mass storage memory that stores data as magnetized spots on a magnetically coated plastic tape.

Magnitude Comparator Digital circuit that compares two input binary quantities and generates outputs to indicate whether the inputs are equal or, if not, which is greater.

Main Memory High-speed portion of a computer's memory that holds the program and data the computer is currently working on. Also called *working memory.*

Mask-Programmed ROM (MROM) ROM that is programmed by the manufacturer according to the customer's specifications. It cannot be erased or reprogrammed.

Mass Storage Storage of large amounts of data; not part of a computer's internal memory.

Maximum Clocking Frequency (f_{MAX}) Highest frequency that may be applied to the clock input of a flip-flop and still have it trigger reliably.

Mealy Model A state-machine model in which the output signals are controlled by combinational inputs as well as the state of the sequential circuit.
Megafunctions A complex or high-level building block available in the Altera library.
Memory Ability of a circuit's output to remain at one state even after the input condition that caused that state is removed.
Memory Cell Device that stores a single bit.
Memory Foldback Redundant enabling of a memory device at more than one address range as a result of incomplete address decoding.
Memory Map Diagram of a memory system that shows the address range of all existing memory devices as well as available memory space for expansion.
Memory Unit Part of a computer that stores instructions and data received from the input unit, as well as results from the arithmetic/logic unit.
Memory Word Group of bits in memory that represents instructions or data of some type.
Microcomputer Newest member of the computer family, consisting of microprocessor chip, memory chips, and I/O interface chips. In some cases, all of the aforementioned are in one single IC.
Microcontroller Small microcomputer used as a dedicated controller for a machine, a piece of equipment, or a process.
Microprocessor (MPU) LSI chip that contains the central processing unit (CPU).
Minuend Number from which the subtrahend is to be subtracted.
MOD Number Number of different states that a counter can sequence through; the counter's frequency division ratio.
Mode The attribute of a port in a digital circuit that defines it as input, output, or bidirectional.
Monostable Multivibrator *See* One-Shot.
Monotonicity Property whereby the output of a digital-to-analog converter increases as the binary input is increased.
Moore Model A state-machine model in which the output signals are controlled only by the sequential circuit outputs.
MOSFET Metal-oxide-semiconductor field-effect transistor.
Most Significant Bit (MSB) Leftmost binary bit (largest weight) of a binary expressed quantity.
Most Significant Digit (MSD) Digit that carries the most weight in a particular number.
MSI Medium-scale integration (12 to 99 gates).
Multiplexer (MUX) Logic circuit that, depending on the status of its select inputs, will channel one of several data inputs to its output.
Multiplexing Process of selecting one of several input data sources and transmitting the selected data to a single output channel.
Multistage Counter Counter in which several counter stages are connected so that the output of one stage serves as the clock input of the next stage to achieve greater counting range or frequency division.
NAND Gate Logic circuit that operates like an AND gate followed by an INVERTER. The output of a NAND gate is LOW (logic level 0) only if all inputs are HIGH (logic level 1).
NAND Gate Latch Flip-flop constructed from two cross-coupled NAND gates.
Negation Operation of converting a positive number to its negative equivalent, or vice versa. A signed binary number is negated by the 2's-complement operation.
Negative-Going Transition When a clock goes from 1 to 0.
Nested To have one control structure embedded within another control structure.
Nibble A group of four bits.
N-MOS (N-Channel Metal-Oxide-Semiconductor) Integrated-circuit technology that uses N-channel MOSFETs as the principal circuit element.
NODE A keyword in AHDL used to declare an intermediate variable (data object) that is local to that subdesign.
Noise Spurious voltage fluctuations that may be present in the environment and cause digital circuits to malfunction.
Noise Immunity Circuit's ability to tolerate noise voltages on its inputs.
Noise Margin Quantitative measure of noise immunity.
Nonretriggerable One-Shot Type of one-shot that will not respond to a trigger input signal while in its quasi-stable state.
Nonvolatile Memory Memory that will keep storing its information without the need for electrical power.
Nonvolatile RAM Combination of a RAM array and an EEPROM or flash on the same IC. The EEPROM serves as a nonvolatile backup to the RAM.
NOR Gate Logic circuit that operates like an OR gate followed by an INVERTER. The output of a NOR gate is LOW (logic level 0) when any or all inputs are HIGH (logic level 1).
NOR Gate Latch Flip-flop constructed from two cross-coupled NOR gates.
NOT Circuit *See* INVERTER.
NOT Operation Boolean algebra operation in which the overbar ($\bar{}$) or the prime ($'$) symbol is used to indicate the inversion of one or more logic variables.

Objects Various ways of representing data in the code of any HDL.
Observation/Analysis Process used to troubleshoot circuits or systems in order to predict the possible faults before ever picking up a troubleshooting instrument. When this process is used, the troubleshooter must understand the circuit operation, observe the symptoms of the failure, and then reason through the operation.
Octal Number System Number system that has a base of 8; digits from 0 to 7 are used to express an octal number.
Octets Groups of eight 1s that are adjacent to each other within a Karnaugh map.

Offset Error Deviation from the ideal 0 V at the output of a digital-to-analog converter when the input is all 0s. In reality, there is a very small output voltage for this situation.

1-of-10 Decoder *See* BCD-to-Decimal Decoder.

1's-Complement Form Result obtained when each bit of a binary number is complemented.

One-Shot Circuit that belongs to the flip-flop family but that has only one stable state (normally $Q = 0$).

One-Time Programmable (OTP) A broad category of programmable components that are programmed by permanently altering the connections (e.g., melting a fuse element).

Open-Collector Output Type of output structure of some TTL circuits in which only one transistor with a floating collector is used.

Optical Disk Memory Class of mass memory devices that uses a laser beam to write onto and read from a specially coated disk.

OR Gate Digital circuit that implements the OR operation. The output of this circuit is HIGH (logic level 1) if any or all of its inputs are HIGH.

OR Operation Boolean algebra operation in which the symbol + is used to indicate the ORing of two or more logic variables. The result of the OR operation will be HIGH (logic level 1) if one or more variables are HIGH.

Output Logic Macrocell (OLMC) A group of logic elements (gates, multiplexers, flip-flops, buffers) in a PLD that can be configured in various ways.

Output Unit Part of a computer that receives data from the memory unit or ALU and presents it to the outside world.

Overflow When in the process of adding signed binary numbers, a carry of 1 is generated from the MSB position of the number into the sign bit position.

Override Inputs Synonymous with "asynchronous inputs."

Oversampling Inserting data points between sampled data in a digital signal to make it easier to filter out the rough edges of the waveform coming out of the DAC.

PACKAGE A VHDL keyword used to define a set of global elements that are available to other modules.

Parallel Adder Digital circuit made from full adders and used to add all of the bits from the addend and the augend together simultaneously.

Parallel Counter *See* Synchronous Counter.

Parallel Data Transfer Operation by which several bits of data are transferred simultaneously into a counter or a register.

Parallel In/Parallel Out Register Type of register that can be loaded with parallel data and has parallel outputs available.

Parallel In/Serial Out Register Type of register that can be loaded with parallel data and has only one serial output.

Parallel Load *See* Parallel Data Transfer.

Parallel-to-Serial Conversion Process by which all data bits are presented simultaneously to a circuit's input and then transmitted one bit at a time to its output.

Parallel Transmission Simultaneous transfer of all bits of a binary number from one place to another.

Parity Bit Additional bit that is attached to each code group so that the total number of 1s being transmitted is always even (or always odd).

Parity Checker Circuit that takes a set of data bits (including the parity bit) and checks to see if it has the correct parity.

Parity Generator Circuit that takes a set of data bits and produces the correct parity bit for the data.

Parity Method Scheme used for error detection during the transmission of data.

Percentage Resolution Ratio of the step size to the full-scale value of a digital-to-analog converter. Percentage resolution can also be defined as the reciprocal of the maximum number of steps of a digital-to-analog converter.

Period The amount of time required for one complete cycle of a periodic event or waveform.

Periodic A cycle that repeats itself regularly in time and form.

Pin-Compatible When the corresponding pins on two different ICs have the same functions.

Pixel Small dots of light that make up a graphical image on a display.

P-MOS (P-channel Metal Oxide Semiconductor) Integrated-circuit technology that uses P-channel MOSFETs as the principal circuit element.

PORT MAP A VHDL keyword that precedes the list of connections specified between components.

Positional-Value System System in which the value of a digit depends on its relative position.

Positive-Going Transition (PGT) When a clock signal changes from a logic 0 to a logic 1.

Power-Down Operating mode in which a chip is disabled and draws much less power than when it is fully enabled.

Power-Supply Decoupling Connection of a small RF capacitor between ground and V_{CC} near each TTL integrated circuit on a circuit board.

Power-Up Self-Test Program stored in ROM and executed by the CPU on power-up to test RAM and/or ROM portions of the computer circuitry.

Preprocessor Commands Compiler commands that are processed before the main program code in order to control how the code is interpreted.

Prescaler A counter circuit that takes base reference frequency and scales it by dividing the frequency down to a rate required by the system.

Present State–Next State Table A table which lists each possible present state of a sequential (counter) circuit and identifies the corresponding next state.

PRESET Asynchronous input used to set $Q = 1$ immediately.

Presettable Counter Counter that can be preset to any starting count either synchronously or asynchronously.

Priority Encoder Special type of encoder that senses when two or more inputs are activated simultaneously and then generates a code corresponding to the highest-numbered input.

PROCESS A VHDL keyword that defines the beginning of a block of code that describes a circuit that must respond whenever certain signals (in the sensitivity list) change state. All sequential statements must occur inside a process.

Product-of-Sums Form Logic expression consisting of two or more OR terms (sums) that are ANDed together.

Program Sequence of binary-coded instructions designed to accomplish a particular task by a computer.

Programmable Array Logic (PAL) Class of programmable logic devices. Its AND array is programmable, whereas its OR array is hard-wired.

Programmable Interconnect Array (PIA) A term Altera Corporation uses to describe the resources used to connect the LABs with each other and also with the input/output modules.

Programmable Logic Array (PLA) Class of programmable logic devices. Both its AND and its OR arrays are programmable. Also called a *field programmable logic array (FPLA)*.

Programmable Logic Device (PLD) IC that contains a large number of interconnected logic functions. The user can program the IC for a specific function by selectively breaking the appropriate interconnections.

Programmable Output Polarity Feature of many PLDs whereby an XOR gate with a polarity fuse gives the designer the option of inverting or not inverting a device output.

Programmable ROM (PROM) ROM that can be electrically programmed by the user. It cannot be erased and reprogrammed.

Programmer A fixture used to apply the proper voltages to PLD and PROM chips in order to program them.

Programming The act of storing 1s and 0s in a programmable logic device to configure its behavioral characteristics.

Propagation Delays (t_{PLH}/t_{PHL}) Delay from the time a signal is applied to the time when the output makes its change.

Pull-Down Transistor *See* Current-Sinking Transistor.

Pull-Up Transistor *See* Current-Sourcing Transistor.

Pulse A momentary change of logic state that represents an event to a digital system.

Pulse-Steering Circuit A logic circuit that can be used to select the destination of an input pulse, depending on the logic levels present at the circuit's inputs.

Quantization Error Error caused by the nonzero resolution of an analog-to-digital converter. It is an inherent error of the device.

Quasi-Stable State State to which a one-shot is temporarily triggered (normally $Q = 1$) before returning to its stable state (normally $Q = 0$).

R/2R Ladder DAC Type of digital-to-analog converter whose internal resistance values span a range of only 2 to 1.

Random-Access Memory (RAM) Memory in which the access time is the same for any location.

RAS (Row Address Strobe) Signal used to latch the row address into a DRAM chip.

RAS-Only Refresh Method for refreshing DRAM in which only row addresses are strobed into the DRAM using the *RAS* input.

Read Term used to describe the condition when the CPU is receiving data from another element.

Read-Only Memory (ROM) Memory device designed for applications where the ratio of read operations to write operations is very high.

Read Operation Operation in which a word in a specific memory location is sensed and possibly transferred to another device.

Read/Write Memory (RWM) Any memory that can be read from and written into with equal ease.

Refresh Counter Counter that keeps track of row addresses during a DRAM refresh operation.

Refreshing Process of recharging the cells of a dynamic memory.

Register Group of flip-flops capable of storing data.

RESET Term synonymous with "CLEAR."

RESET State The $Q = 0$ state of a flip-flop.

Resolution In a digital-to-analog converter, smallest change that can occur in the output for a change in digital input; also called *step size.* In an analog-to-digital converter, smallest amount by which the analog input must change to produce a change in the digital output.

Retriggerable One-Shot Type of one-shot that will respond to a trigger input signal while in its quasi-stable state.

Ring Counter Shift register in which the output of the last flip-flop is connected to the input of the first flip-flop.

Ripple Counter *See* Asynchronous Counter.

Sample-and-Hold Circuit Type of circuit that utilizes a unity-gain buffer amplifier in conjunction with a capacitor to keep the input stable during an analog-to-digital conversion process.

Sampling Acquiring and digitizing a data point from an analog signal at a given instant of time.

Sampling Frequency The rate at which an analog signal is digitized (samples per second).

Sampling Interval Time window during which a frequency counter samples and thereby determines the unknown frequency of a signal.

SBD Schottky barrier diode used in all Schottky TTL series.

Schematic Capture A computer program that can interpret graphic symbols and signal connections and translate them into logical relationships.

Schmitt Trigger Digital circuit that accepts a slow-changing input signal and produces a rapid, oscillation-free transition at the output.

Schottky TTL TTL subfamily that uses the basic TTL standard circuit except that it uses a Schottky barrier diode (SBD) connected between the base and the collector of each transistor for faster switching.

Selected Signal Assignment A VHDL statement that allows a data object to be assigned a value from one of several signal sources depending on the value of an expression.

Self-Correcting Counter A counter that always progresses to its intended sequence, regardless of its initial state.

Sensitivity List The list of signals used to invoke the sequence of statements in a PROCESS.

Sequential Occuring one at a time in a certain order. In HDL, the circuits that are generated by sequential statements behave differently, depending on the order of the statements in the code.

Sequential-Access Memory (SAM) Memory in which the access time will vary depending on the storage location of the data.

Sequential Circuit A logic circuit whose outputs can change states in synchronism with a periodic clock signal. The new state of an output may depend on its current state as well as the current states of other outputs.

Serial Data Transfer Transfer of data from one place to another one bit at a time.

Serial In/Parallel Out Type of register that can be loaded with data serially and has parallel outputs available.

Serial In/Serial Out Type of register that can be loaded with data serially and has only one serial output.

Serial Transmission Transfer of binary information from one place to another a bit at a time.

SET An input to a latch or FF used to make $Q = 1$.

Set A grouping of concatenated variables or signals.

SET State The $Q = 1$ state of a flip-flop.

Settling Time Amount of time that it takes for the output of a digital-to-analog converter to go from 0 to within one-half step size of its full-scale value as the input is changed from all 0s to all 1s.

Setup Time (t_S) Time interval immediately preceding the active transition of the clock signal during which the control input must be maintained at the proper level.

Shift Register Digital circuit that accepts binary data from some input source and then shifts these data through a chain of flip-flops one bit at a time.

Sigma (Σ) Greek letter that represents addition and is often used to label the sum output bits of a parallel adder.

Sigma/Delta Modulation Method of sampling ananalog signal and converting its data points into a bit stream of serial data.

Sign Bit Binary bit that is added to the leftmost position of a binary number to indicate whether that number represents a positive or a negative quantity.

Sign-Magnitude System A system for representing signed binary numbers where the most significant bit represents the sign of the number and the remaining bits represent the true binary value (magnitude).

Simple PLD (SPLD) A PLD with a few hundred logic gates and possibly a few programmable macrocells available.

Simulator Computer program that calculates the correct output states of a logic circuit based on a description of the logic circuit and on the current inputs.

Spike *See* Glitch.

SSI Small-scale integration (fewer than 12 gates).

Staircase Test Process by which a digital-to-analog converter's digital input is incremented and its output monitored to determine whether or not it exhibits a staircase format.

Staircase Waveform Type of waveform generated at the output of a digital-to-analog converter as its digital input signal is incrementally changed.

Standard Cell An application-specific integrated circuit (ASIC) made of predesigned logic blocks from a library of standard cell designs that are interconnected during the system design stage and then fabricated on a single IC.

Standard Logic The large assortment of basic digital IC components available in various technologies as MSI, SSI chips.

State Machines A sequential circuit that advances through several defined states.

State Table A table whose entries represent the sequence of individual FF states (i.e., 0 or 1) for a sequential binary circuit.

State Transition Diagram A graphic representation of the operation of a sequential binary circuit, showing the sequence of individual FF states and conditions needed for transitions from one state to the next.

Static Accuracy Test Test in which a fixed binary value is applied to the input of a digital-to-analog converter and the analog output is accurately measured. The measured result should fall within the expected range specified by the digital-to-analog converter's manufacturer.

Static RAM (SRAM) Semiconductor RAM that stores information in flip-flop cells that do not have to be periodically refreshed.

STD_LOGIC In VHDL, a data type defined as an IEEE standard. It is similar to the BIT type, but it offers more possible values than just 1 or 0.

STD_LOGIC_VECTOR In VHDL, a data type defined as an IEEE standard. It is similar to the BIT_VECTOR type, but it offers more possible values than just 1 or 0 for each element.

Step Size *See* Resolution.

Straight Binary Coding Representation of a decimal number by its equivalent binary number.

Strobe Another name for an enable input usually used to latch a value into a register.

Strobing Technique often used to eliminate decoding spikes.

Structural Level of Abstraction A technique for describing a digital circuit that focuses on connecting ports of modules with signals.

SUBDESIGN Keyword in AHDL used to begin a circuit description.
Substrate Piece of semiconductor material that is part of the building block of any digital IC.
Subtrahend Number that is to be subtracted from a minuend.
Successive-Approximation ADC Type of analog-to-digital converter in which an internal parallel register and complex control logic are used to perform the conversion. The conversion time for this type of analog-to-digital converter is always the same regardless of the value of the input analog signal.
Sum-of-Products Form Logic expression consisting of two or more AND terms (products) that are ORed together.
Supercomputers Computers with the greatest speed and computational power.
Surface Mount A method of manufacturing circuit boards whereby ICs are soldered to conductive pads on the surface of the board.
Synchronous Control Inputs *See* Control Inputs.
Synchronous Counter Counter in which all of the flip-flops are clocked simultaneously.
Synchronous Systems Systems in which the circuit outputs can change states only on the transitions of a clock.
Synchronous Transfer Data transfer performed by using the synchronous and clock inputs of a flip-flop.
Syntax The rules defining keywords and their arrangement, usage, punctuation, and format for a given language.

Test Vector Sets of inputs used to test a PLD design before the PLD is programmed.
Timing Diagram Depiction of logic levels as related to time.
Toggle Mode Mode in which a flip-flop changes states for each clock pulse.
Toggling Process of changing from one binary state to the other.
Top-Down A design method that starts at the overall system level and then defines a hierarchy of modules.
Totem-Pole Output Term used to describe the way in which two bipolar transistors are arranged at the output of most TTL circuits.
Transducer Device that converts a physical variable to an electrical variable (for example, a photocell or a thermocouple).
Transmission Gate *See* Bilateral Switch.
Transparent Of a *D* latch, operating so that the *Q* output follows the *D* input.
Trigger Input signal to a flip-flop or one-shot that causes the output to change states depending on the conditions of the control signals.
Tristate Type of output structure that allows three types of output states: HIGH, LOW, and high-impedance (Hi-Z).
Truth Table Logic table that depicts a circuit's output response to the various combinations of the logic levels at its inputs.
TTL (Transistor/Transistor Logic) Integrated-circuit technology that uses the bipolar transistor as the principal circuit element.
2's-Complement Form Result obtained when a 1 is added to the least significant bit position of a binary number in the 1's-complement form.
Type The attribute of a variable in a computer-based language that defines its size and how it can be used.

ULSI Ultra-large-scale integration (100,000 or more gates).
Unasserted Term used to describe the state of a logic signal; synonymous with "inactive."
Undersampling Acquiring samples of a signal at a rate less than twice the highest frequency contained in the signal.
Unipolar ICs Integrated digital circuits in which unipolar field-effect transistors (MOSFETs) are the main circuit elements.
Up Counter Counter that counts upward from 0 to a maximum count.
Up/Down Counter Counter that can count up or down depending on how its inputs are activated.
Up/Down Digital-Ramp ADC Type of analog-to-digital converter that uses an up/down counter to step up or step down the voltage from a digital-to-analog converter until it intersects the analog input.

VARIABLE A keyword in AHDL used to begin a section of the code that defines the names and types of data objects and library primitives. A keyword used in VHDL to declare a local data object within a PROCESS.
Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) A hardware description language developed by the Department of Defense to document, simulate, and synthesize complex digital systems.
VLSI Very large-scale integration (10,000 to 99,999 gates).
Volatile Memory Memory requiring electrical power to keep information stored.
Voltage-Controlled Oscillator (VCO) Circuit that produces an output signal with a frequency proportional to the voltage applied to its input.
Voltage-Level Translator Circuit that takes one set of input voltage levels and translates it to a different set of output levels.
Voltage-to-Frequency ADC Type of analog-to-digital converter that converts the analog voltage to a pulse frequency that is then counted to produce a digital output.

Weighted Average An average calculation of a group of samples that assigns a different weight (between 0.0 and 1.0) to each sample.

Wired-AND Term used to describe the logic function created when open-collector outputs are tied together.

Word Group of bits that represent a certain unit of information.

Word Size Number of bits in the binary words that a digital system operates on.

WRITE Term used to describe the condition when the CPU is sending data to another element.

Write Operation Operation in which a new word is placed into a specific memory location.

ZIF Zero-insertion-force IC socket.