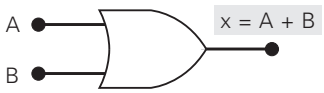
BOOLEAN THEOREMS

1.	$x \cdot 0 = 0$	2.	$x \cdot 1 = x$	3.	$x \cdot x = x$
4.	$x \cdot \overline{x} = 0$	5.	$x + 0 = x$	6.	$x + 1 = 1$
7.	$x + x = x$	8.	$x + \overline{x} = 1$	9.	$x + y = y + x$
10.	$x \cdot y = y \cdot x$	11.	$x + (y + z) = (x + y) + z = x + y + z$	12.	$x(yz) = (xy)z = xyz$
13a.	$x(y + z) = xy + xz$	13b.	$(w + x)(y + z) = wy + xy + wz + xz$	14.	$x + xy = x$
15a.	$x + \overline{x}y = x + y$	15b.	$\overline{x} + xy = \overline{x} + y$	16.	$\overline{x + y} = \overline{x}\,\overline{y}$
17.	$\overline{xy} = \overline{x} + \overline{y}$				

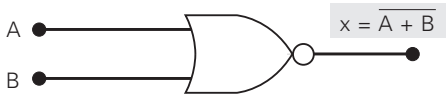
LOGIC GATE TRUTH TABLES

A	B	OR $A + B$	NOR $\overline{A + B}$	AND $A \cdot B$	NAND $\overline{A \cdot B}$	XOR $A \oplus B$	XNOR $\overline{A \oplus B}$
0	0	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	1	0	1	0	0	1

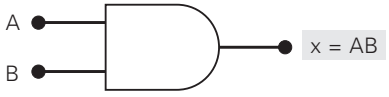
LOGIC GATE SYMBOLS



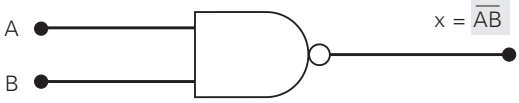
OR Gate



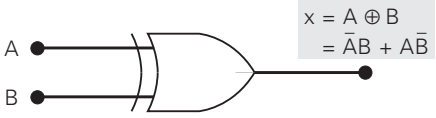
NOR Gate



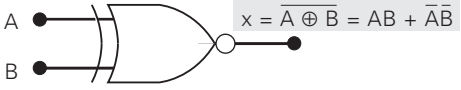
AND Gate



NAND Gate



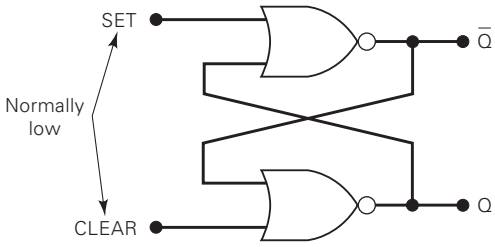
XOR

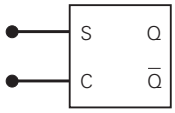


XNOR

FLIP-FLOPS

NOR Latch

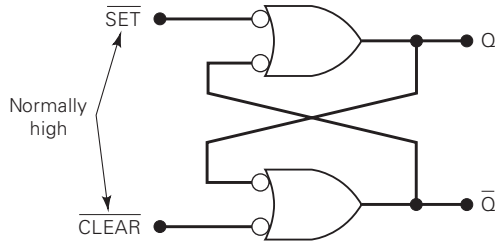


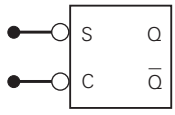


(Alternate symbol)

S	C	Q
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid

NAND Latch

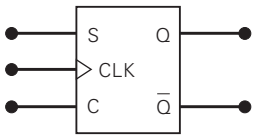




(Alternate symbol)

S	C	Q
0	0	Invalid
1	0	Q = 1
0	1	Q = 0
1	1	No change

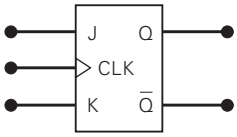
Clocked S-C



S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

↓ of CLK has no effect on Q

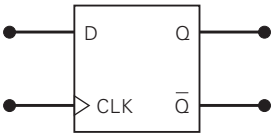
Clocked J-K



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggles)

↓ of CLK has no effect on Q

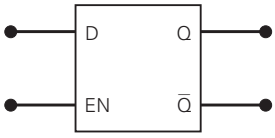
Clocked D



D	CLK	Q
0	↑	0
1	↑	1

↓ of CLK has no effect on Q

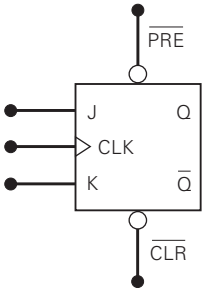
D Latch



EN	D	Q*
0	X	No change
1	0	0
1	1	1

*Q follows D input while EN is HIGH

Asynchronous Inputs



$\overline{PRE}$	$\overline{CLR}$	Q*
1	1	No effect; FF can respond to J, K and CLK
1	0	Q = 0 independent of J, K, CLK
0	1	Q = 1 independent of J, K, CLK
0	0	Ambiguous (not used)

*CLK can be in any state