It is important that the thickness is very uniform over the entire length, because sudden changes in the diameter can lead to fracture of the wire or damage to the wafer surface. The abrasion of the steel wires is also due to the interactions with the grains. Excessive wear can lead to breakage, which is undesirable during sawing because it is very time consuming to build up the wire web inside the machine. Some manufacturers are beginning to develop *in situ* detection systems to control the sawing process and thus prevent the wire breakage.

6.4.4 Cost and Size Considerations

The investigations of the microscopic processes of wire sawing have laid the basis for the selection of the best range of parameters and for further modifications. It allows one to increase the sawing performance, to reduce the consumption of slurry, SiC powder, wire material and etchant, and hence directly the costs of slicing. Furthermore, the quality of the wafers such as roughness, flatness and saw damage of the surfaces can be improved. This is important in view of the development of thinner wafers for solar cells, which will reduce the consumption of expensive silicon. The current sawing technique in production allows the sawing of wafers with thickness down to about 200 μm. The goal is to further reduce the thickness to about 100 to 150 μm in production. Sawing of thinner wafers is possible but at present still at the expense of more breakage. The problem becomes even more severe when the wafer size increases at the same time to $15 \times 15\ \text{cm}^2$ or more. In mass production such a development will only become possible by a careful selection of the parameter range and an *in situ* control of all the factors that determine the slicing process.

6.5 SILICON RIBBON AND FOIL PRODUCTION

Research and development on crystal growth technologies for production of crystalline silicon ribbon have been under way for three decades. Interest in methods of crystalline silicon wafer production was initiated during the oil crises of the mid-1970s. Out of this period arose the first large-scale efforts in R&D to develop low-cost methods of producing substrates for solar cell manufacture. A seminal program was conducted in the US, which was led between 1975 and 1985 by the Jet Propulsion Laboratory (JPL) Flat Plate Array Project [41]. It was the activity in this project in this time period, combined with larger investments from the private sector both in the US and internationally, that developed the seeds of the technology of crystalline silicon ribbon and foil production methods being commercialised today.

The past decade of R&D on crystalline silicon materials has culminated in the expansion of wafer manufacturing at an unprecedented pace. While established methods of production based on Cz growth, directional solidification and ingot casting have flourished, a new generation of ribbon technologies has moved past the R&D stage into large-scale manufacturing and is in competition with these conventional approaches. Ribbon technologies, some of which had entered R&D already in the early 1970s, and have now reached maturity with the start up of manufacturing on a megawatt (MW) scale, include Edge-defined Film-fed Growth (EFG), String Ribbon (STR) and Silicon Film™ (SF).