

EFG and SF ribbon technology have successfully completed their initial scale up of wafer production to the multi-megawatt level. Process control and equipment reliability improvements, which can drive throughput and yield higher, become increasingly more dominant in determining the manufacturing cost. As throughput per furnace increases, capital cost impact on variable manufacturing costs from the growth furnace decreases. There is pressure on all ribbon technologies to concentrate on reducing the capital cost of the wafer production equipment if the transition to large-scale wafer manufacturing of 50- to 100-MW annual capacity factories is to be sustained.

Process variable ranges are firmly established for the EFG process. Octagon tube length, throughput and wafer thickness parameters will remain within the ranges given in Table 6.4 for the next generation of equipment, while octagon face width, and hence the EFG wafer dimension, will increase from 10 to 12.5 cm. The major thrust in R&D on the EFG process in this phase will be on process control and process and equipment automation.

The benefits of the savings in silicon feedstock and potential gains in cell efficiency with a reduction of the ribbon/foil thickness are well understood for all these technologies. However, the pressure to carry out R&D in this direction for the case of wafers made from ribbons is not as acute as for conventional crystalline silicon wafer manufacturing methods because of the large benefit in feedstock savings already realised for ribbons on account of their favourable geometry. The R&D for the next generation of vertical ribbon technology beyond about five years will target the demonstration of production methods for very thin wafers. A strong motivator driving thickness reduction will be the pressure to increase the cell efficiency, which is seen to be capped in the 16 to 17% range (see Table 6.6) for current cell designs and wafer bulk quality. Low-cost cell designs, which can break this barrier and achieve desired targets of 18 to 20% for ribbon, are most easily found for thinner wafers, but this also requires improvements in bulk electronic quality to be achieved concurrently.

The major problem in this development for all vertical growth techniques will be to find methods to reduce the effects of thermal stress. At present, the only means by which this can be done is to reduce the pull speed. The cylinder geometry has the potential to offer some relief to the EFG process at the expense of having to work with thin curved wafers in cell and module processing. Although thermal stress is not a problem with substrate-assisted growth techniques, there probably will be a trade-off between good bulk quality with large grains and throughput.

6.6 NUMERICAL SIMULATIONS OF CRYSTAL GROWTH TECHNIQUES

Commercial finite element simulation tools for structural analysis in computer-aided engineering started to develop at the beginning of the seventies. Today, simulation tools are an essential part in various industry productions; see crash test simulation for automobile development or airflow simulations in the aerospace industry. As an advanced application the descriptions of whole production processes are the goal of the strategies for simulations. If these strategies are successful, computer modelling opens the opportunity to shorten development time for production facilities, to reduce the costs for the