Table 8.2 A summary of various TF-Si solar cells [35–37]

Technique	Institution	Temperature [°C]	Substrate	Processing	Efficiency	Remarks
ZMR	Mitsubishi Electric Co.	>1300	SiO_2 on MG-Si	LPCVD 50–60 micron active layer, alkaline wet etching, P in diffusion, H passivation by ion implantation, DARC, backside etching for rear electrode	4.2%, 100 cm^2 (1993) 16.4%, 4 cm^2	Recrystallization speed = 1 mm/s
	FhG-ISE	>1300	Perforated SiO_2 on Si	No seeding, no texture, no defect passivation, interdigitated grid, 30 micron by thermal CVD	6.1%, 4 cm^2 (1996)	9.3% by Large-Area Recrystallisation (LAR)
		>1300	Graphite	Interdigitated grid, reactive ion etching	11.0%, 4 cm^2 (1997)	9.3% on ceramic, >17% expected for screen printing
SPC	Sanyo Electric Co.	600	Metal	PECVD p-type a-Si:H (SiH_4), ITO sputtering, evaporation of Ag finger contacts	9.2%, 1 cm^2 (1994)	10-um a-Si, 10–600 min annealing
LPE	Astropower Inc.	~1000	Graphite cloth	Gas phase P in diffusion, PECVD H passivation, photolithographic contacts, DARC	13.4%, 1 cm^2 (1994)	Si directly deposited on substrate, active layer = 80 μm
			n/r	$POCl_3$, Al gettering, H passivation, PECVD SiO_2 as ARC	14.6%, 1 cm^2 (1996)	Film thickness unknown
			n/r	n/r	16.6%, 1 cm^2 (1997)	Record thin-film Si on foreign substrate, no vacuum process