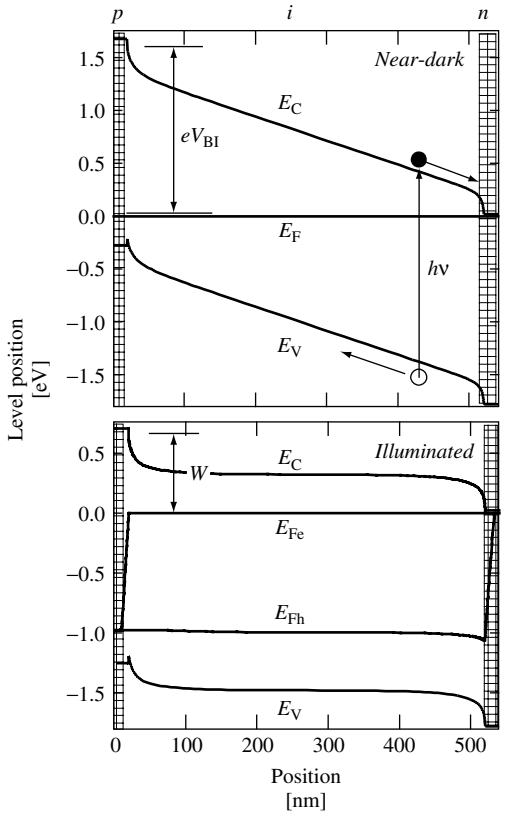

Figure 12.14 Bandedge and Fermi-level profiles in a *pin* solar cell under open-circuit conditions. The open-circuit voltage is precisely the value of E_{Fh} at the left interface ($x = 0$). The built-in potential V_{BI} is illustrated. Note that the p-layer has a slightly (0.2 eV) larger band gap than the i-layer; the calculation assumes symmetrical offsets of the valence and conduction bands at the p/i interface

for an a-Si:H-based *pin* solar cell in the dark and under illumination. The figure is based on calculations using the AMPS-1D© computer program [122, 123] and an idealized set of parameters to describe a-Si:H [124].[6] The electric field $F(x)$ within the device causes all electron level energies such as E_C and E_V to vary in space in the same way; for E_C the expression is $eF(x) = \partial E_C(x)/\partial x$.

Where do these built-in electric fields come from? In isolation, p-type and n-type materials have very different Fermi energies; in the calculation of Figure 12.14, we assumed that E_F was 1.7 eV below E_C for the p-layer and was 0.05 eV below E_C for the n-layer. When the *pin* device is assembled, these Fermi energies must be equalized to create thermal equilibrium. Electrons are donated from the n-layer to the p-layer, which generates a built-in electric field; while the level positions such as E_C and E_V now vary

[6] Many computer modeling codes have been developed; Schropp and Zeman give a good overview in Section 6.1 of their monograph [123].