J_{SC} or FF is reduced sharply. With a smaller spike, electrons can be transported across the interface assisted by thermionic emission [185]. On the other hand, for sufficiently negative ΔE_C the induced type inversion of the Cu(InGa)Se_2 near the interface is eliminated and interface state recombination will limit V_{OC}. An ODC layer at the surface of the absorber layer increases the band gap and primarily affects the valence band [188], so it may enhance type inversion near the junction. However, there is no convincing evidence that this layer exists in devices, so it is not shown in Figure 13.19.

Owing to its importance in the electronic behavior of Cu(InGa)Se_2/CdS devices, several efforts have been made to calculate or measure ΔE_C with varying results. Band-structure calculations gave $\Delta E_C = 0.3$ eV [189]. XPS and ultraviolet photoelectron spectroscopy (UPS) measurements of the valence band alignment indicate a positive ΔE_C between 0.2 and 0.7 eV [52, 190, 191]. These electron spectroscopy methods require ultrahigh vacuum conditions that necessitates that the CdS is deposited by vacuum evaporation. It is possible that the interface formation is different when CdS is grown by chemical bath deposition, for example, due to chemical interdiffusion, resulting in a different alignment of the conduction bands. Indirect measurements of the junction formed with chemical bath deposited CdS using a surface photovoltage technique gave $\Delta E_C = -0.1$ eV [192]. Finally, inverse photoemission spectroscopy showed that substantial chemical intermixing occurs across the interface resulting in $\Delta E_C = 0$ [193].

13.5.4 Wide and Graded Band Gap Devices

While the highest efficiency devices generally have Ga/(In + Ga) $\approx$ 0.1–0.3 giving $E_g \approx$ 1.1–1.2 eV, significant effort has been made to develop high-efficiency solar cells based on wider band gap alloys. This is driven primarily by the expectation that wider band gap alloys will yield higher module efficiencies due to reduced losses related to the trade-off between higher voltage and lower current at maximum power. The resulting reduction in power loss, proportional to I^2R, can be used to either (1) increase the module's active area by reducing the spacing between interconnects or (2) decrease the optical absorption in the TCO layers since they can tolerate greater resistance. Wider band gap should give a lower coefficient of temperature for the device or module output power, which will improve performance at the elevated temperatures experienced in most real terrestrial applications. Wide band gap devices could also be used as the top cell in a tandem or multijunction cell structure.

The wider band gap materials that have attracted the most attention for devices are Cu(InGa)Se_2 and $CuInS_2$. $CuGaSe_2$ has $E_g = 1.68$ eV, which is well suited for the wide band gap cell in tandem structures. $CuInS_2$ has $E_g = 1.53$ eV, which could be nearly optimum for a single-junction device. The highest-efficiency devices based on $CuInS_2$ are deposited with Cu-rich overall composition and then the excess Cu, in the form of a Cu_xS second phase, is etched away before CdS deposition [194]. Cu(InAl)Se_2 solar cells have also been considered [195]. Since $CuAlSe_2$ has $E_g = 2.7$ eV, the alloy requires smaller changes in relative alloy concentration and lattice parameter from $CuInSe_2$ than the Ga alloys to achieve comparable band gap. The highest efficiency devices of different alloys are listed in Table 13.5.

The effects of Ga incorporation on device behavior are not fully understood. The addition of a small amount of Ga to $CuInSe_2$ increased the open-circuit voltage even when