NAME: **Section A1** **CE141 LONG EXAM 1**

PART I. Write the letter of the corresponding answer. *(1.5 pts each)*

R 1. Components like electronic circuits, power supplies, cables, racks, and other physical entities
PP 2. A set of contiguous memory where items are added and retrieved in a LIFO basis
FF 3. The use of binary patterns to encode the control signals for each step of an instruction
A 4. Signal that indicates the CPU has placed a new address over the address bus
SS 5. Microprogramming technique where bits are encoded to reduce length of microinstruction
KK 6. Keeps track of next instruction to be fetched
P 7. Set of unique addresses that can be specified over the address bus
G 8. Request that is processed after the complete execution of the current machine cycle
JJ 9. Instructions that change the content of the program counter
B 10. Different ways to specify the address of an operand
N 11. Instructions that move data between locations without operating on the data themselves
RR 12. Stores the program status word
OO 13. Length of time prior to sampling that the signal must be switched to its appropriate state
Q 14. Automatically set by certain events during arithmetic and logic operations
O 15. The instruction provides the operand address in memory
M 16. Signal that indicates to memory or I/O when to place information on the data bus
I 17. Bits that are set by the program to enable certain modes of CPU operation
X 18. The address of the operand is implicit in the opcode field of the instruction
C 19. Performs arithmetic and logic operations
W 20. The operand is included in the instruction

A. Address Strobe
B. Addressing Modes
C. Arithmetic/Logic Unit
D. Base Register
E. Based Index Mode
F. Based Mode
G. Bus Request
H. Byte
I. Control Bits
J. CPU Control Instructions
K. Data Manipulation Instructions
L. Data Strobe
M. Data Strobe
N. Data Transfer Instructions
O. Direct Address Mode
P. Direct Address Space
Q. Flag Bits
R. Hardware
S. Hold Time
T. Horizontal
U. I/O Address Space
V. I/O Controller
W. Immediate Mode
X. Implied Mode
Y. Index Register
Z. Indexed Mode
AA. Input
BB. Instruction Register
CC. Interrupt Request
DD. Memory
EE. Memory Address Space
FF. Microcoding
GG. Microprogram
HH. Output
II. Peripherals
JJ. Program Control Instructions
KK. Program Counter
LL. Register Direct Mode
MM. Register Indirect Mode
NN. Relative Mode
OO. Set-up Time
PP. Stack
QQ. Stack Pointer
RR. Status/Flag register
SS. Vertical

PART II. Enumeration *(1 pt each)*

Components of a Microprocessor
1. Arithmetic/Logic Unit
2. Registers
3. Control Unit

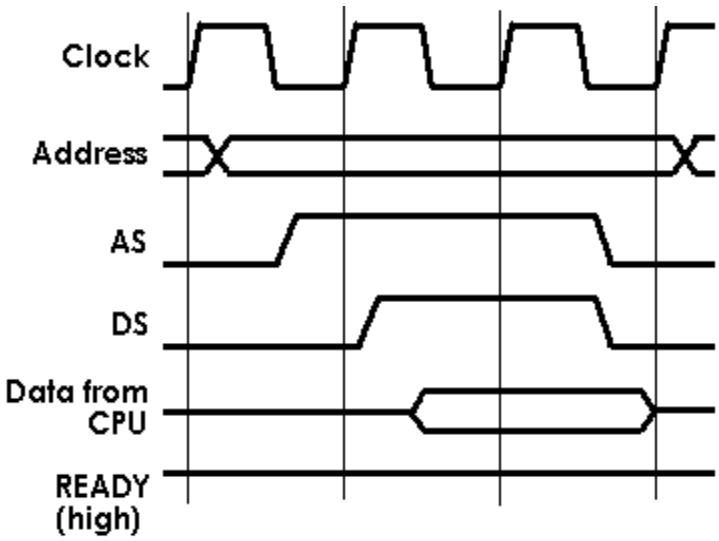
Instruction Execution Phases
4. Fetch Instruction
5. Decode Instruction
6. Determine Operand Addresses
7. Fetch Operands
8. Operate on Operands
9. Store the Result

Buses
10. Address Bus
11. Data Bus
12. Control Bus/Lines

Machine Cycles
13. Memory Read Interrupt Acknowledge
14. Memory Write Bus Grant
15. Internal Operation

PART III. Essay. Write your answers only on the lines provided. Anything written outside the lines will not be considered.

Explain what is wrong with the following **memory write cycle** timing diagram. *(5 pts)*



Why is the data bus used as basis for the categorization of the CPU (into 8-bit µP, 16-bit µP, etc)? *(5 pts)*

What is the difference between an arithmetic shift right and a logic shift right? *(5 pts)*

PART IV.

1. The Motorola 68020 has an address bus with 32 lines.
   What is the direct address space of the Motorola 68020? *(2 pts)* $2^{32} = 4{,}294{,}967{,}296$
   What is the highest address? *(1 pt)* FFFFFFFFh = 4,294,967,295
   What is the lowest address? *(1 pt)* 0

2. The Motorola 6800 is a Big Endian microprocessor. If the 16-bit words 3876h, F2EAh and 97A4h are stored in the given order, how would data appear in memory? *(6 pts)*

7100	38h	7102	F2h	7104	97h
7101	76h	7103	EAh	7105	A4h

3. Consider the Intel 8085 microprocessor. For single-byte instructions, an operand field is four bits long.
   What is the maximum number of opcodes that can be accommodated by a single-byte two address instruction? *(3 pts)* 4
   If all zeroes in either of the operand fields allow opcode expansion, how many additional instructions are accommodated? *(2 pts)* 8

4. Assume an instruction employing based indexed addressing. If the base register contains E305h, the index register contains 1011b, and the operand memory address is at 60000, what is the decimal displacement specified by the instruction? *(5 pts)* 1,872

PART V. Use the uACE programming model to answer the following questions.

Accumulator A initially contains 2Ch. The following code is then executed:

```
        LDX #3h
HERE    ASLA
        DEX
        NOP
        BNE HERE
```

How many times is the instruction ASLA repeated? *(2 pts)* executed 3x (or repeated 2x)
What is the final hexadecimal value of accumulator A? *(3 pts)* 60h
Give the decimal equivalent of the value in accumulator A. *(2 pts)* 96
The instruction ASLA is the same as performing what operation? *(3 pts)* multiplication by 2
If the above code is stored in memory starting at address E0AEh, what will the program counter contain after the code has been executed? *(3 pts)* E0B6h
BNE uses relative addressing mode. What signed displacement in hexadecimal should HERE specify? Hint: Try converting to machine code first. *(5 pts)* FBh
If the system is clocked at 2.5MHz, how long is one clock cycle? *(2 pts)* 400ns
How long would it take to execute the entire code? *(5 pts)* 15.6µs

If the above code is replaced by the following

```
        LDX #3h
HERE    ASLA
        PSHA
        DEX
        BNE HERE
        PULB
```

and the stack pointer is initially at E7FEh, what will accumulator B contain after PULB is executed? *(2 pts)* 60h
What memory location is the top of stack after the code is executed? *(3 pts)* E7FCh