NAME: **Sections B1 & B2** **CE141 LONG EXAM 1**

PART I. Write the letter of the corresponding answer. *(1.5 pts each)*

P 1. Set of unique addresses that can be specified over the address bus
GG 2. A sequence of microinstructions
Q 3. Automatically set by certain events during arithmetic and logic operations
M 4. Signal that indicates the CPU has placed information over the data bus
K 5. Instructions that perform actual data operations
KK 6. Keeps track of next instruction to be fetched
CC 7. Request that is processed after the complete execution of the current instruction
A 8. Signal that indicates the CPU has placed a new address over the address bus
B 9. Different ways to specify the address of an operand
J 10. Instructions that involve operations on the CPU status register
C 11. Performs arithmetic and logic operations
R 12. Components like electronic circuits, power supplies, cables, racks, and other physical entities
T 13. Microprogramming technique where each bit in the microinstruction corresponds to a logic signal
O 14. The instruction provides the operand address in memory
BB 15. Contains a copy of the instruction
X 16. The address of the operand is implicit in the opcode field of the instruction
S 17. How long after sampling the signal must remain in its valid state
PP 18. A set of contiguous memory where items are added and retrieved in a LIFO basis
RR 19. Stores the program status word
V 20. Controls the operation of a peripheral according to commands received from the CPU

A. Address Strobe
B. Addressing Modes
C. Arithmetic/Logic Unit
D. Base Register
E. Based Index Mode
F. Based Mode
G. Bus Request
H. Byte
I. Control Bits
J. CPU Control Instructions
K. Data Manipulation Instructions
L. Data Strobe
M. Data Strobe
N. Data Transfer Instructions
O. Direct Address Mode
P. Direct Address Space
Q. Flag Bits
R. Hardware
S. Hold Time
T. Horizontal
U. I/O Address Space
V. I/O Controller
W. Immediate Mode
X. Implied Mode
Y. Index Register
Z. Indexed Mode
AA. Input
BB. Instruction Register
CC. Interrupt Request
DD. Memory
EE. Memory Address Space
FF. Microcoding
GG. Microprogram
HH. Output
II. Peripherals
JJ. Program Control Instructions
KK. Program Counter
LL. Register Direct Mode
MM. Register Indirect Mode
NN. Relative Mode
OO. Set-up Time
PP. Stack
QQ. Stack Pointer
RR. Status/Flag register
SS. Vertical

PART II. Enumeration *(1 pt each)*

Instruction Execution Phases
1. Fetch Instruction
2. Decode Instruction
3. Determine Operand Addresses
4. Fetch Operands
5. Operate on Operands
6. Store the Result

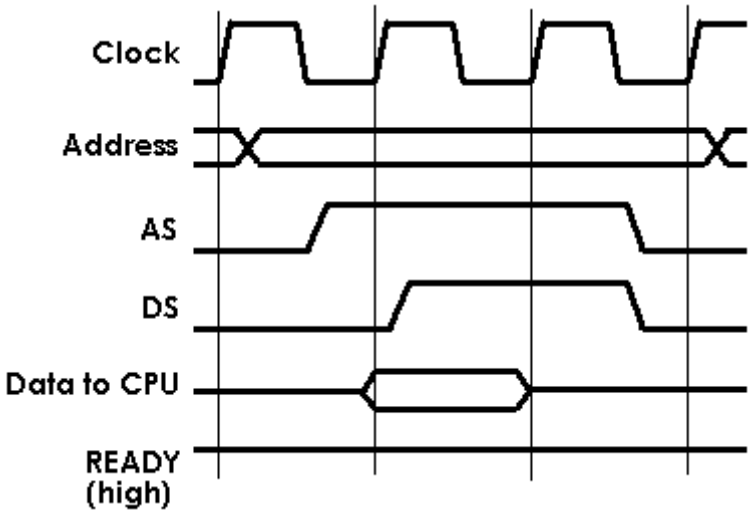
Components of a Computer
7. Central Processing
8. Memory
9. Input/Output

Types of Data Manipulation Instructions
10. Arithmetic Shift/Rotate
11. Logical String Processing
12. Bit Manipulation

Data Transfer Control Lines
13. M/IO* DS
14. R/W* AS
15. WRD/B* Ready

PART III. Essay. Write your answer only on the lines provided. Anything written beyond will not be considered.

Explain what is wrong with the following **memory read cycle** timing diagram. *(5 pts)*



Why is the data bus used as basis for the categorization of the CPU (into 8-bit μP, 16-bit μP, etc)? *(5 pts)*

What is the difference between horizontal and vertical microprogramming? *(5 pts)*

PART IV.

1. The Intel 8080 employs 20 lines to send addresses to memory and I/O.
   What is the direct address space of the Intel 8080? *(2 pts)* 2^{20} = 1,048,574
   What is the highest address? *(1 pt)* FFFFFh = 1,048,575
   What is the lowest address? *(1 pt)* 0

2. The Intel 8080 is a Little Endian microprocessor. If the 16-bit words 3876h, F2EAh and 97A4h are stored in the given order, how would data appear in memory? *(6 pts)*

7100	76h	7102	EAh	7104	A4h
7101	38h	7103	F2h	7105	97h

3. Consider the Intel 8085 microprocessor. For single-byte instructions, an operand field is four bits long.
   What is the maximum number of opcodes that can be accommodated by a single-byte one address instruction? *(3 pts)* 32
   If all zeroes in the operand field allow opcode expansion, how many additional instructions are accommodated? *(2 pts)* 32

4. A jump instruction is three bytes long and employs relative addressing. If the instruction is at E0A4h, calculate the jump address if the signed displacement is 11111010b. (5 pts) E0A1h

PART V. Use the uACE programming model to answer the following questions.

1. Accumulator A initially contains 8Ah. The following code is then executed:

```
        LDX #3h
HERE    ASRA
        DEX
        BNE HERE
```

   How many times is the instruction ASRA repeated? *(2 pts)* executed 3x (or repeated 2x)
   What is the final hexadecimal value of accumulator A? *(3 pts)* F1h
   Give the decimal equivalent of the value in accumulator A. *(2 pts)* -15
   The instruction ASRA is the same as performing what operation? *(3 pts)* division by 2
   If the above code is stored in memory starting at address E050h, what will the program counter contain after the code has been executed? *(3 pts)* E057h
   BNE uses relative addressing mode. What signed displacement in hexadecimal should HERE specify? Hint: Try converting to machine code first. *(5 pts)* FCh
   If the system is clocked at 4MHz, how long is one clock cycle? *(2 pts)* 250ns
   How long would it take to execute the entire code? *(5 pts)* 8.25µs

If the above code is replaced by the following

```
        LDX #3h
HERE    ASRA
        PSHA
        DEX
        BNE HERE
        PULB
```

and the stack pointer is initially at E7FEh, what will accumulator B contain after PULB is executed? *(2 pts)* F1h
What memory location is the top of stack after the code is executed? *(3 pts)* E7FCh