Addressable Failure Site Test Structures (AFS-TS) for Process Development and Optimization

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Abstract-Two types of addressable failure site test structures are developed. In-house program is coded to extract the electrical information and simulate the failure mode. A complete set of test structure modules for 0.25 um logic backend of line process is implemented in a test chip of 22x6.6 mm^2. By using the novel test structure, the yield analysis and defect tracking of BEOL process development as well as low-k Fluorinated SiO_2 (FSG) process optimization are demonstrated.

INTRODUCTION

THE TEST structure of process integration has shown its necessity and importance not only in the field of yield monitor of integrated circuit production line but also at the early regime of process development. The process development and control strategy by using test structure had been profiled and the expert system of analysis was designed by Lukaszek, W. and etc[1]. The test vehicle of static random access memory (SRAM) is typically used for high performance micro-processor process development and in-line process monitor[2, 3]. The force-sense type of test structures with multiplexers had been implemented to reduce chip pad counts as well as increase the testing speed and effective area of test structures[4, 5]. A novel checkerboard test structures without active devices was used to detect defect information and a generic algorithm solve the ambiguity induced by multi-defect inside a test chip[6, 7]. However, the area of probe pad is relatively larger than real chip design, which means, in order to get larger capture rate of yield killer, we have to increase the total chip area[1]. Due to the inherent purpose of process monitoring test vehicle is for process monitoring and control of volume production line, most of test structures are not suitable for short-loop process[2, 3]. For the other test vehicles, either the testing methods is required the digital tester, which are not compatible with in-line process[5, 6], or the multi-fault of the test chip will be derived from the design methodology and defect identification algorithm[6, 7]. Hence, we propose a generic test structure system for all kinds of semiconductor products, called as addressable failure site test structures (**AFS-TS**) [8, 9].

Besides the parametric extraction of test structures such as P/NMOSFET, reliability, overlay measurement, Kelvin 4-point structures, Van der Pauw and etc., the open-circuit and short-circuit of test structures for conductive layers are the major and important items of yield measurements.

In this work, we will present two types of addressable failure site test structure (**AFS-TS**) for the yield measurement of conductive layers. The simulation was performed to extract electrical characteristic of **AFS-TS** and detect the single/multi faults inside test chip. The guideline of test structure design is discussed, and followed as system implementation of in-line process. Finally, the systemic design procedure was verified by implementing the 0.25 um logic BEOL process, and process optimization of low-k Fluorinated SiO_2 (FSG) was illustrated.

DESIGN METHODOLOGY

A. Terminology and Modeling

For the convenience sake on model description, some graphic terminology has been adopted to model the geometry of layout objects inside a test structure[10]. The nodes ($N = \{ N_1, N_2, N_3 ¡ , N_k \}$) stand for the measurement points with conductive layout objects (conductive unit [**CU**]) like comb or meandering lines. The line (L) describes the measurement path between two measuring pads, either short circuit check (**SCC**) or open circuit check (**OCC**). $L = \{ L_{ij}, i, j = 1, 2, 3 ¡ , k$ (a) if i *1* j, the L_{ij} means Short Circuit Check Unit (**SCCU**); (b) If $i = j$, the L_{ij} means Open Circuit Check Unit (**OCCU**); } The whole test structure is noted by $G = (N, L)$. Figure 1 shows the schematic layouts & their geometry graphs of typical test structures. The compound test structure of comb and serpentine for conductive layers is shown in Fig. 1(a-1). $L = \{ L_{12}, L_{13}, L_{24}, L_{34} \}$ are **SCCU**s and $L = \{ L_{11_i}, L_{44_i} \}$ are **OCCU**s, which of corresponding geometry graph is in Fig. 1(a-2). The serpentine test structure of multi-nodes for conductive layers is shown in Fig. 1(b-1). $L = \{ L_{ij}, i, j = 1, 2, 3, 4, 5 \; i \; 1 \; j \}$, are **OCCU**s, which of corresponding geometry graph is in Fig. 1(b-2). The serpentine test structure for inter-connect layers is shown in Fig. 1(c-1). $L = \{ L_{12}, L_{13}, L_{24}, L_{34} \}$ are **SCCU**s and $L = \{ L_{11_i}, L_{22_i} \}$ are **OCCU**s, which of corresponding geometry graph is in Fig. 1(c-2) and Fig. 1(c-3).

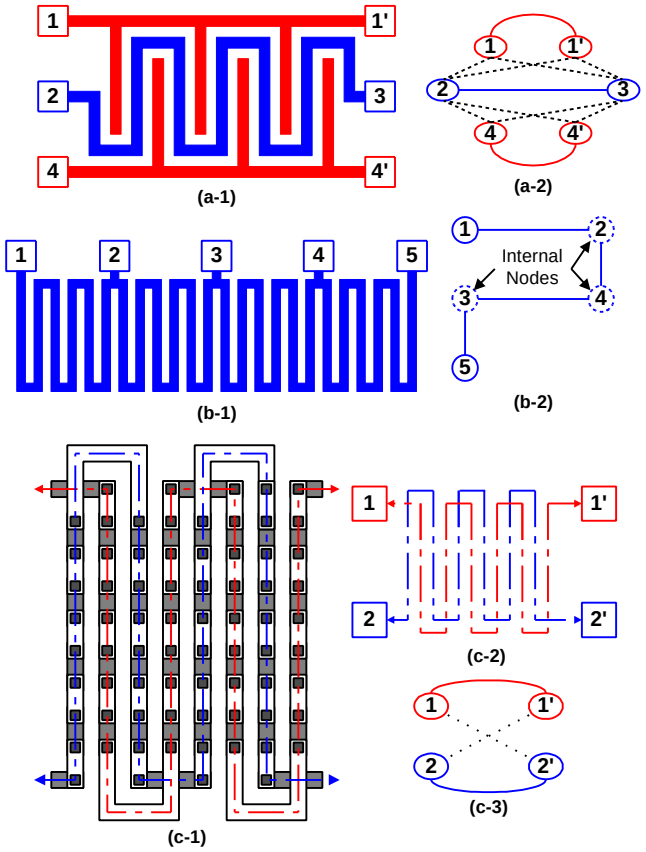

Fig. 1: Typical test structure and their geometry graphs. The solid line represents the conductive component and the dash line stands the possible leakage paths. (a-1), (b-1) Schematic layout of conductive layer. (a-2), (b-2) Geometry graph. (c-1) Schematic layout of Contact/Via chain. (c-2) Placement and routing. (c-3) Geometry graph.

B. Guideline of Test Structure Design

With the high resemblance to the actual IC design and the specific design features of addressable failure site test structure (**AFS-TS**), the systematic design flow of **AFS-TS** is thus brought up as shown in Fig. 2. First, the layout of unit cell is proposed and based on the process requirement, criteria and minimum design rule (**MDR**). The electrical specification of unit cell, such as sheet resistance for conductive layers, via/contact chains resistance for interconnects and leakage current for both can be extracted from the statistical measurement distribution of fault-free unit cell, golden device so-called. Secondly, the unit cells are put into the common placement and routine. While the different placement and routing of AFS-TS chip resulting from different design models, the inter-connect bus must be wide enough to ensure the avoidance of short-circuit and open-circuit occurring inside the bus. Typically, to ensure the lowest yield loss from interconnection bus of unit cells, the width and spacing of interconnection between unit-cells is 2~5 times **MDR** width & spacing. Then, the electrical specification of whole chip can be derived, which of value is the multiple of electrical specification of unit cell. To validate the design, in-house simulator in Matlab 5.3 is programmed to extract the voltage & leakage current spatial distribution of **AFS-TS** chip. With itinerating review on the simulation results and testing methods, an optimal testing method is thus confirmed. Finally, the optimized design of **AFS-TS** is proposed, the **AFS-TS** was implemented into silicon level. The major difference between **AFS-TS** and conventional test structure design is the electrical specification can be defined at the simulation prior to measurement and the frame of **AFS-TS** chip can be used for all kinds of test structures.

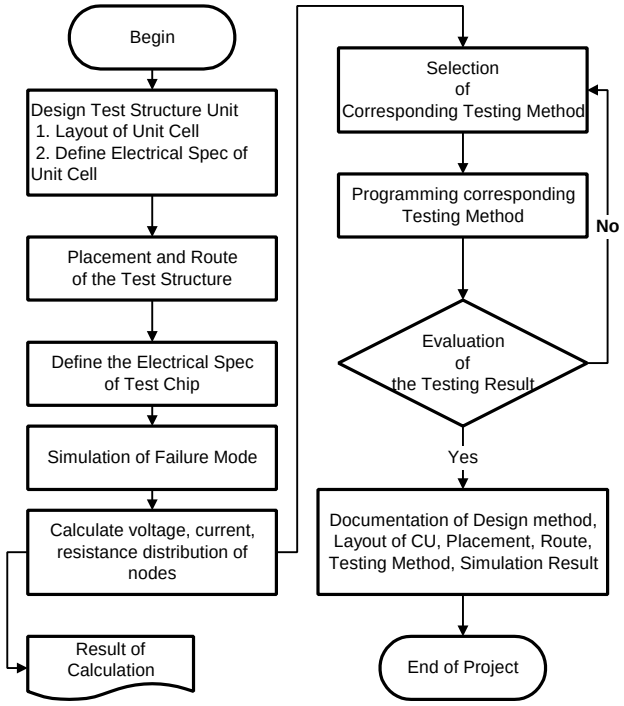

Fig. 2: The flow shows the development methodology of the novel test structure.

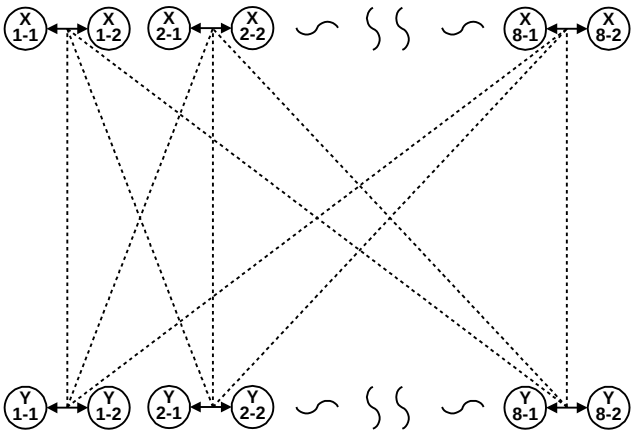

Fig. 3: Geometry graph of (16-nodes, 32 pads) (N=2*m, m=8) test structure. The test structure contains 64 ($(m-1)^2$) SCCUs in solid-line and 16 (2*m) OCCUs in dash-line.

TEST STRUCTURE DESIGN

A. Geometry Graph

Two types of **AFS-TS**, called as **XY**, **CON-Y** type, contains two orthogonal groups of test structures in **X**-, and **Y**-direction, respectively. In **XY** type, **X**- and **Y**-direction of test structures are electrically independent, but in **CON-Y** type, **Y**-direction is electrically connected in series. For the

concern of comparability of probe card used in production line, the design of probe pad is 2-by-16. In **XY**-type, ***L = {L_{XY}, X, Y = 1, 2, 3,¡ , 8}*** are **SCCU**s which of the total is 64 **SCCU**s, and ***L= {L_{XX}, L_{YY}, X, Y = 1, 2, 3,¡ , 8}*** are **OCCU**s which of the total is 16 **OCCU**s, as shown in Fig. 3. In **CON-Y** type, ***L = {L_{XY}, X = 1, 2, 3,¡ , 8; Y = 1, 2, 3,¡ , 15 }*** are **SCCU**s which of the total is 120 **SCCU**s, and ***L= {L_{XX}, L_{YY}, X = 1, 2, 3,¡ , 8; Y = 1, 2, 3,¡ , 15}*** are **OCCU**s which of the total is 23 **OCCU**s, as shown in Fig. 4.

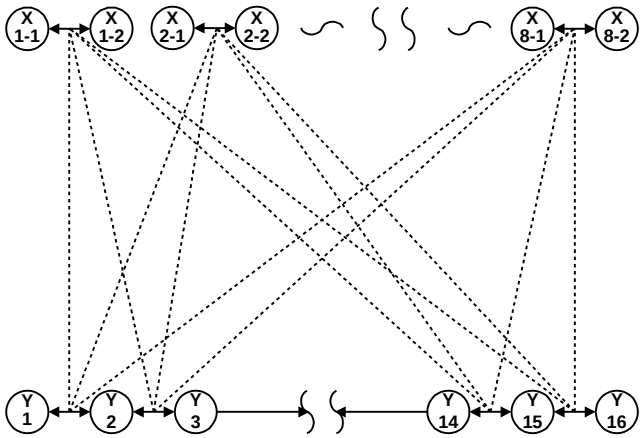

Fig. 4: Geometry graph of (24-nodes, 32 pads) test structure. The test structure contains 120 (8X15) **SCCU**s in solid-line and 23 (8+15) **OCCU**s in dash-line.

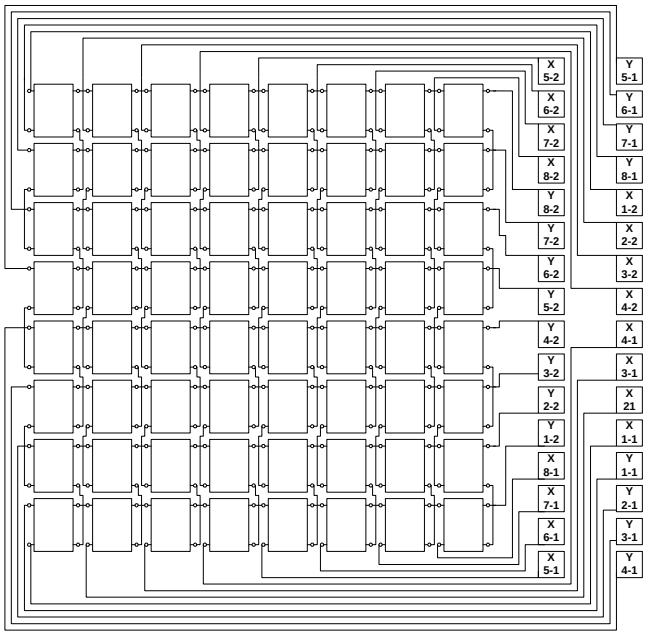

Fig. 5: Placement and routine of **XY** test structure. 32-probepads WAT test probe card is used.

B. Placement and Routing

The placement and routine of **XY** and **CON-Y** types of **AFS-TS** are shown in Fig. 5 and Fig. 6, respectively. The **AFS-TS** chip contains 8-by-8 and 15-by-8 matrixes of unit cells for **XY**, and **CON-Y** types, respectively. For **XY** type**,** the number of unit cells per node is 8 units for both X-, and Y-direction. The short circuit can be detected from every element of matrixes, which is 64 **SCCU**s. The open circuit can be detected from every row and column of matrixes, which are 8 rows and 8 columns, the total is 16 **OCCU**s. For **CON-Y** type**,** the number of unit cells per node is 8 units and 15 units for X-, and Y-direction, respectively. The short circuit can be detected from every element of matrixes, which is 120 **SCCU**s. The open circuit can be detected from every row and column of matrixes, which are 15 rows and 8 columns, the total is 23 **OCCU**s. The two level interconnect scheme is adopted as the interconnect bus between unit cells. The layout structure is the hierarchy type like IC design.

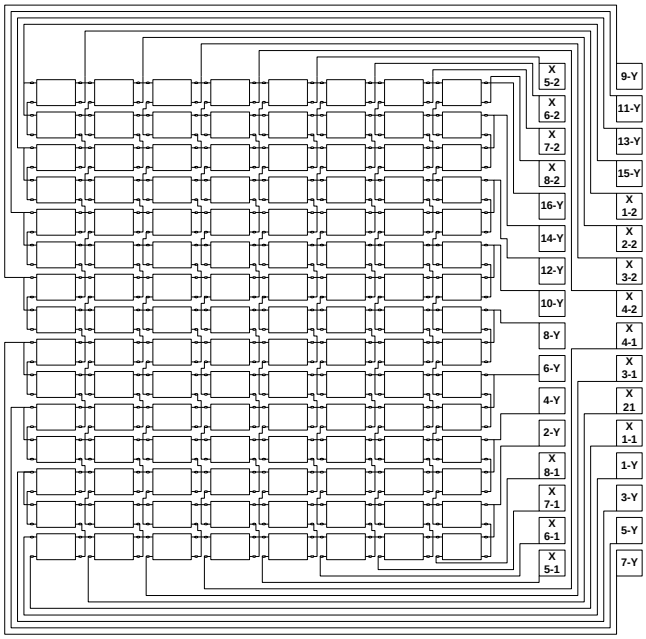

Fig. 6: Placement and routine of **CON-Y** test structure. 32-probepads WAT test probe card is used.

The unit cell contains two entangled serpentines of Via/Contact or conductive layer test structures and the schematic layout of unit cell is presented in Fig. 7. The open-circuit can be detected by forcing the constant voltage at the input port ***I_1/I_2*** then sensing the current at the output port ***O_1/O_2***. The current through the ***Port-1*** and ***Port-2*** can be used as the failure criteria of the open circuit. The short circuit can be detected by forcing the constant voltage at the port ***I_1/O_1*** then sensing the current at the port ***I_2/O_2***. The leakage current between the ***Port-1*** and ***Port-2*** can be used as the failure indicator of the short circuit.

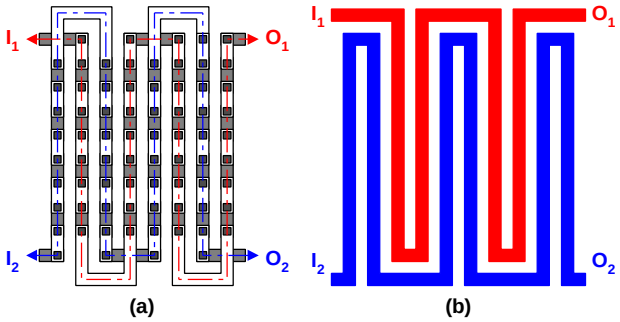

Fig. 7: Schematic layout of unit cell. (a) Schematic layout of Contact/Via chain. (b) Schematic layout of conductive layer.

B. Circuit Modeling

The resistor network model is adopted to extract the voltage and leakage current of **AFS-TS**. The nodes of **AFS-TS** are composed of several unit cells connected in series. The schematic circuits of **AFS-TS** in terms of resistors and nodes are presented in Fig. 8 and Fig. 9, for the **XY** and **CON-Y** type, respectively. For **XY**-type of **AFS-TS**, the ***RX_i,*** and ***RY_i (i = 1, 2, 3, ¡ K, 8*** are composed of 8 unit cells. The resistance of ***RX_i,*** and ***RY_i*** is the sum of the resistance of 8 unit cells. For **XY**-type of **AFS-TS**, the ***RX_i(i = 1, 2, 3, ¡ K, 8***, and ***RY_i(i = 1, 2, 3, ..., 15)*** are composed of 15 and 8 unit cells, respectively. The resistance of ***RX_i,*** and ***RY_i*** is the sum of the resistance of unitl cells. The resistance of unit cell is measured between I_1/O_1 and I_2/O_2, for the ***RX_i,*** and ***RY_i***, respectively.

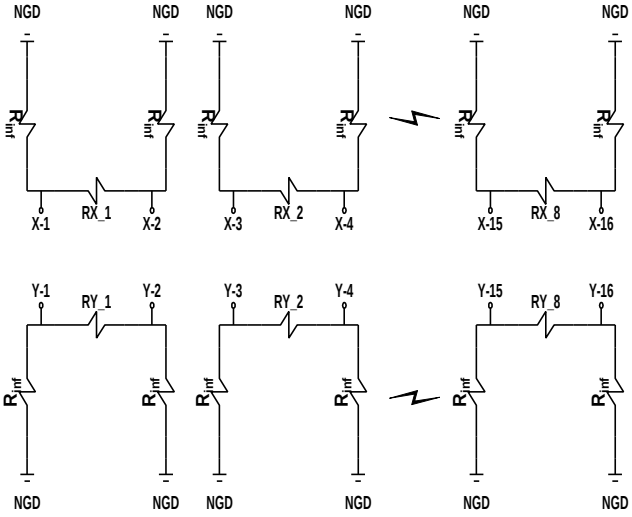

Fig. 8: The major test structure is modeled as 15*2 sub-resistors with R_{Inf} connected to ***GND***, where R_{Inf} represents leakage from measurement system.

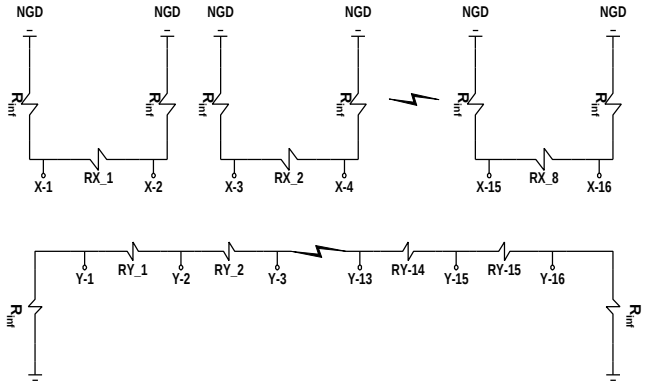

Fig. 9: The major test structure is modeled as 8+15 sub-resistors with R_{Inf} connected to ***GND***, where R_{Inf} represents leakage from measurement system.

C. Failure Simulation

For circuit simulation, the resistance of unit cell is modeled as the statistical distribution of wafer acceptance testing (**WAT**) measurement of fault-free device, golden device so-called. The resistance of defect-***M*** (Rs_{m-1}) of short circuit is modeled as a normal distribution, mean (m_{defect}) is equal to a half of mean (m_{WAT}) of **WAT** and standard deviation (s) is equal to m_{WAT} of **WAT**. R_{inf} is used as leakage current between from measurement system, and 100 **M**W is typical value used for simulation. The defect-***M*** caused short-circuit between ***Node-I*** and ***Node-J*** is modeled as Rs_{m-1}, and the resistance of ***Node-I*** and ***Node-J*** are labeled as $(R_{i-1} + R_{sm-2})$ and $(R_{j-1} + R_{sm-3})$, respectively. The resistance and location of defect-***M*** is generated by the random number generator.

The open circuit fault is defined that the resistance of unit cell is out of specification of golden devices. The measurement of open circuit is the standard **WAT** resistance measurement, which is to force I, then measure V, or to force V, then measure I. The short circuit fault is defined that the leakage current between nodes is lager than leakage current limitation dependent on the technology and process, for example in this work, $\mathbf{3.3*10^{-8}}$ Amp at **3.3** V biased is used for 0.25 um backend of line (BEOL) process test structures. The open circuit measurement is performed in each node, and the short circuit measurement is done between all of nodes. The algorithm of single and multi electrical defect detection could be found in [8, 9].

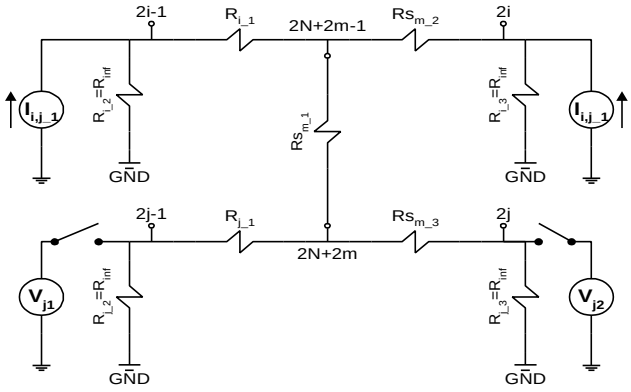

Fig. 10: Schematic graph of short-circuit model.

In order to validate the design of **AFS-TS**, a program in Matlab 5.3 was coded to solve the node voltage and the current of devices. Kirchoff¡¦s current law **KCL**) and voltage law (**KVL**) are the principles of this simulator. The nodes, short circuit and open circuit of **AFS-TS** are models as the different resistors. The voltage source is connected to each of nodes at the **X**-direction, and **GND** is connected to each of nodes at the **Y**-direction. For the measurement repeatability, the reverse circuit configuration is conducted. For **XY** type, 40 nodes for both X-, and Y-direction is simulated in Fig. 11. For **CON-Y** type, 40 and 80 nodes for both **X-**, and **Y**-direction is simulated in Fig. 12. Both of **XY**, and **CON-Y** types have three defects of short circuit located inside the **AFS-TS**. The defects are located at the peak of 3-D surface graph of leakage current. Compared with the signature of 3-D surface graph of leakage current, the peaks of **XY** type are much more abrupt at the **Y**-direction than the ones of **CON-Y** type because the nodes of **CON-Y** type at the **Y**-direction are connected in series and the nodes at the X-direction are electrically independent.

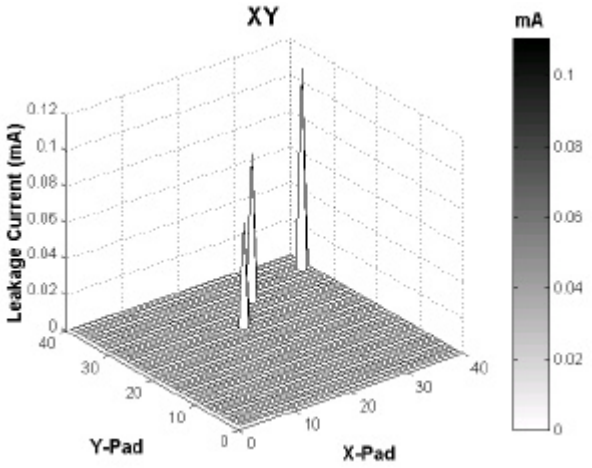

Fig. 11: 3-D surface graph of leakage current between nodes.

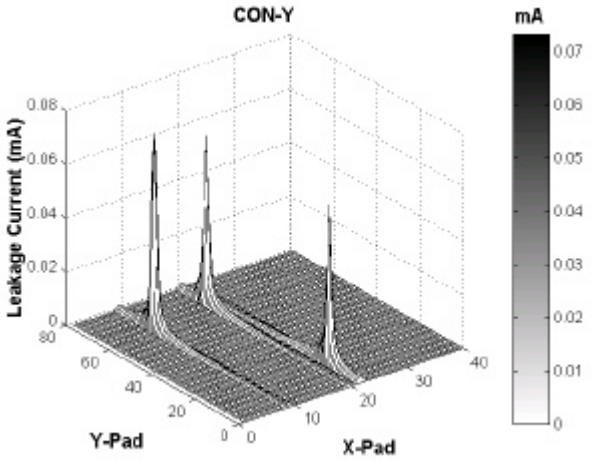

Fig. 12: 3-D surface graph of leakage current between nodes.

VALIDATION OF TEST STRUCTURE

A. Experiment and Discussion

A **t**riple-**l**ayer **m**etalization (**TLM**) systems of 0.25 um backend of line (**BEOL**) process is enacted to validate the **AFS-TS**. The set of **AFS-TS** as shown in Fig. 13 contains the test structures of sheet resistance, via resistance, stacked via resistance, and the critical **BEOL** integration process, where contains 155 dies of a wafer. The **XY**-type and **CON-Y** types are shown in Fig. 13(a) and Fig. 13(b), respectively. The wafer is fabricated on 200 mm p<100> silicon wafer deposited with a PE-oxide as buffer layer, Al-Cu(0.5%) metal and W-plug is used for via1 and via2, low-k Fluorine doped silicon glass (**FSG**) is for inter-metal dielectric-1 (**IMD-1**) and inter-metal dielectric-2 (**IMD-2)**, and the **IMD** chemical/mechanical polish (**CMP**), and W-touchup **CMP** are used as planarization process. The deep UV lithography is done for each photo-layers, except pad layer by I-line lithography.

B. Process Optimization

As the test vehicle is introduced to manufacturing line with other products, the process condition such as lithography etching time, and **CMP** polishing time are not optimized, which the yield of period-1 shows the average yield loss is around 25 % compared with the fine-tuned process shown in period-3. As lithography process is optimized at perion-2, and CMP and etching process tuning is done at period-3, the yield is back to normal condition and the yield loss is contributed by random defects. The yield trend chart of test structures is shown in Fig. 14. The stacked borderless via test structure is used as optimization index of interconnection integration process. Both of yields of open circuit and short circuit are increased as process is fine tuned. Fig. 15 show the low-k fluorine doped silicon glass process optimization, where the yields of Metal1 and Via1 modules of test structures are used as index of process optimization. It indicates that USG7K provide the worst yield of Metal1.

C. Failure Analysis of Root Process Killer

In view of the fact that the failure sites of AFS-TS can electrically defected by **WAT** data, the low yield analysis is easily performed by precisely tracking the failure site of test chip. Therefore, either electrical or physical failure analysis at specific site can be performed and timely provide the root cause of process killer. Fig. 16 shows the wafer distribution of sheet resistance of Metal1, which presents the yield of open circuit. Fig. 17 shows the wafer distribution of leakage current of Metal1, which presents the yield of short circuit(bridging). Fig. 18 displays the short circuit site of defective chip.

CONCLUSIONS

This above mentioned design methodology builds up a systematic design flow and a complete set of test structure of conductive layer and interconnection for process optimization. Defects information including site address, and related process step can be electrically characterized and located prior to physical failure analysis. With this approach, data can be quickly processed in a large volume, and the precise electrical defect density can be extracted as well. This system can thus provide a commonly used defect control tool for memory and logic semiconductor manufacturing.

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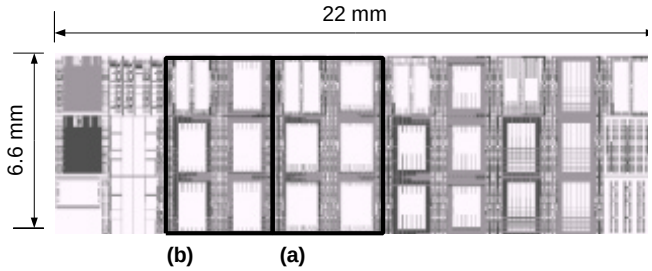

Fig. 13: Layout of addressable failure site test structures. (a)XY type. (b) CON-Y type.

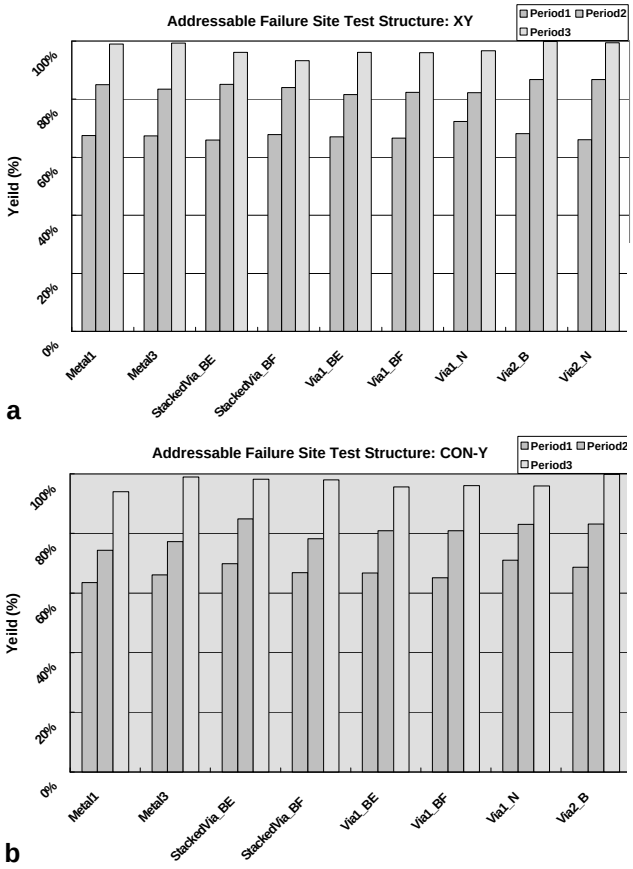

Fig. 14: The yield trends of test structure categorized by test key module. (a) XY type. (b) CON-Y type.

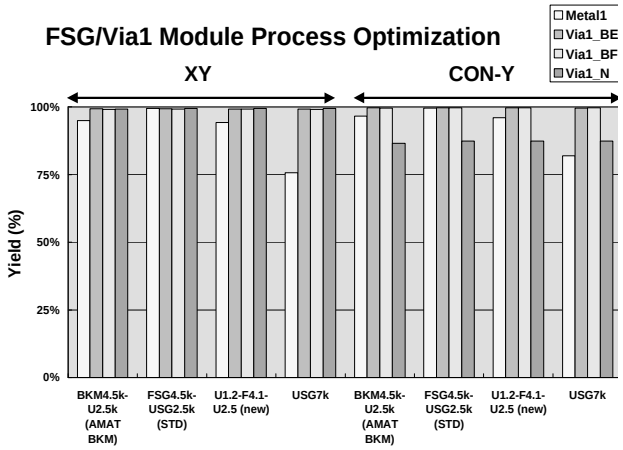

Fig. 15: The yield trends of test structure categorized by different low-k FSG inter-dielectric film process.

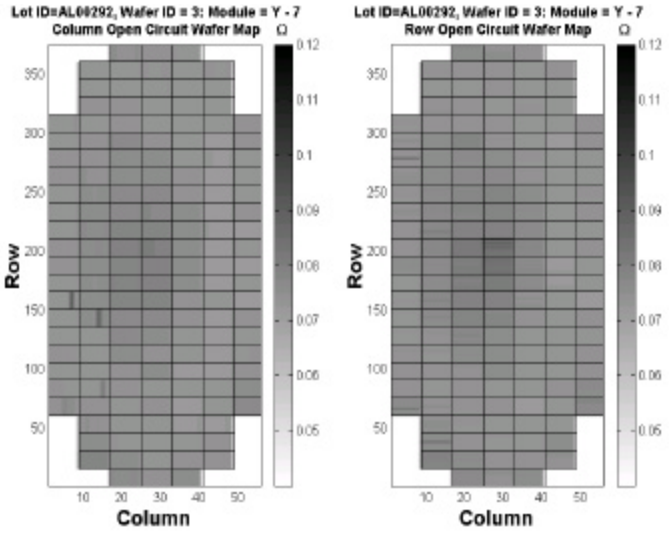

Fig. 16: Wafer map of Metal1 sheet resistance.

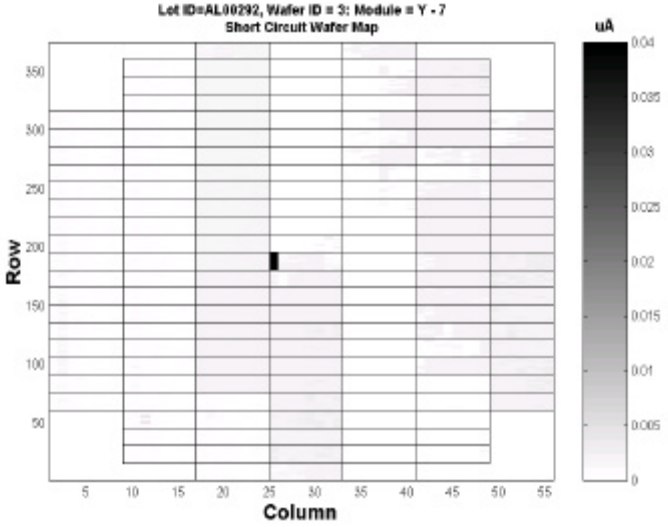

Fig. 17: Bridging fault wafer map of Metal1 test structure.

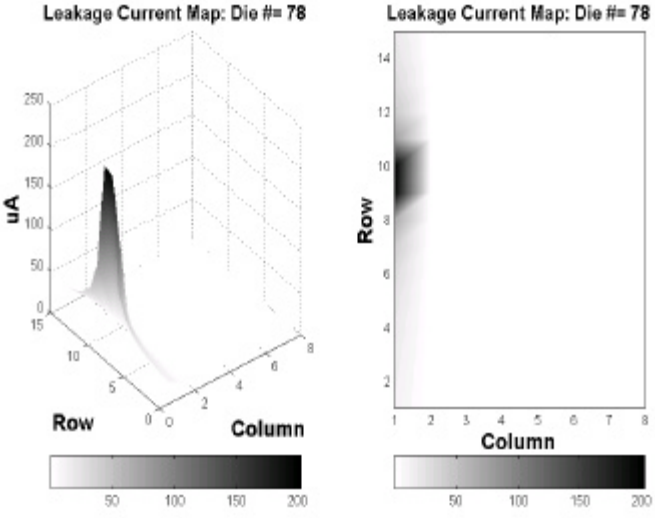

Fig. 18: Chip map of leakage current. The leakage current peak is the bridging fault.