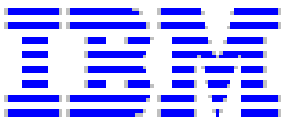

BMC Log Service Translation Guide

IBM x336

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Table of Contents

1 Introduction

1.1 Purpose

This document is intended for IBM Service and Support for the following IBM products:

- x336 all models

Since the BMC code base is common for all of these products, a single document applies. This document specifically deals with situations in which it is required that the BMC IPMI log is the only available source of machine log information. Since this log is designed to the industry standard IPMI specification, it is not formatted in a way that yields explicit service information. This document provides limited translation capabilities for trained service personnel.

When to use BMC logs:

- When a Service Processor is not present in the system, or the Service Processor has failed.
- When internal Lighpath LEDs are not readily accessible
- More Lightpath information may be needed; for example in the following cases:

NMI	LED lit
PLANAR BRD	LED lit

- The system is hung.
- The first part replaced did not fix the problem.

1.2 Viewing BMC logs

There are currently three different methods for BMC System Event Log (SEL) retrieval; BIOS SETUP/CONFIGURATION, DSA and SMBridge. This is important because each of these retrieval methods displays the SEL in a different format. Another very important point is that the majority of data in the SEL is of an informational nature and not useful for problem determination. Once an error entry is identified, this document will provide a look up for a suggested service action plan. This table lookup will be similar to looking up a POST error code in the Hardware Maintenance Manual (HMM) or Problem Determination Guide.

1.3 BIOS SETUP/CONFIGURATION VIEW

Let's look at a single SEL entry using the BIOS SETUP/CONFIGURATION view as shown below. This view can be accessed under SETUP/ ADVANCED SETUP / BMC SETTINGS / BMC SYSTEM EVENT LOG.

Three key fields are: ***Entry Number, Entry Details*** and ***Sensor Number***.

Noting that there can be up to 512 entries in the SEL, the ***Entry Number*** shows where we are in the log and helps from a navigation perspective. SEL entries also occur in chronological order, which is helpful to know when the BMC displays an uncalibrated timestamp due to its lack of a real time clock. The timestamp below is uncalibrated because the year is 1970.

The second field of interest is the ***Entry Details***. The Entry Details field is important because in the majority of cases, it will help classify the log entry is an informational or a critical error. The following key words in the Entry Details field can be used to quickly identify an informational entry:

Deasserted
Presence
Inserted/ Present
Removed / Absent
On / Off
Reset

Notice that in the example below, that none of these key words are shown. At this point we cannot conclude this is an informational message. We must now move to the final step in our classification algorithm, i.e. looking at the Sensor Number.

```
+-------------------------------------------------------------------------+
|                          BMC System Event Log                           |
+-------------------------------------------------------------------------+
|   Get Next Entry                                                        |
|   Get Previous Entry                                                    |
|   Clear BMC SEL                                                         |
|                                                                         |
|   Entry Number=       00001 / 00232                                     |
|   Record ID=          0001                                              |
|   Record Type=        02                                                |
|   Timestamp=          1970/01/14  17:44:40                              |
|   Entry Details:      Generator ID= 0020                                |
|                       Sensor Type= 09                                   |
|                       Assertion Event                                   |
|                       Power Unit                                        |
|                       OEM Specific Type                                 |
|                                                                         |
|                                                                         |
|                                                                         |
|                       Sensor Number= A8                                 |
|                       Event Direction/Type= 71                          |
|                                                                         |
|                       Event Data= A1 20 00                              |
+-------------------------------------------------------------------------+
```

Figure 1-1, SEL entry for BIOS SETUP/CONFIGURATON

In this case we see that the sensor number is A8. When using the BIOS CONFIGURATION/SETUP view, all sensor numbers are shown in hexadecimal format so A8 is more correctly written as A8h. We will now check to see if the sensor number A8h lies within the following error ranges of hexadecimal values:

15h - 2Dh
38h - 4Fh
70h - 80h
90h - 9Bh
ABh
B0h - B5h
B7h

C5h - CFh

In comparing the ranges, we see that A8h is not listed in the range of errors, so we can classify this entry as informational. Had this been an error entry we could have looked up the suggested service action by using the Sensor Number A8h as the error code.

1.4 SMBridge View

So far our classification algorithm for each entry has been:

1) Look at the Entry Details field and go to the final step, (step 2) if no keyword is found.
2) Compare the Sensor Number with known Sensor Number error ranges.

This same algorithm will now be applied to the SMBridge view. In looking at Figure 2-2, we see that the SMBridge view has very similar information to the BIOS SETUT/CONFIGURATION view. Our key fields, Entry Number, Entry Details, and Sensor Number are still shown but this time the in a more tabular form. Since the key fields are the same, the only real difference has to do with the sensor number which is displayed as an integer value proceeded by a # sign. Therefore to make our classification algorithm work, we need only to look up the error sensor number in integer range table.

The integer sensor number error ranges are as shown:

21 - 45
56 - 79
112 - 128
114 - 155
171
176 - 181
183
197 – 207

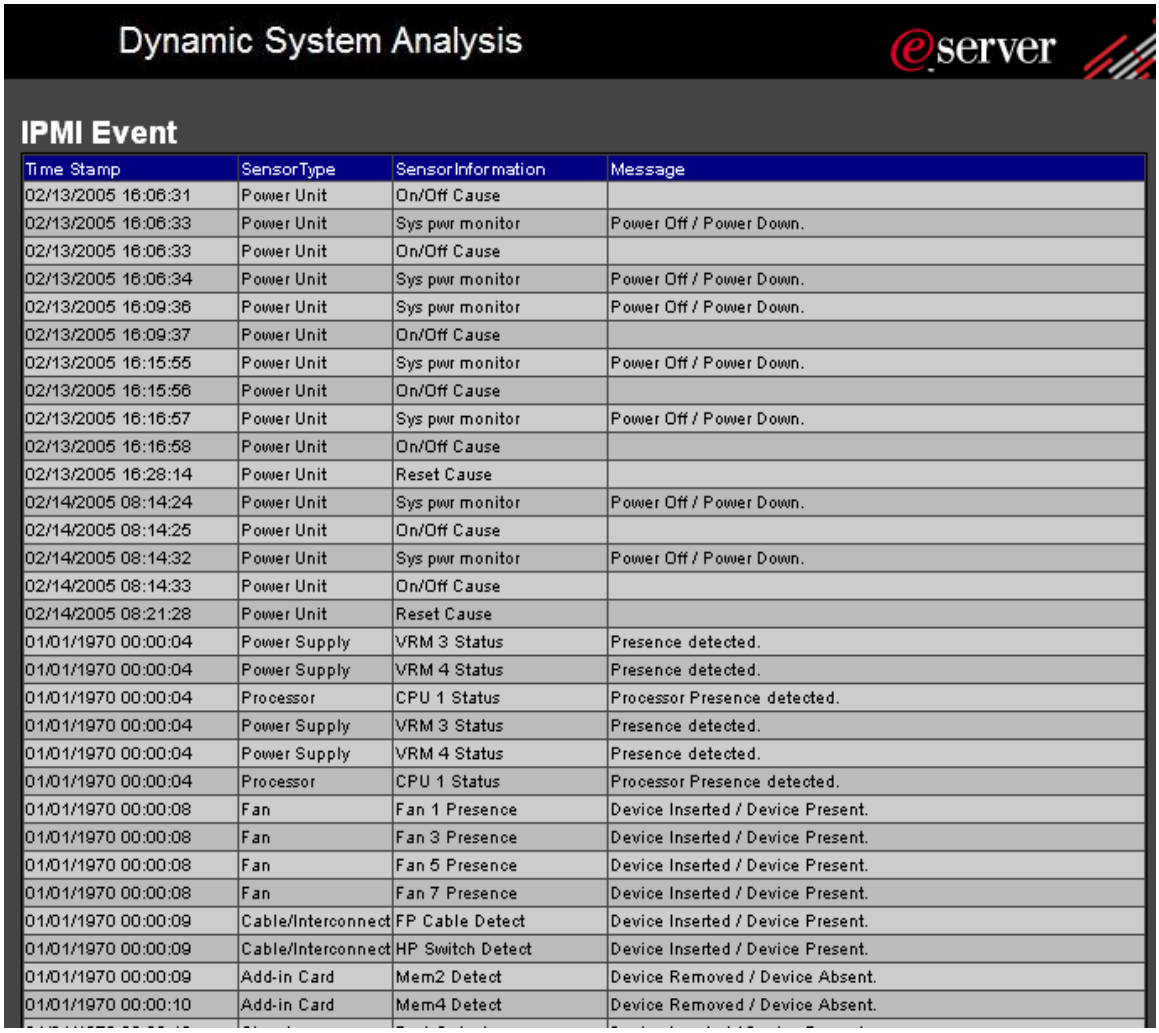
Entry Number	Timestamp	Sensor Number	Entry Details	Entry Details (continued)
1=	2005/02/02 16:46:42,	#182	OEM Reserved,	Upper Non-critical - going high (deassertion event)
2=	2005/02/02 16:46:42,	#182	OEM Reserved,	Upper Critical - going high (deassertion event)
3=	2005/02/02 16:47:40,	#168	Power Unit,	OEM
4=	1970/01/01 00:00:04,	#38	Power Supply,	Presence detected
5=	1970/01/01 00:00:04,	#39	Power Supply,	Presence detected
6=	1970/01/01 00:00:04,	#144	Processor,	Processor Presence detected
10=	1970/01/01 00:00:08,	#80	Fan,	Device Inserted/Device Present
11=	1970/01/01 00:00:08,	#82	Fan,	Device Inserted/Device Present
12=	1970/01/01 00:00:08,	#84	Fan,	Device Inserted/Device Present
13=	1970/01/01 00:00:08,	#86	Fan,	Device Inserted/Device Present
14=	1970/01/01 00:00:09,	#131	Cable,	Device Inserted/Device Present
15=	1970/01/01 00:00:09,	#134	Cable,	Device Inserted/Device Present
19=	1970/01/01 00:00:10,	#169	Power Unit,	OEM
20=	1970/01/01 00:00:10,	#173	Cable,	Device Inserted/Device Present
21=	1970/01/01 00:00:10,	#205	Cable,	State Deasserted
22=	1970/01/01 00:00:11,	#112	Power Supply,	Presence detected
23=	1970/01/01 00:00:12,	#81	Fan,	Device Inserted/Device Present
24=	1970/01/01 00:00:12,	#83	Fan,	Device Inserted/Device Present

25=	1970/01/01 00:00:12,	#85	Fan,	Device Inserted/Device Present
26=	1970/01/01 00:00:12,	#87	Fan,	Device Inserted/Device Present
27=	1970/01/01 00:00:13,	#140	Add-in Card,	Device Removed/Device Absent
28=	1970/01/01 00:00:13,	#132	Cable,	Device Inserted/Device Present
29=	1970/01/01 00:00:13,	#133	Cable,	Device Inserted/Device Present
30=	1970/01/01 00:00:14,	#160	Add-in Card,	Device Inserted/Device Present
31=	1970/01/01 00:00:14,	#162	Add-in Card,	Device Removed/Device Absent
32=	1970/01/01 00:00:14,	#168	Power Unit,	OEM
33=	1970/01/01 00:00:15,	#169	Power Unit,	OEM
34=	1970/01/01 00:00:15,	#174	Cable,	Device Inserted/Device Present

Figure 1-2, SEL, SMBridge View

1.5 DSA View

From figure 2-3, you will notice that the DSA view is slightly different. In an effort to make the log more readable, the Sensor Number has actually been looked up and translated into Sensor Information. If the Sensor Type and Message column look familiar, it's because these columns contain the same information as the Entry Details field. So from our classification algorithm perspective, the Step 1 keyword search will remain unchanged. If no keyword is found, use the Sensor Information to look up the classification and suggested service action.



Time Stamp	SensorType	SensorInformation	Message
02/13/2005 16:06:31	Power Unit	On/Off Cause	
02/13/2005 16:06:33	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/13/2005 16:06:33	Power Unit	On/Off Cause	
02/13/2005 16:06:34	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/13/2005 16:09:36	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/13/2005 16:09:37	Power Unit	On/Off Cause	
02/13/2005 16:15:55	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/13/2005 16:15:56	Power Unit	On/Off Cause	
02/13/2005 16:16:57	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/13/2005 16:16:58	Power Unit	On/Off Cause	
02/13/2005 16:28:14	Power Unit	Reset Cause	
02/14/2005 08:14:24	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/14/2005 08:14:25	Power Unit	On/Off Cause	
02/14/2005 08:14:32	Power Unit	Sys pwr monitor	Power Off / Power Down.
02/14/2005 08:14:33	Power Unit	On/Off Cause	
02/14/2005 08:21:28	Power Unit	Reset Cause	
01/01/1970 00:00:04	Power Supply	VRM 3 Status	Presence detected.
01/01/1970 00:00:04	Power Supply	VRM 4 Status	Presence detected.
01/01/1970 00:00:04	Processor	CPU 1 Status	Processor Presence detected.
01/01/1970 00:00:04	Power Supply	VRM 3 Status	Presence detected.
01/01/1970 00:00:04	Power Supply	VRM 4 Status	Presence detected.
01/01/1970 00:00:04	Processor	CPU 1 Status	Processor Presence detected.
01/01/1970 00:00:08	Fan	Fan 1 Presence	Device Inserted / Device Present.
01/01/1970 00:00:08	Fan	Fan 3 Presence	Device Inserted / Device Present.
01/01/1970 00:00:08	Fan	Fan 5 Presence	Device Inserted / Device Present.
01/01/1970 00:00:08	Fan	Fan 7 Presence	Device Inserted / Device Present.
01/01/1970 00:00:09	Cable/Interconnect	FP Cable Detect	Device Inserted / Device Present.
01/01/1970 00:00:09	Cable/Interconnect	HP Switch Detect	Device Inserted / Device Present.
01/01/1970 00:00:09	Add-in Card	Mem2 Detect	Device Removed / Device Absent.
01/01/1970 00:00:10	Add-in Card	Mem4 Detect	Device Removed / Device Absent.

Figure 1-3 SEL, DSA View

1.6 LED Control x336

Error! Reference source not found.describes the LED population on the x336.

Bit	LED Set 1	x336
0	Fault	✔
1	Info	✔
2	CPU	✔
3	VRM	✔
4	Power Supply	
5	DASD	✔
6	Fan	✔
7	DIMM	✔

Bit	LED Set 2	x336
0	Log	
1	NMI	✔
2	Non Redundant	
3	Over Spec	✔
4	Over Temp	✔
5	Diagnostic Card	
6	Service Processor	✔
7	Post OK	

Bit	LED Set 3	X336
0	Identification	✔
1	CPU Mismatch	✔
2	Any PCI	
3	Activity	✔
4	Non Optimal	
5	Select KVM	
6	Select CD	
7		

Bit	LED Set 4	X336
0	CPU 1	✔
1	CPU 2	✔
2	CPU 3	
3	CPU 4	
4	CPU 5	
5	CPU 6	
6	CPU 7	
7	CPU 8	

Bit	LED Set 5	x336
0	VRM 1	✔
1	VRM 2	✔
2	VRM 3	
3	VRM 4	
4	VRM 5	
5	VRM 6	
6	VRM 7	
7	VRM 8	

Bit	LED Set 6	X336
0	Power Supply 1	✔
1	Power Supply 2	✔
2	Power Supply 3	
3	Power Supply 4	
4	DASD 1	
5	DASD2	
6		
7		

Bit	LED Set 7	x336
0	Fan 1	✔
1	Fan 2	✔
2	Fan 3	✔
3	Fan 4	✔
4	Fan 5	✔
5	Fan 6	✔
6	Fan 7	✔
7	Fan 8	✔

Bit	LED Set 8	x336
0	Fan 9	
1	Fan 10	
2	Fan 11	
3	Fan 12	
4	Fan 13	
5	Fan 14	
6	Fan 15	
7	Fan 16	

Bit	LED Set 9	x336
0	DIMM 1	✔
1	DIMM 2	✔
2	DIMM 3	✔
3	DIMM 4	✔
4	DIMM 5	✔
5	DIMM 6	✔
6	DIMM 7	✔
7	DIMM 8	✔

Bit	LED Set 10	x336
0	DIMM 9	
1	DIMM 10	
2	DIMM 11	
3	DIMM 12	
4	DIMM 13	
5	DIMM 14	
6	DIMM 15	
7	DIMM 16	

Bit	LED Set 11	X336
0	PCI 1	
1	PCI 2	
2	PCI 3	
3	PCI 4	

4	PCI 5	
5		
6		
7		

2 Core Sensor Table

Core sensors from BMC are shown below.

Table 2-1: BMC Core Sensors

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
Power Unit Status	01h	09h	6Fh	0x00 – Power Off 0x04 – AC Lost	0x00 – Power Off	info	
BMC Watchdog	03h	23h	6Fh	0x00 – Timer Expired, status only 0x01 – Hard Reset 0x02 – Power Down 0x03 – Power Cycle		info	
SEL Full		D0h	01h	0x07 – over 75% full 0x09 – over 90% full 0x0B – 100% full		info	

3 Main Sensor Table

Thresholds for threshold based sensors are noted as shown below. Note that only a few of the assertions are actual errors. The repair actions recommendations are only for use when the sensor logs an error condition.

UNC = Upper Non-Critical	
UC = Upper Critical	
UNR = Upper Non-Recoverable	**ERROR**
LNC = Lower Non-Critical	
LC = Lower Critical	
LNR = Lower Non-Recoverable	**ERROR**
NR = Non-Redundant	
LF = Low Fuel	
OS = Over Spec	**ERROR**

Table 3-1: Sensors

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
Planar 1.5V	13h	02h	01h	LC, UC	LC, UC		Was a 12V_C Failure logged? No: Replace System Board Yes: GO to 12V_C action plan
Planar 1.8V	14h	02h	01h	LC, UC	LC, UC		*1.8 Volts powers the DDR2 Memory and the System Board* Procedure: Remove all memory DIMMs. Retest System for same 1.8v failure. 1.8V Failure Logged ? If “No” go to Step 1. If “Yes”go to Step 2. *Step 1*:Defective Memory DIMM Install one DIMM at a time. Repeat test to isolate defective DIMM. *Step 2*: With Memory DIMMs removed: Check the log for a 12V_C failure entry. ? If “No” go to Step 3. If

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
							"Yes" go to 12V_C Action plan. *Step 3*. Replace System Board.
Planar 5V	17h	02h	01h	LC, UC	LC, UC		*5 Volts is generated from 12v_C. 5 Volts powers the PCI, PCI-X, PCI-E Slots, and the IDE CDROM.* Procedure: Remove all PCI adapters. Retest system for same 5V failure. Was a 5V failure logged after the retest ? If "No" go to Step 1. If "Yes"go to Step 2. *Step 1*: Defective PCI Adapter Install one adapter at a time. Repeat test to isolate defective adapter. *Step 2*: With all adapters still removed check the log for a 12V_C failure entry? If "No" go to Step 3. If "Yes" go to 12V_C Action plan. *Step 3*: Unplug CD-ROM IDE cable from System Board. Retest , on error, replace system board.
Planar 12V A	18h	02h	01h	LC, UC	LC, UC		*12Volt_A powers VRM 1, CPU 1, and some of the Fans.* A 12V_A Over Current or Short Circuit condition has been Logged. *Step 1*: Replace Power Supply Power unit on repeat test. If failure still occurs Step 2… *Step 2*: Replace Power

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
							Backplane Power unit on repeat test. If failure still occurs Step 3… *Step 3*: Replace System Board.
Planar 12V B	19h	02h	01h	LC, UC	LC, UC		*12Volt_B powers VRM 2, CPU 2, and some of the Fans* A 12V_B Over Current or Short Circuit condition has been Logged. *Step 1*: Replace Power Supply Power unit on repeat test. If failure still occurs Step 2… *Step 2*: Replace Power Backplane Power unit on repeat test. If failure still occurs Step 3… *Step 3*: Replace System Board
Planar 12V C	1Ah	02h	01h	LC, UC	LC, UC		*12Volt_C powers the system board* A 12V_C Over Current or Short Circuit condition has been Logged. *Step 1*: Replace Power Supply Power unit on repeat test. If failure still occurs Step 2… *Step 2*: Replace Power Backplane Power unit on repeat test. If failure still occurs Step 3… *Step 3*: Replace System Board.

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
Planar - 12V	1Bh	02h	01h	LC, UC	LC, UC		*Goes to PCI, PCI-x and PCI-express connectors feed by 12V_C* Procedure: Remove all PCI adapters. Retest system for same -12V failure. Was a -12 V failure logged after the retest ? If "No" go to Step 1. If "Yes"go to Step 2. *Step 1*: Defective PCI Adapter Install one adapter at a time. Repeat test to isolate defective adapter. *Step 2*: With all adapters still removed check the log for a 12V_C failure entry? If "No" go to Step 3. If "Yes" go to 12V_C Action plan. *Step 3*: Replace System Board
Power 3V Fault	20h	09h	03h	00h – State Deasserted 01h – State Asserted			*Goes to PCI, PCI-x and PCI-express connectors feed by 12V_C* Procedure: Remove all PCI adapters. Retest system for same 3V failure. Was a 3V failure logged after the retest ? If "No" go to Step 1. If "Yes"go to Step 2. *Step 1*: Defective PCI Adapter Install one adapter at a time. Repeat test to isolate defective adapter.

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
							Step 2: With all adapters still removed check the log for a 12V_C failure entry? If "No" go to Step 3. If "Yes" go to 12V_C Action plan. *Step 3*: Replace System Board
Power 5V Fault	21h	09h	03h	00h – State Deasserted 01h – State Asserted			Same As 5 Volt Procedure
Power 12V Fault	22h	09h	03h	00h – State Deasserted 01h – State Asserted			*This is really power_good which comes from the Power Backplane* Procedure: Step 1. Check this log for the specific voltage that has failed and follow that action plan Step 2. Perform a system teardown to minimum configuration. Minimum Configuration: Minimum power configuration consists of: Fans, the On/Off operator information panel, VM1, CPU 1, Power Backplane and one power supply. All Memory DIMMs should be removed. Step 3. Power system on with this minimum configuration. Does system POST with memory beep errors, and remain powered On? If Yes: Add removed components back in one at a time using BIOS POST's inability to run or provide

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
							beep codes to determine the faulty device. If No: 1. Replace system Board and test 2. Replace Power Supply and test 3. Replace power backplane and test 4. Replace CPU 1
VRM 1 Status	24h	08h	6Fh	00h – Presence Detected 01h – Power Supply Failure	00h – Presence Detected 01h – Power Supply Failure		*The VRM error signal monitors the output voltage is in tolerance* If VRM 1 Error: 1. Reseat VRM and recheck for error. 2. Replace VRM 3. Replace CPU 1
VRM 2 Status	25h	08h	6Fh	00h – Presence Detected 01h – Power Supply Failure	00h – Presence Detected 01h – Power Supply Failure		Same As Above
Ambient Temp	32h	01h	01h				
MCH Temp	33h	01h	01h	UNC, UNR	UNC, UNR		*Memory Controller, Temperature Alert* Step 1. Ensure that the server is being properly cooled. Step 2. Check for Fan Failures Step 3. Check Memory Controller Heatsink for proper attachment. The Memory Controller Heatsink is located adjacent to CPU2 and the Memory DIMM sockets. Step 4. Replace System Board

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
DASD Temp	35h	01h	01h	UNC, UNR	UNC, UNR		*DASD temp is only available on the 2.5" backplane* DASD Temperature Alert Ensure that the server is being properly cooled. Check for Fan Failures
Fan 1 Tach	40h	04h	01h	LC	LC		*No Reading From Fan TACH* Step 1. Check connections to the fan Step 2. Reseat the Fan Step 3. Replace Fan
Fan 2 Tach	41h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 3 Tach	42h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 4 Tach	43h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 5 Tach	44h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 6 Tach	45h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 7 Tach	46h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 8 Tach	47h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 9 Tach	48h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 10 Tach	49h	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 11 Tach	4Ah	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Fan 12 Tach	4Bh	04h	01h	LC	LC		*Same Repair Action as above for all FAN Tachs*
Drive 1 Status	60h	C1h	6Fh	00h – Device/Slot Present 02h – Device Faulty	00h – Device/Slot Present 02h – Device Faulty		*Is Hard Disk Drive 0 Status LED is illuminated?* No : Ignore any message

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
							Yes: Step 1. Check that HDDs have proper air flow and cooling . Check log for fan fails or DASD overtemp. Step 2. Replace failing HDD Step 3. Replace DASD backplane. *See also OEM Sensor List*
Drive 2 Status	61h	C1h	6Fh	00h – Device/Slot Present 02h – Device Faulty	00h – Device/Slot Present 02h – Device Faulty		Same As Above *See also OEM Sensor List*
PS 1 Status	70h	08h	6Fh	00h – Presence Detected 01h – Power Supply Failure 03h – Power Supply AC Lost	00h – Presence Detected 01h – Power Supply Failure 03h – Power Supply AC Lost		*Power Supply 1, AC loss or Power Supply Failure* Step 1. Check AC Power Step 2. Replace Power Supply Step 3. Replace Power Backplane
PS 2 Status	71h	08h	6Fh	00h – Presence Detected 01h – Power Supply Failure 03h – Power Supply AC Lost	00h – Presence Detected 01h – Power Supply Failure 03h – Power Supply AC Lost		*Power Supply 2, AC loss or Power Supply Failure* Step 1. Check AC Power Step 2. Replace Power Supply Step 3. Replace Power Backplane
PS 1 Fan Fault	73h	04h	03h	00h – State Deasserted 01h – State Asserted			*The BMC is not monitoring the PS fans. Instead they are monitoring the temperature and will react to temperature changes.* Fan Fault in Power Supply 1 - Replace Power Supply 1
PS 2 Fan Fault	74h	04h	03h	00h – State Deasserted 01h – State Asserted			Fan Fault in Power Supply 2 - Replace Power Supply 2
PS 1 Overspec	76h	08h	03h	00h – State Deasserted 01h – State Asserted			N/A

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
PS 2 Overspec	77h	08h	03h	00h – State Deasserted 01h – State Asserted			N/A
NMI State	80h	13h	6Fh	00h – Front Panel NMI 03h – Software NMI			*An NMI will likely occur as a result of a Non-correctable Memory error or PCI bus Error. Check LightPath Diagnostic Panel.* Is MEM LED illuminated? No: NMI cause unknown, check other log entries such as OS logs, possible software OS reinstall needed or device driver causes. Yes: Step 1 : For PCI-A ==> Remove PCI-Express adapter from slot 2 and retest for error. On error, replace System Board. Step 2.For PCI-B ==> Remove one adapter at a time in PCI slots 1 & 2, and retest for error. With both adapters removed retest,on error replace System Board. Step 3. For PCI-C ==> Verify that the system board Ethernet contollers are working correctly. Check OS log and driver levels of system board ethernet. Replace System Board
FP Cable Detect	83h	1Bh	08h	00h – Device Removed/Absent 01h – Device Inserted/Present			On error …The Front Operator Info Panel Cable is Disconnected. Reseat Cable
USB Cable Detect	84h	1Bh	08h	00h – Device Removed/Absent 01h – Device Inserted/Present			On Error…The Front USB Cable is Disconnected Reseat Cable
RSA II	8Ch	17h	08h	00h – Device			

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
Detect				Removed/Absent 01h – Device Inserted/Present			
Fan Cable 1 Detect	8Ch	17h	08h	00h – Device Removed/Absent 01h – Device Inserted/Present			*Fan Cable 1 Detect, J30 connector, PS Fans & VRM Fan* Fan Cable 1 is disconnected or was removed. This Cable powers fans(1-3) located between the front of the system and the power supplies. Reseat Cable at J30 on the system board
Fan Cable 2 Detect	8Ch	17h	08h	00h – Device Removed/Absent 01h – Device Inserted/Present			*Fan Cable 2 Detect, J33 connector, CPU Fans* Fan Cable 2 is disconnected or was removed this cable powers the fans (4-7) located between the front of the system and the CPUs. Reseat Cable at J33 on the system board.
CPU 1 Status	90h	07h	6Fh	00h – IERR 01h – Thermal Trip 07h – Processor Presence detected 08h – Processor disabled	00h – IERR 01h – Thermal Trip 07h – Processor Presence detected 08h – Processor disabled		*CPU 1 Status* Was this a Thermal Trip ? No: If IERROR do the following: Important - Most IERRORs are caused by I/O Timeouts. Step 1. Check Firmware, Device Drivers levels for all adapters and standard devices such as ethernet or SCSI. Step 2. Run diagnostics on HDD and other I/O devices. Step 3. Replace CPU only after steps 1 and 2.
CPU 2 Status	91h	07h	6Fh	00h – IERR 01h – Thermal Trip 07h – Processor Presence detected	00h – IERR 01h – Thermal Trip 07h –		*Same Repair Action Procedure as for CPU 1 Status Error*

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
				08h – Processor disabled	Processor Presence detected 08h – Processor disabled		
CPU 1 Temp	98h	01h	01h	UNC, UNR	UNC, UNR		*CPU 1 Temperature Alert* Step 1. Check Fans and server for proper cooling Step 2. Check Heatsink is properly installed Step 3. Replace CPU *CPU 2 Temperature Alert* Step 1. Check Fans and server for proper cooling Step 2. Check Heatsink is properly installed Step 3. Replace CPU
CPU2 Temp	99h	01h	01h	UNC, UNR	UNC, UNR		
CPU 1 VCore	B8h	02h	01h	LC, UC	LC, UC		*VRM 1, Voltage Error (Vcore)* 1. Reseat VRM and recheck for error 2. Replace VRM 3. Replace CPU 1 *VRM 2, Voltage Error (Vcore)* 1. Reseat VRM and recheck for error 2. Replace VRM 3. Replace CPU 2
CPU 2 VCore	B9h	02h	01h	LC, UC	LC, UC		
CPU Vtt	BBh	02h	01h	LC, UC	LC, UC		*Vtt regulator is Feed by 12V_C* CPU Bus, Terminator Voltage Failure. Check this log for a 12V_C Failure Entry If CPU 2 is installed, remove CPU 2 and VRM 2 . Retest system for same Terminator Voltage Failure. With only CPU 1 installed, Did a CPU Bus, Terminator Voltage Failure occur?

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
CPU 1 Prochot	C0h	01h	03h	00h – State Deasserted 01h – State Asserted			Yes: Replace System Board, Retest for Same Error. If same error replace CPU 1. No: Replace VRM 2 and CPU2 . *The prochot sensors (0xC0 and 0xC1) will always generate a deassertion event when the sensor is rearmed following a power-on or cold reset of the BMC.* Warning - CPU 1 performance has been slowed due to CPU's Temperature Step 1. Check for Fan Errors Step 2. Check CPU 1 heatsink is installed properly. *The prochot sensors (0xC0 and 0xC1) will always generate a deassertion event when the sensor is rearmed following a power-on or cold reset of the BMC.*
CPU 2 Prochot	C1h	01h	03h	00h – State Deasserted 01h – State Asserted			Warning - CPU 2 performance has been slowed due to CPU's Temperature Step 1. Check for Fan Errors Step 2. Check CPU 2 heatsink is installed properly.
Machine Check	C8h	12h	03h	00h – State Deasserted 01h – State Asserted			*CPU Machine Check* Procedure: Check this log for a CPU Front Side Bus Error Was a CPU Front Side Bus Error logged? Yes: Go to CPU Front Side Bus action

Sensor Name	No.	Sensor Type	Reading Type	Logged Assertions	Logged De-Assertions	Event or Error	Repair Actions
BINIT	C9h	12h	03h	00h – State Deasserted 01h – State Asserted			plan below (BINIT). No: Step1: If CPU 2 is installed, remove CPU 2 and its VRM With only CPU 1 installed….. Retest system for same CPU Machine Check Failure Did a CPU Machine Check error occur? Yes: Replace CPU 1 No: Replace CPU 2 *BINIT# is used to signal any bus condition that prevents reliable future operation of the bus.* CPU Front Side Bus Error Step 1: If CPU 2 is installed, remove CPU 2 and its VRM. Retest system for same CPU FSB Failure Did a CPU Front Side Bus Error occur? No: Replace CPU 2 Yes: Replace System Board, then retest Repace CPU 1 if failure continues

4 OEM Sensor List

In addition to the sensors supported by the core firmware, the BMC on the x336 will implement the following sensors. Thresholds for threshold based sensors are noted as shown below.

- UNC = Upper Non-Critical
- UC = Upper Critical
- UNR = Upper Non-Recoverable
- LNC = Lower Non-Critical
- LC = Lower Critical
- LNR = Lower Non-Recoverable

There are two OEM sensor types used on the x336, the first is type C1h and is a custom Drive/Slot status sensor. The reading type will be 6Fh (Sensor Specific) and the offsets are given in the table below.

Table 4-1: OEM Drive Status Sensor Offsets

Sensor Type	Sensor Type Code	Sensor-specific Offset	Event	Repair Actions
Drive/Slot Status	C1h	00h	Drive Slot Present	
		01h	No Error	
		02h	Device Faulty	*See Main Sensor List*
		03h	Device Rebuilding	*See Main Sensor List*
		04h	In Failed Array	*See Main Sensor List*
		05h	In Critical Array	*See Main Sensor List*
		06h	Parity Check	*See Main Sensor List*
		07h	Predicted Fault	*See Main Sensor List*
		08h	Un-configured Drive	*See Main Sensor List*
		09h-15h	Reserved	

The other OEM sensor type that will be used is a LED sensor to report which LEDs are supported on each system. This sensor will be type D0h and will report a generic event/reading type code of 08h (Device Present/Absent). These records will be used solely to report LED presence, there will be no data logged in relation to these sensors.

5 BIOS Logged Events

System BIOS is able to communicate with the BMC and log architected events. There are two portions to BIOS logging – POST events, which occur during system power up, and SMI events, which are generally run time errors detected by hardware.

5.1 OEM SEL BIOS Entry Definitions

While the IPMI specification defines a wide variety of sensor types and record IDs for possible system events, IBM xSeries servers will log OEM specific messages in the BMC SEL. To provide consistency across all xSeries systems, the OEM record ID and OEM sensor type definitions will remain consistent. The table below will document each OEM record ID and sensor type used by xSeries systems as well as a text description of the event. Outside system software should use this table to provide BMC SEL NLS translations to end users.

Sensor Type	Sensor Type Code	Byte Definitions/Description
OEM POST with Time Stamp	0xC0	Byte 11 POST Error / Event Type 0x00 POST PCI POST Event/Error 0x01 POST PCI Processor Event / Error 0x02 POST Memory Event / Error 0x03 POST Scalability Event / Error (not used x336) 0x04 POST Bus Event / Error 0x05 POST Chipset Event / Error Byte 12-15 Defined per Error / Event Type in below tables Byte 16 Revision Number Format
OEM POST No Time Stamp	0xE0	Byte 4 POST Error / Event Type 0x00 POST PCI POST Event/Error 0x01 POST PCI Processor Event 0x02 POST Memory Error 0x03 POST Scalability Event (not used x336) 0x04 POST Bus Event 0x05 POST Chipset Event Byte 6-15 Defined per Error/Event Type in below tables Byte 16 Revision Number Format
OEM SMI Handler with Time Stamp	0xC1	Byte 11 SMI Error / Event Type 0x00 SMI PCI Event / Error 0x01 SMI Processor Event / Error 0x02 SMI Memory Event / Error 0x03 SMI Scalability Event / Error (not used x336) 0x04 SMI Bus Event / Error 0x05 SMI Chipset Event / Error Byte 12-15 Defined per Error / Event Type in below tables Byte 16 Revision Number Format
OEM SMI	0xE1	Byte 4 SMI Error / Event Type

Handler No Time Stamp		0x00 SMI PCI Event / Error 0x01 SMI Processor Event / Error 0x02 SMI Memory Event / Error 0x03 SMI Scalability Event / Error (not used x336) 0x04 SMI Bus Event / Error 0x05 SMI Chipset Event / Error Byte 6-15 Defined per Error/Event Type in below tables Byte 16 Revision Number Format

Figure 1-POST OEM SEL Definitions

5.2 POST OEM SEL Formats

5.2.1 POST OEM SEL Formats with Time Stamp

Byte	Contents	Description	Repair Actions
11	0x00	POST PCI Event / Error	
	0x01	POST Processor Event / Error	
	0x02	POST Memory Event / Error	
12	0x00	POST Event/Error occurred. **Next non-timestamped OEM SEL entry will contain details of the specific event/error.**	← See Next
13:15		Reserved	
16	0x00	Revision Number	

Figure 2- POST OEM SEL Format

5.2.2 POST PCI Event / Error SEL Format

Byte	Description	Repair Actions
4	0x00 POST PCI Event / Error	
5	Error Type 0x00 Device OK 0x01 Required ROM space not available 0x02 Required IO space not available 0x03 Required memory not available 0x04 Required memory below 1MB not available 0x05 ROM checksum failed 0x06 BIST failed 0x07 Planar device missing or disabled by user 0x08 PCI device has an invalid PCI configuration space header	 See 1801 POST error See 1801 POST error See 1801 POST error See 1801 POST error Remove card, replace Remove card, replace Info

	0x09 Specific PCI Device added (details to follow) 0x0A Specific PCI Device removed (details to follow) 0x0B Device title for removed devices 0x0C Device title for added devices 0x0D Requested resources not available 0x0E Title for added devices 0x0F Vendor ID sub-message 0x10 Device ID sub-message 0x11 Previous slot sub-message 0x12 Slot sub-message 0x13 Planar video disabled due to add in video card 0x14 Partial disable value 0x15 Title for partial disable 0x16 33Mhz dev on 66Mhz bus 0x17 Details for 33mhz card on 66mhz bus 0x18-1F (not used x336)	Remove card, replace Info Info Info Info See 1801 POST error Info Info Info Info Info Info Info Info Info
6	Chassis Number (0xFF if not applicable)	info
7	Slot Number (0xFF if not applicable)	info
8	Bus Number (0xFF if not applicable)	info
9	Device ID (MSB) (0xFF if not applicable)	info
10	Device ID (LSB) (0xFF if not applicable)	info
11	Vendor ID (MSB) (0xFF if not applicable)	info
12	Vendor ID (LSB) (0xFF if not applicable)	info
13	Reserved	
14	Reserved	
15	Reserved	
16	Revision Number = 0x00	

Figure 3- POST PCI Event / Error SEL Format

5.2.3 POST Processor Event / Error SEL Format

Byte	Description	Repair Actions
4	0x01 POST Processor Event / Error	
5	Error Type 0x00 Processor Failed BIST 0x01 Unable to Apply Microcode (Patch) Update 0x02 POST Does Not Support Current Stepping of Processor 0x03 CPU Mismatch Detected	 Replace proc Update BIOS Update BIOS All procs must match
6	Chassis Number (0x00 if not applicable)	Info
7	Processor Number (0x00 if not applicable)	Info
8 – 15	Reserved	
16	Revision Number = 0x00	

Figure 4- POST Processor Event / Error SEL Format

5.2.4 Memory Event / Error SEL Format

Byte	Description	Repair Actions
4	0x02 Memory Event / Error	
5	0x00 (not used x336) 0x01 (not used x336)	Info
6	Chassis (0 if not applicable)	Info
7	Memory Card (1-4) (not used x336)	Info
8	Memory DIMM (1-4)	Info
9	Failing Symbol for Correctable Error	Info
10 -15	Reserved	
16	Revision Number = 0x00	

Figure 5- POST Memory Event / Error SEL Format

Byte	Description	Repair Actions
4	0x02 Memory Event / Error	
5	Event Type 0x02 DIMM Status	
6	0x00 DIMM Enabled 0x01 DIMM Disabled – Failed ECC Test 0x02 DIMM Disabled – Failed POST/BIOS Memory Test 0x03 DIMM Disabled – Non-supported memory device 0x04 DIMM Disabled – Non matching or missing DIMMs	1. Check DIMM P/N. 2. Reseat/replace DIMM in byte 7,8,9
7	Chassis (0 if not applicable)	
8	Memory Card 1-N (0 if not applicable)	
9	Memory DIMM 1-N (0 if not applicable)	
10 -15	Reserved	
16	Revision Number = 0x00	

Figure 6- POST Memory DIMM Event / Error SEL Format

Byte	Description	Repair Actions
4	0x02 Memory Event / Error	
5	Event Type 0x03 Memory Card Status	
6	0x00 Card Enabled 0x01 Card Disabled – Failed BIST	Reseat/replace MEM CARD in byte 7,8
7	Chassis (0 if not applicable)	
8	Memory Card 1-N (0 if not applicable)	
9 – 15	Reserved	
16	Revision Number = 0x00	

Figure 7- POST Memory Card Event / Error SEL Format

5.3 SMI OEM SEL Formats

5.3.1 SMI Event / Error SEL Format with Time Stamp

Byte	Description	Repair Actions
11	0x00 SMI PCI Event / Error - See next non-time stamped entry for details. 0x01 SMI Processor Event / Error - See next non-time stamped entry for details. 0x02 SMI Memory Event / Error - See next non-time stamped entry for details. 0x03 SMI Scalability Event / Error - **see bytes 12-14 below** 0x04 SMI Bus Event / Error - See next non-time stamped entry for details. 0x05 SMI Chipset Event / Error - See next non-time stamped entry for details.	← ← see SP Log ← ←
12	0x00 Scalability Link Down 0x01 Scalability Link Up 0x02 Scalability Link Double Wide Down 0x03 Scalability Link Double Wide Up 0x80 Scalability Link PFA 0x81 Scalability Link Invalid Port 0x82 Scalability Link Invalid Node	see SP Log
13	0x01 – 0x08 Chassis Number (One based)	Info
14	0x01 – 0x03 Scalability Port Number (One based) 0x00 – Scalability Double Wide Link	Info
15	Reserved	
16	Revision Number = 0x00	

Figure 8-SMI Scalability Event/Error SEL Format

5.3.2 SMI PCI Event / Error SEL Format

Byte	Description	Repair Actions
4	0x00 SMI PCI Event / Error	
5	Error Type 0x00 Unknown SERR/PERR Detected on PCI Bus (Bytes 6-15 are 0x00 if not applicable) 0x01-0x0F PCI Standard Error Messages for PCI Devices & Primary Interface of PCI-to-PCI Bridge 0x01 SERR: Address or Special Cycle DPE 0x02 PERR: Master Read Parity Error 0x03 SERR: Received Target Abort 0x04 PERR: Master Write Parity Error 0x05 SERR: Device Signaled SERR 0x06 PERR: Slave Signaled Parity Error	**ALL ERRORS:** 1. Identify PCI device from bytes 6-15 below. 2. Reseat/replace PCI device identified above. 3. Verify latest device driver for device identified above. 4. Replace PCIX

	0x07 SERR: Signaled Target Abort 0x08 PERR: Additional Correctable ECC Error 0x09 SERR: Received Master Abort 0x0A PERR: Additional Uncorrectable ECC Error 0x0B SERR: Split Completion Discarded 0x0C PERR: Correctable ECC Error 0x0D SERR: Unexpected Split Completion 0x0E PERR: Uncorrectable ECC Error 0x0F SERR: Received Split Completion Error Message 0x10 Reserved 0x11-0x1F Same as 0x01-0x0F for Secondary Interface of PCI-to-PCI Bridge 0x20-0x3F PCI Target Error Messages for PCI Host Bridge (Calgary) 0x20 PERR: PCI ECC Error (Corrected) 0x21 SERR: PCI Bus Address Parity Error 0x22 PERR: PCI Bus Data Parity Error 0x23 SERR: SERR# Asserted 0x24 PERR: PERR Received by Calgary on a PCIX Split Completion 0x25 SERR: Invalid Address 0x26 Reserved 0x27 SERR: TCE Extent Error 0x28 Reserved 0x29 SERR: Page Fault 0x2A Reserved 0x2B SERR: Unauthorized Access 0x2C Reserved 0x2D SERR: Parity Error in DMA Read Data Buffer 0x2E Reserved 0x2F SERR: PCI Bus Time Out 0x30 Reserved 0x31 SERR: DMA Delayed Read Timeout 0x32 Reserved 0x33 SERR: Internal Error on PCIX Split Completion 0x34 Reserved 0x35 SERR: DMA Read Reply (RIO) Timeout 0x36 Reserved 0x37 SERR: Internal RAM Error on DMA Write 0x38 Reserved 0x39 SERR: MVE Valid Bit Off 0x3A Reserved 0x3B SERR: MVE Index Invalid 0x3C Reserved 0x3D Reserved 0x3E Reserved 0x3F Reserved 0x40-0x5F PCI Master Error Messages for PCI Host Bridge (Calgary) 0x40 PERR: ECC Error (Corrected) **0x41 SERR: SERR# Detected** 0x42 PERR: PCI Bus Data Parity Error **0x43 SERR: No DEVSEL#**	adapter.

	0x44 Reserved **0x45 SERR: Bus Time Out** 0x46 Reserved **0x47 SERR: Retry Count Expired** 0x48 Reserved **0x49 SERR: Target-Abort** 0x4A Reserved **0x4B SERR: Invalid Size** 0x4C Reserved **0x4D SERR: Access Not Enabled** 0x4E Reserved **0x4F SERR: Internal RAM Error on MMIO Store** 0x50 Reserved 0x51 SERR: Split Response Received 0x52 Reserved 0x53 SERR: PCIX Split Completion Error Status Received 0x54 Reserved 0x55 SERR: Unexpected PCIX Split Completion Received 0x56 Reserved 0x57 SERR: PCIX Split Completion Timeout 0x58 Reserved 0x59 SERR: Recoverable Error Summary Bit 0x5A Reserved 0x5B SERR: CSR Error Summary Bit 0x5C Reserved 0x5D SERR: Internal RAM Error on MMIO Load 0x5E Reserved 0x5F Reserved 0x60-0x7F PCI Machine Check Messages for PCI Host Bridge (Calgary) 0x60 Reserved 0x61 SERR: Bad Command 0x62 Reserved 0x63 SERR: Length Field Invalid 0x64 Reserved 0x65 SERR: Load Greater Than 8 & No Write Buffer Enabled 0x66 Reserved 0x67 SERR: PCIX Discontiguous Byte Enable Error 0x68 Reserved 0x69 SERR: 4K Address Boundary Crossing Error 0x6A Reserved 0x6B SERR: Store Wrap State Machine Check 0x6C Reserved 0x6D SERR: Target State Machine Check 0x6E Reserved 0x6F SERR: Invalid Transaction PM/DW 0x70 Reserved 0x71 SERR: Invalid Transaction PM/DR 0x72 Reserved 0x73 SERR: Invalid Transaction PS/DW 0x74 Reserved	

	0x75 SERR: DMA Write Command FIFO Parity Error 0x76 Reserved 0x77 Reserved 0x78 Reserved 0x79 Reserved 0x7A Reserved 0x7B Reserved 0x7C Reserved 0x7D Reserved 0x7E Reserved 0x7F Reserved **0x80 PCI-to-PCI Bridge Discard Timer Error** **0x81-0xFF Reserved**	
6	Chassis Number (0x00 if not applicable)	
7	Slot Number	
8	Bus Number	
9	Device ID (LSB)	
10	Device ID (MSB)	
11	Vendor ID (LSB)	
12	Vendor ID (MSB)	
13	Status Register (LSB)	
14	Status Register (MSB)	
15	DevFun Number	
16	Revision Number = 0x00	

Figure 9- SMI PCI Event / Error SEL Format

5.3.3 SMI Processor Event / Error SEL Format

Byte	Description	Repair Actions
4	0x01 SMI Processor Event / Error	1. Contact level 3 support for detailed analysis if possible (these errors are rare) 2. See SMI MCA Data D below.
5	0x00 Data A	
6	Reserved	
7	Reserved	
8 - 9	Bank	
10 – 11	APIC ID	
12 – 15	CK4	
16	Revision Number = 0x00	

Figure 10-SMI MCA Data A SEL Format

Byte	Description	Repair Actions

4	0x01 SMI Processor Event / Error	1. Contact level 3 support for detailed analysis if possible (these errors are rare) 2. See SMI MCA Data D below.
5	0x01 Data B1	
6	Reserved	
7	Reserved	
8 – 11	Address high	
12-15	Address low	
16	Revision Number = 0x00	

Figure 11-SMI MCA Data B1 SEL Format

Byte	Description	Repair Actions
4	0x01 SMI Processor Event / Error	1. Contact level 3 support for detailed analysis if possible (these errors are rare) 2. See SMI MCA Data D below.
5	0x02 Data B2	
6	Reserved	
7	Reserved	
8 – 11	Timestamp high	
12 - 15	Timestamp low	
16	Revision Number = 0x00	

Figure 12-SMI MCA Data B2 SEL Format

Byte	Description	Repair Actions
4	0x01 SMI Processor Event / Error	1. Contact level 3 support for detailed analysis if possible (these errors are rare) 2. See SMI MCA Data D below.
5	0x03 Detail C	
6	Reserved	
7	Reserved	
8 – 11	MCA Status Register high	
12 - 15	MCA Status Register low	
16	Revision Number = 0x00	

Figure 13-SMI MCA Data C SEL Format

Byte	Description	Repair Actions
4	0x01 SMI Processor Event / Error	1. Contact level 3 support for detailed analysis if possible (these errors are rare)
5	0x04 Detail D	
6	Chassis Number (00 if not applicable)	
7	Error type 0x00 Recoverable 0x01 Unrecoverable	2. If Unrecoverable, replace CPU from byte 8.
8	Processor ID	
9 – 15	Reserved	
16	Revision Number = 0x00	

Figure 14-SMI MCA Data D SEL Format

5.3.4 SMI Memory Event / Error SEL Format

Byte	Description	Repair Actions
4	0x02 SMI Memory Event / Error	Info only
5	0x00 Sparing/RBS Event	
6	0x00 Sparing/RBS Start 1 0x02 Sparing/RBS Done 1	
7	Failed Row	
8	Spare Row	
9 – 15	Reserved	
16	Revision Number = 0x00	

Figure 15-SMI Sparing/RBS 1 SEL Format

Byte	Description	Repair Actions
4	0x02 SMI Memory Event / Error	Info only
5	0x00 Sparing Event	
6	0x01 Sparing Start 2 0x03 Sparing Done 2	
7	Failed Row 1	
8	Failed Row 2	
9	Spare Row 1	
10	Spare Row 2	
11- 15	Reserved	
16	Revision Number = 0x00	

Figure 16-SMI Sparing/RBS 2 SEL Format

Byte	Description	Repair Actions
4	0x02 SMI Memory Event / Error	
5	0x01 Memory Mirroring Failover Occurred (Running from mirrored memory image)	Replace memory DIMM identified by Lightpath LEDs
6-15	Reserved	
16	Revision Number = 0x00	

Figure 17-SMI Mirroring SEL Format

5.3.5 SMI FSB Bus Event / Error SEL Format

Byte	Description	Repair Actions
4	0x04 SMI Bus Event / Error	
5	Bus Type 0x00 FSB	
6	0x00 FSB A Fatal 0x01 FSB A NonFatal 0x02 FSB B Fatal 0x03 FSB B NonFatal	1. If fatal, for FSB A, test CPU1&2. Replace failed device. 2. If fatal, for FSB B, test CPU3&4. Replace failed device. 3. Replace CPU card.
7 – 8	FSB FERR or NERR or Zero	
9 – 15	Reserved	
16	Revision Number = 0x00	

Figure 18-SMI Front Side Bus Event SEL Format

Author Notes:

Sect 1 – from Warren Price, except 1.6 (differences between…) which comes from the BMC_x336_Spec.doc (Chuck Young/Carl Morrell)
Sect 2 – from BMC Core Spec (these are common to all BMC platforms)
Sect 3 – from BMC_x336_Spec.doc (Chuck Young/Carl Morrell) should use latest version.
Sect 4 – from BMC_x336_Spec.doc (Chuck Young/Carl Morrell) should use latest version.
> Cross reference sect 4 to 3. If entry from 4 is in 3, then 3 action is to see 4.
Sect 5 – from BMC_x336_Spec.doc (Chuck Young/Carl Morrell) should use latest version.
Sect 6 – from bios_bmc_design_guide.doc (Bill Schwartz) should use latest version.
All repair actions (Chap 2, 3,4, 5) columns are from the author.

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