

# DR-06T / DR-M06R

## Service Manual

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**ALINCO, INC.**

# SPECIFICATIONS

## ■ General

	DR-06T	DR-M06R
Frequency coverage	50.000 ~ 53.995MHz ( RX, TX )	
Operating mode	FM 16K0F3E ( Wide mode ) FM 8K50F3E ( Narrow mode )	FM 16K0F3E ( Wide mode )
Frequency resolution	5 , 8.33 , 10 , 12.5 , 15 , 20 , 25 , 30 , 50 kHz	
Number of memory Channels	100	
Antenna impedance	50ohm unbalanced	
Power requirement	13.8V DC +/- 15% ( 11.7 ~ 15.8 V )	
Ground method	Negative ground	
Current drain	Receive	0.6 A ( max. )    0.4 A ( Squelched )
	Transmit	Approx. 11.0 A max.
Operating temperature	-10 °C ~ 60°C	
Frequency stability	+/- 7ppm	
Dimensions	142 ( w ) x 40 ( h ) x 174 ( d ) mm ( 142 x 40 x 188 mm for projection included )	
Weight	Approx. 1.0 Kg	

## ■ Transmitter

Output power	Hi	50 W
	Mid	20 W
	Low	Approx. 5W
Modulation system	Variable reactance frequency modulation	
Maximum deviation	Frequency	+ / - 5kHz ( Wide mode ) + / - 2.5kHz ( Narrow mode )
Spurious emission	- 50 dB	
Adjacent channel power	- 60 dB	
Noise and hum ratio	- 40 dB ( Wide mode ) - 34 dB ( Narrow mode )	- 40 dB ( Wide mode )
Microphone impedance	2kohm	

## ■ Receiver

Sensitivity	- 12 dBu for 12 dB SINAD	
Receiver circuit	Double conversion super-heterodyne	
Intermediate frequency	1st 10.7 MHz    2nd 450kHz	
Squelch sensitivity	- 16 dBu	
Adjacent channel selectivity	- 65 dB ( Wide mode ) - 50 dB ( Narrow mode )	- 65 dB ( Wide mode )
Inter-modulation rejection ratio	60 dB	
Spurious and image rejection ratio	70 dB	
Audio output power	2.0 W ( 8ohm , 10 % THD )	

! NOTE : All specifications are subject to change without notice or obligation.

# CIRCUIT DESCRIPTION

## 1) Receiver System

The receiver system is a double superheterodyne system with a 10.7 MHz first IF and a 450 kHz second IF.

### 1. Front End

The received signal at any frequency in the 50.000MHz to 53.995MHz range is passed through the low-pass filter (L115, L114, L113, C204, C203, C202, C216 and C215) and tuning circuit (L105 and D105), and amplified by the RF amplifier (Q107). The signal from Q107 is then passed through the tuning circuit (L104, L103, L102, and varicaps D104, D103 and D102) and converted into 10.7 MHz by the mixer (Q106). The tuning circuit, which consists of L105, L104, varicaps D105 and D104, L103, L102, varicaps D103 and D102 is controlled by the tracking voltage from the VCO. The local signal from the VCO is passed through the buffer (Q125), and supplied to the source of the mixer (Q106). The radio uses the lower side of the superheterodyne system.

### 2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (XF101A, XF101B) selects 10.7 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q105) then amplifies the signal of the selected frequency.

### 3. Demodulation Circuit

After the signal is amplified by the first IF amplifier (Q105), it is input to pin 16 of the demodulator IC (IC108). The second local signal of 11.15 MHz, which is oscillated by the internal oscillation circuit in IC108 and crystal (X601), is input through pin 1 of IC108. Then, these two signals are mixed by the internal mixer in IC108 and the result is converted into the second IF signal with a frequency of 450 kHz. The second IF signal is output from pin 3 of IC108 to the ceramic filter (FL101 or FL102), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC108 through pins 5.

The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC108, and output as an audio signal through pin 9.

### 4. Audio Circuit

The audio signal from pin 9 of IC108 is amplified by the audio amplifier (IC120:A), and switched by the signal switch IC (IC111) and then input it to the de-emphasis circuit.

and is compensated to the audio frequency characteristics in the de-emphasis circuit (R203, R207, R213, R209, C191, C218, C217) and amplified by the AF amplifier (IC120:B). The signal is then input to volume (VR1). The adjusted signal is sent to the audio power amplifier (IC117) through pin 1 to drive the speaker.

## 5. Squelch Circuit

The detected output which is outputted from the pin 9 of IC108 is inputted to pin 8 of IC108 after it was been amplified by IC120:A and it is outputted from pin 14 after the noise component was been eliminated from the composed band pass filter in the built in amplifier of the IC. The adjusted voltage level at VR101 is delivered to the comparator of the CPU.

The voltage is led to pin 2 of CPU and compared with the setting voltage. The squelch will open if the input voltage is lower than the setting voltage. During open squelch, pin 30 (SQC) of the CPU becomes "L" level, AF control signal is being controlled and sounds is outputted from the speaker.)

## 6. WIDE / NARROW Switching Circuit

The 2nd IF 450 kHz signal which passes through filter FL101 (wide) and FL102 (narrow) during narrow, changes its width using the width control switching D115 and D116.

## 2) Transmitter System

### 1. Modulator Circuit

The audio signal is converted to an electrical signal by the microphone, and input it to the microphone amplifier (Q6). Amplified signal which passes through mic-mute control IC109 is adjusted to an appropriate mic-volume by means of mic-gain adjust VR106.

IC114:C and D consists of four operational amplifiers; one amplifier (pins 12, 13, and 14) is composed of pre-emphasis and IDC circuits and the other (pins 8, 9, and 10) is composed of a splatter filter. The maximum frequency deviation is obtained by VR107. and input to the signal switch (IC113) (9600 bps packet signal input switch) and input to the cathode of the varicap of the VCO, to change the electric capacity in the oscillation circuit. This produces the frequency modulation.

### 2. Power Amplifier Circuit

The transmitted signal is oscillated by the VCO, amplified by the drive amplifier (Q145) and younger amplifier (Q115, Q701), and input to the final power amplifier (Q702). The signal is then amplified by the final power amplifier (Q702) and led to the antenna switch (D110) and low-pass filter (L113, L114, L115, C215, C216, C202, C203 and C204), where unwanted high harmonic waves are reduced as needed, and the resulting signal is supplied to the antenna.

### 3. APC Circuit

Part of the transmission power from the low-pass filter is detected by D111, converted to DC. The detection voltage is passed through the APC circuit (IC114:B), then it controls the APC voltage supplied to the younger amplifier Q701 and the final power amplifier Q702 to fix the transmission power.

## 3) PLL Synthesizer Circuit

### 1. PLL

The dividing ratio is obtained by sending data from the CPU (IC1) to pin 10 and sending clock pulses to pin 9 of the PLL IC (IC116). The oscillated signal from the VCO is amplified by the buffer (Q134 and Q135) and input to pin 8 of IC116. Each programmable divider in IC116 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

## 2. Reference Frequency Circuit

The reference frequency appropriate for the channel steps is obtained by dividing the 11.15 MHz reference oscillation (X601) by 4250 or 3400, according to the data from the CPU (IC1). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, 25, 30, and 50 kHz are used. When it is 6.25 kHz, the 12.5 kHz channel step is used.

## 3. Phase Comparator Circuit

The PLL (IC116) uses the reference frequency, 5 or 6.25kHz. The phase comparator in the IC116 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25kHz, which is obtained by the internal divider in IC116.

## 4. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 5) of IC116 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

## 5. VCO Circuit

A Colpitts oscillation circuit driven by Q131 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC1) and PLL circuit is input to the varicaps (D123). This change the oscillation frequency, which is amplified by the VCO buffer (Q134) and output from the VCO area.

# 4) CPU and Peripheral Circuits

## 1. LCD Display Circuit

The CPU turns ON the LCD via segment and common terminals with 1/4 the duty and 1/3 the bias, at the frame frequency is 64Hz.

## 2. Dimmer Circuit

The dimmer circuit makes the output of pin 13 of CPU (IC1) into "H" level at set mode, so that Q9 and Q3 will turn ON to make the lamp control resistor R84 short and make its illumination bright. But on the other hand, if the dimmer circuit makes pin 13 into "L" level, Q9 and Q3 will turn OFF, R84's illumination will become dimmer as its hang on voltage falls down in the working LED (D11, D2, D5, D3 and D6).

## 3. Reset and Backup

When the power from the DC cable increases from Circuits 0 V to 2.5 or more, "H" level reset signal is output from the reset IC (IC4) to pin 33 of the CPU (IC1), causing the CPU to reset. The reset signal, however, waits at 100, and does not enter the CPU until the CPU clock (X1) has stabilized.

## 4. S (Signal) Meter Circuit

The DC potential of pin 12 of IC108 is input to pin 1 of the CPU (IC1), converted from an analog to a digital signal, and displayed as the S-meter signal on the LCD.

## 5. DTMF Encoder

The CPU (IC1) is equipped with an internal DTMF encoder. The DTMF signal is output from pin 10, through R35, R34 and R261 (for level adjustment), and then through the microphone amplifier (IC114:D), and is sent to the varicap of the VCO for modulation. At the same time, the monitoring tone passes through the AF circuit and is output from the speaker.

## 6. Tone Encoder

The CPU (IC1) is equipped with an internal tone encoder. The tone signal (67.0 to 250.3 Hz) is output from pin 9 of the CPU to the varicap (D120) of the VCO for modulation.

## 7. DCS Encoder

The CPU (IC1) is equipped with an internal DCS code encoder. The code (023 to 754) is output from pin 9 of the CPU to the PLL reference oscillator. When DCS is ON, DCS MUTE circuit (Q126-ON, Q133-ON, Q132-OFF) works. The modulation activates in D601 side only.

## 8. CTCSS, DCS Decoder

The voice band of the AF output signal from pin 1 of IC120:A is cut by sharp active filter IC104:A and D (VCVS) and amplified, then led to pin 4 of CPU. The input signal is compared with the programmed tone frequency code in the CPU. The squelch will open when they match. During DCS, Q108 is ON, C419 is working and cut off frequency is lowered.

## 5) Power Supply Circuit

When power supply is ON, there is a "L" signal being inputted to pin 39 (PSW) of CPU which enables the CPU to work. Then, "H" signal is outputted from the pin 41 (C5C) of CPU and drives ON the power supply switch control Q8 and Q7 which turns the 5VS ON. 5VS turns ON the PLL IC116, main power supply switch Q127 and Q122, AF POWER IC117 and the 8 V of AVR (IC115). During reception, pin 29 (R5) of CPU outputs "H" level, Q124 is ON, and the reception circuits supplied by 8 V. While during transmission, pin 28 (T5) of CPU outputs "L" level which is reverse by Q11 so that the output in Q128 will be "H" level, Q123 is ON, and the transmission circuit is supplied by 8 V. Or, in the case when the condition of PLL is UNLOCK, "L" level is outputted from pin 7 of IC116, UNLOCK switch Q11 is ON, Q129 is ON, transmission switch Q128 is OFF which makes the transmission to stop.

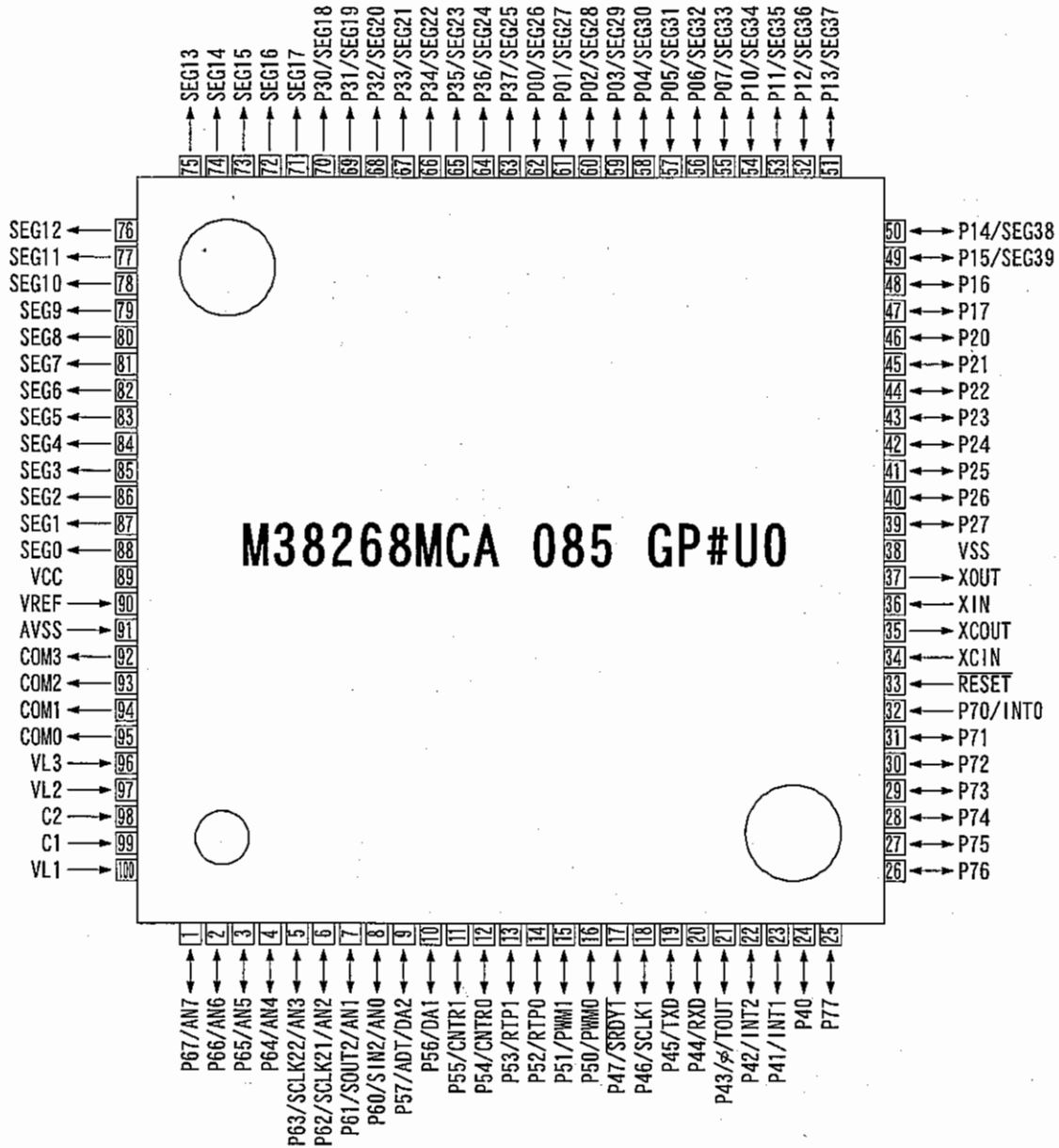
### 1. ACC External Power Supply Terminal

When optional power supply cord EDC-37 etc. is connected to the external power supply terminal JK101, with ACC power supply ON, switch Q101 will turn ON, 5 V of AVR IC101 pin 2 (STB) becomes "L" which makes C5V to turn ON. With this, it can turn the power supply of the radio ON.

# 6) M38268MCA085GP#U0 (XA1170B)

CPU

Terminal Connection  
(TOP VIEW)



No.	Terminal	Signal	I/O	Description
1	P67/AN7	SMT	I	S-meter input
2	P66/AN6	SQL	I	Noise level input for squelch
3	P65/AN5	BAT	I	Battery voltage input
4	P64/AN4	TIN	I	CTCSS tone input / DCS code input
5	P63/SCLK22/AN3	BP1	I	Band plan 1
6	P62/SCLK21/AN2	BP2	I	Band plan 2
7	P61/SOUT2/AN1	DCSW	O	DCS signal mute
8	P60/SIN2/AN0	RE2	I	Rotary encoder input
9	P57/ADT/DA2	TOUT	O	CTCSS tone output / DCS tone output
10	P56/DA1	DOUT	O	DTMF output
11	P55/CNTR1	SCL	O	Serial clock for EEPROM
12	P54/CNTR0	TBST	O	Tone burst output
13	P53/RTP1	BP4	I/O	Band plan 4 / lamp dimmer HI / LOW switch
14	P52/RTP0	MUTE	I/O	Microphone mute / Security alarm SW
15	P51/PWM1	CLK	O	Serial clock output for PLL, scramble
16	P50/PWM0	DATA	I/O	Serial data output for PLL scramble / PLL unlock signal input
17	P47/SRDY1	TSTB	I/O	Trunking board detection / Strobe signal to trunking board
18	P46/SCLK1	STB	O	Strobe for PLL IC
19	P45/TXD	UTX	O	UART data transmission output
20	P44/RXD	RTX	I	UART data reception output
21	P43/□/TOUT	BEEP	I/O	Beep tone / Band plan 3
22	P42/INT2	SEC	I	Security voltage input
23	P41/INT1	RE1	I	Rotary encoder input
24	P40	DSQ	I	Digital squelch input
25	P77	PTT	I	PTT input
26	P76	SSTB	O	Strobe signal to scramble IC / Security mode
27	P75	W/N	O	Wide Narrow SW
28	P74	T5	O	TX power ON / OFF output
29	P73	R5	O	RX power ON / OFF output
30	P72	SQC	O	SQL ON / OFF
31	P71	C/S	O	Digital scramble ON / OFF
32	P70/INT0	BU	I	Backup signal detection input
33	RESET	RESET	I	Reset input
34	XCIN	Xcin	-	-
35	XCOU	Xcout	-	-
36	XIN	Xin	-	Main clock input
37	XOUT	Xout	-	Main clock output
38	VSS	GND	-	CPU GND
39	P27	PSW	I	Power switch input
40	P26	SDA	O	Serial data for EEPROM
41	P25	C5C	O	C5V power ON / OFF output
42	P24	AIR	O	Air band SW / Tx middle power
43	P23	LOW	O	Tx low power
44	P22	EXP	O	Trunking / Packet data SW
45	P21	SW6	I	Key sw 6 (SQL)
46	P20	SW5	I	Key sw 5 (CALL)
47	P17	SW4	I	Key sw 4 (TSQ)
48	P16	SW3	I	Key sw 3 (MHz)
49	P15/SEG39	SW2	I	Key sw 2 (V/M)
50	P14/SEG38	SW1	I	Key sw 1 (FUNC)

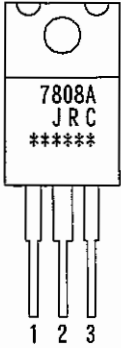


No.	Terminal	Signal	I/O	Description	
51	P13/SEG37	DOWN	I	Mic down input	
52	P12/SEG36	DUD	I	Digital unit detect	
53	P11/SEG35	SCR	I	Scramble IC ready signal / PTT input for 9600bps	
54	P10/SEG34	UP	I	Mic up input	
55	P07/SEG33	S33	O	LCD segment signal	
56	P06/SEG32	S32	O		
57	P05/SEG31	S31	O		
58	P04/SEG30	S30	O		
59	P03/SEG29	S29	O		
60	P02/SEG28	S28	O		
61	P01/SEG27	S27	O		
62	P00/SEG26	S26	O		
63	P37/SEG25	S25	O		
64	P36/SEG24	S24	O		
65	P35/SEG23	S23	O		
66	P34/SEG22	S22	O		
67	P33/SEG21	S21	O		
68	P32/SEG20	S20	O		
69	P31/SEG19	S19	O		
70	P30/SEG18	S18	O		
71	SEG17	S17	O		
72	SEG16	S16	O		
73	SEG15	S15	O		
74	SEG14	S14	O		
75	SEG13	S13	O		
76	SEG12	S12	O		
77	SEG11	S11	O		
78	SEG10	S10	O		
79	SEG9	S9	O		
80	SEG8	S8	O		
81	SEG7	S7	O		
82	SEG6	S6	O		
83	SEG5	S5	O		
84	SEG4	S4	O		
85	SEG3	S3	O		
86	SEG2	S2	O		
87	SEG1	S1	O		
88	SEG0	S0	O		
89	VCC	VDD	-		CPU power terminal
90	VREF	Vref	-		AD converter power supply
91	AVSS	Avss	-		AD converter GND
92	COM3	COM3	O	LCD COM3 output	
93	COM2	COM2	O	LCD COM2 output	
94	COM1	COM1	O	LCD COM1 output	
95	COM0	COM0	O	LCD COM0 output	
96	VL3	VL3	-	LCD power supply	
97	VL2	VL2	-	LCD power supply	
98	C2	I	-	-	
99	C1	C1	-	-	
100	VL1	VL1	I	LCD power supply	

# SEMICONDUCTOR DATA

## 1) NJM7808FA (XA0102)

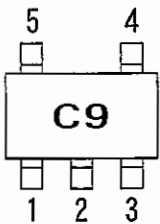
8V (1A) Voltage Regulator



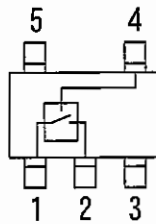
- 1. INPUT
- 2. COMMON
- 3. OUTPUT

## 2) TC4S66F (XA0115)

Bilateral Switch



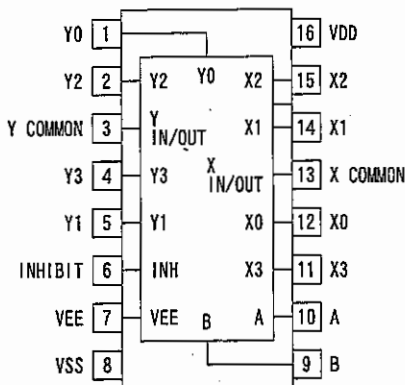
- 1. IN / OUT
- 2. OUT / IN
- 3. VSS
- 4. CONT
- 5. VDD



CONT	Function (IN-OUT)
L	Disconnect (Hi Z)
H	Connect (290ohm typ.)

## 3) BU4052BF (XA0236)

Analog Multiplexer / De-multiplexer

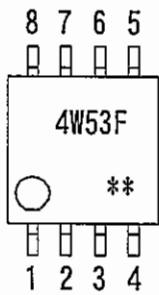


INHIBIT	A	B	COMMON	ON SWITCH
L	L	L	X Y	X0 Y0
L	H	L		X1 Y1
L	L	H		X2 Y2
L	H	H		X3 Y3
H	*	*		NONE

\* Don't care

#### 4) TC4W53FU (XA0348)

Multiplexer / De-multiplexer



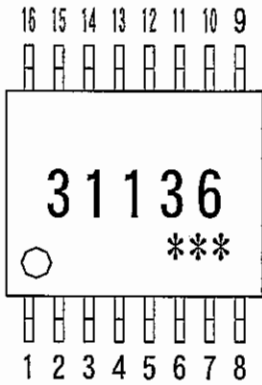
1. COMMON
2. INH
3. VEE
4. VSS
5. A
6. ch 1
7. ch 0
8. VDD

Controll input		ON channel
INH	A	
L	L	ch 0
L	H	ch 1
H	*	NONE

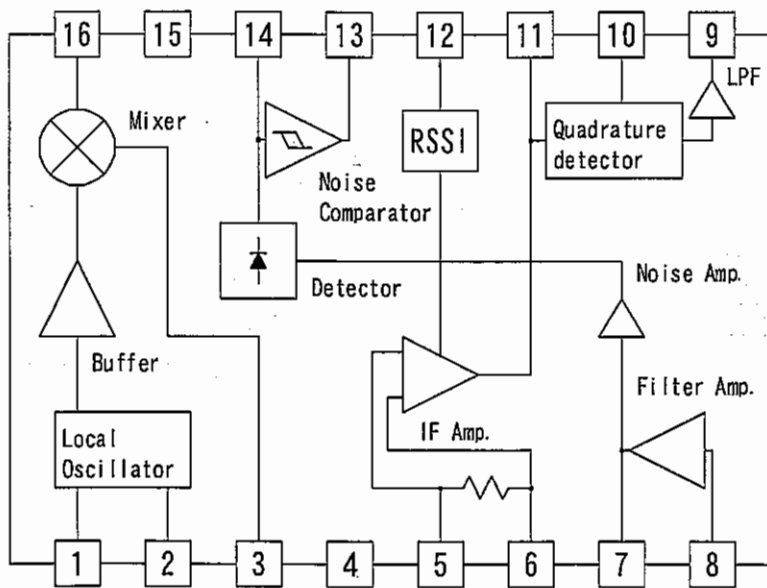
\* Don't care

#### 5) TA31136FN (XA0404)

Narrow Band FM IF IC

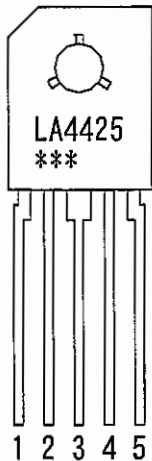


- |  |  |
|--|--|
| <ol style="list-style-type: none"> <li>1. OSC IN</li> <li>2. OSC OUT</li> <li>3. MIX OUT</li> <li>4. Vcc</li> <li>5. IF IN</li> <li>6. DEC</li> <li>7. FIL OUT</li> <li>8. FIL IN</li> </ol> | <ol style="list-style-type: none"> <li>9. AF OUT</li> <li>10. QUAD</li> <li>11. IF OUT</li> <li>12. RSSI</li> <li>13. N-DET</li> <li>14. N-REC</li> <li>15. GND</li> <li>16. MIX IN</li> </ol> |
|--|--|



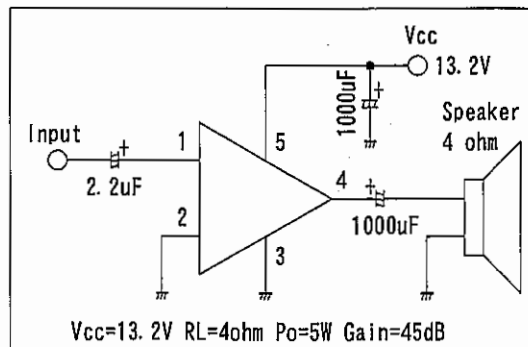
## 6) LA4425A (XA0410)

5W Audio Power Amplifier



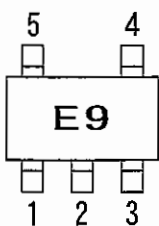
1. Input
2. Small signal GND
3. Large signal GND
4. Output
5. Vcc

Test Circuit

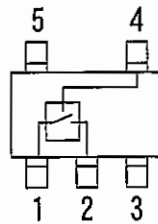


## 7) TC7S66FU (XA0524)

Bilateral Switch



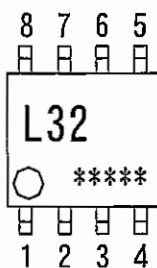
1. IN / OUT
2. OUT / IN
3. VSS
4. CONT
5. VDD



CONTROL	Switch Function
H	ON
L	OFF

## 8) BR24L32FJ (XA0604Z)

32K-Bit EEPROM

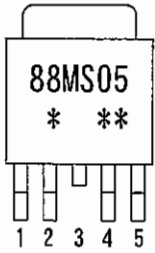


1. A0
2. A1
3. A2
4. Vss
5. SDA
6. SCL
7. WP
8. Vcc

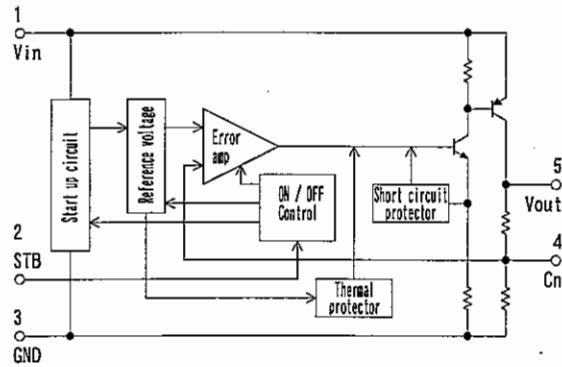
Name	Function
A0...A2	User Configurable Chip Select
Vss	Ground
SDA	Serial Address / Data / I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5 ~ 6.0V Power Supply

## 9) L88MS05TLL (XA0675)

5V (500mA) Voltage Regulator with On/Off Function



1. Vin
2. STB
3. GND
4. Cn
5. Vout

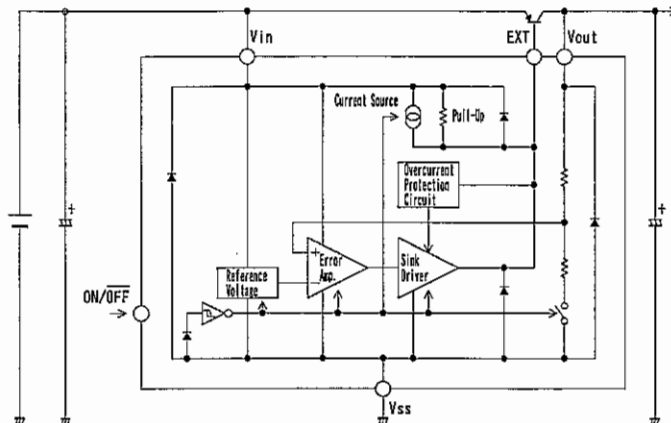


## 10) S-816A50AMC (XA0925)

External Transistor Type 5V Voltage Regulator with On/Off Function

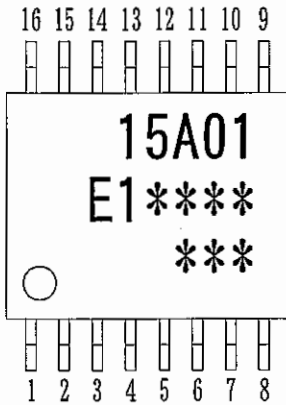


1. EXT
2. Vss
3. ON/OFF
4. Vin
5. Vout

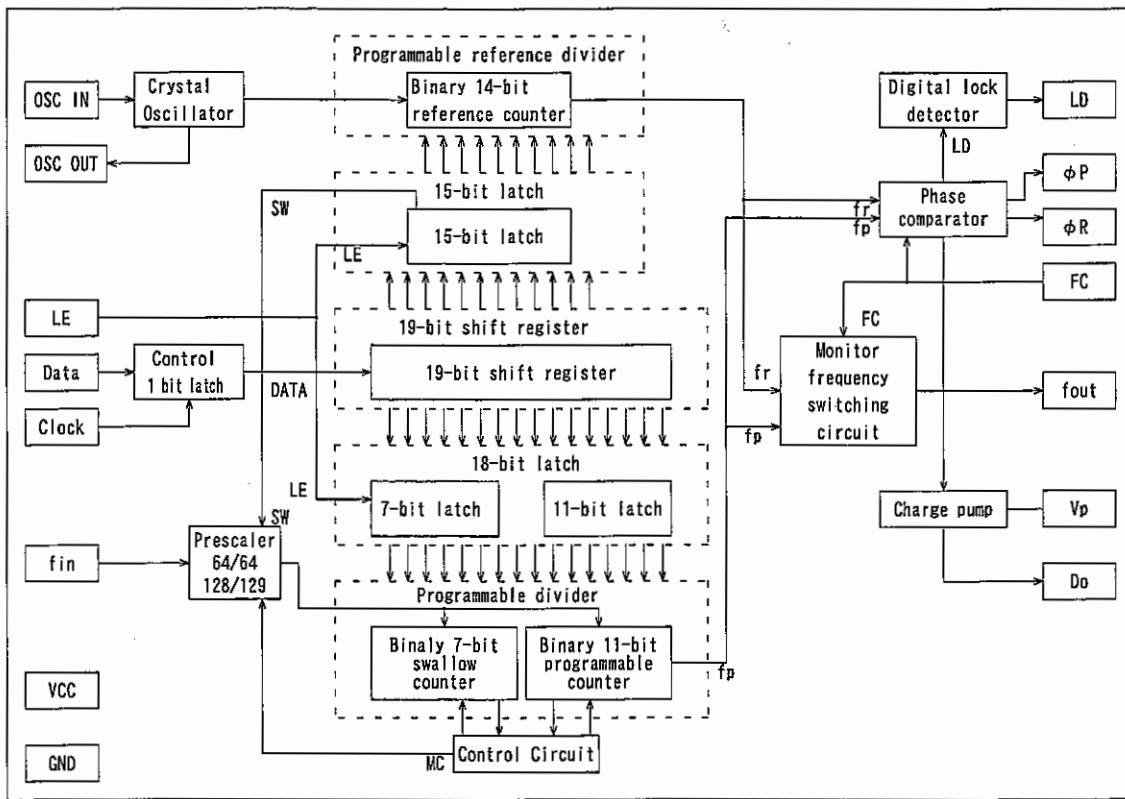


# 11) MB15A01PFV1 (XA1010)

## PLL Synthesizer



- |            |              |
|------------|--------------|
| 1. OSC IN  | 9. Clock     |
| 2. OSC OUT | 10. Data     |
| 3. Vp      | 11. LE       |
| 4. Vcc     | 12. FC       |
| 5. Do      | 13. N. C.    |
| 6. GND     | 14. fout     |
| 7. LD      | 15. $\phi P$ |
| 8. fin     | 16. $\phi R$ |

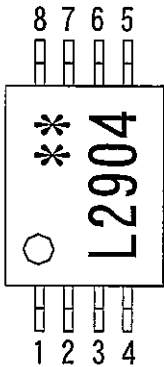


(  $V_{cc} = 2.7$  to  $3.5V$ ,  $T_a = -40^{\circ}C$  to  $+85^{\circ}C$  )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	$V_{cc}$	-	2.7	3.0	3.5	V
Power supply current	$I_{cc}$	2500MHz $V_{cc}=V_p=3.75V$		6.5		mA
LPF supply voltage	$V_p$	-	$V_{cc}$	-	6.0	V
Local oscillator input level	$V_{fin}$	-	-10		+6	dBm
Local oscillator input frequency	$f_{in}$	-	10		1100	MHz
Xin input level	$V_{xin}$	-	0.5		-	Vp-p
Xin input frequency	$F_{xin}$	-	-	12	23	MHz

## 12) LM2904PWR (XA1103)

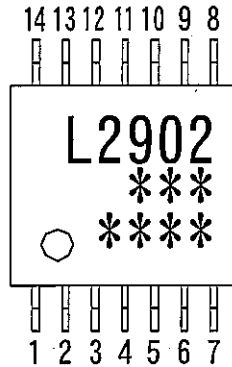
Dual Operational Amplifiers



1. Output A
2. Inverting Input A
3. Non-inverting Input A
4. GND
5. Non-inverting Input B
6. Inverting Input B
7. Output B
8. Vcc

## 13) LM2902PWR (XA1106)

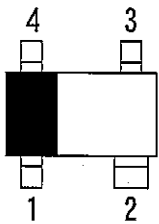
Quad Operational Amplifiers



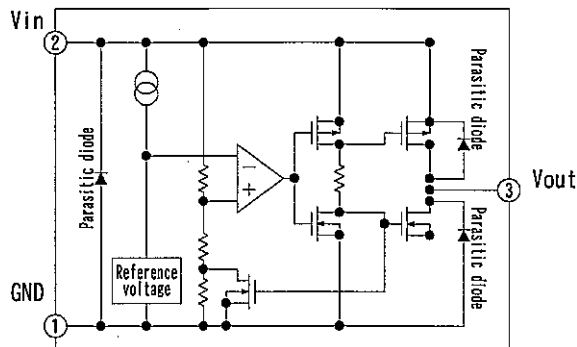
1. Output A
2. Inverting Input A
3. Non-inverting Input A
4. Vcc
5. Non-inverting Input B
6. Inverting Input B
7. Output B
8. Output C
9. Inverting Input C
10. Non-inverting Input C
11. GND
12. Non-inverting Input D
13. Inverting Input D
14. Output D

## 14) S-80845CLNB (XA1120)

4.5V Voltage Detector

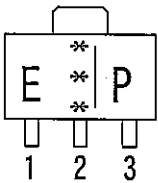


1. Vout
2. Vin
3. NC
4. GND

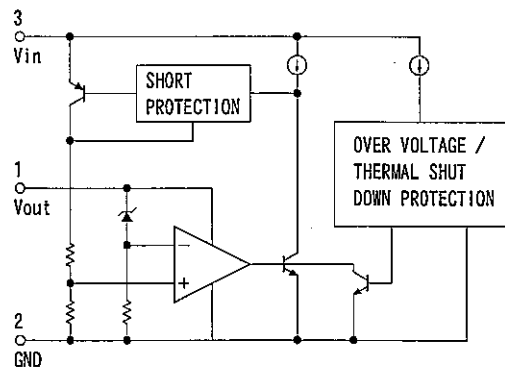


## 15) TA78DS10F (XA1249)

10V (30mA) Voltage Regulator
































































1. OUTPUT
2. COMMON
3. INPUT



# 16) Transistor, Diode and LED Outline Drawing

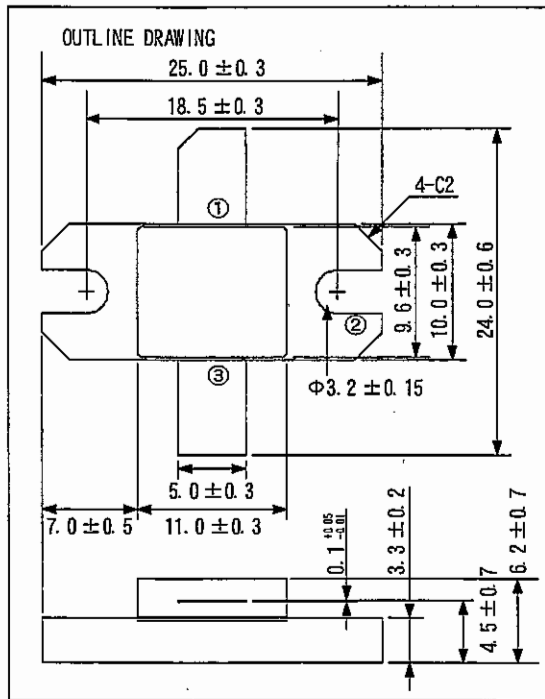
Top View

MI 407 XD0013	DA204U XD0130	1SV231 XD0260	1SV268 XD0301	DAN235E XD0320	RLS-73 XD0363	CRG01 XD0391
 	 	 	 	 	 	 
VDZ5. 1B XD0402	S3V60 XD0414	1SS383 XD0426	JDV2S14 XD0427	1SS383 XD0461	1SS406 XD0462	2SK880GR XE0021
 	 	 	 	 	 	 
3SK293 XE0053	2SK2539 XE0066	FA1111C XL0069	FA1111C XL0077	2SC3356T1 XT0030	2SA1576A XT0094	2SA1036K XT0110
 	 	 	 	 	 	 
2SC4915 XT0178	2SB1386 XT0190	2SC5551 XT0194	2SC6026MFV XT0210	2SA2070 XT0223	2SC4738 XT0224	RN1104 XU0195
 	 	 	 	 	 	 
EMD6 XU0209	RN1107MFV XU0210	RN2107MFV XU0211	RN1711 XU0226	RN2109MFV XU0231		
 Rb=4.7kohm Rbe=none	 Rb=10kohm Rbe=47kohm	 Rb=10kohm Rbe=47kohm	 Rb=10kohm Rbe=none	 Rb=47kohm Rbe=22kohm		



# 17) RD70HVF1 (XE0047)

Nch MOS FET



- PIN  
 ① DRAIN  
 ② SOURCE  
 ③ GATE

## ABSOLUTE MAXIMUM RATING ( Tc = 25 °C, unless otherwise noted )

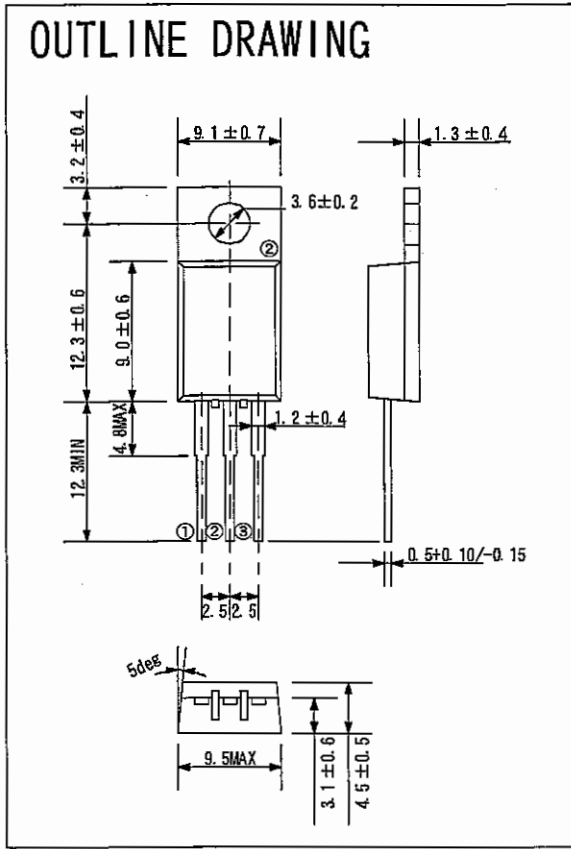
Symbol	Parameter	Test Conditions	Ratings	Unit
Pch	Channel dissipation	Tc = 25 °C	150	W
VDSS	Drain to source voltage	Vgs = 0V	30	V
VGSS	Gate to source voltage	Vds = 0V	+/- 20	V
Tj	Channel temperature	-	175	°C
Tstg	Storage temperature	-	-40 to +125	°C

## ELECTRICAL CHARACTERISTICS ( Tc = 25 °C, unless otherwise noted )

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
Idss	Saturated drain current	Vds = 17V, Vgs = 0V	-	300	μA
Igss	Gate to source leak current	Vgs = 10V, Vds = 0V	-	5	μA
VTH	Threshold voltage	Vds = 12V, Ids = 1mA	1.3	2.3	V
Pout1	Output Power 1	f = 175MHz, Pin = 6W, Vds = 12.5V	70	-	W
ηD1	Drain Efficiency 1	Ids (idle) = 2.0A (Vgs Control)	55	-	%
Pout2	Output Power 2	f = 520MHz, Pin = 10W, Vds = 12.5V	50	-	W
ηD2	Drain Efficiency 2	Ids (idle) = 2.0A (Vgs Control)	50	-	%
VSWRT1	Load VSWR Tolerance	f = 175MHz, Vds = 15.2V Ids (idle) = 2.0A (Vgs Control) Po = 70W (Pin Control) ρl ≤ 20:1 (ALL Phase)	No degradation		-
VSWRT2	Load VSWR Tolerance	f = 520MHz, Vds = 15.2V Ids (idle) = 2.0A (Vgs Control) Po = 50W (Pin Control) ρl ≤ 20:1 (ALL Phase)	No degradation		-

# 18) RD06HHF1 (XE0054)

Nch MOS FET



- PIN  
 ① GATE  
 ② SOURCE  
 ③ DRAIN

## ABSOLUTE MAXIMUM RATING ( Tc = 25 °C, unless otherwise noted )

Symbol	Parameter	Test Conditions	Ratings	Unit
Pch	Channel dissipation	Tc = 25 °C	31.3	W
VDSS	Drain to source voltage	Vgs = 0V	50	V
VGSS	Gate to source voltage	Vds = 0V	+/- 20	V
ID	Drain to source Current	-	3	A
Tj	Channel temperature	-	150	°C
Tstg	Storage temperature	-	-40 to +150	°C
Rth j-c	Thermal resistance	Junction to case	4.0	°C/W

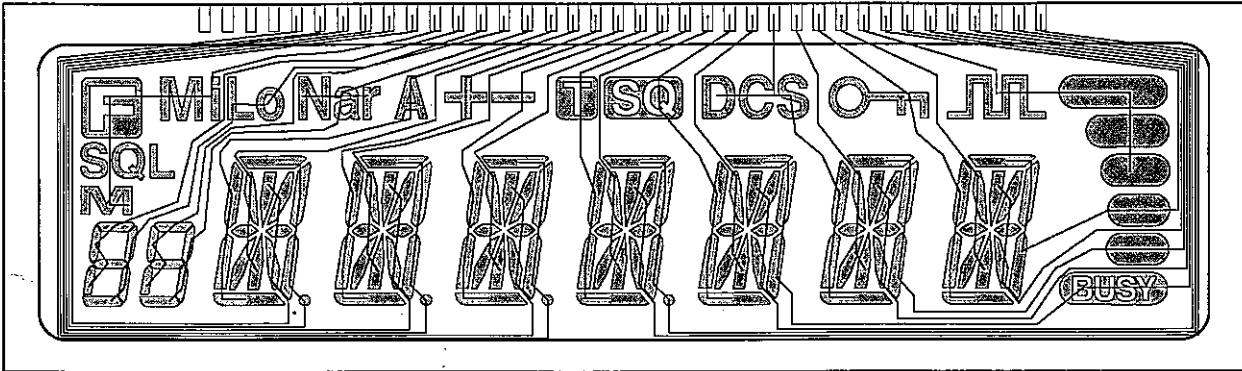
## ELECTRICAL CHARACTERISTICS ( Tc = 25 °C, unless otherwise noted )

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
Idss	Saturated drain current	Vds = 17V, Vgs = 0V	-	10	μA
Igss	Gate to source leak current	Vgs = 10V, Vds = 0V	-	1	μA
VTH	Threshold voltage	Vds = 12V, Ids = 1mA	1.9	4.9	V
Pout	Output Power	f = 30MHz, Pin = 0.15W, Vdd = 12.5V	6	-	W
ηD	Drain Efficiency	Idq = 0.5A (Vgg Control)	55	-	%
VSWRT	Load VSWR Tolerance	f = 30MHz, Vdd = 12.5V Idq = 0.5A (Vgg Control) Po = 6W (Pin Control) ρl ≤ 20:1 (ALL Phase)	No degradation		-

# 19) LCD Connection (TTR3626UPFDHN)

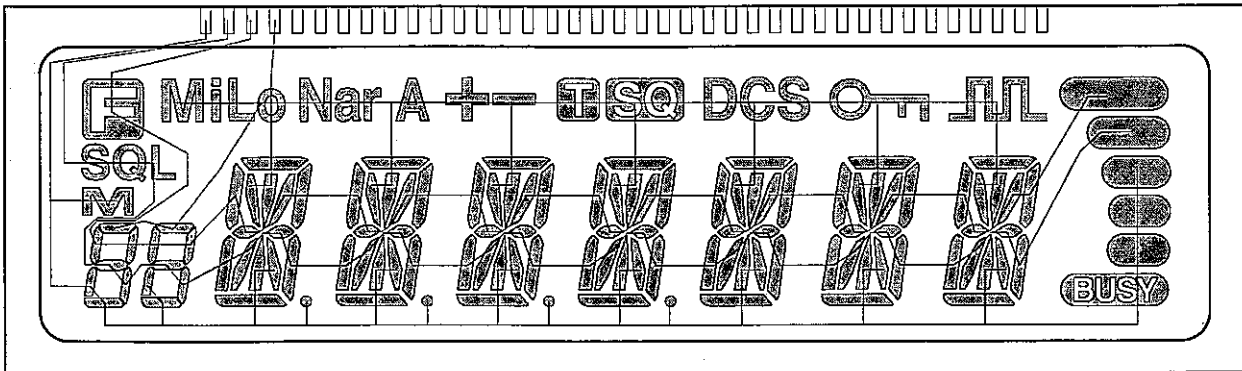
SEG

SEG33  
SEG32  
SEG31  
SEG30  
SEG29  
SEG28  
SEG26  
SEG25  
SEG24  
SEG23  
SEG22  
SEG21  
SEG20  
SEG19  
SEG18  
SEG17  
SEG16  
SEG15  
SEG14  
SEG13  
SEG12  
SEG11  
SEG10  
SEG9  
SEG8  
SEG7  
SEG6  
SEG5  
SEG4  
SEG3  
SEG2  
SEG1  
SEG0



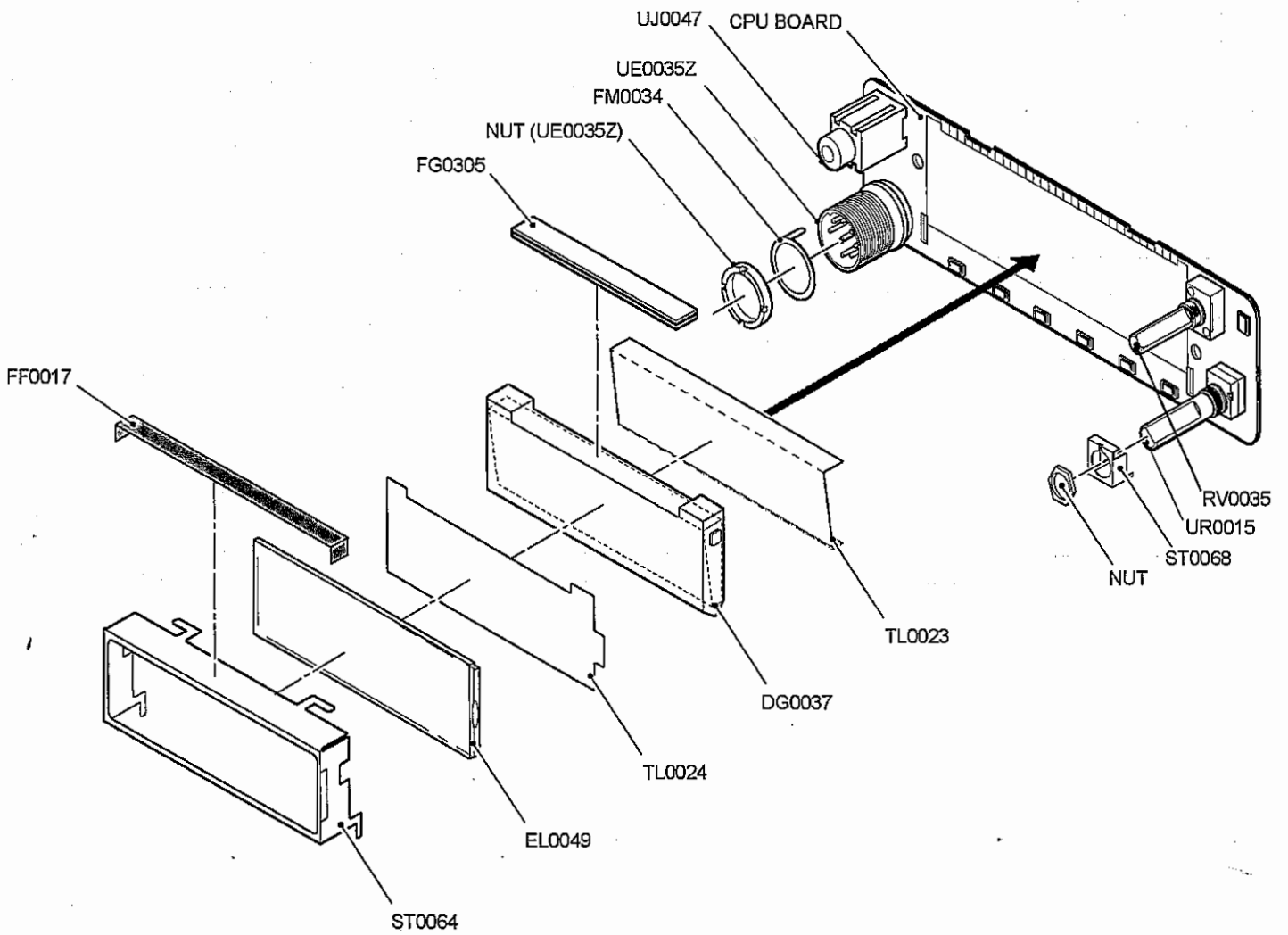
COM

COM3  
COM2  
COM1  
COM0

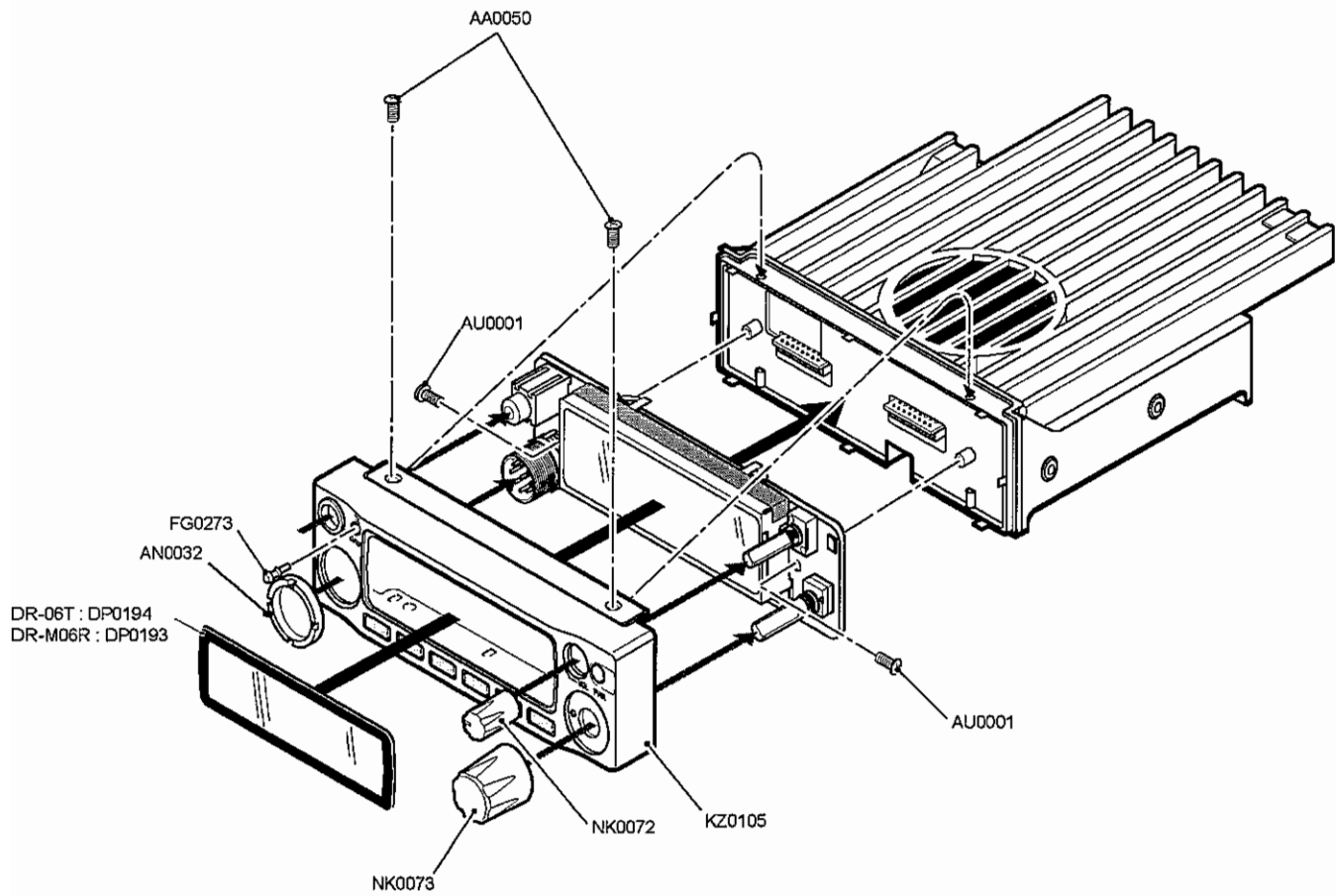


# EXPLODED VIEW

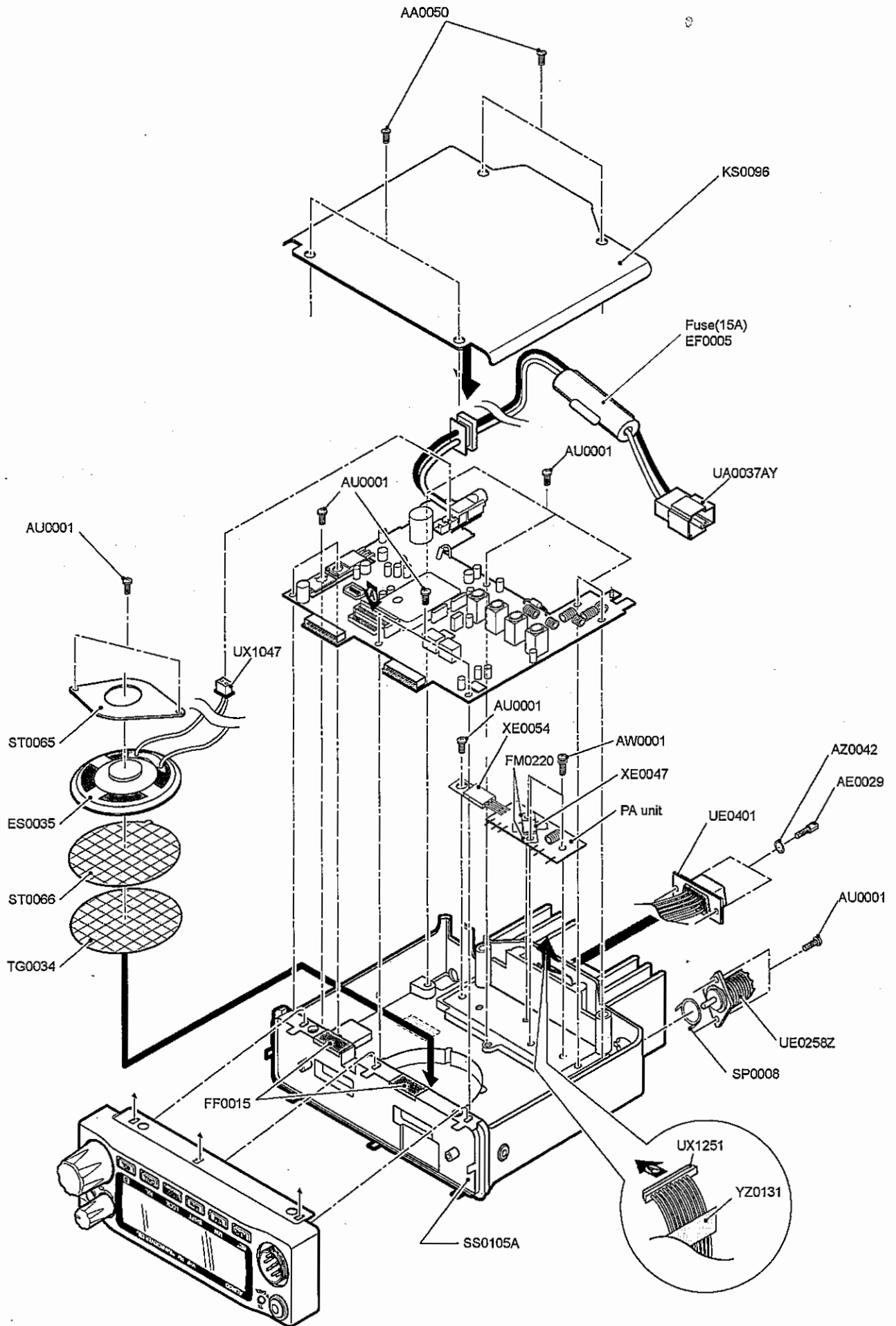
## 1) LCD Assembly



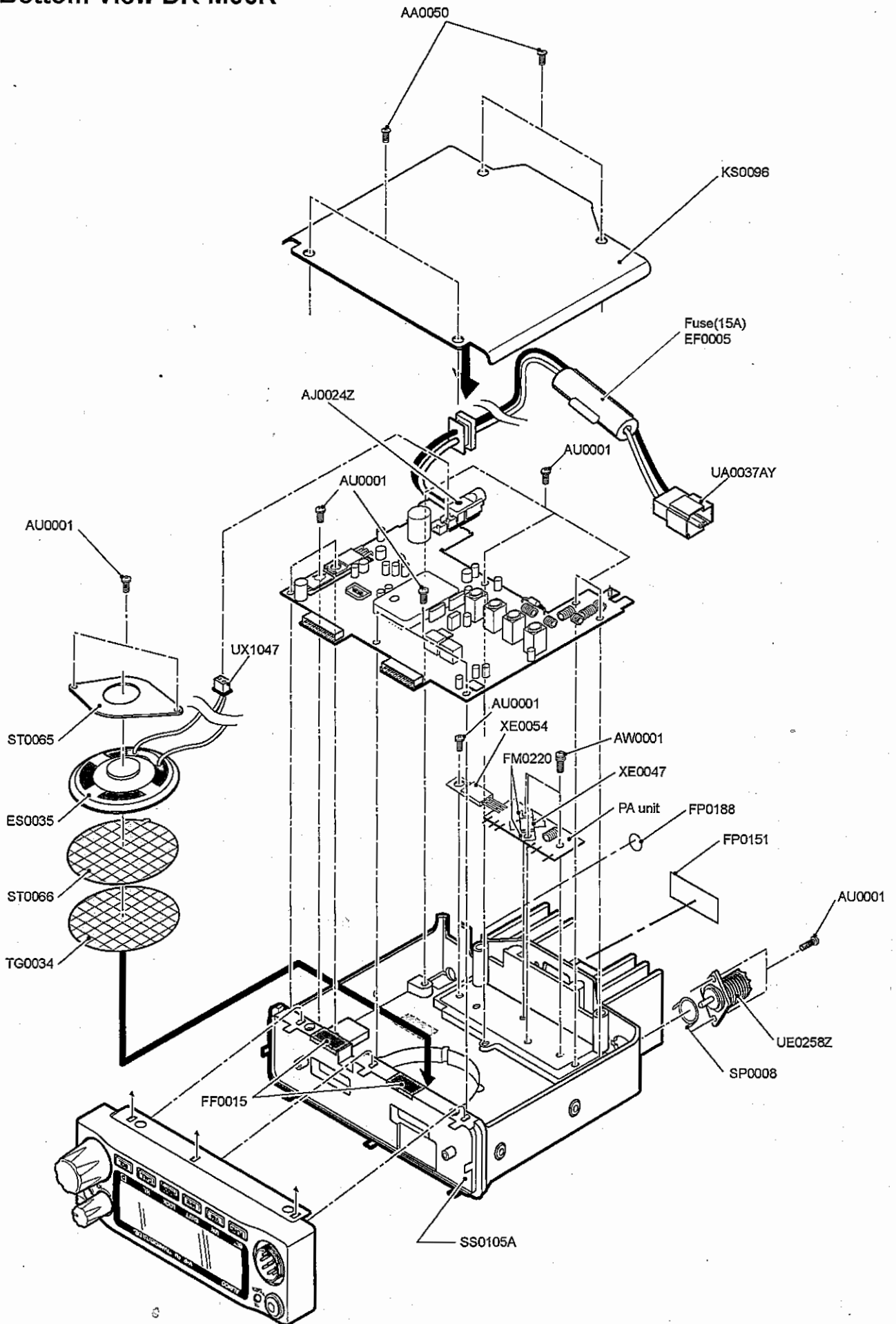
## 2) Top and Front View



### 3) Bottom View DR-06T



# 4) Bottom View DR-M06R















## Packing Parts

Ref No.	Part No.	Description	Parts Name	Qty.	
				DR-06T	DR-M06R
	HK0675	Package	INDIVIDUAL BOX DRM06	0	1
	HK0676	Package	INDIVIDUAL BOX DR06	1	0
	HM0218Z	Carton Box	MASTER CARTON DR135Z	0.2	0.2
	HP0035	Plastic Bag	E.BAG 5X200X250	1	1
	HU0099Z	P.MTL/Carton	FRONT INNER DR605	1	1
	HU0159Z	P.MTL/Carton	INNER DR135T	1	1
	HU0161Z	P.MTL/Carton	INNER 5 PCS	0.4	0.4
	PR0478	Label	SERIAL SEAL	0.2	0.2
	PR0513	Label	NITTO 13X13 LABEL(W)	5	5
	PR0514	Label	EPSON 10X49 LABEL(W)	2	2
	PR0515	Label	NITTO 25X40 LABEL(W)	1	0

## ACCESSORIES

Ref No.	Part No.	Description	Parts Name	Qty.	
				DR-06T	DR-M06R
	ADFM78	Bracket	BRACKET DR130	1	1
	ADUA38	Power Cable	R-B2.0X3M RECEPT.15A	1	1
	AJ0025	Screw	PH T3.5+10 FE/N 1	2	2
	EBC-7	Mic Hanger	MIC HANGER	1	1
	EHM53B	Microphone	MICROPHON EMS53B	0	1
	EHM57D	Microphone	MICROPHON EMS57D	1	0
	HP0009	Plastic Bag	PLA.BAG 5X125X250	1	1
	HP0016	Plastic Bag	PLA.BAG 5X75X90	1	1
	PH0015	Sheet	WARRANTY CEAT EXPOR	1	0
	PK0126	Diagram	SCHEMATIC DR06T	1	0
	PR0454Y	Label	SECURITY STICKER T	2	0
	PS0530B	Manual	INSTRUCTION DR135LH	1	1
	UX1259	Wire	WIRE SCR1 DR135T	1	0
	UX1260	Wire	WIRE SCR2 DR135T	1	0
	YZ0138	Tape	TAPE EBC7	1	1

## ACCESSORIES (SCREW SET)

Ref No.	Part No.	Description	Parts Name	Qty.	
				DR-06T	DR-M06R
	AA0013	Screw	BH M5+20 FE/ZN	4	4
	AE0012	Nut	HEXH/D M4+8 FE/3BBC	4	4
	AJ0003	Screw	BH T5+20 FE/ZN 1	4	4
	AN0002	Nut	HEX N5X0.8 FE/ZN	4	4
	AZ0009	Washer	SW 5X9.2X1.3 FE/ZN	4	4
	AZ0010	Washer	SW 5X12X0.8 FE/ZN	4	4
	EF0005	Fuse	FGBO 15A	2	2
	FM0079Z	Spanner	SPANNER DR130	1	1
	HP0006	Plastic Bag	5X90X170	1	1
	YZ0121	Tape	TAPE 10MM	2	2



# ADJUSTMENT

## 1) Adjustment Spot

Power Supply Voltage 13.8V

Output of SSG is all EMF indication.

If without instruction, WIDE mode.

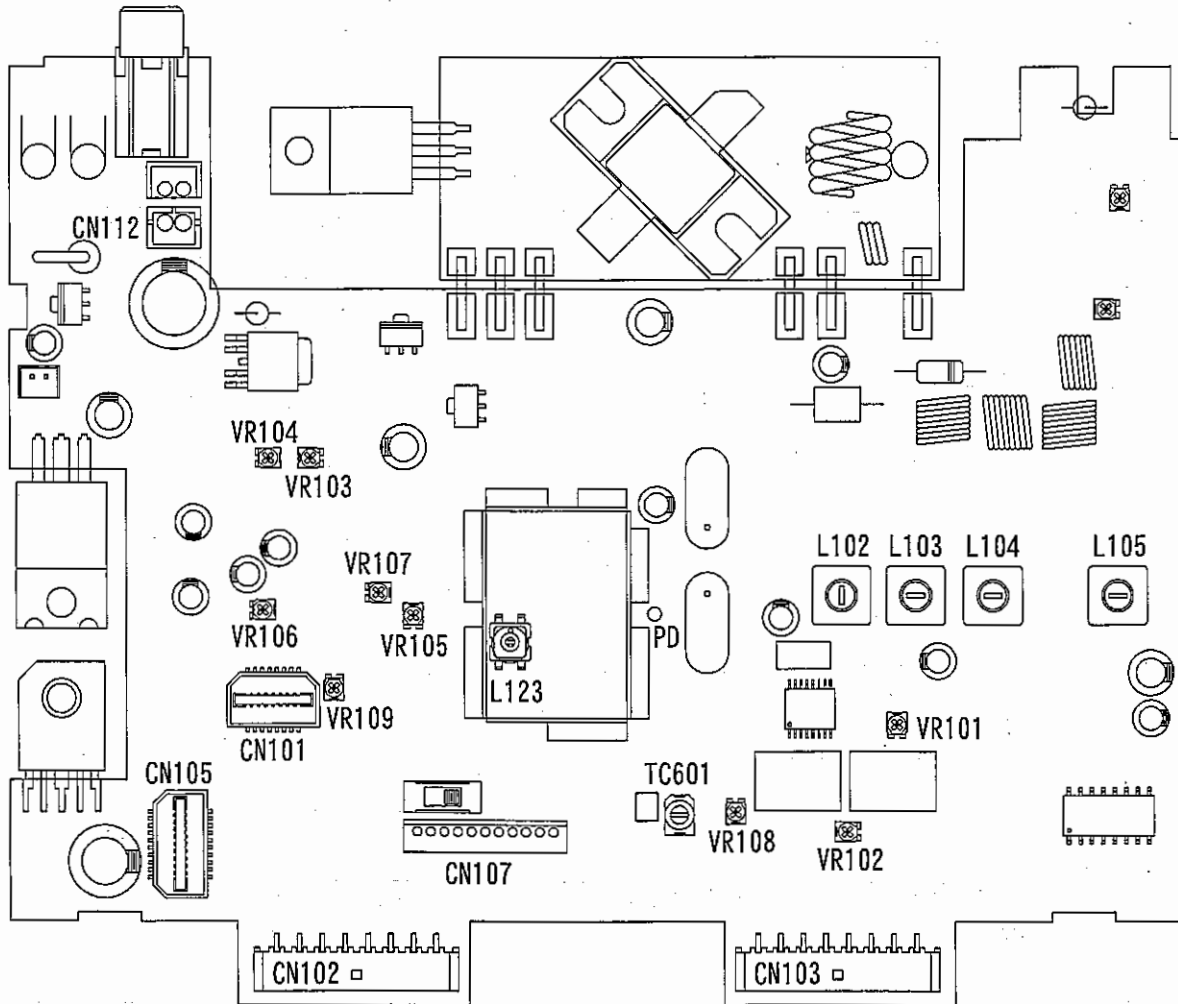
If without instruction, SSG output is MOD 1KHz WIDE DEV 3.5KHz/DEV,  
NARROW DEV 1.75KHz/DEV.

Standard modulation is also based above.

Speaker load is 8 ohm and output is 50 ~ 100 mV.

NARROW Mode : ONLY DR-06T

Rx expansion : MHz + PWR ON (ONLY DR-06T)





## 2) VCO and RX Adjustment Specification

ITEM	CONDITION	UNIT	ADJ. SPOT	ADJUSTING MRTHOD
Adjustment Frequency	52.00MHz TX	MAIN	TC601	Adjust so that Tx Frequency becomes within 52.00MHz +/- 100Hz
VCO Adjustment	52.00MHz RX	MAIN	L123	Adjust so that PD voltage becomes 4.6 +/- 0.1V
Rx Signal Sensitivity Adjustment	52.05MHz  40.05MHz 50.05MHz 52.05MHz 54.05MHz 69.95MHz	MAIN	L105, L104 L103, L102	Repeatedly adjust so that the Rx sensitivity becomes in maximum/. Confirm: At 0dBu SINAD more than 12dB At -9dBu SINAD more than 12dB At -9dBu SINAD more than 12dB At -9dBu SINAD more than 12dB At 0dBu SINAD more than 12dB
Squelch Adjustment	52.05MHz SSG OFF Indicate 01	MAIN	VR101	Adjust so that the squelch stops at perfectly close location
S Meter Adjustment	52.05MHz SSG 20dBu 1KHz 3.5KHz/DEV	MAIN	VR102	Adjust so that all the indicator appears

## 3) TX Adjustment Specification

ITEM	CONDITION	UNIT	ADJ. SPOT	ADJUSTING MRTHOD
HI POWER Adjustment	52.00MHz HI POWER	MAIN	VR103	Adjust to 50.0 +/- 0.5W
MID POWER Adjustment	52.00MHz MID POWER	MAIN	VR104	Adjust to 20.0 +/- 0.5W
LOW POWER Confirmation	52.00MHz LOW POWER	MAIN		Confirm if it becomes 5.0 +/- 3.0W
Maximum Deviation Adjustment	52.00MHz MOD 1KHz 40mVemf	MAIN	VR107	4.5 +/- 0.1KHz/DEV
Maximum Deviation Adjustment	52.00MHz MOD 1KHz 40mVemf NARROW	MAIN	VR105	2.2 +/- 0.1KHz/DEV (ONLY DR-06T)
Mic Gain Adjustment	52.00MHz MOD 1KHz 4mVemf	MAIN	VR106	3.0 +/- 0.1KHz/DEV
CTCSS Modulation Level Confirmation	52.00MHz 88.5Hz	MAIN		800 +/- 200Hz/DEV 3KHz LPF ON
DCS Modulation Level Adjustment	52.00MHz 255 Code	MAIN	VR108	800 +/- 100Hz/DEV 3KHz LPF ON
1750Hz Modulation Level Adjustment	52.00MHz 1750Hz	MAIN	VR109	3.0 +/- 0.1KHz/DEV
DTMF Modulation Level Confirmation	52.00MHz DTMF 1 Press the V/M key during TX	MAIN		3.0 +/- 0.5KHz/DEV



#### 4) RX Test Specification

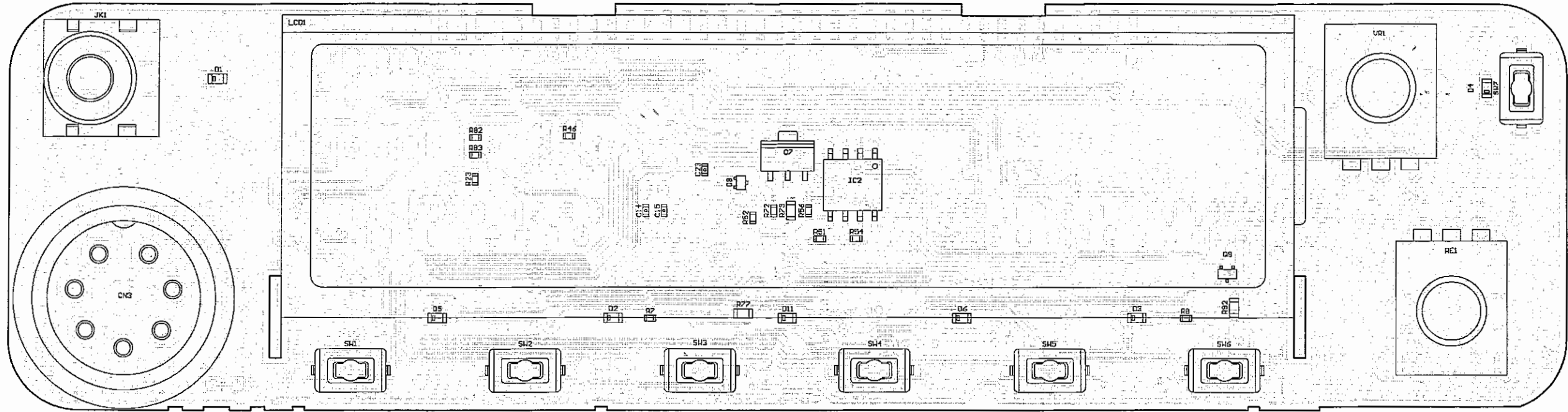
TEST ITEM	CONDITION	ADJ. STANDARD	TEST STANDARD	NOTE
RX Signal Sensitivity	40.05MHz 50.05MHz 52.05MHz 54.05MHz 69.95MHz	Less than 0dBu Less than -9dBu Less than -9dBu Less than -9dBu Less than 0dBu	Less than 0dBu Less than -8dBu Less than -8dBu Less than -8dBu Less than 0dBu	12dB SINAD
	52.05MHz NARROW	Less than -9dBu	Less than -8dBu	12dB SINAD (ONLY DR-06T)
RX Distortion	52.05MHz WIDE	Less than 4%	Less than 5%	SSG Output 30dBu
	52.05MHz NARROW			SSG Output 30dBu (ONLY DR-06T)
RX S/N	52.05MHz WIDE	More than 40dB	More than 38dB	SSG Output 30dBu 0.3 ~ 3KHz BPF OFF
	52.05MHz NARROW	More than 34dB	More than 32dB	SSG Output 30dBu 0.3 ~ 3KHz BPF OFF (ONLY DR-06T)
Squelch Sensitivity	52.05MHz Indication 02	Squelch Open	Squelch Open	SSG Output -10dBu
		Squelch Close	Squelch Close	SSG Output OFF
S Meter	52.05MHz 1KHz 3.5KHz/DEV	All appears at 20dBu	All appears at 25dBu	Decrease SSG level and decrease S Meter level
AF Output	52.05MHz	More than 2W	More than 2W	SSG Output 30dBu
CTCSS Sensitivity	29.05MHz WIDE	Open at 500Hz/DEV	Open at 500Hz/DEV	SSG Output 0dBu 88.5Hz
	52.05MHz NARROW	Open at 250Hz/DEV	Open at 250Hz/DEV	SSG Output 0dBu 88.5Hz (ONLY DR-06T)
DCS Sensitivity	52.05MHz WIDE	Opens when Test Equipment is in TX	Opens when Test Equipment is in TX	255 Code
	52.05MHz NARROW	Opens when Test Equipment is in TX	Opens when Test Equipment is in TX	255 Code (ONLY DR-06T)
Drain Current	52.05MHz	Less than 0.65A	Less than 0.65A	Max volume
Power off Current	52.05MHz	Less than 10mA	Less than 10mA	Power off
Howling	52.05MHz	Don't occur	Don't occur	SSG Output 60dBu Mod off, Max volume

## 5) TX Test Specification

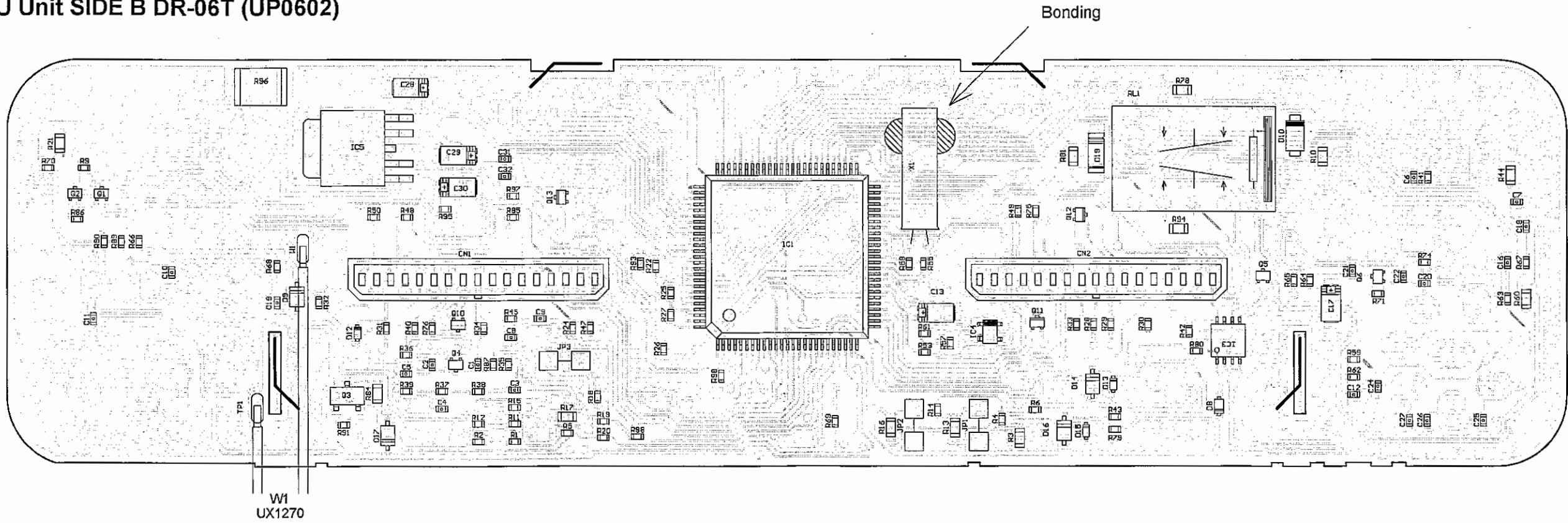
TEST ITEM	CONDITION	ADJ. STANDARD	TEST STANDARD	NOTE
Tx Output HI POWER	50.00MHz 52.00MHz 53.95MHz	50 +/- 0.5W	51 +/- 4W 50 +/- 3W 50 +/- 3W	
Tx Output MID POWER	52.00MHz	20 +/- 0.5W	20 +/- 2W	
Tx Output LOW POWER	52.00MHz	5 +/- 3W	5 +/- 3W	
Drain Current	52.00MHz	Less than 10A	Less than 11A	
Frequency Deviation	52.00MHz	Within +/- 0.1KHz	Within +/- 0.5KHz	
Spurious	50.00MHz 52.00MHz 53.95MHz	More than 65dB More than 65dB More than 65dB	More than 60dB More than 60dB More than 60dB	MID and LOW standard power is also the same as of HI power level
Modulation Level	52.00MHz WIDE	3.0 +/- 0.1KHz/DEV 4.5 +/- 0.1KHz/DEV	3.0 +/- 0.2KHz/DEV 4.5 +/- 0.2KHz/DEV	MIC in 1KHz 4mVemf MIC in 1KHz 40mVemf
	52.00MHz NARROW	2.2 +/- 0.1KHz/DEV	2.2 +/- 0.2KHz/DEV	MIC in 1KHz 40mVemf (ONLY DR-06T)
CTCSS Modulation Level	52.00MHz	800 +/- 200Hz/DEV	800 +/- 300Hz/DEV	88.5Hz 3KHz LPF ON
DCS Modulation Level	52.00MHz WIDE	800 +/- 100Hz/DEV	800 +/- 200Hz/DEV	255 Code 3KHz LPF ON
	52.00MHz NARROW	500 +/- 200Hz/DEV	500 +/- 200Hz/DEV	255 Code 3KHz LPF ON (ONLY DR-06T)
1750Hz Modulation Level	52.00MHz	3.0 +/- 0.1KHz/DEV	3.0 +/- 0.5KHz/DEV	
DTMF Modulation Level	52.00MHz	3.0 +/- 0.5KHz/DEV	3.0 +/- 0.5KHz/DEV	Press the V/M key during TX
Modulation Distortion	52.00MHz	Less than 3%	Less than 4%	
TX S/N	52.00MHz WIDE	More than 40dB	More than 38dB	0.3 ~ 3KHz BPF ON
	52.00MHz NARROW	More than 34dB	More than 32dB	0.3 ~ 3KHz BPF ON (ONLY DR-06T)

# PC BOARD VIEW

## 1) CPU Unit SIDE A DR-06T (UP0602)

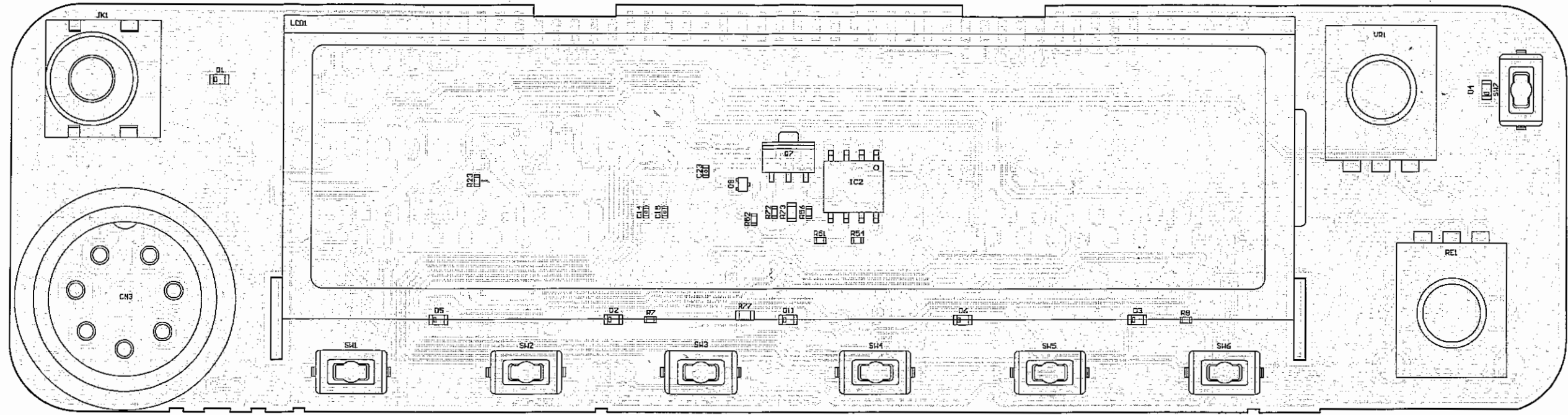


## 2) CPU Unit SIDE B DR-06T (UP0602)

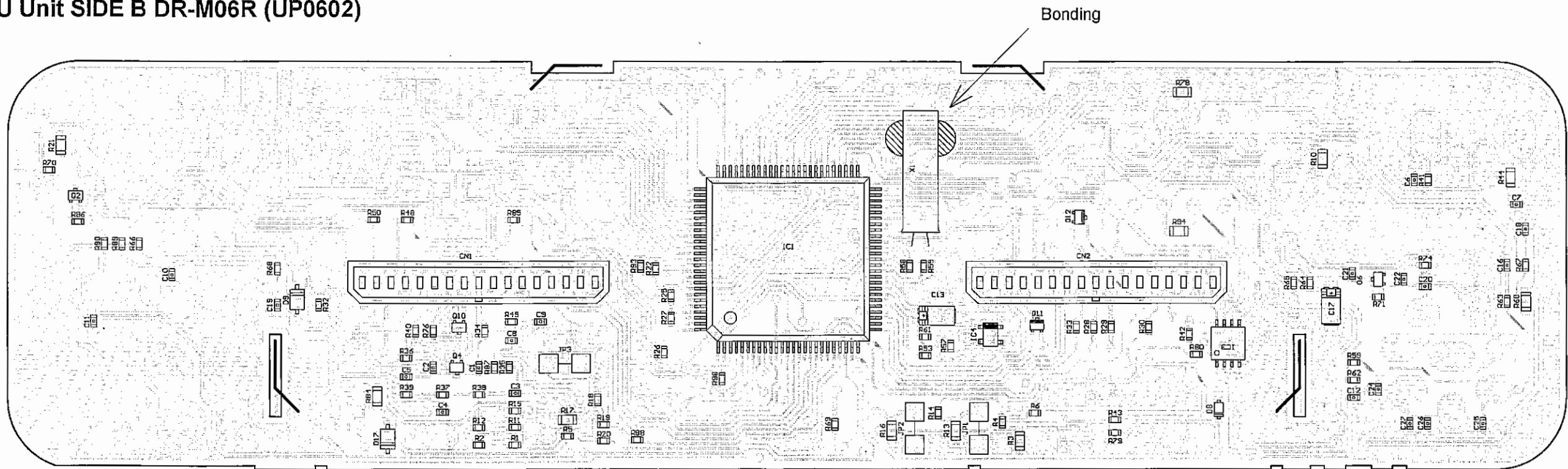


# PC BOARD VIEW

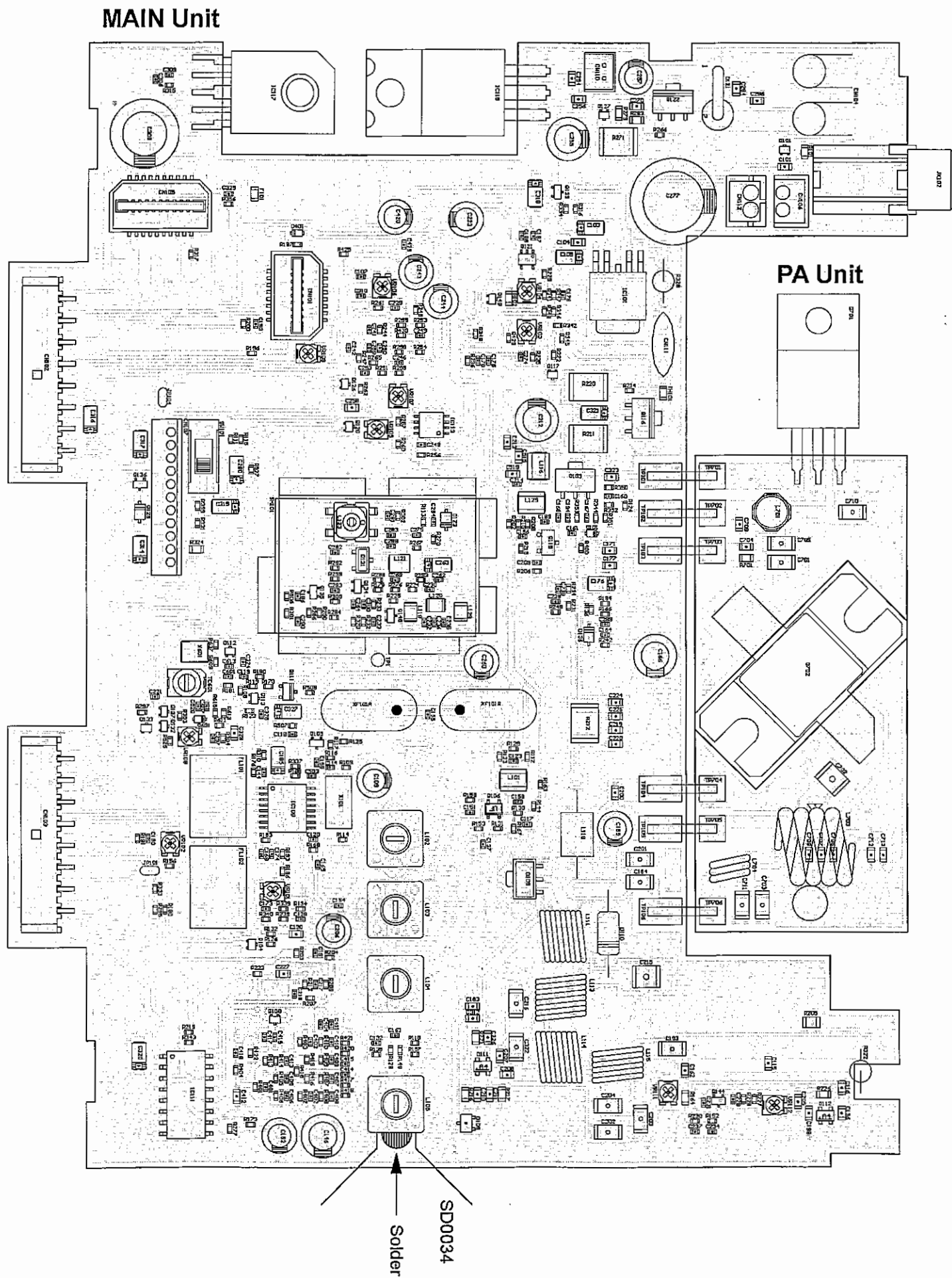
## 3) CPU Unit SIDE A DR-M06R (UP0602)



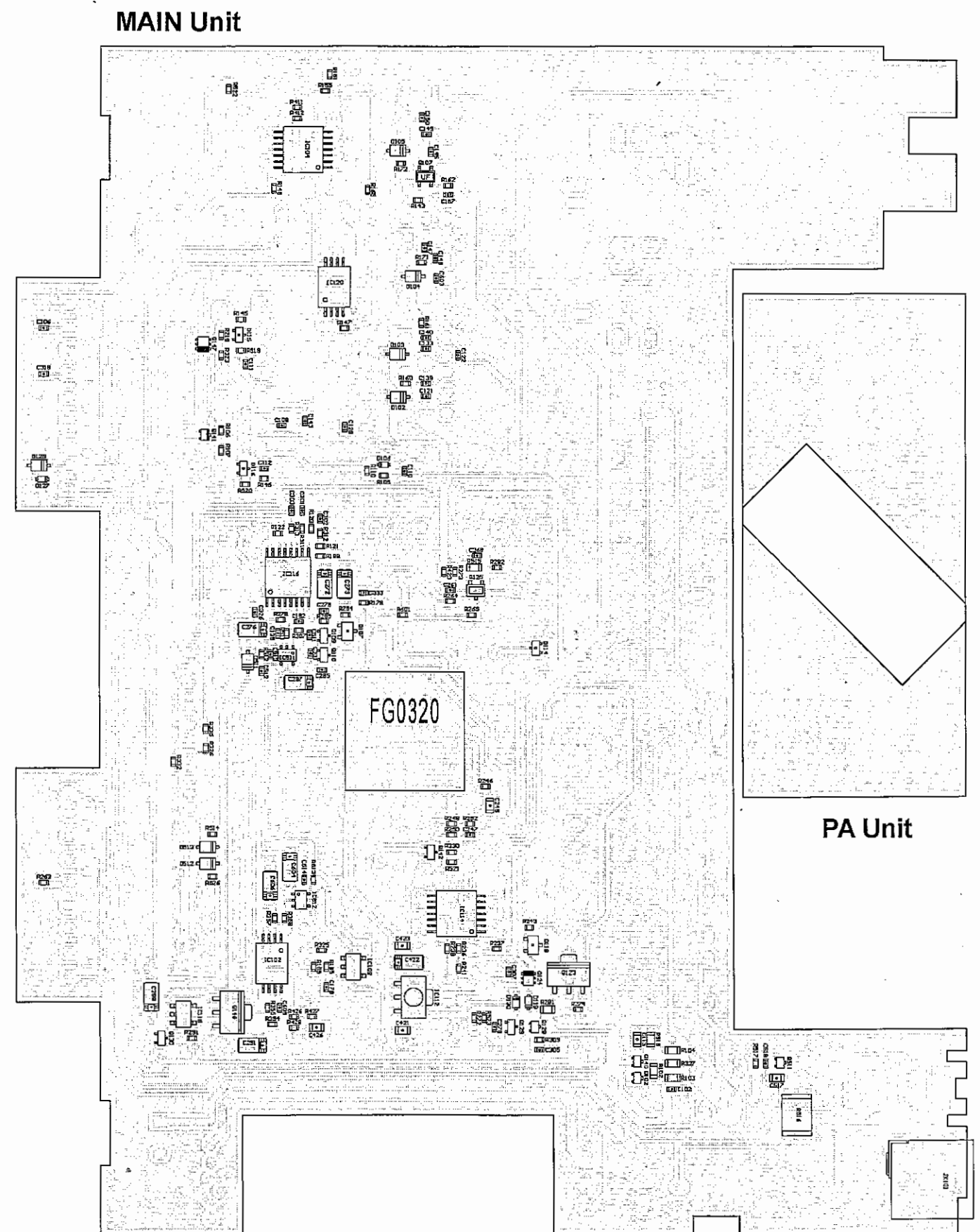
## 4) CPU Unit SIDE B DR-M06R (UP0602)



5) MAIN / PA Unit Side A DR-06T (UP0602)

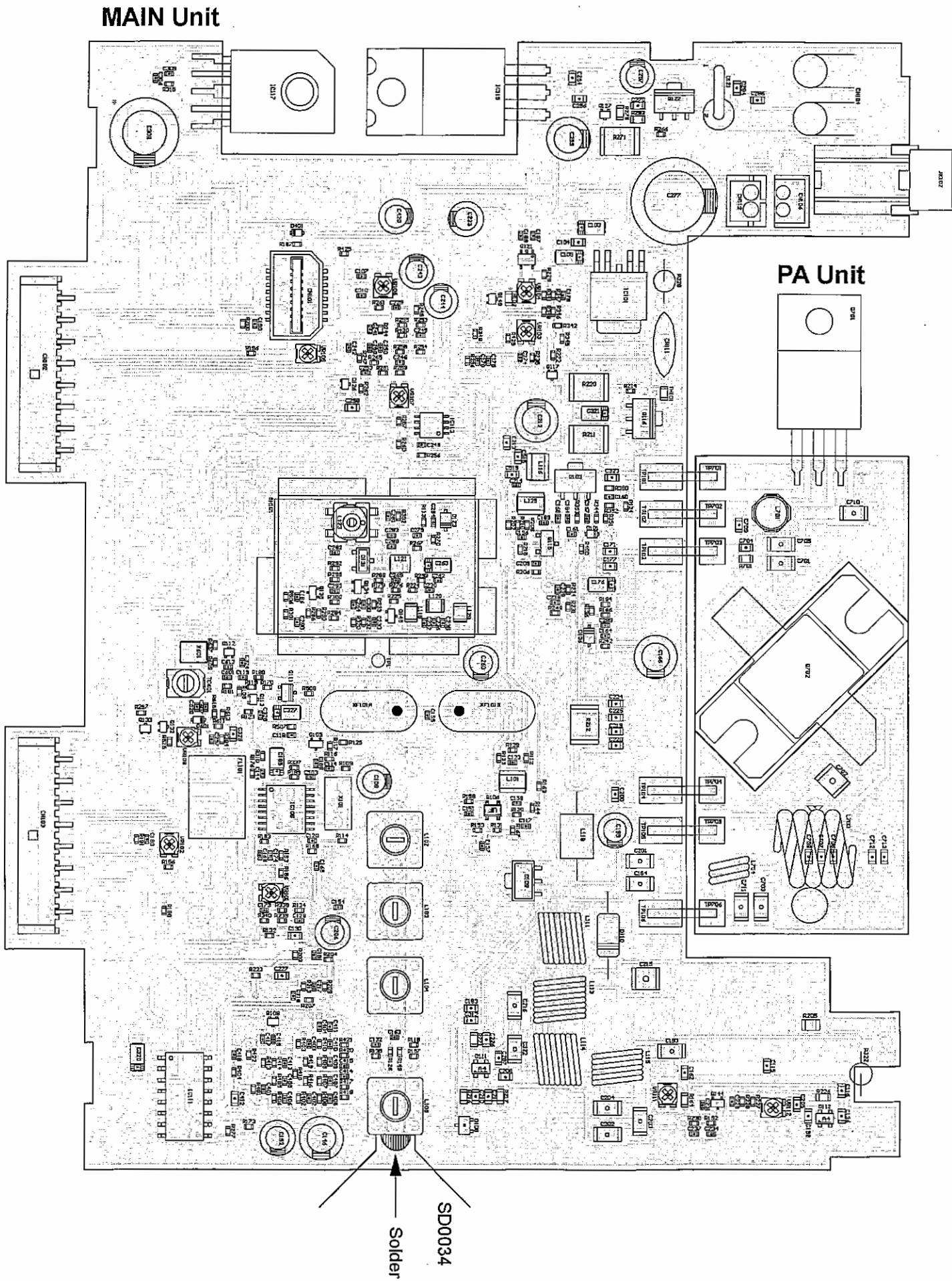


6) MAIN / PA Unit Side B DR-06T (UP0602)

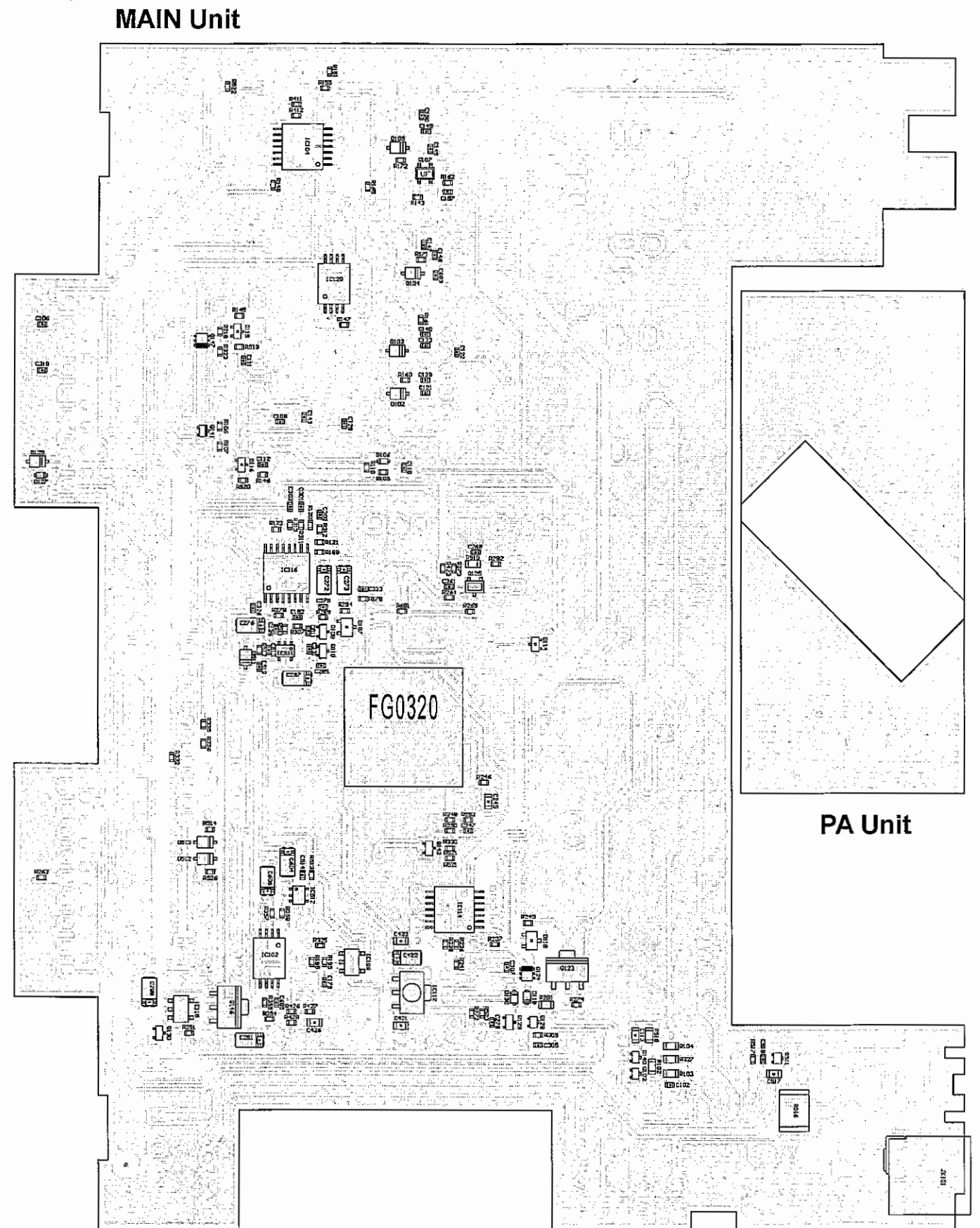




7) MAIN / PA Unit Side A DR-M06R (UP0602)

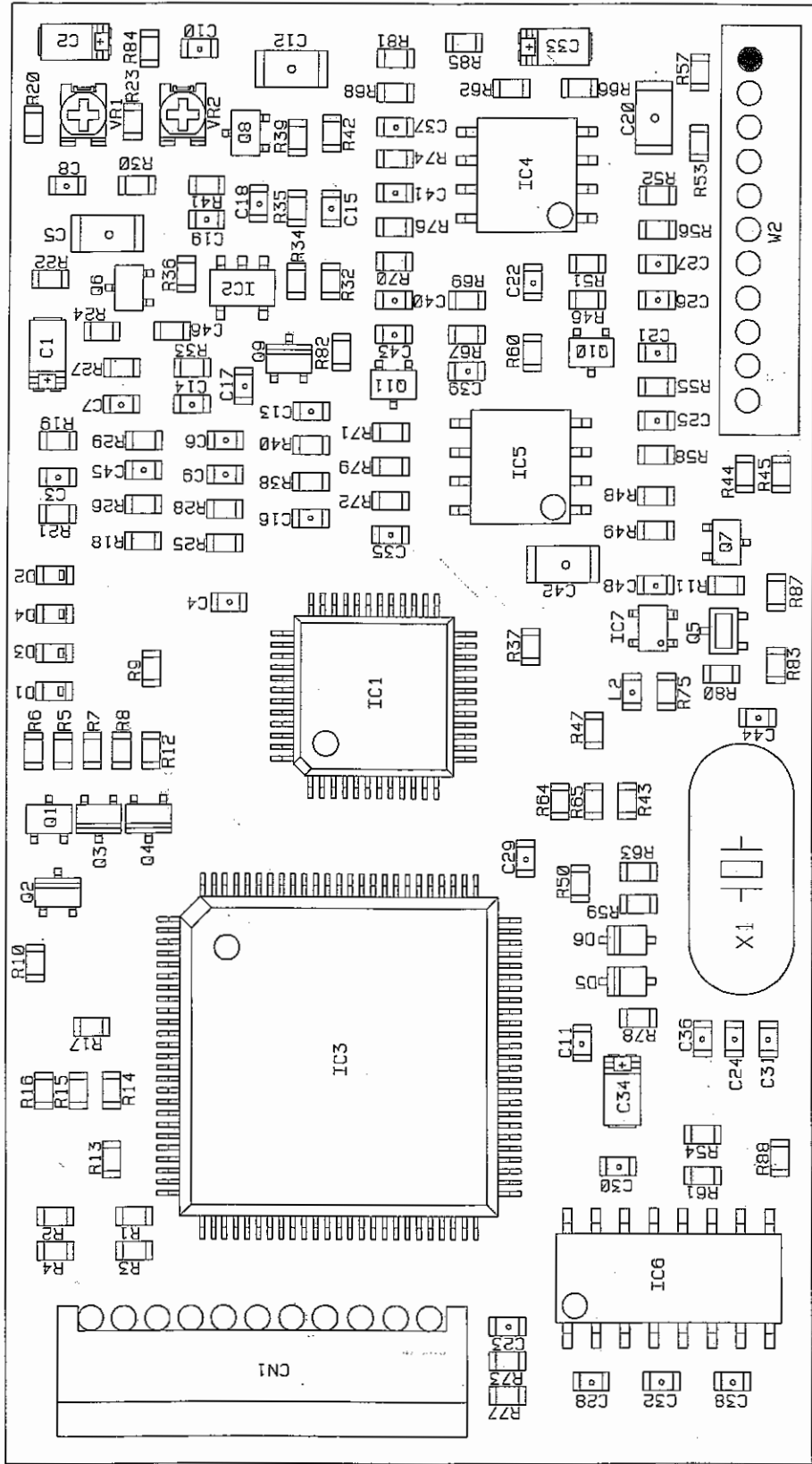


8) MAIN / PA Unit Side B DR-M06R (UP0602)

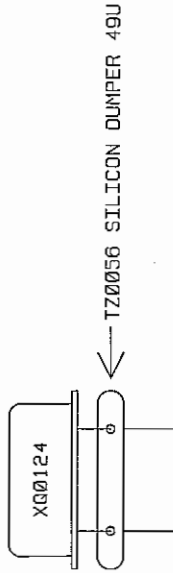
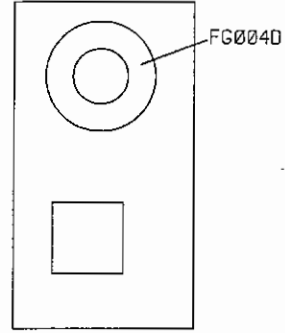


### 9) TNC Unit Side A (UP0402)

OPTION unit (EJ41U)



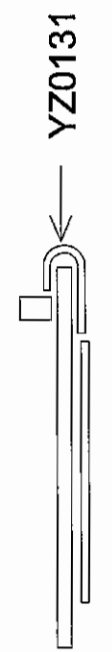
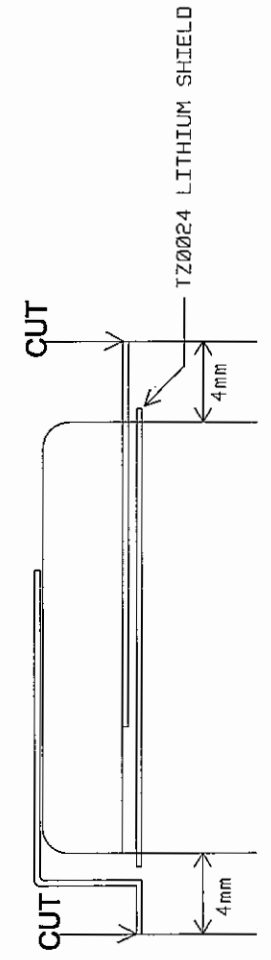
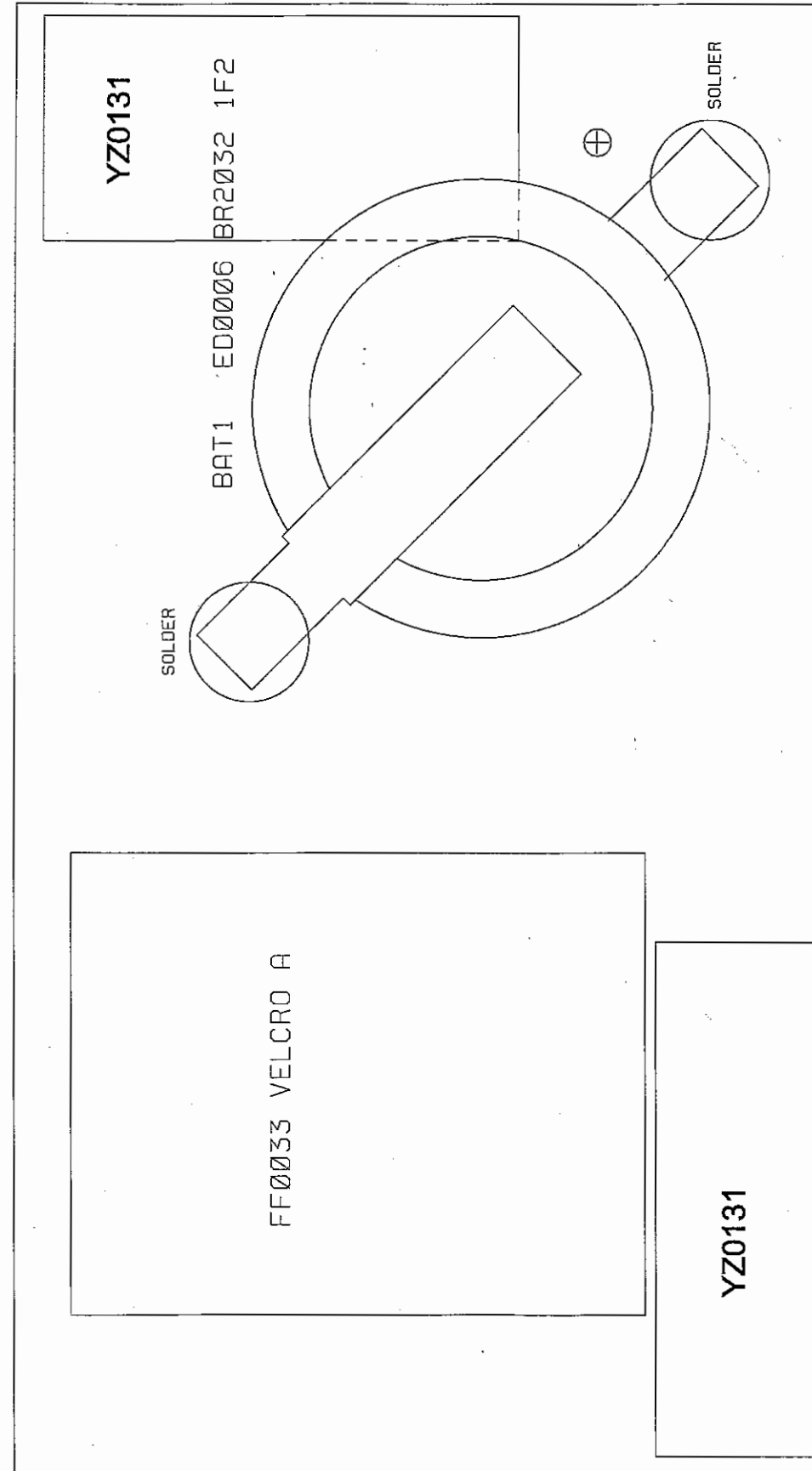
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 CSV  
 AFIN  
 S0C  
 1200  
 SCRCPTJ  
 DMOD  
 MIC1  
 SPO  
 TXD  
 RXD



TZ0056 SILICON DUMPER 49U

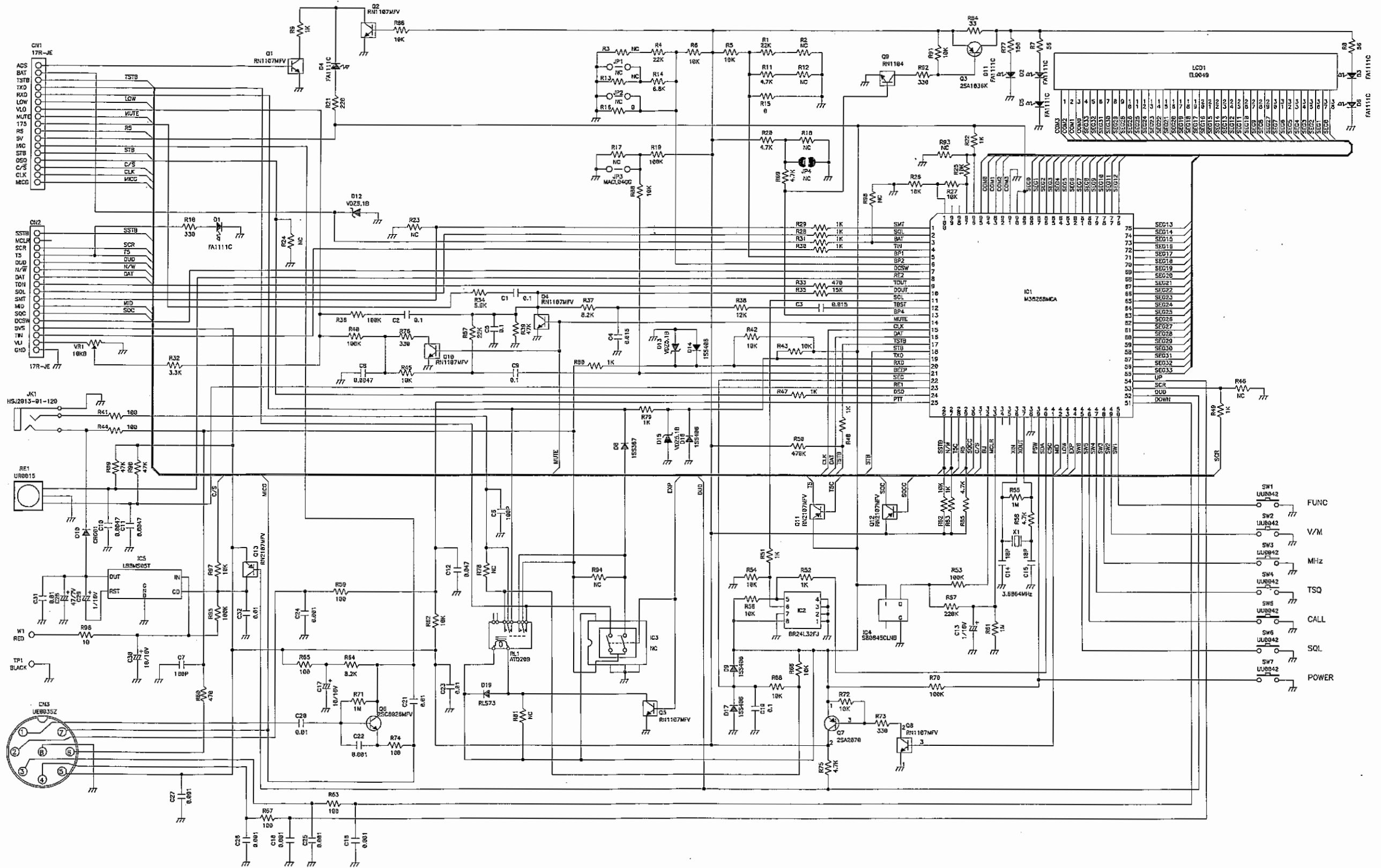
### 10) TNC Unit Side B (UP0402)

OPTION unit (EJ41U)



# SCHEMATIC DIAGRAM

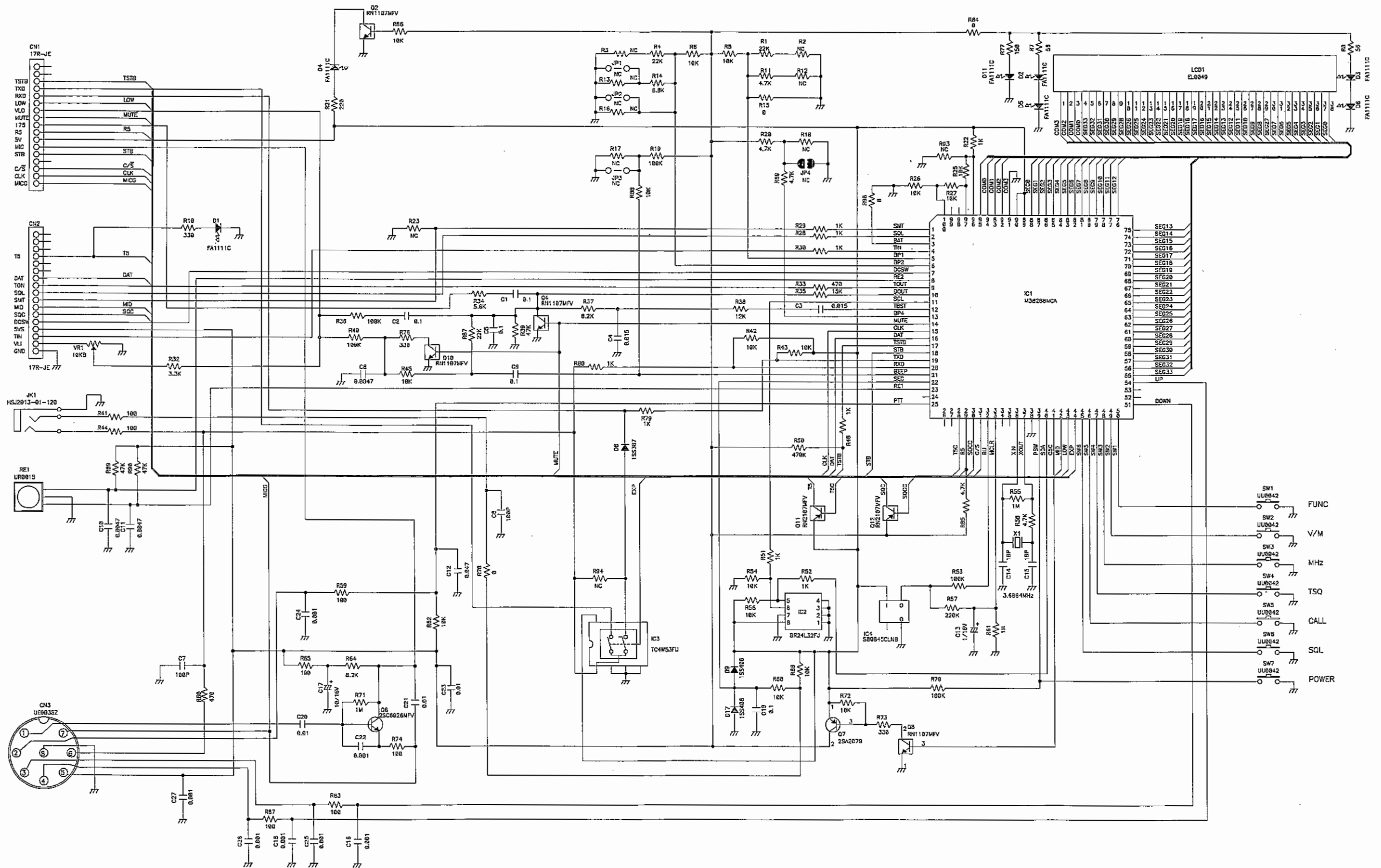
## 1) CPU Unit DR-06T



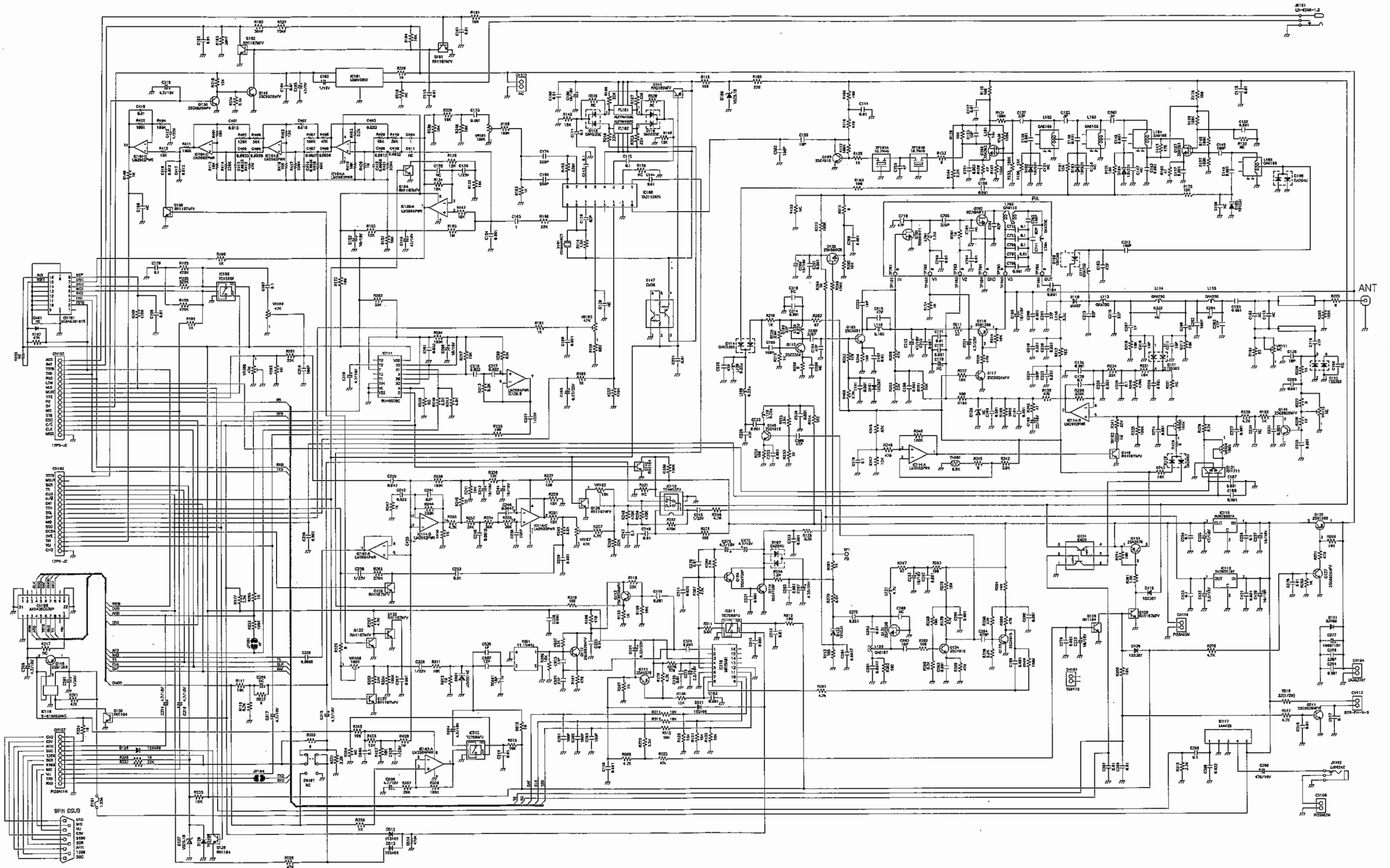


# SCHEMATIC DIAGRAM

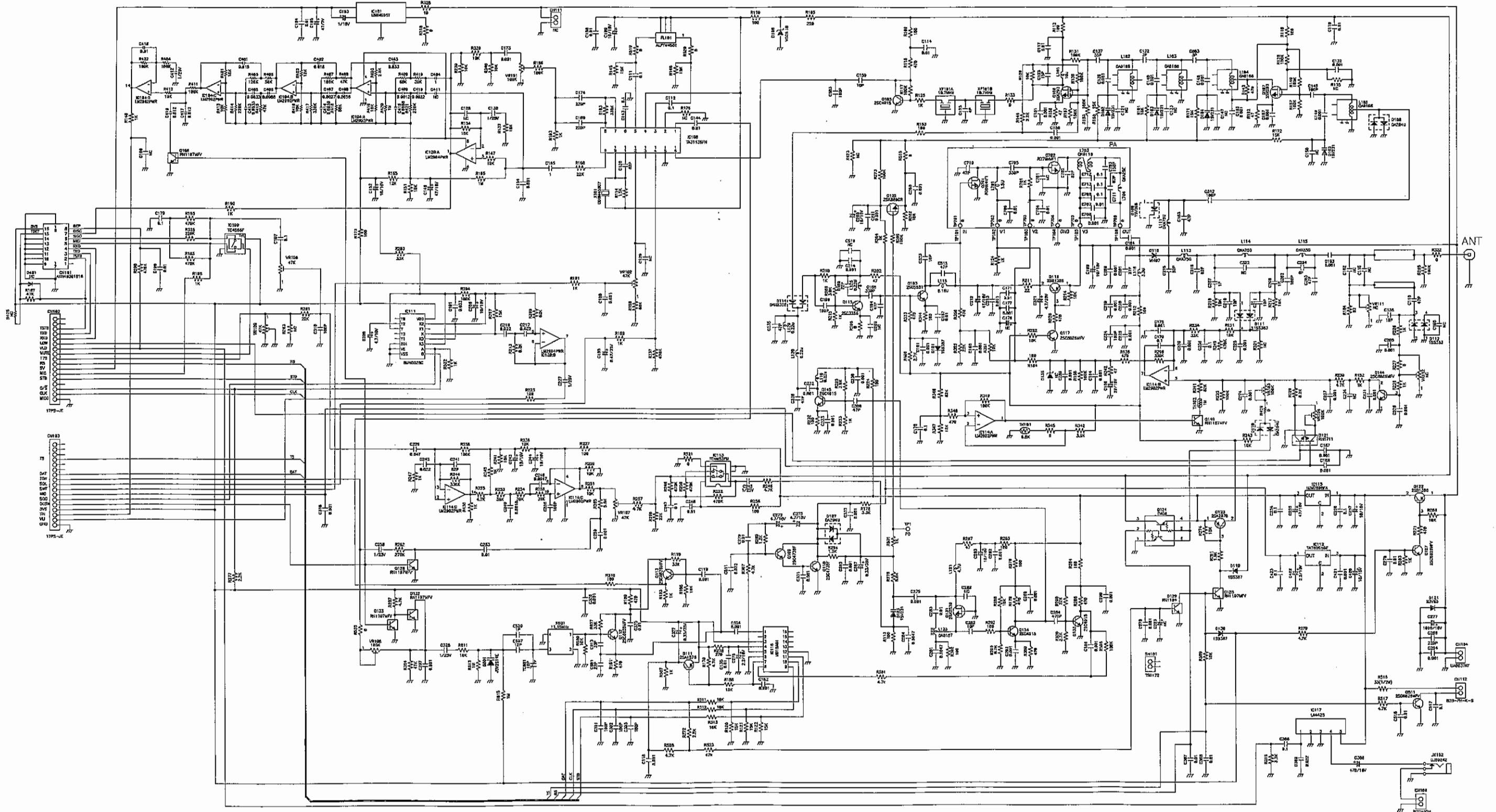
## 2) CPU Unit DR-M06R



### 3) MAIN Unit DR-06T

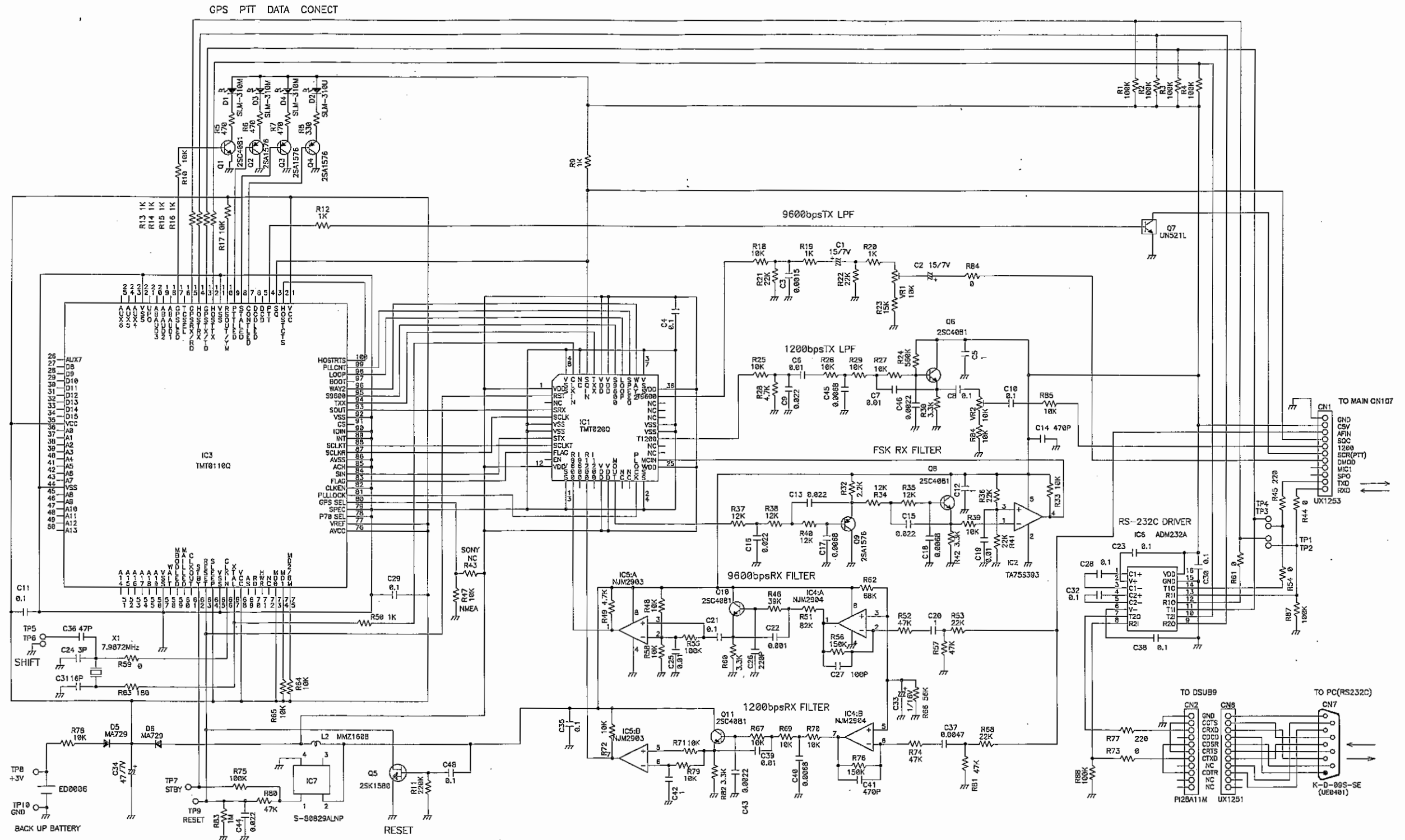


# 4) MAIN Unit DR-M06R



# 5) TNC Unit

## OPTION Unit (EJ41U)







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Dealer/Distributor