KENWOOD

ALL BAND HF TRANSCEIVER

TS-940S

TECHNICAL INFORMATION

CONTENTS

DX'cellence!!

TRIO-KENWOOD is a multi-national, high-technology company with annual sales in the hundreds of millions of dollars. Founded in 1946, it has come to be recognized all over the world as a producer of the highest quality, most technologically advanced electronics equipment.

TRIO-KENWOOD produces a broad line of amateur radio and land mobile radio products, home video equipment, the finest quality home and car stereo, and a complete line of electronic test equipment, including state-of-the-art solid-state wide band oscilloscopes.

TRIO-KENWOOD enjoys a strong position of leadership, based on a long history of involvement in the design and production of the highest quality amateur radio products. Our engineering department is always hard at work developing new concepts, especially in the field of digital technology and basic performance. Quickly recognizing the tremendous potential for product sophistication through the application of its digital know-how, TRIO-KENWOOD developed a new, state-of-the-art competition class HF transceiver, the TS-940S. The TS-940S has every conceivable feature, and is designed for SSB, CW, AM, FM and FSK operation on all amateur bands, 160 through 10 meters. It incorporates an outstanding 150 kHz to 30 MHz general coverage receiver having superior dynamic range.

FEATURES

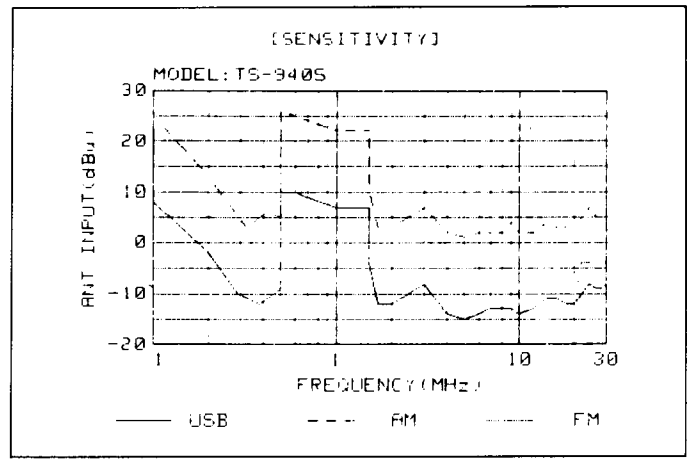
OUTSTANDING RECEIVER PERFORMANCE AND SENSITIVITY.

Superior Dynamic Range Receiver Front End.

The TS-940S RF circuits have been specifically designed to provide the lowest noise floor level coupled with a superior dynamic range. Use of 2SK125 junction-type FET's wired in a cascode amplifier circuit, followed by two 2SK125's each in the first balanced mixer and in the push-pull source follower buffer amplifier, and working into a 2nd balanced mixer circuit, results in outstanding two signal characteristics accompanied by a substantially improved noise floor level.

160-m to 10-m Amateur Band Operation with 150kHz to 30 MHz General Coverage Receiver.

The TS-940S covers all Amateur bands from 160 to 10 meters, including the new WARC 30, 17, and 12 meter bands. Its general coverage receiver provides reception on any frequency from 150 kHz to 30 MHz. The TRIO-KENWOOD conceived and engineered digital PLL cirouit provides superior frequency accuracy and stability since only the standard frequency crystal oscillator determines those parameters. Selection of a specific Amateur band may be speedily and efficiently accomplished by the touch of the appropriate band access key (10 keys provided), or through use of the UP/DOWN 1 MHz step band switches, allowing easy access to all frequencies in the 150 kHz to 30 MHz range. Each of the two digital VFO's is continuously tunable from band to band across the full range of the transceiver.



All-Mode Operation.

Modes of operation include USB, LSB, CW, AM, FM, and FSK. Mode selection is quickly effected through use of the proper front panel mode key. An adjacent LED confirms the selection. When a key is depressed, the first letter of the mode selected is announced in Morse code, through the internal speaker, e.g., "L" for LSB, "F" for FM, etc. When

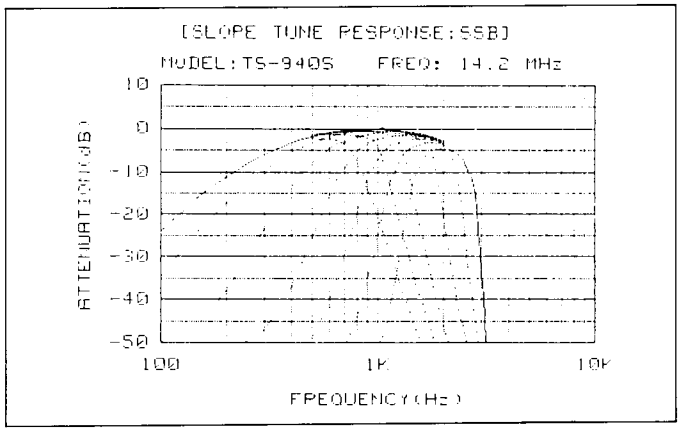
FSK is selected, the Morse code letter "R" (for RTTY) is heard.

Superb Interference Reduction.

The TS-940S incorporates a number of special interference control circuits perfected by TRIO-KENWOOD and described in the following, that give the operator maximum capability to minimize the effect of interference of all kinds.

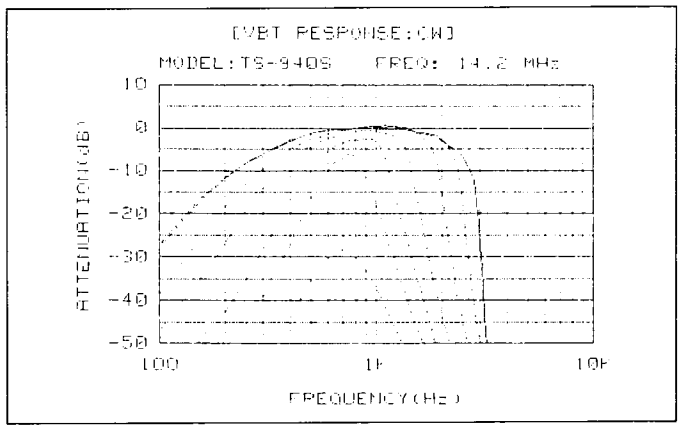
(1.) SSB IF Slope Tuning.

This feature operates in the LSB and USB modes. Front panel controls are provided to allow independent adjustment of either the low frequency or high frequency slopes of the IF passband. These HIGH CUT and LOW CUT controls permit the operator to easily and quickly define the most ideal IF passband width consistent with readability and interference rejection, and based on conditions as they exist at the time of the contact. The settings of the controls may be graphically illustrated on the LCD sub-display panel.



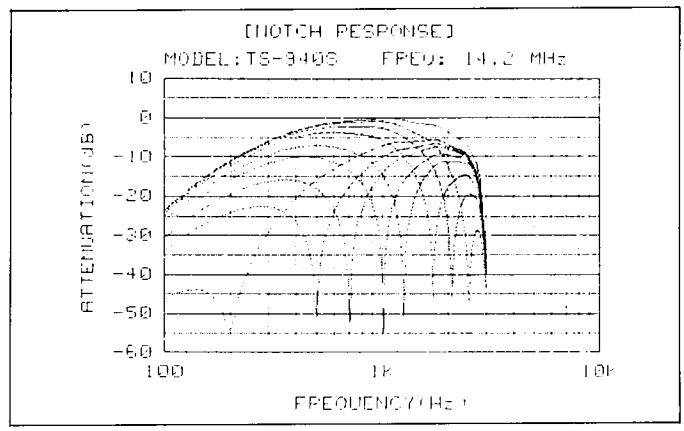
(2.) CW VBT (Variable Bandwidth Tuning.)

When all optional filters are installed, CW VBT operates in the CW, FSK, and AM modes. When none of the optional filters are installed, CW VBT operates in the CW and FSK modes with the filter switch positioned at WIDE, and in the AM mode with the filter switch positioned at NARROW. In the CW mode of operation, the CW VBT and pitch control circuits are automatically enabled. The VBT control allows the passband width to be continuously varied within the range of the control without affecting the center frequency. Graphic illustration of these adjustements is accomplished on the LCD sub-display panel.



(3.) IF Notch Filter.

A tunable notch filter is located between the 4th receive mixer and the 100 kHz IF amplifier. The use of L-C-R components in a bridged-T filter circuit at the 100-kHz IF frequency results in deep, sharp notch characteristics that provide attenuation on the order of 40 dB to the interfering signal. This filter operates in all mode (except FM mode).



(4.) AF-Tune.

The AF-Tune operates to reduce interfering signals and white noise, providing a peak tuning characteristic for the AF frequency response. When the front panel "AF-Tune" switch is depressed to the "ON" position, the "AF-Tune" circuit is activated, allowing operation only in the CW mode. The circuit consists of a three pole active filter located between the SSB/CW demodulator and the AF amplifier. It is tunable to a center frequency of 800 Hz, variable ±400 Hz or greater.

(5.) Narrow/Wide Filter Selection.

A front panel "NAR/WIDE" switch allows narrow/wide IF filter selection as required, based on interference conditions.

Built-in CW Variable Pitch Circuit.

The CW pitch control shifts the 4th IF passband in the demodulator circuit while, at the same time, raising or lowering the pitch of the audible beat frequency. This is very useful in avoiding interference or for changing the pitch tone to a frequency that is easier to copy.

Dual-Mode Noise Blanker ("Pulse" or "Woodpecker".)

The noise blanker consists of two circuits, NB-1 and NB-2, each actuated by its own front panel switch. The NB level control adjusts the threshold level of the noise amplifier, allowing the operator to control the effectiveness of the noise blanker under the specific noise and signal level conditions. Depressing the "NB1" switch is most effective in suppressing pulse-type (ignition) noise. Depressing the

NB2 switch is most effective in suppressing noise of a longer duty cycle nature, such as the so-called "woodpecker" type of interference. The threshold level in the NB2 position is factory optimized for maximum effectiveness with minimum degradation of the desired signal. The noise blanker circuitry is also used to suppress "clicks" sometimes introduced by the step reset pulse of the digital VFO's.

Built-in RIT/XIT.

The front panel "RIT" (Receiver Incremental Tuning)/"XIT" (Transmitter Incremental Tuning) control shifts the receive or transmit frequency in 10 Hz steps across a range of ±9.99 kHz, using an optical encoder, to tune sations that are slightly off frequency, without affecting the VFO transmit/ receive frequency. RIT/XIT frequency shifts are displayed in the main display area. A "CLEAR" switch resets the RIT/XIT frequency to zero. The "RIT/XIT" control may be used in any mode of operation.

All-Mode Squelch Circuit.

The squelch circuit is effective in suppressing background noise in all operating modes during key-up intervals.

RF Attenuator.

The meticulously engineered receiver section front end includes a 4-step, (0, 10, 20 or 30 dB) RF attenuator, for optimum rejection of intermodulation distortion.

Switchable AGC Circuit (OFF/FAST/SLOW).

The automatic gain control (AGC) is activated by a 3-position (OFF/FAST/SLOW) switch, to provide optimum receiver operation in all modes of operation, and under all signal strength conditions.

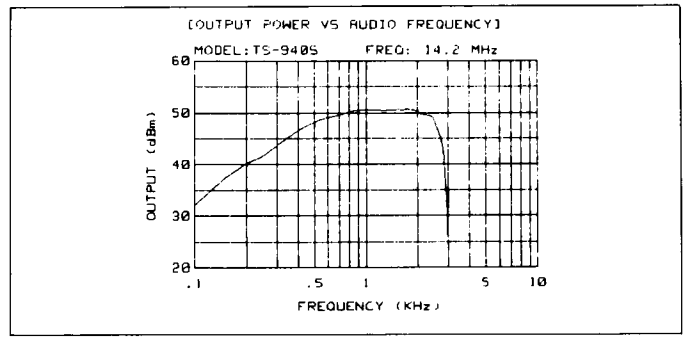
AUTOMATIC ANTENNA TUNER PLUS LOW DISTORTION, HIGH RELIABILITY TRANSMISSION.

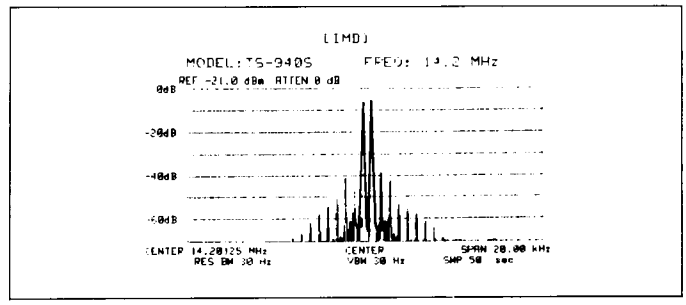
Automatic Antenna Tuner (160-10 meters) Built-in.

The TS-940S is available with a completely automatic antenna tuner covering all Amateur bands from 160 through 10 meters built-in, or may be ordered without the tuner installed. The AT-940 antenna tuner is available for future installation in transceivers initially ordered without the automatic antenna tuner.

Low Distortion, High Reliability 28 Volt Powered Final Amplifier.

Through the use of a 28 volt power source, the quality of the transmitted signal has been measurably improved (3rd order intermodulation distortion less than −37 dB) compared to other contemporary designs. Temperature and VSWR monitoring circuits are incorporated in the final amplifier protection circuit to guard against failure of these important components. Continuous operation in the CW or RTTY modes of operation is possible, due to the oversize heatsink design coupled with the new, super-quiet, ducted cooling system with two speed fans.





CW Full Break-in.

A full break-in capability allows the DX or contest operator to respond more quickly to the calling station. To the "ragchewer", it means a more natural conversation. This capability is made possible through use of CMOS IC's in the timing logic circuitry. The actual switching is accomplished using a specially constructed, fast-acting reed-type relay, which also serves to eliminate the distracting sounds typical of a conventional relay. A front panel switch permits switching to semi break-in operation.

Built-in Speech Processor.

The TS-940S employs speech processing circuitry based on RF clipping techniques. A marked improvement in the intelligibility threshold is attainable, depending on the positions of separate front panel "IN" and "OUT" controls. A higher average "talkpower" plus the improved intelligibility makes for outstanding DX performance.

RF Output Power Control.

Using a front panel control, the RF output power may be continuously varied from 10 watts to the maximum power, in any mode of operation.

OPERATING FREQUENCY CONTROL USING NEW MICROPROCESSOR PLUS DIGITAL TECHNOLOGY.

The use of a new microprocessor plus advanced digital technology to control the various tuning functions, including the 2 digital VFO's, the 40 channels of memory, band scan and memory scan, etc., assure maximum flexibility and ease of operation under the most difficult operating conditions.

10 Hz Step Dual Digital VFO's with Optical Encoder.

Special tuning logic, working in conjunction with the basic 10 Hz step, high stability digital VFO design, provides a variable speed tuning characteristic that is directly related to the speed of tuning knob rotation. A large, die-cast tuning knob with molded rubber cover, rotated at normal tuning speeds, results in frequency shift in 10 Hz increments, or 10 kHz per tuning knob revolution. Rotation of the tuning control at speeds in excess of approximately 2 to 3 revolutions per second causes the tuning step size to be increased proportionally, speeding up the rate of frequency change. Each VFO tunes continuously across the full coverage of the transceiver, utilizing the KENWOOD engineered special optical encoder tuning system.

Built-in Dual VFO A/B Switching System.

An "A/B" switch allows the operator to specify the VFO to be used. A "SPLIT" switch is available for split frequency operations. An "A=B" switch makes it possible to quickly duplicate the tuning data (frequency, mode, RIT data) programmed into the active VFO, in the data banks of the inactive VFO. A "T-F SET" switch is provided to permit reversal of the transmit and receive frequencies during split frequency operations. All of these switches are front panel mounted.

40 Memory Channels.

The 40 memory channels are divided into 4 groups of 10 channels each, for operating purposes. Both mode and frequency data are stored, making all operations simple and convenient. The operator may select any 1 of the 4 memory groups for operations, using the 4 position memory bank switch located on the top panel. Depressing the "VFO/M" switch on the front panel permits selection of the memory channel, using the 10 band keys. The "M VFO" switch is used to transfer memory data (frequency, mode) to the active VFO. Memory information is backed-up by an internal lithium battery. (Est. 5 yr. life.)

Built-in Scan Functions.

Memory scan is initiated by depressing the "MS" switch. Memories in which no data is stored are skipped. Programmable band scan is initiated by depressing the "PG.S" switch, and scans in 10 Hz (100 Hz in AM, FM modes) steps from the lowest frequency within the frequency limits specified in memory channels "9" and "0". A "HOLD" switch is provided to interrupt the scanning process during memory and program scan operations. When the "HOLD" switch has been depressed during program scan, the VFO operating frequency may be adjusted within the frequency limits established in memory channels "9" and "0".

Rapid Band Selection.

The specific Amateur band may be quickly selected by depressing the appropriate front panel band key. 1-MHz step "UP" and "DOWN" switches on the front panel or on the microphone allow rapid selection of tuning frequency for general coverage. An "F.LOCK" switch prevents accidental loss of the selected frequency.

Keyboard Frequency Selection

The VFO frequency may be directly entered using the front panel number keys. Simply press the "ENT" key, followed by the desired frequency.

MULTI-FUNCTION MAIN DISPLAY AND SUB-DISPLAY.

The TS-940S incorporates a large fluorescent tube digital display with a unique analog-type sub-scale, plus a new dot-matrix LCD sub-display that displays alpha-numeric information and graphic characteristics.

Large Fluorescent Tube Digital Main Display.

The large, built-in, multi-function fluorescent tube display and its analog-type sub-scale provides improved readability and allows increased operating ease. Transmit/receive frequencies appear on a 7 numeral digital display/analog sub-scale combination, indicating tuning across a selected 1 MHz/100 kHz band segment in 20 kHz/2 kHz steps. A red indicator on the analog scale keeps pace with the tuning knob rotation. A separate 2-digit display indicates RIT/XIT frequency shift to ±9.99 kHz. There are also indicators for VFO "A" or "B", memory "ON", memory channel number, "F.LOCK", and RIT/XIT "ON". The use of the fluorescent tube display makes reading easy, and minimizes eye fatigue. A "DIM" switch has been provided to allow dimming the display and the meter illumination, if desired.

LCD Dot-matrix Sub-display.

The sub-display is capable of displaying a maximum of 16 digits and 2 lines of data. Frequency, graphic characteristics, messages, and clock time are the 4 different kinds of information that can be displayed.

■ **Frequency.**
The upper line shows frequency and mode of VFO "B" when VFO "A" is indicated on the main display. The lower line indicates memory group (1~4), memory channel (CH-1, 2, ... 9, 0), plus frequency and mode during VFO operations.

■ **Graphic Characteristics.**
Graphically indicates the effect on bandwidth when "SSB SLOPE TUNE" or "CW VBT" controls are operated.

■ **Messages.**
Displays messages relating to operation of the Automatic Antenna Tuner, as follows:

1. "ANTENNA TUNER AUTO TUNE READY" when "AT.T" switch is depressed.
2. "ANTENNA TUNER TUNING" when the transmitter is keyed within 3 seconds after pressing "AT.T" switch.

3. "TUNING FINISHED TX-READY" when automatic antenna tuner has finished tuning.

■ **Clock.**

Indicates the current time, or the preset timer time.

The clock has a built-in battery back up. (Est. 3 yr. life)

MECHANICAL DESIGN AND CONSTRUCTION TYPICAL OF COMPETITION-CLASS EQUIPMENT.

Rugged Zinc Die-cast Front Panel and VFO Control Knob.

The Zinc die-cast front panel assures maximum mechanical stability under even the most severe operating conditions. The large die-cast VFO control knob, with a textured rubber cover provides a positive tuning "feel" coupled with a strong flywheel effect, further enhancing the unit's flexibility of use and ease of operation.

New Highly Efficient Cooling System.

The 100 W final amplifier stage is mounted directly on its die-cast aluminum heat sink, providing maximum thermal conduction efficiency.The high efficiency of the cooling system permits continuous transmission at full power for periods of exceeding one hour without thermal shut-down. The power supply unit has its own independent cooling system.

A VARIETY OF EXTRA, EASY-TO-OPERATE FUNCTIONS.

Built-in AC Power Supply and Speaker.

The TS-940S is a self-contained HF station, including a built-in power supply, and a rugged, top-mounted, high quality, 10 cm (4 inch) speaker. The power supply circuit provides ample capacity thru the use of a special, compact, laminated core transformer, assuring maximum stability of operation in the final transistor circuits. The correct AC circuit polarity is achieved through use of the 3-wire connector and cable assembly supplied with the unit.

Clock/Timer Function.

In addition to a 24-hour clock function, a single event timer is provided for scheduled un-attended recording of a specified transmission. Clock/Timer program data may be displayed on the LCD sub-display at the operator's option.

Transmission Monitor Circuit.

A built-in transmit monitor circuit operating in the SSB, FM, and FSK modes may be operator activated by depressing the front panel "MONI" switch. This circuit monitors the product detector signal from the output of the IF section during transmission, allowing the operator to check his audio quality, and the effectiveness of the speech processor.

High Stability RTTY Transmit Circuit.

The stability of RTTY transmissions is greatly improved through design that obtains the FSK signal information from the reference oscillator. The FSK shift width is 170 Hz.

Optional SO-1 TCXO.

An optional high stability temperature compensated crystal oscillator may be installed in place of the reference oscillator. This unit operates at 20 MHz with an accuracy of 0.5 ppm between −10 degrees Celsius and +50 degrees Celsius, upgrading the transceiver to a level challenging professional standards.

Voice Synthesizer Unit (Optional).

An optional VS-1 "Voice Synthesizer Unit", which announces the operating frequency on demand by depression of the front panel "VOICE" key, is available. Installation within the cabinet is simple and easy.

ADDITIONAL FEATURES, PLUS ACCESSORY TERMINALS.

Dimmer Switch.

A front panel "DIM" switch permits selection of either normal or reduced intensity on the digital display and SWR/POWER meter.

100-kHz Marker.

A 100 kHz marker signal, controlled by a switch located under the sliding panel on top of the unit, is available for use in calibrating the fundamental oscillator against received standards such as WWV or MSF.

VOX Circuit.

The VOX gain, VOX delay, and Anti-VOX controls are located beneath the sliding panel on the top of the cabinet.

Meter Transmission Functions.

"COMP" (Compression), "ALC" (Automatic Level Control), "POWER" (RF Output Power), "SWR" (Standing-wave Ratio), "IC" (Final Amplifier Collector Current), and "VC" (Final Amplifier Collector Voltage.) 5 units and dB on receive.

LED Indicators for Miscellaneous Functions.

"ON AIR", "AT", "TUNE", "SPLIT", "NOTCH", "NAR".

Input/Output Terminals.

Receiver antenna terminal and switch, transverter terminal, IF OUT 1 (For PAN-DISPLAY) and IF OUT 2 (Oscilloscope Modulation Monitor) terminals, phone patch IN/OUT terminals, accessory terminals 1 and 2, remote control terminal.

Frequency configuration

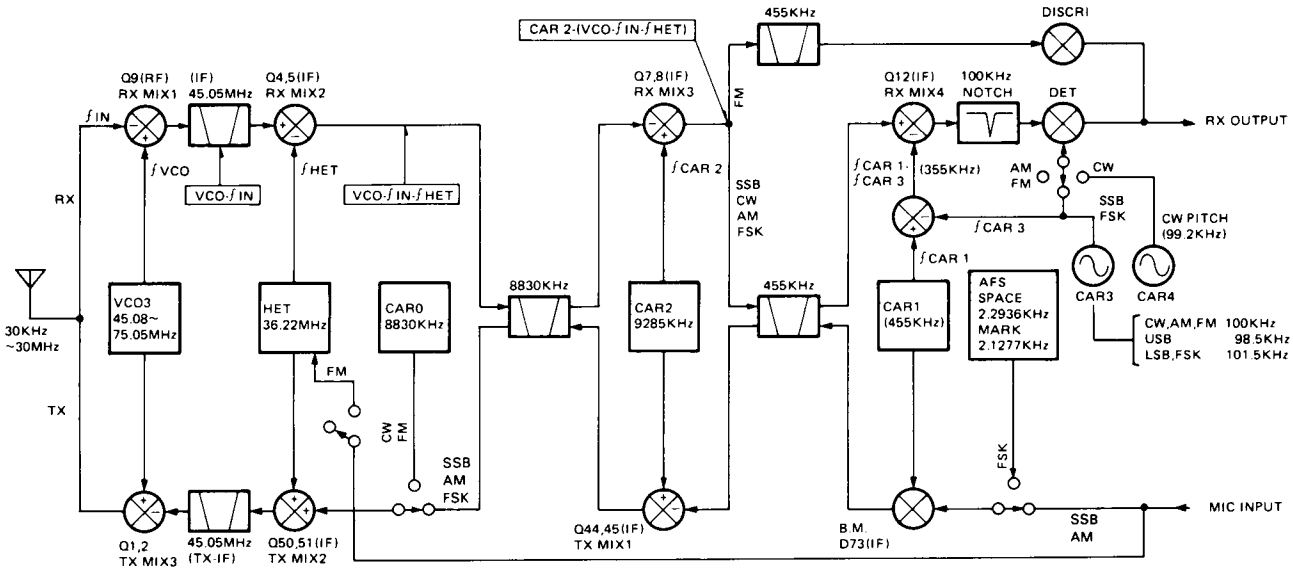


Fig.-1 The frequeny configuration of signal channels

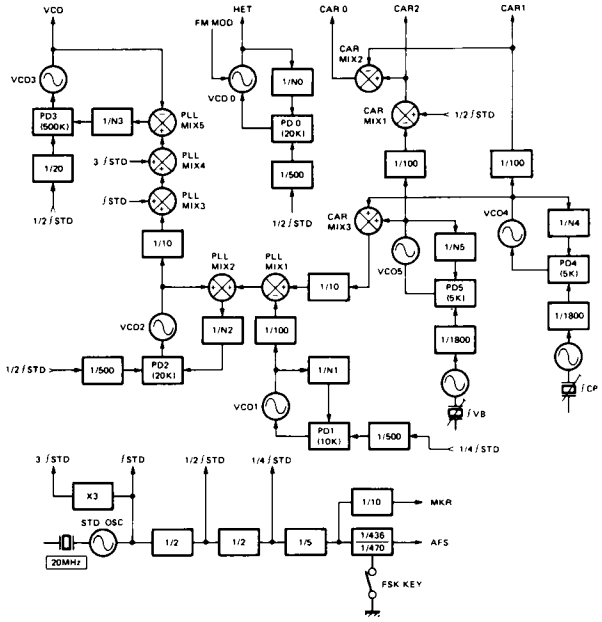


Fig.-2 PLL channel

The TS-940S is quadruple conversion in SSB, CW, AM and FSK modes and triple conversion in FM mode. As a transmitter, it is double conversion in CW and FM modes and triple conversion in SSB, AM and FSK modes.

Fig. 1 shows the frequency configuration of the signal channels as both a transmitter and a receiver. The receiver frequency in SSB mode will be described now. It is assumed that the input frequency entered from the antenna is f_{IN} the local oscillator input of RX MIX1 is f_{VCC} the local oscillator input of RX MIX2 is f_{HET} the local oscillator input of RX MIX3 is f_{CAR2} and the local oscillator input of RX MIX4 is $f_{CAR1} - f_{CAR3}$.

When the receiver output tone frequency by f_{IN} is zero beat (namely, at zero to the SSB signal with a carrier point of f_{IN}), the relationship between these signals is expressed by the following equation:

$$\underbrace{\underbrace{\underbrace{[f_{CAR2} - \{(f_{VCO} - f_{IN}) - f_{HET}\}]}_{MIX1} - (f_{CAR1} - f_{CAR3})}_{MIX2} = f_{CAR3}}_{MIX3}$$

MIX4

The equation is arranged as follows:

$$f_{IN} = f_{VCO} - f_{HET} + f_{CAR1} - f_{CAR2} \quad \ldots\ldots (1)$$

The term f_{CAR3} is eliminated as it is not related to the receiver frequency itself. As for the remaining terms, all are generated in the PLL (Phase Locked Loop) circuit in the configuration shown in **Fig. 2**. The frequencies generated are now examined for each loop.

In VCO_0

$$\frac{f_{VCO0}}{N_0} = \frac{\frac{1}{2} \cdot f_{STD}}{500}$$

$$\therefore f_{VCO0} = \frac{N_0}{1000} \cdot f_{STD} \quad \ldots\ldots (2)$$

In VCO_1

$$\frac{f_{VCO1}}{N1} = \frac{\frac{1}{4} \cdot f_{STD}}{500}$$

$$\therefore f_{VCO1} = \frac{N1}{2000} \cdot f_{STD} \quad \ldots\ldots (3)$$

In VCO_2

$$\frac{f_{VCO2} + \frac{f_{VCO4} + f_{VCO5}}{10} - \frac{f_{VCO1}}{100}}{N2} = \frac{\frac{1}{2} \cdot f_{STD}}{500}$$

$$\therefore f_{VCO2} = \frac{N_2}{1000} \cdot f_{STD} + \frac{f_{VCO1}}{100} - \frac{f_{VCO4}}{10} - \frac{f_{VCO5}}{10} \quad \ldots\ldots (4)$$

In VCO_3 $\dfrac{\frac{f_{VCO2}}{10}+f_{STD}+3\cdot f_{STD}-f_{VCO3}}{N3}=\dfrac{\frac{1}{2}f_{STD}}{20}$

$$\therefore f_{VCO3}=\frac{160-N_3}{40}\cdot f_{STD}+\frac{f_{VCO2}}{10} \quad \cdots\cdots (5)$$

In VCO_4 $\dfrac{f_{VCO4}}{N_4}=\dfrac{f_{CP}}{1800}$ $\therefore f_{VCO4}=\dfrac{N_4}{1800}\cdot f_{CP}$ $\cdots\cdots (6)$

In VCO_5 $\dfrac{f_{VCO5}}{N_5}=\dfrac{f_{VB}}{1800}$ $\therefore f_{VCO5}=\dfrac{N_5}{1800}\cdot f_{VB}$ $\cdots\cdots (7)$

The above equations are thusly arranged so the frequencies of each local oscillator are expressed as follows.

$$f_{VCO}=\left(\frac{160-N_3}{40}+\frac{N_2}{10000}+\frac{N_1}{2000000}\right)\cdot f_{STD}$$
$$-\frac{N_4}{180000}\cdot f_{CP}-\frac{N_5}{180000}\cdot f_{VB} \quad \cdots\cdots (8)$$

$$f_{HET}=f_{VCO0}=\frac{N_0}{1000}\cdot f_{STD} \quad \cdots\cdots (9)$$

$$f_{CAR1}=\frac{1}{100}f_{VCO4}=\frac{N_4}{180000}\cdot f_{CP} \quad \cdots\cdots (10)$$

$$f_{CAR2}=\frac{1}{2}f_{STD}-\frac{1}{100}f_{VCO5}=\frac{1}{2}\cdot f_{STD}-\frac{N_5}{180000}\cdot f_{VB} \quad \cdots (11)$$

$$f_{CAR0}=f_{CAR2}-f_{CAR1}=\frac{1}{2}\cdot f_{STD}-\frac{N_5}{180000}\cdot f_{VB}-\frac{N_4}{180000}\cdot f_{CP} \quad (12)$$

Therefore, the term "f_{IN}" of equation (1) is re-written as follows.

$$f_{IN}=\left(\frac{160-N_3}{40}+\frac{N_2}{10000}+\frac{N_1}{2000000}-\frac{N_0}{1000}\right)\cdot f_{STD} \quad \cdots\cdots (13)$$

As shown in equation (13), the receiver frequency is determined only by the reference f_{STD} and the dividing ratio NO-N3. This shows the following.

1. N is the numeric value determined by the microprocessor in accordance with the operating frequency and, essentially, it does not include the error component.
2. With the primary term of f_{STD} only, the reference frequency accuracy is directly considered as an operating frequency accuracy.
3. The operating frequency does not change even if N4, N5, f_{CP} and f_{VB} change.

The accuracy of the reference crystal oscillator used in the TS-940S is 10PPM (−10~+50°C). It is 0.5PPM (−10~+50°C) when the optional TCXO (Temperature Compensated Crystal Oscillator) SO-1 is used.

According to 1 and 2, the overall accuracy of the TS-940S is highly stable with the same value as described above obtainable at any point in the 30 kHz~30 MHz range. Utilizing the characteristic of 3 above, the TS-940S has variable band width functions such as VBT and slope turning controlled by the microprocessor, which operates N4 and N5. At the same time, the TS-940S sets the carrier point by making fine adjustment of f_{CP} and adjusts the initial setting of VBT by making fine adjustment of f_{VB}. The receiver frequency in SSB mode has been described. In other modes or when used as a transmitter, likewise, the frequency is determined by the reference f_{STD} and dividing ratio.

The display frequencies are shown in the following table.:

USB, LSB	Carrier point frequency
CW	Transmission carrier frequency
AM, FM	IF filter center frequency
FSK	Space transmitter frequency

Table-1, Display frequencies in each mode

In CW mode, the TS-940S receiving pitch can be changed to the required frequency while the desired signal remains in the center of the IF filter passband. (Variable CW pitch system)

The receiving pitch varies with the transmitter CW side tone. It is thus possible to immediately zerobeat by receiving the desired signal at the same pitch as the side tone. FSK transmission is executed in LSB mode. The audio signal made by dividing the reference frequency

(Space $=\frac{f_{STD}}{8720}=2.2936$ kHz, mark $=\frac{1}{9400}=2.1277$ kHz)

is used as the AFSK (Audio Frequency Shift Keying) signal.

In FSK mode, unlike the operation is LSB mode, the IF is shifted (the dividing frequency N4 is shifted) for both transmission and reception so that the signal at 2.2936 kHz/2.1277 kHz passes through the center of the IF filter. The f_{VCO1} is shifted, since the display frequency is the space transmitter frequency. (The dividing ratio N1 is shifted.)

FM transmission is obtained in this system by modulating the f_{HET} by applying the audio signal from the microphone to the VCO_0.

The specifications of each frequency element are as follows.

f_{STD} 20 MHz — Standard: ±10 PPM (−10°C~+50°C) max.
SO-1 mounted: ±0.5 PPM (−10°C~+50°C) max.

f_{CP} 9 MHz±△CP — △CP = Carrier point adjustment component

f_{VB} 9 MHz±△VB — △VB = VBT initial setting adjustment component

Dividing ratio

N_0 1811

N_1 10000~10999 — Applicable to the display frequency 0.00 kHz~9.99 kHz. +229 added in FSK mode.

N_2 2310~2555 — Applicable to the display frequencies 000.00~490.00 kHz and 500.00~990.00 kHz. (Only the integer multiple of 5 is used)

N_3 77~17 — Applicable to every multiple of 500 kHz of 30 kHz~30 MHz

N_4 9100 + (Mode shift) ±△4 — △4 = Variable band

USB	−30	AM-W, N	0
LSB	+30	FM	0
CW-W	−14	FSK-W, N	+44
CW-N	0		

N_5 14300±△5 — △5 = Variable band

CIRCUIT DESCRIPTION

Local oscillator

PLL Circuit

This is a digital VFO (Variable Frequency Oscillator) to cover a frequency range of from 45.08 MHz~75.05 MHz in 10 Hz steps, in accordance with the TS-940S operating frequency of 150 kHz~30 MHz. Three PLL loops are linked in analog mode. The dividing ratio data to each PLL is controlled by the microprocessor.

Each loop is of a single crystal frequency control system: the VCO phase is compared with the unique reference frequency f_{STD} ·CAR1 and CAR2 frequencies are inserted halfway in the analog link, enabling variable bandwidth functions such as VBT and slope tuning.

Operation of the PLL circuit is explained with reference to **Fig. 3** "PLL block diagram".

The PLL-1 consists mainly of IC9: MN6147. VCO1 of Q12: 2SC2668 is locked in the 100~109.99 MHz range. The 1/4 f_{STD} (5 MHz) signal is supplied from the reference signal generator to IC9, where it is divided to 1/500 and output as a 10 kHz comparison frequency.

The VCO1 output is applied to the same IC9 via buffer amplifier Q11, where it is divided to 1/N1. The signal is then coupled to the phase comparator, where it is compared with the above 10 kHz signal, and the output locks VCO1 in 10 kHz steps.

As N1, the 1000 steps (10000~10999) of dividing data equivalent to the low order 9.99 kHz width of the operation frequency is sent from the digial A unit to the PLL unit as a 4 bit serial data stream. A microprocessor is used for this data sending operation (DA0—DA3, CK1). In FSK mode, as the space frequency is used as an operating frequency, N1 is shifted to 10229~11228.

The PLL-1 output is divided to 1/100 by IC10: M54459L and becomes a signal of 1 MHz~1.0999 MHz (1.0229~1.1228 MHz in FSK mode) in 100 Hz steps. This signal sent from the PLL-1 channel to IC6: SN16913P, i.e., the signal sent from the PLL-1 channel to IC6 is:

$$\frac{f_{VCO1}}{100}=\frac{1}{100}\times\frac{N_1}{500}\times\frac{1}{4}\cdot f_{STD}=\frac{N_1}{200000}\cdot f_{STD} \quad \ldots\ldots (1)$$

On the other hand, the $f_{VCO4}+f_{VCO5}$ signal (approx. 117 MHz) is sent from the carrier unit to PLL unit. This signal is divided to 1/10 by IC5: HD10551 and applied to the mixer IC6. This signal is expressed by the equation:

$$\frac{1}{10}\cdot(f_{VCO4}+f_{VCO5})=\frac{1}{10}\left\{100\cdot f_{CAR1}+100\left(\frac{1}{2}f_{STD}-f_{CAR2}\right)\right\}$$

$$=5\cdot f_{STD}+10f_{CAR1}-10f_{CAR2} \quad \ldots\ldots (2)$$

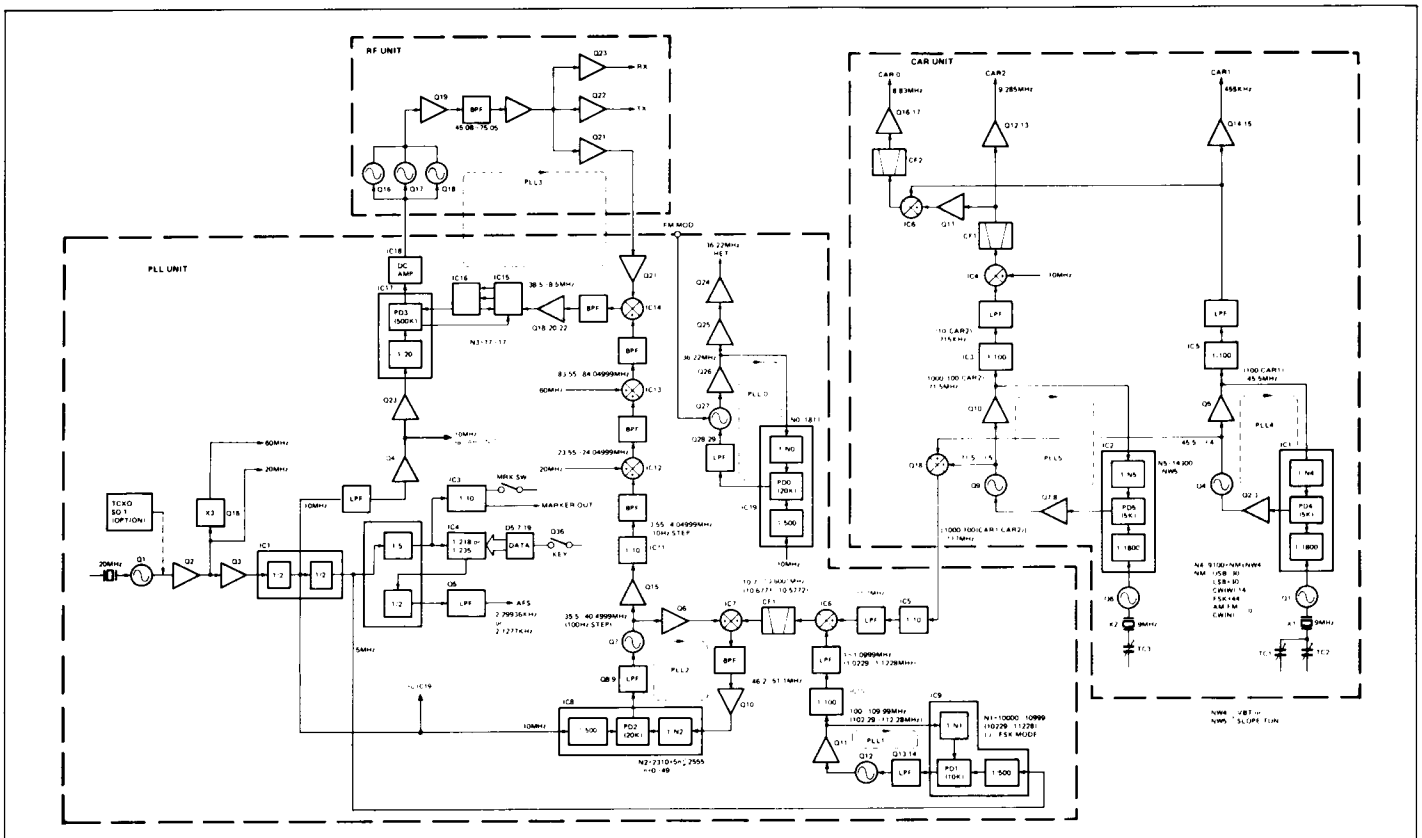


Fig.-3 PLL block diagram

It becomes a signal of approx. 11.7 MHz. Therefore, IC6 output becomes a signal of approx. 10.65 MHz expressed by:

$$5f_{STD}+10f_{CAR1}-10f_{CAR2}-\frac{N_1}{200000}\cdot f_{STD} \quad \ldots\ldots (3)$$

Any mixer spurious signal is eliminated by ceramic filter CF1: SFJ10.7MA-D and applied to the next PLL-2 loop. PLL-2 consists mainly of IC8: MN6147, which locks the output signal of mixer IC7: SN16913P, which is the VCO2 output of Q7: 2SC2668 and the signal from CF1, in the range of 46.2~51.1 MHz. The 1/2 f_{STD} (10 MHz) signal is supplied from the reference frequency generator to IC8, where it is divided to 1/500 to make a comparison frequency of 20 kHz. The VCO2 output is applied to mixer IC7 via buffer amplifier Q6: 2SC2668 and added to the signal (the configuration of equation (3) = 10.65 MHz) from CF1, and this output is sent to IC8 via a BPF (Band Pass Filter) and amplifier Q10: 2SC2668.

This signal is divided to 1/N2, compared in phase with the above 20 kHz signal and used to control VCO2. This operation is expressed by:

$$\left(f_{VCO2}+5f_{STD}+10f_{CAR1}-10f_{CAR2}-\frac{N_1}{200000}\cdot f_{STD}\right)\times\frac{1}{N_2}$$

$$=\frac{1}{500}\times\frac{1}{2}\cdot f_{STD} \quad \ldots\ldots (4)$$

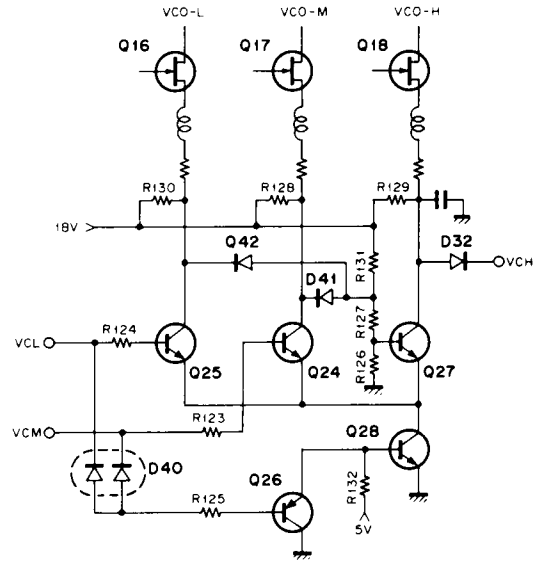
N2 means to cover the low order 500 kHz width of the operating frequency in 10 kHz steps and takes a numeric value of 50 steps which becomes an integer multiple of 5 in the range 2310~2555. Like N1 in PLL-1, this data is sent by the microproceesor from the digital A unit to the PLL unit as a 4 bit serial data stream. (DA0—DA3, CK2). Therefore, the output signal of PLL-2 is expressed by the equation:

$$f_{VCO2}=\left(\frac{N_1}{200000}+\frac{N_2}{1000}-5\right)f_{STD}-10f_{CAR1}+10f_{CAR2} \ldots (5)$$

According to the values of N1 and N2, a frequency of 35.5~40.4999 MHz is generated in 100 Hz steps. The PLL-2 output is divided to 1/10 by IC11: HD10551 via buffer amplifier Q15: 2SC2668, and becomes a signal in 10 Hz steps in the 3.55~4.04999 MHz range.

First, f_{STD} (20 MHz) is added in mixer IC12: SN16913P and then, 3.f_{STD} (80 MHz) is added in mixer IC13: SN16913P and the signal is converted to 83.55~84.04999 MHz. As a result, 4.f_{STD} (80 MHz) is added, but such a frequency configuration is employed in order to avoid unwanted mixer spurious components. This signal is applied to mixer IC14, where it is mixed with the final VCO output signal.

The final VCO is located on the RF unit and consists of three elements: Q16 : 2SK192A handling the frequency below 9.5 MHz, Q17: 2SK192A for 9.5~19.5 MHz and Q18: 2SK192A for 19.5 MHz~30 MHz. Each VCO is selected by the VCO select information (VCM or VCL, VCH is derived) sent from the Digital A unit by the microprocessor. The VCO selector circuit is shown in Fig. 4.



Freq' (Hz)	VCO selected data VCM	VCL	Q25	Q24	Q27	VCO freq' (MHz)	VCH
30k~9.5M	L	H	○	X	X	45.08~54.55	H
9.5M~19.5M	H	L	X	○	X	54.55~64.55	H
19.5~30M	L	L	X	X	○	64.55~75.05	L

○ ON X CUT OFF

Fig.-4 VCO selector circuit

The oscillator output runs through the buffer amplifier Q19: 2SC1907 and the high frequency component is eliminated by a BPF. The signal runs through the buffer amplifier Q20: 2SC1907 and is then separated into three channels of buffered output. The Q21: 2SC2668 output is supplied to the PLL unit, composing a final PLL loop. The Q22: 2SC1907 output is applied to the third transmitter mixer. From Q23: 2SC1907, the VCO output is applied to the first receiver mixer via amplifier Q6: 2SC2053.

The signal from the RF unit, final VCO is connected to the PLL unit VCO terminal and is applied to mixer IC14 via buffer amplifier Q21: 2SC2668. Therefore, the mixer output becomes:

$$\frac{f_{VCO2}}{10}+f_{STD}+3f_{STD}-f_{VCO}$$

$$=\left(\frac{N_1}{2000000}+\frac{N_2}{10000}+\frac{7}{2}\right)f_{STD}-f_{CAR1}+f_{CAR2}-f_{VCO} \ldots (6)$$

This signal goes through a BPF and is amplified by Q18, 19: 2SC2668, Q20: 2SC1907 and Q22: 2SC2668 and then, the waveform is shaped by IC15-1/3: SN74S10N and applied to 1/3 or 1/4 prescaler IC16: SN74S112N. IC16 is originally a dual function flip-flop circuit and works as a 1/4 divider, but its function is changed to a 1/3 divides by the control signal from the later stage PLL IC17: MC145158, i.e., a pulse swallow divider is composed of IC17 internal divider, IC16 and IC15-1/3.

PLL IC17, the primary element of the final PLL loop PLL-3, is provided with the modulus control function which externally sets both the reference dividing ratio and comparison dividing ratio by serial data, and composes a pulse swallow counter using an external prescaler.

The 1/2 f_{STD} (10 MHz) signal is supplied from the reference frequency generator to IC16 via buffer amplifier Q23: 2SC2668. The signal is divided to 1/2 in IC16 to make a comparison output frequency of 500 kHz.
The signal supplied from IC14 to the swallow counter via the BPF and amplifier is divided to 1/N3 and compared in phase with the 500 kHz signal in the phase comparator. This controls the RF unit final VCO by the error correction voltage.
The operation is expressed by:

$$\left\{\left(\frac{N_1}{2000000}+\frac{N_2}{10000}+\frac{7}{2}\right)f_{STD}-f_{CAR1}+f_{CAR2}-f_{VCO}\right\}\times\frac{1}{N_3}=\frac{1}{20}\times\frac{1}{2}f_{STD} \quad \ldots (7)$$

N3 means to cover the overall operating frequency range (30 kHz—30 MHz) in 500 kHz steps and becomes 60 steps of 77—17. This data is also sent by the microprocessor from the Digital A unit to the PLL unit as serial data. (PLD, PLE and CK3)
As a result, the final VCO output signal is expressed by:

$$f_{VCO}=\left(\frac{160-N_3}{40}+\frac{N_2}{10000}+\frac{N_1}{2000000}\right)\cdot f_{STD}-f_{CAR1}+f_{CAR2} \quad . \quad (8)$$

According to the values of N1, N2 and N3, a frequency of 45.08—75.05 MHz is generated in 10 Hz steps. If f_{CAR1} is expressed by N4 and f_{CP} and f_{CAR2} by N5, f_{VB} and f_{STD}' respectively, equation (8) becomes the same as equation (8) provided in "Frequency Configuration".

• HET (Heterodyne Oscillator)

The HET oscillator is provided in the PLL unit, which is a PLL circuit (PLL-0) to generate a constant frequency signal of 36.22 MHz. This output signal is connected to the IF unit and supplies the second transmitter/receiver mixer. In FM transmission mode, the audio signal from the microphone is applied to this PLL to yield FM modulation.

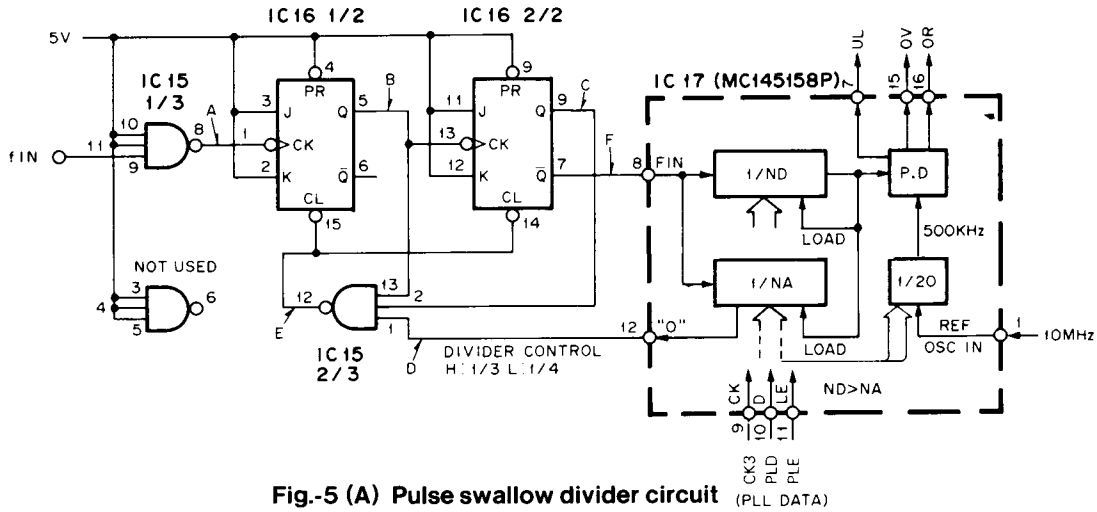


Fig.-5 (A) Pulse swallow divider circuit

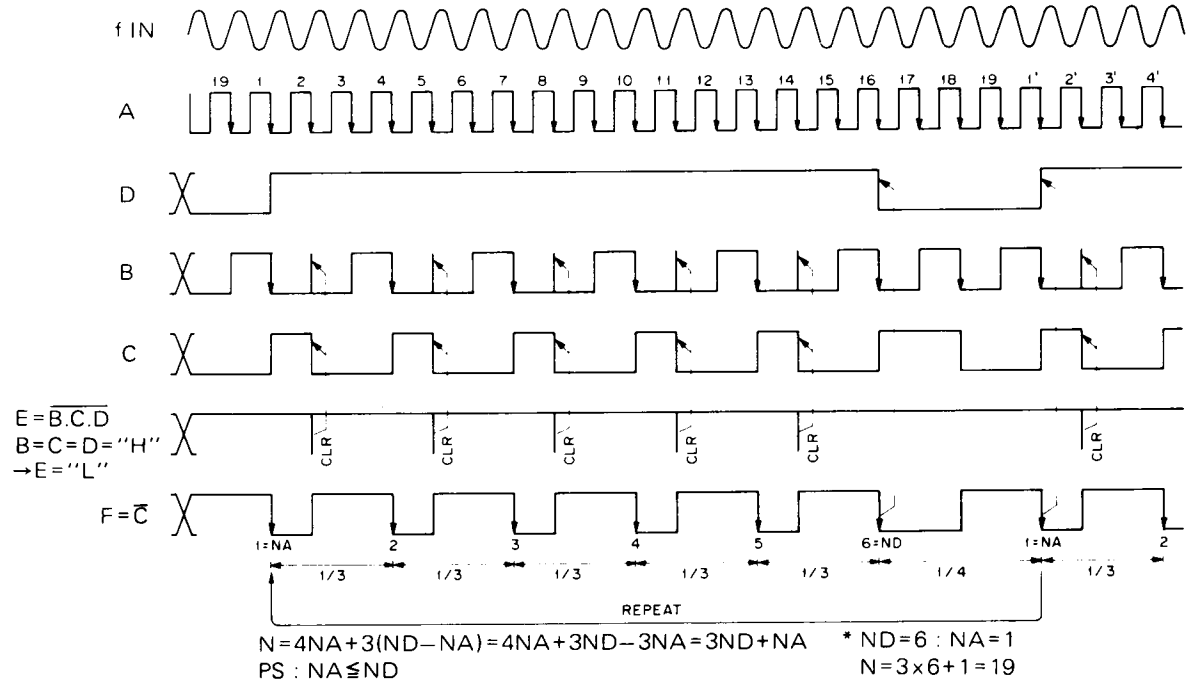


Fig.-5 (B) Pulse swallow divider timing chart

PLL-0 consists mainly of IC19. VCO_0 is Q29: 2SK192A, locked to 36.22 MHz. A signal of 1/2 f_{STD} (10 MHz) is supplied from the reference frequency generator to IC19, where it is divided to 1/500 to make a 20 kHz comparison output frequency.
The oscillator output of VCO_0 is applied to IC19 via buffer amplifier Q26: 2SC2668 and divided to 1/N0 (1/1811 constant) and the output is phase compared with the 20 kHz reference signal in the phase comparator. This is used to lock the fequency of VCO_0. N0 (1811) is sent from the Digital A unit to the PLL unit. The PLL-0 output is sent to the IF unit via buffer amplifiers Q25: 2SC2668 and Q24: 2SC1907 and an LPF (Low Pass Filter).

• CAR1

The CAR1 generator is provided in the digital B (CAR) unit, which makes a signal of approx. 45.5 MHz on the basis of the 9 MHz crystal oscillator and divides it to 1/100 in the PLL-4 circuit to generate a 455 kHz signal. This signal is sent to the IF unit and mixed with the CAR3 signal to becomes a 355 kHz signal. This is sent to the fourth receiver mixer in reception mode. In transmission mode, the signal is sent to the balanced modulator to generate a 455 kHz DSB (Double Side Band) signal.
PLL-4 consists mainly of IC1: MN6147. VCO4 (Q4: 2SC2668) is locked to approx. 45.5 MHz. A 9 MHz signal is supplied from the f_{CP} oscillator Q1: 2SC2787 to IC1 and divided to 1/1800 to make a 5 kHz comparison output frequency. VCO4 output is applied to IC1 via buffer amplifier Q5: 2SC2668 and divided to 1/N4, and the output is phase compared with the 5 kHz signal and is then used to lock VCO4 in 5 kHz steps. The output signal from PLL4 is divided to 1/100 by IC5: M54459L to become a signal of approx. 455 kHz in 50 Hz steps. This passes through the LPF and is supplied from output buffer Q14/Q15: 2SC2458 to the IF unit as the CAR1 signal.
The non-divided 45.5 MHz signal is applied to the mixer Q18: 3SK73, where the PLL-5 output (the base of CAR2 signal) is added to the signal, and the output is sent to the PLL unit to form a part of the digital VFO.
Thus, the operating frequency is not changed even if the CAR1 frequency is changed, i.e., f_{CP} and N4 are optional. When f_{CAR1} is changed, IF shift is effected in both transmission and reception modes. This characteristic is used to realize USB/LSB mode switching functions, variable bandwidth, fine adjustment of carrier point, centering CW/FSK signals in the IF bandpass, etc. Fine adjustment of carrier point is provided by trimmer capacitors TC1 (for USB) and TC2 (for LSB) connected to the f_{CP} crystal oscillator ×1. The other functions are executed by controlling N4 from the microprocessor. N4 is sent from the Digital A unit (a part of it is relayed by the PLL unit) as 4 bit serial data. (A0—A3, CL4).

• CAR2

The CAR2 circuit is provided in the digital B unit, which generates a signal of approximately 71.5 MHz on the basis of the 9 MHz crystal oscillator. This is divides to 1/100 in the PLL-5 circuit to generate a 9.285 MHz signal. This signal is sent to the IF unit and used as a local oscillation signal for the third receiver mixer in reception mode, and that of the first transmitter mixer in transmission mode.
PLL-5 consists mainly of IC2: MN6147.
A 9 MHz signal is supplied from the f_{VB} oscillator Q6: 2SC2787 to IC1 and divided to 1/1800 to make a 5 kHz comparison output frequency. The output of VCO5, Q9: 2SC2668 is applied to IC2 via buffer amplifier Q10: 2SC2668 and divided to 1/N5, and the output is compared in phase with the 5 kHz signal and used to lock VCO5 to approx. 71.5 MHz in 5 kHz steps. The PLL-5 output signal is divided to 1/100 by IC3: M54459L to become a signal of approx. 715 kHz in 50 Hz steps. It passes through a LPF and goes to IC4: SN16913P, where it is mixed with 1/2 f_{STD} (10 MHz) from the reference frequency generator to become the CAR2 signal at 9.285 MHz. Any mixer spurious components within this signal are eliminated by ceramic filter CF1. The filtered signal is applied to the IF unit via buffer amplifier Q12/Q13: 2SC2458. The 71.5 MHz output signal from PLL-5 is applied to mixer Q18, where the PLL-4 output signal (the basis of the CAR4 signal) is added to the signal, and the output is sent to the PLL unit to form a part of digital VFO. Thus, like CAR1, the operating frequency is not changed even if the CAR2 frequency is changed, i.e., f_{VB} and N5 are optional.
However, if the f_{CAR2} is changed, IF shift is effected across the 8.83 MHz filter (the second receiver IF filter) in both transmission and reception. (When the f_{CAR2} is changed, the 455 kHz filter is not shifted.) This characteristic is used to realize the variable bandwidth function.

Mode	Basic N4—Slope Tune/CW VBT	CAR1 frequency
USB	9070 → 9039	453.50 kHz → 451.95
LSB	9130 → 9161	456.50 → 458.05
CW-W	9086 → 9071	454.30 → 453.55
CW-N	9100 → 9093	455.00 → 454.65
AM-W	9100 → 9069	455.00 → 453.45
AM-N	9100 → 9085	455.00 → 454.25
FM	9100 → —	455.00 → —
FSK-W	9144 → 9173	457.20 → 458.75
FSK-N	9144 → 9151	457.20 → 457.55

Table-2 N4 Data Shift

Mode	Basic (units missing) N5—Slope Tune or CW VBT (max)	CAR2 frequency
USB	14300 → 14378	9285.00 kHz → 9281.10 kHz
LSB	14300 → 14222	9285.00 → 9288.90
CW-W	14300 → 14362	9285.00 → 9281.90
CW-N	14300 → 14315	9285.00 → 9284.25
AM-W	14300 → 14362	9285.00 → 9281.90
AM-N	14300 → 14330	9285.00 → 9283.50
FM	14300 → —	
FSK-W	14300 → 14238	9285.00 → 9288.10
FSK-N	14300 → 14285	9285.00 → 9285.75

Table-3 N5 Data Shift

Initialization of the VBT (Variable Bandwidth Tuning) adjustment (making the band center frequencies of the 8.83 MHz and 455 kHz filters the same) is performed by trimmer capacitor TC3 connected to the fVB crystal oscillator X2. The actual variable bandwidth function is realized by controlling N5 by the microprocessor. N5 is sent from the Digital A unit as A0—A3, and CL5 data.

• CARϕ

CAR0 is a signal of approx. 8.83 MHz, which is derived by subtracting CAR1 from CAR2 in mixer IC6 provided on the CAR unit. Any mixer spurious components generated by IC6: SN16913P are eliminated by ceramic filter CF2. The signal is then applied to both the IF and Control units via Q16: 2SC2787 and Q17: 2SC2458.
The signal applied to the IF unit is used as a transmission carrier in the CW and FM modes. The signal applied to the Control unit is used as the demodulation carrier for the monitor circuit in the SSB and FSK modes.

• CAR3

CAR3 on the IF unit generates three different frequencies depending on the mode (100 kHz = CW, AM and FM, 98.5 kHz = USB and 101.5 kHz = LSB and FSK.) These are used as the BFO (Beat Frequency Oscillator) in the SSB and FSK modes, as a side tone generating carrier in the CW mode, and as a local oscillators signal for the fourth receiver mixer after being mixed with the CAR1 signal.
In CAR3, the tuning capacitors for each mode are selected by diode switches D69 and D70. Q33: 3SK92A is the oscillator. The output is supplied from the CAR3 terminal to the side tone generator on the Control unit via buffer amplifier Q32: 2SC2458 and, at the same time, it is mixed with the CAR1 signal from CAR unit in mixer Q34: 3SK73 to generate a local oscillator signal ($f_{CAR1}-f_{CAR3}$) to be applied to the fourth receiver mixer. The output of Q32 is further applied to the SSB and FSK product detectors via buffer amplifiers Q31 and Q14: 2SC2458.

• CAR4

CAR4 on the IF unit serves as a BFO dedicated to CW demodulation, and as a side tone generating carrier. The oscillator frequency is 99.2 kHz, but it is varied by the CW PITCH control so the receiving pitch can be set to the desired frequency in the CW mode. The CAR4 signal is generated by Q16: 2SK192A and is applied to buffer amplifier Q15: 2SC2458. The output is supplied from the CAR4 terminal to the Control unit generator side tone and, at the same time, it is applied to buffer amplifier Q14 via diode switches D34 and D68 and connects to the CW detector.

• Reference frequency generator

The reference frequency f_{STD}, the frequency control base of the TS-940S, is generated by the 20 MHz crystal oscillator X1 and Q1: 2SC2668 on the PLL unit, and further applied to buffer amplifier Q2: 2SC2787. X1 and Q1 are replaceable by the optional TCXO (Temperature Compensated Crystal Oscillator) SO-1.
The output of Q2 is used as the 20 MHz f_{STD} as is. It is also multiplied three times to provide 60 MHz $3f_{STD}$. Further, it is divided to 1/2 by half of IC1: SN74LS73AN to provide 10 MHz 1/2 f_{STD}. This 1/2 f_{STD} is supplied to the CAR unit via buffer amplifier Q4: 2SC2787 as well as being used in the PLL unit. The 1/2 f_{STD} is further divided to 1/2 by the other half of IC1 to provided a 5 MHz 1/4 f_{STD}.

• AFSK signal and marker signal

A part of the 5 MHz (1/4 f_{STD}) signal generated by the PLL unit frequency generator reference is applied to 1/5 divider IC2: SN74LS90N to provide a 1 MHz (1/20 f_{STD}) signal. This signal is applied to programmable divider IC4: MC569BCP. The dividing ratio of this IC is switched between 218/235 interlocked with the FSK key SPACE/MARK setting. The output of IC4 returns to IC2, passes through the 1/2 divider, establishes a 50% duty cycle and is then sent to the microphone amplifier circuit of the IF unit via active LPF Q4: 2SA1115, where it is converted to an FSK modulation signal. The total dividing ratio is 1/8720 f_{STD} (2.2936 kHz) in SPACE and 1/9400 f_{STD} (2.1277 kHz) MARK. The shift width is 165.9 Hz, which is a slight deviation from the standard value, but no problem in practical use.

The carrier frequency and shift width during transmission are the same in accuracy as f_{STD}, and are very stable. In modes other than FSK, IC4 stops operation and thus, an AFSK signal is not transmitted.
The marker signal chain divides the 1 MHz (1/20 f_{STD}) signal from the preceding stage IC2 to 1/10 through IC3: SN74LS90N to generate 100 kHz signals (1/200 f_{STD}). When the marker switch is off, IC3 is reset and the operation is stopped.

RECEIVER

The signal received through the antenna is applied to the RF unit ANT terminal. The signal passes through the transmitter/receiver selector circuit and goes out from the EXT terminal. The output is connected to the RF unit RXA terminal via the selector circuit provided on the rear panel. This signal is applied to the receiver BPF through the RF attenuator (0, 10, 20, or 30 dB selectable) via relays RL1 and RL2. The BPF divides the received frequency range (up to 30 MHz) into nine bands, which are automatically selected by RX BPF control data (RB0—RB3) from the Digital A unit.

Receive frequency (MHz)	RX BPF information				RX BPF
	RBϕ	RB1	RB2	RB3	
~0.5	0	0	0	0	A
0.5~1.5	1	0	0	0	B
1.5~3	0	1	0	0	C
3~4	1	1	0	0	D
4~7	0	0	1	0	E
7~8.5	1	0	1	0	F
8.5~14	0	1	1	0	G
14~20	0	0	0	1	H
20~30	1	1	1	0	I

Table-4 Selection of RX BPF

The signal from the BPF runs through the RF AGC circuit composed of PIN diodes D23 and D26: MI204. It is then amplified by RF amplifier comprising Q10: 2SK125 pair and applied to the first receiver mixer Q9: 2SK125 pair, where it is mixed with the VCO signal, and the output is converted to the first IF signal at 45.05 MHz. This signal is applied to the grounded gate post amplifier Q7, 8: 2SK125, and the output is applied from the RIF terminal to IF unit.
The unwanted signal components are eliminated from the 45.05 MHz first IF signal when it passes through the MCF XF1 with 15 kHz bandwidth. The signal is then applied to the second receiver mixer Q4 and Q5: 2SK125, mixed with the HET signal (36.22 MHz) and converted to the second IF signal (8.83 MHz). This signal is separated into two channels: one is supplied to the noise blanker on the Control unit, and the other is applied to the second IF signal filter circuit via the noise blanking gate comprised of diodes D3—D6: 1S1587.
This filter circuit is provided with crystal filter XF2: YK-88S1 with a 2.7 kHz bandwidth for SSB (used also for wide CW/FSK and narrow AM), and wide band LC filters L37, L38 for FM (used also for wide AM when the optional AM filter is not provided.) As an option, the filter circuit permits use of two kinds of filters: a YK-88C-1 with 500 Hz bandwidth for CW and a YK-88A-1 with 6 kHz bandwidth for AM. These four filter types are automatically selected by the W/N-mode information (WN, ND2 and MD1) from the Digital A unit via the keyboard.

W/N switch	WIDE		NARROW	
Mode	2nd IF filter	3rd IF filter	2nd IF filter	3rd IF filter
SSB	2.7 kHz	2.7 kHz	2.7 kHz	2.7 kHz
CW, FSK	2.7 kHz	2.7 kHz	0.5kHz*2	0.5 kHz*3 or 0.25 kHz*4
AM	6 kHz*1	6 kHz	2.7 kHz	2.7 kHz
FM	Wide band	6 kHz	Wide band	6 kHz

*0: 2.7 kHz+2.7 kHz=2.4 kHz (Total selectivity)
*1: option YK-88A-1 installed *3: option YK-455C-1 installed
*2: option YK-88C-1 " *4: option YK-455CN-1 "

Table-5 Selection of filters

The received signal, having passed through the second IF filter, is applied to the third receiver mixer Q7, 8: 3SK73 to be mixed with the CAR2 signal (9.285 MHz) and then converted to the third IF signal (455 kHz). The output is then separated into two channels. One is connected to the Control unit FIN terminal, goes through IF amplifier Q45: 2SC2787 and third IF filter CF1: CFV455F. It is then applied to limiter amplifiers IC11 and IC12: μPC577H for amplitude limiting, and the output is applied to ceramic discriminators L12: CFY455S for FM detection. The detected output is supplied from the FMV terminal to the IF unit or the FM mode signal via the de-emphasis circuit and, at the same time, the noise component near 40 kHz is eliminated. The signal is then connected to the squelch circuit, noise amplifier Q46 and Q47: 2SC2458, noise rectifier D80 and D81: 1SS33 and the comparator consisting of IC13 2/2: NJM4558S. The above Control unit circuits function not only in the FM mode, but in all modes. Therefore, one noise squelch system is employed in all modes. The squelch control output mutes the IF unit audio amplifier via the MTU terminal. (IF unit Q28) The third IF signal is amplified by Q10: 3SK73 no the IF unit and is then applied to the filter circuit as the third IF signal. This filter circuit is provided with ceramic filter CF1: CFJ455K12 with a 2.7 kHz bandwidth for SSB (used also for wide CW/FSK and narrow AM) and ceramic filter CF2: CFW455HT with a 6 kHz bandwidth for AM wide. As an option, the filter circuit provides for use of either a CW 500 Hz crystal filter: YG-455C-1 or 250 Hz: YG-455CN-1 bandwidth filter. These three filter types are automatically selected by information from the Digital A unit, like the second IF filters. For selection operation data, refer to Table. 5. The signal from the third IF filter is amplified by Q11: 3SK73 and applied to the fourth receiver mixer to be mixed with the 355 kHz (CAR1—CAR3) signal and converted o the fourth IF signal. The output is applied to Q13: 2SK73 via the notch filter circuit. This amplifier output is detected by either the SSB/CW product detector or the AM detector. The detected signal is applied to AF GAIN control via the squelch gate Q28: 2SC2458 and preamplifier Q29: 2SC2459. In CW mode, it is also possible to pass the signal through the AF TUNE circuit, IC1 and IC2: BA718. The output of Q3 is also applied to the AGC circuit. The received AF signal from the AF GAIN control is applied to the Control unit, where it is amplified by the audio power amplifier IC15: HA1368 and used to drive the speaker.

• Front end

The TS-940S RF circuit has been specifically designed to provide high immunity to strong adjacent signals. The incoming signal from the antenna is first applied to a source follower buffer consisting of two 2SK125s, and then to a balanced mixer (consisting of two 2SK125s) where it is converted to the 45.05 MHz first IF signal. This IF signal is then applied to a grounded gate amplifier-pair. The VCO signal is delivered to the RF unit at low level, and is applied to the balanced mixer after being high-gain amplified. The use of a source follower for the first receiver stage reduces pre-mixer distortion and harmonics to negligible levels.

The junction FET balanced mixer contributes immunity to strong adjacent signals. The amplifier which follows allows low mixer gain. This design practically eliminates mixer saturation.

Figure 6 shows the IM (intermodulation) dynamic range characteristic. The characteristic shown was measured with a TS-940S in the CW mode with an optional YG-455C-1 IF filter (center freq.: 455 kHz, bandwidth: 500 Hz) installed. The noise floor level is −138 dB, IM dynamic range is 102 dB, and the intercept point is +14 dB.

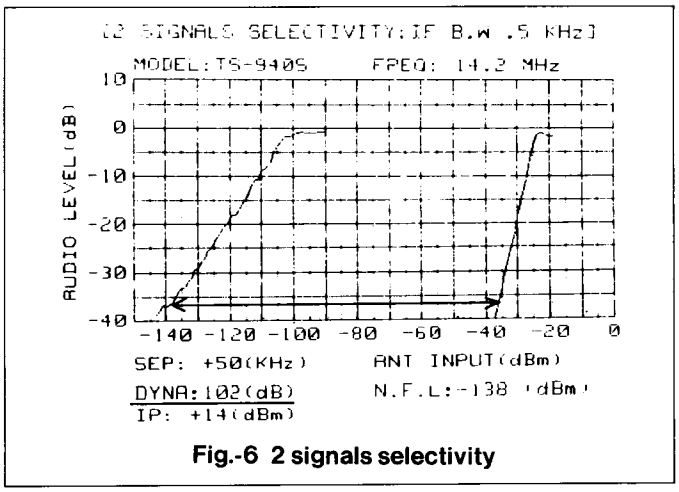


Fig.-6 2 signals selectivity

Additional receiver circuit

• Noise blanker (provided on the Control circuit)

Fig. 7 gives a block diagram of the noise blanker. This circuit is comprised of two channels, NB1 and NB2. The signal taken from the tuned output circuit of the second receiver mixer, comprised of Q4 and Q5 on the IF unit, is supplied from the NA terminal to the Control unit and amplified approx. 70 dB by Q12—Q15.

In the case of the NB1 channel, the noise signal is detected by diodes D64 and D65 through the buffer Q16 and then applied to the switching transistors Q18 and Q22. In the case of the NB2 channel, the noise is directly applied to the noise detector comprising D61 and D62. The NB1 channel takes out only the pulse noise contained in the input signal and switches the noise blanking gate composed of diodes D3—D6, located before the IF unit XF2.

NB1 channel operation is conventional. On the other hand, the noise output detected by D61 and D62 in the NB2 channels is waveform shaped by IC5 after running through D63 and Q19, and only the high level pulse component is taken out as a square wave.

This component is switched by Q18 and in turn is used to switch the NB gate via D66 and Q22. At the same time, it is also used for switching the third receiver mixer Q7, Q8 on the IF unit via Q20 and Q21. The NB2 channel is especially effective for that special noise known as "The woodpecker".

In addition, in the TS-940S, the "click" noise generated when the frequency is changed one step by the digital VFO is eliminated through the NB2 channel by utilizing the BLK signal from the Digital unit. The functions of the NB circuit are described in detail below.

In Fig. 8, Q18 and Q22 form a conventional NB circuit, which controls the NB gate. When the NB1 switch S14 is turned on, Q18 turns on and controls Q22 according to whether or not a pulse noise exists, and opens or closes the NB gate comprising D3—D6 on the IF unit.

NB LEVEL (VR7) varies the operating threshold of Q18 so the NB effect can be varied.

Next, NB2 is explained. When a signal corresponding to a noise is applied to Q19, the collector of Q19 is set to a low level (hereafter abbreviated Lo. (and high level to Hi.) IC5, pins 11 and 9 are Hi, because pin 12 is Lo due to R172. As described above, when the collector (IC5, pin 8) of Q19 becomes Lo, IC5, pin 10 becomes Hi. As pin 10 next becomes Hi, a charging current flows in C176, pin 12 becomes Hi and pins 11 and 9 become Lo, in sequence.

As pin 9 becomes Lo, pin 10 is held Hi. This holding time is determined by the charge constant of C76 and R172, approx. 4 ms. If this time is exceeded, pins 11 and 9 are returned to their initial states, Hi.

During this period, the conventional NB1 channel is operating through D66, and Q27 and Q21 are operating, whereby the third mixer (Q7 and Q8 on the IF unit) is cut off. Even if pins 11 and 9 become Hi, the base voltage of Q21 is in the state of cutting off the charging voltage determined by R175 and C78, and it continuously cuts off the third mixer. This is the control for NB2.

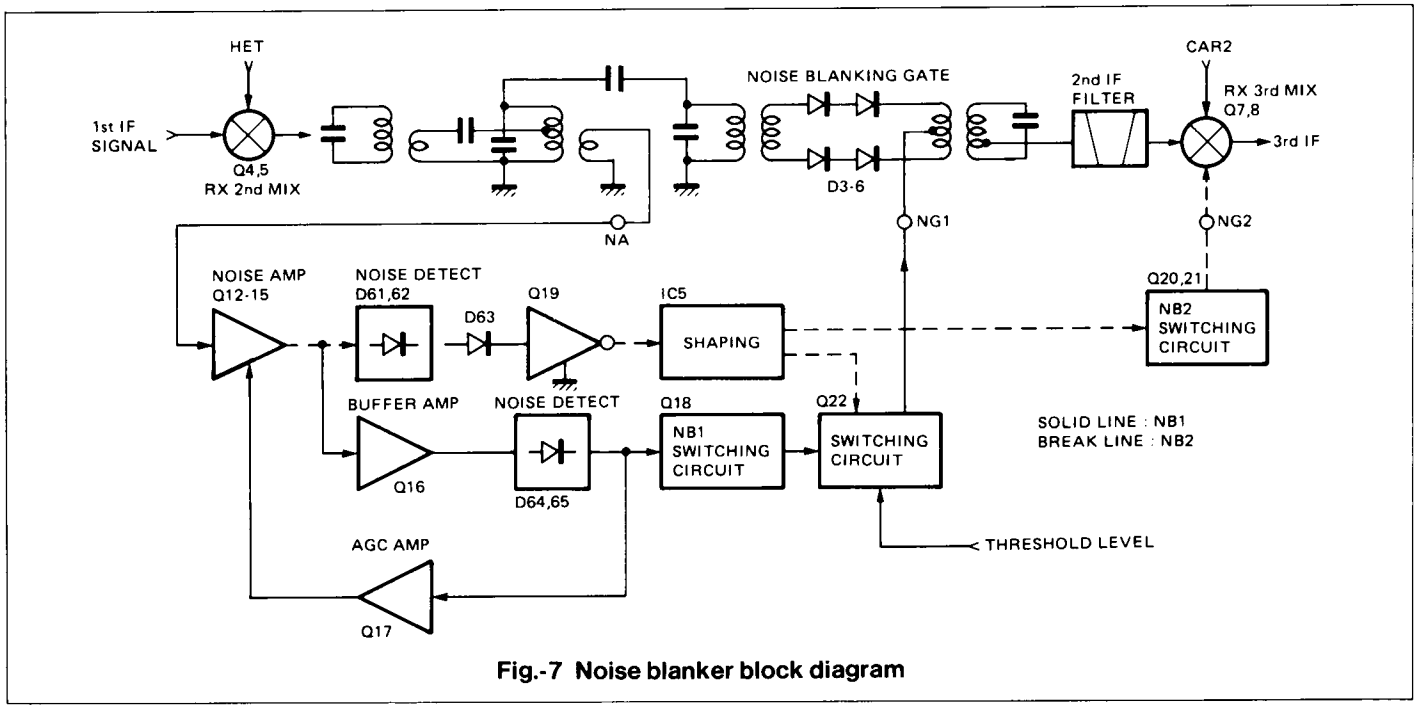


Fig.-7 Noise blanker block diagram

IC5, pin 6 is connected by R171 (56 kΩ) and returned to Hi when the NB2 control time (about 4 ms) elapses. Upon this change from Lo to Hi, a charging current flows in C77 through R178 and changes pins 1 and 2 from Lo to Hi. IC5, pins 3 and 5 become Lo, keeping pin 4 Hi and holding the charging time determined by C77 and R173, approx. 80 ms. During this period, IC5, pin 13 is held Lo (pin 11 is Hi) through D68 so the NB2 does not mis-fire with a normal pulse for approx. 80 ms from the time the first noise pulse goes out, even if a pulse noise is again entered. This is the operation for periodic woodpecker noise. When the NB2 channel is on, conventional noise is also blanked because one pole of S15 operates the NB1 circuit.

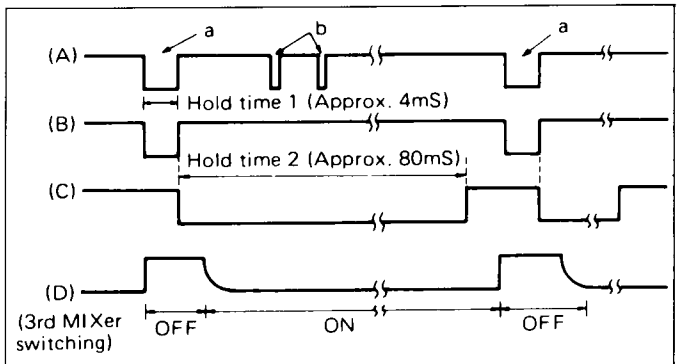


Fig.-9 NB2 timing chart

• CW-VBT, SSB-SLOPE-TUNE (RF/IF and PLL/CAR unit)

The TS-940S is equipped with SSB SLOPE TUNE and CW VBT circuits, a notch filter, and an AF TUNE cirucit which operates in the CW mode.

The TS-940S provides the best variable characteristic depending on operating mode and IF bandwidth, using digital technology controlled by microprocessor. In this parented systems, the effective intermediate frequencies of two filters are shifted independently to allow control of the overall bandwidth (U.S. PAT No. 4267605). The principle of the IF shift system is briefly explained below.

Assume that the desired signal (f_0) and an adjacent signal (f_1) are input to the receiver. These two signals are converted to the intermediate frequency and applied to the IF filter. If the filter has the selectivity characteristic shown in Figure 10 (b), the adjacent signal passes through the filter and is demodulated, resulting in interference.

If the local oscillator frequency is shifted by -Δf. This is indicated by f_0' and f_1' in Figure 10 (b). In this case, only the desired signal passes through the filter However, the pitch of the demodulated audio signal will change unless the carrier frequency (fc) is shifted by the same amount as

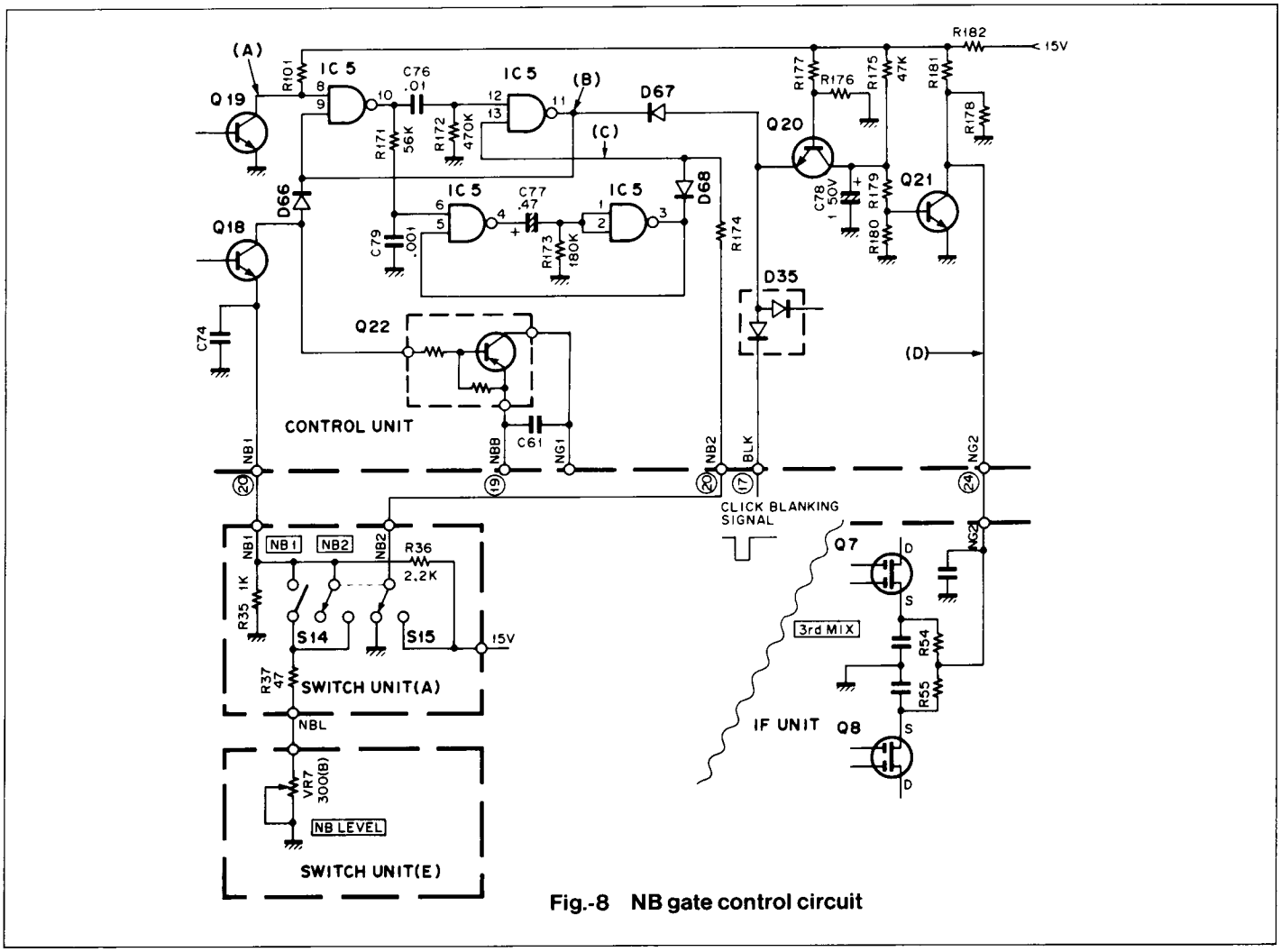


Fig.-8 NB gate control circuit

the local oscillator frequency. Otherwise, this would make the demodulated SSB signal unrecongnizable.

With the circuit shown in Figure 10 (c), both the local oscillator and carrier shift together. When the carrier frequency is changed by -△f, the local oscillator frequency input to the mixer is also changed by an equal amount. In Figure 10 (b), the f_0' and f_1' indicate the same signals as previously described. In this example, however, the carrier frequency is changed from fc to fc'. This is equivalent to shifting the frequency of the filter by +△f (as indicated by B) without the resultant frequencies of the incoming signals being changed.

The IF shift system avoids interference from adjacent signals by causing an apparent shift in the center frequency of the filter, as shown above.
Assume that there are two adjacent signals as shown in Figure 10 (d). When the filter frequency is as indicated by A, signal f_1 causes interference and, when it is as indicated by B, signal f_2 causes interference. The IF shift system cannot prevent interference when two or more signals are within the filter passband and the desired signal is between them.

In the new interference reduction system, the apparent center frequencies of two IF filters are shifted independently to vary the overall IF bandwidth.

The circuit shown in Figure 11 (a) simply combines two IF shift systems. This system can narrow the overall IF bandwidth as shown in Figure 11 (b) by independently shifting the carrier oscillator frequencies (fc1 and fc2). In Figure 11 (b), A represents the overall IF frequency response when the apparent frequencies of both the IF filters are equal; at this time, the overall bandwidth is maximum. When the center frequency of the 1st filter is shifted as indicated by dotted line B (by varying fc1) and that of the 2nd filter is shifted as indicated by C (by varying fc2), the overall IF bandwidth is reduced to that indicated by line D.

Interference caused by two or more adjacent signals, previously discussed and shown in Figure 10 (c) can be reduced by this new cirucit. Practically speaking, however, this circuit configuration is too complex and expensive. A simplified circuit is shown in Figure 11 (c). This circuit operates in the same basic manner as the circuit shown in Figure 11 (a), but the number of mixers and oscillators has been reduced.

Figure 12 shows the TS-940S "rough" block diagram which is more complex than that shown in Figure 11 (c) because the 1st IF frequency is 45.05 MHz to achieve general coverage, the notch filter circuit is designed to operate independently of the VBT, and a CW pitch control circuit is employed. The 1st IF filter has a bandwidth of 15 kHz and has no influence on the interference reduction system. (In practice, the 1st IF filter has the same apparent center frequency as the 2nd filter, even if the 2nd filter is shifted.) The overall or composite frequency response of the 2nd and 3rd IF stages is as shown by line A in Figure 13 when the CAR1 and CAR2 frequencies are at their normal positions.

Assume that the CAR1 frequency is lowered by f_1 (that is, the VCO frequency f_L is lowered by $\triangle f_1$) to shift the overall center frequency of the 2nd and 3rd IF stages to the position indicated by dotted line B. The overall bandwidth does not vary at this time. When the CAR2 frequency is lowered by $\triangle f_2$, the 2nd filter center frequency is shifted, indicated by C. Thus, the composite IF bandwidth is reduced.

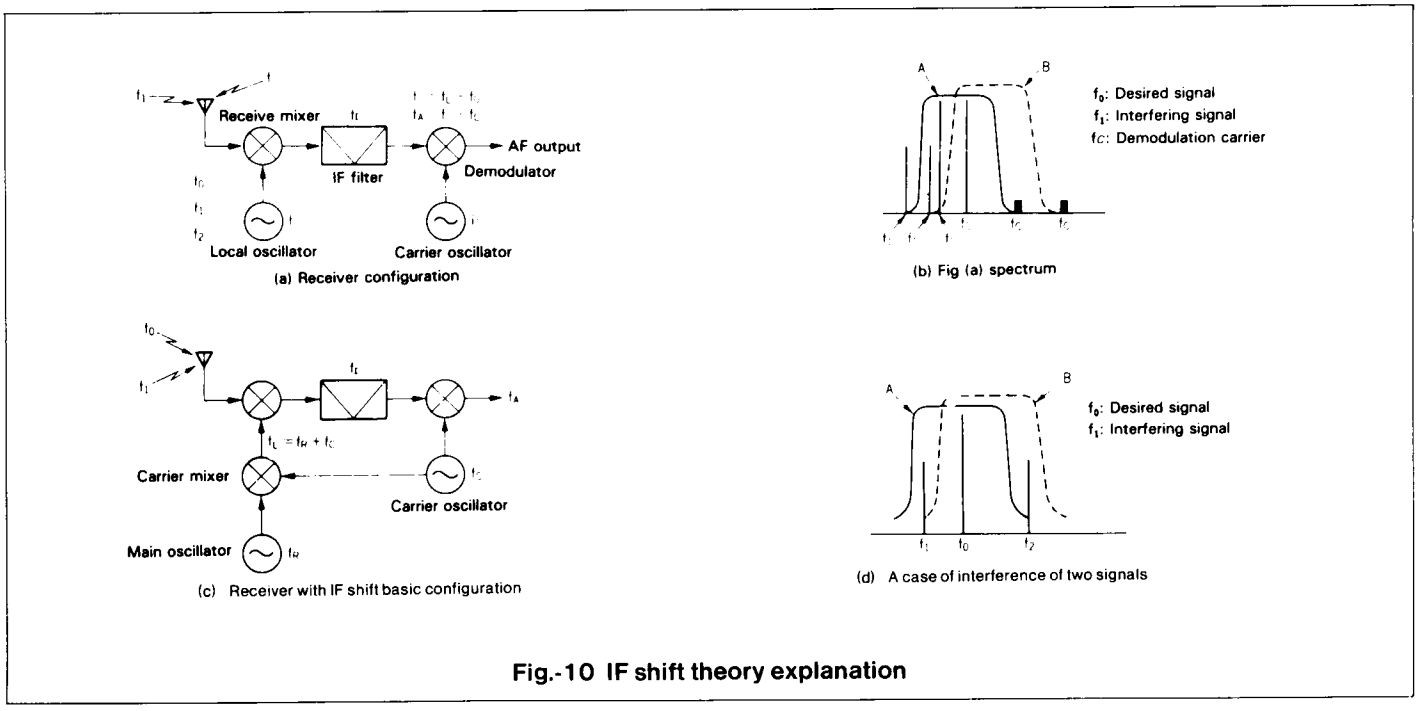


Fig.-10 IF shift theory explanation

In the TS-940S, CAR1 and CAR2 frequencies are generated by the PLL cirucit and controlled by the microprocessor, and the amount of change $\triangle f_1$ and $\triangle f_2$ is digitally tracked, allowing only the bandwidth to narrow without changing the center frequency of composite passband. This is the principle of the CW-VBT feature used in the TS-940S.

When $\triangle f_1 = \triangle f_2$, the low frequency cutoff point is raised, allowing low frequency interference rejection.

The high frequency cutoff can be varied by lowering the CAR2 frequency by $\triangle f_2$ without changing the CAR1 frequency. With the TS-940S SSB SLOPE TUNE system, these two functions are individually adjustable by separate controls, and correspondence between the function and the control is reversed according to the sideband mode.

These HIGH and LOW CUT controls are concentrically arranged on the front panel and can be easily manipulated. they are audio high and low cut controls.

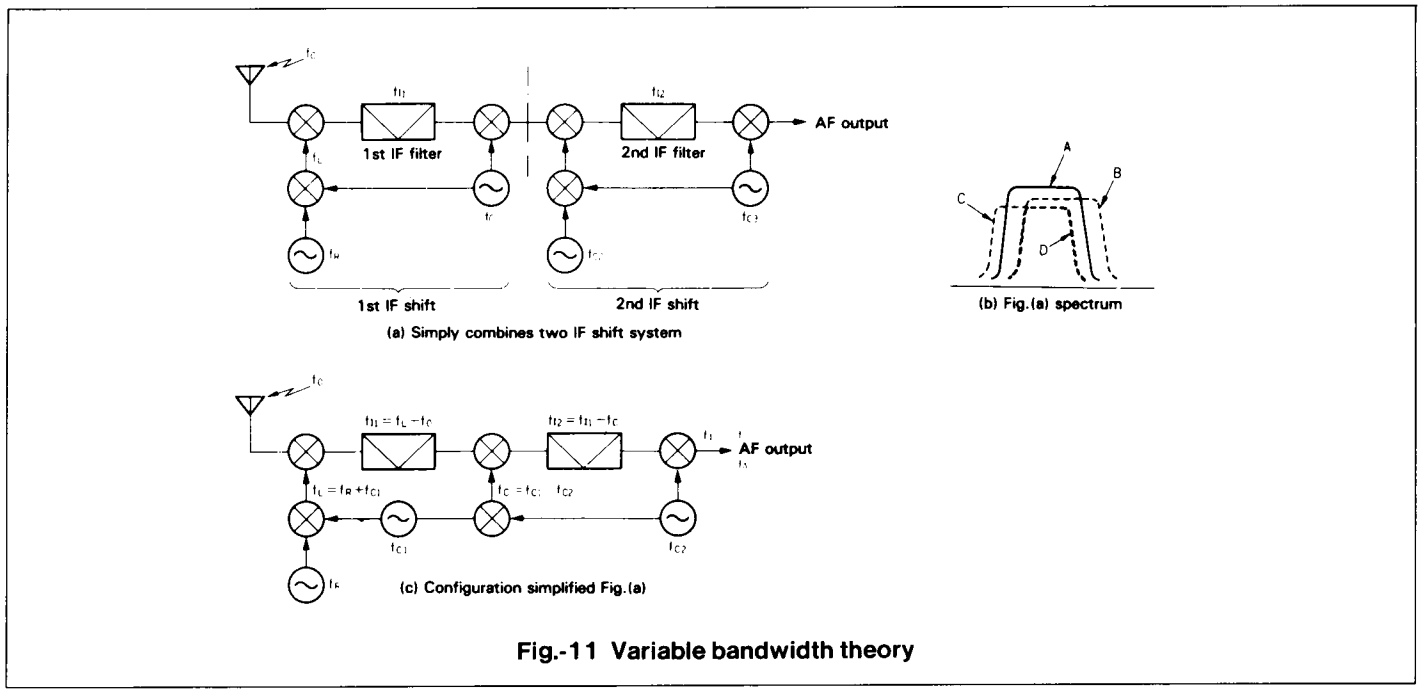


Fig.-11 Variable bandwidth theory

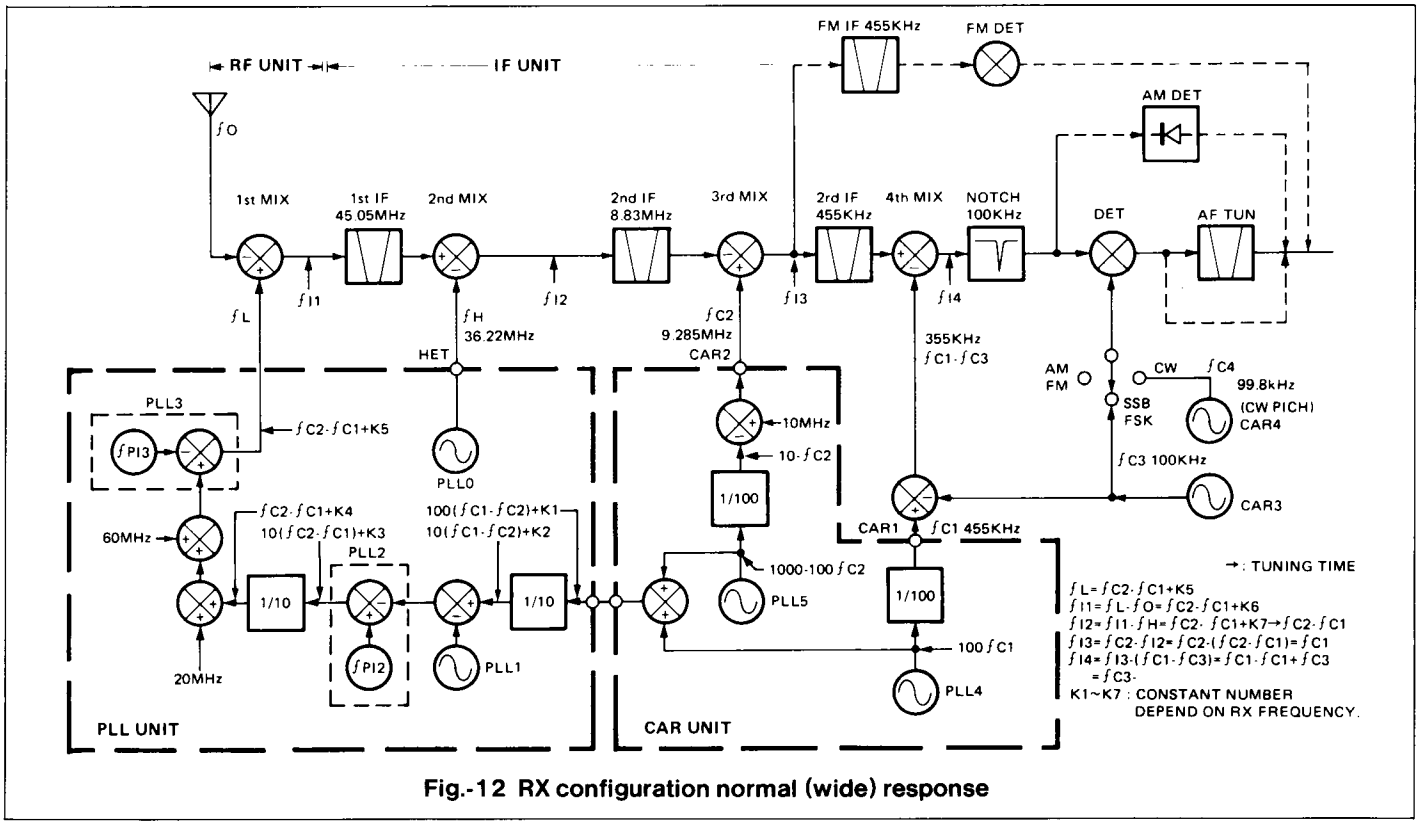


Fig.-12 RX configuration normal (wide) response

The SSB SLOPE TUNE system operates in the LSB and USB modes. The CW VBT system operates in the CW, FSK, AM and TUNE modes when all optional filters are installed. When no optional filters are installed, the CW VBT system operates in the CW, FSK and TUNE modes with the filter selector switch placed at WIDE, and in the AM mode with the filter switch placed at NARROW. (For the precise relationship between the optional filters and their interference reduction features, please see the paragraph on filter options.)

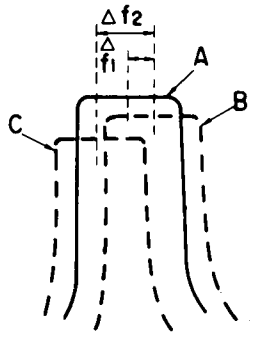


Fig.-13 VBT operation

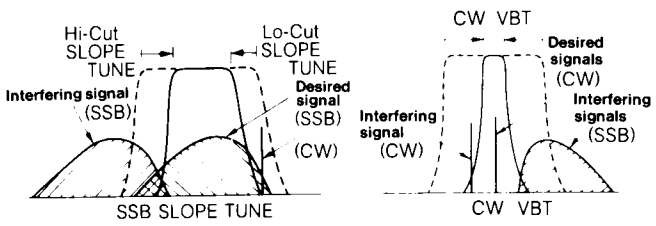


Fig.-14 Variation in overall frequency response

- **Notch filter (provided in the IF unit)**

This is a bridge T filter composed of L, C and R elements, which is inserted between the fourth receiver mixer and the 100 kHz IF amplifier Q13. The notch filter, which has the sharp characteristic that provides attenuation on the order of 40 dB to the interfering signal shown in Fig. 15. It varies the voltage applied to the cathode of varicap diode D38, thereby changing the resonant frequency. The notch filter functions in all modes except FM.

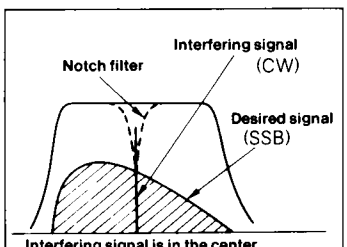
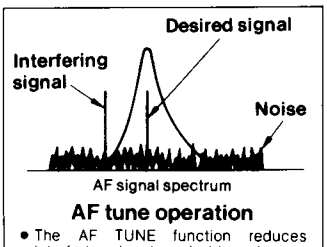


Fig.-15 Notch Filter



AF tune operation

- The AF TUNE function reduces interfering signals and white noise.
- This function should only be used during operation in the CW mode.

Fig.-16 AF tune operation

- **AF-TUNE (provided on the IF unit)**

Figure 16 illustrates the principle of the AF TUNE feature, which reduces interfering signals and white noise.

This is an active filter using IC12, which is inserted between the SSB/CW product detector and AF amplifier Q29. The frequency of this filter is over 800 (±400) Hz and functions only in the CW mode. When the AF-TUNE switch is off, the audio signal is bypassed by diode D63.

TRANSMITTER

The audio signal from the microphone is applied to the IF unit MIC terminal and is preamplifier by Q36: 2SC2459. The output is split to the MIC GAIN control (on the front panel), the FM MIC GAIN control (on the top panel) and VOX circuit in the SSB and AM modes. The SSB signal channel is returned to the IF unit, amplified by IC3: TA7140P and applied to balanced modulator D73: ND487R1-3R. A diode switch is provided at the input of IC3, which selects the audio signal in the SSB and AM mode, and the AFSK signal (2.2936 kHz/2.1277 kHz) from the PLL unit in the FSK mode. Balanced modulator D73 is constructed as a package containing four Schottky diodes of matched characteristics, which provides stable modulation characteristic against varying operating conditions such as temperature fluctuation. The 455 kHz DSB (Double Side Band) signal from D73 is converted to SSB by filter CF1 (or CF2 in the AM mode), which is shared by the third receiver IF filter after passing through the buffer amplifier Q37: 3SK73.

The filter output runs through buffer amplifier Q39: 2SC2458 and is then applied to the RF speech processor circuit Q40: 2SC2458, IC4: TA7302P and Q43: 3SK73. When the processor is off, the signal is applied directly to the first transmitter mixer Q44 and Q45: 3SK73 via diode switch D78 and D79: 1S1587. In FSK mode, even if the processor switch is off, approx. 10 dB compression is automatically applied. This effectively suppresses any level difference between MARK and SPACE in AFSK. Note, however, that the compression meter does not deflect.

In the AM mode, even if the processor switch is off, the signal runs through D78 and D79 but does not pass through the processor. The processor output signal is applied to the first transmitter mixer via diode switch D83. Here, the audio signal is mixed with the CAR2 signal (9.285 MHz) and converted to 8.83 MHz. The 8.83 MHz signal runs through SSB filter XF2 (a wide band filter L37, L38 or optional YK-88A-1 in AM mode) shared by the second receiver IF filter, where any splatter component which may be generated in the speech processor is eliminated.

The signal is then applied to the transmitter IF amplifier Q48: 3SK73. However, in CW and FM modes or during auto antenna tuning, the CAR0 signal is applied to Q48 via buffer amplifier Q46: 3SK73. Therefore, in these modes, since the transmitter signal does not pass through the narrow band filter, full CW break-in operation is enabled.

ALC is applied to transmitter IF amplifier Q48, and a part of its output is supplied from the MON terminal to the monitor circuit on the Control unit via buffer amplifier Q49: 2SC2787.

The transmitter signal is then applied to the second transmitter mixer Q50 and Q51: 3SK73, where it is mixed

with the HET signal (36.22 MHz), yielding a TIF signal at 45.05 MHz, whose output is connected to the RF unit. In the RF unit, the signal is mixed with the VCO signal in the third transmitter mixer Q1 and Q2: 3SK73, providing the final transmitter frequency.

Any unwanted components in this signal are eliminated in the transmitter BPF (1.8—30 MHz), amplified by wideband amplifier Q3: 3SK73, Q4: 2SC1907 and Q5: 2SC1973 and supplied from the DRV terminal to the Final unit as the drive-level output. This drive output is automatically disconnected from the Final unit input if a connection is plugged into the transverter connector. The signal applied to the Final unit is amplified by wideband drivers Q2, Q3: MRF485 and finals Q4, Q5: MRF422.

The output of the Final unit passes through the Filter unit where unwanted the higher harmonic component element is eliminated. The Filter unit divides the transmitter frequency range into bands, and each LPF is automatically selected by TX LPF information (LP0—LP2) supplied from the Digital A unit.

After passing through the Filter unit, the transmitter output runs through the AT (optional) unit, the transmitter/receiver selector circuit and then is connected to the ANT terminal on the rear panel.

Additional transmitter circuit

- **ALC circuit (provided on the Control unit)**

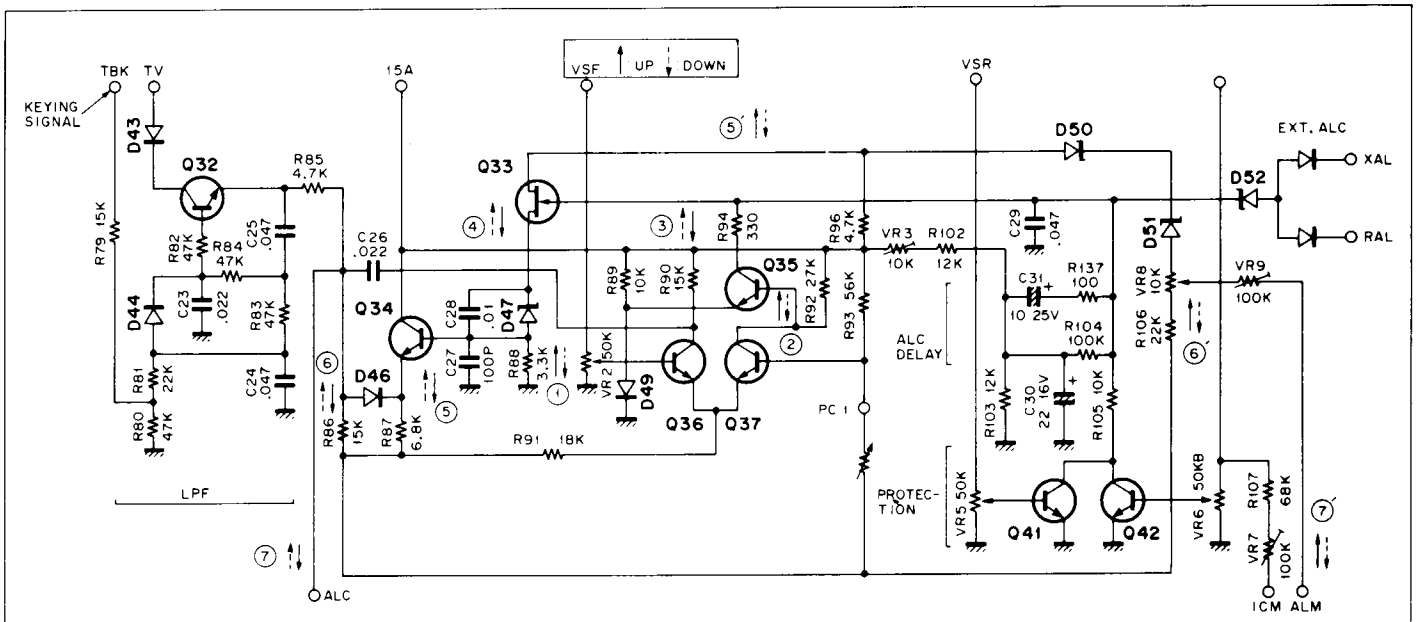


Fig.-17 ALC circuit

Forward wave voltage VSF detected in the Filter unit is applied to the base of Q36 in the Control unit. Q36 and Q37 are differential amplifiers. When the VSF voltage rises, the collector voltage of Q37 rises and that of Q35 lowers. Therefore, the gate voltage of Q33 lowers and the base and emitter voltages of Q34 lower. As a result, the ALC line voltage decreases due to D46 and Q34 being connected to the ALC line, thus controlling TX RF output power.

The drain (output) of Q33 operates the ALC meter. Trim controls VR8, VR9 are the internal set points for the ALC meter circuit. The TBK line voltage delivers the keying signal through active low-pass filter Q32 where any key click components are eliminated, its output becomes ALC voltage, and this is supplied to the ALC line. As seen from this description, the ALC voltage is used not only for controlling transmitter output power, but is also for keying the output in the CW operating mode.

- **Power control**

The power control provided on the front panel permits control of transmitter output from full power to 10 W or less. The power control is a 2-ganged potentiometer, which controls the first gate voltage of voltage amplifier Q3 in the RF unit to vary the voltage gain. Secondly, it controls the base voltage of ALC circuit differential amplifier Q37 in the Control unit and therefore the threshold level of the ALC amplifier. Therefore, when the Power control is varied, ALC is held nearly constant at any setting.

If the auto antenna tuner were to be used with the transmitter output set to minimum (10 W or less) by the Power control, the RF output power might be too low to detect the necessary controlling current and voltage and normal tune operation would not be possible.

To solve this problem, the TS-940S is designed to automatically switch FET Q3 gate voltage the RF unit voltage amplifier to its maximum value, regardless of the power control, set position, and at the same time, switch the base voltage of Q37 to provide a 50 W RF output level to properly operate the auto tuner.

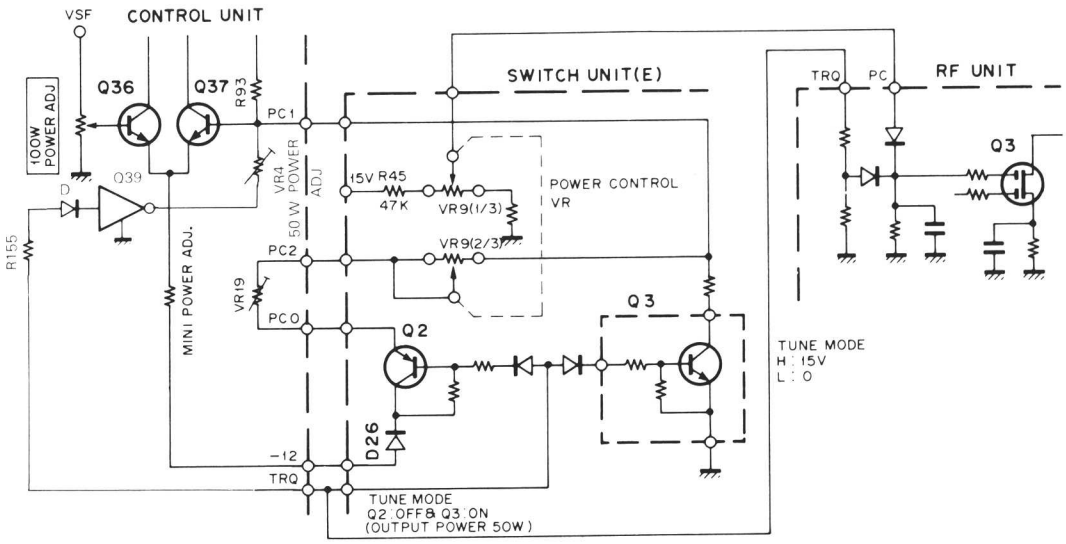


Fig.-18 Power control circuit

- **Speech processor (provided on the IF unit)**

The block diagram is shown in Fig. 19. An input signal runs through 455 kHz filter CF1 and buffer Q39. The signal is then amplified by Q40 and applied to detector D80 and limiter amplifier IC4. The detector output is applied to DC amplifier Q41 and Q42, where it is compressed logarithmicly. The output signal is coupled to the compression meter, indicating the compression level. The signal applied to IC4 is held constant in output level regardless of the input level. The signal is then applied to the first transmitter mixer via gain control amplifier Q43.

When the processor is off, the signal is bypassed by switching diodes D78 and D79. In FSK mode, even if the processor is off, approximately load compression is applied to level the amplitude change between the mark and space signals. In the FSK mode, the ALC level is adjusted by the processor OUT control

Figure 20 demonstrates the speech processor is effect.

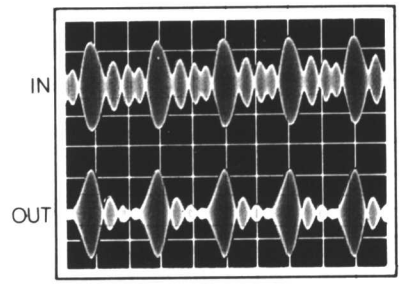


Fig.-20 The speech processor's effect (Approx. 10 dB compression)

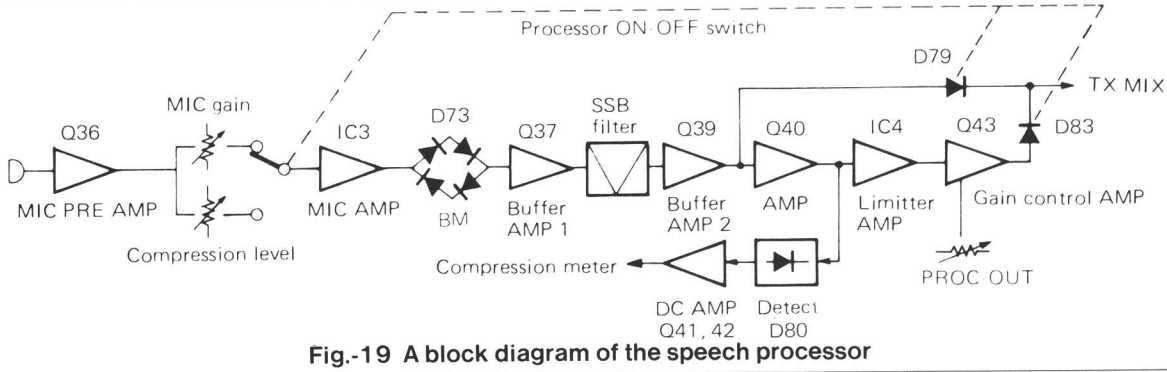


Fig.-19 A block diagram of the speech processor

- **Monitor circuit (provided on the Control unit)**

SSB/FSK mode

The signal taken from the drain of the secnd transmitter IF amplifier Q48 on the IF unit is amplified by Q49 and applied to the MON terminal. The output signal from the MON terminal is applied to IC16: μPC1037H via the Control unit buffer Q58.

In IC16, the CAR0 (8.83 MHz) is injected for signal product detection. This is amplified by Q59 and applied to the audio power amplifier IC15 via the monitor level internal adjustment control VR13.

FM mode

The output of the FM microphone amplifier Q64, Q65 and IC14 is amplified by Q62 and supplied to VR13, as in the SSB/FSK mode.

CW mode

Side tone circuit (provided on the Control unit)
CAR3 and CAR4 signals of 100 kHz and 99.2 kHz are product detected by Q57 to generate an audio beat at 800 Hz. Q57 is switched by the STK line through diode D71 and turned on when the key is closed, generating side tone. The 99.2 kHz CAR4 signal is frequency controlled by the pitch control on the front panel, allowing simultaneous variation of the CW side tone frequency and receiver CW tone pitch. Zero-beat adjustment with a received signal is acheived by simply making the receiving tone pitch equal to the side tone pitch.

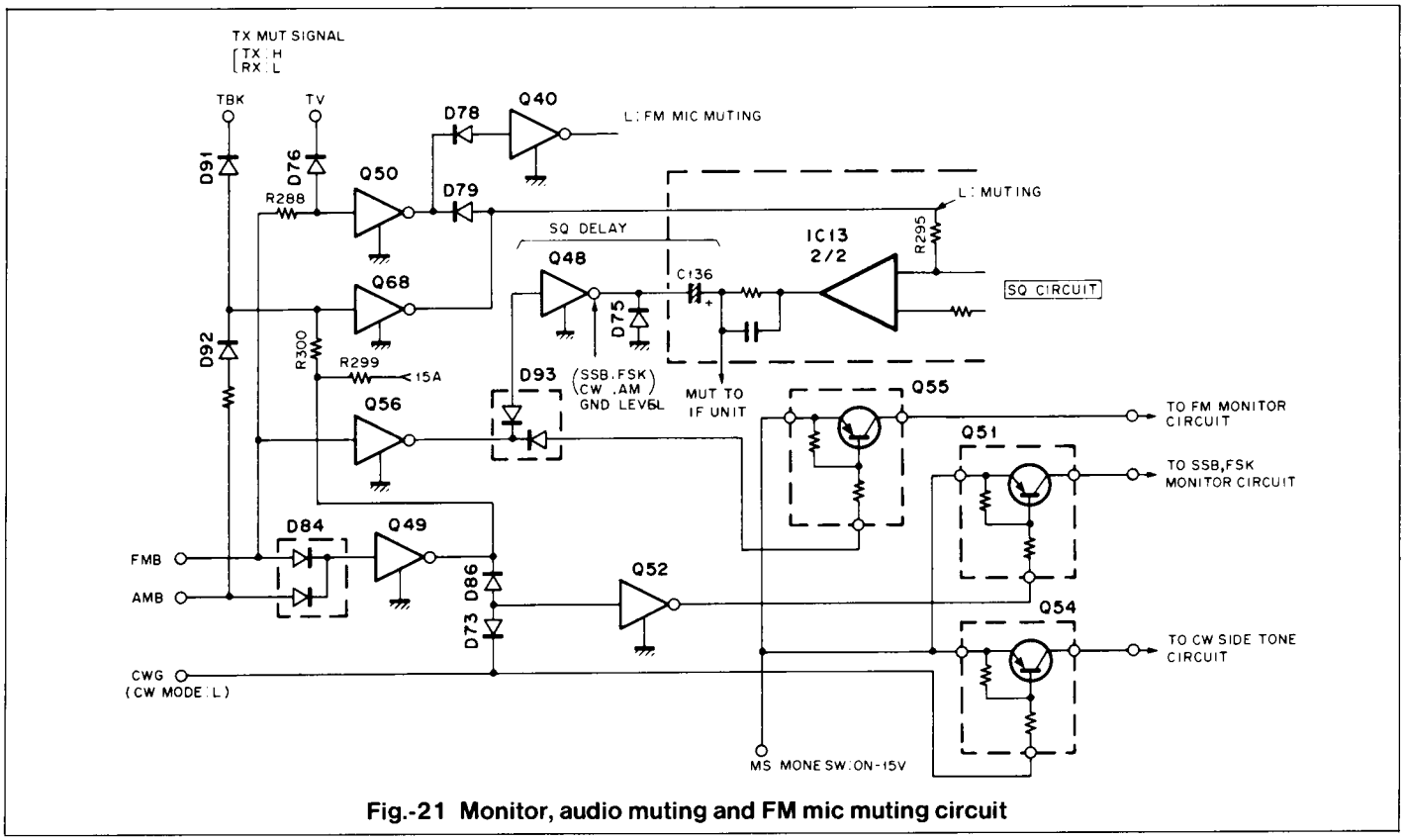


Fig.-21 Monitor, audio muting and FM mic muting circuit

- **SWR automatic arithmetic circuit (provided on the Control unit)**

The TS-940S employs the automatic SWR arithmetic computation circuit. The forward wave voltage VSF and reflected wave voltage VSR from the Filter unit are applied to an analog arithmetic circuit on the Control unit, output from IC9, pin 1 as VSR/VSF level, and indicated by the SWR meter. IC9 contains an integrating circuit and V-I converter for the auto tuner, while IC10 contains a triangular wave generator and voltage comparator. Q43 and Q44 are used for switching the forward and reflected wave input signals at an equal duty ratio.

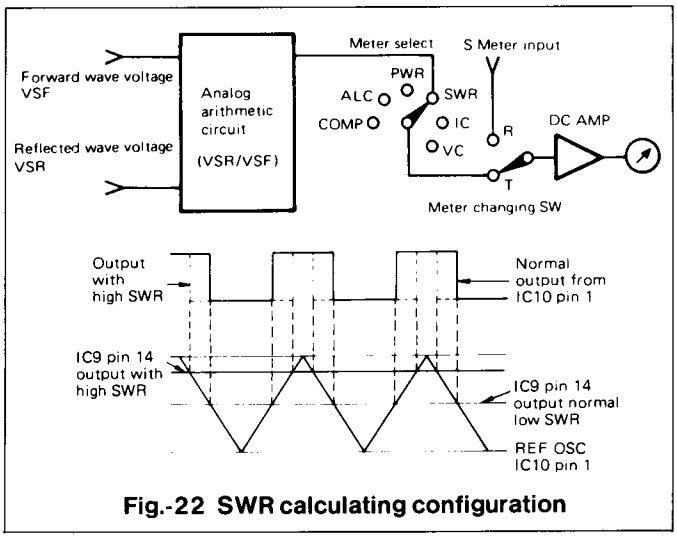


Fig.-22 SWR calculating configuration

- **Timing circuit**

The TS-940S has five kinds of timing signals for switching between transmission and reception; TV, RV, TR, TBK and ALC. Fig. 23 shows the timing relationship between these signals. This is the timing chart for SSB, MF, FSK and CW full break-in keying. The timing charts for CW keying in the CW semi-break-in and standby modes are shown in Fig. 24, (a) and (b).

TV and RV are the supply voltage to be applied to each of the various transmitter and receiver channel circuits. A pause of approx. 3 ms is designed between the switching of each voltage.

The transient state of each circuit stabilizes within this period. The TR live information the PLL channel of the transmit/receive status, and is used to switch transmitter and receiver frequencies during "cross band" mode operation. The transient state of this signal is also stabilized within the 3 ms pause time.

TBK is the keying signal in the CW operating mode. This signal is allowed to pass through the active low filter to

eliminate any key click component and then, the output is used to generate ALC voltage. Therefore, ALC voltage is used not only for controlling the transmitter output, but also for output keying in the CW mode.

In modes other than CW, output keying is unnecessary, but the timing remains the same. Fig. **24**, (a) and (b) give the timing charts fow CW semi-break-in operation and CW mode with just the standby switch. If Fig. **24**, the timing of RV, TR, etc. are omitted, as they are the same as those in Fig. **23**.

The trailing edge of TV is approx. 6 ms after that of TBK. During this period, the transmitter output breaks together with ALC voltage. TB and RB are the transmitter and receiver channel bias voltage; the timing is synchronized with the TV signal. RB is inverted. Fig. **25**. gives the basic block diagram to generate each of these timing signal previously discussed.

Fig. **26** shows the operating timing chart in this configuration. The actual operation of the timing chart will now be described. (See Fig. **27**. "Block diagram")

This circuit is operated by the keying input, standby switch (PTT) input, VOX input, ANTI-VOX input, etc. In the block diagram (Fig. 27), STBY SW Gate 3 (IC1 4/4) opens (D30, goes Hi) only at keying by the standby switch in CW mode. Operation by the standby switch in modes other than CW makes transistor Q6 turn off as D26 drops to GND in send mode. Thus, a high voltage is applied to inverter IC3 2/6 via D31. (In CW mode, since the cathode of D27 becomes low, a high voltage is not applied to D31.)

When the VOX is on, a high voltage is applied to inverter IC3 2/6 from the one-shot multivibrator via D4. (The VOX circuit is explained in a following section.) The output of inverter IC3 2/6 (pin 6) goes low, the cathode of D14 becomes low, and TR switching transistor Q7 turns off.

Thus, a high voltage is supplied to the TR terminal via D9. (As Q7 is on in the receive mode, the TR terminal is low.) At the same time, the RV AND gate 5 (IC4 2/3), pin 4 goes low (TX protection OFF → BTR terminal L), the output terminal, pin 6 becomes low and the RV switching circuit (Q30, Q28) turns off.

Therefore, as soon as the transistor level becomes high RV voltage level becomes low. (Fig. **23** — B)

The output of inverter IC3 2/6 enters the delay circuit composed of IC1 3/4, R29 and C13. The output signal delayed approx. 3 ms (H level) is applied to IC1 3/4, pin 4. (Fig. **23** — C). This signal becomes the TBK keying signal in the CW operating mode.

When the TBK signal is applied to the YV gate IC4 3/3 (pin 13) via Q24, a TV switching signal synchronized with the leading edge of the TBK voltage is generated at pin 10 as an output. At this time, as the RV gate output (IC4 2/3 pin 6) is at low level (D21 is off), IC4 2/3, pin 12 is at high level, like the output of inverter IC3 6/6. IC4 3/3, pin 11 is usually at high level when the PLL is in the lock states.

When this signal (IC3 3/3, pin 10) is applied to the TV switching circuit, a TV voltage is generated. (See Fig. 27, "Block diagram".)

Based on the TV voltage, an in-phase TB voltage and inverted RB voltage are generated. (Fig. **23** — D and E). The leading edge (RX → TX) of the timing circuit will now be discussed. When the key is up in the CW operating mode, as the output (pin 13) of the STBY switch gate 3 changes from high to low level and the output (pin 3) of gate 2 changes from low to high level, the output (pin 10) of oneshot multivibrator IC2 3/4 goes low and D4 turns off.

Since the cathode of D27 is at low level due to the CWG signal, the anode of D31 is held at low level, i.e., D4 D30 and D31 turn off. Thus, the input to inverter IC3 2/6 changes from high to low level, and the output of IC3 2/6, pin 6 changes from low to high level. When the VOX turns off during VOX operation or the standby switch is set to the REC position, the output of inverter IC3 2/6 becomes high level as in the previous narrative.

This signal is applied to the delay circuit and after 3 ms, the TBK voltage breaks.

TBK voltage is inverted by inverter IC3 3/6, and is used to change the input signal level of BK gate 7 (IC4 1/3, pin 8) from low to high.

Since pin 2 is at high level at break-in, gate 7 changes the output level at pin 9 from low to high at the trailing edge of the TBK timing signal. During semi-break-in, since pin 2 is held low during the delay time, output pin 9 changes from a low to a high level stage after the delay. At this time, the BK gate 7, pin 1 is high because the key is up. The BK gate 7

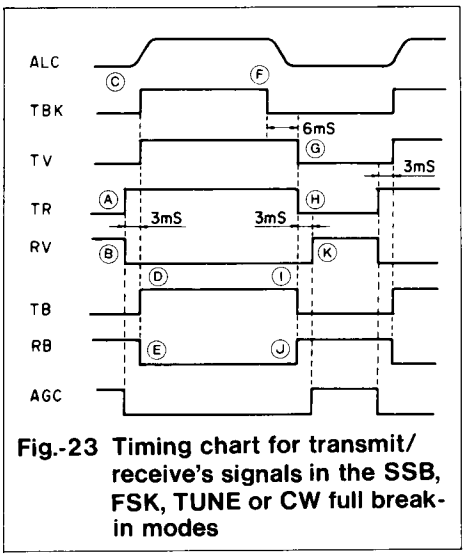


Fig.-23 Timing chart for transmit/ receive's signals in the SSB, FSK, TUNE or CW full break-in modes

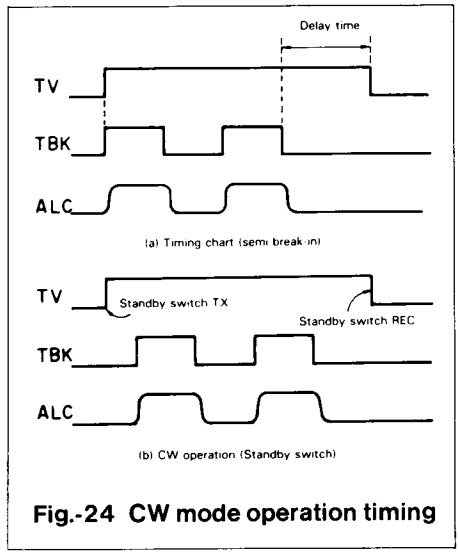


Fig.-24 CW mode operation timing

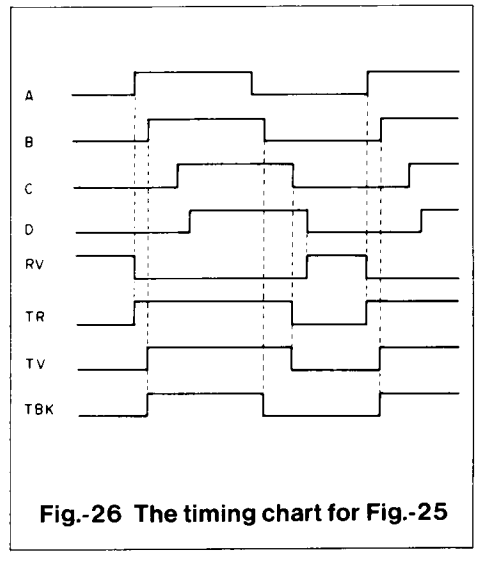


Fig.-26 The timing chart for Fig.-25

output signal is applied to delay circuit II and after approx. 5 ms, the signal becomes low level, and D23 turns off to change the TV gate 6, pin 13 from a high to a low logic level. Therefore, the output (pin 10) of TV gate 6 changes from high to low, and the TV voltage is lowered. (Fig. 23 — G).

At the same time, the TB voltage breaks and inversely, the RB voltage rises. (Fig. 23 — I and J) In addition, as the TV voltage being supplied from D36 to the TR line breaks at the same time, the TR voltage changes from high to low level.

Further, the output signal of delay circuit II is applied to the integrating circuit of delay circuit III, where it becomes a 3 ms delayed signal, and this output changes the RV gate 5, pin 3 from a low to a high logic level. (At this time, pin 4 and pin 5 are high level.) Thus, the output of RV gate 5 changes from low to high and RV voltage rises. (Fig. 23 — K) When a temperature protection signal or band protection signal are applied from the filter unit to the BTP terminal, the RV switching circuit functions via D21 and generates RV voltage. At the same time as TV gate 6, pin 12 is changed from high to low level by inverter IC3 6/6, the output signal level is also changed from high to low and the TV switching circuit turns off. Thus, TV voltage drops and the transceiver goes into the receiving state.

- **VOX, ANTI-VOX circuit (provided on the Control unit)**

In Fig. 27, "Timing circuit configuration", the MIC preamplifier output is applied to the VXZ terminal on the Control unit via the VOX gain control, amplified by VOX amplifier Q1—Q3 and applied to the following stage R-S flip-flop (IC1 1/4, pin 13). On the other hand, the AF output signal (SP2 signal) from the speaker is applied to ANTI-VOX amplifier Q10, Q11 to be DC rectification, and this output is applied the R-S flip-flop IC1 2/4, pin 9.

By using this logic function, the faster input either VOX or ANTI-VOX, is given priority. When the VOX input is given priority, a signal pulse is applied to VOX gate 1 (IC2 1/4, pin 12) and the gate is opened. However, gate 1, pin 13 is high when the VOX switch is on in SSB, FM or AM mode. When ANTI-VOX is given priority, VOX gate 1 (IC2 1/4, pin 12) is low and the gate is closed.

In CW mode the STK terminal signal (low at key down) is applied to VOX gate 2 (IC 2/4, pin 2) after being switched by Q9. Thus, a high level signal is applied to VOX gate 2 (IC2 2/4, pin 2) and the gate is opened when the key closed. Gate 2, pin 1 is high when the VOX switch is on in CW mode. Gate 1 or 2 signal goes through one-shot multivibrator IC2 3/4 and IC3 1/6 and enters the time constant circuit composed of C9, R18 and Q4, where the

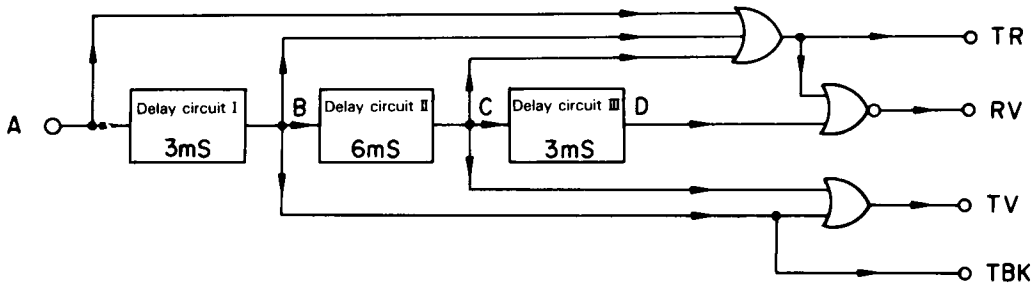


Fig.-25 Timing circuit basic configuration

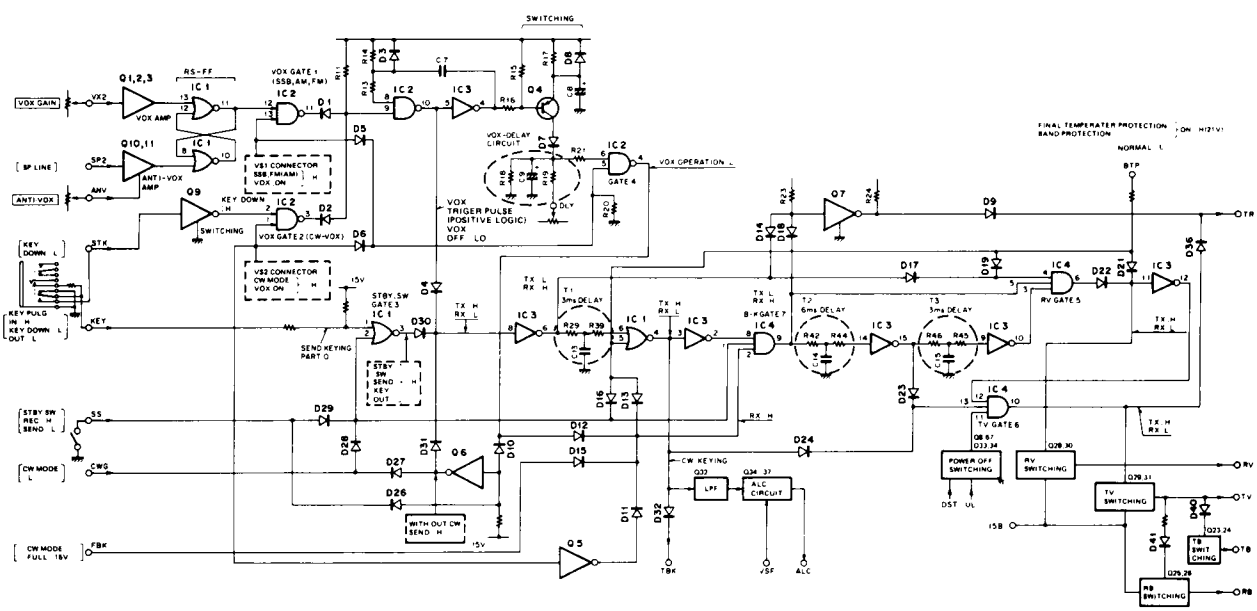


Fig.-27 Timing circuit block diagram

VOX hold time is established. Use of this type of logic circuitry increases response speed of the VOX and eliminates VOX/ANTI-VOX cycling.

- **Antenna tuner**

The block diagram is shown in Fig. 28. The TS-940 operates in the 1.8—29 MHz bands and is automatically adjusted so that the SWR becomes 1.2: 1 or less. For smooth antenna tuning the mode is stored before antenna tuning and set again after tuning. Fig. 31 shows the antenna tuner timing chart.

The AUTO-THRU relay protecture circuit (Q120, 121, 122, 123 and 126) holds the AUTO-THRU relay condition during transmission. This circuit monitors the AUTO-THRU switch condition and the TV line (Transmit-high level/receiver-low level) and allows a change in the AUTO-THRU switch to affect the relay condition only when the TS-940S is in the receiver mode.

A change in the AUTO-THRU switch during transmission change the relay only after the TS-940 returns to recieve. (See Fig. 29") Relay protection circuit diagram.)

To operate, the AUTO-THRU switch must be set to the AUTO position. When the ATT switch is pressed, the antenna tuner start pulse (At start pulse) of 40—50 μs, from the digital unit A microprocessor, triggers the AT-B unit timer IC204a (pin 6) generating an approx. 3 second pulse. Through inverter IC208d and gate IC207a, this pulse clocks JK flip-flop IC205a at pin 3 so that the pin 1 output level toggles from how to high (approx. 14 V). A clear pulse, generated by IC208a and b when the power switch is turned on, sets IC205a pin 1 to its initial low level. The IC205a pin 1 high level turns on Q202 and Q201 to switch approx. 15 V to the TRQ terminal (AT ready signal.)

At this AT Ready state, the microprocessor sets tune mode (MODE LED goes out) and, at the same time, the power down circuit for setting the power to 50 W operates (in the Control unit)

If, during the 3 second timer operation, the STBY (or mic. PTT) switch is not set to the SEND position, gate IC207d switches at the trailing edge of the timer and clears IC205a (pin 4). This sets the pin1 output to a low level which switches the TRQ terminal to a low level. When the TRQ terminal goes low, the microprocessor returns the radio to the original mode and the power down circuit is released.

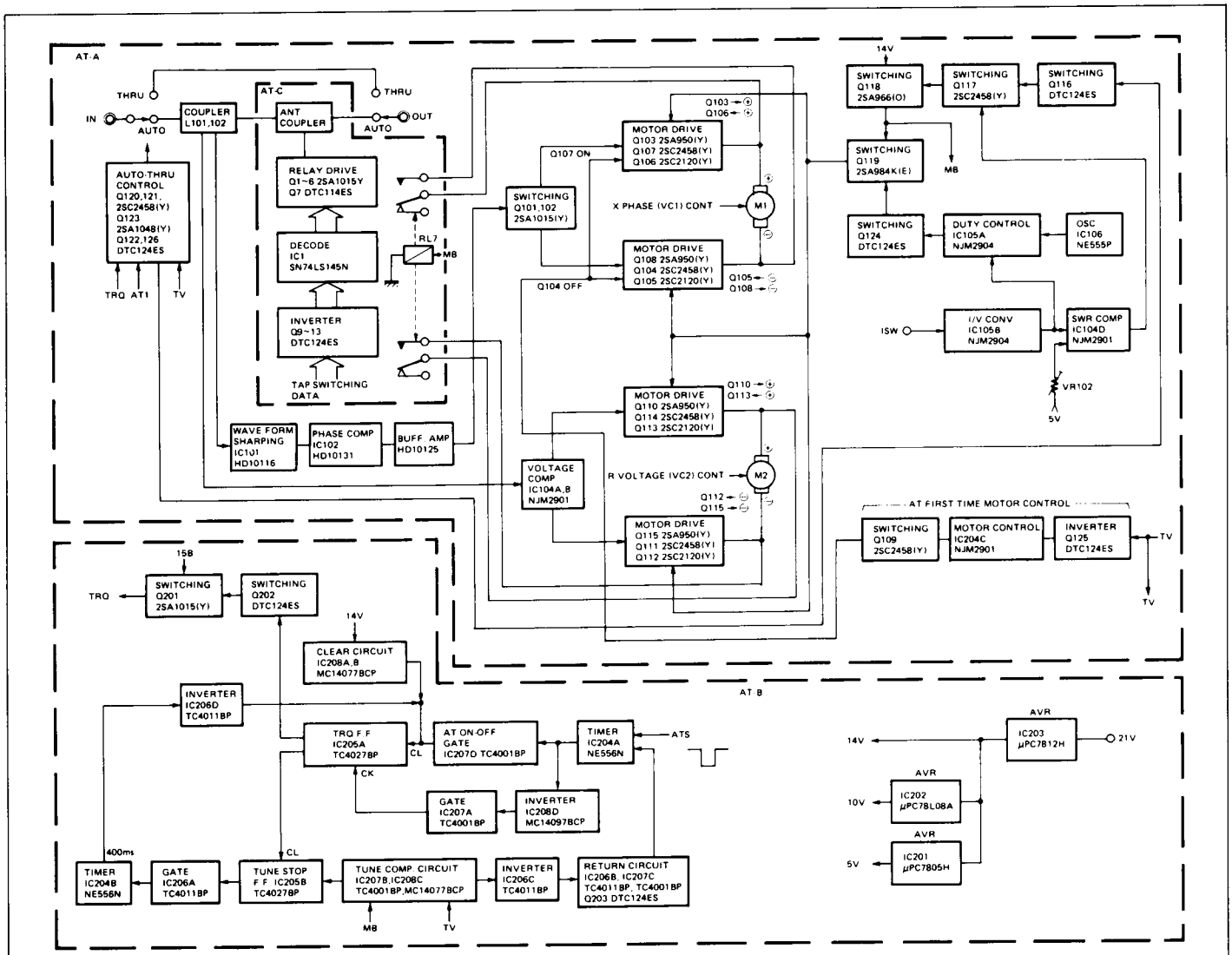
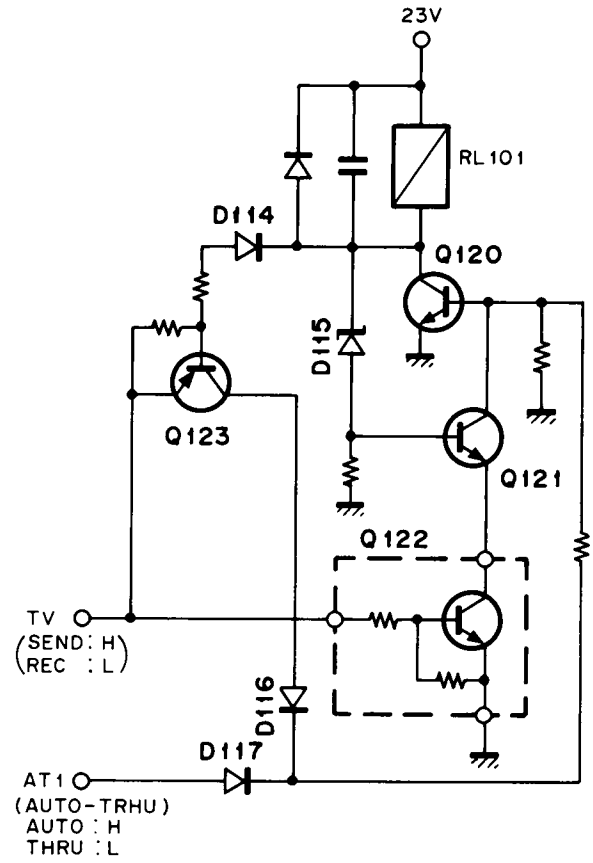


Fig.-28 Antenna tuner unit block diagram

(See Fig. 31 "Timing chart" Ⓐ)
If during this 3 second period, the STBY switch is set to the send position, the TV line goes high at IC207d input pin 13. The gate closes and the IC205a pin 1 output is held high. At that time, the antenna tuner circuit starts tuning. When tuning is finished, the capacitor variable antenna coupler motor stops. This state is monitored at the MB terminal and JK flip-flop: IC205b is toggles to a high level by the gates IC208c and IC207b.
This flip-flop is in the clear state when the AT Ready signal is not generated. Gate IC206a detect the leading edge of this JK flip-flop signal and triggers another timer (IC204b). IC206d detects the trailing edge of this approx. 400 ms pulse and clears IC205a at pin 4.
This starts the sequence of the TRQ terminal switching to a low level, the microprocessor restoring the mode, the power down circuit being released, and completion of tuning. (Fig. 31 Ⓑ) The timer IC204b works as a tuning delay circuit when a momentary rattling of the motor stop relay occurs. If the STBY switch is set to the REC position during the tuning operation, the AT Ready signal is generated for three seconds, The tuning operation is started if the STBY switch is again set the SEND position.
The MB and TV terminals are monitored by IC206c, IC206b and IC207c and when these terminal levels are changed quickly from high to low (when the STBY switch is set to the REC position before the tuning operation is finished), the first timer (IC204a) is again triggered to operate. Therefore, when the STBY switch is held in the REC position for more than 3 seconds, the AT Ready signal goes low and the original mode is returned. (Fig. 30 Ⓒ)
The antenna tuning circuit is explained next. When the AUTO-THRU selector switch is set to the AUTO position, the ATT switch is pressed and the STBY switch is set to the SEND position, transmit power is supplied from the final via the Filter unit. It passes through the current and voltage detecting transformers (L101 and L102) which use toroidal cores. The current and voltage components are applied to IC101 (pins 9 and 13) and waveform shaped. The output signal is applied to IC102 (D type master-slave flip-flop), where the phase is compared. The output of IC102 (pin 14) runs through the buffer IC103 (pins 10 and 15) and switches the emitter coupled circuit Q101 and Q102.
The motor driving circuit Q103—Q108 is operated by this ON-OFF signal, and the variable capacitor (VC1) is rotated forward or backward by the motor M1. The current and voltage components from L101 and L102 are also applied to the voltage comparator IC104a and b (pins 6 and 4), and the output operates the motor driving circuit Q110—Q115 so that the variable capacitor (VC2) is rotated forward or backward by the motor M2 to minimize the amplitude difference.
Therefore, the phase control variable capacitor (VC1) is controlled so that the phases of current and voltage coincide with each other. The voltage control variable capacitor (VC2) is controlled so that the amplitude difference between current and voltage is minimized. (SWR1 with coincidental phases and zero amplitude difference)
VC1 and VC2 are designed to rotate independently. However, since the phase and voltage influence each other, the voltage changes as the phase is changed and the rotations of VC1 and VC2 change accordingly. Also the forward and reflected wave detected in the Filter unit are applied to the Control unit SWR arithmetic circuit, from



REC	Q122 : OFF	Q120 : OFF	RL101 : OFF
	Q121 : OFF	Q123 : OFF	
↓			
AUTO-THRU	Q120 : ON		RL101 : ON
AUTO			
↓			
STBY SW	Q122 : OFF	Q123 : ON	
SEND	Q121 : OFF	Q120 : ON	RL101 : ON
↓	(Relay protection operation)		
AUTO-THRU	Q122 : OFF	Q123 : ON	
THRU	Q121 : OFF	Q120 : ON	RL101 : ON
↓			
STBY SW	Q122 : OFF	Q123 : OFF	
REC	Q121 : OFF	Q120 : OFF	RL101 : OFF
↓			
STBY SW	Q122 : ON	Q123 : OFF	
SEND	Q121 : ON	Q120 : OFF	RL101 : OFF
↓	(Relay protection operation)		
AUTO-THRU	Q122 : ON	Q123 : OFF	RL101 : OFF
AUTO	Q121 : ON	Q120 : OFF	

Fig.-29 .Relay protection circuit diagram

which they are sent to the AT-A unit ISW terminal as an SWR signal.
This SWR signal is in the current mode and is converted in the AT-A unit (IC105b) to make an SWR signal of voltage mode. The signal is then applied to the SWR comparator IC104d (pin 9). The voltage equivalent to SWR 1.2: 1 is applied to the reference voltage terminal (IC104d, pin 8) through the semi-fixed resistor. Thus, when the SWR is greater than 1.2: 1 the IC104d output terminal (pin 14) is high and switch Q118 turns the motor voltage supply on.
The motor driving circuit is actuated. When the SWR is lowered to below 1.2: 1 the output terminal (pin 14) of IC104d switches to low, and the switching transistors Q117 and Q118 turn off (motor stop signal), the motor driving circuit turns off and the motor stops.
High motor speed is desired for fast antenna tuning. However, this can cause the match point of SWR less than 1.2:1 to be overrun due to increased inertia, the capacitors reversing and tuning past the match point continuously. A slower speed prolongs the operation. Therefore, the TS-940S uses the following method to vary the speed with the SWR: That is, faster with an SWR increase, and slower with an SWR reduction.
The SWR signal sent to the SWR comparator IC104d is also sent to the variable duty motor voltage circuit (IC105a,

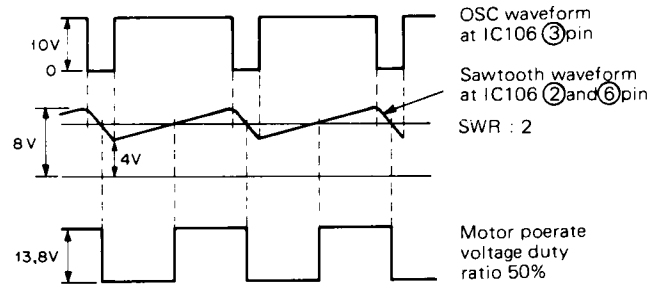
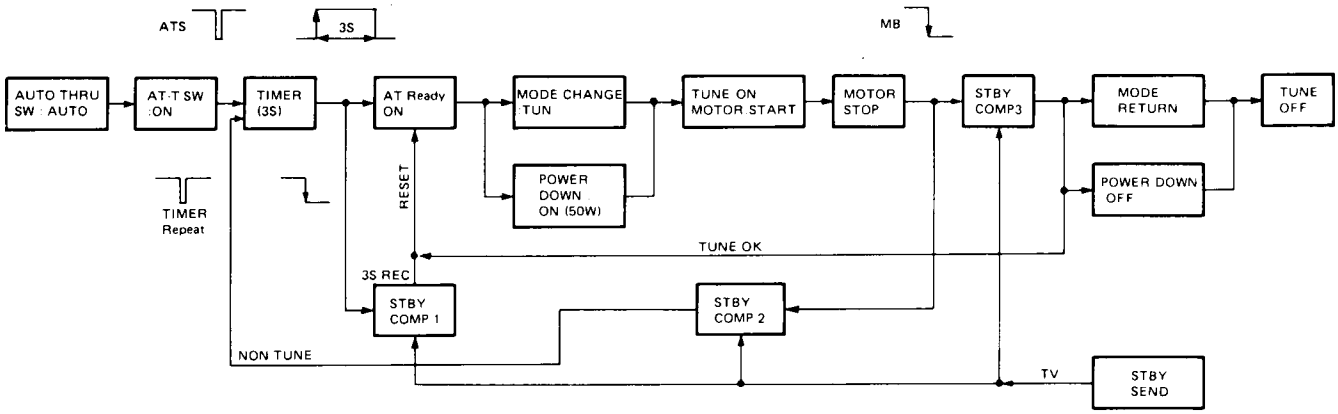


Fig.-30 Tuning motor speed control



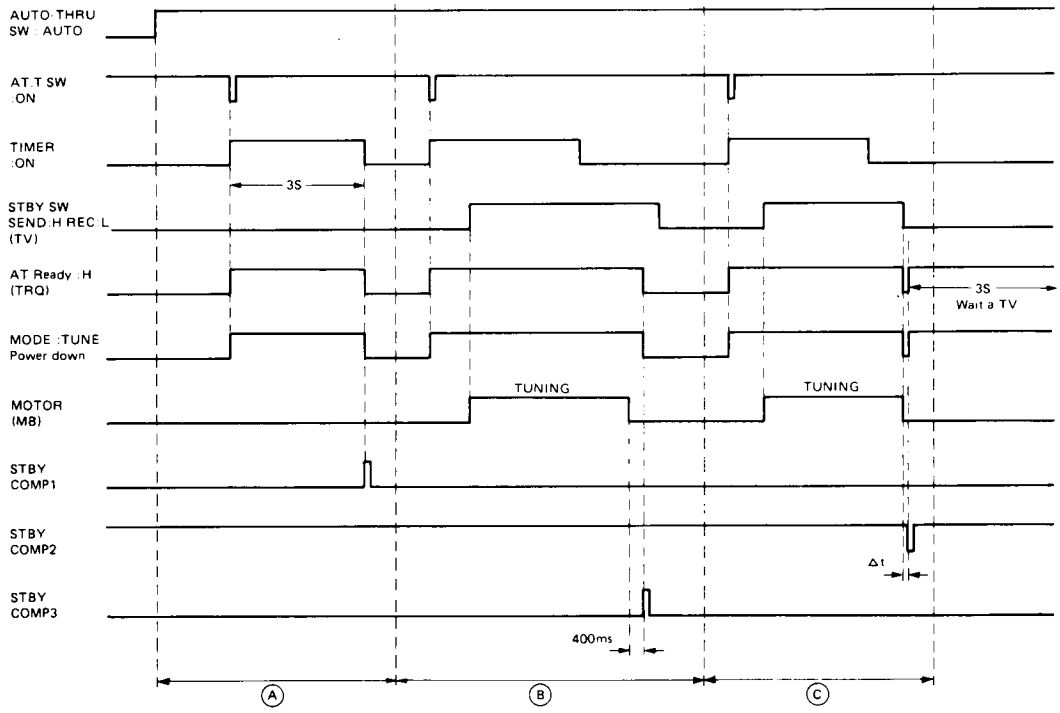


Fig.-31 Antenna tuner timing chart

pin 5). The variable duty circuit uses timer IC106 as a triangle wave oscillator andits output is applied comparator (IC105a, pin 6) to vary the duty of the output pulse (pin 7). (Fig. 30)

Therefore, when the SWR is higher than 5:1, the motor driving voltage is at 100% duty, and the motor rotates at high speed. When the SWR value is lowered to 2:1, the duty ratio is also lowered (50%) and the motor speed becomes low. As soon as the SWR lowers to below 1.2:1 and the motor driving voltage disappears, the motor brake circuit RL7 operates to immediately stop the motor rotation. The antenna coupler of the TS-940 is a T type and the tap positions from 1.8 MHz to 30 MHz are switched by eight relays (RL1—6 and 8). The tap switching data is given in Table 6.

BAND	WRC	AT0	AT1	AT2	AT3	RL-1	RL-2	RL-3	RL-4	RL-5	RL-6	RL-8
1.8	0	1	0	1	1	○	○	○	○			
3.5	0	0	0	1	1		○	○	○			
7	0	0	1	0	1			○	○			
10	1	1	0	0	1				○			
14	0	0	0	0	1							
18	1	1	1	1	0					○		
21	0	1	1	1	0					○		
24.5	1	0	1	1	0						○	
28	0	0	1	1	0						○	○

Table-6 Antenna tuner band selection data

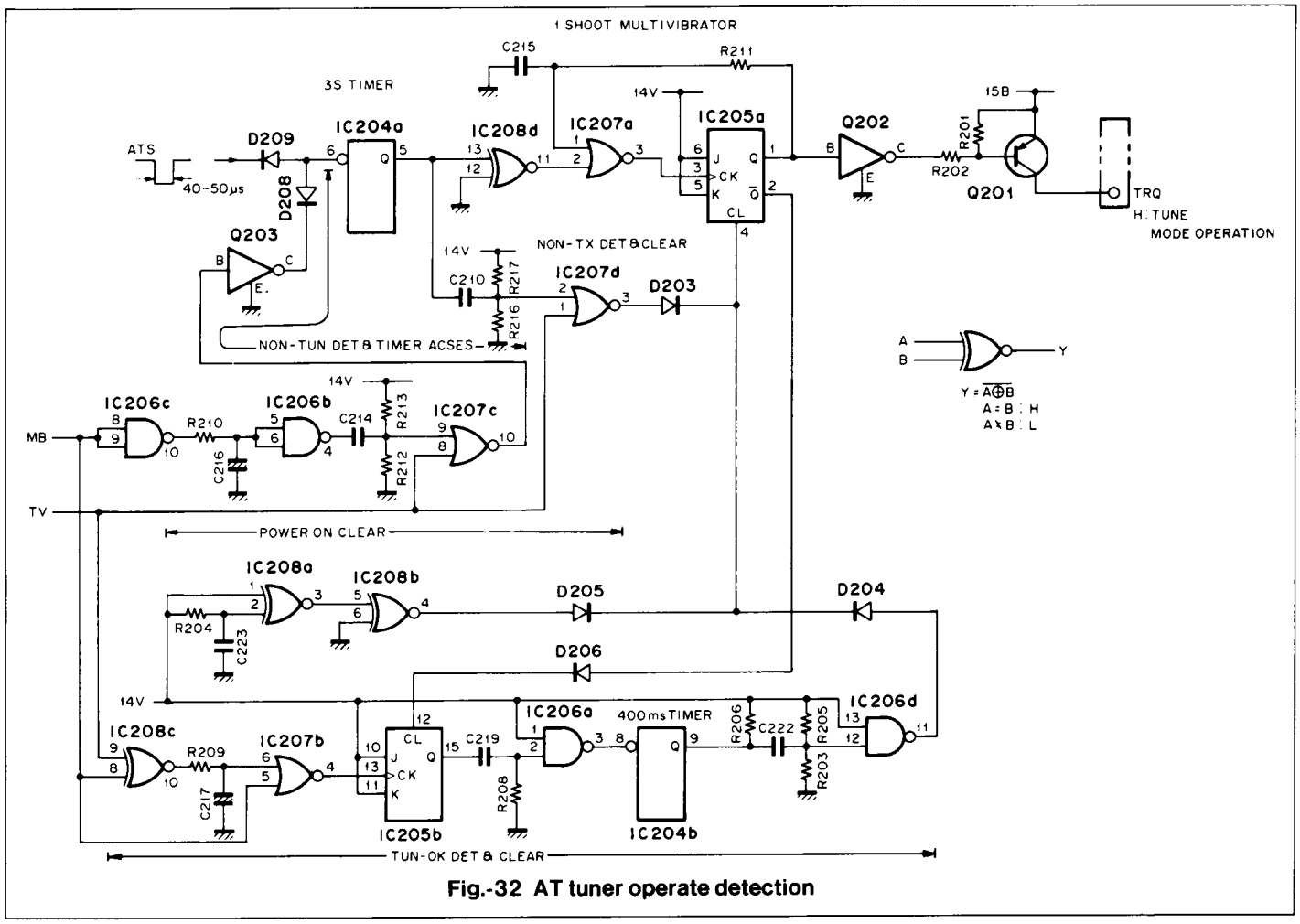


Fig.-32 AT tuner operate detection

• Final amplifier circuit

The TS-940S transmitter final amplifier stage is an improved version of the transistorized circuits used in the TRIO-KENWOOD HF transceivers. With transistorized final stages, important considerations include improving electrical characteristics such as gain, linearity (IMD, or intermodulation distortion), and bandwidth, and improving transistor reliability under adverse conditions such as current overload, overdrive, mismatched loss and overheating.

Generally, the low input impedance of high power transistors makes them vulnerable to thermal runaway resulting from excess load variations, elevated temperatures, or momentary current excursions due to parastic oscillation, etc.

Increasing the emitter resistance of an H.F. high power transistor tends to reduce its susceptability to breakdown but degrades certain electrical characteristics such as power gain and IMD.Conversely, increasing the power gain increases susceptability to failure.

Currently, almost all commercially available solid state HF transceivers use 12 V transistors in their final amplifier stage. However, the TS-940S uses 28 V transistors to improve both electrical performance and reliability. The output characteristic of the TS-940S is shown in Figure 33.

A transistor's IMD indicates its linearity. Generally, linearity of a transistor amplifier is represented in terms of its 3rd order IMD, and 3rd order IMD is included in the transistors specifications. In practice, however, a good 3rd order IMD figure is not a sufficient indication of performance of a transmitter's final stage. This is because poor 5th, 7th, 9th and/or 11th order IMDs adversely affect quality of the transmitted signal; that is, the spectrum of the transmitted signal is widely spread around its frequency. This may cause interference to other signals. The spectrum of a two-tone signal power amplified by a stage with such IMD is shown in Figure 34. The final transistors used in the TS-940S have lower 3rd, 5th, 7th and 11th order IMDs than do conventional final transistors. Figure 35 shows the TS-940S IMD characteristic. The transistors used in the final amplifier are Motorola MRF422s (with a Vc of 28 V). These are manufacture on larger substrates than is the case with other 100 W transistors and have superior linearity. Table 7 shows the maximum ratings for the MRF422. Figure 36 shows MRF422 output power versus input power and 3rd and 5th order IMD characteristics.

However, if transistors with high gain and good IMD characteristics are used, driver stage quality may become an apparent problem. If the IMD characteristics of the driver transistors are poor, the high performance of the final transistors will be wasted. Since transistorized wideband HF amplifiers have no interstage tuning circuits, matching errors between the driver output and the final input will degrade the IMD characteristic. Furthermore, poor matching can result in abnormal temperature excursions in the coupling circuit and unwanted oscillation.

The TS-940S uses push-pull MRF-485s operating at a Vc of 28 V with good linearity. As a result, 3rd IMD level of −50 dB and a 5 th IMD level of −60 dB is obtained for the driver stage output. Table 7 shows the maximum ratings of the MRF485 and Figure 37 shows output power versus input power and IMD characteristics. The final bias circuit uses an IC regulator (MC1723CL) and a bias drive transistor to supply stable bias voltage. To reduce IMD and provide stable operation, separate NFB negative feed back circuits are provided for the pre-driver, driver and final stage amplifiers.

Yet another reason for using 28 V transistors in the final stage is that they provide higher reliability. As shown in Table 7, these transistors have a maximum dissipation (collector power rating) of 290 W. And finally, the MRF485 is more resistant to high VSWR and parasitic oscillation than 12 V transistors.

One of the most likely causes of final transistor destruction is that a large current can be concentrated in one area of the substrate due to load variation, overdrive, or parastic oscillation, this results in deposition of bonding material on the emitter, causing a short circuit between the collector and emitter. To obtain 100 W of output power, a collector current of 14 to 16 A (7 to 8 A for each transistor in a push-pull configuration) flows through the final stage when 12 V transistors are used; however, with 28 V transistors, a

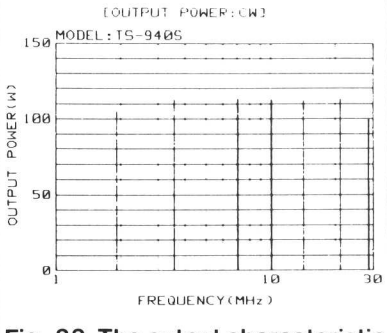


Fig.-33 The output characteristic of the TS-940S

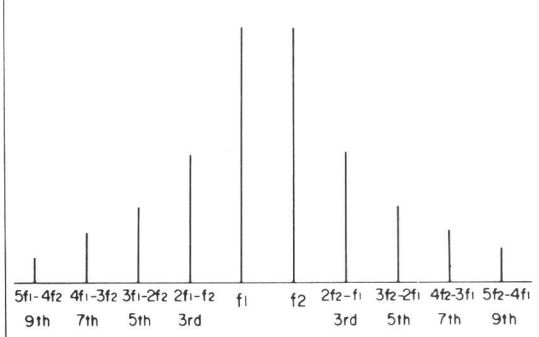


Fig.-34 Output spectrum

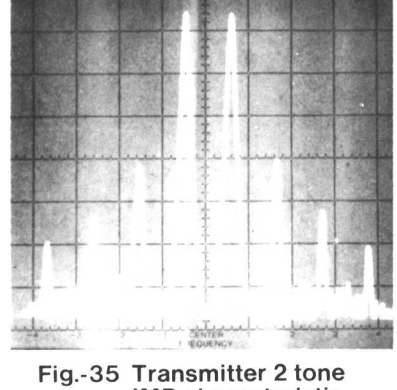


Fig.-35 Transmitter 2 tone IMD characteristic

Table-7 The maximum rating of the MRF422

Item	V_{CEO}	V_{CBO}	V_{EBO}	I_C	P_C	T_{Vstg}	$R_{\theta jc}$
Unit	V	V	V	A	W	°C	°C/W
Rated value	40	85	3.0	20	290	−65～+200	0.7
Reference value	25	45	4.0	20	250	−65～+200	0.7

collector current of only 7 to 8 A (3.5 to 4 A for each) flows into the final stage. Therefore, there is less current flowing through the bonding material holding the transistor together. Further, the collector resistance of 28 V transistors is larger than of 12 V transistors because of their smaller collector current. This means that they exhibit greater resistant to variations in load impedance.

The TS-940S final incorporates pre-driver (2SC2075), driver (MRF485 × 2) and final (MRF422 × 2) and final (MRF422 × 2) stages and power amplifies signal of from 1.8 to 29.7 MHz. The gain of the final stage is 40 dB. A varistor is mounted on each pre-driver and driver transistor for bias circuit temperature compensation. The final stage utilizes the diode characteristic between a transistor base and emitter to detect the temperature of the heat sink and compensate for thermal variations. To stabilize the final stage, laminated chip capacitors are used as coupling and bypass capacitors for the power supply lines. This conserves space, and prevents matching errors resulting from capacitor lead inductance, collector efficiency degradation resulting from capacitor heating, and parastic oscillation which may occur when conventional ceramic disc capacitors or dipped mica capacitors are used. The TS-940S temperature protection circuit detects the heat sink temperature, rather than the output transformer core temperature.

Although the TS-940S final stage has ample resistance to breakdown, a cooling fan is provided and operates to protect the final transistors if the heat sink temperature reaches a certain level. Additionally, the temperature protection circuit forcibly switches the transceiver from transmission to reception if the heat sink temperature exceeds a given level. The circuit uses a thermistor affixed to the Final unit to detect the temperature. The TS-940S is also equipped with a VSWR protection circuit which decreases the drive power when the VSWR deteriorates (to 3:1 or worse) and an overcurrent protection circuit which decreases the drive power if excessive current flows in the final stage.

Even order harmonics are suppressed to a reasonable level by the push-pull amplifier cirucit used in final stage, but odd harmonics remain. The odd harmonics are removed by the low pass filters following the Final unit. There are 7 low pass filters which cover the 1.5 to 30 MHz range in 7 band segments. The use of relays to select these low pass filters greatly decreases the number of coaxial cables for wiring and makes it possible to use electronic push switches for band selection.

The 3-bit data from the Digital unit is converted by a decoder (MB74LS42M) to select one of the 7 low pass

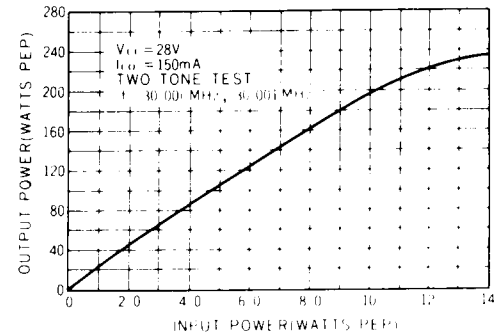


Fig.-36 (a) MRF422 output power versus input power

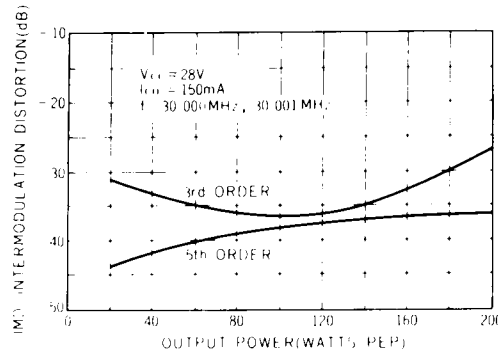


Fig.-36 (b) MRF422 intermodulation distortion versus output power

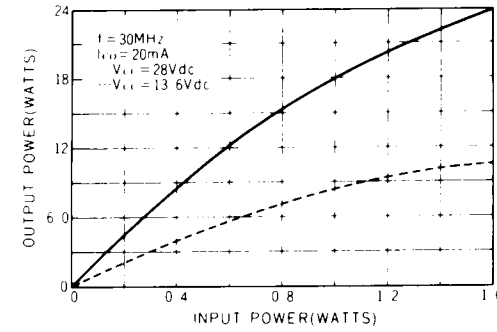


Fig.-37 (a) MRF485 output power versus input power

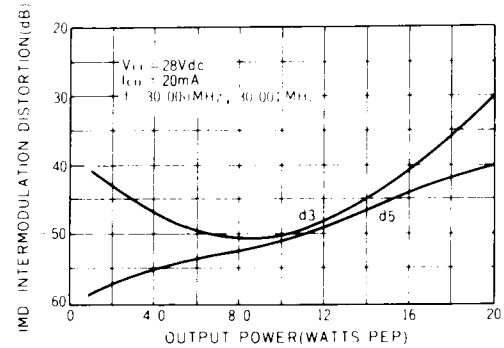


Fig.-37 (b) MRF485 intermodulation distortion versus output power

Table-8 The maximum rating of the MRF485

Item	V_{CEO}	V_{CBO}	V_{EBO}	I_C	P_C	TV_{stg}	$R_{\theta jc}$
Unit	V	V	V	A	W	°C	°C/W
Rated value	35	65	4.0	1.0	30	−65～+150	3.33

filters. Table 9 shows the relationship between the band segments and the 3-bit data. The passband of these filters has a flat impedance characteristic. The 18 MHz band shares one with the 21 MHz band, and the 24.5 MHz band shares one with the 28 MHz band. As shown in Figure 39 the attenuation points of each m-derived filter are set to frequencies which are twice (2fmin) and three times (3fmin) the frequency at the low end of the passband. Each filter is designed so that the Amateur band is near the cutoff frequency. Thus, sufficient attenuation of harmonics is obtained.

Figure 40 shows the harmonic and spurious signal output of the TS-940S during transmission on the 14 MHz band. The Filter unit includes not only the low-pass filters, but also a VSWR detection circuit (which uses toroidal cores) and is located between the filters and antenna (or the antenna tuner). This VSWR detection circuit uniformly detects forward and reflected waves over the 1.8 to 30 MHz range, and delivers them to the Signal unit as VSF and VSR.

Band	L_0, L_1, L_2
1.8~2.0	1 1 0
3.5~4.0	0 0 1
7.0~7.5 10.0~10.5	1 0 0
14.0~14.5	0 1 0
18.0~18.5 21.0~21.5	0 0 0
28~29.7	0 1 1

Table-9 The relationship between the band segments and the 3-bit data

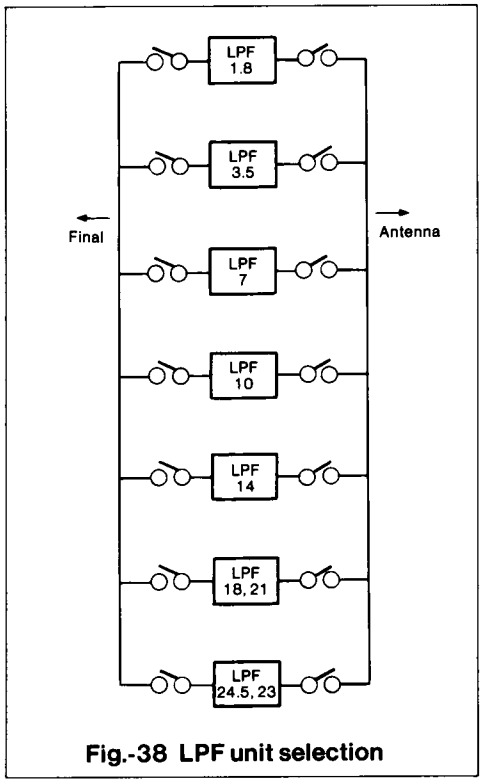


Fig.-38 LPF unit selection

Final Amplifier Circuit

- **Final cooling fan driving circuit (provided on the Filter unit)**

First, the final heat sink temperature is detected by thermistor TH1 provided on the Final unit. If the heat sink temperature rises to approx. 50°C. Comparator IC1A functions (high level) to start cooling fan operation and Q7 turns on. At this time, the temperature protection comparator IC1B is low level, and Q8 is on. Therefore, approx. 10 V (D11: Zener voltage 5.1 V, D13: Zener voltage 4.3 V, Q8: VCF SAT 0.1—0.3 V) appears at the MOT terminal and drives the fan motor.
This circuit is designed with hysteresis so the fan stops when the Final heat sink temperature fails to approx. 45°C.

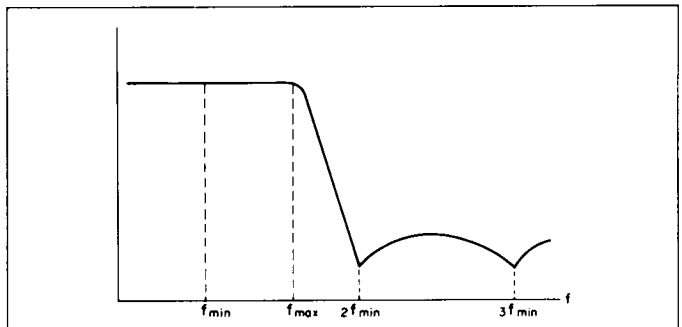


Fig.-39 The attenuation points of each M-derived filter

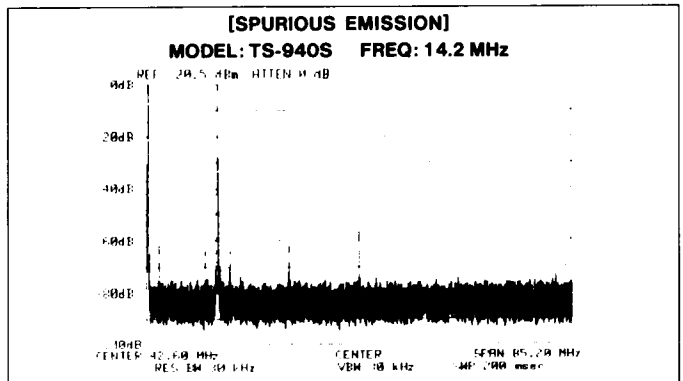


Fig.-40 Spurious emission

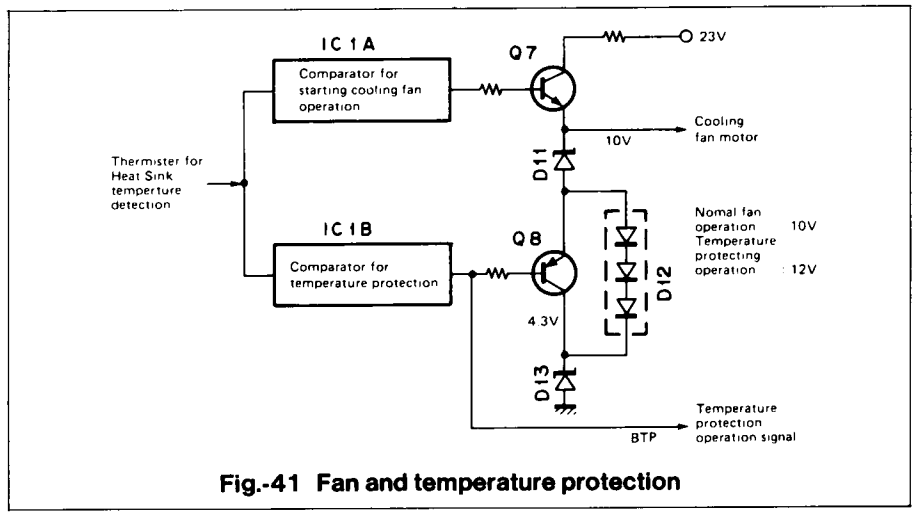


Fig.-41 Fan and temperature protection

- **Final temperature protection circuit (provided on the Filter unit)**

If the Final heat sink temperature rises to approx. 90°C, temperature protection comparator IC1B on the Filter unit switches from low to high level, and Q8 turns off. Therefore, approx. 12 V, the total voltage of zener diode D11, variable resistor D12 (1.7 V) and zener diode D13, is generated at the MOT terminal, the motor speed is increased and the final heat sink is cooled more rapidly.

At the same time, the high level signal from IC1B is sent to the Control unit via the BTP terminal to stop transmission and forces the set into the receive mode.

When the sink temperature falls to approx. 65—70°C, this circuit is released and transmit mode is again enabled. Thereafter, the fan is driven by the cooling fan driving circuit until the heat sink temperature further lowers to approx. 45°C.

DIGITAL CIRCUIT

As shown by the block diagram in Fig. 42, the digital control section is the heart of the TS-940S and controls all its units. The digital section consists of the Digital A unit , Digital B unit, Digital C unit, DC-DC unit, Switch unit, Main Encoder ass'y RIT Encoder unit and Keyboard ass'y, a total of 8 units. The TS-940S is capable of versatile functions, using the latest microprocessor technology. Consequently, about 50 data for the input and about 70 data for the output are handled, requiring an input/output function with much greater capacity than conventional models. To meet this requirement, the microprocessor has an 8-bit multitip construction designed to minimize the number of ICs used: the input/output uses a series of three I/O control ICs 8255 and three LC7800 are used for multiplexing the input signal for the input data.

Separate descriptions for each unit now follow.

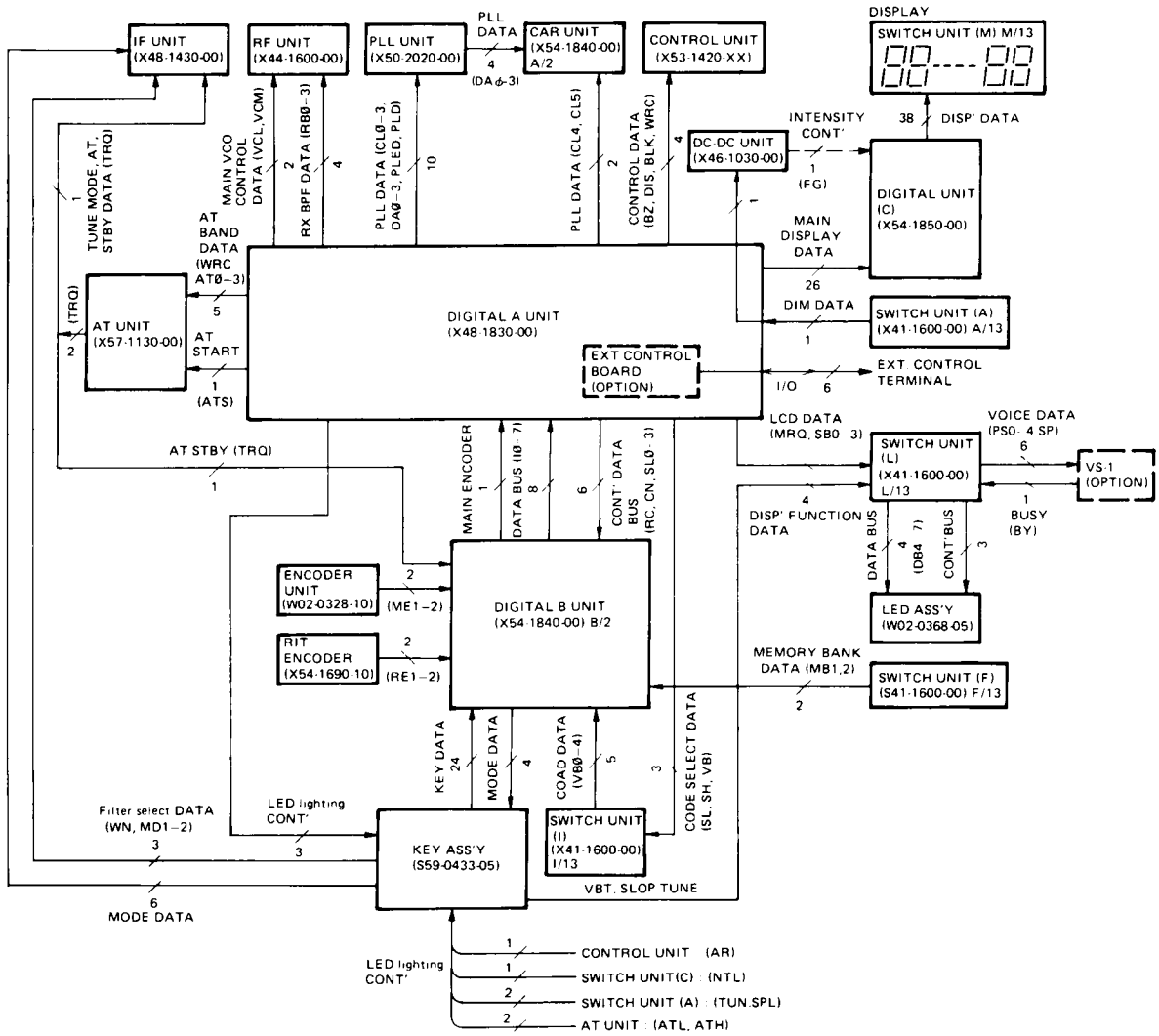


Fig.-42 Digital control block diagram

- **Digital B unit**

This unit performs multiplexing of the input, waveform shaping of encoder pulses and detection of AT IN/Through. The input SW data in the Digital B unit goes to ICs 109, 110 and 111, selected by the port select signal from the Digital A unit, and supplied to the Digital A unit.

Two optical encoders, for the main VFO and for RIT, are provided. Each converts one dial rotation into pulses and shapes the waveform. In the main encoder, 250

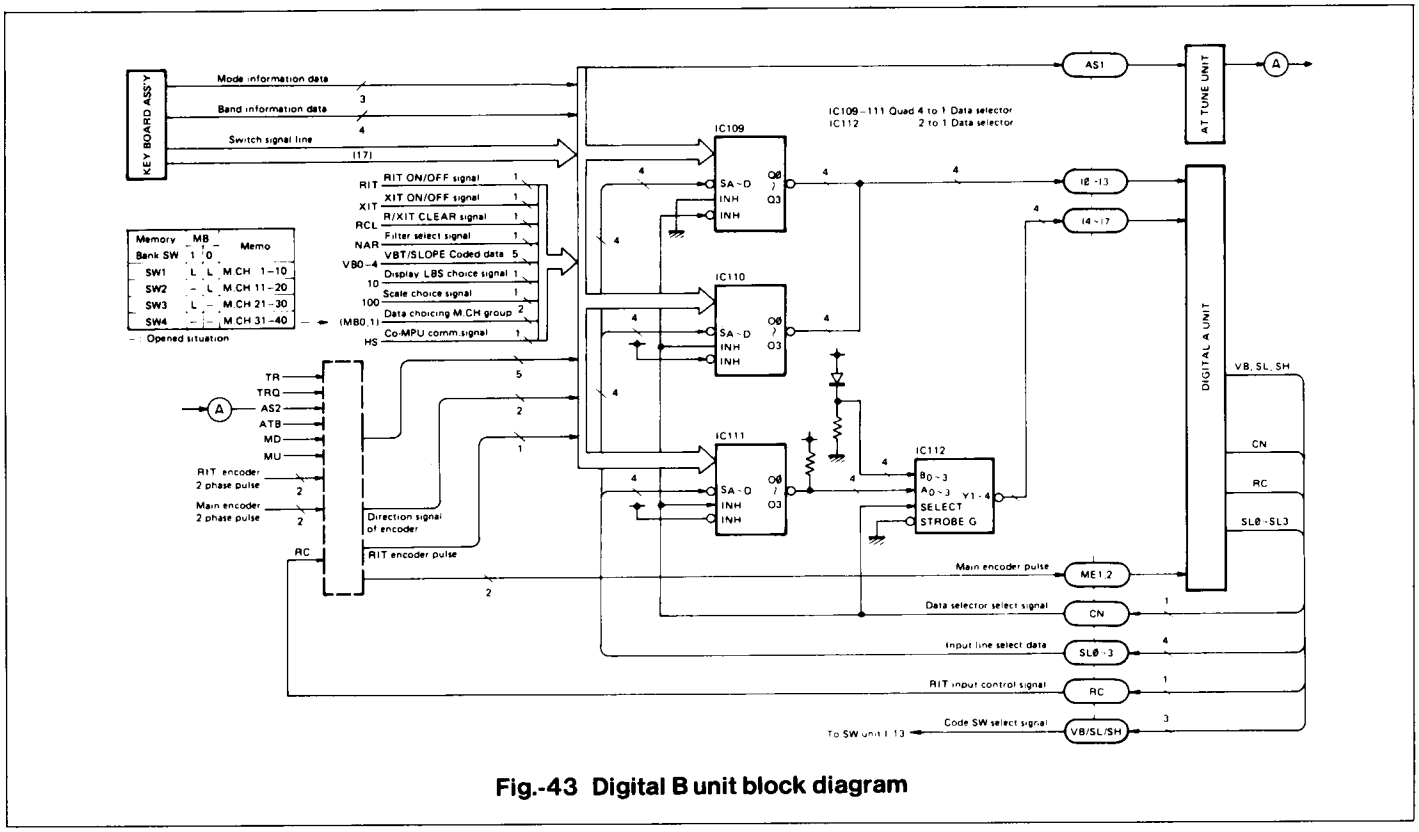


Fig.-43 Digital B unit block diagram

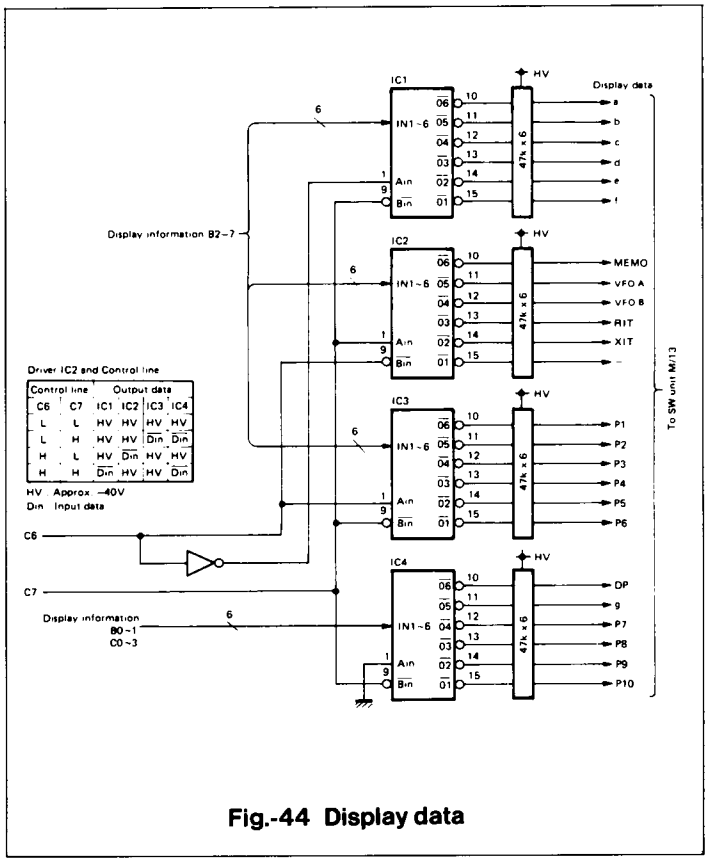


Fig.-44 Display data

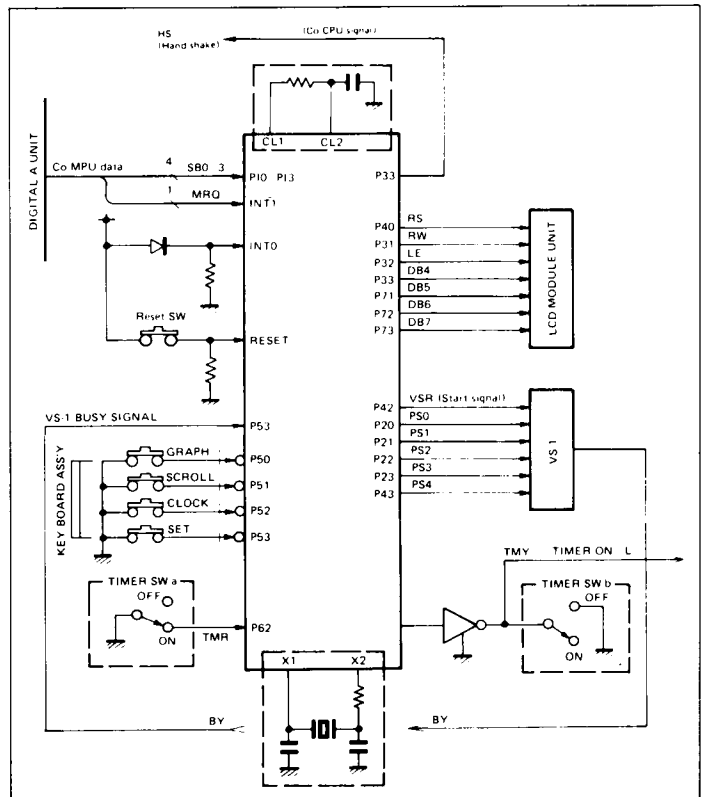


Fig.-45 Co-MPU data

pulses are converted to 1000 pulses; one rotation corresponds to the encoder signal of 10 kHz with a resolution of 10 Hz. In the fast tuning mode with more than 2 or 3 rotations per second, the variation of frequency progressively increases thanks to a "speed-up" function. (Main encoder ICs 101, 102, 103, 2/4, IC7. RIT encoder ICs 104, 105, 106, 2/4, 107.)

- **Digital C unit**
  This unit is used to drive the fluorescent display tube along with the analog dial scale.
  As the display data supplied from the Digital A unit has TTL level voltage, the display tube cannot be directly driven. To light the display tube, the drive voltages (heater voltage and display tube drive voltage) from the DC-DC unit are used together with the control data. The display data consists of time-division multiplexing of three data; the 7-segment data for digits, indicator data such as VFOA, MEMO, RIT, etc., and analog dial scale data. These data are also separated at this occasion.

- **DC-DC unit**
  This unit generates the filament voltage for driving the fluorescent tube and the negative high voltage.
  The 21 V voltage from the Control unit is converted into −40 V by the DC-DC converter.

- **Main Encoder ass'y and RIT Encoder unit**
  These optical encoders consisting of photoetched disks, and a photo-interrupter, both output 2-phase pulses with a phase difference of 90°. The direction of rotation is judged from this phase difference.

- **Switch unit**
  Description will be given for the circuitry around the liquid crystal display (hereafter abbreviated LCD.)
  The TS-940S uses a dual-display system using a newly-developed dot matrix LCD, in addition to a fluorescent tube: in addition to the operating frequency, the display can be switched for the frequency and mode of the alternate VFO, frequencies and modes of the memory channels, bandwidth of interference suppression systems, and clock/timer display. The LCD ass'y consists of the dot matrix LCD and drive IC and is driven from the 4 bit/8 bit data bus. A new 4 bit microprocessor is used for this model and interfacing to the drive IC is performed in 4 bits. The 4 bit microprocessor performs operations such as switching of the display mode, setting of the clock and timer, switching of various displays, data communication with the main microprocessor, outputting of the audio data output from the optional voice synthesizer unit (VS-1), etc.

- **Digital A unit**
  This unit is the control center of units 1) to 5) and for data communications between them. It has a multitip 8-bit construction and the CPU uses a Z-80 operated at a clock rate of 2.5 MHz.
  The main memory has a large 8-kByte capacity and the 2-kByte RAM backs up several data including the 40-ch memory data, VFO data, RIT frequency, and ON/OFF condition using a lithium battery. The backup timing is controlled by the system reset IC (IC20, RST5184), which interrupts execution at the instant the supply voltage falls below 4.2 V to activate the backup mode. (Fig. 46)
  The I/O system uses the memory-mapped I/O system: the 1st 8255 outputs the display data: the 2nd 8255 outputs the AT band data, LPF band data, data outputs for the three main loop PLL ICs and data outputs for the two carrier PLL ICs; and the 3rd 8255 inputs the switch data and outputs the switch data output and the outputs for the LEDs.

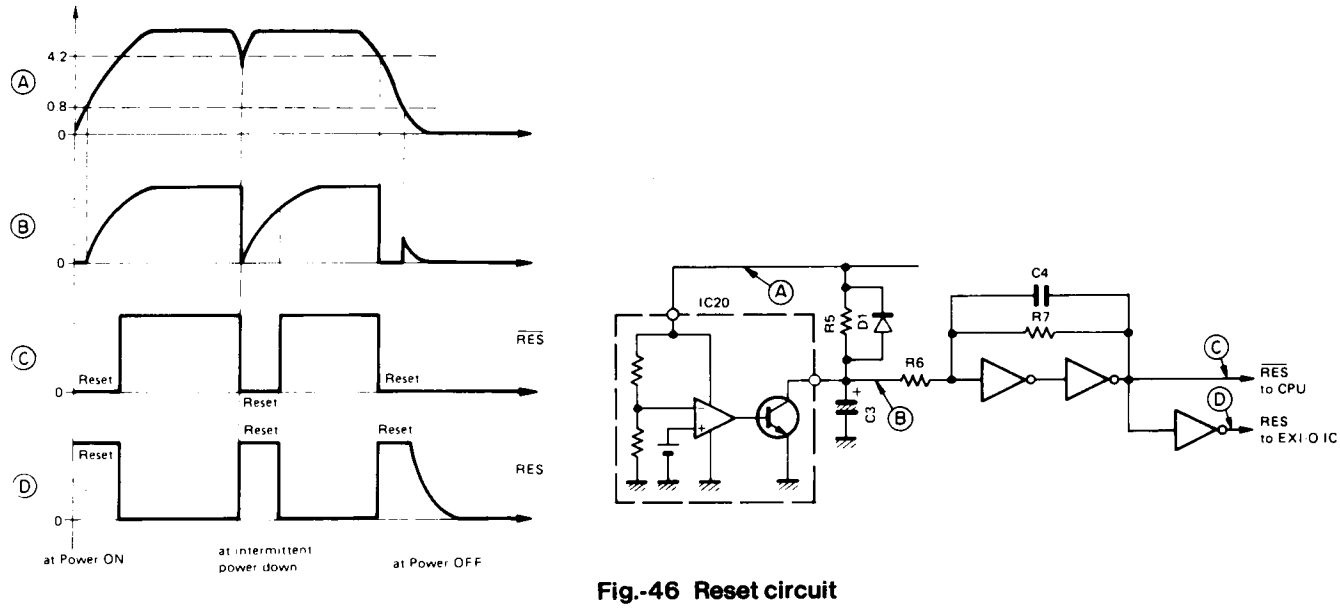


Fig.-46 Reset circuit

The terminals for the RX bandpass data output and LCD-use submicroprocessor data output are also provided by using the latch output method.

For the antenna tuner standby operation, the AT In/Through condition (and also the presence of an AT in export models) is judged when the ATT SW is pressed: when the condition is OK, the AT standby pulse (active low, about 100 μs) is output to the AT unit, which then stands by and sends back the AT Ready signal.

The microprocessor detects this Ready signal, automatically changes the mode to TUN. The mode changes back to the previous mode when tuning is complete. The AT coupler is always supplied with current band data for band switching. (Fig. 49) The standby signal is also supplied to the submicroprocessor so that the AT standby message is also output on the sub display. Other circuits used include the mode announce circuit (which indicates the switching of mode by CW codes) the PLL noise blanking circuit which suppresses noise during PLL reset pulse, and the "beep" sound control circuit which indicates when the various tactile switches are pressed.

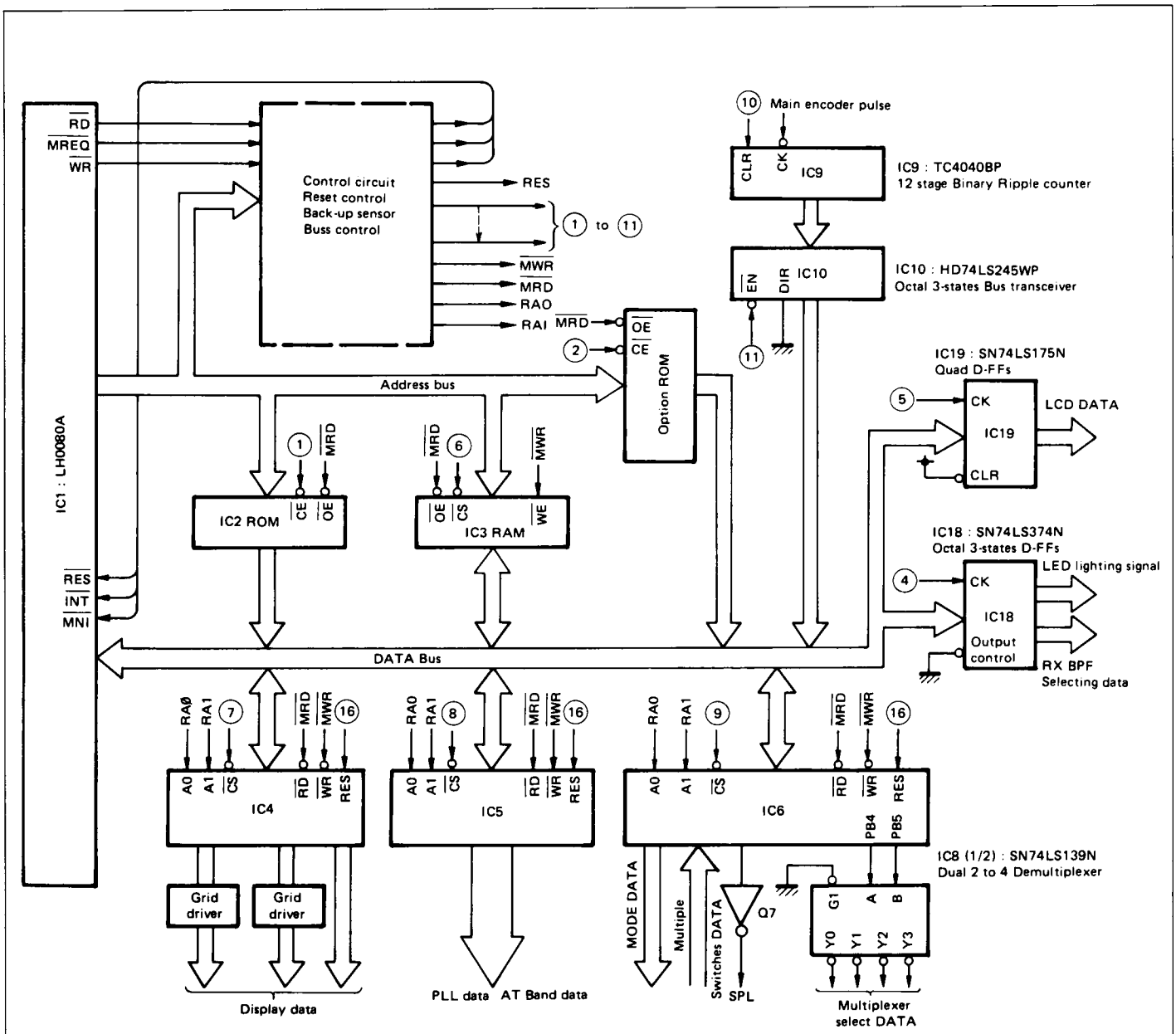


Fig.-47 Digital A unit block diagram

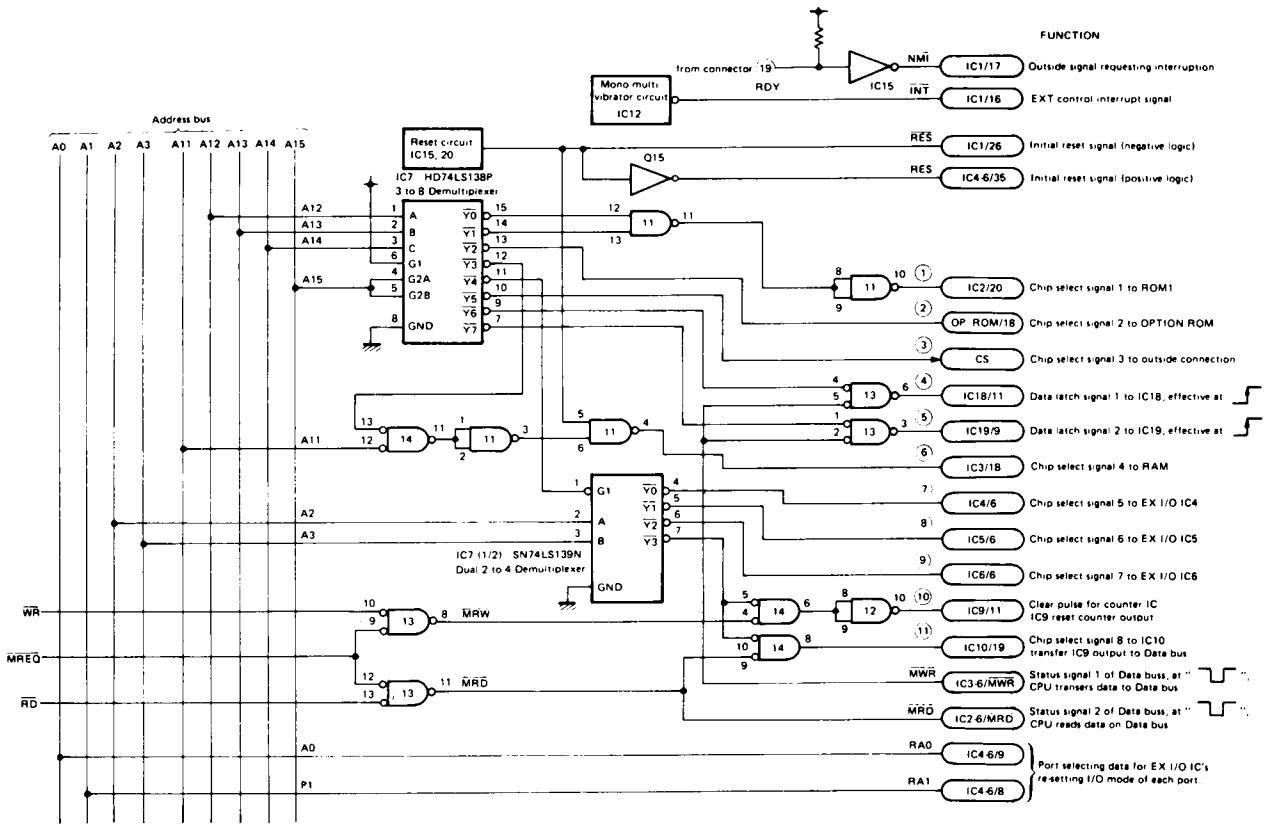


Fig.-48 Digital A unit control logic diagram

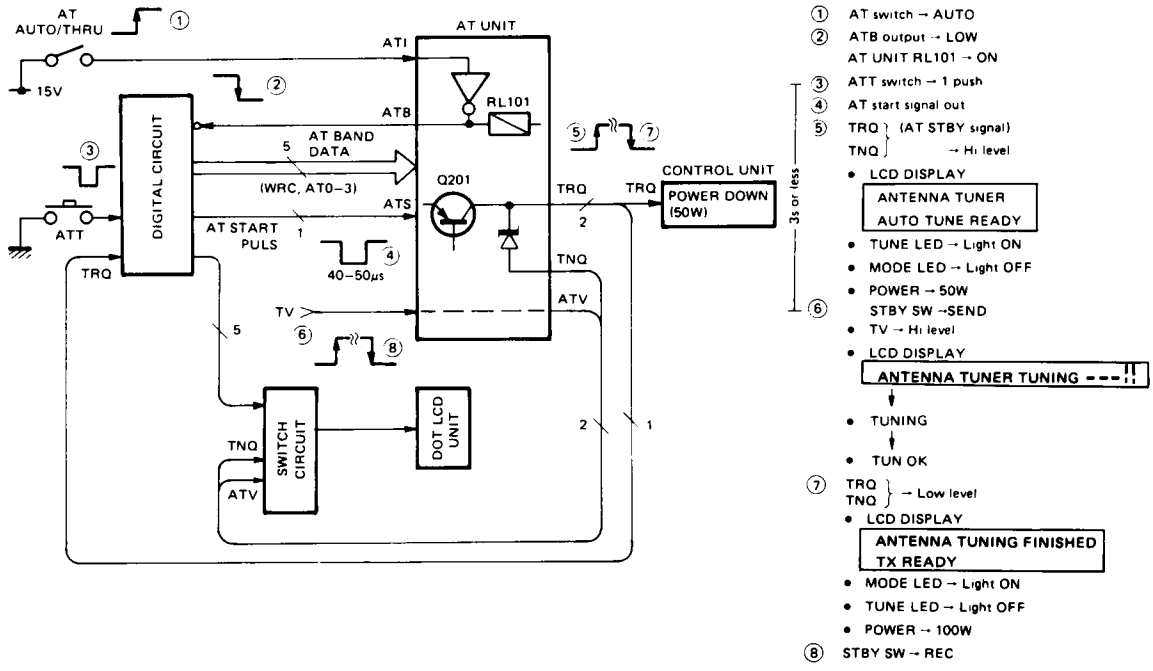
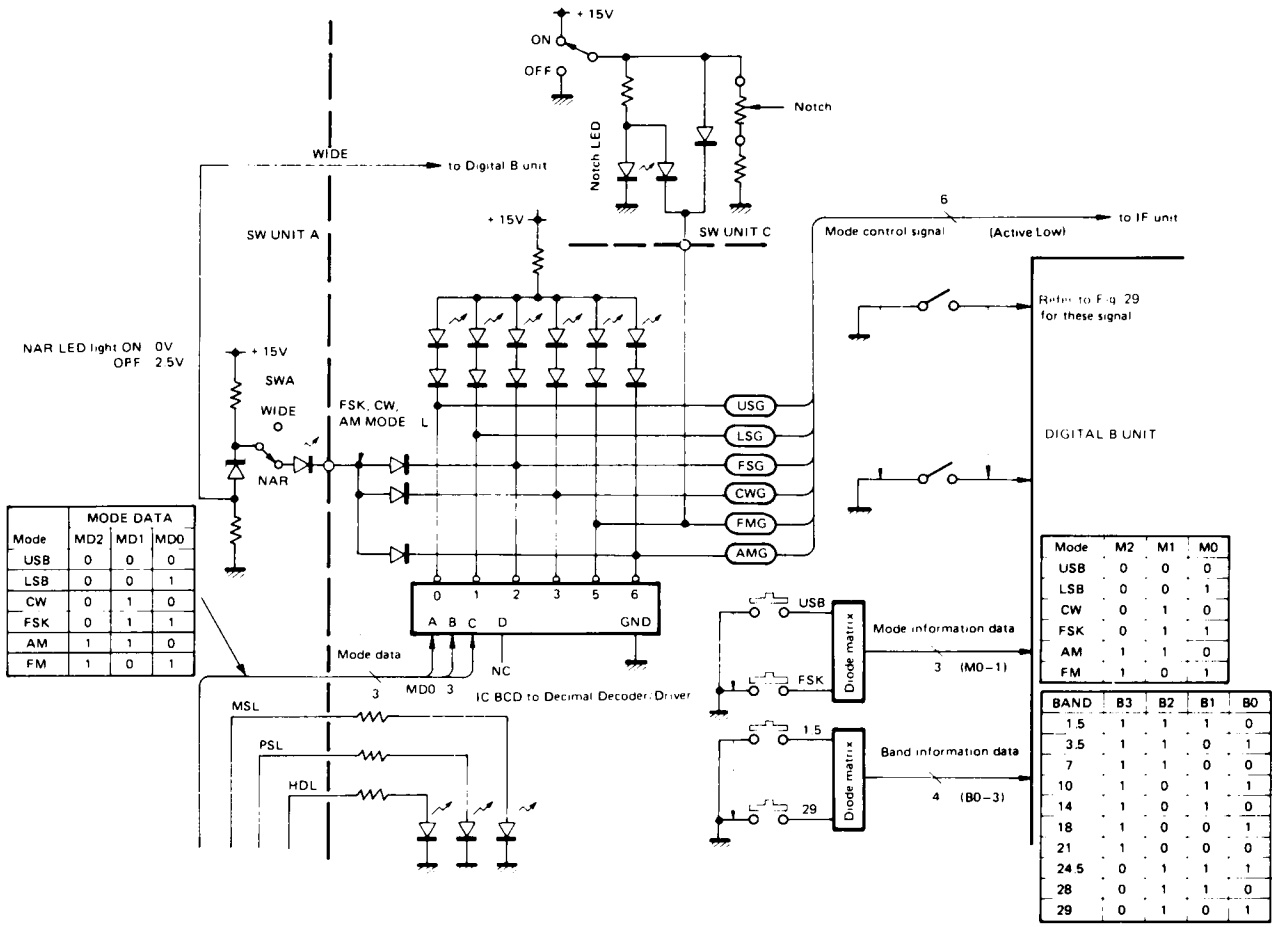


Fig.-49 Power control and AT unit



Mode	MODE DATA MD2	MD1	MD0
USB	0	0	0
LSB	0	0	1
CW	0	1	0
FSK	0	1	1
AM	1	1	0
FM	1	0	1

Mode	M2	M1	M0
USB	0	0	0
LSB	0	0	1
CW	0	1	0
FSK	0	1	1
AM	1	1	0
FM	1	0	1

BAND	B3	B2	B1	B0
1.5	1	1	1	0
3.5	1	1	0	1
7	1	1	0	0
10	1	0	1	1
14	1	0	1	0
18	1	0	0	1
21	1	0	0	0
24.5	0	1	1	1
28	0	1	1	0
29	0	1	0	1

Fig.-50 Keyboard assy

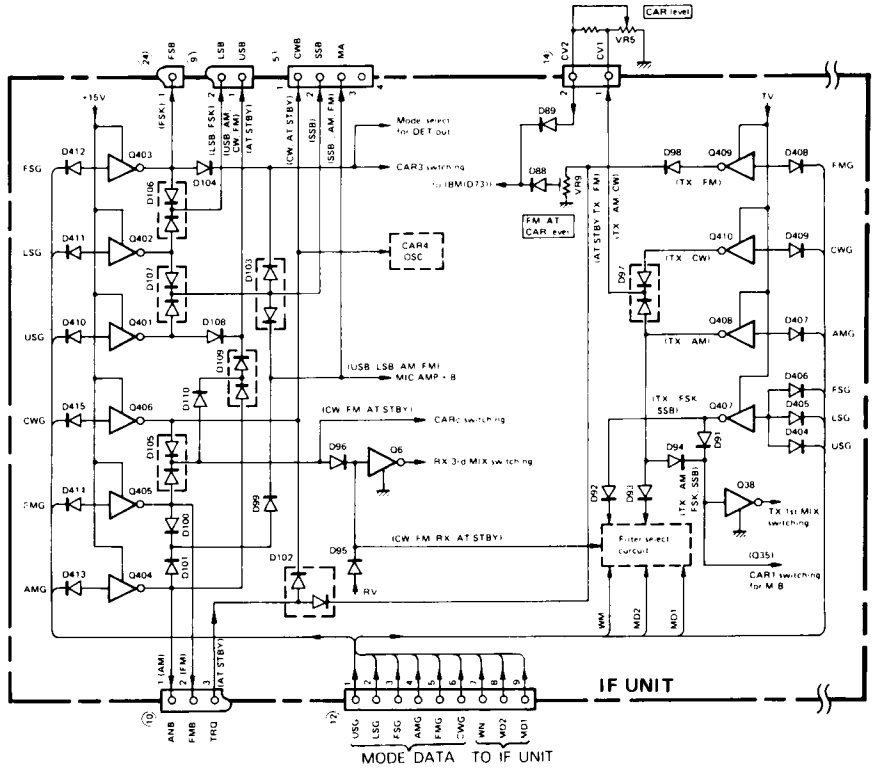


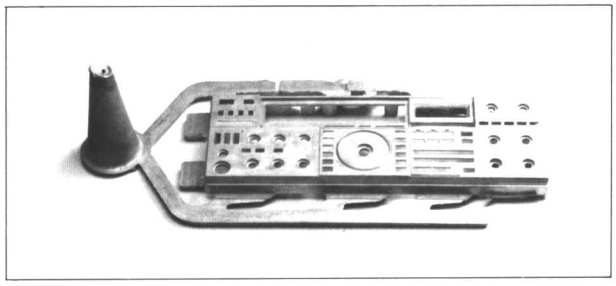
Fig.-51 Mode selector signal block diagram

Mechanical Design and Construction

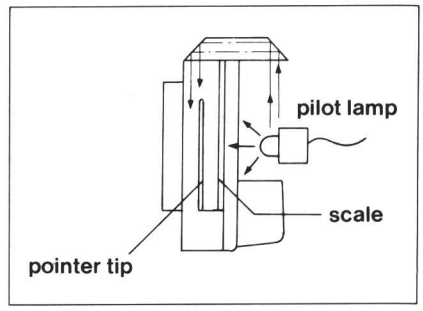
Using the latest digital technology, a combination of a variety of functions and the multi-function display has improved operability and visibility of the TS-940S. In addition, the clean, sharp lines and functional stability so characteristic of die-cast construction are quickly recognized in the beautiful front panel and in the highly efficient heat sink designs found on the rear of the unit.
Temperature control of critical components is accomplished with peak efficiency through use of a new air distribution system that allows operation on a 100% transmit duty cycle basis for periods of approximately one hour.
The high-density design concept enables the complete power supply circuitry and the automatic antenna tuner, as well as the balance of the transceiver electronics to be built into a compact cabinet normally sized for the transceiver electronics alone.

(1) Panel a Zinc die-cast

The panel is coated with melamine (dark blue). The coating is baked at about 140°C to secure its adhesion to the die-cast.



The main display of the indicator uses a large multi-function fluorescent indicating tube of two-color light emission. It can display frequencies and other different indications including RIT, XIT, MEMO, and the memory channel number. Transmit and receive frequencies appear on a 7 numeral digital display with sub-scale combination, indicating tuning across a selected 1 MHz/100 KHz band segment in 20 kHz/2 kHz steps, and offset frequencies in the RIT/XIT mode are displayed in two digits. The LCD (Liquid Crystal Display) sub-display uses a dot matrix (5 × 7 dots) module of a maximum of 16 digits and 2 lines of data. This LCD sub-display displays messages relating the operating conditions of the antenna/tuner, grahic characteristics, 24hour clock function, and times for timer on/off as well as frequencies can be displayed by entering a variety of commands.
Sharp contrast of the display eliminates cross talk (interference of correct indication caused by unwanted brightening of dots) together with the excellent temperature characteristics (−15°C to +70°C) and wide visible angle. The lighting of the LCD is uniform, green indirect lighting obtained from the pilot lamp through a light-conducting plate.
The front panel POWER/SWR meter utilizes a black



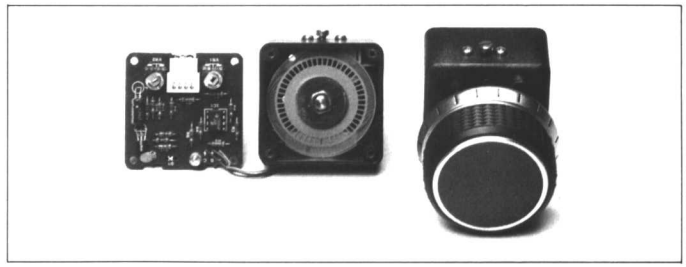
background color selected to harmonize with the main display. Backlighted calibration numerals, and a pointer tip superior readability and easy detection of minor variations in the reading.

■ Panel layout

Around the main VFO are thirty-seven control functions by the use of the latest digital technology. Increase of the available functions may cause less operability and more operation errors. To prevent this, studies on how to facilitate the operation have been made by different approaches like panel design and coloration to ensure visual confirmation of the functions under a human engineering point.
Shapes and the operating order of the control knobs are unique to each group of functions. The MODE and FUNCTION keytops are arranged lengthwise, while the MEMORY, BAND/KEY, CLOCK (located under the LCD), and GRAPH keys are rowed across the panel. The keytops are colored by function groups, and the special keys in a group have another color to prevent operation errors. The MODE keytop has a V-shaped light-conducting plate through which light from a tip LED passes, allowing you to check the operating mode quickly.

(2) VFO mechanism

Special tuning logic, working with the 10 Hz step high stability digital VFO, provides frequency changes directly related to the speed of tuning knob rotation. The special TRIO-KENWOOD-engineered optical encoder tuning system provides smooth, backlash-free tuning.
This VFO mechanism, which counts pulses optically by LEDs and phototransistors, consists of moving encoder disks processed by photoetching and fixed slits to obtain phase differences. They are overlapped with small clearances. The encoder disk has 250 accurate, uniform photoetched slits.
Rotating the VFO knob at normal tuning speeds shifts the frequency in 10 Hz increments, or 10 kHz per VFO knob revolution. Turning the knob faster (approximately 2 to 3

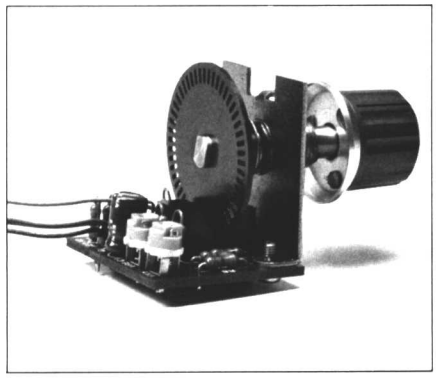


revolutions per second), increases frequency step size proportionally under control of a microprocessor.

A large die-cast VFO control knob, with a textured rubber cover, provides a positive tuning "feel" coupled with a strong flywheel effect, further enhancing the unit's flexibility of use and ease of operation.

(3) RIT/XIT mechanics

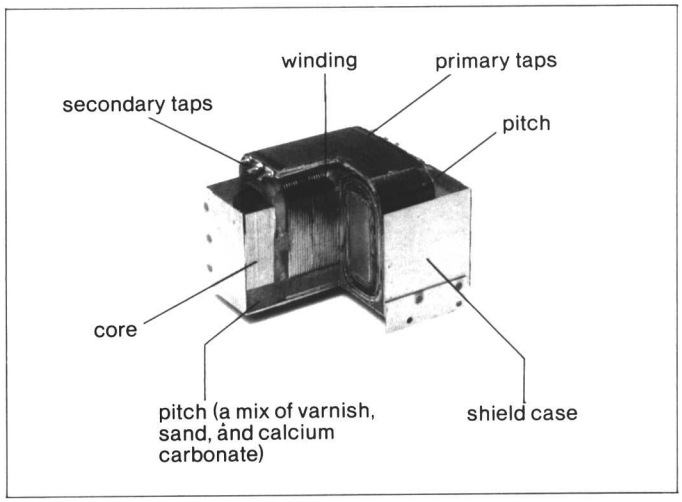
The RIT/XIT control employs a molded optical encoder disk having fifty slits located along its outer circumstance, providing a total of 2 kHz frequency shift in 10 Hz steps, for each 360 degrees of knob rotation.



(4) Construction

The chassis is box-bending structure. This construction provides excellent productivity and withstands impact and vibration forces increasing as the component units become larger and heavier. Heavy components like the power transformer, final unit, and antenna tuner concentrate the load on the center of the chassis. For this reason, the chassis is reinforced by angle steels in various parts. Especially, by screwing the radiating plate for the control unit at the bottom of the chassis to the lower case, plastic deformation of the chassis and stress on the PCBs of component units, which may damage the patterns or break the PCBs, are prevented when the set is applied impact and vibration forces during transportation.

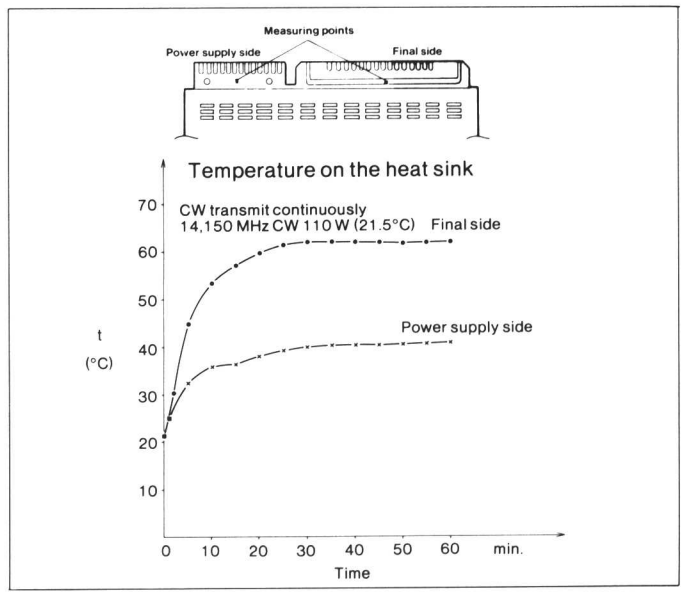
The laminated core power transformer is compact, light-weight, shielded and potted to protect the windings and connections from vibration and impact damage.



(5) Highly Efficient, Ducted Air-Flow, Cooling System for the Final and Power Supply unit

The heat sink cooling fins are designed to be an integral part of the ducted air-flow system, which is constructed in such a manner as to assure a continual flow of air across the front and rear surfaces of the heat sink, as well as over the fins themselves. Ports of varying sizes have been strategically located throughout the air-flow system to prevent dead-air pockets. Cooling air is drawn through the cabinet area by a whisper-quiet, two-speed fan that then directs its discharge air-flow into the ducting at a point immediately adjacent to the final amplifier transistors, assuring maximum heat transfer from these important components. Fan operation is controlled through use of automatic switching initiated by a detecting thermistor that senses final amplifier temperature. The high efficiency of the cooling system permits continuous transmission at full power for periods of approximately one hour without thermal shut-down.

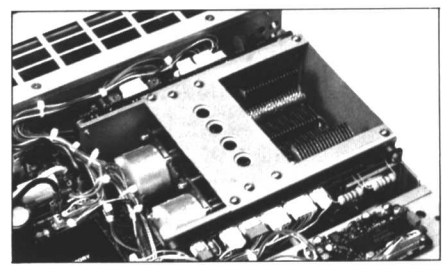
The power supply unit has its own independent cooling system and fan, also incorporating the ducted air-flow concept.



(6) Automatic antenna tuner

Forward and reflected waves are detected by a directional coupler. Signals proportional to the antenna line voltage and current are processed for phase comparison. These signals are used to control servo motors which quickly turn the two antenna tuner capacitors for minimum SWR within a range of all Amateur band, 1.8 and 30 MHz.

The gear mechanism of the automatic antenna tuner consists of a large torque DC servo motors and a spur gear with reduction ratios of 1/200 and 1/300 and drives the variable capacitor. During the tuning cycle, an LCD indicates "ANTENNA TUNER TUNING." When SWR is minimized (1.2:1 or less), the motors stop and the tuning display indicates "TUNING FINISHED—TX READY." If the antenna cannot be loaded properly, the LCD sub-display indicates "ANTENNA TUNER NO MATCH." The tuning cycle takes approximately three seconds.



OPTIONAL ACCESSORIES

Filters

The following optional filters are available.

YK-88C-1

CW 500 Hz narrow band filter with a center frequency of 8.83 MHz.

YK-88A-1

AM 6 KHz filter with a center frequency of 8.83 MHz. Although the TS-940S has a built-in AM ceramic filter in the 3rd IF stage, installing this filter further enhances performance.

YG-455C-1

8-element CW crystal filter with a 455 KHz center frequency and a 500 Hz bandwidth. Has an excellent shape factor.

YG-455CN-1

8-element CW crystal filter with 455 KHz center frequency and 250 Hz bandwidth. Effective when very sharp selectivity is required.

Table 7 lists the optional filters. These filters can be installed easily since they are plug-ins. When the Selectivity switch is set to NARROW in the CW mode, the VBT system rate of variation is decreased for convenience. That is, when the YK-88C-1 and YG-455C-1 are installed, the IF width can be varied from 150 to 500 Hz.

Optional filter

Type	Center frequency	Band width (−6 dB)	Band width (−60 dB)
YK-88C-1	8830.0 kHz	500 Hz	1.5 kHz
YK-88A-1	8830.0 kHz	6 kHz	11 kHz
YG-455C-1	455.0 kHz	500 Hz	820 Hz
YG-455CN-1	455.0 kHz	250 Hz	480 Hz

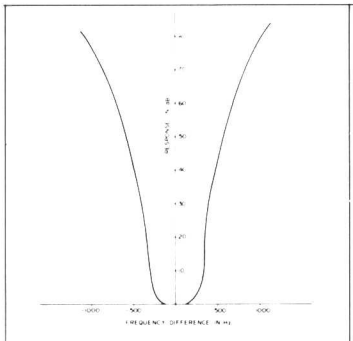
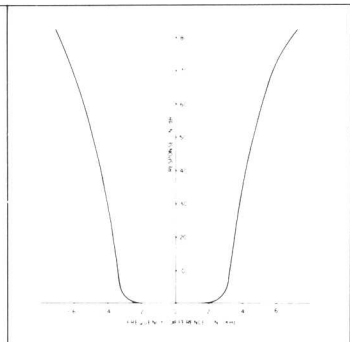
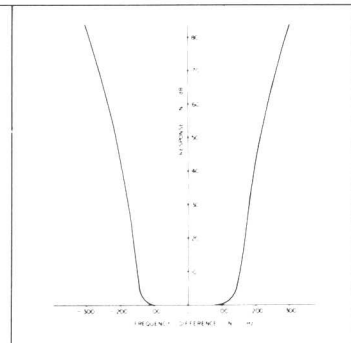


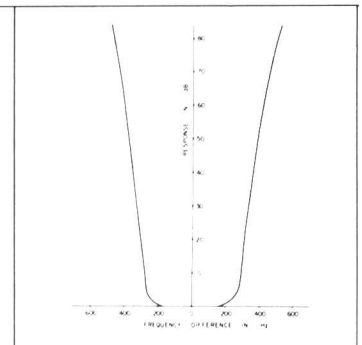
Fig.-52(a) YK-88C-1 characteristic



YK-88A-1 characteristic



YG-455C-1 characteristic



YG-455CN-1 characteristic

AT-940

Automatic Antenna Tuner

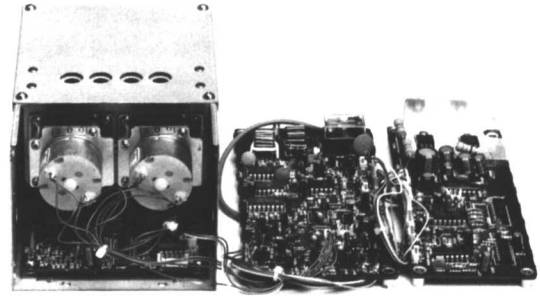
The AT-940 is an optional automatic antenna tuner that can be installed in the TS-940S.

FEATURES

- Full coverage of 160 through 10 meters, including the new WARC bands.
- Automatic motor speed control. The motor automatically stops when the SWR drops to its minimum value (1.2:1 or less).
- The AUTO-THRU circuit is disabled during transmission to protect the final transistors in case the AUTO-THRU switch is accidentally operated.
- The "tune" condition for automatic antenna tuning remains unchanged during transmission when the "AT.T" switch is depressed.

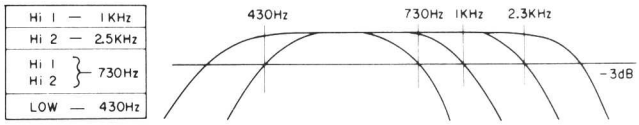
SPECIFICATIONS

●Frequency Range: All Amateur bands from 1.8 to 29.7 MHz ●Input Impedance: 50 Ω unbalanced ●Output Impedance: 20～150 Ω unbalanced ●Insertion Loss: Less than 0.8 dB ●Through Power: 150 W ●Maximum Tuning time: Less than 15 seconds.



SP-940
External Speaker

The SP-940 is a high class external speaker designed to match the TS-940S in size, color and appearance. The SP-940 uses a panel made of reinforced ABS plastic and an expanded metal speaker grill to improve tone quality. It is a low-distortion speaker with selectable frequency response for high intelligibility in any mode. The frequency response is determined by the built-in audio filters, which are effective in improving signal-to-noise-ratio under certain interference conditions, or when receiving weak signals. On the front panel is a headphone connector, for listening to audio output passed through the filters. Also on the front panel is a switch for selecting either of two audio inputs to the SP-940.



SP-940 filter characteristics

SPECIFICATIONS

●Speaker Diameter: 100 mm (3.94 inch) ●Input Power (max.): 1.5 W (3.0 W) ●Impedance: 8 Ω ●Frequency Response: 100 Hz~5 kHz ●Filter Cut-off Frequency: LOW 430 Hz (−3 dB)/HIGH1 1 kHz (−3 dB)/HIGH2 2.5 kHz (−3dB)/HIGH1 + HIGH2 730 Hz (−3 dB) ●Filter Attenuation: −6 dB/OCT ●Dimensions: 180 (7.01) W × 140 (5.51) H × 290 (11.4) D mm (inch) (Projections not included) ●Weight: 2 kg (4.41 lbs.) approx.

SO-1
TCXO "Temperature Compensated Crystal Oscillator"

High-stability TCXO, model SO-1, may be installed in place of the reference oscillator. This unit operates at 20-MHz with an accuracy of ±5 × 10 to the 7th negative power across a temperature range of −10 degrees C to +50 degrees C when installed, overall frequency stability is upgraded to a level approximating professional standards.

Oscillation frequency		20,000,000 Hz
Stability	Long period	$\pm 1 \times 10^{-6}$/year
	Temperature	$\pm 5 \times 10^{-7}$
Frequency compensation		More than ±60 Hz

MC-42S (8 pin)
UP/DOWN Hand Microphone

The MC-42S is handy dynamic microphones with PTT switch and UP/DOWN switches.

MC-60A (8 pin)
Deluxe Desk-Top Microphone with built-in Preamplifier

The zinc die-cast base provides high stability, and the MC-60A is completed with PTT and LOCK switches. UP/DOWN switches, an impedance selector switch and a built-in pre-amplifier.

MC-80 (8 pin)
Desk-Top UP/DOWN Microphone with built-in Preamplifier

The MC-80 is an omnidirectional electret condenser microphone provided with UP/DOWN switch, volume adjustment for output level, PTT and LOCK switch, and built-in pre-amplifier.

MC-85 (8 pin)
Multi-function Desk-Top UP/DOWN Microphone with built-in Audio Level Compensation

The MC-85 is a unidirectional high-class electret condenser microphone provided with the output selective switch, audio level compensation circuit, low cut filter, level meter, PTT and LOCK switch.

Specifications \ Model	MC-42S	MC-60A	MC-80	MC-85
Type (Microphone)	Omnidirectional dynamic	Unidirectional dynamic	Omnidirectional electret condenser	Unidirectional electret condenser
Connector	8 pin	8 pin	8 pin	8 pin
Output Impedance	500 Ω ±30%	Dual impedance 50 kΩ ±30% 500 Ω ±30%	700 Ω ±30% (at 1000 Hz)	700 Ω ±30% (at 1000 Hz)
Sensitivity 0 dB=1 V/μ bar 1000 Hz	−69 dB ±3 dB	Pre-amp out −56.0 ±3 dB/50 kΩ −71.0 ±3 dB/500 Ω Pre-amp in −50.5 ±3 dB/50 kΩ −59.0 ±3 dB/500 Ω	−40 dB ±6 dB (VR., MAX.)	Mic level max. −40 ±6 dB (COMP OFF) −34 ±6 dB (COMP ON)
Frequency Response	300 Hz−5 kHz (±6 dB)	150 Hz−10 kHz (−6 dB) (Pre-amp off) 200 Hz−7 kHz (−6 dB) (Pre-amp in)	200−7000 Hz (±6 dB)	300−7000 Hz (±6 dB) Low Cut 300 Hz (−12 dB)
Power Supply (Supplied by TRIO-KENWOOD transceivers.)		3 V (1.5 V × 2) "AA" Alkaline (not NiCd)	6 V (1.5 V × 4) ("AA" batteries)	6 V (1.5 × 4) ("AA" batteries)
Current Consumption			Approx. 7 mA	Approx. 9 mA (RX) 11 mA (TX)
Dimensions [mm (lich)] and weight	53 (2.1) W × 82 (3.2) H × 33.5 (1.3) D 190 g (0.42 lbs.)	85 (3.4) W × 200 (8.0) H × 161 (6.4) D 1.1 kg (2.4 lbs.)	119 (4.7) W × 55 [270] (2.2) H × 157 [180] (6.2) D 700 g (1.54 lbs.)	177 (7.0) W × 55 [270] (2.2) H × 157 [180] (6.2) D 1 kg (2.2 lbs.)
Others	Built-in UP/DOWN SW	UP/DOWN SW Built-in Pre-amplifier	UP/DOWN SW Built-in Pre-amplifier	UP/DOWN SW Built-in audio level compensation

SM-220
Station Monitor

Based on wide-frequency-range oscilloscope (up to 10 MHz), the SM-220 station monitor features, in combination with a built-in two-tone generator, a wide variety of waveform-observing capabilities. When the BS-8 is installed in the SM-220 and connected to the transceiver, signal conditions in the vicinity of the receive frequency can be viewed over a ±20 kHz or ±100 kHz range. The SM-220 provides efficient station operation as it monitors transmitted waveforms, and it also serves as a high-sensitivity, wide-frequency range oscilloscope for various adjustments and experiments.

SPECIFICATIONS

(Transmit Signal Monitor Terminal) ●Frequency range: 1.8−150 MHz ●Maximum power: 1 kW (1.8−54 MHz), 50 W (150 MHz) ●SWR: 1.2:1 or less ●Deflection sensitivity: Better than 1 div. at 2 W input ●Attenuator: 6 steps (Trapezoid waveform observation) ●Frequency range: 1.8−30 MHz ●Maximum power at DRIVE TERMINAL: 2−100 W ●SWR: 1.2:1 or less (Two-tone generator) ●Oscillator frequency: 1,000 Hz and 1,575 Hz ●Output voltage: 10 mV/50 kΩ (at TWO TONE) (Pan display unit ●Input center frequency: 8.830 MHz ●IF frequency: 455 kHz ●IF bandwidth: More than 1 kHz (−6 dB) ●Input sensitivity: Better than 10 μV/div. ●Scan width: ±20 kHz, ±100 kHz, switchable gain (Horizontal amplifier) ●Deflection sensitivity: More than 300 mV/div. ●Frequency response: DC−250 kHz or over (EXT GAIN at MAX): DC−40 kHz (EXT GAIN at 1/2) ●Input resistance/capacitance: 1 MΩ (±20%)/35 PF or less (SYNC switch at INT) ●Attenuator: Fully variable to 0 ●Max. input voltage: 100 Vp-p (Sweep circuit) ●Sweep frequency: 10 Hz−100 kHz (4 ranges, with fine adjustment) ●Sweep linearity: Better than 5% ●Sync system: Synchronized sweep, internal negative sync and external sync ●Sync amplitude: Internal: Better than 1 div. on CRT external: Better than 2 Vp-p (Vertical amplifier) ●Deflection sensitivity: Better than 20 mV/div. ●Frequency response: 2 Hz−10 MHz (−3 dB) ●Input resistance/capacitance: 1 MΩ/40 PF ●Overshoot: Less than 5% ●Attenuator: 1, 1/10, 1/100 and GND/MONITOR (Error between steps: 5% max.) ●Max. input voltage: 300 V (DC+AC peak) or 600 Vp-p ●Power supply: 120/220/240 V AC±10%, 50/60 Hz 20 W ●Dimensions: 215 (8.6) W × 153 (6.1) H × 335 (13.4) D mm (inch) ●Weight: 5 kg (11 lbs.)

OPTIONAL ACCESSORIES

●BS-8・・・Pan Display for TS-830S/TS-530S/TS-180S/TS-820 series/TS-940S ●BS-5・・・Pan Display for TS-520/TS-520SE

TL-922/TL-922A
HF Linear Amplifier

The TL-922 and TL-922A are class AB_2 grounded-grid linear amplifier developed by TRIO-KENWOOD through advanced high-power technology using two high-performance EIMAC 3-500Z power tubes. It covers all bands 160 m through 10 m (without the three new Amateur bands) for SSB, CW and RTTY modes of operation. (not usable with full break-in, semibreak-in only)

FEATURES

●Pair of EIMAC 3-500Z high performance transmitting tubes ●Class AB_2 G-G circuit ●Excellent IMD (intermodulation products distortion) characteristics ●Perfect safety protection ●Blower turn-off DELAY circuit ●Variable threshold level type ALC circuit ●Two easy-to-read meters ●Attractive matching with TRIO-KENWOOD HF transceivers.

SPECIFICATIONS

Frequency range: 1.8−2.0 MHz, 3.5−4.0 MHz, 7.0−7.3 MHz, 14.0−14.35 MHz, 21.0−21.45 MHz, 28.0−29.7 MHz (not on TL-922A) ●Mode: SSB CW, RTTY ●Drive power: 80 W or more for full output ●RF input power:

SSB=2,000 W PEP, CW, RTTY=1,000 W DC
●Circuitry: AB_2 class grounded-grid linear amplifier
●Input impedance: 50 Ω ●Output impedance: 50~75 Ω ●Cooling: Forced air ●Fan motor delay stop time: 140±30 seconds ●ALC: Negative going adjustable threshold −8 V DC max. output (typical)
●Tubes:2×3-500 Z (optional) ●Power requirement: 120/220 V 28 A, 50/60 Hz type, 220/240 V 14 A, 50/60 Hz type ●Dimensions: 390 (15.4) W×190 (7.5) H×407 (16.0) D mm (inch) ●Weight: 31 kg (68 lbs.)
*The model TL-922A with tubes is available only in U.S.A.

SW-200A, SW-2000

SWR/POWER Meter (supplied with a coupler)

SW-200A supplied with SWC-1, SW-2000 supplied with SWC-3 Selectable Peak-reading/RMS, SWR/POWER meters cover 1.8~150 MHz (SW-200A), 1.8~54 MHz (SW-2000) in range of 0~20/200 W (SW-200A), 0~200/2000 W (SW-2000) full scale for base stations use.

SPECIFICATIONS

●Impedance: 50~52 Ω ●Frequency range: 1.8~150 MHz (SW-200A). 1.8~54 MHz (SW-2000) ●Power measuring range: 0~20/200 W (SW-200A), 0~200/2000 W (SW-2000) ●Accuracy: Less than ±10% of full scale ●Sensitivity: Less than 2 W (SW-200A), 20 W (SW-2000) ●Power supply: 12 VDC 100 mA ●Dimensions: 193 (7.6) W×62 (2.4) H×79 (3.1) D mm (inch) ●Weight: 0.7 kg (1.5 lbs.) approx.

HS-4

HS-5

HS-6

HS-7

Headphones

The TRIO-KENWOOD headphones are specifically designed for communications equipment.

Specifications \ Model	HS-4	HS-5	HS-6	HS-7
Impedance	8 Ω	8 Ω	12.5 Ω	16 Ω
Max. input (100 Hz)	3 W	200 mW	100 mW	50 mW
Frequency Response (−6 dB)	300−3000 Hz	150−4000 Hz	100−10000 Hz	100−10000 Hz
Weight (including cord)	330 g (0.73 lbs.)	350 g (0.77 lbs.)	100 g (0.22 lbs.)	15 g (0.03 lbs.)

PC-1A

Phone Patch Controller (Available only where phone patch operation is legal)

Model PC-1A phone patch has been carefully engineered and manufactured under rigid quality standards, and should give satisfactory and dependable operation for many years.

FEATURES

●Provides connection between a transceiver and a telephone line ●High isolation between receive input and transmit output ●Compact design for easy installation in a limited space.

SPECIFICATIONS

[Impedance levels]
●Line: 600 Ω nominal ●RX in: 8 Ω nominal ●SP out: 8 Ω nominal ●Mic: 50 kΩ nominal

LF-30A

Low-Pass Filter

SPECIFICATIONS

●Cutoff frequency: 30 MHz ●Attenuation: More than 90 dB between 90 and 300 MHz ●Durability against input power: 1 kW PEP ●Insertion loss: Less than 0.5 dB at 30 MHz ●Input/output impedance: 50 Ω ●Dimensions: 244 (9.6) W×50 (1.97) H×40 (1.57) D mm (inch) ●Weight: Less than 560 g (1.2 lbs.)

Some accessories may not be available in your area.

SPECIFICATIONS

[GENERAL]

Transmitter Frequency Range ..... 160-m band 1.8~2.0 MHz
80-m band 3.5~4.0 MHz
40-m band 7.0~7.3 MHz
30-m band 10.1~10.15 MHz
20-m band 14.0~14.35 MHz
17-m band 18.068~18.168 MHz
15-m band 21.0~21.45 MHz
12-m band 24.89~24.99 MHz
10-m band 28.0~29.7 MHz

Receiver Frequency Range ..... 150 kHz~30 MHz
Mode ..... A3J [J3E] (USB, LSB), A1 [A1A] (CW), F1 [F1B] (FSK), F3 [F3E] (FM), A3 [A3E] (AM)
Frequency Stability ..... $\pm 10 \times 10^{-6}$ (−10°C~+50°C)
Frequency Accuracy ..... $\pm 10 \times 10^{-6}$ (at normal temperatures)
Antenna Impedance ..... 50 Ω (20~150 Ω with the AT-940 antenna tuner installed, transmission only)
Power Requirements ..... 120/220/240 VAC, 50/60 Hz
Power Consumption ..... Max. transmit 510 W Receive (no signal) 80 W
Dimensions ..... 401 (15.79) W × 141 (5.55) H × 350 (13.78) D mm (inch) (Projections not included)
Weight ..... 18.5 kg (40.78 lbs.) approx.
20 kg (44.09 lbs.) approx. (with antenna tuner)

[Transmitter]

Final Power Input ..... SSB/CW/FSK/FM=250 W PEP
AM=140 W
Modulation ..... SSB=Balanced Modulation
FM=Reactance Modulation
AM=Low Level Modulation
FM Maximum Frequency Deviation ..... ±5 kHz
FSK Shift Width ..... 170 Hz
Carrier Suppression ..... Less than −40 dB
Spurious Response ..... Less than −40 dB (CW)
Unwanted Sideband Suppression ..... Better than 50 dB (Modulation frequency: 1.5 kHz)
Third Harmonic Intermodulation Distortion ..... Better than −37 dB (at 14.2 MHz) (based on single tone output)
Microphone Impedance ..... 500 Ω~50 kΩ
Frequency Response (SSB) ..... 400~2600 Hz (−6 dB)

[Receiver]

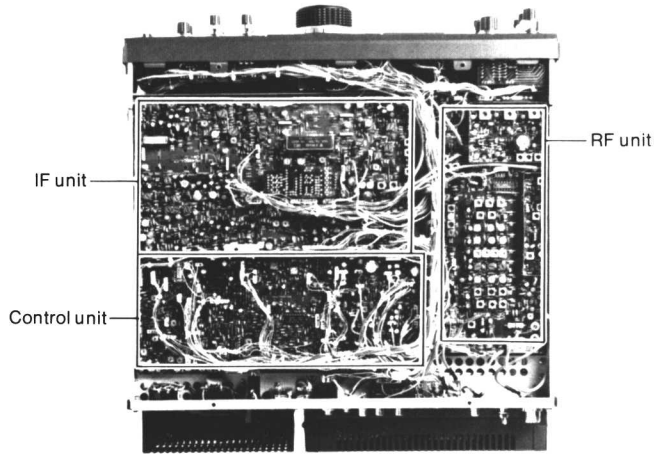
Circuitry ..... SSB/CW/AM/FSK: Quadruple conversion system
FM: Triple conversion system
Intermediate frequency ..... 1st IF 45.05 MHz
2nd IF 8.83 MHz
3rd IF 455 kHz
4th IF 100 kHz

Sensitivity ..... at 10 dB (S/N) (0 dBμ=1 μV)

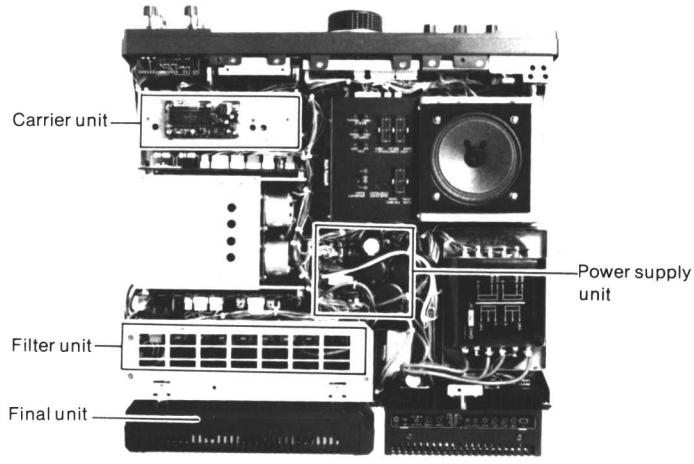
Mode \ Frequency	150~500 kHz	500 kHz~1.8 MHz	1.8~30 MHz
SSB, CW, FSK	Less than 1 μV	Less than 4 μV	Less than 0.2 μV
AM	Less than 10 μV	Less than 32 μV	Less than 2 μV
FM (SINAD 12 dB)	—	—	Less than 0.5 μV

Squelch Sensitivity ..... Less than −10 dBμ (0.32 μV)
Image Ratio ..... More than 80 dB (1.8~30 MHz)
IF Rejection ..... More than 70 dB (1.8~30 MHz)
Selectivity ..... SSB, CW, AM (N), FSK
2.4 kHz (−6 dB)
3.6 kHz (−60 dB)
AM (W)
6 kHz (−6 dB)
15 kHz (−50 dB)
FM
12 kHz (−6 dB)
22 kHz (−60 dB)
Variable Frequency Range ..... SSB slope tuning (with SSB filter)
High-cut=more than 1500 Hz
Low-cut=more than 700 Hz
CW VBT (without optional filter)
600 Hz~2.4 kHz (continuous)
RIT/XIT Variable Range ..... ±9.99 kHz
Notch Filter Attenuation ..... More than 40 dB
Audio Output Power ..... 1.5 W (8 Ω at 10% distortion)

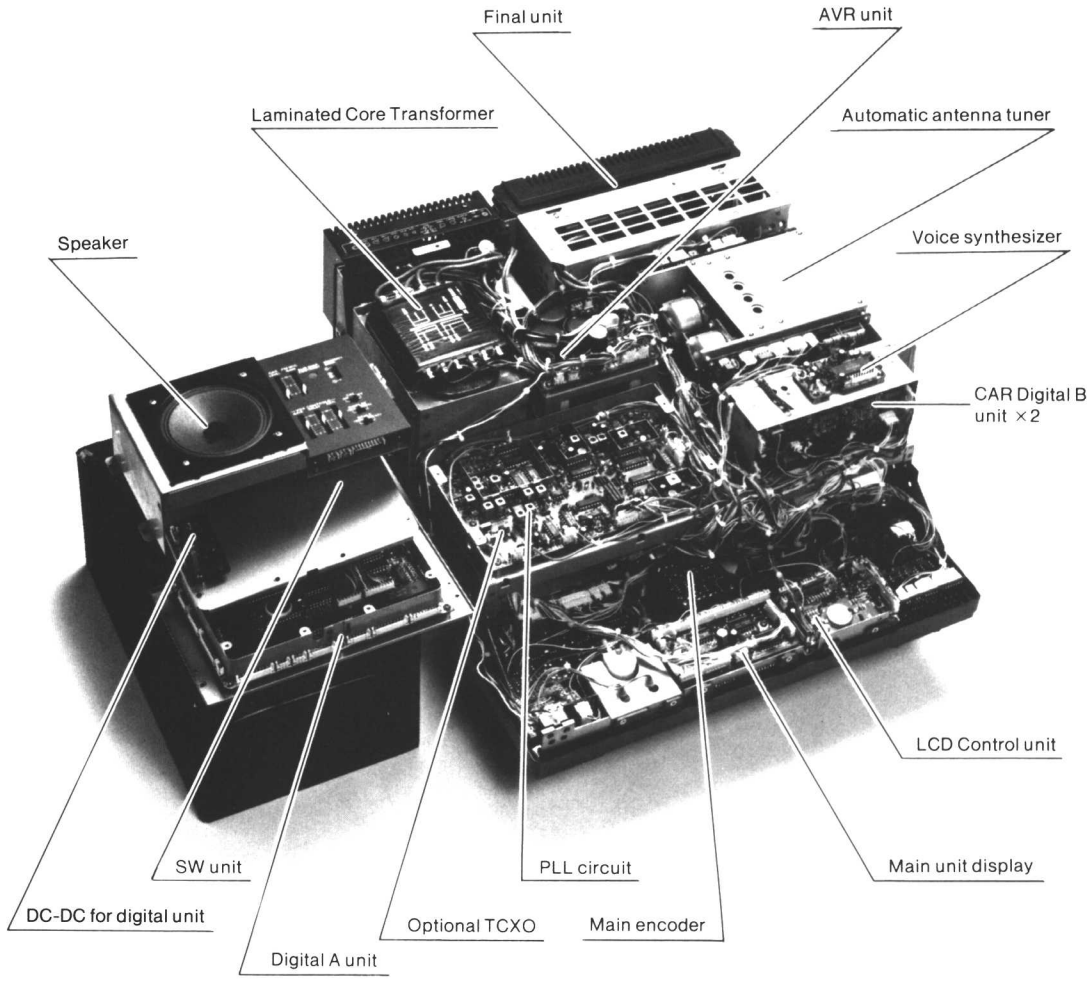
The equipment meets or exceeds published specifications.
Specifications are subject to change without notice due to advances in technology.



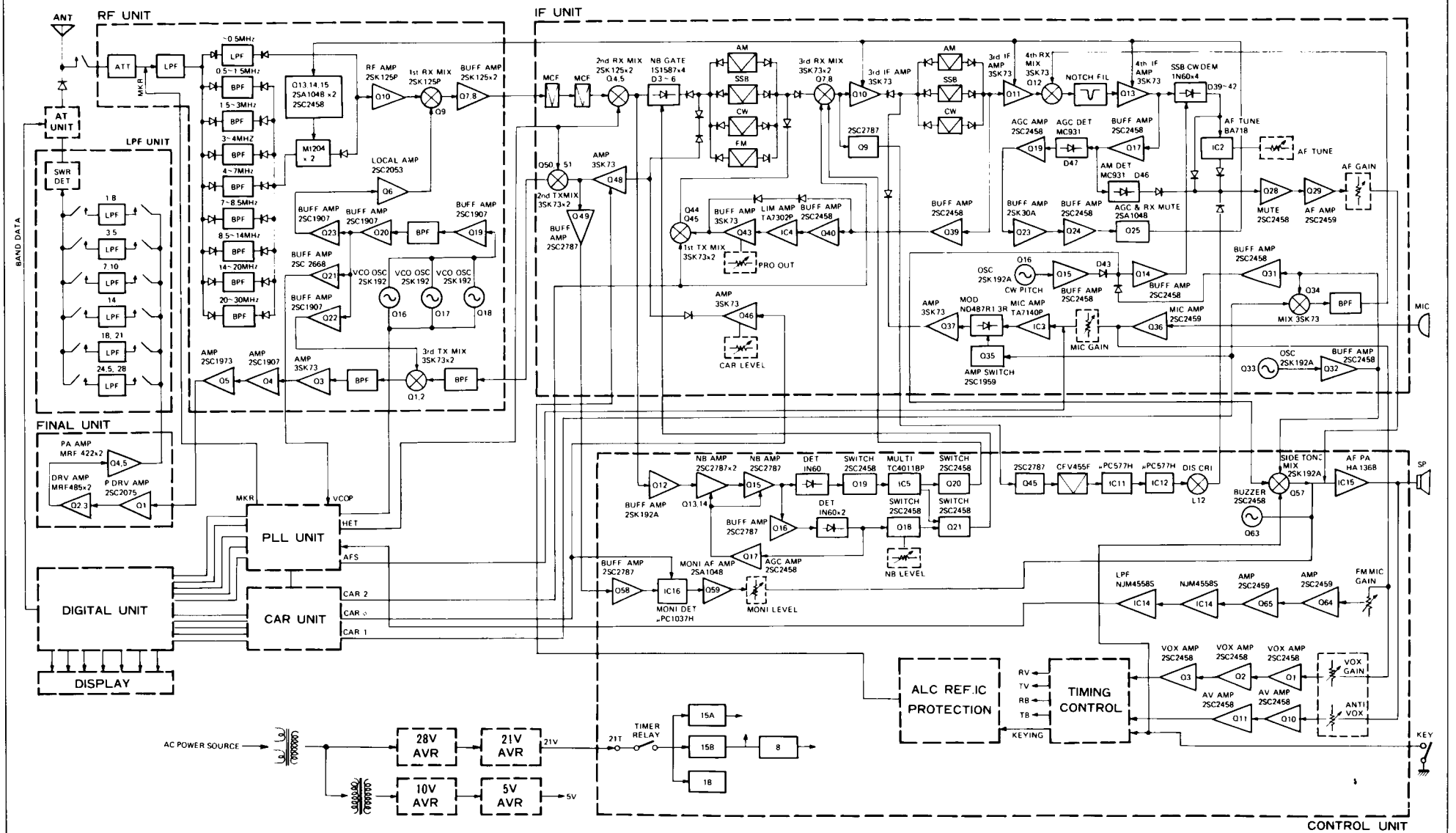
Top view



Bottom view



TS-940S BLOCK Diagram



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