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SERVICE INFORMATION - MODEL FL2/A

AUTOMATIC NOTCH FILTER MODULE

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Principles of operation

The function of the circuit is to sweep a narrow notch filter back and forth over the audio speech frequency range. Whenever a continuous audio tone appears in the filters pass-band the sweep circuit is disconnected automatically and instead an automatic frequency control loop tunes the filter to the centre of the tone. So far as the operator is concerned the tone is notched out leaving the speech signal unaffected.

The basic principles of operation are similar to Model FL1 but Model FL2/A utilises the special features of a switched capacitor filter chip (National MF10) to (a) simplify the circuit and (b) give better lock performance.

The MF10 contains two separate state variable filter functions. Each can provide simultaneously notch, peak and low-pass outputs and the centre frequency of each filter is controlled by an external clock at CMOS logic levels. In FL2/A the clock is at 100 times the filters centre frequency. Because the two filters are on the same chip they are very well matched and this feature is used to advantage.

Refer now to the simplified block diagram. The input signal enters the first filter and the notch output of this filter provides the output signal directly. The low-pass and band-pass outputs of this filter are simultaneously available and although not needed for audio purposes they are used in the automatic control circuitry. The latter relies on the fact that if the filter is tuned below resonance the notch output is in phase with the low-pass output while above resonance the two are 180° out of phase. The phase transition is very abrupt and therefore if the low-pass and notch outputs are compared in a phase sensitive detector its output will switch rapidly from a low value to a high value on either side of the correct tuning position. This output can then be used in a negative feedback loop to control the centre frequency of the filter (by using it to control the clock frequency applied to the MF10).

Although the above system would work as described it is better to use the second half of the MF10 to feed the phase sensitive detector. The first half of the filter is then used as a pre-filter for the second half. Thus the band-pass output of the first stage is used as input to the second half and the LP and NOTCH outputs of the latter are fed to the phase sensitive detector in the automatic control loop.

The advantage is that the control loop is then much more immune to noise. In effect therefore the loop operates to tune the second filter to an incoming tone, but the accurate matching ensures that the first filter will also be perfectly tuned.

A second phase detector compares the low-pass outputs of the two filters. Only when these two signals are in phase will PSD2 give an output and this will occur only when the filter is tuned to a signal. This output therefore represents the "lock" condition. When the $\overline{\text{LOCK}}$ output is high the loop integrator in the AFC system is connected as a triangular wave generator and the filter frequency sweeps up and down between its limits. When $\overline{\text{LOCK}}$ goes low the sweep stops and the loop integrator is allowed to control the filter frequency which therefore tracks the incoming signal.

Detailed circuit description

Refer to the complete circuit diagram in the following discussion.

Pins 20, 19, 18 of the MF10 represent low-pass, band-pass and notch outputs of filter 1 and 1, 2, 3 the corresponding outputs of filter 2. The Q of filter 1 is equal to R6/R7 = 10 and similarly for filter 2, Q = R4/R5 = 10. The gain of filter 1 is set at ten (gain = R6/R8 = 10) while that of filter 2 is set at unity (gain = R4/R3 = 1). Outputs from the two filters are amplified to give CMOS logic levels in CMOS inverters and then fed to two phase sensitive detectors. PSD 1 is part of a CD4046 phase lock loop chip (IC8) while PSD 2 is built up using two analogue gates in CD4066 (4B, 4C, of IC4).

The output of PSD 1 (pin 2 of IC8) feeds an active integrator based on 3 CMOS inverters (IC1D, E, F). R22, C11, C12 merely provide closed loop stabilisation while R14, C10, R24 control the characteristics of the integrator proper. IC1A and R13, 15, 18 are included to compensate for offsets in the integrator inverter. In the absence of R16 and D4 therefore, the integrator output (pin 8 of IC1F) is fed back to the VCO control voltage input of IC8 (pin 9) thereby closing the automatic frequency control loop. The VCO output provides the clock signal for the MF10 filters and is always 100 times the filter frequency.

If the filter is not locked the output of PSD2 will be high and therefore gates IC4D and IC4A will be in a low resistance state. This activates a positive feedback loop within the loop integrator via the Schmitt trigger formed from IC1B, IC1C, R23, R21 and as a result the output at pin 8 ramps linearly up and down from zero to the supply rail at a rate determined by R16 and C10 (about 1Hz). Also the LOCK lamp D2 stays off.

When PSD2 first produces a signal the output of IC3D (used as an integrator) goes low. This signal discharges C14 rapidly through IC4D and very shortly after the output of IC3F (pin 6) goes low. This has several effects. First it increases the charging resistance for C14 to 1M; secondly it opens gate IC4A so that R16 is disconnected (this stops the sweep); thirdly after a delay due to R30 & C15 the LOCK lamp D2 illuminates.

Muting circuit

In the absence of any signal at all the sweeping filter produces a slight "swishing" noise. A circuit is therefore provided to stop the sweep in the absence of any signal at all. IC7B amplifies any input signal and after rectification in D5/D6 it is used to switch pin 1 of IC7A low. In the absence of any signal pin 1 goes high and via D4 the sweep is disabled and the filter frequency is forced to its lower limit (pin 9 of IC8 low).

If necessary this circuit can be disabled by removing D4 or R31. This may be useful during servicing.

Notch trim

Some specimens of MF10 show a slight interaction between sections which tends to reduce the notch depth. This effect is cancelled by the feedback path via R35 & VR3 between pins 1 and 16 of the MF10. VR3 is adjusted for best notch depth when the filter is locked at a frequency near its upper limit, say 3.5 kHz. Components C20, VR5, C19 were originally fitted to help with this compensation but later experience showed that VR3 is adequate.

Other trimmers

VR4 sets the threshold at which the lock detect circuit operates. It has a big effect on sweep speed since if turned fully clockwise (to negative end) the sweep will never stop while if fully anticlockwise the sweep will never start.

BEWARE: with insufficient input the sweep will never start anyway because of the mute circuit!

VR1 and VR2 set the upper and lower limits respectively of the tuning range.

Useful test points

1. The sweep can be monitored at pin 8 of IC1F. In normal operation (with a wide band input signal such as hiss or speech) the waveform should be a randomly stepped triangle waveform. The steps are caused by trial attempts at locking and their length is determined by R38/C25.

2. The filter frequency can be monitored with a frequency counter connected to pin 4 of IC8, remembering that the indicated frequency will be 100 times the actual frequency.

Test procedure

1. Apply supply voltage (12 volts) and check that the current is normal (about 35 mA). Check that Vcc is 8 v at pin 14 of any of the CMOS chips. Check the "power on" LED, D1.

2. Remove one end of either D4 or R31 to disable the mute circuit.

3. Set VR4 fully clockwise. Then with no input signal applied monitor pin 8 of IC1F and check for a symmetrical triangle waveform sweeping linearly from 0 to Vcc at about 1Hz.

4. Adjust VR1 so that the upper sweep limit is 4 kHz and then adjust VR2 so that the lower sweep limit is 200 Hz. (Monitor the filter frequency using a frequency counter at pin 9 of IC8: it will read 100 x the filter frequency. If necessary temporarily hold the sweep at the upper or lower limits by shorting pin 13 of IC1D to ground or to Vcc respectively).

5. Connect a source of wideband noise with peak-to-peak amplitude about 2 volts to the input of the filter at the PCB pads and while monitoring pin 8 of IC1F with an oscilloscope set VR4 so that the sweep slows down considerably but not completely.

6. Connect an audio signal generator to the filter input and an oscilloscope (and/or an audio amplifier) to the filter output using the PCB connector pads. Check that the filter locks correctly and rapidly at representative frequencies between 200 and 4000 Hz, and that the "LOCK" lamp functions.

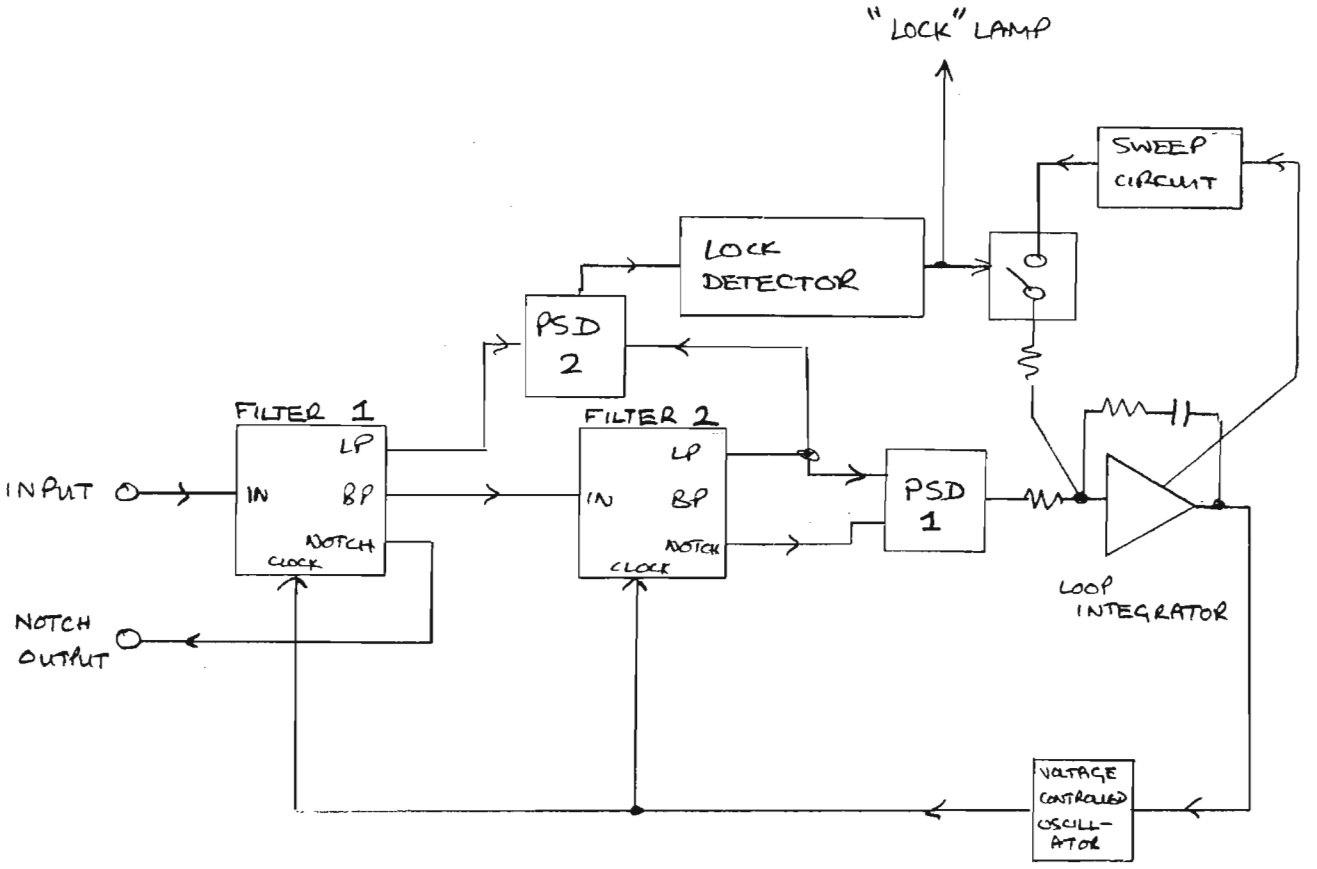
7. Repeat 6 with input signal levels of 20 mV pk-pk (minimum) and 600 mV pk-pk (near to clipping level).

8. Repeat 7 with noise added to the tone to give a signal-to-noise ratio of about unity.

9. With the filter locked to a tone at 3500 Hz adjust VR3 for best notch depth.

10. Reconnect the mute circuit (see step 2) and by monitoring pin 1 of IC7A check that the mute operates with input levels at or below 20 mV pk-pk.

11. Check that the "BYPASS" switch functions correctly.



SIMPLIFIED BLOCK DIAGRAM – MODEL FL2/A