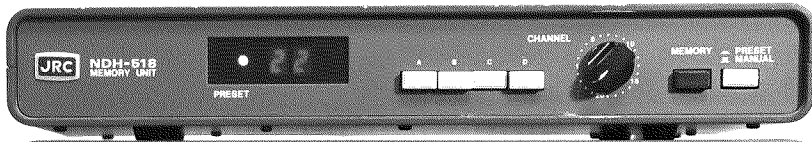


SERVICE MANUAL  
FOR  
MODEL NDH-518 MEMORY UNIT



**JRC**

*Japan Radio Co., Ltd.*

## SERVICE INSTRUCTIONS : NDH518 MEMORY UNIT

### GENERAL

The block diagram and schematic for the memory unit are shown in the appendix. The unit is made up of a memory circuit utilising six integrated circuits type  $\mu$ PD5101LC. These IC's are 1K CMOS static RAM (256 x 4) where the FF is used to store data, clocks are not needed, and the information stays in storage as long as power is supplied. It should be noted that an optional battery(s) can be installed to back up data stored.

Important - Alkaline batteries should be used as commonly used manganese types will possibly leak when they become exhausted. Any consequent damage is not covered by warranty.

Frequency data is transferred from the receiver via the three state buffers (IC 9, 10, 11, 12, 13, 14).

Data input and memory output is via the cable terminated with the plug P4.

96 frequencies can be put in memory (24 channels per channel switch x 4 - A, B, C, D, selected by the push button switches).

The channel is designated by specifying the address of the RAM's by the channel switches and this information is simultaneously sent to the channel display circuit, IC7 and IC3.

The power source voltage detecting circuit controls the chip enable terminal of the RAM's in order to protect the memory frequency data from being lost when the power switch is turned off.

The power detecting circuit is TR2/IC16.

### POWER

Since CMOS is used, power supply requirements are low. 10-11V from the receiver is supplied through P4 and P7/J7 pin 2,3 and regulated to 5V through IC17.

### DATA - TESTING

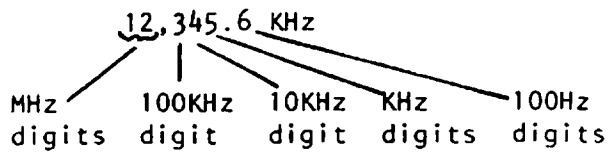
The table below shows the INPUT state of data from the receiver for each of the digits that are capable of being displayed on the receiver. Levels for all digits representing 100Hz, 1KHz, etc. are similar, the exception being the digits representing tens of MHz and the 20MHz digit.

If incorrect levels are being returned from the memory resulting in an incorrect display, isolation of the faulty digit(s) may be made by comparing actual level on the appropriate pins of J7.

### PROCEDURE

1. Set the receiver in manual.
2. Check with logic tester to see if the levels are according to the following table as each digit is selected. Increment the tuning

knob or band switch as required to access the digits corresponding to their place in the dialled up frequency, e.g.



J7 PINS

<u>100Hz UNITS</u>	<u>5</u>	<u>6</u>	<u>7</u>	<u>8</u>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = HIGH ≈ 5V

Similar levels will be evident for KHz, tens KHz, and 100KHz digits.  
 1KHz Pins are on J7 Pins 9 and 10, J6 Pins 1 and 2  
 10KHz Pins are on J6 Pins 3,4,5 and 6  
 100KHz Pins are on J6 Pins 7,8,9 and 10  
 Levels for 1MHz are on J5 Pins 1,2,3 and 4

Note: Levels will be same as in 100Hz sample chart as above, with pins taken in sequence listed.

For tens of MHz, J5 pin 9 is "High" for a reading of "1", and pin 8 is "High" for a reading of "2".

MEMORY IC

Levels noted on all pins including the supply rail for IC 1,2,3,4,5 and 6 are shown in the table below.

TEST CONDITIONS

1. Dial up a frequency of 12,345.6 MHz on the receiver, with memory unit connected.
2. Select CH1, depress button "A" and "preset" button.
3. Check levels per table below.

	<u>PINS</u>																					
	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>	<u>8</u>	<u>9</u>	<u>10</u>	<u>11</u>	<u>12</u>	<u>13</u>	<u>14</u>	<u>15</u>	<u>16</u>	<u>17</u>	<u>18</u>	<u>19</u>	<u>20</u>	<u>21</u>	<u>22</u>
IC1	L	L	L	H	L	H	H	L	H	H	L	L	H	H	H	H	L	L	H	L	H	
IC2	L	L	L	H	L	H	H	L	L	L	H	H	L	L	L	L	H	L	L	H	L	H
IC3	L	L	L	H	L	H	H	L	0	H	H	H	L	L	L	L	H	L	L	H	L	H
IC4	L	L	L	H	L	H	H	L	L	L	L	L	H	H	L	L	H	L	L	H	L	H
IC5	L	L	L	H	L	H	H	L	H	H	L	L	H	H	L	L	H	L	L	H	L	H
IC6	L	L	L	H	L	H	H	L	L	L	H	H	H	H	L	L	H	L	L	H	L	H

Levels for the three state buffer IC's, IC 9,10,11,12,13 and 14 are shown on the table below. Frequency reading on the receiver is 12,345.6 MHz.

	<u>PINS</u>													
	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>	<u>8</u>	<u>9</u>	<u>10</u>	<u>11</u>	<u>12</u>	<u>13</u>	<u>14</u>
IC9	H	H	H	H	L	L	L	H	H	H	H	H	H	H
IC10	H	L	L	H	H	H	L	L	L	H	L	L	H	H
IC11	H	H	0	H	H	H	L	L	L	H	L	L	H	H
IC12	H	L	L	H	L	L	L	H	H	H	L	L	H	H
IC13	H	H	H	H	H	L	L	H	H	H	L	L	H	H
IC14	H	L	L	H	H	H	L	H	H	H	L	L	H	H

COMPONENTS

1. Parts list for the NDH518 is appended.
2. Schematic diagram.
3. Block diagram.  
IC's specifications of the major IC used in the memory unit are also appended.

## Testing

How do you know whether the I/O works OK, and all is well with the data bits?  
Are all address lines all well connected?

Fill channel 1 to 10 of bank A  
with:

Chan	figures	binary
1	11.111.1	0001
2	22.222.2	0010
3	3.333.3	0011
4	4.444.4	0100
5	5.555.5	0101
6	6.666.6	0110
7	7.777.7	0111
8	8.888.8	1000
9	9.999.9	1001
10	10.000.0	0000

### First test

Choose Bank A (all switches adresbit B, C and D would be dis-engaged, contact problems with those adresbit pull-down than not applicable)  
With the table left you quickly see whether there are any address or data bit errors.

Because never programmed channels can contain invalid data noise, you can see the strangest characters or dark spots on the display prior to a real channel MEM write action. This is normal and NOT worrying!  
So do: → tune in something → press MEM → press Preset → identical? → OK.

You can quickly erase all noise everywhere: set tune to 000.0, hold MEM, and rotate 24 steps quickly, everything is reset to 0. Next bank.

After a long standstill, the switches B, C and D may have contact cracking, use intensely or perhaps a tiny drop contact cleaner or spray?

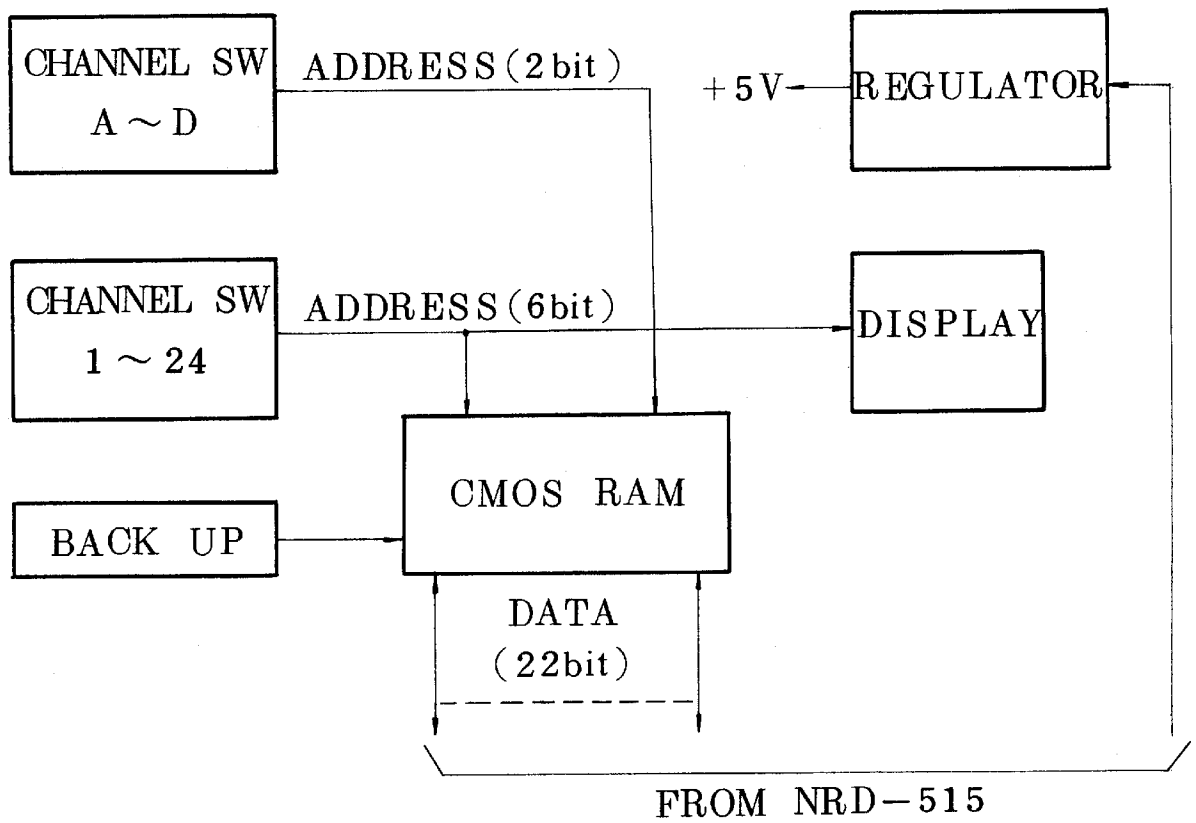


Fig. 1 Block diagram of NDH-518 Memory Unit

図 1 NDH-518 メモリユニット系統図

## 1024 BIT (256x4) STATIC CMOS RAM

**DESCRIPTION** The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

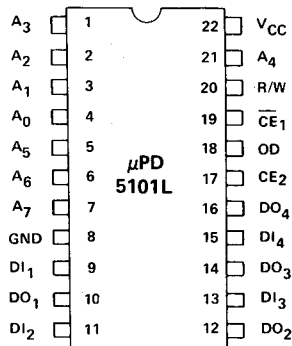
All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ( $\overline{CE}_1$ ,  $CE_2$ ) are provided, with the devices being selected when  $\overline{CE}_1$  is low and  $CE_2$  is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving  $\overline{CE}_1$  high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving  $CE_2$  low.

The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

- FEATURES**
- Directly TTL Compatible — All Inputs and Outputs
  - Three-State Output
  - Access Time — 650 ns (μPD5101L); 450 ns (μPD5101L-1)
  - Single +5V Power Supply
  - $CE_2$  Controls Unconditional Standby Mode
  - For operation at +3V Power Supply, Contact the NEC Sales Office.

### PIN CONFIGURATION

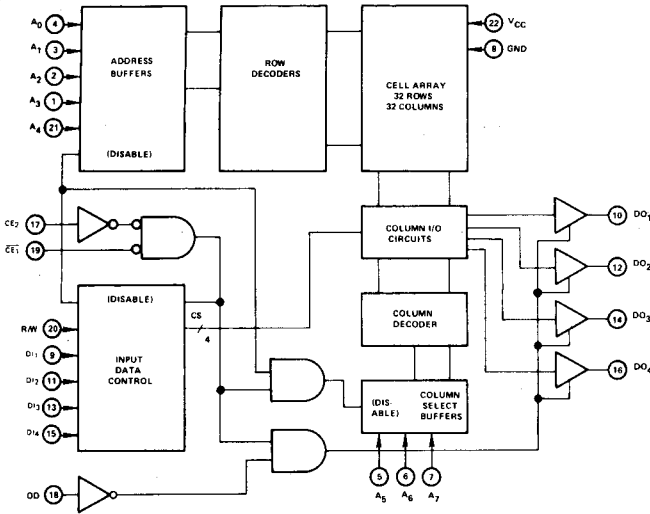


### PIN NAMES

DI <sub>1</sub> - DI <sub>4</sub>	Data Input
A <sub>0</sub> - A <sub>7</sub>	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$ , $CE_2$	Chip Enables
OD	Output Disable
DO <sub>1</sub> - DO <sub>4</sub>	Data Output
VCC	Power (+5V)

# μPD5101L

## BLOCK DIAGRAM



Operating Temperature ..... 0°C to +70°C  
 Storage Temperature ..... -40°C to +125°C  
 Voltage On Any Pin With Respect to Ground ..... -0.3 Volts to V<sub>CC</sub> +0.3 Volts  
 Power Supply Voltage ..... -0.3 to +7.0 Volts  
 T<sub>a</sub> = 25°C

## ABSOLUTE MAXIMUM RATINGS\*

\*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T<sub>a</sub> = 0°C to 70°C; V<sub>CC</sub> = +5V ± 5%, unless otherwise specified.

## DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input High Leakage	I <sub>LIH</sub> ②			1	μA	V <sub>IN</sub> = V <sub>CC</sub>
Input Low Leakage	I <sub>LIL</sub> ②			-1	μA	V <sub>IN</sub> = 0V
Output High Leakage	I <sub>LOH</sub> ②			1	μA	$\overline{CE}_1 = 2.2V, V_{OUT} = V_{CC}$
Output Low Leakage	I <sub>LOL</sub> ②			-1	μA	$\overline{CE}_1 = 2.2V, V_{OUT} = 0.0V$
Operating Current	I <sub>CC1</sub>			22	mA	V <sub>IN</sub> = V <sub>CC</sub> Except $\overline{CE}_1 \leq 0.65V$ , Outputs Open
Operating Current	I <sub>CC2</sub>			27	mA	V <sub>IN</sub> = 2.2V Except $\overline{CE}_1 \leq 0.65V$ , Outputs Open
Standby Current	I <sub>CCL</sub> ②			10	μA	V <sub>IN</sub> = 0 to 5.25V CE <sub>2</sub> ≤ 0.2V
Input Low Voltage	V <sub>IL</sub>	-0.3		0.65	V	
Input High Voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Output Low Voltage	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 2.0 mA
Output High Voltage	V <sub>OH1</sub>	2.4			V	I <sub>OH</sub> = -1.0 mA
Output High Voltage	V <sub>OH2</sub>	3.5			V	I <sub>OH</sub> = -100 μA

Notes: ① Typical values at T<sub>a</sub> = 25°C and nominal supply voltage.

② Current through all inputs and outputs included in I<sub>CCL</sub>.

## CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (All Input Pins)	C <sub>IN</sub>		4	8	pF	V <sub>IN</sub> = 0V
Output Capacitance	C <sub>OUT</sub>		8	12	pF	V <sub>OUT</sub> = 0V



T<sub>a</sub> = 0°C to 70°C; V<sub>CC</sub> = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t <sub>RC</sub>	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: 1TTL Gate and C <sub>L</sub> = 100 pF
Access Time	t <sub>A</sub>			650			450	ns	
Chip Enable (CE <sub>1</sub> ) to Output	t <sub>CO1</sub>			600			400	ns	
Chip Enable (CE <sub>2</sub> ) to Output	t <sub>CO2</sub>			700			500	ns	
Output Disable to Output	t <sub>OD</sub>			350			250	ns	
Data Output to High Z State	t <sub>DF</sub>	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t <sub>OH1</sub>	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t <sub>OH2</sub>	0			0			ns	



WRITE CYCLE

T<sub>a</sub> = 0°C to 70°C; V<sub>CC</sub> = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t <sub>WC</sub>	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts Input rise and fall times: 20 ns Timing measurement reference level: 1.5 Volt Output load: 1TTL Gate and C <sub>L</sub> = 100 pF
Write Delay	t <sub>AW</sub>	150			130			ns	
Chip Enable (CE <sub>1</sub> ) to Write	t <sub>CW1</sub>	550			350			ns	
Chip Enable (CE <sub>2</sub> ) to Write	t <sub>CW2</sub>	550			350			ns	
Data Setup	t <sub>DW</sub>	400			250			ns	
Data Hold	t <sub>DH</sub>	100			50			ns	
Write Pulse	t <sub>WP</sub>	400			250			ns	
Write Recovery	t <sub>WR</sub>	50			50			ns	
Output Disable Setup	t <sub>DS</sub>	150			130			ns	

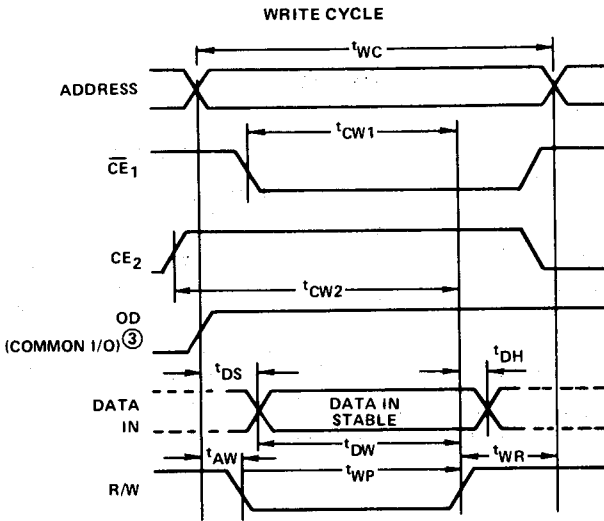
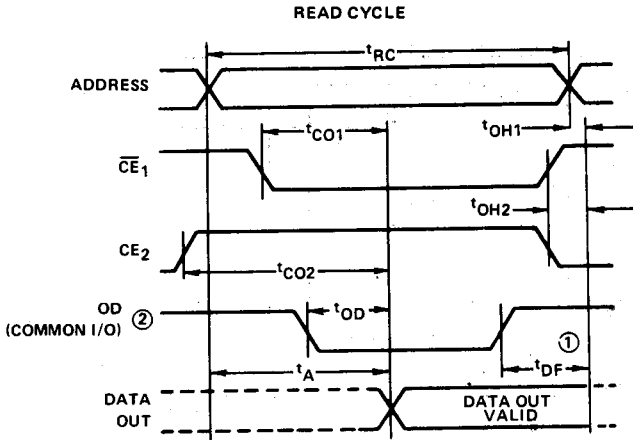
LOW V<sub>CC</sub> DATA RETENTION CHARACTERISTICS

T<sub>a</sub> = 0°C to 70°C

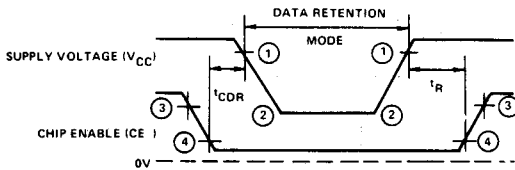
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V <sub>CC</sub> for Data Retention	V <sub>CCDR</sub>	+2.0			V	CE <sub>2</sub> < +0.2V
Data Retention Current	I <sub>CCDR</sub>			+10	μA	V <sub>CCDR</sub> = +2.0V CE <sub>2</sub> < +0.2V
Chip Deselect Setup Time	t <sub>CDR</sub>	0			ns	
Chip Deselect Hold Time	t <sub>R</sub>	t <sub>RC</sub> ①			ns	

Note: ① t<sub>RC</sub> = Read Cycle Time

**TIMING WAVEFORMS**

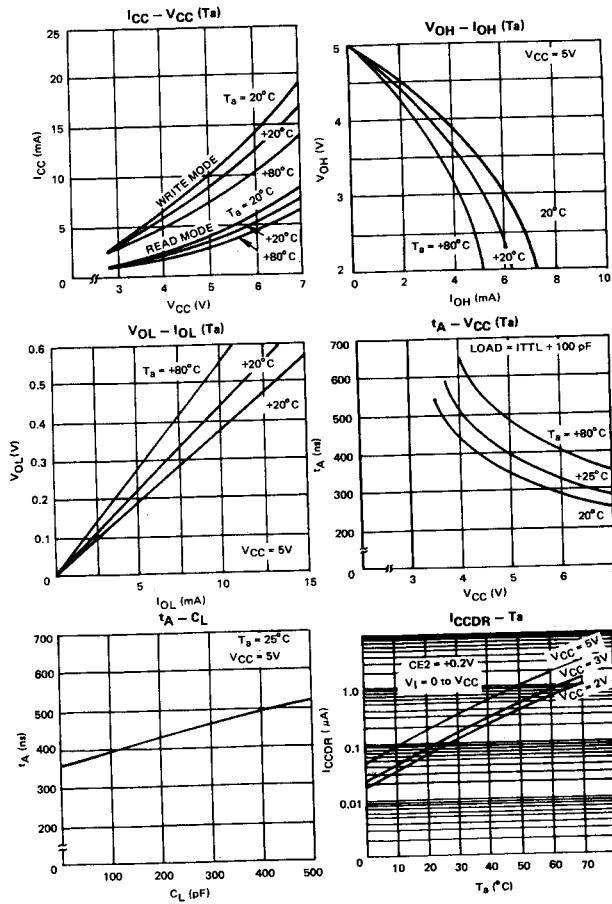


- Notes:
- ① Typical values are for  $T_a = 25^\circ\text{C}$  and nominal supply voltage.
  - ② OD may be tied low for separate I/O operation.
  - ③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.



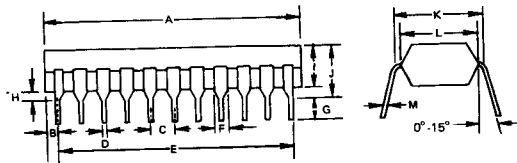
- Notes:
- ① 4.75V
  - ②  $V_{CCDR}$
  - ③  $V_{IH}$
  - ④ 0.2V

TYPICAL OPERATING CHARACTERISTICS



3

PACKAGE OUTLINE  
μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 0.10	0.02 0.004
E	25.4	1.0
F	1.40	0.065
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	+0.10 0.25 0.06	+0.004 0.01 0.002

5101LDS-REV1-12-81-CAT

PARTS LIST  
FOR  
MEMORY UNIT  
MODEL NDH-518

MARCH, 1982



*Japan Radio Co., Ltd.*

PARTS LIST

MEMORY UNIT

MODEL NDH-518

1. MEMORY CDD-206
2. DISPLAY CDE-162

The table lists parts in alphanumeric order of their reference designations "NO." (see abbreviations below), and provides the following information on each part:

- A. JRC code number.
- B. Type.
- C. Description of part.

**Ordering information**

To obtain replacement parts, address order or inquiry to our Japan Radio CO, LTD. Sales Offices. Identify parts by their JRC code number. To obtain a part that is not listed, included:

- A. Equipment model number.
- B. Equipment serial number.
- C. Description of the part.
- D. Function and location of the part.

**ABBREVIATIONS**

A	Assembly	MIC	Microphone
ANT	Antenna	MG	Motor generator
AR	Arrester	MP	Heat dissipating device (heatsink, etc.), mechanical part
AT	Attenuator	MR	Shunt, multiplier
B	Rotary machine	MT	Centering magnet
BEL	Bell	P	Plug
BT	Battery	PC	Printed circuit
BZ	Buzzer	I	Lamp
C	Fixed capacitor	IS	Lamp socket
CB	Circuit breaker	PU	Pick-up
CD	Rectifier, detector, diode, varistor	R	Fixed resistor, thermistor
CV	Variable capacitor	RS	Lead selector
D	Dynamotor	RV	Variable resistor
DC	Directional coupler	S	Switch, key, thermostat, interlock
DL	Delay line	SP	Speaker
E	Earth, ground	T	Transformer
F	Fuse	TH	Terminal board
FL	Filter	TC	Thermocoupler
FS	Fuse holder	TF	Tuning fork
G	Generator, vibrator	TP	Testpoint
HC	Hybrid circuit	TR	Transistor
HR	Thermostatic oven, heater	TRS	Transistor socket
HS	Handset	V	Electron tube
HT	Telephone receiver	VR	Voltage regulator
HY	Hybrid coil	VS	Electron tube socket
IC	Integrated circuit	W	Wire, cable, wave guide
J	Jack	X	Crystal
K	Relay	XD	Discriminator
KS	Relay socket	XS	Crystal socket
L	Inductor, coil	XU	Crystal oscillator
M	Meter	Z	Tuned cavity, pulse forming network, dummy

PARTS LIST

ORDER		TITLE		LIST NO.	SHEET NO.
		MEMORY		CDD-206	1
PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
BTS1	BT HOLDER				6Z7A801858
BTS2	BT HOLDER				6Z7A801858
BTS3	BT HOLDER				6Z7A801858
C1	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
5 C2	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C3	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C4	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C5	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C6	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
10 C7	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C8	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C9	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C10	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C11	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
15 C12	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C13	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C14	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C15	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C16	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
20 C17	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C18	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C19	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C20	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C21	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
25 C22	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C23	CAP, FXD CER	DD112SL102J50V02	50V 1000PF		5CA44A01112
C24	CAP, FXD PLSTC	FCD-41H104KZ	0.1UF		5CB4400123
C25	CAP, FXD FL CTLT	FCE-41ES100	25V10UF		5CE4401348
C26	CAP, FXD CER	DD109E103P50V02	50V 10000PF		5CB4800301
C27	CAP, FXD CER	DD109E103P50V02	50V 10000PF		5CB4800301
C28	CAP, FXD EL CTLT	FCE-41ES100	25V10UF		5CE4401348
C29	CAP, FXD CER	DD109E103P50V02	50V 10000PF		5CB4800301
C30	CAP, FXD CER	DD109E103P50V02	50V 10000PF		5CB4800301
C31	CAP, FXD FL CTLT	FCE-41ES100	25V10UF		5CE4401348
35 C32	CAP, FXD CER	DD109E103P50V02	50V 10000PF		5CB4800301

## PARTS LIST

ORDER		TITLE	LIST NO.	SHEET NO.	
MEMORY			CDD-206	2	
PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CONF
C33	CAP, FXD CTLT	EL	FCE-A1ES100	25V10UF	5CEAA01349
C34	CAP, FXD CTLT	EL	FCE-A1ES101	25V100UF	5CEAA01349
C35	CAP, FXD CER		00112SL102J50V02	50V 1000PF	5CAAA01112
C36	CAP, FXD CER		00112SL102J50V02	50V 1000PF	5CAAA01112
5 C37	CAP, FXD CER		00112SL102J50V02	50V 1000PF	5CAAA01112
C04	DIODE	10D2		200V 1A	5TXAG00001
C05	DIODE	1S1589LB-10			5TXA000248
C06	DIODE	1S1589LB-10			5TXA000248
C07	DIODE	HZ3HC1			5TXAE00118
10 C08	DIODE	10D8			5TXAG00002
IC1	IC	UPD5101LC			500AC00151
IC2	IC	UPD5101LC			500AC00151
IC3	IC	UPD5101LC			500AC00151
IC4	IC	UPD5101LC			500AC00151
15 IC5	IC	UPD5101LC			500AC00151
IC6	IC	UPD5101LC			500AC00151
IC7	IC	HD74LS47P			5004F00390
IC8	IC	HD74LS47P			5004F00390
IC9	IC	SN74LS126AN			5004L00422
20 IC10	IC	SN74LS126AN			5004L00422
IC11	IC	SN74LS126AN			5004L00422
IC12	IC	SN74LS126AN			5004L00422
IC13	IC	SN74LS126AN			5004L00422
IC14	IC	SN74LS126AN			5004L00422
25 IC15	IC	TC4049BP			5004F00044
IC16	IC	TC4049BP			5004F00044
IC17	IC	HA17905P			50A1600067
J1	CONNECTOR	PCN6-20PA-2.5DS	20P		5J0AA00049
J5	CONNECTOR	HNC2-2.5P-10DS	10P		5J0AA00275
J6	CONNECTOR	HNC2-2.5P-10DS	10P		5J0AA00275
J7	CONNECTOR	HNC2-2.5P-10DS	10P		5J0AA00275
K1	RELAY	RF-HD-5V			5KLA000039
L1	COIL	LF1-100K	10UH		5LCA000001
P4	CONNECTOR	H-67CJ000012			6ZCJ000012
35 P5	CONNECTOR	HNC2-2.5S-10	10P		5J0AA00277



PARTS LIST

CRDEC		TITLE		LIST NO.	SHEET NO.
		MEMORY		CDD-206	3
PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
P6	CONNECTOR	HNC2-2.55-10	10P		5JDA000277
P7	CONNECTOR	HNC2-2.55-10	10P		5JDA000277
PC1	PCR	MPPC0895R			MPPC0895R
R1	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R2	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R3	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R4	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R5	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R6	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R7	RESISTOR	IHR-1/8-4-471JR	1/8W 470 Ω HM X4		5FZAR00024
R8	RESISTOR	IHR-1/8-4-471JB	1/8W 470 Ω HM X4		5FZAR00024
R9	RESISTOR	IHR-1/8-4-471JR	1/8W 470 Ω HM X4		5FZAR00024
R10	RESISTOR	IHR-1/8-4-471JB	1/8W 470 Ω HM X4		5FZAR00024
R11	RESISTOR	ERD-25UJ471	1/4W 470 Ω HM		5FZAR001337
R12	RESISTOR FXD	ERD-25UJ472	1/4W 4.7K OHM		5FZAR001361
R13	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R14	RESISTOR	IHR-1/8-4-473JA	1/8W 47K Ω HM X4		5FZAR00029
R15	RESISTOR FXD	ERD-25UJ472	1/4W 4.7K OHM		5FZAR001361
R16	RESISTOR FXD	ERD-25UJ473	1/4W 47K Ω HM		5FZAR001395
R17	RESISTOR FXD	ERD-25UJ102	1/4W 1K Ω HM		5FZAR001345
R18	RESISTOR FXD	ERD-25UJ271	1/4W 220 Ω HM		5FZAR001329
R19	RESISTOR FXD	ERD-25UJ471	1/4W 470 Ω HM		5FZAR001337
R20	RESISTOR FXD	ERD-25UJ104	1/4W 100K OHM		5FZAR001393
R21	RESISTOR FXD	ERD-25UJ105	1/4W 1K Ω HM		5FZAR001417
R22	RESISTOR FXD	ERD-25UJ105	1/4W 1K Ω HM		5FZAR001417
R23	RESISTOR FXD	ERD-25UJ330	1/4W 33 Ω HM		5FZAR001309
R24	RESISTOR FXD	ERD-25UJ473	1/4W 47K Ω HM		5FZAR001395
R25	RESISTOR FXD	ERD-25UJ473	1/4W 47K Ω HM		5FZAR001395
S1	SWITCH	H-6SSJ000014	6BITS L=30 HM		6SSJ000014
S2	SWITCH	H-6SCJ000115			6SCJ000115
S4	SWITCH	H-6SCJ000114			6SCJ000114
T91	TRANSISTOR	2SC1815-Y			5TCAR00219
T92	TRANSISTOR	2SC1815-Y			5TCAR00219

PARTS LIST

CODE		TITLE	LIST NO.	SHEET NO.	
DISPLAY		CDE-167			
PART NO.	PART NAME	TYPE	DESCRIPTION	REMARKS	CODE
CD1	LED	TLR313			5T7A000003
CD2	LED	TLR313			5T7A000003
CD3	LED	TLG103	GREEN		5T2A000023
P1	CONNECTOR	PCN6-20S-2.50S			5J0AA00000
PC2	PCB	MPPC07987			MPPC07987

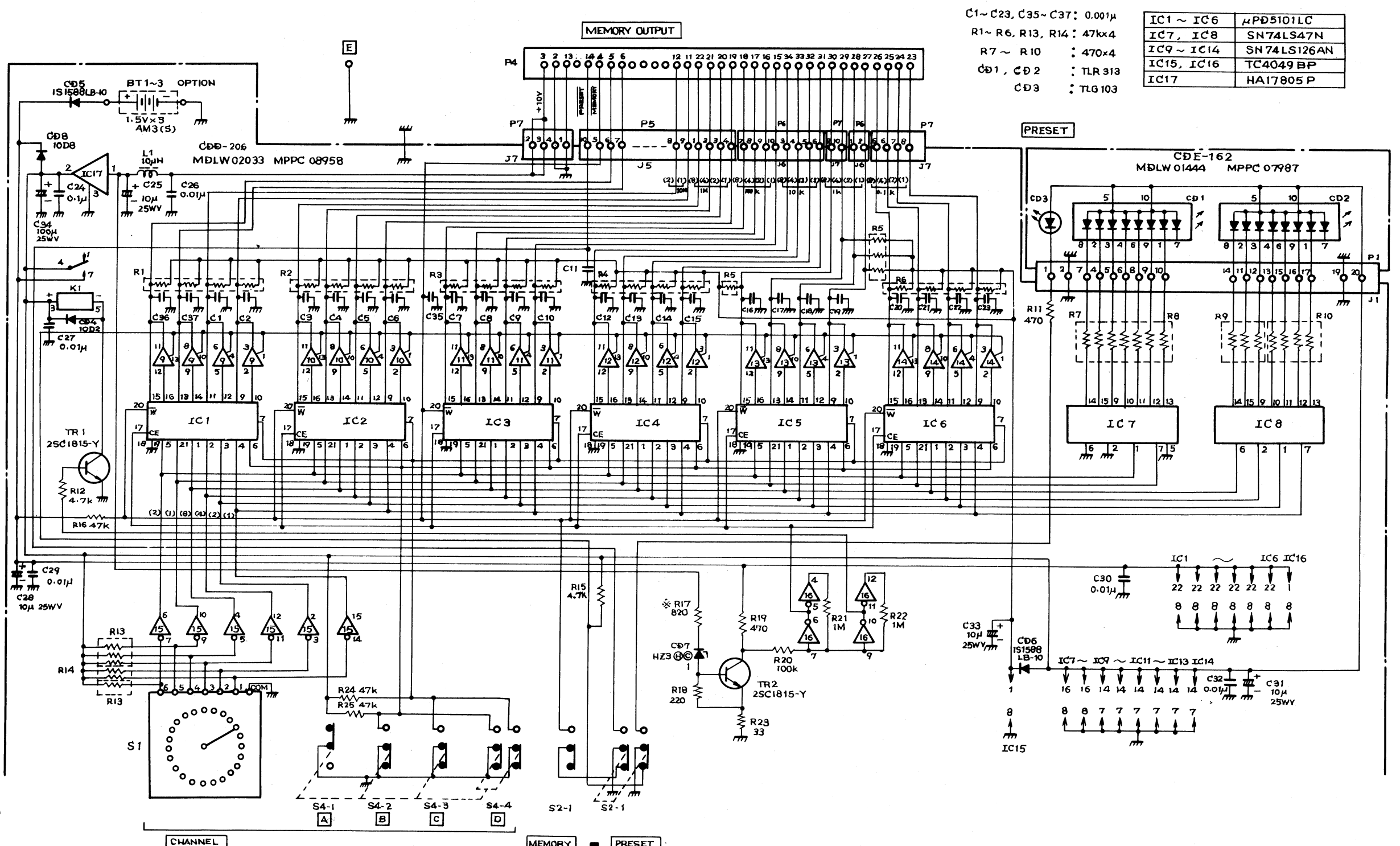
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C1~C23, C35~C37: 0.001μ  
 R1~R6, R13, R14: 47kx4  
 R7~R10: 470x4  
 CD1, CD2: TLR 313  
 CD3: TLR 103

IC1 ~ IC6	μPD5101LC
IC7, IC8	SN74LS47N
IC9 ~ IC14	SN74LS126AN
IC15, IC16	TC4049BP
IC17	HA17805P

注 1) 特記外の抵抗は全てΩおよび1/4Wを示し容量はpFを示す。  
 2) \*印は調整用部品を示す。  
 NOTES 1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS CAPACITANCES ARE IN MICRO-MICRO FRADS.  
 2. \* VALUES SELECTED IN MANUFACTURE.

付図 1  
 NDH-518  
 メモリユニット接続図  
 MEMORY UNIT SCHEMATIC DIAGRAM  
 APPENDIX 1  
 1/1