



HF SSB Transceiver

8525B/8528 series

Technical Service Manual

Volume 1

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General Information

1.1 Introduction

The Type 8525B Series and 8528 Series transceivers feature synthesized frequency generation and have sealed membrane controls. The two series differ only in control and display facilities. All differences are in the front panel and the controlling EPROM. All transceiver functions are controlled by a central microprocessor, enabling facilities such as clarifier, emergency call, etc to be included as standard fit.

The 8525B comprises two versions: one for front panel control and one for extended control. The extended control transceiver has a blank front panel and is connected by up to 100 metres of cable to an 8530 control head. The control head may also be used with the front control version allowing for both local and extended control. Channel capacity of the 8525B is 99 single or two-frequency simplex channels in EPROM, and channel display is by a two-digit LED whose brightness is controlled by ambient illumination.

The 8528 series comprises two basic models: the land-based 8528 and the marine 8528S. Two versions of each model are available: one for front control and one for extended control. The extended control transceiver has a blank front panel and is connected by up to 100 metres of cable to an 8532 or 8531S control head. The control head may also be used with the front control version allowing for both local and extended control.

Channel capacity of the 8528 is 501 single or two frequency simplex channels in EPROM and 99 channels in EEPROM. Transmit frequencies may be front-panel entered by a qualified technician or where permitted, by the operator. Receive frequencies may be entered by the operator.

The 8528 series has a twenty-digit liquid crystal display showing the transmit and receive frequencies and channel number, or selective call send and receive identification. Selective call addresses may be entered by keypads on the 8528.

For transmission power in excess of 100W, the internal PA in the 8528S is replaced by a PA driver and an external HF4000 series PA is used. The external PAs are covered in a separate Technical Service Manual.

1.2 Specifications

Specification figures will normally be exceeded by production equipment. Where relevant, acceptance limits are given in parentheses. All measurements are made at 13.6V DC, 50Ω source and load, and 25°C ambient temperature (unless otherwise specified).

1.2.1 General

Specifications cover	8525B series; 8528 series including 8528S and H versions. (H transmission specifications included in a separate Technical Service Manual (code 2037), covering the 4402 and 4404 PA units).
Frequency Range	Transmit: 2 to 24MHz Receive: 0.25 to 30MHz
Frequency Generation	All frequencies generated by synthesizer.
Channel Capacity	8525B: 99 single or two-frequency simplex channels with 10Hz resolution controlled by plug-in EPROM 8528: single or two-frequency simplex channels with 10Hz resolution controlled by plug-in EPROM and 99 EEPROM controlled channels with 100Hz resolution. The total number of channels will depend on the version of 8528 series to a maximum of 600. Receive frequencies of the EEPROM—controlled channels can be entered from the front panel by the operator. Transmit frequencies of the EEPROM—controlled channels can be entered from the front panel by qualified technical personnel or (where authorised) by the operator.
Operating Modes	Land: Single sideband (J3E) USB, with LSB (Option L) or switched sideband (Option LU) available as options. Marine: Single sideband (J3E) USB. LSB may be programmed for specific frequencies (requires Option L). On 2182kHz J3E or H3E USB selectable.
Frequency Stability	USB: ±2(3)ppm –30°C to +60°C LSB: ±2(3)ppm ± 20Hz –30°C to +60°C
Long term ageing	1ppm per year.

Oven warm-up time	1 minute.
Controls	Sealed membrane switches.
Indicators	Refer to illustrations for details. 8525B: All indicators except Tx automatically dimmed for low ambient light levels. 8528: All indicators except Tx may be manually dimmed by front panel controls if required.
Transmit/Receive Switching	Approximately 20ms using the Option PS connection. Transmit/receive frequencies may be separated by up to 1MHz.
Connectors	RF—UHF connector Extended/Local control (Option R) required for Control Head operation or remote control. Antenna control Extension Loudspeaker External Selective Call (Option PS) External Alarm (for Options SDE and SDEM) and/or unswitched battery for remote control (Option PP) Note: Options PS and PP are mutually exclusive.
RF Input/Output Impedance	50 ohms nominal.
Supply Voltage	12V DC nominal, negative earth. Normal operating range 10.5 to 15V DC. Maximum operating range 9 to 16V DC.
Overvoltage Protection	Shutdown at 16V DC (nominal) for duration of overvoltage.
Supply Current	8525B: Receive, no signal 400–550mA 8528: Receive, no signal, display illumination on: 400mA; off: 340mA Transmit: see section 1.2.3

Environmental

Ambient Temperature	Relative Humidity
–30°C to +30°C	95%
+30°C to +60°C	from 95% at +30°C to 30% at +60°C

Derate upper ambient temperature by 1°C per 330m above sea level.

Cooling	Convection or fan (Option F).
Size and weight	<p>Transceiver only: 250mm W x 78mm H x 350mm D; 3.41kg</p> <p>With mounting cradle: 270mm W x 90mm H x 350mm D; 3.92kg</p> <p>8530 Control Head: 180mm W x 65mm H x 70mm D</p> <p>With mounting bracket: 190mm W x 78mm H x 70mm D; 700g</p> <p>8531 Control Head: 248mm W x 78mm H x 70mm D</p> <p>With mounting bracket: 252mm W x 92mm H x 70mm D; 900g</p> <p>Note: Depth measurements (D) include rear connectors/cables.</p>
Finish	<p>Case: Silver-grey Panel surround and heat sink: Matt black Panel overlay: Lexan—Matt black</p> <p>Painted surfaces are scratch-resistant textured polyester powdercoat.</p>

1.2.2 Receiver

Type	Dual conversion superheterodyne.								
IF Frequencies	45MHz, 1650kHz.								
Sensitivity	<table> <tr> <td>0.25 to 0.5MHz:</td> <td>Not specified</td> </tr> <tr> <td>0.5 to 2MHz:</td> <td>Approximately 8μV PD</td> </tr> <tr> <td>2 to 28MHz:</td> <td>0.25(0.35)μV PD [–119(–116)dBm] for 10dB SINAD with greater than 50mW audio output.</td> </tr> <tr> <td>28 to 30MHz:</td> <td>0.5μV PD</td> </tr> </table>	0.25 to 0.5MHz:	Not specified	0.5 to 2MHz:	Approximately 8 μ V PD	2 to 28MHz:	0.25(0.35) μ V PD [–119(–116)dBm] for 10dB SINAD with greater than 50mW audio output.	28 to 30MHz:	0.5 μ V PD
0.25 to 0.5MHz:	Not specified								
0.5 to 2MHz:	Approximately 8 μ V PD								
2 to 28MHz:	0.25(0.35) μ V PD [–119(–116)dBm] for 10dB SINAD with greater than 50mW audio output.								
28 to 30MHz:	0.5 μ V PD								
Input Protection	Will withstand 50V rms RF from a 50 Ω source.								
Selectivity	<p>Greater than 70(65)dB at –1kHz and +4.2kHz ref SCF USB.</p> <p>Pass band –6(–8)dB 300 – 2800Hz.</p> <p>Ripple 1.5(3)dB pp 500 – 2500Hz.</p>								

Desensitisation	10dB SINAD reduced to 7dB SINAD. -1 and +4.4kHz ref SCF (USB) 62(55)dB. ±10kHz 85(80)dB. ±50kHz 100(95)dB.
Image Rejection	Better than 90(80)dB
Spurious Responses	Better than 90(70)dB. Self generated signals >0.25µV PD; 6.6MHz, 9.998MHz, 13.2MHz, 19.8MHz, 26.4MHz.
Cross Modulation	A signal 90(85)dB above a signal producing 10dB SINAD, modulated 30% and removed at least 20kHz from the wanted signal will produce an increase in receiver noise of less than 3dB.
Blocking	As for desensitisation.
Intermodulation	To produce a third order intermodulation product equivalent to a wanted signal producing 10dB SINAD, two unwanted signals greater than 30kHz removed from the wanted signal must have a level greater than 85(80)dB above the wanted signal. Third order intercept +10(7)dBm, not affected by AGC.
AGC	Less than 6dB variation in output level for input variations between 1.5(2.5)µV and 100mV PD. Fast attack, slow release.
AF Response	-1 typ(-3)dB 300 to 2800Hz.
AF Power and Distortion	2.5W into 8 ohms: 5% THD 5W into 4 ohms: 5% THD 8W into 2 ohms: 5% THD
Clarifier	Land: Nominal ±0.001% Marine: ±180Hz Clarifier is automatically reset to mid-range with channel change.
Inband IMD	Better than 25dB IMD with two 50mV PD RF inputs.
Signal to noise vs Input Level	5µV PD: 34dB S/N 50µV PD: 53dB S/N 500µV PD: 60dB S/N

1.2.3 Transmitter

Power Output Land	100W PEP at 2MHz falling linearly with frequency to 90W PEP at 24MHz ± 0.5 dB.
Marine	125W PEP at 2MHz falling linearly with frequency to 90W PEP at 24MHz ± 1 dB. CW or single tone: approximately 60% of PEP with average PEP control.
Duty Cycle	100% normal speech over full temperature range. 100% ARQ up to 30°C. 25% continuous data mode (5 minutes on maximum) at ambient temperature up to 30°C. 100% all modes up to maximum ambient of 45°C with Option F.
Supply Current	Output power 100/125W 2-tone or CW: 9 to 12A Average speech: 6A for battery life calculations.
Protection	Safe under all load conditions by limiting reflected power to 6W and limiting PA transistor collector voltage swing. Thermal protection against excessive heatsink temperature.
AF Response	Overall response of microphone and transmitter rises approximately 6dB/octave 300 – 2800Hz. Electrical input $-6(-8)$ dB, 300 – 2800Hz. Ripple 1.5(3)dB pp, 500 – 2500Hz.
Spurious & Harmonic Emissions	Better than 60(48)dB below PEP.
Carrier Suppression	60(50)dB below PEP.
Unwanted Sideband	50(45)dB below PEP (400Hz) 70(65)dB below PEP (1kHz)
Intermodulation Distortion 2-tone Test	100W: 32(26)dB below each tone 38(32)dB below PEP 125W: 30(26)dB below each tone 36(32)dB below PEP

ALC	A 10dB increase in input level above compression threshold produces less than 0.5dB increase in power output. Maximum ALC range greater than 30dB. ALC attack time approximately 1ms.
Residual Noise	65(55)dB below PEP in 3kHz channel.
Transmitter Noise Floor	Transmitter noise output below cut-off frequency of harmonic filter in 3kHz bandwidth typically -67dBm.
Microphone	Dynamic type with push-to-talk switch fitted in case.

1.2.4 Rear Panel Connectors

The following tables show the pin connections, functions, and signal levels for the rear connectors.

Antenna Select Facility (15-way, D-type Socket)

Pin Number	Function	Signal Level
1	Channel Number Bit 3	Logic (Open Collector)
2	Channel Number Bit 4	Logic (Open Collector)
3	N/C	
4	TUNE IN/OUT	5V Logic (Active Low)
5	SCAN (Active Antenna)	Logic (Open Collector)
6 & 7	N/C	
8	PTT out	+10V (1k Ω source)
9	Channel Number Bit 1	Logic (Open Collector)
10	Channel Number Bit 2	Logic (Open Collector)
11	TUNED IN	5V Logic (Active Low)
12 & 13	A rail	+ Battery supply out
14 & 15	0V	Ground

N/C = Not Connected

All channel number bits active high. (Pull-up resistors required).

Option R (15-way, D-type Plug)

Pin Number	Function	Signal Level
1	Loudspeaker	Ref Spec
2	Remote PTT	0 Volts = PTT
3	Receiver Audio Output	Special *
4	Power On	Momentary 0V for Power ON
5	Data	5 Volt Logic
6	Data Line Enable	5 Volt Logic
7	Clock	5 Volt Logic
8	Transmit Lamp	Modulated by Tx output
9 & 10	0V	Ground
11	Transmit Audio I/P	Nom. 1.5Vpp (8k Ω input impedance)
12	Receiver Demodulator O/P	Nom. 1.5Vpp (1k Ω output impedance) (Min. load 5k Ω)
13	Receiver Audio I/P	Special*
14	Interrupt	5 Volt Logic
15	A rail	+ Battery supply out

* Special: adjusted to suit attached equipment

Option PS

Note: Option PS cannot be fitted with internal option SDE or SDEM.

Pin Number	Function	Signal Level
1	0V	Ground
2	Rx FSK Tones Output	Nom. 1.5Vpp (From 2k ohms)
3	FSK Tx Tones Input	3Vpp (22k ohm Input Impedance)
4	Quiet Line	+10V (ON) or floating (OFF)
5	Alarm Tones I/P	3Vpp into 100K ohms
6	PTT	Input: 0V = PTT
7	Scan	+10V output in scan
8	A rail	+ Battery supply out

Options SDE, SDEM (External Alarm) and PP (Supply for remote control)

Note: Options SDE or SDEM cannot be fitted with Option PS.

Pin Number	Function	Signal Level
1	Unswitched Supply	Battery +ve (PP only)
2 & 3	External Alarm	Contacts rated at 50V 1A DC. Closed when external alarm required.
4	Unswitched Supply	Ground (PP only)

1.2.5 Front Panel Connector

Microphone Connector

Pin Number	Function
1	PTT ground
2	PTT active low
3	Microphone input
4	Microphone ground
5	Speaker connection*
6	Audio output
7	Audio output

*Linked to pin 7 for front panel speaker operation.

1.3 Options and Accessories

1.3.1 Options

The following is a list of the options available with brief descriptions. The references in brackets indicate more detailed descriptions will be found in those sections of this manual.

AD	Fit antenna driver interface for 8558 automatic tuning whip antenna.
F	Fit fan for continuous data transmission.
LF	1.6 to 2MHz—Receive at 0.25 μ V sensitivity.
LU	Fit for USB and LSB operation on selected channels. USB or LSB selected on front panel (land only) (4.4.5).
L	Fit for LSB only operation on selected channels (4.4.5).
M*	CW facility (4.6.7).
PH*	Headphone output (4.6.6).
PP	Fit unswitched battery power output facility.
PS	External selective call interface (4.13).
R*	Extended/remote control interface (4.6.3).
SE	Programmable 4 digit (internally preset) selective call encoder (4.11).
SDE	Programmable 4 digit (internally preset) selective call encoder/decoder (4.11).
SDEM	Front panel programmable 4 digit (mesh) selective call encoder with (internally preset) decoder: 8525B only (4.11).
SD	Fit Selective Call Decode: 8528/8528S only.
TD	Tone-operated decoder: (4.12).

* Required for front control transceivers only.

Programmable Options (per channel)

E	RFDS Emergency call.
O	Transmit clarifier (land only).
TE	Program two-tone encode (specify frequency).
SE	Program Selective Call Encode: 8528/8528S only.
INHIBIT	Receive only.

1.3.2 Accessories

The following is a list of the accessories available.

Code

112	Vehicle installation hardware kit.
114	Marine suppression kit.
117	Vehicle mounting cradle—front entry.
118	Vehicle mounting cradle—top/bottom entry. Supplied complete with transceiver DC power cable (6 metres).
121	2-module clamp suitable for locking transceiver with another unit of compatible mechanical design.
164	Rack mounting frame 483mm (19").
602	Headphone complete with cable and connector.
654	Telephone handset complete with cable and connector.
641	Desk microphone complete with cable and connector.
649	Extension loudspeaker.
651PC	Program package (8525B/8528 series). For use with IBM compatible PC.
652	Morse key complete with base, cable and connector.
704	Vehicle interference suppression kit.
726	Channel decoder (1 of 14)—active low. For use with relay switched antenna systems.
2036	Service manual for type 8528 series.
2037	Service manual for type 4402 and 4404.
Type 8530	Control head complete with 6 metres of interface cable fitted with connectors and plug-in hand PTT microphone. Suitable for transceiver 8525B. (Requires Option RS to be fitted to the transceiver).
Type 8531	As above, suitable for 8528. (Requires Option R to be fitted to the transceiver).
Type 8531S	As above, suitable for 8528S. (Requires Option R to be fitted to the transceiver).
Type 8532	As above, suitable for 8528. (Requires Option R to be fitted to the transceiver).

1.4 Abbreviations

A/D	Analog to digital
A/F	Across flats (hexagon)
AC	Alternating Current
ACIA	Asynchronous Communication Interface Adapter
ADJ	Adjust
AF	Audio Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ALC	Automatic Level Control
ALF	Absorption Limited Frequency
AM	Amplitude Modulation
ASCII	American Standard Code for Information Interchange
ASSY	Assembly
ATU	Antenna Tuning Unit
AUX	Auxiliary
AV	Average
BAL	Balance
BALUN	Balanced to Unbalanced Transformer
BCD	Binary Coded Decimal
BPF	Band Pass Filter
BW	Bandwidth
C/O	Change-over
CAL	Calibrate
CCT	Circuit
CCW	Counterclockwise
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor
COAX	Coaxial
COM	Common
CPU	Central Processing Unit
CRO	Cathode Ray Oscilloscope
CRT	Cathode Ray Tube
CSK	Countersink

CW	Continuous Wave, Carrier Wave or Clockwise
D/A	Digital to Analog
DC	Direct Current
DEMUX	Demultiplexer
DMA	Direct Memory Access
DPDT	Double Pole, Double Throw
DPST	Double Pole, Single Throw
DRG	Drawing
DSB	Double Sideband
DTL	Diode Transistor Logic
DVM	Digital Voltmeter
dB	Decibel
dBm	Decibel relative to 1mW
EAPROM	Electrically Alterable Programmable Read Only Memory
ECL	Emitter Coupled Logic
EDP	Electronic Data Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
EMF	Electromotive Force
EMI	Electromagnetic Interference
EPROM	Erasable Programmable Read Only Memory
EXT	External
F/V	Frequency to Voltage
FET	Field Effect Transistor
FM	Frequency Modulation
FREQ	Frequency
FSK	Frequency Shift Keying
FTTL	Fast Transistor Transistor Logic
GND	Ground
GPIO	General Purpose Interface Bus
HCMOS	High Speed Complementary Metal Oxide Semiconductor
HEX	Hexadecimal or Hexagon
HF	High Frequency
HMOS	High Speed Metal Oxide Semiconductor
HORIZ	Horizontal

HPF	High Pass Filter
I/COM	Intercom
I/F	Interface
I/O	Input Output
I/P	Input
IF	Intermediate Frequency
IMD	Intermodulation Distortion
INT	Internal
ISB	Independent Sideband
JFET	Junction Field Effect Transistor
J3E	Single Sideband Suppressed Carrier Telephony Emission
LC	Inductance-Capacitance
LCD	Liquid Crystal Display
LDR	Light Dependent Resistor
LED	Light Emitting Diode
LF	Low Frequency
LIN	Linear Law
LNA	Low Noise Amplifier
LO	Local Oscillator
LOG	Logarithmic Law
LPF	Low Pass Filter
LS	Loudspeaker or Low Power Schottky
LSB	Lower Sideband or Least Significant Bit
LSI	Large Scale Integration
LSTTL	Low Power Schottky Transistor Transistor Logic
LTU	Line Terminating Unit
MAX	Maximum
MF	Medium Frequency
MIN	Minimum
MODEM	Modulator-Demodulator
MOL	Maximum Operating Level
MOS	Metal Oxide Semiconductor
MPU	Microprocessor

MSB	Most Significant Bit
MSI	Medium Scale Integration
MUF	Maximum Useable Frequency
MUX	Multiplex, Multiplexer
N/C	Normally Closed
N/O	Normally Open
NC	Not Connected
NMOS	N Type Metal Oxide Semiconductor
NOL	Normal Operating Level
NOM	Nominal
NORM	Normal
NPO	Zero Temperature Coefficient
NTC	Negative Temperature Coefficient
O/C	Open Circuit
ODU	Outdoor Unit
OMT	Orthomode Transducer
O/P	Output
OPR	Operator
OPT	Option
OSC	Oscillator
OWF	Optimum Working Frequency
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Potential Difference
PEP	Peak Envelope Power
PH	Phase
PIA	Peripheral Interface Adapter
PIV	Peak Inverse Voltage
PKG	Package
PLL	Phase Locked Loop
PMOS	P Type Metal Oxide Semiconductor
POL	Peak Operating Level

POT	Potentiometer
PP	Peak to Peak
PPM	Parts per Million
PROM	Programmable Read Only Memory
PSU	Power Supply Unit
PTC	Positive Temperature Coefficient (Resistor)
PTT	Push To Talk
PUT	Programmable Unijunction Transistor
PWM	Pulse Width Modulation
RAM	Random Access Memory
R/C	Remote Control
RC	Resistance-Capacitance
RCU	Remote Control Unit
REF	Reference
REG	Regulated, Register
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root Mean Square
ROL	Reference Operating Level
ROM	Read Only Memory
RTL	Resistor Transistor Logic
RTTY	Radio Teletype
Rx	Receive, Receiver
S/C	Short Circuit
S/N	Signal To Noise
(S+N)/N	Signal Plus Noise to Noise Ratio
SCF	Suppressed Carrier Frequency
SCR	Silicon Controlled Rectifier
SINAD	Signal + Noise + Distortion to Noise + Distortion Ratio
SMPS	Switching Mode Power Supply
SOT	Select On Test
SPDT	Single Pole Double Throw
SPST	Single Pole Single Throw

SSB	Single Sideband
STTL	Schottky Transistor Transistor Logic
SWR	Standing Wave Ratio
SYNC	Synchronisation
SYNTH	Synthesizer
T/R	Transmit Receive
TC	Temperature Coefficient
TCVR	Transceiver
TCW	Tinned Copper Wire
TCXO	Temperature Compensated Crystal Oscillator
TVRO	Television Receive Only
TDM	Time Division Multiplex
THD	Total Harmonic Distortion
TRIG	Trigger
TS	Tag Strip
TSM	Technical Service Manual
TTL	Transistor Transistor Logic
TYP	Typical
Tx	Transmit, Transmitter
UART	Universal Asynchronous Receiver Transmitter
UJT	Unijunction Transistor
USART	Universal Synchronous/Asynchronous Receiver Transmitter
USB	Upper Sideband
UT	Universal Time
UTC	Universal Co-ordinated Time
V/F	Voltage to Frequency
VA	Voltampere
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VDR	Voltage Dependent Resistor
VERT	Vertical
VFO	Variable Frequency Oscillator
VHF	Very High Frequency

VOX	Voice Operated Switch
VSWR	Voltage Standing Wave Ratio
VU	Volume Unit
WRT	With Respect To
WT	Weight
XTN	Extension
XTND	Extend
λ	Wavelength
+ve	Positive
-ve	Negative
\varnothing	Phase, Diameter in mm

Note: EMF is the source voltage behind the output resistance (R_s) and is independent of the signal generator loading. Many signal generators are calibrated in PD (across the load) assuming a total load resistance equal to the generator source resistance; for these, the EMF is twice the attenuator scale reading.

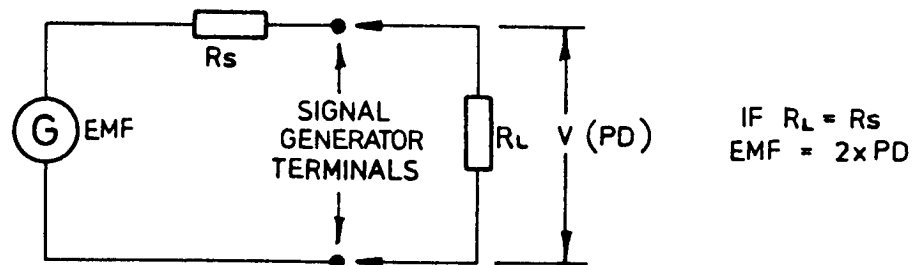


Figure 1.1 EMF Verses PD

1.5 Circuit Reference Designations

A	Assembly
B	Transducer—Microphone, Loudspeaker, etc
C	Capacitor
D	Diode—small signal and power
E	Heating device
F	Protection device—Fuse, etc
G	Generator—battery, etc
H	Signalling/indicating device—Lamp, LED, Buzzer, etc
IC	Integrated Circuit, thick film hybrid
J	Jack socket
K	Relay, key switch
L	Inductor
M	Indicating device—meter, etc
P	Plug
R	Resistor
S	Switch
T	Transformer, common mode choke
TP	Test Point
U	Modem, Modulator
V	Semiconductor (not including small signal and power diodes)
X	Terminals
Z	Quartz Crystal, Crystal Filter, Frequency Network

1.6 Units

A	Ampere	m	metre
C	Celsius (degrees)	min	minute
C	Coulomb	N	Newton
F	Farad	Pa	Pascal
g	gram	S	Siemen
h	hour	s	second
H	Henry	T	Tesla
Hz	Hertz	V	Volt
J	Joule	W	Watt
K	Kelvin (degrees)	Wb	Weber
l	litre	Ω	Ohms

1.7 Unit Multipliers

T	tera	one million million	10^{12}
G	giga	one thousand million	10^9
M	mega	one million	10^6
k	kilo	one thousand	10^3
h	hecto	one hundred	10^2
da	deca	ten	10
d	deci	one tenth	10^{-1}
c	centi	one hundredth	10^{-2}
m	milli	one thousandth	10^{-3}
μ	micro	one millionth	10^{-6}
n	nano	one thousand millionth	10^{-9}
p	pico	one million millionth	10^{-12}



3

Brief Description

3.1 General

This description should be read in conjunction with Block Diagram 03-00636.

The same frequency conversions are used in both transmit and receive modes, therefore many circuits are common to both modes of operation. Signal routing is determined by switching and control voltages according to the mode selected.

3.2 Receive

The RF signal from the antenna passes through the PA low-pass filters, then via the transmit/receive relay and broadcast filter on the PA PCB, to the switched high-pass filters on the RF, Mixer, and Dual Synthesizer PCB. Filters are automatically selected according to the frequency band in use.

The band-pass filtered signal is applied to the first mixer. This double-balanced, diode-ring mixer, driven from VCO1, converts the signal up to a 45MHz IF signal.

The 45MHz signal is amplified and filtered with a 20kHz wide 'roofing' filter. The output of this filter is mixed with the output of VCO2 in another double-balanced, diode-ring mixer. This produces a second IF of 1650kHz.

The second IF signal is passed to the IF amplifier and noise limiter. The noise limiter is designed to suppress impulse noises such as motor vehicle ignition noise. The limiter operates by 'gating' the IF signal path for the duration of the noise pulses.

The crystal filter on the Audio and 1650kHz IF PCB reduces the bandwidth to 2.5kHz before passing the signal to the 1650kHz tuned AGC controlled IF amplifier.

The signal is then demodulated to provide an audio signal which is fed via the mute gate to the digital volume control and audio PA where it is amplified before being passed to the speaker.

3.3 Transmit

The audio signal is amplified and levelled in the microphone amplifier and compressor, then fed to the balanced modulator where it is mixed with the 1650kHz (USB) or 1647kHz (LSB) local oscillator to produce a DSB signal. The resulting signal is filtered by the 2.5kHz crystal filter to produce the SSB signal (USB or LSB) required for transmission.

In the transmit mode, the IF amplifier is switched to produce a buffer to feed the mixer where the SSB signal is mixed with the output of VCO2 to produce the 45MHz IF signal.

After the 'roofing' filter, the signal is mixed with VCO1 output to produce the required channel frequency (2MHz to 24MHz). This is taken, via the transmit/receive switch, to the PA and Filter PCB where it is amplified and filtered (band-switched filters) before being passed to the antenna.

Forward and reflected power circuits are used to control the power amplifier. If a high VSWR is detected, the PA's output power is reduced to prevent damage.

3.4 Synthesizers

Two single-loop synthesizers are used, the main synthesizer (VCO1) generating a 45.25MHz to 75MHz signal i.e. 0.25 to 30MHz, plus 45MHz, in 2kHz steps, and a 'vernier' synthesizer (VCO2) generating 43.352 to 43.350MHz in 10Hz steps.

The synthesizers are controlled by the microprocessor which controls the transceiver. Serial data is loaded into both synthesizers; the data varying according to the required channel frequency preprogrammed into memory.

The system uses a single ovened crystal reference oscillator of 6.6MHz. This reference is also used to provide the 1650kHz (6.6MHz divided by 4) signal for the audio modulator/demodulator.

3.5 Display, Control and Switching

All the transceiver functions are microprocessor controlled with the required channel frequencies, facilities, etc being preprogrammed into an Erasable Programmable Read Only Memory (EPROM).

The front-panel and extended (8530, 8532 or 8531S) control head displays, and switch-pads are controlled via a four-wire serial bus.

Other functions such as filter switching, PTT and tone generation are controlled either by buffered microprocessor signals or the relay-switched 'C' and 'D' supply voltages. The microprocessor switches the associated relay (K1 on the Motherboard), depending on the transceiver mode. The relay is energised during transmit and de-energised in receive.

3.6 External Power Amplifiers

In suffix H transceivers, the PA is replaced by a PA Exciter Interface Assembly to drive an external PA assembly. The transceiver is powered from the external PA.



4

Technical Description

This section of the manual contains a detailed description of the circuitry used in the land and marine transceivers and associated control heads. Unless otherwise stated, the description applies equally to the 8525B, 8528 and 8528S transceivers.

All circuit paths of the following PCB assemblies are made through the Motherboard and Chassis (04-02453), where the connector and pin numbers of the interconnections are shown:

RF Mixer & Dual Synthesizer	(04-02450)
Audio & IF 1650kHz	(04-02093)
Microprocessor Controller	(04-02451 and 04-03031)
Display PCB	(04-02579) (8525B)
Display PCB, LCD	(04-02454) (8528)
PA & Filter	(04-02452)
PA/Exciter Interface	(04-02434)

4.1 Control and Supply Voltages

All switching, except 'power-on', is controlled either directly or indirectly by the microprocessor on the Microprocessor Controller PCB.

4.1.1 Supply Voltages

The supply voltages used are as follows:

- **'A' rail**—unregulated battery supply.
- **'B' rail**— +10 Volt regulated supply derived from the 'A' rail.
- **Volt supplies**—individual three-terminal regulators supplied from 'A' rail.
- **Volt supply**—'pump up' switching supply on the RF Mixer and Dual Synthesizer PCB (IC1).

4.1.2 Power and Control Lines

By controlling relay K1 on the Motherboard, the microprocessor on the Microprocessor Controller PCB generates two switched +10V power and control lines designated as the 'C' and 'D' rails. These rails are defined as follows:

- 'C' rail—+10 volts on receive; 0 volts on transmit.
- 'D' rail—0 Volts on receive; +10 Volts on transmit

All other control lines come directly from the Microprocessor Controller PCB and are described in section 4.5.

4.1.3 Overvoltage and Reverse Voltage Protection (refer Dwg 04-02452)

Overvoltage protection is provided by V3, V2, R4, R5 and V1 on the PA and Filter PCB. If the battery voltage rises above the 15V reference of V1, plus V2 V_{be} drop and the 0.6V diode drop of D6, transistor V2 turns on and hence turns off V3 to de-energise the power-on relay K7. This occurs at nominally 16V. Diode D6 provides reverse voltage protection.

4.1.4 Transceiver Power On/Off

When primary power is first applied to the transceiver, V3 on the PA and Filter PCB (04-02452) is turned on (by R5 to ground) charging C56 through D6 and K7 which momentarily pulses on. With primary power applied and in the power off condition, K7 is de-energised and the dual-coil latching relay K2 on the Motherboard (04-02453) is in the 'off' position.

Switching power on is a hardware operation; switching off is basically a software operation.

When the power on-off pad on the front panel is pressed, a ground is applied to the cathode of D4 on the Display PCB. This will forward bias V2 via R12 on the Motherboard. The emitter of V2 is connected to the positive supply via K7, V3 and D6 on the PA PCB. When V2 on the Motherboard conducts, latching relay K2 contacts close, operating the power-on relay K7. C56 ensures that there is sufficient current to toggle K2.

Operation of the on/off pad on a control head (when connected), switches on V2 via the rear panel connector P502 pin 4. This has the same effect as operation of the front panel on/off pad.

Once power 'on' has been established, the diodes connected to the power on/off switch-pad are reverse biased, and no longer affect the operation of those lines.

Pressing the power on/off pad with relay K2 set to 'on' has no effect on V2 on the Motherboard. However, via the front panel I²C bus control, the microprocessor grounds the Power Off line, J3 pin 5. This energises the 'off' coil of K2, toggling the relay back to its 'off' state. Contacts of K2 open to break the energising path for relay K7 on the PA and filter PCB.

4.1.5 High Power Transceiver Protection and Power On/Off

In place of the PA and Filter PCB, transceivers fitted for external PA operation have a PA/Exciter Interface PCB (08-03691). This does not contain overvoltage and reverse voltage protection circuits. In these transceivers the power supply is connected to the PA unit where reverse voltage protection is provided. Operation of the on/off pad on the transceiver grounds a line which is taken, via the PA Exciter Interface, to the PA unit. This energises relays in the unit which in addition to switching power on to the unit, also switch the supply back to the transceiver. The supply to the transceiver is taken, via the PA/Exciter Interface, to energise relay K2 and switch on the transceiver in the normal way.

4.2 Receiver

4.2.1 Input Filters (Refer 04-02452)

The receiver input signal is passed through the PA low-pass filter selected by the PA band line, the transmit/receive relay K6 and the 2MHz high-pass broadcast filter to the RF, Mixer & Dual Synthesizer PCB.

Option LF adds a 1nF capacitor C111 in parallel with C47, reducing the broadcast filters passband to 1.6MHz. D3 and D4 provide protection against excessive input signals.

4.2.2 Mixers, First IF Amplifiers and Filters (Refer 04-02450)

The receive input signal enters the PCB at pin 1 of J1. Five high-pass filters are used to complete the bandpass filter characteristics and are switched according to the frequency band in use by grounding the appropriate select line (the band 2.0 to 3.1MHz is not filtered on this board). From the selected filter, the received RF is passed via a 28MHz low-pass filter (C32 to C37 and L15 to L18) to the first mixer.

The first mixer is a double-balanced, diode-ring mixer consisting of transformers T1 and T2, and diode ring D13 to D16. The 0.25MHz to 30MHz signal is mixed with the output of VCO1 (45.25MHz to 75MHz) to produce the first IF signal, at 45MHz.

FETs V7 and V8 are switched as a grounded-gate amplifier through diodes D22 to D24 by the C rail being high and D rail being 0V. The amplified output is passed, via a crystal roofing filter Z1 (approx. 20kHz bandwidth) to FET V9.

FET V9 is switched as a source follower by the C and D rails through diodes D26 to D29. The output is applied to the second mixer, formed by transformers T5 and T6, and diode ring D31 to D34. The 45MHz signal is mixed with the output of VCO2 (43.350MHz to 43.352MHz) to produce the second IF signal at 1650kHz. This signal is passed to both the second IF amplifier and the noise blanker.

FETs V16 and V17 are switched to form the second IF amplifier as a grounded gate amplifier by the C and D rails through diodes D35 to D38.

4.2.3 Noise Blanker

The 1650kHz IF signal is amplified by the RC coupled stages V15 and V18 and fed to the tuned collector amplifier V20. V21 is an active rectifier. Noise bursts produce negative going pulses at the emitter of V21 which drives the monostable flip-flop V25 and V26. The output of V25 and V26 are complementary gating pulses which are fed to FET gates V23 and V24 respectively. With V23 on and V24 off, the IF signal is passed to the crystal filter. With V23 off and V24 on, the IF signal is blocked.

The average DC component of the collector current of V21 passing through R65 is amplified by V22 and applied as reverse AGC to V15 and V18. Thus only impulse type signals produce sufficient rectified output at V21 emitter to trigger the monostable. C119 sets the monostable pulse width such that the noise burst has finished before the IF is again enabled.

C rail biases off V15 and V18 in transmit and the noise blanker may be disabled for test purposes by grounding TP6.

4.2.4 IF Crystal Filter and Amplifier (04-02093)

The 1650kHz IF signal from the noise gate on the RF Mixer and Dual Synthesis PCB (V23, V24 04-02450) enters the board at P1 and is filtered by Z1 to pass 1647.2kHz to 1649.7kHz (2.5kHz bandwidth) to the two-stage AGC amplifier V2 and V3. IF output amplifier V4 drives the demodulator IC8 and the AGC active rectifier V6. AGC attack time is set by R21/C17 and release time by R24/C17, giving a fast attack/slow release response. Divider R23/R24 sets the AGC threshold level while the voltage set by the divider, combined with the gain of IC1a, IC1b and the bias on IC1b positive input, determines the static AGC voltage. D2 and D3 hold the sources of V2 and V3 positive to enable the AGC voltage applied to gate 2 of these FETs to go negative with respect to sources for full AGC control.

4.2.5 Demodulator

The IF from V4 is converted to the required audio output by double balanced mixer IC8. When receiving an RF USB signal, the IF signal is LSB with an SCF of 1650kHz due to the sideband inversion in the first mixer. With an RF LSB signal, the IF signal is USB with an SCF of 1647kHz. Thus the demodulator requires a 1650kHz local oscillator for USB reception and a 1647kHz local oscillator for LSB reception at P2. The oscillators are described in Section 4.4.5.

The audio output (pin 6) of IC8 passes through a third-order low-pass filter IC4a and associated components to remove noise above the wanted audio passband.

4.2.6 Audio Mute

The audio from the output of IC4a is looped back through the Motherboard to the Audio and IF 1650kHz PCB and applied to the audio mute input (R63/C37) and the mute gate (V12).

IC4b and IC3a are arranged as a squaring amplifier. The squared signal charges C38 via D8 during negative excursions and the charge is transferred to C39 by V13 during positive excursions. The resultant DC voltage on C39 is proportional to the frequency of the audio. IC3b and its associated components form a low-pass filter with a cut-off frequency of approximately 10Hz. The output from IC3b is a DC voltage varying at the syllabic rate of the received speech.

IC5a and IC5b form a window comparator whose window width is adjusted by R73, setting the mute sensitivity. The divider formed by R75 and R76, together with C42, averages the output of IC3b and provides the reference voltage for the window comparator. If the output from IC3b rises above or below this reference by the amount set by R73, then the output of either IC5a or IC5b will go high.

The comparator outputs are diode ORed into C43 to provide a fast attack, slow release (3 seconds) mute control signal.

The microcontroller on the Microprocessor Controller PCB can override the mute control circuit in two ways:

- It can force the unmuted condition by grounding the inverting input of IC6b (via J3 pin 9). This applies a high to the gate of V12 to switch it on.
- It can force the muted condition by grounding the gate of V12 via J3 pin 8.

The control circuit is also over-ridden at D7 by the C rail being taken to 0V in transmit. This forces the mute condition, thus preventing acoustic feedback during transmission.

4.2.7 Volume Control and Audio Amplifier

The post-mute audio from V12 is passed to the volume control section. The switches in IC9 control a resistive ladder network used as an attenuator. Sixteen steps are available with each step, giving approximately 4dB attenuation for a total of 64dB. The switches in IC9 are controlled by the microprocessor on the Microprocessor Controller PCB.

IC6a buffers the attenuated audio and passes it to the audio amplifier, IC10. The audio amplifier is capable of 8 Watts output into a 2 ohm load and gives approximately 2 Watts into the internal 8 ohm speaker.

4.3 Transmitter Exciter

4.3.1 Microphone Amplifier (Refer Dwg 04-02093)

The input to the microphone amplifier is J1, pin 6. Transistor V7 is an audio clamp which is released only when the microphone PTT button is pressed. This prevents the microphone picking up background noise and sidetone from the loudspeaker when transmitting emergency calls etc.

IC2a amplifies the microphone input to approximately 1V pp (gain=100). The signal is then connected to the AGC detector (IC2b, V10) and the modulator (IC8).

The output of IC2a to the AGC detector is fed directly to V10, and via inverter IC2b, to V11. Transistors V10 and V11 form a full wave rectifier to drive V9, which in turn drives V8 to complete the AGC loop by shunting the input signal to ground.

The release time-constant of the amplifier is set by R37 and C25. Diode D4 allows the gain to rise exponentially to maximum. The three-terminal regulator IC7 prevents power supply variations affecting the AGC circuit.

4.3.2 Modulator

The microphone amplifier output is capacitively coupled via C28 to the temperature compensating resistor network R55 and R56. R55 is an NTC resistor; as the temperature increases its resistance decreases and so the audio signal level passed to IC8 increases. This is to compensate for reduced gain at higher temperatures mainly in the 45MHz IF amplifier.

In the 8528S, the selection of the AM (H3E) mode forward biases V3 on the Motherboard (04-02453). This switches R17, R27 and C23 (also on the Motherboard) into circuit between the microphone amplifier output J1 pin 3 and ground. This attenuates the audio signal to the lower level required by the modulator in this mode. Link Y is inserted in H versions which reduces the audio drive by approximately 3dB to improve the exciter IMD products.

IC8 is the modulator during transmit and mixes the audio signal with the 1650kHz (1647kHz, LSB) local oscillator to produce a DSB signal output, centred on the LO frequency, from pin 12.

This signal is then passed via the transmit/receive switch V1 and D1 to the 1650kHz crystal filter.

4.3.3 Crystal Filter

One sideband of the DSB signal from the modulator is selected by the crystal filter to give an SSB signal. During transmit, the C rail is at 0 Volts, and forces a low output from IC1b for maximum AGC to V2 and V3. Thus, none of the transmit signal passes through the IF Amplifier.

4.3.4 Mixers, IF Filters, and IF Amplifier (Refer Dwg 04-02450)

The SSB signal from the crystal filter is applied to J4 on the RF Mixer and Dual Synthesizer PCB. As the C rail is at 0 Volts in transmit, the noise blanker is disabled, switching V23 on and V24 off.

V16 and V17 are switched as a source follower selected by the C and D rails, via diodes D35 to D37. The output is applied to the double-balanced, diode-ring mixer formed by T5, T6, and D31 to D34. Here the signal is mixed with the output of VCO2 (43.352 to 43.350MHz) to produce the 45MHz IF.

The 45MHz IF signal is amplified by V9 switched as a grounded-gate amplifier by C and D rails, via diodes D26 to D29. The amplified output is passed to the crystal roofing filter (Z1) to remove the unwanted mixer products.

V7 and V8 are switched as a source follower by the C and D rails, via diodes D22 to D25. The output is passed to the double-balanced, diode-ring mixer formed by T1, T2 and D13 to D16. Here the 45MHz IF signal is mixed with the output from VCO1 to produce the required channel frequency. This signal is filtered by the 28MHz low-pass filter then passed by D12 to the Power Amplifier input.

The receive band-switched filters are switched off while transmitting.

4.4 Local Oscillators (04-02450)

Two synthesized oscillators are used to drive the first and second mixers. The first oscillator operates between 45.250MHz and 75MHz in 2kHz steps to convert the 250kHz to 30MHz received signal to 45MHz for the first IF. The second oscillator operates between 43.352 and 43.350MHz in 10Hz steps to convert the 45MHz first IF to the 1650kHz second IF.

Each oscillator consists of a voltage controlled oscillator (VCO), a divider, a phase/frequency detector and loop amplifier/filter together with a reference crystal oscillator and divider.

The division ratios required are provided in serial data form from the microprocessor from data stored in the memory. The reference frequency crystal (6.6MHz) is held at a constant temperature by a power PTC thermistor and is divided by 4 to provide the 1650kHz drive to the modulator/demodulator in USB operation. For LSB operation, a separate 1647kHz crystal oscillator is required.

4.4.1 Voltage Controlled Oscillators (VCO)

As VCO1 and VCO2 are virtually identical, only VCO1 will be described in detail:

- FET V2 operates as a Hartley oscillator tuned by varicaps D17 to D20. The output is levelled by schottky diode D21 which generates a negative bias voltage for V2 gate.
- Unity gain feedback amplifier V3/V4 provides a buffer between the oscillator and the cascade connected amplifier V5/V6. The amplifier provides the +7dBm drive to the ring diode mixer and also drives the divide by 64/65 prescaler IC6.
- VCO2 differs from VCO1 only in having a single varicap because of the reduced frequency range required.

4.4.2 Phase/Frequency Detectors and Dividers

IC5 generates a DC voltage which controls the varicaps in VCO1 in order to lock the oscillator to its nominated frequency. A 6.6MHz oscillator in IC5 controlled by the crystal Z2, is divided within the IC to give a 2kHz reference for a phase/frequency detector also in the IC. VCO1 output is divided in a prescaler, IC6, and applied to further dividers in IC5, allowing for the VCO frequency to be changed in 2kHz steps. The divided output is compared with the 2kHz reference frequency.

When the phase/frequency difference is considerable, e.g. immediately after a change of channel, the output from PDB (IC5 pin 2) consists of pulses with their mark:space ratio proportional to the difference. These are integrated by R82 and C123 to provide an input to IC2b. The signal is further filtered by R85 and C127, while the output from IC2b is filtered by R90, R91, C131, C132, C133 and C134. At the same time PBA pin 1 gives an analogue output proportional to the phase/frequency difference. This is also applied to the input of IC2b, via R80. The resulting output drives VCO1 in the direction required to obtain the correct frequency, thus providing a coarse control of the frequency.

When the phase/frequency difference becomes small the PDB output goes high impedance and the analogue output from PDA becomes the only input to IC2b. This provides the fine control of the VCO1 output.

IC7 generates the DC voltage required to control the varicaps in VCO2. A similar arrangement of prescaler and internal dividers divides the VCO2 output in the same way as VCO1 was divided in IC5. The result is compared with a reference frequency within IC7. The 6.6MHz crystal oscillator output from IC5 is applied in IC7 to a divider which can be programmed to provide reference frequencies between 1.1 and 2kHz. This allows VCO2 frequency to be changed in 10Hz steps.

Coarse control of VCO2 is provided by the Freq output (pin 6) from IC7. This consists of low pulses if the VCO frequency is too high, and high pulses if it is too low. These are integrated in C147 to provide the correcting voltage to VCO2. Fine control is provided by the Phase output (pin 17).

4.4.3 Lock Signals

Both phase/frequency detectors give an output which is low while the VCO and reference frequencies are locked, and high when they are unlocked. The LD output from IC5 pin 3 is applied to the base of V28 and the Charge output from IC7 pin 4 is applied to V29. Thus the corresponding transistor is switched on to light the LED indicator (H1 or H2) in its collector circuit if either loop loses lock. The collector circuits are ORed by D45 and D46 so that if either collector is low, i.e. one loop has lost lock, an Unlock output is passed to the Microprocessor Controller PCB.

4.4.4 Loading Frequency Data to Synthesizers

Data containing the required division factors for both synthesizers is applied from the Microprocessor Controller PCB over the Data line. The serial data is clocked into IC7 under the control of the signal on the clock line. The first twenty-eight bits are clocked through IC7 and into IC5, via SR Out (pin 14) of IC7. When the twenty-eight bits have been clocked they are loaded in IC5 by the Enable 1 pulse from the Microprocessor Controller PCB. Similarly the next thirty-two bits are loaded into IC7 by the Enable 2 pulse.

4.4.5 1650/1647kHz Local Oscillators

When receiving (or transmitting) a USB signal, a 1650kHz local oscillator is required. This is obtained by dividing the buffered oscillator output of IC7 (6.6MHz) by 4 in IC9.

When receiving (or transmitting) an LSB signal, a 1647kHz local oscillator is required. This is obtained from IC10c and crystal Z3. A high on J3 pin 11 enables IC9 and disables IC10c giving 1650kHz (USB). A low on J3 pin 11 gives 1647kHz.

A tune output is provided from IC10a to the gate of source follower V16 and V17 when the tune line J3 pin 12 is low. The DC component of the tune output holds V26 conducting which switches V23 to open circuit, disconnecting the crystal filter from V16 and V17.

In the 8528S with compatible AM fitted, resistor R76 is removed, preventing V23 from switching off. This is necessary to permit the carrier to be re-inserted for AM transmission. Because of excessive loading of SSB filter Z1 at 1647kHz, the 1650kHz LO is automatically selected in the tune mode when LSB is selected.

4.4.6 Clarifier

Operation of the clarifier control varies the frequency of VCO2 in 10Hz steps. This is achieved by varying both the VCO and reference frequency dividers according to a 'look-up' table in the transceiver's operating system. Thus the phase comparison frequency is not constant but varies from 1.1 to 2.0kHz.

The range of the clarifier differs between land and marine transceivers:

- Land—The limits of the clarifier are 0.001% (± 10 ppm) of carrier frequency. Consequently the number of steps are also a function of the carrier frequency. At low frequencies dummy steps are inserted to increase the time the clarifier takes to go from end to end of its range.
- Marine—The limits of the clarifier are ± 180 Hz at all frequencies, i.e. ± 18 steps.

An audible indication is given when the clarifier reaches its upper or lower limit. The clarifier automatically resets to mid frequency when the channel is changed.

4.5 Microprocessor Controller PCB (04-02451 and 04-03031)

Circuits on the Microprocessor Controller PCB govern the functions of the transceiver including the operator controls and displays. The microcontroller on the board accepts inputs from within the transceiver and from the operator's controls. Under control of the program in the EPROM, it outputs the data necessary to achieve the appropriate response to input signals.

The microcontroller is connected with other devices on the board by three buses: a conventional microcontroller bus (8-bit data, 16 bit address) and two 'Inter-Integrated Circuit' (I²C) buses.

Note that during the manufacturing period of the 8528 series transceiver the microprocessor controller 04-02451 was replaced with that shown against 04-03031.

For reference, both sets of drawings have been included in this manual. The following description relates to either microprocessor controller.

4.5.1 Microcontroller Bus

The microcontroller (IC11) is an 80C31 which is a member of the Intel 8051 8-bit microcontroller family. It has 128 bytes of internal RAM, no internal program memory, two counter/timers, two external interrupt sources and an internal clock oscillator.

The microcontroller operates in a conventional 8-bit data, 16-bit address configuration. To minimise the pin count, the low-order address bits are multiplexed with the data on pins 32 to 39 onto a common 8-bit bus. IC13 is used to latch the low order address bits to facilitate access to the external non-multiplexed devices. The address latch enable (ALE) signal (IC11 pin 30) indicates to the latch when the address is present on the bus. The high order address bits are provided directly on pins 21 to 28 of IC11.

The following external devices are connected to the bus:

- IC14—an EPROM containing radio control software and customer channel information. The microcontroller selects the EPROM via the program store enable (SE) signal (pin 29).
- IC10—a RAM device supplementing the microcontroller's internal RAM. It is selected via the Read or Write signals (IC11 pins 16 and 17) in conjunction with address line 15 (IC11 pin 28).
- IC12—a triple tone generator used to generate all audio tones required in the transceiver, e.g. emergency call tones, error beeps, etc. It is selected via the Read and Write signals in the same way as IC10 but in conjunction with address line 14 (IC11 pin 27).

Three audio tone outputs are generated within IC12 by dividing the clock inputs on pins 18, 15 and 9 by factors programmed into its data input. The clock input signal is derived from the microcontroller's ALE output. During those cycles when the microcontroller does not generate the ALE, the Read or

Write signals are inserted via D3 and D4 to maintain a steady square wave signal.

4.5.2 Internal I²C Bus

The internal I²C bus consists of four lines: data, clock, interrupt and data-line enable. The data and clock lines operate as an I²C bus; the data line carries data and address bits serially, with their transfer being synchronised by transitions on the clock line.

Data, clock and interrupt lines connect the microcontroller with 8-bit I/O IC's, IC3 and IC4. Each 8 bit I/O IC converts parallel data on its eight ports to serial data for application to the bus and conversely, converts serial data from the bus to parallel data on its ports. Each IC has a separate address set by the connections to its address pins (1, 2 and 3). When a data transfer is required, the microcontroller first outputs on the data line the address bits of the required IC and follows this with a Read/Write command. Data is then read from, or written to, the selected 8-bit IC.

When an input to any of the ports changes, the IC sends an interrupt to the microcontroller. As all the interrupts are connected to a single input, the microcontroller must interrogate each IC in turn until the changed data is read. When this is done, the IC removes the interrupt and the microcontroller can resume its other operations.

Part of IC3 is used for connection to selective call options. The remainder of IC3 and all of IC4 carry data to and from various functions within the transceiver.

The clock and data lines of the internal bus also connect the microcontroller with IC5 and IC15 which operate as I²C bus receivers. Under control of the data, each IC accepts serial bits from the bus. A set of bits consists of two address bits and sixteen data bits. On completion of the transfer of a set, the IC to which the set is addressed latches the data bits as 16-bit parallel data on its outputs. These two IC's provide 32 open drain outputs to various circuits throughout the transceiver.

The microcontroller is connected via the data and clock lines to the non-volatile memory, IC6. This stores the channel selection, volume control, clarifier and scan channel settings. When power is switched off, the data is retained in the memory by battery G1. Drain on the battery is very low, therefore the battery life is limited mainly by its shelf life i.e. approximately 10 years. A discharged battery will cause the channel, volume, clarifier and scan channel settings to require resetting each time the transceiver is switched on, but will allow normal operation of all other facilities.

Also connected to the microcontroller via the bus are two EEPROMs, IC16 and IC17. These provide the non-volatile memory for assemblies 04-02451 to store data entered on the front panel pads. For the 04-03031 version of assemblies, IC16 only is shown being of a different component type to the earlier design.

The clock and data lines are also connected to the synthesizer circuits on the RF, Mixer and Dual Synthesizer PCB via J4. Data for setting the two synthesizer frequencies is sent over the data lines and on completion of the transfer, the synthesizer latch line is pulsed.

The clock and data lines are also taken to connector P1 for application to I/O ports in the Selective Calling PCB when this is fitted. Provision is made for all four lines of the bus to be connected via P3 to further I/O IC's if required.

4.5.3 External Bus

A second four-line bus is provided for connection to 8-bit I/O IC's and 16-bit open-drain output IC's on the Display PCB of the front panel and Extended Control Head. All four lines are buffered in IC1 to allow for the longer lines to the Extended Control Head and to protect the microcontroller. Since the buffers can carry data in only one direction, data read from the control panels is buffered in IC1 and returned to a separate input of the microcontroller.

To allow control of the transceiver from both the front panel and the extended control head 8530/1, the 8-bit I/O ports at these locations must have different addresses. This is arranged by a link on each Display PCB which is set for extended (E) or direct (D) control, thus allowing boards of the same design to be used in both locations.

The interrupt line from the Display PCB is ORed with the internal bus interrupt by diode D5 and is also taken via two buffers in IC1 to a separate input of the microcontroller. By this means, the microcontroller can detect whether an interrupt has come from the internal or external bus.

4.5.4 Reset and Watchdog Circuit

The microcontroller is reset by a +5V level on pin 9. This may be applied in three ways: by applying power to the unit, by the low voltage detection circuit or by the watchdog circuit.

When power is switched on, the reset input is held high, thus resetting the microcontroller ready for initial operation.

If the supply voltage (A rail) falls below 8 volts, IC7 output goes low. This switches on V3 which holds the microcontroller in the reset condition until the supply voltage is restored.

Schmitt Trigger IC8a, together with R9 and C4, form an oscillator with a period of approximately 600ms. However during normal operation, the microcontroller outputs a positive pulse from pin 14 at regular intervals of less than 600ms. Each pulse switches on V1 which discharges C4 thus preventing the oscillator from starting. Should the microcontroller operation fail, or be affected by abnormal inputs, the pulses cease thus allowing the oscillator to start. Each negative excursion of the oscillator output will switch on V3, resetting the microcontroller. The reset will therefore be applied at regular intervals until normal operation is resumed.

4.5.5 RS-232 Port (ALE Option Only)

On 04-03031 there is shown an RS-232 I/O port. V5 is used for the O/P driver and level translator. V6 is used for input level translation.

4.6 Motherboard and Chassis (04-02453)

The Motherboard interconnects circuit boards which are mounted directly on it and provides connections to other assemblies mounted on the chassis. It also provides connections which link these assemblies to external connectors. In addition the board carries components associated with these interconnections and with the power supplies and their switching.

4.6.1 Power Supplies

The Motherboard contains relays with their switching transistors associated with the power supplies as described in Section 4.1.

The board also contains two voltage regulators, IC1 and IC2. These provide stabilised DC supplies of 10V and 5V respectively from the A battery supply. The 10V and 5V supplies are used throughout the transceiver.

4.6.2 Antenna Control Facility

The Antenna control socket J201 on the rear panel of the transceiver provides an interface for various antenna tuning systems. The socket is connected to P201 on the Motherboard. Interconnections within the Motherboard provide access to the 12V supply, 4-bit binary-coded data indicating the channel selected, and various other outputs for use by automatic tuning systems. On entering the board the lines are filtered to prevent RF picked up on the external cable, from interfering with the operation of the transceiver. The table in Section 1.2.4 shows the pin connections and the signal level of each function.

4.6.3 Extended or Remote Control—Option R

The Remote Control plug (P502) on the rear panel of the transceiver provides an interface for extended or remote control equipment. When fitted the plug is connected to the Remote Control and Filter PCB mounted on the Motherboard. Transceivers manufactured for extended or remote control include these components. Transceivers with front panel controls can have them fitted as Option R.

The extended or remote control lines carry the services shown on the circuit diagram. Components on the Remote Control and Filter PCB prevent RF picked up on the external cable, from interfering with the operation of the transceiver.

The table in Section 1.2.4 shows the pin connections and levels of each function.

4.6.4 External Microphone Audio Clamp

The audio input from the Remote Control connector at pin 11 P502 (Option R) is connected, via C102, R103, R101 and C101 to the Aux Compressor input of the Audio and IF 1650kHz PCB. FET V101 is normally biased on via R104 and R105, thus clamping the microphone input to ground. Operation of the remote PTT switch grounds the junction of R104 and R105 removing the bias from V101. This allows the microphone input to be applied to the compressor input.

4.6.5 Additional Audio Facilities—Option RC

Two summing amplifiers, IC401a and IC401b, can be fitted to provide for special applications. IC401b can accept two inputs from the Audio and IF 1650kHz PCB. Inputs are selected, according to the application, by the inclusion or omission of R401 and C401 or R402 and C402. R19 is omitted when the option is fitted and the amplifier output is connected to the Remote Control connector Option R.

Similarly, by the inclusion or omission of input resistor-capacitor combinations, IC401a can accept up to three inputs from various sources. Its output is connected to the pre-volume control input of the IF and Audio PCB.

4.6.6 Headphone Output—Option PH

A 6.4mm switched jack socket can be fitted to the transceiver front panel and connected to the loudspeaker circuit to provide for connection of headphones. The headphone signal is attenuated by a 330 Ω resistor in the line.

4.6.7 CW facility—Option M

A 3.2mm jack socket can be fitted to the transceiver rear panel for connecting a morse key. When the key is operated, a ground is applied via the jack socket to the Microprocessor Controller PCB (P2 pin 3). The microprocessor detects the key function via the I/O port of IC3 and generates the required PTT and audio tone for transmission.

4.6.8 External Selective Call or RTTY—Option PS

Connector J301 on the rear panel of the transceiver provides an interface for selective calling or radio teletype equipment. Operation of the external equipment via this interface is described in Section 4.11.

4.6.9 AGC Dump Circuit

The synthesizer latch from the Microcontroller PCB pin 1 P10 is used to turn on V4 thus grounding the AGC line on the Audio and IF 1650kHz PCB via R23. This discharges the reservoir capacitor in the AGC circuit so that the receiver has maximum gain immediately after a frequency change. This is particularly important when in the scan mode.

4.7 8525B Front Panels and Control Head (04-02579)

The front panels of 8525B series transceivers and extended control heads are similar. Overlays on these panels contain sealed tactile membrane switches. A 2-digit numeric display and LED's on a board behind the panel show through the appropriate part of the overlay when lit. Circuits on a further board behind the panel interface with the microprocessor in the transceiver to drive the displays and indicators and decode the operations of the front panel switches. In the extended control head, circuits on the Microphone Amplifier PCB compensate for the long lines which connect the head with the transceiver.

4.7.1 Display PCB

The Display PCB (08-03944) for the transceiver and the Display PCB (08-03945) for the extended control head differ in size and layout to fit their individual panels. They are, however, electrically identical.

Common connections of the numeric displays and the LED indicators (except the Tx indicator) are taken to a positive supply controlled by IC1. Indicators and segments of the displays are lit by grounding the appropriate connection via IC2 and IC3.

The conduction of phototransistor V1 increases in proportion to the intensity of the light falling upon it. Increasing conduction of V1 reduces that of V2 and V3 thus raising the reference voltage to IC1. Consequently, increasing ambient light raises the output voltage of IC1 thus increasing the display and indicator brightness. The circuit sensitivity is adjusted by R1.

The Tx indicator LED is lit by grounding its cathode via a transistor on the PA and Filter PCB.

Two 16-output open drain drivers, IC2 and IC3 ground individual lines in response to data received on the I²C bus.

A remote 8-bit I/O port, IC4, accepts inputs from switches on the front panel, and under control of the microprocessor, converts them to a suitable format and applies them to the I²C bus.

4.7.2 Switch Matrix

The switches on the panel overlay (substrate) form a 4 x 4 matrix. The row and column connections are taken to the Display PCB. (A table listing the switch functions and corresponding connections is given in Section 6.2.3.) The row connections are polled by the microprocessor, via IC2 by taking them to 0V one at a time. A switch operation is detected by the corresponding column connection to IC4 going to 0V. Data indicating the switch closure is encoded and returned, via the I²C bus, to the microprocessor.

4.7.3 Digiswitches (8525B)

Transceivers and control heads fitted with selective call mesh (SDEM) have thumbwheel digiswitches on their front panels. The BCD outputs of these are applied to the Display PCB. Individual switches are polled so that switch settings are detected and returned to the microprocessor in a similar way to the matrix switches.

4.7.4 Microphone Amplifier and Interface (04-02096)

To compensate for the long lines connecting the Control Head to the transceiver, a Microphone Amplifier and Interface (08-03039), interfaces the Display PCB with the lines to the transceiver. On entering the board each line is filtered to prevent interference picked up on the lines from affecting the operation of the head.

The board contains buffers for the Data, Clock and Enable lines of the data bus. A 3-terminal regulator, IC1, on the A rail provides the 5V supply for use by these buffers and the Display PCB.

An amplifier formed by IC3 and its associated components amplifies the microphone input to a suitable level for application to the lines. V2 on the input to the amplifier operates as a clamp in the same way as V7 on the Audio and IF 1650kHz PCB. This circuit is powered by a separate 10V supply derived from the A rail by zener diode V1.

4.8 8528 Front Panel and Control Head

The front panels of 8528 series transceivers and extended control heads are identical. Overlays on the panels contain sealed tactile membrane switches. A liquid crystal display (LCD) and light-emitting diode (LED) indicators on a board behind the panel show through the appropriate part of the overlay when activated. Circuits on the board interface with the microprocessor in the transceiver to drive the displays and indicators, and to decode the operations of the front panel switches. In the extended control head, circuits on a further board compensate for the long lines which connect the head with the transceiver.

Surface mounted components are used on the Display PCB, LCD. For removal and replacement of these components it is essential to use tools specifically designed for the purpose. Repairs to the board should not be attempted unless the appropriate tools are available.

4.8.1 Display PCB, LCD (04-02454)

The same Display PCB, LCD (08-03745) is used in the transceiver and the Extended Control Head.

The LCD on the board has twenty digits and two enunciators which allow it to display the channel number and transmit and receive frequencies of the currently selected channel. In addition it can display the identification number of a called or calling selective call station. The LCD is driven by IC4. The display data is applied to the driver via the I²C bus. The drive mode is 1:4 multiplexed with 1/3 bias.

The viewing angle is preset by adjustment of R12. This sets the voltage applied to the non-inverting input of IC1a while the voltage at the junction of R10 and D1 is applied to the inverting input. The output of IC1a is proportional to the difference between the two voltages. The temperature coefficient of D1 applies temperature compensation tending to keep the set viewing angle constant over a wide range of temperatures.

R12 is normally set during manufacture for viewing at right angles to the face of the panel. It can be adjusted for viewing angles above or below if required.

Six incandescent lamps, H1 to H6, are mounted behind the LCD to provide back-lighting so that the display can be read in low ambient light. V1 is mounted in a position which allows ambient light to fall on the transistor. Conduction of the transistor increases with the light, i.e. the collector voltage, applied to the comparator IC1b, decreases. IC1b compares this voltage with the fixed voltage at the junction of R3 and R4. In low ambient light, V1 collector voltage is higher than the reference voltage, therefore IC1b output is high. This turns on V2 to light the lamps. If the ambient light increases to the point where the collector voltage of V1 no longer exceeds the reference, the output of IC1b goes low, switching off V2 to extinguish the lamps. The threshold level can be adjusted by R1.

Completion of Link D connects R30 and R31 in parallel with V2. This provides an alternative path for the lamp current, therefore the LCD back-lighting is only reduced to approximately half brightness in high ambient light.

Common connections of the LED indicators H8 to H13 are taken to a positive supply regulated by IC2. The indicators are lit by grounding the appropriate connection via the 16-output driver IC3.

The Tx indicator LED is lit by grounding its cathode via a transistor on the PA and Filter PCB.

4.8.2 Indicator and Display Dimming

The current sinking provided in IC3 for the indicator LEDs H8 to H13, can be varied by operation of the Recall pad on the front panel. Any indicators lit will be at full brightness when the transceiver is first switched on. Pressing the Recall pad twice within one second reduces the current sinking thus reducing the brightness of the indicators. Pressing the pad twice again restores the original brightness.

The dimming operation is also applied to the LCD back-lighting via IC3 pin 4. Normally high impedance (tristate), this output goes low in the dimmed condition. This is applied to the base of V2 to override the input from the comparator IC1b. Thus if the LCD back-lighting H1 to H6 is lit, it will be extinguished (or reduced to half brightness) when the indicators are dimmed.

4.8.3 Links

A moveable jumper link closes either Link E for extended control, or Link F for front panel control. Closing the appropriate link modifies the address of the I/O port IC5 so that the microprocessor can recognise the type of control in use.

Link 1 is used in programming the transceiver options (refer Operator's Handbook) and link 2 is for possible future use.

Link D is used in the display dimming facility (4.8.1).

4.8.4 Switch Matrix

Switches on the panel overlay (substrate) form a 4 x 6 matrix. The row and column connections are taken to the Display PCB. (A table listing the switch functions and the corresponding connections is given in Section 6.2.3). In the Display PCB the row connections are polled by the microprocessor, via IC3, by taking them to 0V one at a time. (Three of the four lines are taken to 0V via open collector drivers V4, V5 and V6). A switch operation is detected by the corresponding column connection to the 8-bit I/O port IC5 going to 0V. Data indicating the switch closure is encoded and returned, via the bus, to the microprocessor.

4.8.5 Microphone Amplifier and Interface (04-02096)

The board used in the extended control head to compensate for the long lines connecting the head to the transceiver is the same as the one used for the same purpose in the 8525B series. (Refer to Para 4.7.4).

4.8.6 8532 Display Head

The Type 8532 Extended Control Head has a smaller frontal area and depth (180mm w x 62mm h x 45mm d) than the Type 8531, making it more suitable for mounting in confined spaces. It has all the features of the 8531 except the loud speaker is external and the control panel is back illuminated for use at night.

Overlays on the front panel of the control head contain sealed tactile membrane switches. A liquid crystal display (LCD) and light emitting diode (LED) indicators on a board behind the panel show through the appropriate part of the overlay when activated. Circuits on the board interface with the microprocessor in the transceiver to drive the displays and indicators, and to decode the operations of the front panel switches.

Surface mounted components are used in the display PCB. For removal and replacement of these components it is essential to use tools specifically designed for the purpose. Repairs to the board should not be attempted unless the appropriate tools are available.

A single PCB, Display PCB (Assembly 08-04666), is used in the Extended Control Head (Refer to circuit Diagram 04-02875).

The LCD, H14, has twenty digits and two enunciators which allow it to display the channel number and the transmit and receive frequencies of the currently selected channel. In addition it can display the identification number of a called or calling selective call station. The LCD is driven by IC5. The display data is applied to the driver via an I²C bus. The drive mode is 1:4 multiplexed with 1/3 bias. The driver is powered by a separate supply derived from the A rail by diode D7 and zener diode V7.

The viewing angle is preset by the adjustment of R34. This sets the voltage applied to the non-inverting input of IC4a, while the voltage at the junction of R32 and D6 is applied to the inverting input. The output of IC4a is proportional to the difference between the two voltages. The temperature coefficient of D6 applies temperature compensation tending to keep the set viewing angle constant over a wide range of temperatures.

R34 is normally set during manufacture for viewing at right angles to the face of the panel. It can be adjusted for viewing angles above or below if required through the hole in the bottom of the case.

Nine incandescent lamps, H1 to H6 and H15 to H17 are mounted on the board. Six are behind the LCD and the remaining three in various areas of the board. These provide back lighting so that the LCD and the panel annotations can be read in low ambient light.

Common connections of the LED indicators H8 to H13 are taken to a positive supply derived from the A rail and regulated by IC1. The indicators are lit by grounding the appropriate connection via the 16-output driver IC2.

The Tx indicator LED, H7, is lit by grounding its cathode via a transistor on the PA and Filter PCB.

The current sinking provided by IC2 for the indicator LEDs H8 to H13 on the front panel can be varied by the operation of the **Recall** pad on the front panel. Any indicators lit will be at full brightness when the transceiver is first switched on. Pressing the Recall pad twice within one second reduces the current sinking thus reducing the brightness of the indicators. Pressing the pad twice again restores the original brightness.

The dimming operation is also applied to the LCD back lighting via IC2 pin 4. Normally high impedance (tristate), this output goes low in the dimmed condition. This is applied to the base of V1 to override the hold-on voltage applied via R1. With the transistor switched off the current for H1 to H6 is drawn through R3 and R4 thus reducing the brightness of the LCD back lighting. The panel back lighting is not controlled and remains at full brightness at all times.

A moveable jumper link closes either Link E for normal extended control, or Link F for special applications front panel control. Closing the appropriate link modifies the address of the I/O port, IC3, so that the microprocessor can recognise the type of control in use.

Link 1 is used in programming the transceiver options (Refer to the Operator's Handbook). Link 2 is for possible future use.

Switches on the panel overlay (substrate) form a 4 x 6 matrix. The row and column connections are taken to the Display PCB. (A table listing the switch functions and the corresponding connections is given in Section 6.2.3.) In the Display PCB the row connections are polled by the microprocessor, via IC2, taking them to 0V one at a time. (Three of the four lines are taken to 0V via open collector drivers V2, V3 and V4.) A switch operation is detected by the corresponding column connection to the 8-bit I/O port, IC3, going to 0V. Data indicating the switch closure is encoded and returned, via the bus, to the microprocessor.

To compensate for the long lines connecting the Control Head to the transceiver, on entering the board each line is filtered to prevent interference picked up on the lines from affecting the operation of the head. The Clock line is also buffered by a small amplifier formed by V8 and V9.

The A rail from the transceiver is used by various circuits on the board and is also applied to a regulator, IC6, to provide the +5V supply for other circuits within the board.

An amplifier formed by IC4b and its associated components amplifies the microphone input to a suitable level for application to the lines. V5 on the input to the amplifier operates as a clamp in the same way as V7 on the Audio and IF 1650kHz PCB. This circuit is powered by a separate supply derived from the A rail by zener diode V6.

4.9 PA and Filters (04-02452)

4.9.1 Introduction

8528S Series transceivers may be fitted with a PA and Filter PCB, forming an internal PA stage, or with a PA Exciter Interface PCB for use with an external PA unit. Software appropriate to the board fitted is installed in the controlling EPROM on the Microprocessor Control PCB. Transceivers fitted for use with an external PA assembly are identified by a letter H suffixed to their type numbers on the rear panel. The board fitted for the internal PA version is described in this section. The PCB fitted for the other version is described in Section 4.10.

4.9.2 PTT Control

The driver and output stages are permanently connected to the supply voltage when the Power On relay K7 is energised. Power to the rest of the PA and the bias for the driver and output stages is switched by V14 when the PTT input (D rail, P1 pin 2) goes high causing pin 10 of IC1 to sink base current from V14 through the antenna change-over relay K6 coil. In transmit, the input stage V7 and V9 becomes active when its emitter circuit is connected to ground on the C rail through D12 on the RF Mixer and Dual Synthesizer PCB (04-02450).

4.9.3 Gain Control Stage

The RF input to the PA is terminated in R21 and drives the common base long tailed pair V7 and V9 through R29 and R30 in parallel for signal currents.

The input voltage is also buffered by V8 and additional input current fed to V7 and V9 through L17, C66 and R32 to compensate for PA high frequency gain roll-off.

The gain of V9 is controlled by the ratio of emitter DC currents in V7 and V9. The RF input current is split between the emitters of V7 and V9 in inverse proportion to their input impedance. The gain of V9 is therefore reduced when the ALC increases the current in V7.

4.9.4 Pre-Driver Stages

The output current of V9 drives the collector-base feedback stage V10 which is direct coupled to the transformer feedback stage V12. High frequency peaking is provided by C72. D11 and D12 provide temperature compensation for V10 and V12.

4.9.5 Driver Stage

The driver stage V16 and V17 is voltage driven from the secondary of T2 and with emitter resistors R52 to R55 provides a current drive to the output stage. L20, C78 and R56 provide damping for a harmonic resonance in T3.

The bias for V16 and V17 is provided by the current of the pre-driver stages passing through the diode-connected transistor V13. The bias may be increased by R46, the current through R46 causing a voltage drop across R47 in addition to the base-emitter voltage of V13. The current in V16 and V17 may be measured at the link in the DC feed to T3.

4.9.6 Output Stage and Bias Regulator

The output stage V18 and V19 is current fed from the secondary of T3 with low frequency current feedback through R58 and R59 from a winding on the output transformer T4. C93, C94 with C116 and C81 with C82 provide frequency compensation for T3 and T4 respectively.

The balanced output auto transformer also contains a balun winding so that one output can be AC coupled to ground and the other output capacitively coupled to the load.

The bias regulator (V11 and V15) provides a constant voltage to the bases of V18 and V19. V11 and V15 form a feedback voltage regulator, the output voltage being the base-emitter voltage of V11. R76 and V23 cause the bias to increase at low supply voltage (10V approx) to reduce intermodulation distortion.

V11 is mounted on the PA heatsink and provides temperature compensation based on heatsink temperature.

When low power is selected (8528S only), V21 is turned on by V20 collector going high. This increases the bias voltage via R71 and therefore the bias current in V16 and V17. This is required to improve the intermodulation distortion at low power.

4.9.7 Output Filters and Control

The output of the PA is passed through one of six low-pass filters to remove harmonics generated in the PA. These filters are relay selected (K1 to K5 and K8) by the band lines generated by the microprocessor controller and buffered by IC1.

4.9.8 ALC Control

ALC control is provided from the following sources:

- Forward power
- Reflected power
- Battery voltage
- Low Power control (8528S only)
- Heatsink over-temperature
- Output stage collector swing.

The ALC control inputs are applied to IC2a which provides a fast attack, slow decay control voltage to the base of V7. In the absence of any ALC input, the negative input of IC2a is held at 3.9V by voltage divider R16, R17 and R19 and the voltage on C59 and V7 base is held at a similar level. V7 is cut off and V9 then operates at maximum gain.

The R16, R17 and R19 voltage divider chain is used to control ALC action for heatsink temperature. When the heatsink temperature exceeds 80°C, PTC resistor R16 rapidly increases in value, reducing the ALC threshold level and reducing the power output such that the heatsink does not rise above 90°C.

The output voltage from the RF bridge T1, L1, R2, R3, C1 and C2 is rectified by D1 as forward power and by D2 as reflected power. The forward power output is divided by R9, R10 and R11 and ORed by D8 with the output of the reflected power detector into the positive input of the ALC level comparator IC2a. The power output is set by R10.

The output voltage of the forward power detector is averaged by R68, C92 and ORed into the ALC comparator. The value of R68 is chosen so that a average forward power of 60W will provide ALC control.

When the DC supply drops below 12.5V, V5 starts to conduct, increasing the voltage across R11. This effectively raises the forward power detector level, resulting in increased ALC, reducing the output power.

A low on the LO PWR input (P3 pins 1 and 2) will cause V20 to conduct also raising the current in R11 and reducing the power output.

The peak positive swings of the PA output transistors V18 and V19 are rectified by D13 and D14, divided by R61 and R62 and buffered by V22 before being ORed into the ALC comparator. Thus excessive swings of the PA collector voltage reduces the output power to prevent damage to the PA transistors. The output from V22 is also applied to one input of IC2b where it is compared with the forward power to the antenna. If the forward power is very low (or absent) indicating a fault in the antenna circuit, the output power is reduced to prevent damage to the PA transistors.

4.9.9 Transmit Indicator

The forward power voltage developed by D1 is divided and applied to V4 base producing a current in V4 proportional to power output to illuminate the Tx LED indicator.

4.10 PA Exciter Interface (04-02434)

4.10.1 Introduction

8525B and 8528 Series transceivers may be fitted with a PA and Filter PCB forming an internal PA stage, or with a PA Exciter Interface PCB for use with an external PA unit. Software appropriate to the board fitted is installed in the controlling EPROM on the Microprocessor Controller PCB.

Transceivers fitted for use with an external PA unit are identified by a letter H suffixed to their type numbers on the rear panel. The PA Exciter Interface is designed for use with Codan Type 4402 or 4404 power amplifiers and is described in this section. The PCB fitted for the internal PA is described in Section 4.9.

4.10.2 Control Lines

Control lines from the transceiver are taken through the board for connection to the external PA unit. The lines are filtered on the board to prevent RF, picked up on the cable to the PA Unit, from interfering with the operation of the transceiver.

4.10.3 Power On/Off

The DC supply for the transceiver is connected to the external PA unit. Operation of the On/Off switch pad on the transceiver front panel grounds the Power On line to the PA unit. This energises a relay in the PA unit, supplying 12V to the transceiver. A fuse on the PCB protects the supply before it is taken to the remainder of the transceiver to form the A rail. The latching relay on the Motherboard operates in a similar manner as described in section 4.1.4.

4.10.4 PTT Circuit

The D rail (10V in transmit) switches on V4 in the transmit mode to ground the PTT line to the external PA unit.

4.10.5 Transmit Amplifier

The RF input to the board is applied to a grounded base amplifier V1. The DC path for the emitter of V1 is completed via D12 and the C line (0V) on the RF Mixer and Dual Synthesizer PCB. R6 in the collector circuit of this transistor provides a range of approximately 6dB of gain control. The signal from the collector of V1 is passed to an emitter follower V2, the output of which drives V3. V3 with T1 forms a fixed gain feedback amplifier. The secondary of T1 is adjusted for 2.0V pp output by preset R6 to drive the 4402 or 4404 PA units.

4.10.6 Receive Circuit

Received RF from the PA unit is applied to the Rx I/P (P3 pins 9 and 10). The signal passes to the receiver circuits via a broadcast band high-pass filter formed by L1 to L3 and C1 to C7. Diodes D1 and D2 limit the output swing of the signal. In the transmit mode the D rail forward biases D2, clamping the receiver input to ground.

4.10.7 Antenna Control

Lines to control an external antenna or antenna control unit are also taken through the board for connection to the Antenna Control connector at the rear of the transceiver. The Scan, Tune and Tuned In control signals are also taken to and from the PA unit.

4.10.8 PA Unit

Details of the Codan 4402 and 4404 PA Units are given a separate service manual Code 2037.

4.11 Selective Calling (04-02250)

Selective calling facilities may be either internal to the 8525B or 8528, or by external control using option PS. It should be noted that option PS **cannot** be used when internal selective call is fitted.

The following selective call variants are available:

- SE2 4–digit encoder internally preset.
- SDE 4–digit encoder/decoder—separate internal presets for encode and decode.
- SDEM 4–digit encoder/decoder—internally preset for decode, externally set for encode.

Note: When an 8530 control head is used with SDEM, the encode switches only are mounted on the control head while the remainder of the circuit is in the transceiver. SE2 uses assembly 08-03303; SDE and SDEM use assembly 08-03300.

Selective Calls are sent as FSK signals using 1700Hz and 1870Hz at 100 Baud.

4.11.1 Selective Calling

The call is initiated by pressing the Call pad on the front panel. On recognising the request for a call, the microcontroller first checks that the channel selected is one on which selective calls are programmed. If it is, the microcontroller generates the required codes including the Called Address and Self Ident codes set in the transceiver. The settings of each pair of switches are encoded by the corresponding 8-bit I/O port IC4, IC5, IC6 and IC7 and sent to the microcontroller as serial data when the appropriate port is addressed. The Self Ident switches on the PCB are used for all options. When external digiswitches are fitted (SDEM), the microcontroller disregards the settings of any internal Called Address switches duplicated on the panel or control head.

The microcontroller (04-02451) applies the generated code to the tone generator IC12. The resulting FSK tones from IC12 pin 10 are filtered by C20 and R21 and applied via J3 pin 9 to the auxiliary compressor input of the Audio and IF 1650kHz PCB. The FSK tones are also attenuated by R23 and applied as a side tone via J3 pin 10 to the auxiliary LS input of the Audio and IF 1650kHz PCB. At the same time, the microcontroller generates a PTT signal so that the FSK tones are transmitted. On completion of the coded transmission, the PTT signal is removed and the transceiver returns to the receive mode.

Note: If selective and 2-tone calling are required on the same frequency, the frequency must be allocated to two channels; one with selective calling and one with 2-tone calling.

4.11.2 Selective Call Detection (04-02250)

The Selective Call PCB fitted for Options SDE and SDEM includes circuits for the detection of selective calling signals. The received audio is applied via J1 pin 2 to a band-pass filter formed by IC1a, IC1b and their associated components. The filter has a 3dB bandwidth of 400Hz centred on 1775Hz. The filter output passes to the phase locked loop IC2.

The voltage controlled oscillator frequency in IC2 is set by C10, R15 and R16. In the absence of FSK signals, the lock detect output from pin 6 will fluctuate and the resulting charge on C8 will be less than half the supply voltage. This is applied via R11 to the comparator input pin 8, resulting in a low output from pin 7. Some of the output is fed back to the input via R13 to provide hysteresis. The comparator output is taken via D3 to the non-inverting input of IC3b. This results in a low output from IC3b which effectively cuts off V1. When FSK signals are detected the lock detect output goes high. The resulting high comparator output reverse biases D3, enabling IC3b.

When FSK signals are applied, the data appears on the loop phase detector output pin 11. This is applied to the data filter IC3a and associated components. This is a low-pass filter at approximately 80Hz which passes the resulting data to the input of IC3b. The data filter output is also peak rectified by D1, D2, C17 and C18. The voltages on the two capacitors are summed at the inverting input of IC3b to give a reference voltage equal to the mean frequency of the FSK signal. Consequently, IC3b regenerates the data, ignoring any frequency shift in the RF path.

Demodulated FSK signals are applied via P2 pin 6 to the Microprocessor Controller PCB (04-02451) on P1 pin 1. From there they are applied to the microcontroller which decodes the addresses contained in the data. If the selective call is found to be addressed to the transceiver, the microcontroller sends a revertive message to the caller. At the same time the controller gives outputs which activate the necessary audio and visual indications that a selective call has been received.

If the transceiver PTT is not pressed, on completion of the audio alarm period, the microprocessor applies a low on J1 pin 6 (04-02451). This is fed to J1 pin 4 (on 04-02250) which, through V2 and V3, energises relay K1 for 2 minutes, operating an external alarm (if fitted). K1.1 contacts are rated at 50V 1A. Operation of the PTT cancels the alarm.

Refer to section 7.3.15 for setting up instructions.

4.12 Two-Tone Calling System

The two tone calling system consists of the transmission of two simultaneous audio tones. The difference frequency is detected to provide a narrow bandwidth independent of frequency shifts in the RF path.

4.12.1 Two-Tone Calling

The call is initiated by pressing the Call pad on the front panel. On recognising the request for a call, the microcontroller first checks that the channel selected has two-tone calling programmed. If enabled, the microcontroller activates the tone generator IC12 and the required tones are generated, one from pin 10 and one from pin 13. These pass through the filters formed by C18, R21, C14, R14, etc. to be mixed at the junction of R21 and R22. The mixed tones are applied via J3 pin 9 to the auxiliary compressor input of the Audio and IF 1650kHz PCB. The tones are also attenuated by R23 and applied as a side tone to the auxiliary LS input of the Audio and IF 1650kHz PCB. At the same time the microcontroller generates a PTT signal so that the tones are transmitted.

An RFDS emergency call (as determined by the programming) is transmitted for 15 seconds after the Emgcy Call pad has been held for at least 2 seconds. For other calls, the transceiver reverts to the receive mode as soon as the pad is released.

Note: If selective call and 2-tone calls are required on the same frequency, the frequency must be allocated to two channels; one with selective calling and one with 2-tone calling.

4.12.2 Two-Tone Detection

Received audio signals are applied to the Two-tone Decoder PCB (refer to 04-02231) J2 pin 1. IC1b and its associated components form a high-pass filter, while IC1a and its components form a low-pass filter. Together, these form a band-pass filter which accepts frequencies between 850 and 1500Hz, i.e. the band used for 2-tone calling.

The accepted frequencies are applied to an audio compressor circuit formed by IC2a, V1, V2 and their associated components. Transistor V2 conducts during positive half cycles of the output of IC2a to charge capacitor C9 so that the potential on the capacitor is proportional to the amplitude of the audio signals. This potential controls the gate of V1 thus controlling the drain-to-source resistance of the FET and consequently the gain of the circuit. Thus the audio signals at the output of IC2a are maintained at a constant amplitude.

The two-tone audio signal is further filtered by a high pass filter formed by IC2b, IC3a and their associated components. The filter output is applied to a phase splitter V3, so that equal anti-phase waveforms are produced. Each of these is applied to one of the two transistors V4 and V5 which operate as a full-wave rectifier. The output from the emitters of these is a half-wave sinusoidal waveform containing the sum and difference of the two tones. This output is applied to the high-Q low-pass filter formed by IC3b and its associated components removing unwanted frequencies. R25 and R26 set the peak of the response.

The difference frequency is then applied to the input of tone decoder IC5. The internal oscillator of the tone decoder is set to 360Hz or 440Hz by the value of C24, R30 and R31. When the difference frequency matches the setting of the internal oscillator within a narrow bandwidth (approximately $\pm 15\text{Hz}$), pin 8 of the tone decoder goes low. Thus the receipt of any two tones with a difference in frequency corresponding to the frequency to which the tone-decoder is set (normally 360 or 440Hz) causes this output from the Two-tone Decoder PCB.

The output is taken via J3 pin 4 to P2 on the Microprocessor Controller PCB. This activates the tone generator IC12 to generate three short pips to indicate the receipt of a two-tone call.

Refer to section 7.3.16 for setting up instructions.

Note: The S'call mute facility can be used with the two-tone decoder in the same way as it is used with selective calling.

4.13 Option PS—External Signalling Interface

Connector J301 can be fitted to the transceiver rear panel to provide connection for Codan 8422 or 8511 Selective Call Controllers, radio teletype (RTTY) or other signalling equipment. When the option is fitted, J301 is connected to P301 on the Motherboard (refer to 04-02453) and components associated with the interface are installed on the board. J301 pin allocations and signal levels are given in Table 1.2.4.

4.13.1 External Selective Calling

Power is applied to the external unit via J301 pins 8 (A rail) and 1(0V). Audio received on the channel to which the transceiver is tuned is applied via pin 2 to the external unit. Any FSK signals in this audio are demodulated and examined for the selective call code preset into the external unit. While no selective calls are detected, the external unit holds the Quiet Line input to the transceiver (pin 4) Hi (+10V). In converting this 10V to the levels required by the transceiver, V303 inverts the Quiet Line input to hold low the corresponding input to the Microprocessor Controller PCB so that the audio is not reproduced by the loudspeaker.

On receipt of a selective call code addressed to the transceiver, the external unit generates tones forming the revertive message to be sent to the calling station. These are applied to the transceiver via pin 3 while the PTT line (pin 6) is taken low. The PTT is applied to the Microprocessor Control PCB and if other conditions are satisfied this switches the transceiver into the transmit mode so that the tones are transmitted on the channel to which the transceiver is set. At the same time, the Quiet Line input goes low so that audio is reproduced as soon as the transceiver returns to the receive mode and the alarm tones are applied via pin 5 to the auxiliary L/S input so that the alarm sounds.

When a selective call is initiated at the external unit, the appropriate FSK signal is generated. The signal is applied to the transceiver at J301 pin 3 while the PTT line is taken low. Consequently if all conditions at the microprocessor are satisfied the FSK signal is transmitted.

4.13.2 Selective Call Scanning

With Option PS fitted and Codan 8422 or 8511 units connected to J301, the scan facility of the transceiver can be used to scan up to eight channels for selective calls. This mode of operation is initiated by selecting Scan on the transceiver front panel and Mute on the external equipment. Selection of the scan mode is indicated to the external equipment by the Scan output line (pin 7) being taken high via V301 and V302, which convert the levels in the transceiver to the +10V or 0V levels required by the external equipment. The external equipment switches the Quiet Line input high in response. This is inverted by V303 and applied to the Microprocessor Controller PCB. As a result of this the speaker is muted, the S'call Mute indicator is lit and scanning is restricted to the first eight channels of the scan program.

When any selective call is detected, the external equipment takes the PTT line low. This does not cause a PTT function but stops the scan long enough for the whole selective call message to be decoded. If it is found not to be addressed to the transceiver, the PTT line is released and scanning is resumed.

If, however, the selective call is found to be addressed to the transceiver the alarm tones generated by the external unit are connected to pin 5 of J301. The alarm tones are applied to the audio circuits so that they are reproduced by the loudspeaker. They are also applied to the Microprocessor Control PCB (04-02451) where they are integrated by diode D6 and capacitor C23. The voltage on C23 falls rapidly to the low logic level and this is detected by the microprocessor which initiates the transmit mode. The revertive tones are produced by the external equipment and applied to the transceiver. During this period the microprocessor ensures that scanning stops and the Quiet Line input goes high to unmute the receiver. The microprocessor also lights the Called indicator and the decimal point in the channel display on the transceiver front panel.

If the call is answered immediately (by the operator pressing the microphone PTT switch) the alarm tones will cease, the transceiver will leave the scan mode, i.e. it will not scan again until the Scan pad is pressed and the Called indicators will be extinguished.

If, however, the call is not answered within a short time the alarm tones will cease and the audio will be muted again. Scanning will be resumed approximately 2.5 minutes after this but the Called indicator and the decimal point will remain lit until the PTT switch is pressed (refer to Fig 4.1.)

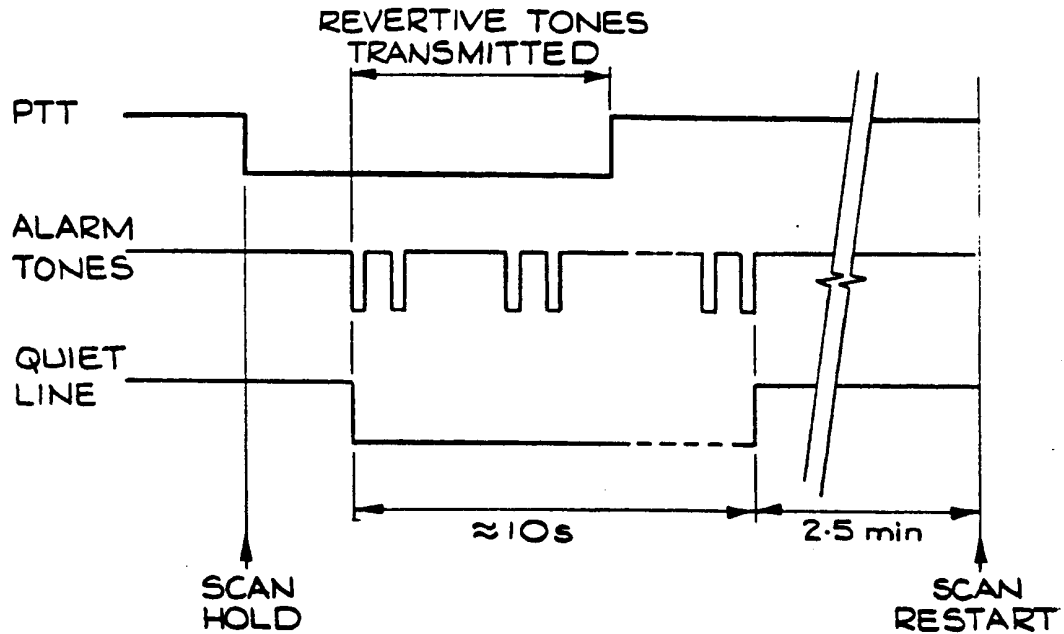


Figure 4.1 Selective Call Scanning

4.13.3 RTTY—ARQ Mode

With Option PS fitted the transceiver can be used for ARQ mode teletype transmission and reception. The teletype interfacing equipment is connected to J301 in the same way as the selective calling equipment. Refer to the table in section 1.2.4 for the pin connections and the levels acceptable for each function. Note that Option PS cannot be fitted if any of the internally fitted selective calling function are fitted.

Note: It is essential to use J301 for the PTT connection in this mode. The switching time of the PTT function at the microphone connector on the front panel is unacceptably long for ARQ operation. (The transmit/receive switching time at J301 is 20ms).

If scanning is used in this mode (depending upon the external equipment used), it may be necessary to enter the same channel into consecutive positions in the scan program in order to dwell on each channel long enough (in the order of 2 seconds) for the detection of RTTY - ARQ mode signals. This will, of course, restrict the number of channels that can be scanned. Scanning must be carried out in the Quiet Line mode, i.e. with +10V applied to the Quiet Line input. The Alarm Tones input must be taken low (0V) by the external equipment to stop the scanning.

4.14 Options

Options may be fitted to the transceivers as described in the sections which follow.

4.14.1 F—Fan Assembly

Option F is a factory-fitted assembly containing an axial flow fan and its control circuit. Mounted over the heatsink the fan enhances the heat dissipation of the transmitter. When the option is fitted, heatsinks are added to the driver and output transformers on the PA and Filter PCB.

The Fan Controller circuit (assembly 08-03334) switches on the fan if a transmission lasts longer than 75 seconds, and keeps the fan switched on even if short breaks (up to 600ms) are made during the transmission.

The circuit is powered from the transceiver A rail (12V) and the positive side of this is taken through the PCB to the fan. Transistor V2 is in the ground return line of the fan. The D rail (10V in transmit) is applied at the PTT input. During reception, the 0V on the PTT input cuts off V1 allowing C3 to charge via R3. The positive voltage applied to the MR input of IC1 holds the timer in the reset condition. In the reset condition the Q output of IC1 is low so that V2 is cut off, breaking the return line of the fan supply.

When the PTT is operated the input goes high which switches on V1. This immediately discharges C3 and the 0V on the MR input allows IC1 to start timing. After 75 seconds the Q output of IC1 goes high to switch on V2 which completes the supply circuit to the fan.

If transmission stops, the PTT input goes low and V1 is switched off. However, C3 must charge via R3 before the MR input to IC1 can go high enough to reset the timer. This takes approximately 600ms and if transmission is resumed in this period, C3 is immediately discharged again and the timer is not affected. Consequently short breaks in transmission, either during the initial timing period or after the fan has been switched on, have no effect on the cooling.

4.14.2 LU—Switched LSB Operation

Individual channels can be programmed to operate on upper and lower sidebands; the choice being made and indicated at the USB/LSB pad on the front panel. For LSB operation, a 1647kHz crystal is fitted in the Z3 location on the RF Mixer and Dual Synthesizer PCB 08-03740. Adjustment is carried out as described in section 7.3.11 of this manual. Selection and operation of the oscillator circuit is described in Section 4.4.5. The required facilities are programmed into the EPROM.

4.14.3 L—Lower Sideband Operation

Individual channels can be programmed to operate on LSB in lieu of the normally programmed USB. The LSB crystal must be fitted as for option LU. The required facilities are programmed into the EPROM.

4.14.4 M—CW Facility

A 3.2mm jack socket can be fitted to the transceiver rear panel and connected to pin 3 of P2 on the Microprocessor Controller PCB (08-02451). This provides the connection for an external morse key.

4.14.5 PH—Headphone Output

A 6.4mm switched jack socket can be fitted to the transceiver front panel and connected to the loudspeaker circuit as shown in 04-02453. This provides the connection for a headset. Insertion of the jack in the socket breaks the loudspeaker circuit, thus muting the loudspeaker. The headset signal is attenuated slightly by a 330 Ω resistor in the line, thus making it unnecessary to adjust the volume when changing to or from headset operation.

4.14.6 R—Extended/Remote Control Interface

A 15-way connector can be fitted on the transceiver rear panel to provide the connections for an extended or remote control head to be used in addition to the controls on the transceiver front panel. The connector is included in the normal build standard of transceivers manufactured specially for remote or extended control only. The circuit is described in Section 4.6.3.

4.14.7 AD—Antenna Driver

Option AD enables Type 8525B/8528 Series Transceivers to be used with Codan Automatic Tuning Whip Antennas Type 8558 while still retaining the capability of using antennas with preset tuning.

The option consists of a single PCB (Antenna Driver PCB Assembly (08-04285)). The PCB plugs into J202 on the Mother Board of the transceiver after disconnecting the ribbon cable previously connected to this plug. The ribbon cable, which carries the antenna control facility to J201 on the rear panel of the transceiver, is then connected to a plug (P1) on the Antenna Driver PCB. Two further connections are made: J2 of the Antenna Driver PCB is connected to J1 of the Microprocessor Board and J3 of the Antenna Driver PCB is connected to P4 on the PA and Filter Board.

(Refer to Circuit Diagram 04-02724)

The inclusion of the option is indicated to the microprocessor in the transceiver when the IO device, IC3, on the board responds to being polled, on the I²C bus to its Clock and Data lines, when the transceiver is switched on.

When the Tune pad on the transceiver control panel is pressed the microprocessor causes some RF, at the required transmission frequency, to be applied to the antenna. At the same time the microprocessor prepares the IO device, IC3, to respond to the VSWR measurement. Voltages proportional to the forward and reflected power at the antenna are applied from the PA and Filter Board to J3 of the Antenna Driver PCB.

The forward power is compared in IC4a with a preset voltage to establish whether the RF is adequate for the VSWR measurement to be made. If the voltage proportional to the forward power exceeds the preset voltage the output of IC4a goes to the low logic level to indicate ADEQUATE RF. The result of the comparison is passed, via IC3, to the microprocessor.

The microprocessor has recorded the last used frequency and is given the new frequency and it uses this information to drive the antenna tuning motor in the appropriate direction to improve the VSWR. It does this by sending data to IC3 to switch on one of the transistors, V4, V6, V8 or V10. These switch on the corresponding Darlington transistors V5, V7, V9 or V11. The antenna motor is a 4-phase, uni-polar stepper motor and is driven in the wave mode (i.e. one phase at a time). +12V is applied to one end of all four windings of the motor and, when switched on, each Darlington transistor grounds the other end of one winding.

The forward and reflected power are compared in IC4b, IC5a and IC5b. One input to each of these comparators is from a potential divider on the forward power voltage, while the other input to each is the reflected power voltage. The potential divider values are such that the output of IC4b will go low when the VSWR is less than 3:1, IC5a will go low when it is less than 2:1 and IC5b will go low when it is less than 1.5:1.

The outputs of the comparators are sent to the microprocessor via IC3 and, as the antenna tuning changes, the microprocessor detects any improvement in the VSWR. As soon as an improvement is detected, provided the RF has been found to be adequate, the microprocessor stops the tuning and a positive voltage is applied to the Load input to the board (J1 pin 7). This switches on V2 so that the Load output (P1 pin 4) goes low.

The Load output is applied to a circuit in the antenna which controls a 2-coil latching type relay (K2 on the Auto Antenna PCB). The low level on the Load input to the antenna causes the load presented by the antenna to be 22 ohms, while a high level on the input causes the load to be 35 ohms. The microprocessor assesses whether the change of load has improved the VSWR.

The microprocessor continues the process of changing the antenna tuning and the load until either the VSWR is found to be less than 1.5:1 or no further improvement can be made. Provided the final VSWR is less than 3:1 a Pass indication is given. If it is greater than 3:1, or the RF is inadequate, a Fail indication is given.

On completion of the tune operation a positive voltage is applied to the Brake input (J1 pin 6). This switches on V1 which bypasses R1 to lower the output of IC1 to approximately 1.3V. This is applied to the antenna motor windings. At the same time V5 is switched on so that a small current (approximately 120mA) is passed through one motor winding. This has a braking effect so that the antenna tuning does not change with vibration.

Power for the comparator circuit is derived from the A rail by IC2. This remains operative on completion of the tune operation so that any change in the VSWR will still be detected. If a transceiver fitted with the option is used with a non-tunable antenna an excessive VSWR will cause an 'Untuned' indication which cannot be corrected. The reflected power voltage, via R10, is, therefore, taken to the disable line (P1 pin 5). When the transceiver is used with a non-tunable antenna, pin 3 of the rear panel D connector (J201) can be linked to pin 14 to disable the comparator so that no 'Untuned' indication is given.

When the transceiver Scan mode is selected, the \overline{SCAN} input (J1 pin 9) is taken low to switch on transistor V3. The collector current of the transistor energises relay K1 in the antenna. This switches into circuit a wide-band amplifier in the antenna which provides good reception over the entire range of the antenna.

To retain the ability to use a transceiver fitted with the option with a pretuned antenna, the lines from the Microprocessor Controller Board carrying the BCD data for presetting the antenna are carried through the option board to the rear panel D connector (J201).



5

Operating Instructions

Refer to the relevant Operator's Instructions booklets.



6

Maintenance

6.1 General

6.1.1 CMOS Devices

A number of Complementary Metal Oxide Semiconductor (CMOS) devices are used in the transceiver. Although protection is built into most of these, their extremely high open-circuit impedance makes them susceptible to damage from static charges. Care must therefore be used when shipping and handling the devices and in servicing equipment in which they are installed. The following precautions should be observed:

- **Packaging**—Replacement CMOS devices are supplied in special conductive packaging. They should be left in this packaging until required for use.
- **Switch off**—Ensure that supplies are switched off before disconnecting or reconnecting any connections between circuit boards and the remainder of the transceiver.
- **Handling**—Handling of circuit boards and particularly touching any conductive parts should be kept to a minimum.
- **Grounding**—Anything connected to or touching the circuit board tracks should be grounded. Observe the following:
 - Test equipment connected to a board should be grounded via its mains lead.
 - Static charges which may build up on the person can be discharged by touching a grounded metal surface with both hands. This should be done before, and at frequent intervals while, working on circuit boards.
 - Wearing a suitably grounded conductive wrist strap will minimise the static build up on the person.

6.1.2 Circuit Boards

When servicing printed circuit boards the following should be observed:

- **Excessive heat**—Excessive heat may lift the track from circuit boards, causing serious damage. Avoid the use of high powered soldering irons: a 60W maximum iron, preferably temperature controlled at approximately 370°C, is sufficient for most tasks. A slightly higher temperature (425°C) iron may be required for heavier components such as PA transistors. Apply the iron only long enough to unsolder an existing joint or to solder a new one.

- **Unsoldering**—When unsoldering use a solder-sucker or Solderwick to remove solder. **DO NOT USE SHARP METAL TOOLS SUCH AS SCREWDRIVERS OR TWIST DRILLS AS THESE WILL DAMAGE THE PRINTED CIRCUIT TRACK.**
- **Component substitution**—Avoid unnecessary component substitution as this may damage the component, the circuit track or adjacent components.
- **Component replacement**—When a component is diagnosed as defective, or the fault cannot be diagnosed in any other way than by substitution, observe the following when installing the replacement:
 - **Axial leads**—Components with axial leads, e.g. resistors and tubular capacitors, can often be replaced without unsoldering the joints on the boards. The defective component can be removed by clipping its leads close to the component leaving the leads soldered to the board. These leads should be straightened so that the leads of the replacement can be wrapped around them and soldered. After soldering the excess lead should be clipped off.
 - **Remove solder**—When a component has been unsoldered from the board ensure the holes are clear of solder before inserting the leads of the replacement. **ON NO ACCOUNT FORCE THE LEADS THROUGH THE HOLES AS THIS WILL DAMAGE THE CIRCUIT TRACK PARTICULARLY WHERE PLATED THROUGH HOLES ARE USED.**
 - **Observe orientation**—When replacing diodes, transistors, electrolytic capacitors or integrated circuits, before removing the defective component, observe any marking indicating polarity or orientation. It is essential that these types of components are installed with the correct connections. If necessary consult the manufacturer's data for indications of the polarity of diodes or capacitors and connectors of transistors.
 - **Heat sinking**—Whenever possible use long-nosed pliers or some other form of heat sinking on the leads of heat sensitive components while soldering them to the board.
 - **Thermal conduction**—When replacing transistors which are mounted on heat sinks ensure good thermal conduction between the heat sink and the replacement by cleaning the mounting surfaces and recoating them with a thermal conduction compound such as Jermyn Thermaflow A30.
- **Track repair**—Broken or burned sections of printed circuit track can be repaired by bridging the damaged section with tinned copper wire. The section where the repair is to be made must be cleaned observing the precautions outlined above before soldering.

- Integrated circuit replacement—In some cases it is possible to desolder and remove components from the board without damage to the component or the board. However, integrated circuits with a large number of connections, mounted on double-sided circuit boards with plated-through holes are almost impossible to remove intact, and the operation is likely to damage the circuit boards. To replace these components their leads must be cut individually until the body of the component can be removed from the board. Individual leads must then be unsoldered and removed. Excess solder must be removed before inserting the replacement component.

6.1.3 Transmitter Precautions

When making measurements of the low level stages of the exciter it is advisable to remove the drive to the PA stages by disconnecting P2 on the PA and filter PCB. The supply voltage is applied to the PA at all times when the transceiver is switched on. Due care should be exercised when connecting probes.

6.1.4 Probe Precautions

The following should be observed when connecting CRO probes to the transceiver:

- When connecting probes to the PA assembly, the earth clip lead should be wound around the body of the probe so that the earth clip just reaches the probe tip. This reduces stray pick-up.
- The earth clip should be connected to the ground plane immediately adjacent to the point of measurement to which the probe tip is connected.
- It is not advisable to connect two probes at the same time, particularly when one is earthed to the PA ground plane and the other is earthed to the chassis, as this may cause earth loop problems.
- Probes should be connected after power has been applied to the transceiver and the test equipment. The earth connection should be made first and disconnected last.

6.1.5 Surface Mounted Components

Surface mounted components are used on some printed circuit boards. For removal and replacement of these components it is essential to use tools specifically designed for the purpose. Repairs to these boards should not be attempted unless the appropriate tools are available.

6.2 Fault Diagnosis

6.2.1 General

The removal and substitution of components may damage the components and/or the printed circuit boards. In some cases it is impossible to remove components without destroying them. It is important therefore to carry out as much fault diagnosis as possible with components in situ. Specific tests are described later in this section. The general points which follow should also be of assistance:

- Spare boards—If spare boards are held in stock, they may be substituted in order to positively localise the fault to one board.
- Transistor tests (static)—Transistor failures are most often due to open-circuit base-emitter or base-collector junctions, or a short circuit between emitter and collector.

These types of faults can often be detected without removing the transistor, using the ohms range of a multimeter. The two junctions should both give the appearance of a diode, i.e. high resistance with the multimeter leads one way round and low resistance when the leads are reversed. (Polarity depends on whether a PNP or NPN transistor is being tested.) Resistance between collector and emitter should be high with the multimeter leads either way round. The circuit diagram should be examined for parallel paths before a transistor failing these tests is removed.

- Transistor tests (dynamic)—Some transistor faults can be diagnosed by measuring voltages within the circuit. One of the most significant voltage measurements is the base-emitter voltage. The polarity of this will depend on the type of the transistor (PNP or NPN). A base emitter voltage between 0.5 and 0.9V should be measured on a forward-biased base-emitter junction.

With its base emitter junction forward biased the transistor should conduct. Some indication of satisfactory operation of the transistor can be obtained by measuring the voltage drop across its collector or emitter resistor and short circuiting its base to the emitter. The short circuit will remove the forward bias cutting off the transistor so that the voltage across the resistor will be considerably reduced.

- Integrated circuits—If there appears to be no output from an integrated circuit, before replacing the device, it should be ascertained whether the fault is due to the IC or its load. As a general rule, if changes in input cause absolutely no changes in the corresponding output the IC should be suspected. If, however, even a very small change in output can be detected the load is more likely to be the cause. Depending upon the circuit, further tests should be made by disconnecting resistors, capacitors, etc to verify this diagnosis before removing the IC.

6.2.2 Voltage Measurement

The circuit diagrams and the relevant circuit notes give voltages at various points under the various conditions to enable the faulty section of the transceiver to be located.

The parameters listed below should always be checked first:

1. Supply voltages on the Motherboard and Chassis:
 - Main B rail regulator (IC1) $10V \pm 0.2V$
 - C rail, B rail voltage in Receive, 0V in Transmit,
 - D rail, 0V in Receive, B rail voltage in Transmit,
 - Main 5V regulator (IC2) $5V \pm 0.4V$.
2. Supply voltages on the RF Mixer and Dual Synthesizer PCB:
 - +5V supply (IC4) $5V \pm 0.4V$
 - +26V supply (TP7) $26V \pm 1V$
 - +9V supply (V1 emitter) $9V \pm 0.25V$
3. Supply voltage on the Microphone Amplifier and Interface PCB in the Control Head: 5V regulator (IC1) $5V \pm 0.4V$.

6.2.3 Front Panel Controls

IN THE TEST WHICH FOLLOWS CARE MUST BE TAKEN WHEN MAKING CONTACT WITH THE CONNECTIONS TO THE SWITCH SUBSTRATE NOT TO SCRATCH THE SILVER PLATING.

Lack of response to controls may be due to malfunction of one or more of the sealed membrane switches. These can be tested by disconnecting the connector from the front panel (or control head) switches at J4 on the Display PCB and testing between pins of the connector as shown in the table below. A meter connected between each pair of pins in turn should indicate open circuit with the corresponding switch not operated and continuity (less than 100Ω) when the switch is pressed.

Front Panel Switch Test (8528)

Connector Pin	8528S	8528
1 - 2	Mute On/Off	Mute On/Off
1 - 4	Scan	Scan
1 - 5	AM Mode	S'call Mute
1 - 7	Tx Power	USB/LSB
1 - 8	Power On/Off	Power On/Off.
1 - 10	Tune	Tune
3 - 2	2182	Display
3 - 7	Enter	Enter
3 - 8	–	Emgcy Call
3 - 10	Recall	Recall
6 - 2	Volume (up)	Volume (up)
6 - 4	Clarifier(up)	Clarifier (up)
6 - 5	Channel (up)	Channel (up)
6 - 7	Tune Rx (up slow)	Tune Rx (up slow)
6 - 8	Call (red)	-
6 - 10	Tune Rx (up fast)	Tune Rx (up fast)
9 - 2	Volume (down)	Volume (down)
9 - 4	Clarifier (down)	Clarifier (down)
9 - 5	Channel (down)	Channel (down)
9 - 7	Tune Rx (down slow)	Tune Rx (down slow)
9 - 8	Test	Call
9 - 10	Tune Rx (down fast)	Tune Rx (down fast)

Front Panel Switch Tests (8525B)

Connector Pin	8525B
1 - 5	Scan
1 - 6	Audio Mute
1 - 7	S'call Mute
1 - 8	Power On/Off
2 - 5	Tune
2 - 6	Mute off
2 - 7	USB/LSB
2 - 8	Emgcy Call
3 - 5	Clarifier
3 - 6	Channel
3 - 7	Channel
3 - 8	Call
4 - 5	Clarifier
4 - 6	Volume
4 - 7	Volume
4 - 8	-

6.2.4 Logic Levels

If the switches are found to be satisfactory, the lack of response may be caused by faults in the main microprocessor or the associated data buses. If this type of fault is encountered, the I²C bus lines should be monitored with an oscilloscope. This can be done at J1 pins 1 to 4 and P3 pins 1 to 3 on the Microprocessor Controller PCB. Operation of any of the front panel controls should cause the exchange of data via the bus lines. This should be seen on the oscilloscope as rapidly changing levels between +5 and 0V. No data on a line, or failure of the levels to change cleanly should be investigated further. Failure may be due to an IC or its load. Refer to 6.2.1. Ensure that the terminations of all interconnecting ribbon cables are correctly mated and aligned.

6.2.5 No Reception

If no signal is received, after confirming the supply voltages described in 6.2.2, the signal path should be traced back from the output stages by applying the appropriate signals at convenient points. Voltages to be expected at various points are shown in the circuit diagrams.

6.2.6 No Transmission

If no signal is transmitted, after confirming the supply voltages described in 6.2.2, a single tone approximately 1kHz at 20mV rms should be applied to the microphone input. The voltages to be expected in the transmit mode at various points with this input applied are shown in the circuit diagram.

6.2.7 Unlocked Synthesizer

Should the synthesizer lose lock (indicated by UL being shown on the channel display and Unlock indicators H1 or H2 on the RF Mixer and Dual Synthesizer PCB, being lit) the following procedure should locate the cause of the failure:

- Verify the correct voltage on Z2 as shown on the circuit diagram 04-02450.
- Verify that the Enable, Data and Clock pulses on J3 pins 3, 4 and 5 respectively are the correct levels (0 or +5V).
- Verify the correct output level from IC6 and IC8 as shown on the circuit diagram.
- Verify the VCO control voltages at TP8 and TP9 are within the range shown on the circuit diagram.
- Verify that the VCO frequencies and levels (V6 and V14 emitters) are as shown on the circuit diagram.

6.2.8 Typical PA Voltages

In order to optimise the amplifier performance the PA amplifier transistors are matched in pairs identified by a coloured dot. Measurements taken in this area will depend upon the matched pair of transistors fitted and the frequency of transmission.

The tables below are a guide to the peak-to-peak voltages to be expected at specified points in the PA circuit. They are given for full power output when driven with a two-tone input. For the tests the supply voltage is 13.6V and the output is terminated into a 50Ω load.

Frequency (MHz)	Battery Current (Amps)	V18/V19		V16/V17		V12	
		C Vpp	B Vpp	C Vpp	E Vpp	C Vpp	B Vpp
2	9.7	27	2.4	13.2	0.4	3.2	0.9
4	9.8	27	2.4	13.2	0.5	3.2	0.9
6	9.2	27	1.9	12.0	0.4	2.7	0.9
8	9.0	32	2.5	13.5	0.5	2.7	0.9
16	10.4	24	2.8	14.0	0.7	5.0	1.5
18	8.9	26	2.3	11.5	0.7	6.3	1.3
24	8.9	22	2.4	12.5	0.8	7.5	1.8

6.3 Dismantling and Re-assembly

6.3.1 General

It may be necessary to remove printed circuit boards from the transceiver in order to carry out certain repairs. The paragraphs which follow give instructions for the removal and re-installation of boards. While carrying out these the following general points should be observed:

- **Screwdriver**—Screws with Pozidrive heads are used in almost all locations. Ensure that the appropriate screwdriver of the correct size is used.
- **Connectors**—The ribbon cable header and multiway connectors used in some locations can be incorrectly mated with their corresponding connectors. Care must therefore be taken when re-installing to ensure that these connectors are correctly mated.

6.3.2 Top and Bottom Covers

To gain access to the boards, the top or bottom cover must be removed from the transceiver. To remove either cover, the two screws (one on each side) must be removed and the rear edge of the cover lifted and drawn back so that the front edge is released from the panel surround.

When re-installing the cover, it should first be placed on the transceiver with its front edge resting on the two spring clips of the panel surround. The front edge must then be pressed firmly down while it is slid forward under the panel surround. When the cover is correctly positioned the rear edge can be pressed down so that the retaining screws can be re-inserted and tightened.

6.3.3 Circuit Board Removal

Printed circuit boards connected directly to the Motherboard are easily removed. After disconnecting any flexible leads connected to the board, its retaining screws can be removed and the multiway sockets on the board can be withdrawn from the corresponding pins of the Motherboard. This should be done by progressively raising each socket a small amount so that the board rises evenly. The procedure is reversed to re-install the boards.

Note: When removing the Audio and IF 1650kHz PCB, the heat sink secured to the side of the cabinet should be released before the screws retaining the board. On re-installation it should be secured last.

To remove the boards mounted behind the front panel, the flexible leads should be disconnected and the two countersunk screws released from each side so that the panel can be withdrawn from the cabinet. The two boards can then be released and separated.

6.3.4 PA and Filter Assembly

Note: The PA output transistors can be replaced without removing the board from the heat sink. Refer to para 6.3.5.

The PA and Filter PCB (08-03021) can be removed as follows:

1. Disconnect:
 - Ribbon cable(s) connecting rear panel connector(s) to the Motherboard.
 - Cable loom connecting the Option PS connector (if fitted) to the Motherboard. (This connection is made by two 4-way connectors. Note their positions to avoid cross-overs when reconnecting.
 - The ribbon cable connecting the PA and Filter PCB to the Motherboard. (This can be disconnected at both ends and removed.)
 - The 4-way Molex connector connecting two coaxial cables to the PA and Filter PCB.
2. Release the two screws at each side of the PA and Filter PCB which secure the board and the heat sink to the chassis side rails.
3. Release the two screws at the rear edge of the Motherboard which secure it to the heat sink assembly. Note that these two screws are shorter than the other screws securing the board.
4. Slide the heat sink assembly complete with rear panel and PA and Filter PCB away from the chassis.
5. Release the four screws securing the PA transistors to the heat sink. Note that at least one of these screws may be concealed by a capacitor, one end of which may have to be unsoldered to gain access to the screw.
6. Release the screw securing the clamp on the two driver transistors. Note that this screw is longer than the other screws used to secure the board.
7. Release a further two screws which secure the board to the heat sink.
8. Release the earth screw and the three screws that secure the rear panel to the heatsink.
9. Lift the board clear of the heat sink.
10. If work on the PA and Filter PCB is extensive, the dc power input lead may be unsoldered so that the rear panel can be taken away from the board.

11. Before re-installing the board, clean all the components in contact with the heatsink and the corresponding surfaces of the heat sink. Re-coat the cleaned areas with Jermyn Thermaflow A30. To re-install the board reverse the removal procedure taking particular care with the following:
 - When remounting the board on the heatsink, ensure that R16 and V11 are correctly located in their holes in the heat sink and that a mica insulator is under V15.
 - Ensure that the screws removed in disassembly are re-installed in their correct locations.
 - Screws should not be tightened until the reassembly is complete. To avoid straining connections to the PA transistors the screws securing these should be tightened last.

6.3.5 Replacement of PA Transistors

Since the PA output transistors are fitted in matched pairs they should be replaced only in matched pairs. The gain groupings of the SRFH1008 (selected MRF455s) transistors are identified by a coloured dot. Transistors of the same dot colour only should be fitted.

The PA transistors can be replaced without removing the PA and Filter PCB from the heatsink. It is necessary to release only the screws securing the transistors and to unsolder connections as follows:

1. Remove the transistor flange fixing screws.
2. Use a de-soldering tool or 'Solder-wick' to remove the bulk of the solder from each connection. Gently pull the leads away from the PCB while heating the joint.
3. Clear away any excess solder from the emitter, base and collector pads.
4. Thoroughly clean the transistor mating surface on the heatsink with a cloth or tissue.
5. Form the leads of the replacement transistor using the discarded transistor as a guide.
6. Coat the transistor flange with a thin film of thermal compound, e.g. Jermyn Thermaflow A30.
7. Check the orientation and fit the new transistor. Tighten the flange fixing screws evenly.
8. Carefully resolder the transistor connections. This should be carried out quickly using a very hot tipped soldering iron.
9. Re-adjust the bias current. Refer to 7.3.13.

6.3.6 Replacement of Escutcheon or Switch Substrate

In replacing the switch substrate or the escutcheon on either the transceiver or the control head the two parts can only be removed from the front panel together and it is impracticable to separate them. It is therefore necessary to have replacements for both parts (and the window fitted over the numeric display behind the escutcheon) before the work is undertaken. Proceed as follows:

1. Release the two screws at each side of the front panel and disconnect the leads to the panel so that it can be removed completely from the transceiver or control head. (Be careful to retain the screws for re-assembly. Damage will result if they are replaced with longer screws.)
2. On the transceiver panel only: release the nut retaining the microphone connector and withdraw the connector and loom through the front panel.
3. On either transceiver or control head panels fitted with selective calling switches: disconnect the switches from the Display PCB, then squeeze the retaining fingers of the switch assembly while pressing the assembly forward out of the panel.
4. Disconnect the switch substrate connections from the Display PCB.
5. Taking care not to scratch the paint, insert a screwdriver blade or similar instrument under one of the left hand corners of the escutcheon and switch substrate and raise the corner. Grip the raised corner and peel off the escutcheon and substrate towards the right.
6. Withdraw the substrate connections through the slot at the right hand edge of the panel.
7. Clean away as much sealant as possible from the slot in the right hand side of the panel. (The slot must be at least clear enough for the connections of the new substrate to be inserted clearly.)
8. Use a heat gun to soften the connections of the replacement substrate, then form them to the required shape using the discarded substrate connections as a pattern.
9. When the connections have cooled the substrate should be offered into position to ensure that the correct settings have been made. If they are not correct the connections can be reheated and reset.
10. When the substrate connections have been satisfactorily formed, peel off the backing sheet from the substrate and position it on the front panel. When it is correctly positioned, press firmly on its face to ensure its adhesion to the panel.
11. Connect the switch substrate connections to the Display PCB
12. Test the switch operation as described in paragraph 6.2.3.
13. Refill the slot through which the connections pass with Expandite Silicone Sealant 88 (Codan Pt No. 71-30000-007). Ensure that the slot is completely sealed but that no excess sealant remains around the slot, particularly on the front face.
14. Peel off the backing sheet surrounding the window opening in the escutcheon and press the replacement window into place.

15. Peel off the backing sheet from the front face of the switch substrate and place the escutcheon over the substrate. When the escutcheon is correctly positioned press firmly all over its face to ensure its adhesion to the substrate.
16. If the panel was originally fitted with selective calling switches use a scalpel to cut out the required hole in the escutcheon. Refit the switches.
17. Reinstall the front panel on the transceiver or control head. Remake the connections and test the transceiver.



7

Adjustments

7.1 Introduction

Two types of adjustment are covered under separate headings.

- Channel Addition: change EPROM (no internal adjustments necessary)
- Preset Adjustments: normally factory-set adjustments will require attention only if components which affect their settings are replaced.

7.2 Channel Addition (EPROM Replacement)

The EPROM is mounted in a socket on the Microprocessor Controller PCB and may be changed as follows:

1. Place the transceiver upside-down on a bench with the power supply disconnected.
2. Remove the bottom cover by unscrewing the two retaining screws (either side of the transceiver) and lift the rear edge of the cover.
3. Two socket-mounted IC's will be found near the centre of the transceiver. The EPROM is identified by the number either:
 - 90-20283 (8525B)
 - 90-20278 (8528)
 - 90-20275 (8528S)
4. Carefully remove the EPROM from the socket. (A small screwdriver may be needed to prise it free.)
5. Plug in the new EPROM.
Note: The notch on the end of the EPROM must be on the left when viewed from the front of the transceiver, i.e. in the opposite direction to the other socketed IC.
6. Re-install the bottom cover by placing it on the transceiver so that the front edge rests on the two spring clips. Press down firmly on the cover's front edge and slide it forward until the screw holes are aligned. Re-install the screws.

7.2.1 Channel Addition, Programming P Channels (8528)

In 8528 series transceivers, ninety-nine 'P' channels can be programmed from the front panel to suit the user's requirements. However, to prevent transmission on frequencies for which the operator is not authorised, option TxD inhibits the entry of new transmit frequencies by the operator. This can be overridden by an internal link in order to program new transmit frequencies.

Enabling

Transmitter programming is enabled by shorting link 1 on the Microprocessor Interface PCB (refer to Fig. 7.1). The status of the link is noted by the microprocessor during the initialisation program; therefore it is only necessary to short the link (e.g. with a pair of tweezers) at switch on. Once the display panel is lit, the link may be removed but will remain effective until power is switched off. It should be noted that normal operation of the transceiver is inhibited in the programming mode. If it is intended to change or delete existing P channels, refer also to Program Inhibit Indication below.

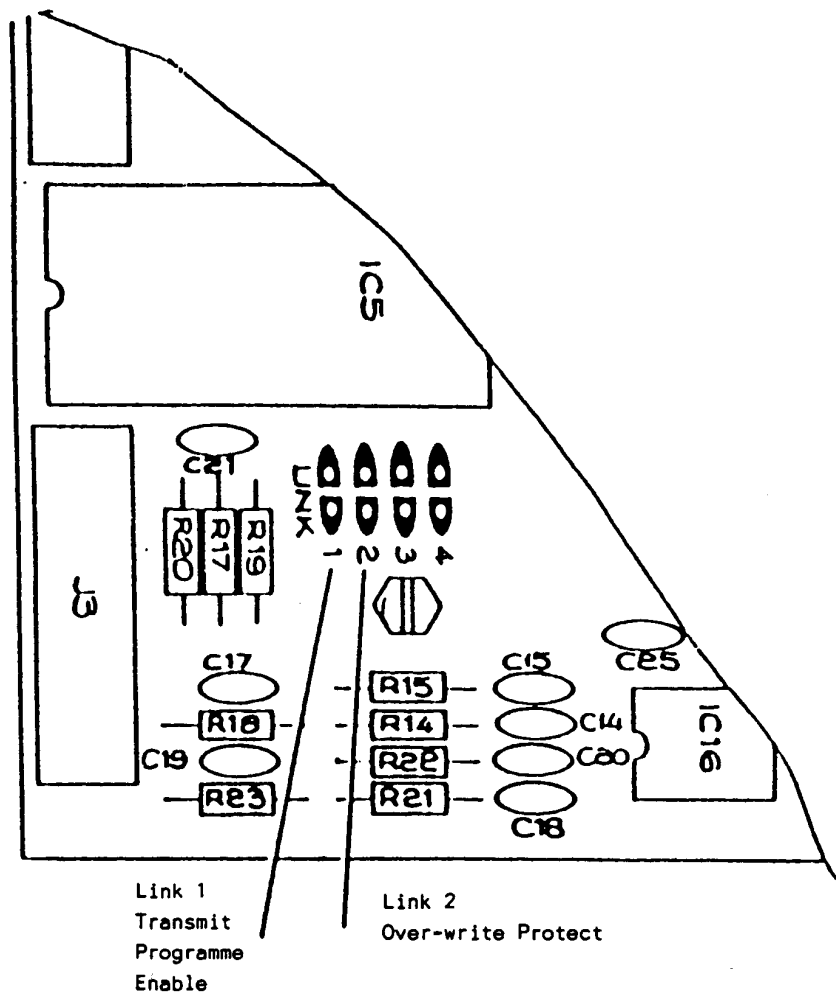


Figure 7.1 Microprocessor Interface PCB

Transmit Frequency Programming

Once the link is effective, transmit frequencies can be entered from the front panel as follows:

Action	Display will show	Remarks
Select any channel	Tx and Rx frequencies Channel No.	
Press Enter	Tx _____	Next action must be started within 60 seconds
Press number pads for transmit frequency	Tx 12.345.6	2000.0 to 24000.0
Press number pads for receive frequency (if same as Tx, press Enter only)	Rx _____	(23.000 in suffix H)
Press Enter	Rx 12.345.6	250.0 to 30.000.0
Press Enter	OPTION ___U__	Refer to Operators Handbook, section 5
Press Enter	P _____	
Press number pads for channel number	Pxx	
Press Enter	Tx and Rx frequencies P channel number	If the display shows prog inhib, USED or Full , refer to the corresponding heading below

Program Inhibit Indication

Established P channels can be protected from being accidentally deleted or over-written by the insertion of Link 2 on the Microprocessor PCB inside the transceiver (refer to figure 7.1). If an attempt is made to over-write or delete a channel when the link is installed, the display will show prog inhib for a few seconds when Enter is pressed. The Tx and Rx parameters can still be accepted by entering a new channel number and pressing Enter again. To over-write or delete existing channels, the transceiver must be switched off and the link unsoldered. The link should be resoldered with the transceiver switched off when the programming has been completed.

Used Indication

Channel numbers will normally be accepted on pressing the **Enter** pad. However, if a channel with the entered number has previously been programmed and the over-write link is not installed, the display will show USEd. The channel number can be either:

1. changed by entry of a new number on the number pads, or
2. accepted and the previously programmed frequencies over-written by a second operation of the Enter pad.

Full Indication

When all ninety-nine P channels have been programmed, on pressing the Enter pad to accept another channel, the display will show Full. A further press of the Enter pad will over-write the nominated channel. Alternatively some redundant channels can be deleted and then re-used. If the over-write protection link is installed, this must first be removed before channels can be deleted.

Too Hi, Too Lo Indications

If an attempt is made to program a channel with either a Tx or Rx frequency outside the range of the transceiver, an error message will be displayed. The error can be corrected by simply entering a new number on the number pads.

7.3 Preset Adjustments

7.3.1 Test Equipment Required

- A calibrated CRO with 10X probe with $10\text{M}\Omega$ and less than 12pF input impedance. Y amplifier frequency response of at least 25MHz .
- RF dummy load, 50Ω 100W RMS minimum and Power Meter to suit.
- RF signal generator covering the range 250kHz to 30MHz and capable of providing calibrated signals down to $0.25\mu\text{V}$ EMF from a 50Ω source.
- Frequency counter capable of resolving to 1Hz frequencies up to 24MHz .
- Regulated Power Supply which can be set to $13.6\text{V} \pm 0.2\text{V}$ and capable of supplying 20A peak current.
- Two-tone (i.e. 700Hz and 2300Hz) audio generator capable of providing $0\text{--}100\text{mV}$ RMS.
- Spectrum analyser suitable for SSB
- Multimeter or meters for measuring voltages ($20\text{k}\Omega/\text{V}$ or better) and current (100mA and 1A ranges) and an audio voltmeter.
- Transceiver Test Unit to Codan drawing 04-01868. (The isolating transformer should be screened to prevent pick-up from nearby mains transformers.)
- Square-wave generator capable of 5.5V pp at 100Hz .
- Decade resistance box for ease of determining select-on-test (SOT) resistors. (A resistance box constructed using the E12 series values of resistors is very useful.)

Before making any adjustments, the supply voltage must be set to $13.6\text{V} \pm 0.2\text{V}$.

When working on the low level stages, e.g. the receiver and exciter, the PA may be isolated by removing the dual coax socket to the PA and Filter PCB. This will prevent unnecessary heating of the heatsink and removes the possibility of high level RF fields being picked up by test leads which may cause erroneous measurements or transmitter instability. Note that this also disconnects the receive path (between the PA and Filter PCB and RF Mixer and Synthesizer PCB).

7.3.2 Voltage Regulators

None of the voltage regulators used are adjustable, so only their output voltage can be checked. The location and correct output voltages are as follows:

1. B rail regulator, $10V \pm 0.2V$; IC1 on Motherboard.
2. +5V regulators, $5V \pm 0.4V$.
 - IC2 on Motherboard.
 - IC7 on Audio and 1650kHz PCB
 - IC4 on RF, Mixer, and Dual Synthesizer PCB.
 - IC9 on Microprocessor Controller PCB
 - IC1 on Mic Amp and Interface PCB (8530 Control Head only).
3. 26V regulator, $26V \pm 1V$; TP7 on RF Mixer and Dual Synthesizer PCB.
4. 9V regulator, $9V \pm 0.25$ Volts; emitter of V1 on RF Mixer and Dual Synthesizer PCB.

These voltages should be checked with the transceiver in receive mode.

7.3.3 Crystal Oven

The oven temperature cannot be adjusted but should be checked after allowing a five minute warm-up period. The temperature should be approximately 60°C .

7.3.4 VCO Adjustments (RF Mixer and Dual Synthesizer PCB)

These adjustments must be made with the metal shields in place.

VCO1

1. Select 30MHz frequency.
2. Using a DC Voltmeter or CRO, monitor TP8.
3. Adjust C42 via access hole in shield cover for $22.5V \pm 0.5V$ DC on TP8.
4. Select 250kHz; check TP8 is at $2V \pm 1V$ DC, and the 'unlock' LED for VCO 1 is not lit.

VCO2

1. Select any frequency.
2. Using a DC Voltmeter or CRO, monitor TP9.
3. Adjust C79 via access hole in shield cover for $2.7V \pm 0.2V$ DC

7.3.5 45MHz IF Alignment—Receive

1. Ensure the dual coax socket is connected to the PA and Filter PCB.
2. Connect the signal generator to the antenna socket.
3. Select a channel (USB) and adjust the signal generator output to the selected channel frequency plus 1kHz.
4. Increase the signal generator output until the signal is heard from the loudspeaker.
5. Connect the audio voltmeter to the Demodulator output on the Audio and IF 1650kHz PCB (TP2).
6. Adjust the 45MHz IF trimmer capacitors (outermost holes in shield lid) to half mesh i.e. screwdriver slots parallel to the long edge of the shield.
7. Adjust L29 and L32 (centre holes) for a maximum signal on the audio voltmeter.
8. Reduce the signal generator output and repeat step (7) until no further increase can be obtained on the audio voltmeter (below AGC threshold).

7.3.6 1650kHz IF Alignment

1. Align the 45MHz IF as above.
2. While still in Rx, peak the audio voltmeter reading by adjusting L1, L2, and L3 (on the Audio and 1650 IF PCB) and reducing the signal generator output to remain below AGC threshold.
3. When no further increase in the audio voltmeter reading can be achieved, check that the signal generator output is below 0.35 μ V PD for 10dB SINAD.

7.3.7 45MHz IF Alignment—Transmit

CAUTION

THE PROCEDURE WHICH FOLLOWS INVOLVES ALTERNATELY APPLYING A SIGNAL GENERATOR TO THE ANTENNA SOCKET TO SET RECEIVER ADJUSTMENTS AND SWITCHING TO TRANSMIT TO SET TRANSMIT ADJUSTMENTS. THE SIGNAL GENERATOR WILL BE DAMAGED IF IT REMAINS CONNECTED WITH THE TRANSCEIVER IN TRANSMIT.

1. Align the 45MHz IF in receive as above.
2. Align the 1650kHz IF as above.
3. DISCONNECT SIGNAL GENERATOR FROM ANTENNA SOCKET.
4. Disconnect dual coax socket from PA and Filter PCB.
5. Connect audio two-tone source to microphone input and switch transceiver to transmit.
6. Connect CRO across TP1 on the RF Mixer and Dual Synthesizer PCB.

7. Adjust L29 and C64 (second and fourth holes from left-transceiver facing toward operator) for maximum amplitude of the displayed waveform.
8. Set the transceiver to receive and repeat steps (1) to (5) of 7.3.5.
9. Adjust C58 and L32 (extreme left and third hole from left) for maximum signal on the audio voltmeter.
10. DISCONNECT THE SIGNAL GENERATOR FROM ANTENNA SOCKET.
11. Switch the transceiver to transmit.
12. Ensure the two-tone signal is applied to the input and observe the amplitude of the waveform displayed on the CRO:
 - If the amplitude is below 200mV pp return to step (7) and repeat the procedure.
 - If the amplitude is greater than 200mV pp, disconnect the dual coax socket from the PA and Filter PCB and confirm that the amplitude increases to at least 400mV pp.
13. Reconnect the dual coaxial socket.

7.3.8 Highpass Filters

Five adjustments are required for the highpass filters, one for the Broadcast filter on the PA and Filter PCB and one each for the band selected filters on the RF, Mixer, and Dual Synthesizer PCB.

To adjust these filters:

1. Connect a CRO, set for maximum sensitivity, across TP1 on the RF Mixer and Dual Synthesizer PCB.
2. Connect a signal generator to the antenna socket.
3. Select a channel within each of the Frequency ranges shown in table below, in turn.
4. With each channel selected set the signal generator to the corresponding Sig Gen Freq and adjust its output level until adequate indication is seen on the CRO. (A starting level of 100mV is suggested.) Adjust the corresponding inductor for minimum indication on the CRO.

Channel Frequency (MHz)	Sig Gen Freq (MHz \pm 20kHz)	Inductor	Location of inductor
2 - 3.1	1.45	L14	PA & Filter PCB
3.1 - 4.8	2.2	L11	RF Mixer & Dual
4.8 - 7.5	3.4	L8	Synth PCB
7.7 - 11.6	5.3	L5	"
11.6 - 18	8.2	L2	"
18 - 24	10-12	No Adjustment	"

Note: When Option LF is fitted, the first adjustment (2 – 3.1) must be made with the signal generator frequency set to 1.18MHz.

7.3.9 Noise Limiter

1. Connect a DC Voltmeter to TP6 on the RF, Mixer, and Dual Synthesizer PCB. With no signal applied TP6 should be at approximately 2.5V DC.
2. Connect a signal generator to the antenna socket, select a channel (USB) and set the signal generator output to the selected channel frequency plus 1kHz.
3. Increase the signal generator output until the voltage at TP6 reduces to 2 Volts DC.
4. Adjust L47 for a minimum voltage on TP6.

Note: The null is not well defined.

7.3.10 Frequency Adjustment (USB)

1. Select the highest channel frequency (above 10MHz if possible) that is not transmit inhibited. Remove the dual coax socket to the PA and Filter PCB.
2. Connect the frequency counter across TP1 on the RF Mixer and Dual Synthesizer PCB.
Allow at least 5 minutes warm up before adjustment.
3. Press and hold the **Tune** pad.
4. Adjust C143 on the RF Mixer and Dual Synthesizer PCB for the correct frequency for the channel selected.

Note: If the adjustment range of C143 is not enough, the value of capacitor C142 may be changed. The temperature coefficient of the replacement capacitor must match that of the factory-fitted capacitor.

5. Reconnect the dual coax socket.

7.3.11 Frequency Adjustment (LSB)

8525B/8528

1. Perform USB frequency adjustment as above.
2. Select a channel with LSB mode enabled.
3. Press the TUNE pad and adjust C162 until the output frequency (at TP1) is correct for the selected channel.
4. If the range of C162 is insufficient C161 may be altered to compensate.

8528S

If the transceiver is fitted for LSB operation:

1. Select a channel with LSB mode enabled.
2. Connect the frequency counter, via a high impedance (x10) probe, to the inner conductor of the Local Oscillator cable on the RF Mixer and Dual Synthesizer PCB.
3. Adjust C162 for 1647kHz 1Hz indication on the counter.
4. If the range of C162 is insufficient C161 may be altered to compensate.

7.3.12 Mute Adjustment

1. Connect the transceiver to an antenna (a short length of wire will suffice) and select an unoccupied channel.
2. Press the Audio Mute pad (8525B), or the Mute On/Off pad (8528), to get the Mute indicator lit.
3. Begin with R73 on the Audio and IF 1650kHz PCB fully anti-clockwise and slowly rotate the control clockwise until the mute audio gate opens.
4. This is the threshold of mute operation. In order to reduce the sensitivity, rotate the control anti-clockwise 1/4 turn.
5. The mute circuit should now be sensitive enough to detect weak signals without false triggering on noise pulses. However, if desired, the sensitivity may be varied from this setting to suit individual requirements.

7.3.13 PA Adjustments

Disconnect the dual coax socket from the PA and Filter PCB.

Driver Bias

1. On the PA and Filter PCB (08-03743) remove the link feeding the centre tap of T3 primary and replace with an ammeter set to read 10 to 20mA.
2. Select on test a value for R46 for a current reading between 10 and 15mA with the microphone PTT switch pressed.
3. Remove the ammeter and re-install the link.

PA Bias

1. Remove link marked 'PA' on the PA and Filter PCB (F2 on circuit diagram 04-02452).
2. Replace link with an ammeter set to read 100 to 200mA.
3. Adjust R48 for a current reading between 100 and 150mA with the microphone PTT switch pressed.
4. Remove the ammeter and re-install the link.
5. Reconnect the dual coax socket.

7.3.14 Output Power

1. Ensure the dual coax socket is connected to the PA and filter PCB.
2. Connect an RMS or PEP power meter with dummy load to the antenna socket.
3. Connect a CRO via a $47\text{k}\Omega$ resistor to the antenna socket.
4. Connect the audio output of the two-tone source to the test unit (AF in). Ensure the microphone amplifier is into compression.
5. Select the lowest frequency channel on the transceiver and operate the microphone PTT switch.
6. Select a value for the SET PWR resistor (R10) to set the two-tone output to:
 - for type 8525B/8528—100W PEP (i.e. 200Vpp into 50Ω)
 - for type 8528S—125W PEP (i.e. 224Vpp into 50Ω)
7. Check the IMD (Intermodulation Distortion) over the band 2MHz to 24MHz. The power output may be reduced if necessary to give -26dB IMD on the worst channel.

7.3.15 Options SD, SDE and SDEM

With these options fitted the oscillator frequency of the phase locked loop on the Selective Call PCB must be set up as follows:

1. Apply a 1775Hz sine wave at 1.0Vpp to pin 2 of J1 on the Selective Call PCB. (Pin 3 ground.)
2. Connect a dc voltmeter between TP2 and TP3 of the PCB. (Polarity may be either way, connect so that meter deflection is forward.)
3. Adjust R15 for 0V \pm 50mV deflection of the voltmeter.

7.3.16 Option TD

With this option fitted the Two-tone Decoder PCB can be set up, if necessary, as follows:

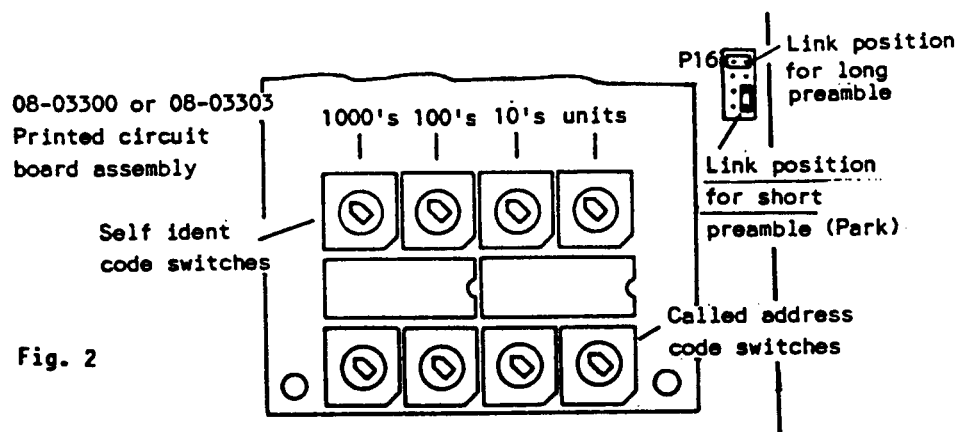
1. Using the table on Drawing 04-02231 select values for R25, R26 and R31 appropriate to the frequency nearest the nominated difference frequency to which the Two-tone Decoder is to respond. Connect these into the appropriate locations.
2. Connect a high-impedance frequency counter via a 100k Ω resistor to TP4 on the Two-tone Decoder PCB.
3. Disconnect J2 (Audio input).
4. Switch on power to the unit and observe the frequency counter. Adjust R30 on the Two-tone Decoder PCB for an indicated frequency within 2Hz of the nominated difference frequency.

Note: If the nominated frequency cannot be obtained within the range of R30, coarse adjustment can be made by selection of the value of R32.

5. Reconnect J2.
6. Arrange for the reception of two-tone calls with various difference frequencies and ensure that the transceiver responds to only those calls which contain the nominated frequency difference.

7.3.17 Selective Call Code Setting (8525B)

When any of the selective calling options are fitted, identity code switches within the unit (refer to Figure 7.2) must be set. With Options SE2 or SDE, both the self ident and the called address (i.e. the identification of the station it is intended to call) are set entirely on the internal switches. With Options SDEM or SM the self identification is set on the internal switches but some or all of the called address switches are duplicated on the front panel of the unit or the control head. This allows the operator to control at least some of the digits in the called address. With these options, therefore, only those switches not duplicated on the front panel need be set. The front panel switches always control the lower order digits leaving the higher orders to be set on the internal switches, e.g. if there are two switches on the front panel they will control the units and 10's leaving the 100's and 1000's to be controlled by the internal switches. In most cases all four digits are controlled from the front panel.



16-00036-002

Figure 7.2 Selective Call Settings

The switches can be set as follows:

1. Remove the transceiver bottom cover by unscrewing the two retaining screws (one on either side) and lifting it clear of the main assembly by raising the rear edge of the cover first.
2. Locate the Selective Call PCB 08-03300 or 08-03303 and identify the code switches shown in Figure 7.2.
3. Set the self ident switches to the digits of the identification number of the local station.

Note: Codes ending in '00' should not be used since they are reserved for operation of the group call facility.

4. Set the called address switches:
 - With Options SE2 or SDE fitted—set all the switches in the group to the digits of the identification number of the station to be called.
 - With Options SDEM or SM fitted—set any of the switches in the group which are not duplicated on the panel. The settings of switches corresponding to those on the front panel can be disregarded, e.g. if there are three switches on the front panel, the 1000's internal switch must be set to the first digit of the group of numbers which can be called. Other switches can be left at any setting.
5. Record the code numbers to which the self ident and called address switches have been set on the frequency label/chart.
6. Re-install the bottom cover by first placing it on the transceiver so that the front edge rests on the two spring clips. Then press firmly on the front edge of the cover and slide it forward under the panel surround until the screw holes are aligned. Resecure with the fixing screws.

7.3.18 Message Length Setting

When a transceiver is to work into a station which uses the selective call scan facility, the transmitted identification code preamble time must be extended. This is achieved by the position of a link on P16 as shown in Figure 7.2.

7.3.19 Selective Call Settings (8528)

Refer to Operator's Handbook.

7.4 Receiver Performance Checks

7.4.1 Sensitivity and Signal + Noise to Noise Ratio

Connect an AC voltmeter across the audio output. Set the signal generator to 0.35 μ V PD output, connect it to the antenna socket and adjust the frequency to produce a 1kHz audio output.

Adjust the signal generator to a frequency outside the receiver passband and check that the audio output drops by at least 10dB.

7.4.2 AGC Check

Reset the signal generator output to 50mV PD and adjust the frequency to produce a 1kHz audio output. Reduce the volume to a convenient level. Reduce the signal generator output until the receiver output drops by 6dB. The signal generator level should be less than 2.5 μ V PD.

7.4.3 Audio Output

Increase the signal generator output to 50 μ V PD, adjust the frequency for 1kHz audio output. The audio output should exceed 4V RMS at the onset of clipping, as displayed on a CRO.

7.4.4 Selectivity (USB Operation)

Set the signal generator output to 0.5 μ V PD and note the audio output reference level. Increase the signal generator output 60dB and, using the Frequency Counter on the signal generator, adjust the frequency to -1 kHz and then to $+4.2$ kHz from SCF. At these points the audio output should be less than reference level.

7.4.5 Clarifier Operation

With an input signal of SCF $+1$ kHz (SCF preferably greater than 10MHz) adjust clarifier and ensure frequency shifts of 0.001% (10ppm) can be made in the type 8525B/8528, or 180Hz in the 8528S.

7.4.6 Noise Limiter Operation

Connect a BNC T-piece into the 50 Ω coax from the signal generator to the transceiver. To the unoccupied socket add a BNC to two-terminal adaptor. Connect the output from a square-wave generator at a level of 5Vpp at 100Hz via a 100pF capacitor to the adaptor.

With the signal generator output set to produce a 1kHz audio output at a 0.5 μ V PD level switch the noise limiter on and off by shorting TP6 on the RF Mixer and Dual Synthesizer PCB. When ON, the audio tone should be clearly heard if the noise limiter is effective.

7.5 Transmitter Performance Checks

7.5.1 Frequency

Check as in section 7.3.10.

7.5.2 Clarifier (when enabled on 8525B-0 only)

Select highest channel frequency on which the clarifier is enabled. Measure output frequency (Tune pad pressed) at upper and lower clarifier limits for a range of 0.001% (10ppm).

7.5.3 ALC

Use the Transceiver Test Unit and Audio Two-tone Source to modulate the transmitter. Slowly increase the audio input until the output power just ceases to increase (ALC threshold). Note the PEP output and increase the audio input by 30dB. The increase in output should be less than 0.5dB.

7.5.4 Power Output and Intermodulation Distortion

8525B/8528

The power output at 2MHz is 100W PEP falling to 90W PEP at 24MHz (± 0.5 dB) and the IMD should be better than -26 dB as measured on the spectrum analyser (use 700Hz and 2300Hz Audio Tones).

8528S

Power output at 2MHz is 125W PEP falling to 90W PEP at 24MHz (± 1 dB); the IMD should be better than -26 dB as measured on the spectrum analyser. (Use 700Hz and 2300Hz Audio Tones.)

Note: The indication of 100W PEP with two-tone modulation will depend upon the type of meter used to make the measurement, as follows:

- Peak reading meter: 100W
- RMS reading (thermal): 50W
- Average reading (Bird Model 43): 40.5W

7.6 Emergency Call Frequencies

8525B/8528 RFDS

Select an RFDS channel and disconnect dual coax socket to PA and Filter PCB. Press the **Emgcy Call** pad and measure the frequencies on pins 10 and 13 of IC12 on the Microprocessor Controller PCB. Frequencies should be 880Hz \pm 2Hz and 1320Hz \pm 2Hz respectively. Reconnect dual coax socket.

8528S Marine

On pressing the Emergency Call Test pad the marine emergency call is generated for approximately 45 seconds by the two-tone generator on the Microprocessor Controller Assembly (pressing the Test pad alone generates the tones without keying the transmitter.) The signal consists of alternate bursts of 1300 2Hz and 2200 2Hz; each burst lasting approximately 250ms. This can be monitored at pin 10 of IC12 on the Microprocessor Assembly 08-02451, using an oscilloscope with the time base set so that these 250ms bursts can be seen as two different frequencies. The individual frequencies can be measured using a Lissajous figure technique.



8

Parts List

8.1 General Information

The parts list for each assembly contains the following information:

- circuit reference number.
- description giving the value and type of component.
- manufacturer and manufacturer's part number.
- Codan part number.

Note: Items having numerical references identifying specific components or subassemblies may be encountered in the parts lists included in this handbook. These items, selected from master manufacturing information, identifying parts which either are useful for maintenance purposes or relate to other items as cross referenced in the remarks column.

The following abbreviations are used for resistor and capacitor types:

Resistors	Capacitors
CC—carbon composition	AS—solid aluminium electrolytic
CF—carbon film	CC—ceramic multilayer chip
MF—metal film	CE—ceramic
MG—metal glaze	EL—wet aluminium electrolytic
MO—metal oxide	M—stacked mica
WW—wire wound	PC—polycarbonate
PE—polyester	
PP—polypropylene	
PS—polystyrene	
PT—PTFE	
TA—solid tantalum	

8.1.1 Ordering Information

When ordering replacement components, all the following information should be quoted to minimise the risk of obtaining the wrong part and to expedite despatch:

- equipment type (i.e. Type 8525B Transceiver)
- component location (e.g. Audio & IF 1650kHz PCB 08-03025)
- component circuit reference number (e.g. R3)
- full component description (e.g. Resistor 330k Ω 5% 0,33W CF)
- manufacturer and manufacturer's Part Number
- Codan Part Number.

8.1.2 Component Substitution

Due to continuous process of updating equipment and changes in component availability, minor variations in components may be noted from those listed. Equipment performance is in no way adversely affected by their substitution.

When replacing general purpose components (resistors, capacitors etc.), equivalent parts of other manufacture may be used provided that they have similar tolerances, voltage/power rating and temperature coefficients as those of the specified part.

8.2 Parts List

8.2.1	Transceiver Sundry Parts	08-03786-100
	Includes Control Head Parts	
8.2.2	RF Mixer and Dual Synthesizer 03740-001	08-
	Includes: 45MHz IF PCB	08-03097
	VCO1 PCB	08-03098
	VCO2 PCB	08-03099
8.2.3	Audio and IF 1650kHz PCB	08-03025
8.2.4	Microprocessor Controller	08-03779-001
	Includes: Microprocessor Interface	08-03741-001
	Microprocessor Assembly	08-03742-001
8.2.5	Motherboard	08-03744-001
	Includes: Filter, Remote Control PCB	08-03127
	Option R	15-10272
	Option PS	15-10271
8.2.6	Display PCB, LCD	08-03745-001
8.2.7	Display PCB, 8532	08-04666-001
8.2.8	Display PCB, Transceiver	08-03944-001
8.2.9	Display PCB, Head	08-03945-001
8.2.10	Mic Amp and Interface PCB	08-03039
8.2.11	PA and Filter	08-03743-001
8.2.12	PA/Exciter Interface	08-03692
8.2.13	Selective Call SDE, SDEM PCB	08-03300
8.2.14	Selective Call SD	08-03300-000
8.2.15	Two-tone Decoder PCB	08-03273

8.2.16	Cover and Fan Assembly	08-03690
Includes:	Fan Controller	08-03334
8.2.17	Antenna Driver PCB	08-04285-001
8.2.18	Cable Interface (Transceiver/Head)	08-03051
8.2.19	Data Mode Switch PCB	08-05041-001
8.2.20	Microprocessor Controller (RS232)	08-05090-001
Includes:	Microprocessor Interface	08-05088
	Microprocessor Assembly	08-05089



9

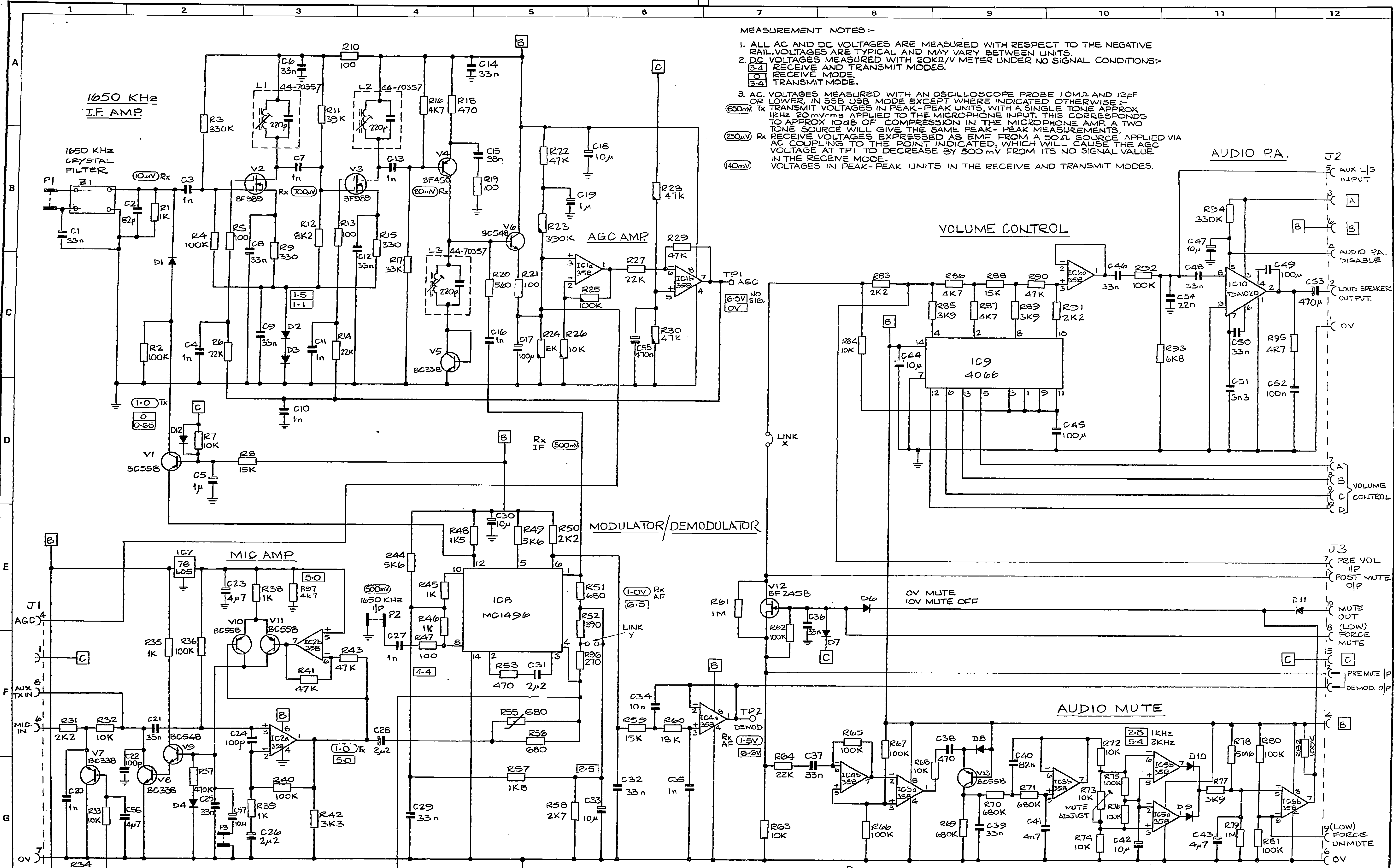
Drawings

Drawings

Transceiver Layout		16-00035-004
Control Head Layout,	8530	16-00035-003
Control Head Layout,	8531	16-00035-005
RF Mixer and Dual Synthesizer	Circuit Diagram	04-02450
45MHz IF	PCB Assembly	08-03740
VCO1 and Mixer	PCB Assembly	08-03097
VCO2 and Mixer	PCB Assembly	08-03098
	PCB Assembly	08-03099
Audio and IF 1650kHz	Circuit Diagram	04-02093
	PCB Assembly	08-03025
Microprocessor Controller	Circuit Diagram	04-02451
Microprocessor Interface	PCB Assembly	08-03741
Microprocessor Assembly	PCB Assembly	08-03742
Microprocessor Controller	Circuit Diagram	04-03031
Microprocessor Interface	PCB Assembly	08-05088
Microprocessor Assembly	PCB Assembly	08-05089
Motherboard and Chassis	Circuit Diagram	04-02453
Motherboard	PCB Assembly	08-03744
Filter Remote Control	PCB Assembly	08-03127
Display PCB, LCD	Circuit Diagram	04-02454
	PCB Assembly	08-03745
Display PCB, 8532	Circuit Diagram	04-02875
	PCB Assembly	08-04666
Display PCB's	Circuit Diagram	04-02579
Display PCB, Transceiver	PCB Assembly	08-03944
Display PCB, Head	PCB Assembly	08-03945
Mic Amp & Interface, Control Head	Circuit Diagram	04-02096
	PCB Assembly	08-03039
PA & Filter	Circuit Diagram	04-02452
	PCB Assembly	08-03743

PA & Exciter Interface	Circuit Diagram PCB Assembly	04-02434 08-03691
Selective Call SD/SDE/SDEM Selective Call	Circuit Diagram PCB Assembly	04-02250 08-03300
Two-tone Decoder	Circuit Diagram PCB Assembly	04-02231 08-03273
Fan Controller	Circuit Diagram PCB Assembly	04-02260 08-03334
Antenna Driver	Circuit Diagram PCB Assembly	04-02724 08-04285
Data Mode Switch	Circuit Diagram PCB Assembly	04-03018 08-05041
Option R	Fitting Instructions	15-10272-001
Option PS	Fitting Instructions	15-10271-001
Option SM 8530	Fitting Instructions	15-10282-001
Option SD 8528	Fitting Instructions	15-10366-001
Option SDE 8525B	Fitting Instructions	15-10274-001
Option SDEM 8525B	Fitting Instructions	15-10275-001
Option TD	Fitting Instructions	15-10276-001
Option AD	Fitting Instructions	15-10384-001
Option DM	Fitting Instructions	15-10411-001 (2 pages)
Option RS-8528	Fitting Instructions	15-10412-001
Option F	Fitting Instructions	15-10339-010
Test Unit	Circuit Diagram	04-01868





MEASUREMENT NOTES:-

- ALL AC AND DC VOLTAGES ARE MEASURED WITH RESPECT TO THE NEGATIVE RAIL. VOLTAGES ARE TYPICAL AND MAY VARY BETWEEN UNITS.
- DC VOLTAGES MEASURED WITH 20KΩ/V METER UNDER NO SIGNAL CONDITIONS:-
 - 3-4 RECEIVE AND TRANSMIT MODES.
 - 3-4 RECEIVE MODE.
 - 3-4 TRANSMIT MODE.
- AC VOLTAGES MEASURED WITH AN OSCILLOSCOPE PROBE 10MΩ AND 12PF OR LOWER, IN SSB USB MODE EXCEPT WHERE INDICATED OTHERWISE:-
 - 650mV Tx TRANSMIT VOLTAGES IN PEAK-PEAK UNITS, WITH A SINGLE TONE APPROX 1KHz 20mVrms APPLIED TO THE MICROPHONE INPUT. THIS CORRESPONDS TO APPROX 10dB OF COMPRESSION IN THE MICROPHONE AMP. A TWO TONE SOURCE WILL GIVE THE SAME PEAK-PEAK MEASUREMENTS.
 - 250μV Rx RECEIVE VOLTAGES EXPRESSED AS EMF FROM A 50Ω SOURCE APPLIED VIA AC COUPLING TO THE POINT INDICATED, WHICH WILL CAUSE THE AGC VOLTAGE AT TP1 TO DECREASE BY 500mV FROM ITS NO SIGNAL VALUE IN THE RECEIVE MODE.
 - 140mV VOLTAGES IN PEAK-PEAK UNITS IN THE RECEIVE AND TRANSMIT MODES.

ALL DEVICES BASE VIEW UNLESS OTHERWISE STATED

ASSY 08-03025
PCB 07-00385

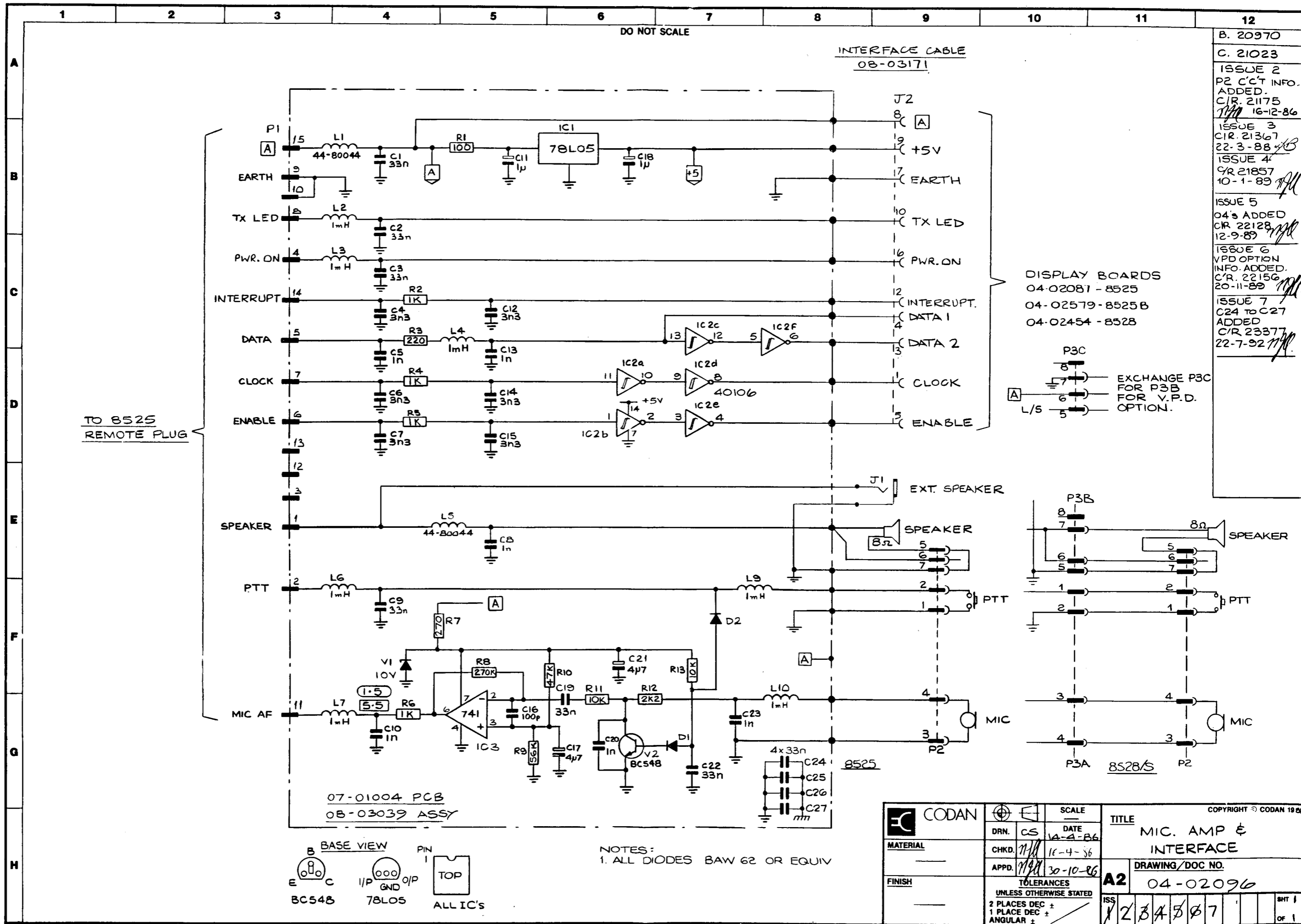
NOTES
1. ALL DIODES BAW62 OR EQUIVALENT
2. RESISTORS SHOWN ARE 2%

CODAN		SCALE	TITLE	DATE
DRN.	DO	17-4-86	AUDIO & IF	17-4-86
CHKD.	17/11	21-4-86	1650 KHz	
APPD.	17/11	30-10-86	DRAWING/DOC NO.	
FINISH		TOLERANCES	A1	04-02093
UNLESS OTHERWISE STATED		2 P.ACES DEC ±	ISS	10/12
1 PLACE DEC ±		ANGULAR ±	SHT	1

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ISSUE 8
ISSUE 9
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ISSUE 11
ISSUE 12

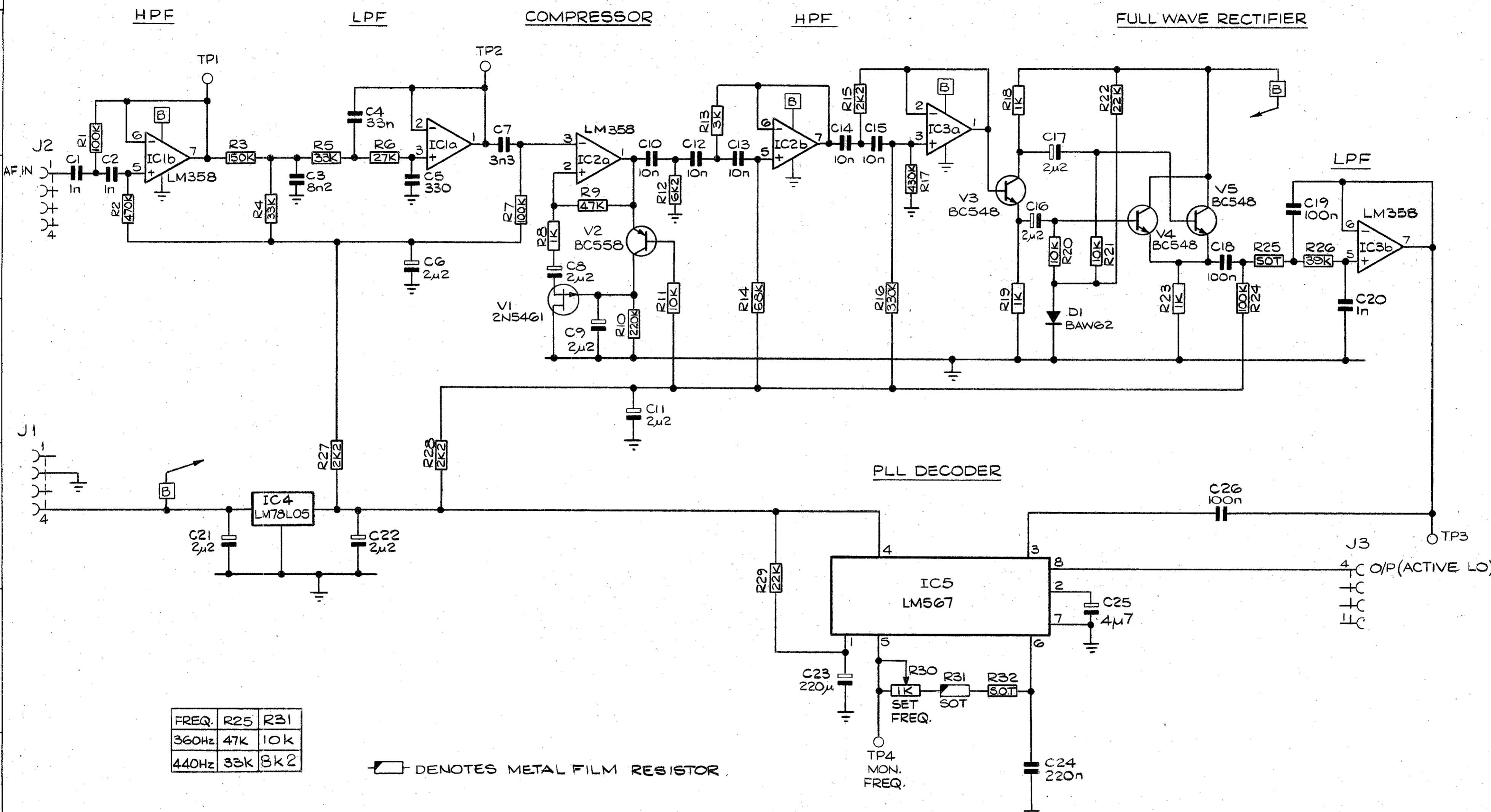
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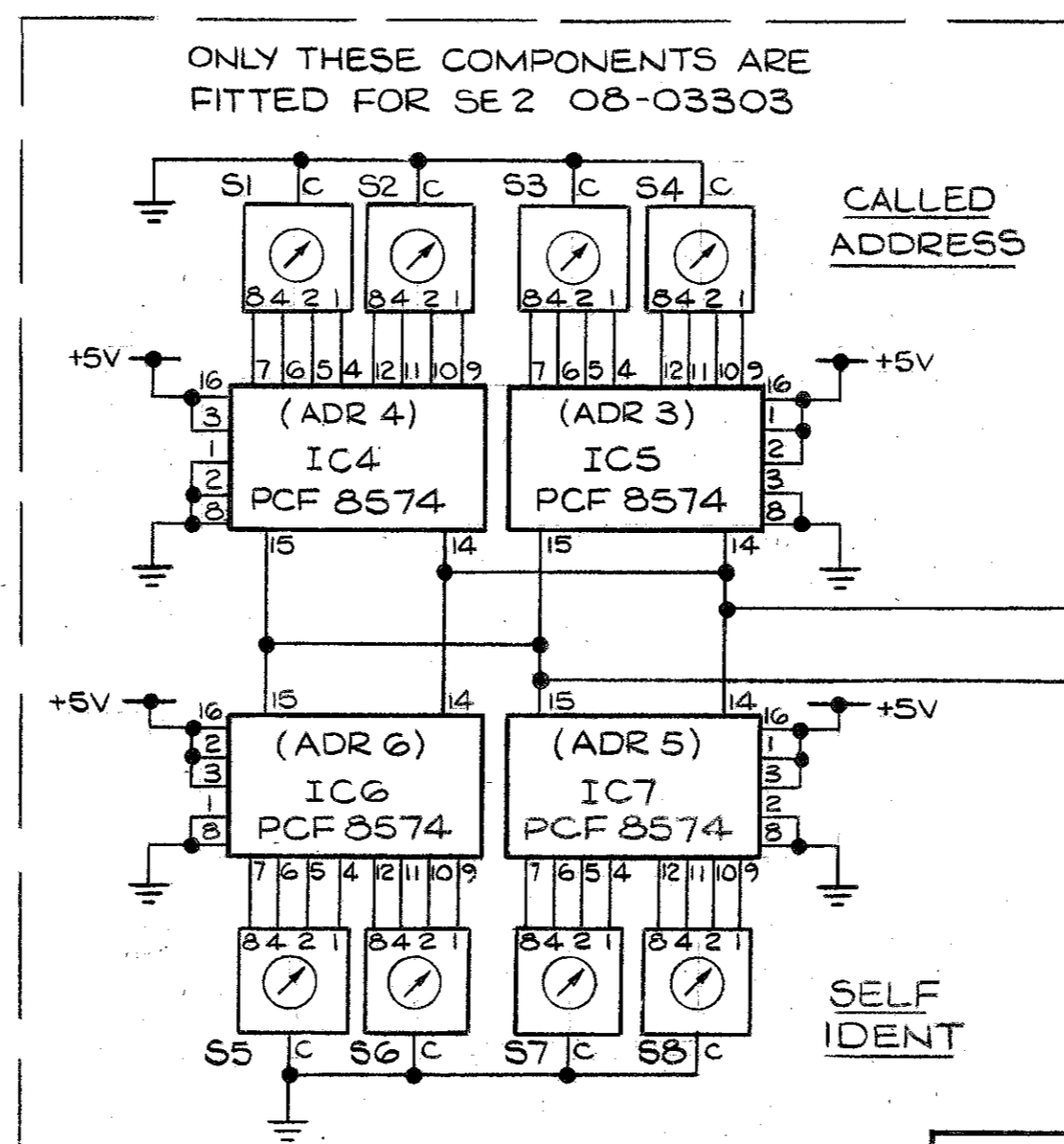
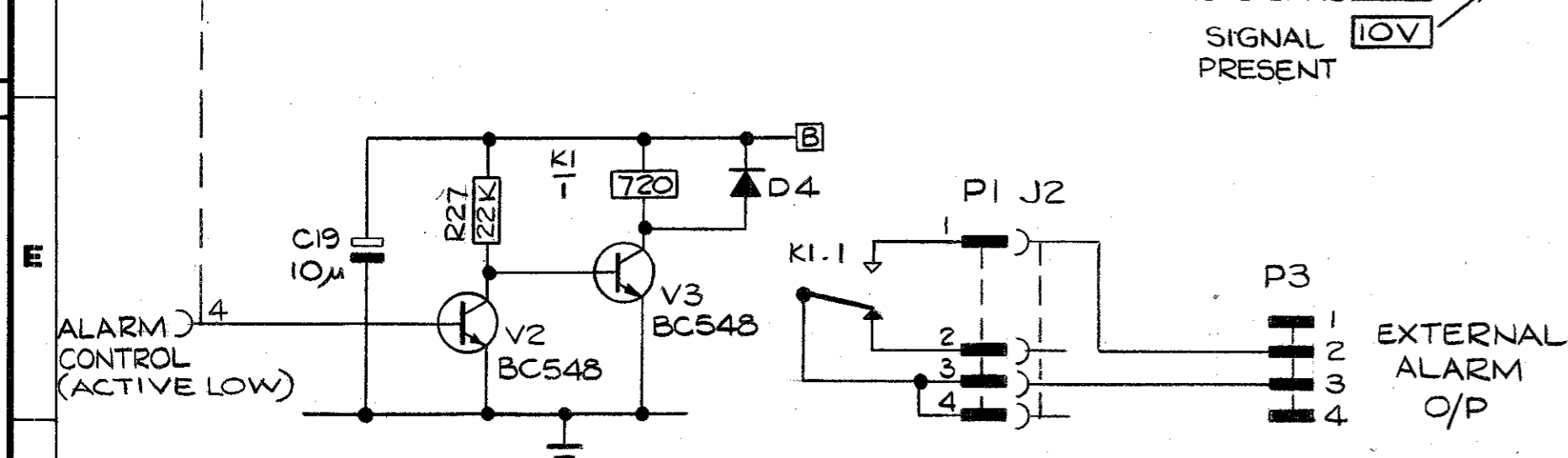
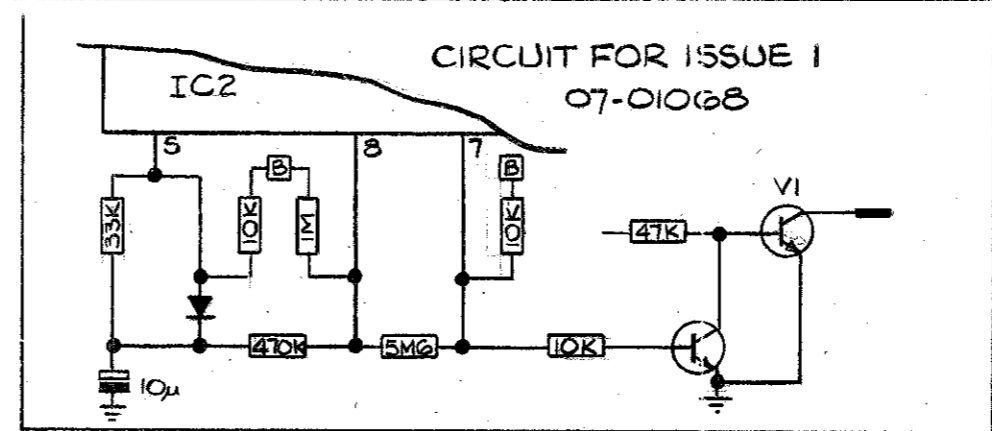
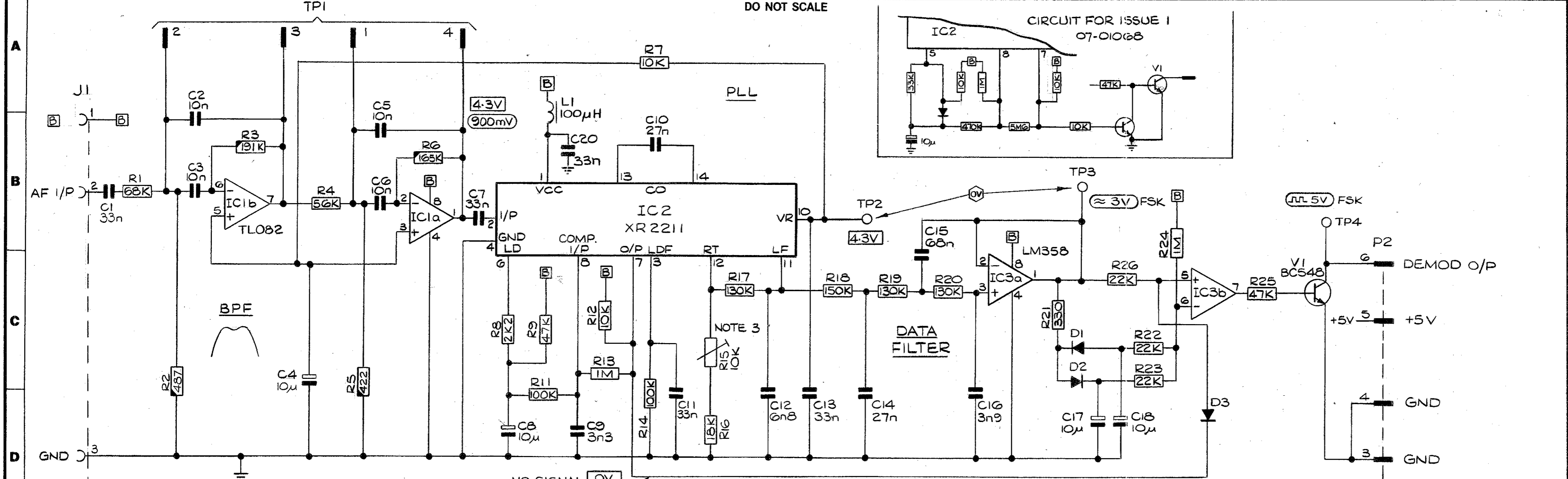
DO NOT SCALE

ISSUE 1
C/R. 21226
10-2-87
ISSUE 2
R26 WAS SOT
R31 " CR25
R25 " 39K
C25 " 47μ
C/R. 21354
14-10-87
ISSUE 3
R16 WAS 270K
C/R. 22276
27/3/90
ISSUE 4
C4 WAS 33n
R5 " 27K
C/R. 22637
27-3-91



PCB. 07-01075
ASSY 08-03273

	DRN.	A.P.J.	DATE	3-9-86	TITLE TWO-TONE DECODER PCB	COPYRIGHT © CODAN 19					
	CHKD.	RCM	10-9-86			DRAWING/DOC NO.					
MATERIAL	APPD.		10-2-87		A2 04-02231	ISS				SHT	
FINISH	TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±									OF	



ONLY THESE COMPONENTS FITTED FOR SD

ALL COMPONENTS ARE FITTED FOR SDE & SDEM

NOTE: DIGI SWITCHES FOR SDEM ARE FITTED TO FRONT PANEL PCB.

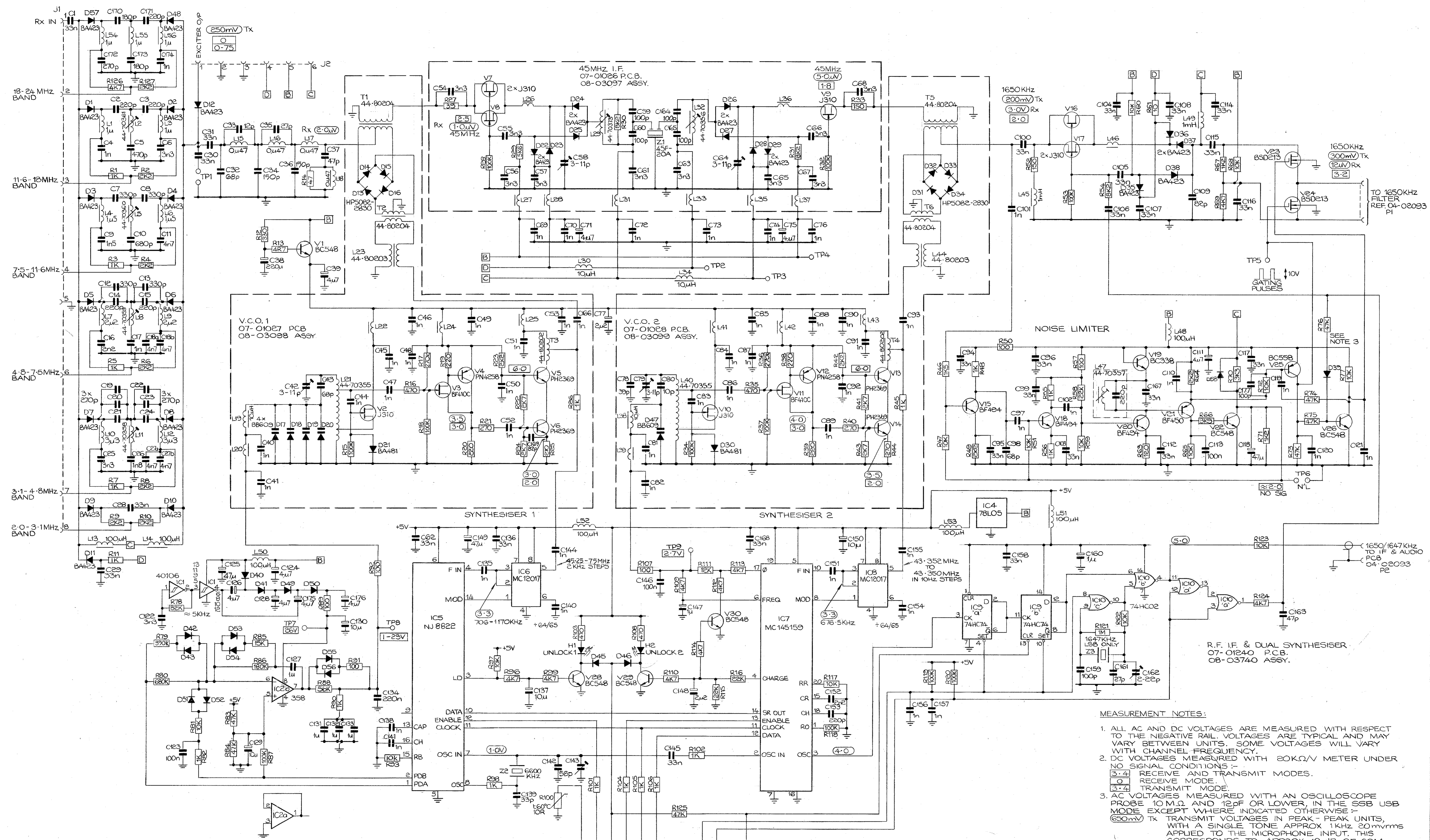
- NOTES:
1. ALL DIODES ARE BAW62 OR EQUIVALENT.
 2. RESISTORS SHOWN \square ARE 1%
 3. Δ DIFFERENTIAL DC VOLTAGE WITH I/P OF 1775Hz AT IVPP AND ADJUST R15 FOR 0V
 4. Δ PP AC VOLTAGE MEASURED WITH I/P OF 1775 Hz AT IVPP.
 5. Δ FSK PPAC VOLTAGE MEASURED WITH FSK I/P AT IVPP
 6. Δ DC VOLTAGE MEASURED WITH NO SIGNAL I/P

ASSY. 08-03300
PCB. 07-01068

B.C.I.R. 21202
ISSUE 1
C/R. 21226
10-2-87
ISSUE 2
L1 & C20
ADDED
C/R. 21339
3/2/87
ISSUE 3
C/R. 21367
22-3-88
ISSUE 4
NOTE ADDED
C/R. 22128
12-9-89
ISSUE 5
C/R. 22812
R1 WAS 50K
R3 WAS 100K
15-4-91

CODAN	SCALE	TITLE	COPYRIGHT © CODAN 1986	
	DRN. APJ.	DATE 3-11-86	SELECTIVE CALL PCB	
MATERIAL	CHKD. <i>Mayo</i>	12-11-86	DRAWING/DOC NO.	
FINISH	APPD. <i>Mayo</i>	10-2-87	A2 04-02250	
	TOLERANCES UNLESS OTHERWISE STATED		ISS	
2 PLACES DEC ±		1 PLACE DEC ±		SHT
ANGULAR ±		1 2 3 4 5		OF

04-02250



ALL DEVICES VIEWED FROM BASE, UNLESS SHOWN OTHERWISE

						ALL IC'S	
J310	BF400	BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62
		BC548	PN4258	BF450	BSD213		BAW62

- NOTES
1. ALL DIODES ARE BAW62 OR EQUIVALENT UNLESS OTHERWISE STATED.
 2. ALL UNMARKED INDUCTORS ARE FERRITE BEADS.
 3. DELETE R76 FOR 85285
 4. COMPONENTS NOT PRESENT :-
R94
R95

MEASUREMENT NOTES:

1. ALL AC AND DC VOLTAGES ARE MEASURED WITH RESPECT TO THE NEGATIVE RAIL. VOLTAGES ARE TYPICAL AND MAY VARY BETWEEN UNITS. SOME VOLTAGES WILL VARY WITH CHANNEL FREQUENCY.
2. DC VOLTAGES MEASURED WITH 20KΩ/V METER UNDER NO SIGNAL CONDITIONS :-
[3.4] RECEIVE AND TRANSMIT MODES.
[1.0] RECEIVE MODE.
[3.4] TRANSMIT MODE.
3. AC VOLTAGES MEASURED WITH AN OSCILLOSCOPE PROBE 10 MΩ AND 12pF OR LOWER, IN THE SSB USB MODE EXCEPT WHERE INDICATED OTHERWISE :-
[50mV] TX TRANSMIT VOLTAGES IN PEAK-PEAK UNITS, WITH A SINGLE TONE APPROX 1KHz 20mVrms APPLIED TO THE MICROPHONE INPUT. THIS CORRESPONDS TO APPROX 10 dB OF COMPRESSION IN THE MICROPHONE AMP. TWO TONE SOURCE WILL GIVE THE SAME PEAK-PEAK MEASUREMENTS.
RECEIVE VOLTAGES EXPRESSED AS EMF FROM A 50Ω SOURCE APPLIED VIA AC COUPLING TO THE POINT INDICATED, WHICH WILL CAUSE THE AVG VOLTAGE AT TPI ON THE AUDIO & 1650 IF. P.C.B. TO DECREASE BY 50mV FROM ITS NO SIGNAL VALUE IN THE RECEIVE MODE.
VOLTAGES IN PEAK-PEAK UNITS IN THE RECEIVE AND TRANSMIT MODES.

ISSUE B
R79 WAS 100K
C17 WAS 50p
C32 WAS 50p
C34 WAS 100p
C36 WAS 100p
C12 WAS 47p
C18 220K
C19 220K
C7-B7 7777

ISSUE C
C17 WAS 50p
C32 WAS 50p
C34 WAS 100p
C36 WAS 100p
C12 WAS 47p
C18 220K
C19 220K
C7-B7 7777

ISSUE D
C160 WAS 33n
C17 221K
C30-B30 7777

ISSUE 2
R37 WAS D47
D50 WAS 33n
C42 WAS 50p
C18 220K
C19 220K
C7-B7 7777

ISSUE 3
C17 221K
R66 DELETED
TP6 VOLTAGE
WAS 2.5V
C18 220K
C19 220K
C7-B7 7777

ISSUE 4
D48 ADDED
C17 221K
C18 220K
C19 220K
C7-B7 7777

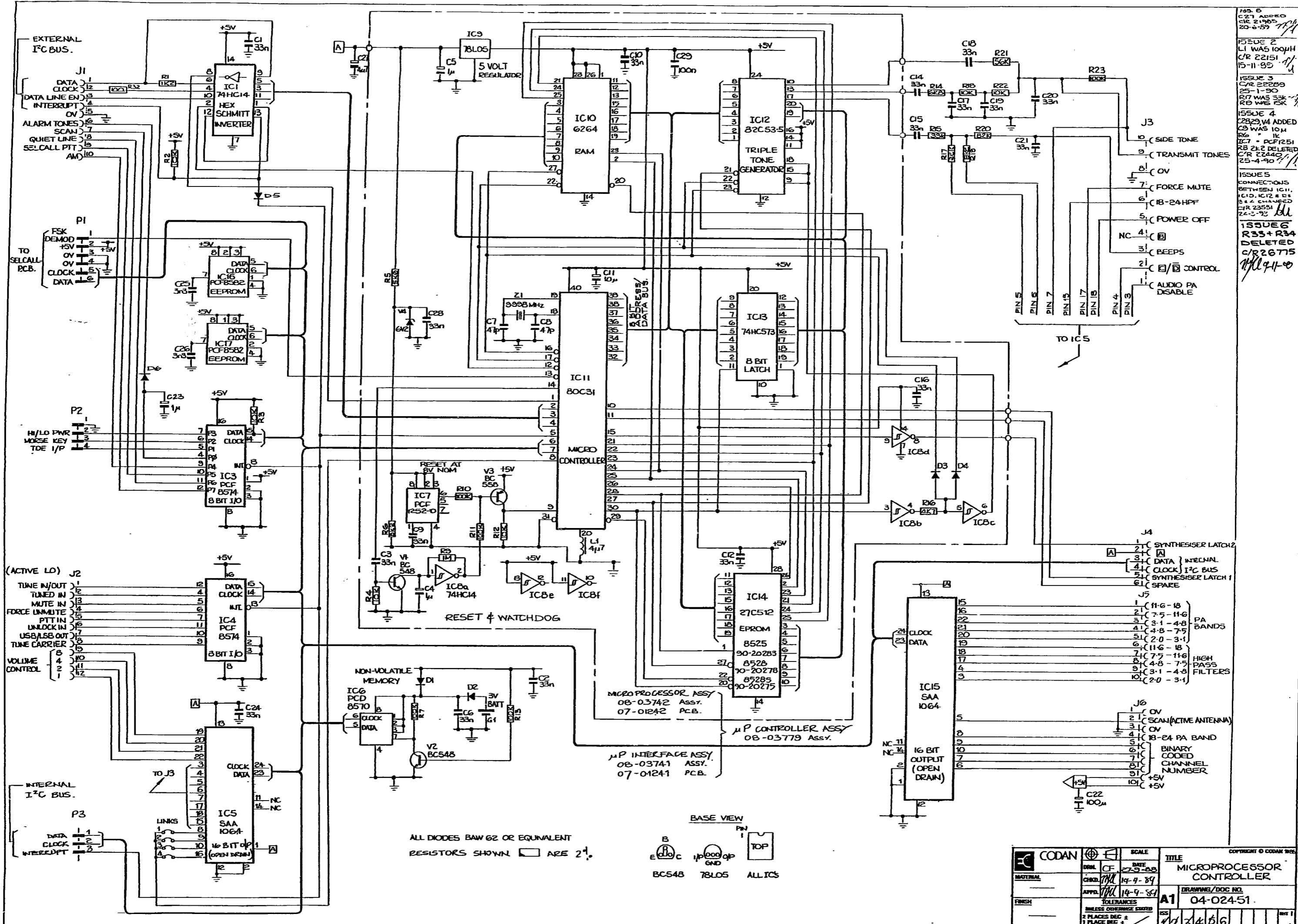
ISSUE 5
R15 WAS 22K
C18 220K
C19 220K
C7-B7 7777

ISSUE 6
R27 WAS 150
C18 220K
C19 220K
C7-B7 7777

ISSUE 7
C18 pin 13
WAS pin 5
C18 220K
C19 220K
C7-B7 7777

CODAN	SCALE	DATE	TITLE
	DRN. CF	19-9-89	RF MIXER & DUAL SYNTHESISER
MATERIAL	CHKD	19-9-89	DRAWING/DOC NO.
	APPD	19-9-89	B 04-02450
FINISH	TOLERANCES UNLESS OTHERWISE STATED	ISS	1 2 3 4 5 6 7
	2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±	SHT	1 of 1

04-02450



ISSUE 2
C27 ADDED
C/R 21905
20-6-89

ISSUE 3
C/R 22208
25-1-90
R7 WAS 53K
R9 WAS 15K

ISSUE 4
C28, V4 ADDED
C9 WAS 10M
R6 " 1K
IC7 - PCF8582
R8 2K2 DELETED
C/R 22440
25-4-90

ISSUE 5
CONNECTIONS
BETWEEN IC11,
IC10, IC12 & IC1
B & C CHANGED
C/R 23551
22-3-92

ISSUE 6
R33 + R34
DELETED
C/R 26715
11/1/94

EXTERNAL I2C BUS.
J1
DATA 1
CLOCK 2
DATA LINE EN 3
INTERRUPT 4
OV 5
ALARM TONES 6
SCAN 7
QUIET LINE 8
SEL CALL PTT 9
AM 10

TO SELCALL PCB.
P1
FSK DEMOD 1
+5V 2
OV 3
CLOCK 4
DATA 5

H/LD PWR MORSE KEY TDE I/P
P2
1
2
3
4

(ACTIVE LD) J2
TUNE IN/OUT 1
TUNED IN 2
MUTE IN 3
FORCE UNMUTE 4
PTT IN 5
UNLOCK IN 6
USB/LSB OUT 7
TUNE CARRIER 8
VOLUME CONTROL 9
10
11
12

INTERNAL I2C BUS.
P3
DATA 1
CLOCK 2
INTERRUPT 3

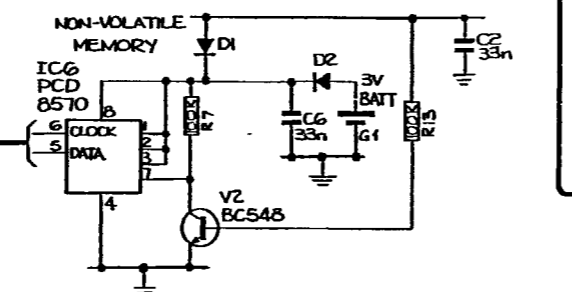
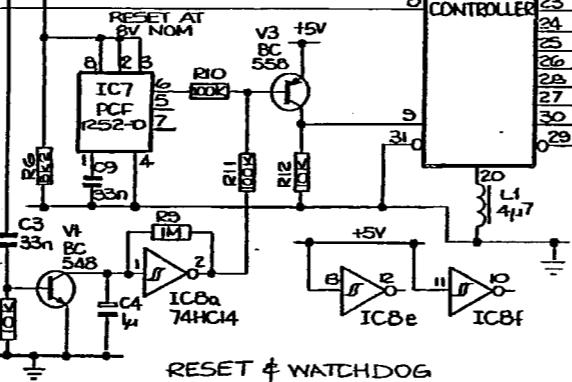
J3
10 (SIDE TONE)
9 (TRANSMIT TONES)
8 (OV)
7 (FORCE MUTE)
6 (18-24 HPF)
5 (POWER OFF)
NC 4
3 (BEEPS)
2 (CONTROL)
1 (AUDIO PA DISABLE)

TO IC5
PIN 5
PIN 6
PIN 7
PIN 15
PIN 17
PIN 18
PIN 19
PIN 4
PIN 3

J4
1 (SYNTHESISER LATCH 2)
2 (DATA) INTERNAL
3 (CLOCK) I2C BUS
4 (SYNTHESISER LATCH 1)
5 (SPARE)
6 (SPARE)

J5
1 (11-6-18)
2 (7-5-11-6)
3 (3-1-4-8)
4 (4-8-7-5)
5 (2-0-3-1)
6 (11-6-18)
7 (7-5-11-6)
8 (4-8-7-5)
9 (3-1-4-8)
10 (2-0-3-1)
HIGH PASS FILTERS

J6
1 (OV)
2 (SCAN (ACTIVE ANTENNA))
3 (OV)
4 (18-24 PA BAND)
5 (BINARY CODED CHANNEL NUMBER)
6
7
8
9
10 (+5V)
11 (+5V)

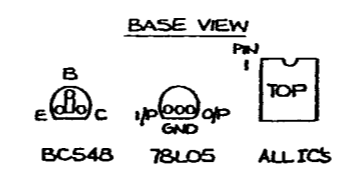


MICROPROCESSOR ASSY
08-03742 ASSY.
07-01242 PCB.

μP CONTROLLER ASSY
08-03779 ASSY.

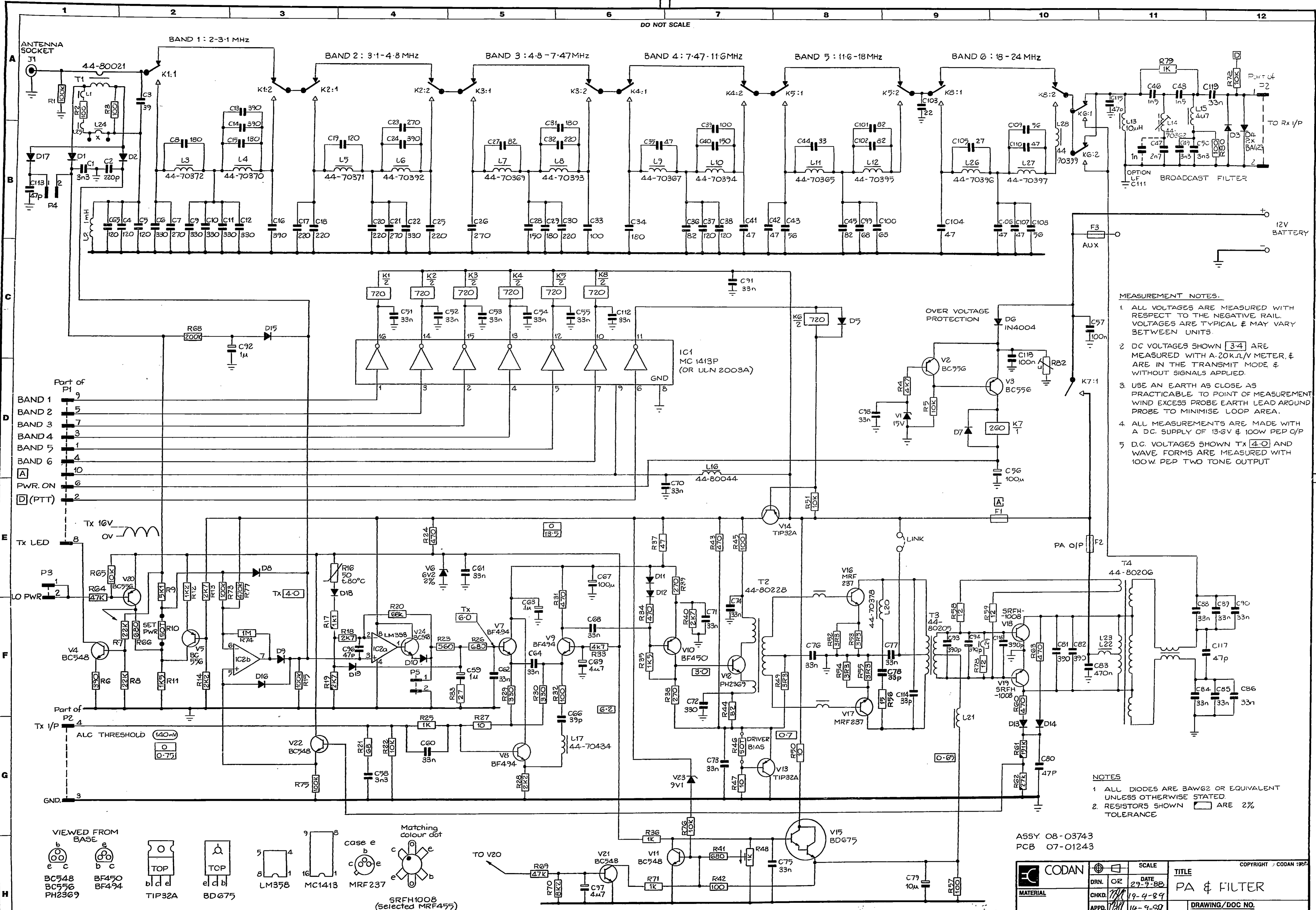
μP INTERFACE ASSY
08-03741 ASSY.
07-01241 PCB.

ALL DIODES BAW 62 OR EQUIVALENT
RESISTORS SHOWN ARE 2%



CODAN	SCALE	DATE	TITLE
	DATE	14-9-89	MICROPROCESSOR CONTROLLER
APPD.	14-9-89	DRAWING/DOC NO.	A1 04-024-51
TOLERANCES		ISS	
UNLESS OTHERWISE SPECIFIED		12 3 4 5 6	
2 PLACES DEC ±		REV 1	
1 PLACE DEC ±		OF 1	
ANGULAR ±			

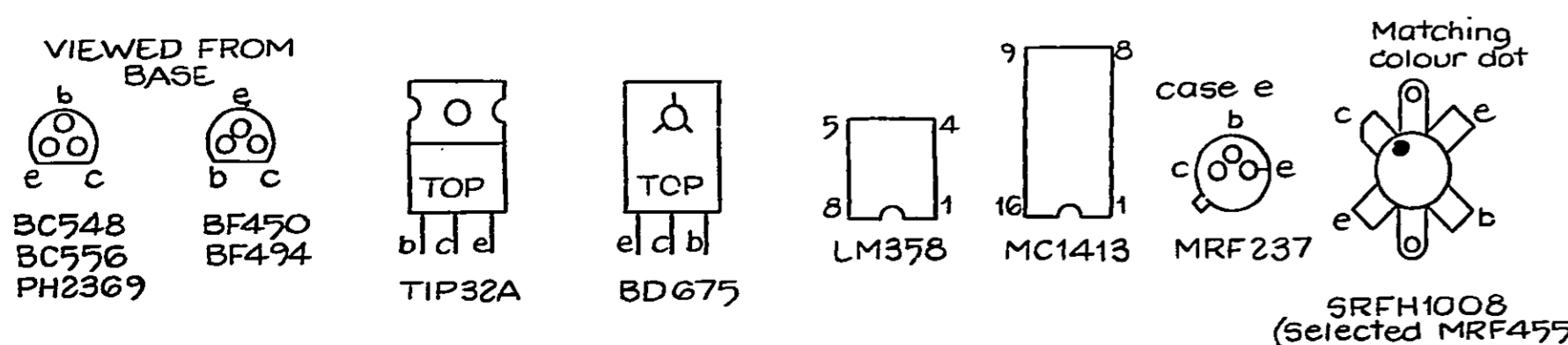
DO NOT SCALE



- MEASUREMENT NOTES.**
1. ALL VOLTAGES ARE MEASURED WITH RESPECT TO THE NEGATIVE RAIL. VOLTAGES ARE TYPICAL & MAY VARY BETWEEN UNITS.
 2. DC VOLTAGES SHOWN [3.4] ARE MEASURED WITH A 20K Ω /V METER, & ARE IN THE TRANSMIT MODE & WITHOUT SIGNALS APPLIED.
 3. USE AN EARTH AS CLOSE AS PRACTICABLE TO POINT OF MEASUREMENT WIND EXCESS PROBE EARTH LEAD AROUND PROBE TO MINIMISE LOOP AREA.
 4. ALL MEASUREMENTS ARE MADE WITH A DC SUPPLY OF 13.6V & 100W PEP C/P
 5. D.C. VOLTAGES SHOWN TX [4.0] AND WAVE FORMS ARE MEASURED WITH 100W PEP TWO TONE OUTPUT

- NOTES**
1. ALL DIODES ARE 1N4148 OR EQUIVALENT UNLESS OTHERWISE STATED.
 2. RESISTORS SHOWN [] ARE 2% TOLERANCE

ASSY 08-03743
PCB 07-01243

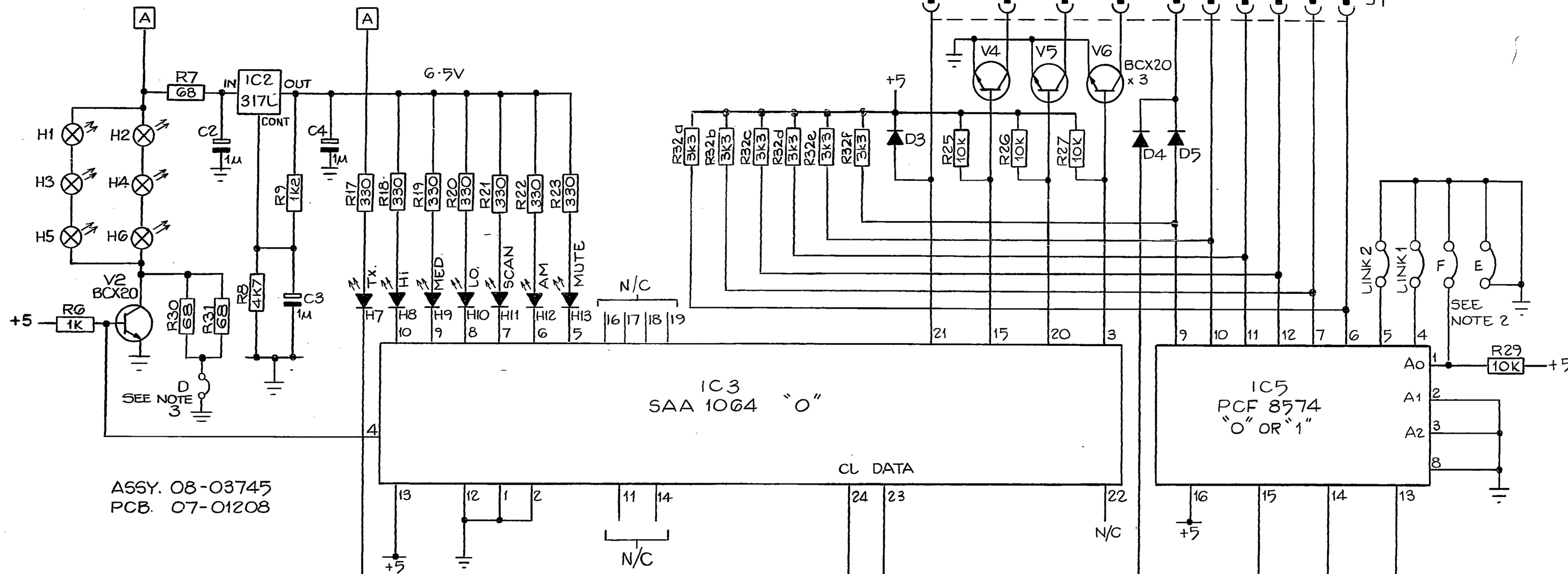


CODAN	SCALE	DATE	TITLE
	DRN. OR	29-9-88	PA & FILTER
MATERIAL	CHKD.	19-9-89	DRAWING/DOC NO.
	APPD.	14-9-89	A1 04-02452
FINISH	TOLERANCES	ISS	SHT 1
	UNLESS OTHERWISE STATED	2 PLACES DEC \pm	OF 1
	1 PLACE DEC \pm		
	ANGULAR \pm		

586
801

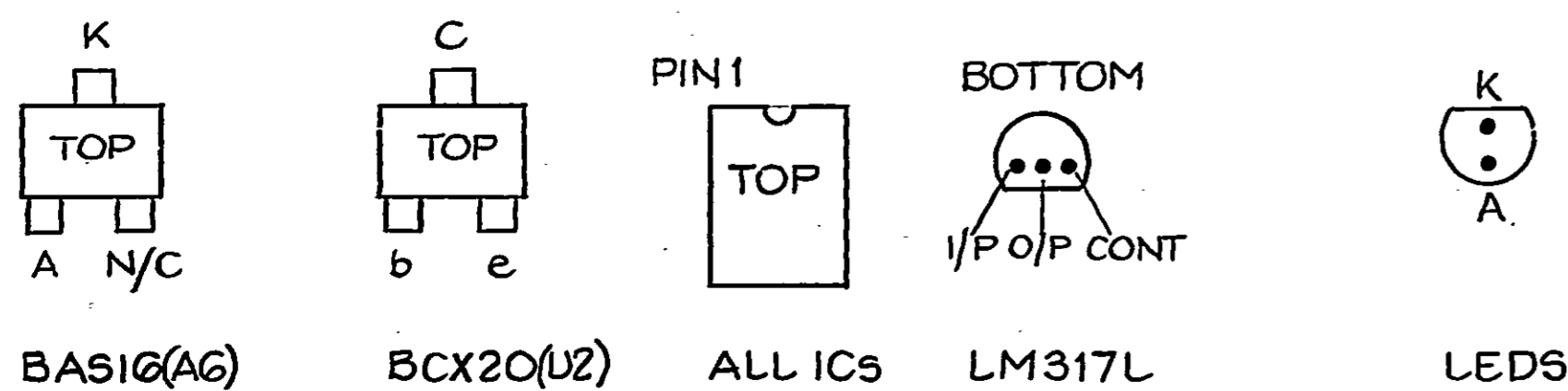
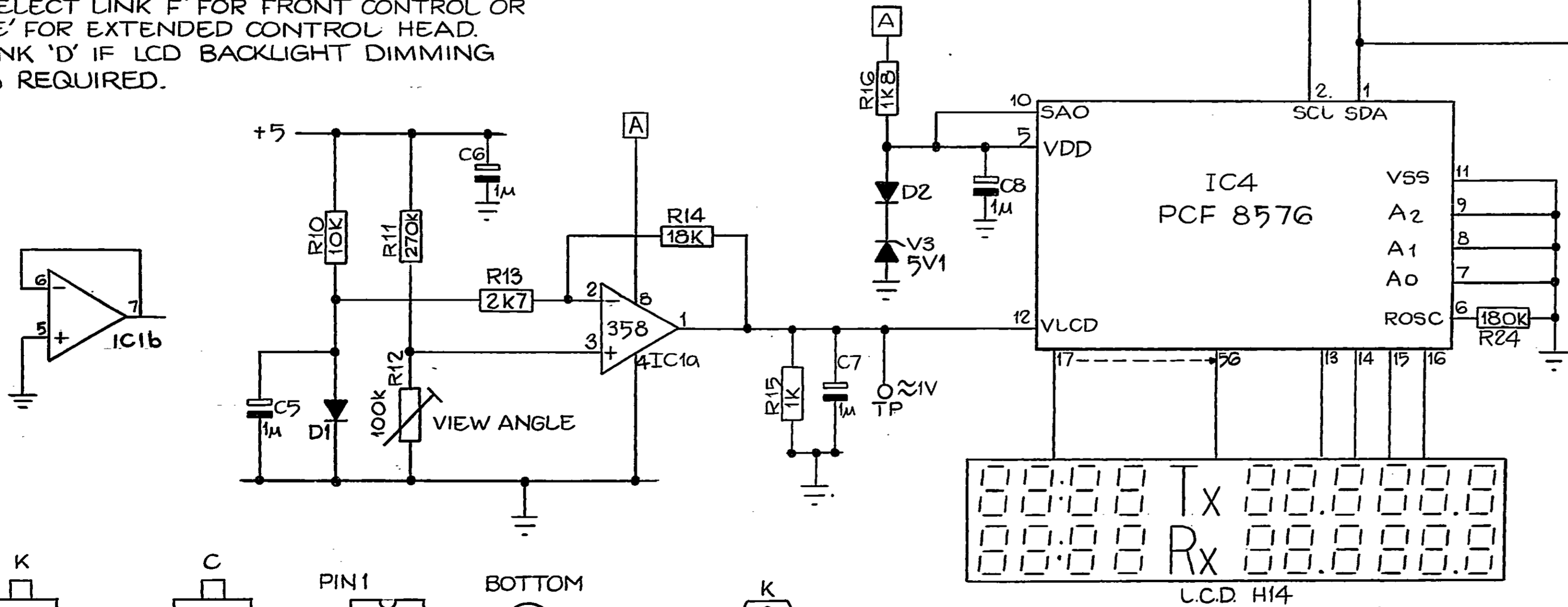
DO NOT SCALE

KEY PAD



ASSY. 08-03745
PCB. 07-01208

- NOTE:-
1. ALL DIODES BAS 10 OR EQUIV.
 2. SELECT LINK 'F' FOR FRONT CONTROL OR 'E' FOR EXTENDED CONTROL HEAD.
 3. LINK 'D' IF LCD BACKLIGHT DIMMING IS REQUIRED.



ISSUE B
R30 ADDED
C/R 21965
27-6-87 *MJL*

ISSUE C
R28 WAS 10K
C/R 22125
14-9-89 *MJL*

ISSUE 2
VI NOW OPTIONAL
C/R 22156
15-11-89 *MJL*

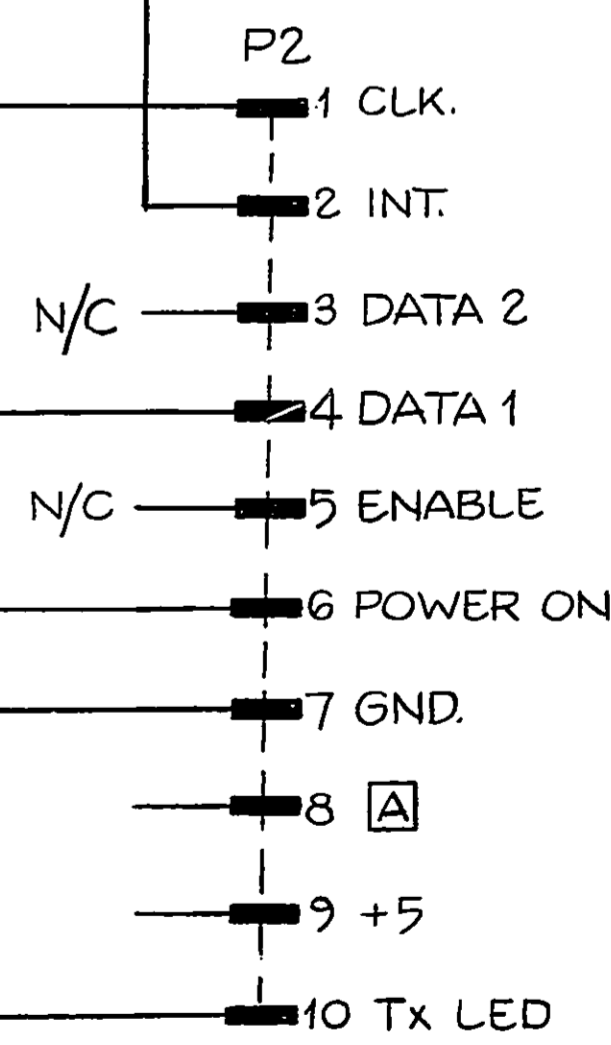
ISSUE 3
LINKS E&F TRANSPOSED
C/R 22253
20-12-85 *MJL*

ISSUE 4
C/R 22289
25.1.90
R9 WAS 1K *MJL*

ISSUE 5
H2 WAS H4
H3 " H2
H4 " H5
H5 " H3
C/R 22903
8-5-91 *MJL*

ISSUE 6
R1, R2, R3, R4,
R5 # C1 DELETED
C/R 23589
4-3-93 *MJL*

ISSUE 7
R11 WAS 390K
IC1 PIN 8 WAS
+5V
C/R 24093
14-11-94 *MJL*



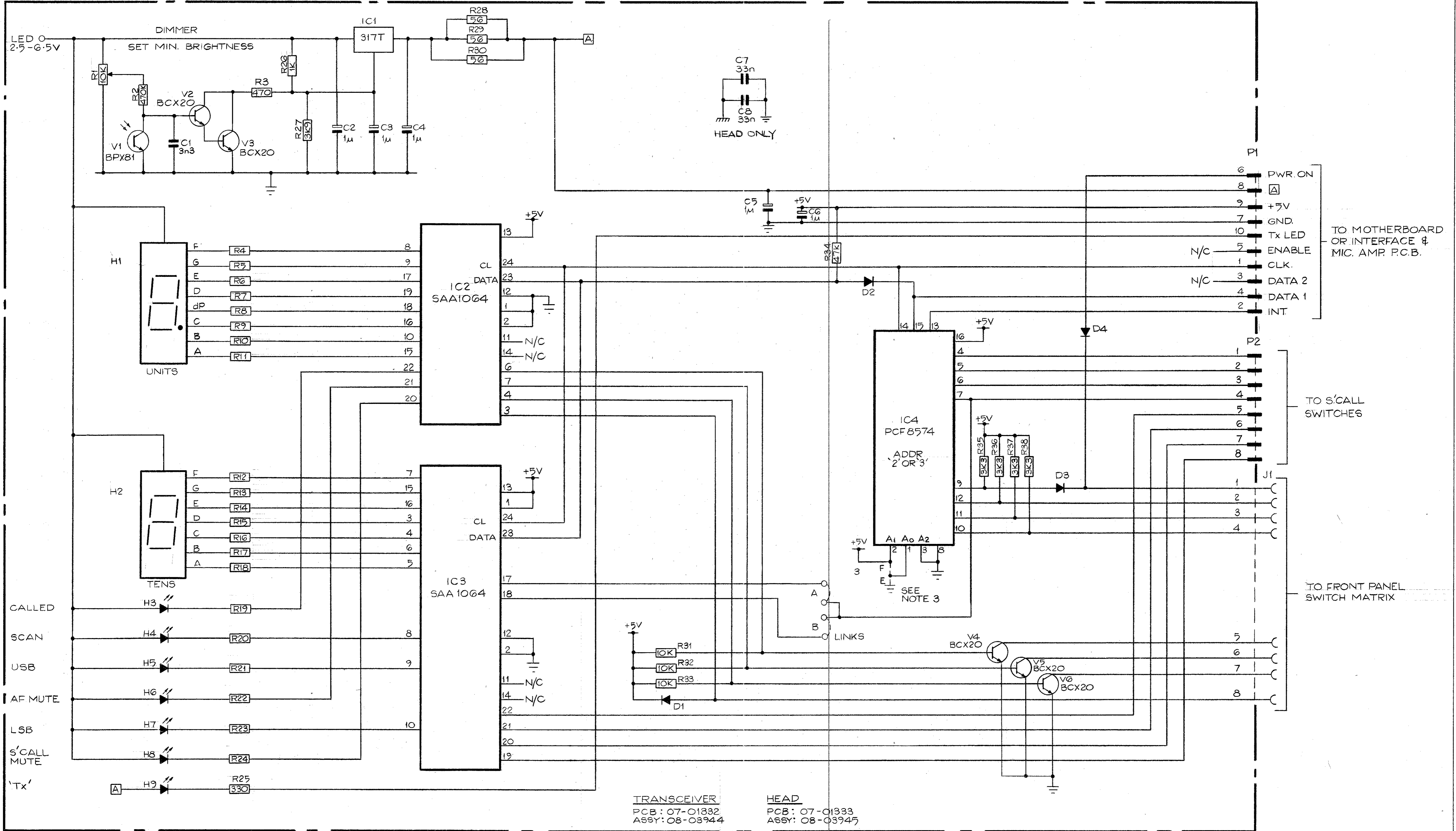
CODAN	DRN.	O.R.	SCALE	TITLE
	CHKD.	19-4-84	4-10-88	DISPLAY BOARD, L.C.D.
MATERIAL	APPD.	14-9-84	DRAWING/DOC NO.	
FINISH	TOLERANCES		A2	04-02454
UNLESS OTHERWISE STATED				ISS
2 PLACES DEC ±				123A567
1 PLACE DEC ±				SHT
ANGULAR ±				OF

DO NOT SCALE

ISSUE 1
R24 WAS 4K7
CIR 22128
14-9-89

ISSUE 2
R28 WAS R25
R29 WAS R24
CIR 22538
27-8-90

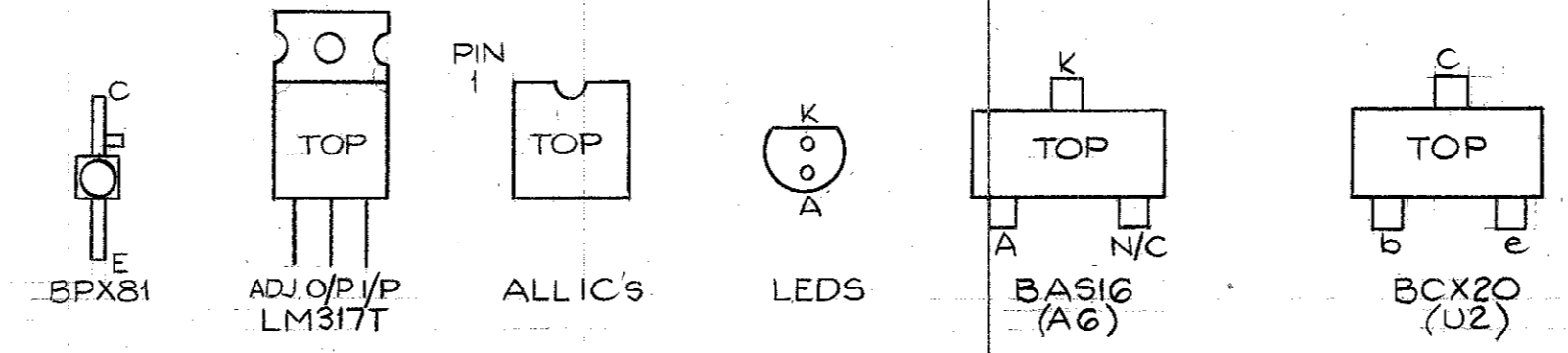
ISSUE 3
C7 AND C8
ADDED
CIR 23377
22-7-92



NOTES:
 1. ALL DIODES BAS 10(A6) UNLESS OTHERWISE STATED.
 2. R4 TO R24 470Ω.
 3. THE F CONNECTION IS MADE FOR TRANSCEIVERS.
 THE E CONNECTION IS MADE FOR CONTROL HEADS.

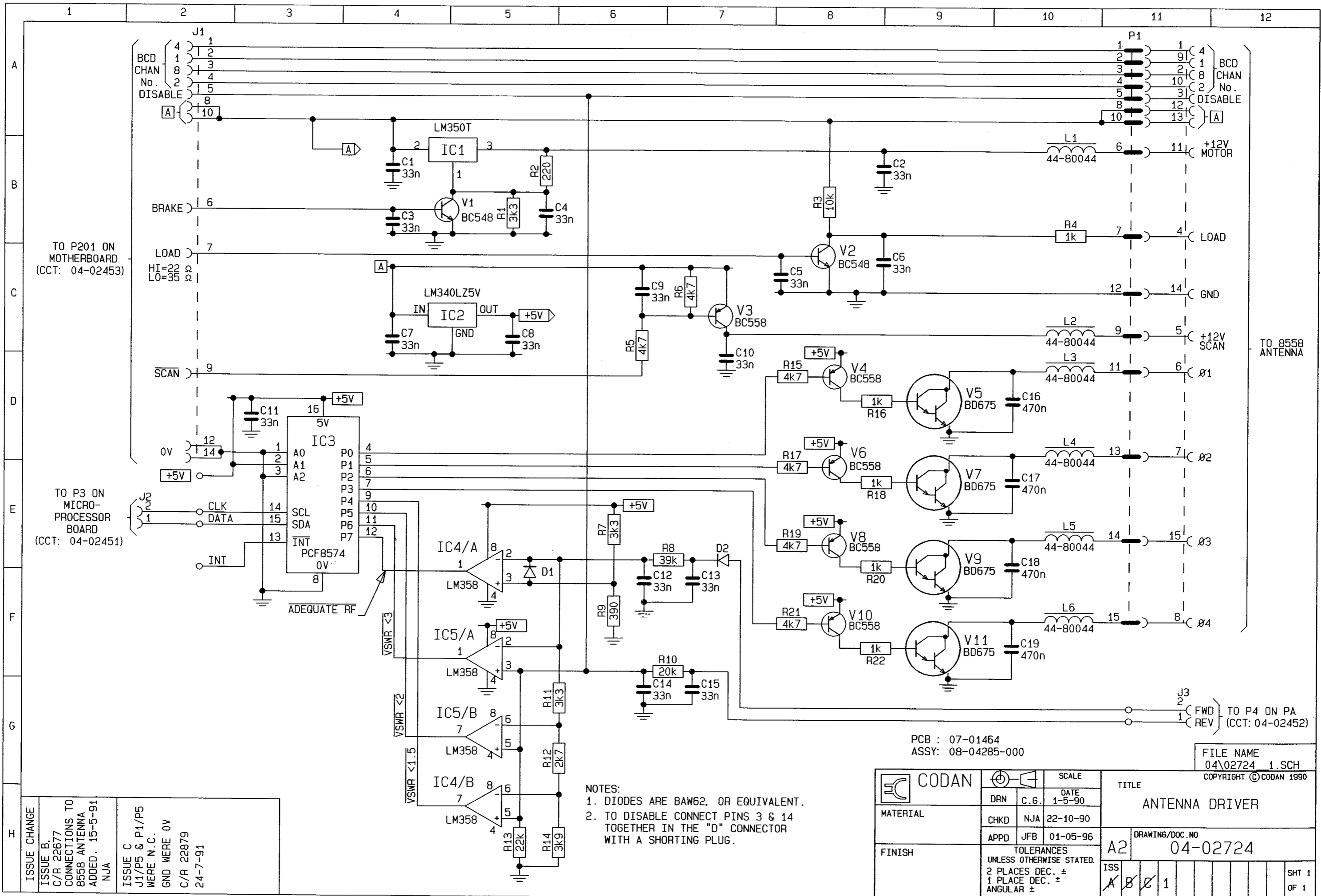
TRANSCEIVER
 PCB: 07-01332
 ASSY: 08-03944

HEAD
 PCB: 07-01333
 ASSY: 08-03945



	SCALE	DATE	TITLE	COPYRIGHT © CODAN 19
	DRN. O.S.	5-6-89	DISPLAY BOARD	
	CHKD. <i>MJ</i>	1-9-89	DRAWING/DOC NO.	
	APPD. <i>MJ</i>	14-9-89	A1 04-02579	
FINISH	TOLERANCES	ISS		SHT
	UNLESS OTHERWISE STATED	1/2/3		OF
	2 PLACES DEC ±			
	1 PLACE DEC ±			
	ANGULAR ±			

566



TO P201 ON MOTHERBOARD (CCT: 04-02453)

TO P3 ON MICRO-PROCESSOR BOARD (CCT: 04-02451)

TO 8558 ANTENNA

TO P4 ON PA (CCT: 04-02452)

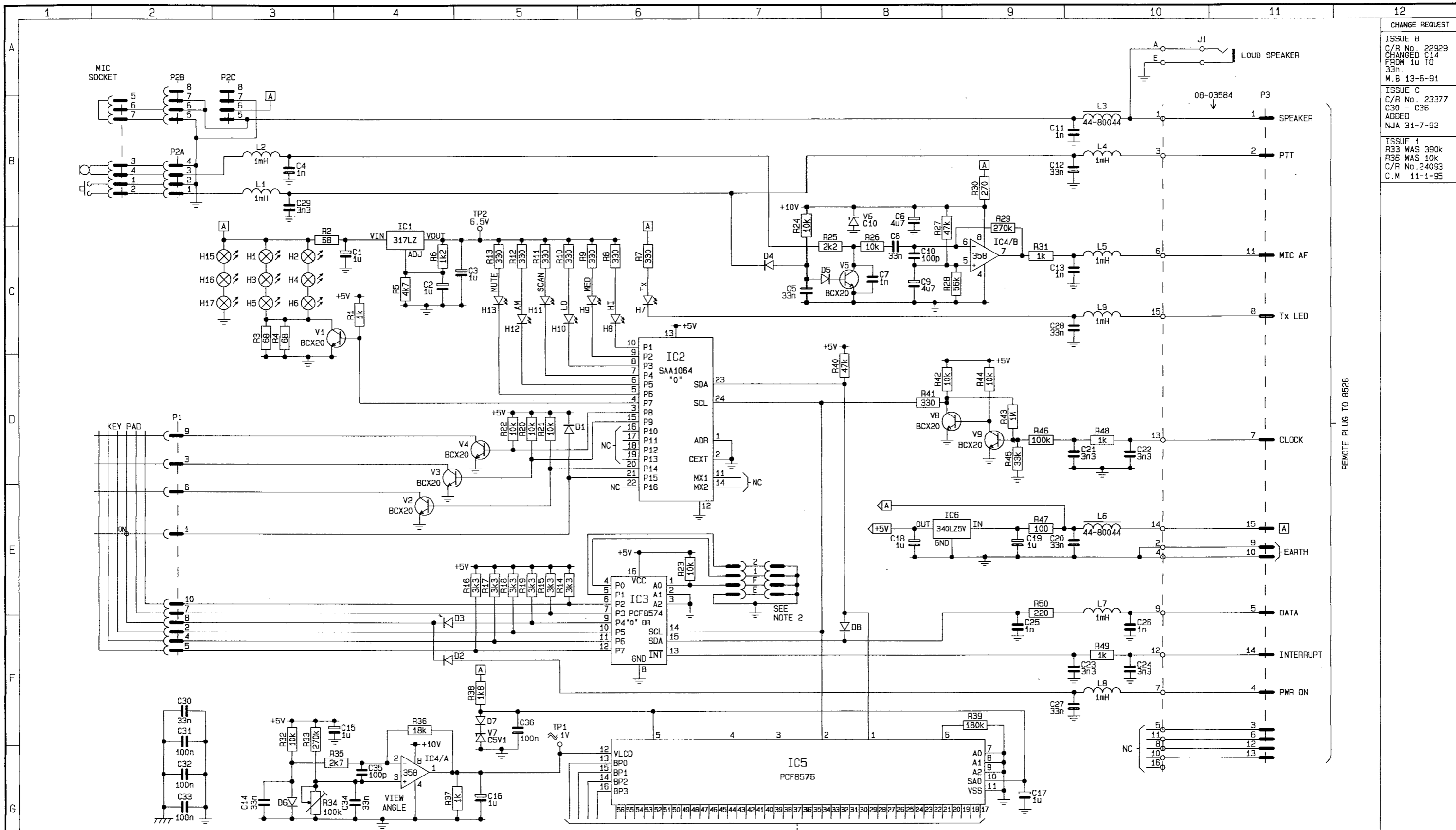
PCB : 07-01464
ASSY: 08-04285-000

FILE NAME
04\02724_1.SCH
COPYRIGHT © CODAN 1990

- NOTES:
1. DIODES ARE BAW62, OR EQUIVALENT.
2. TO DISABLE CONNECT PINS 3 & 14 TOGETHER IN THE "D" CONNECTOR WITH A SHORTING PLUG.

	DRN	C.G.	SCALE	TITLE
	1-5-90			
MATERIAL	CHKD	NJA	DATE	DRAWING/DOC. NO
	APPD	JFB	01-05-96	
FINISH	TOLERANCES UNLESS OTHERWISE STATED.			ISS
	2 PLACES DEC. ± 1 PLACE DEC. ± ANGULAR ±			
				SHT 1 OF 1

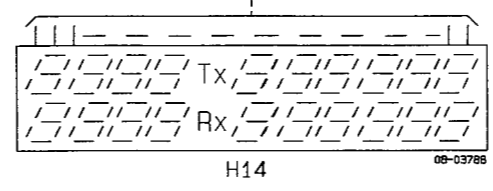
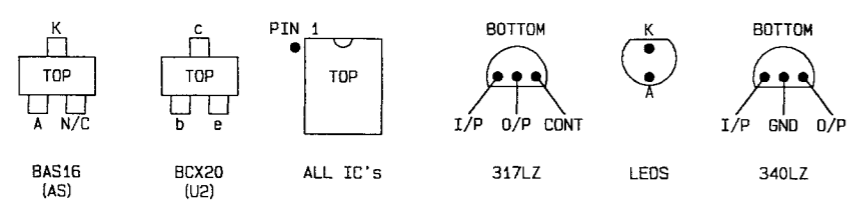
ISSUE CHANGE	ISSUE B.	ISSUE C
C/R 22677	C/R 22677	J1/P5 & P1/P5 WERE N.C.
CONNECTIONS TO 8558 ANTENNA ADDED. 15-5-91 NJA		GND WERE 0V
		C/R 22879
		24-7-91



CHANGE REQUEST
 ISSUE B
 C/R No. 22929
 CHANGED C14
 FROM 1u TO
 33n.
 M.B 13-6-91
 ISSUE C
 C/R No. 23377
 R36 WAS 10K
 C30 - C36
 ADDED
 NJA 31-7-92
 ISSUE 1
 R33 WAS 390K
 R36 WAS 10K
 C/R No. 24093
 C.M 11-1-95

REMOTE PLUG TO 8528

NOTES:
 1. DIODES ARE BAS16, OR EQUIVALENT, UNLESS OTHERWISE STATED.
 2. SELECT LINK 'F' FOR FRONT CONTROL OR 'E' FOR EXTENDED CONTROL HEAD.

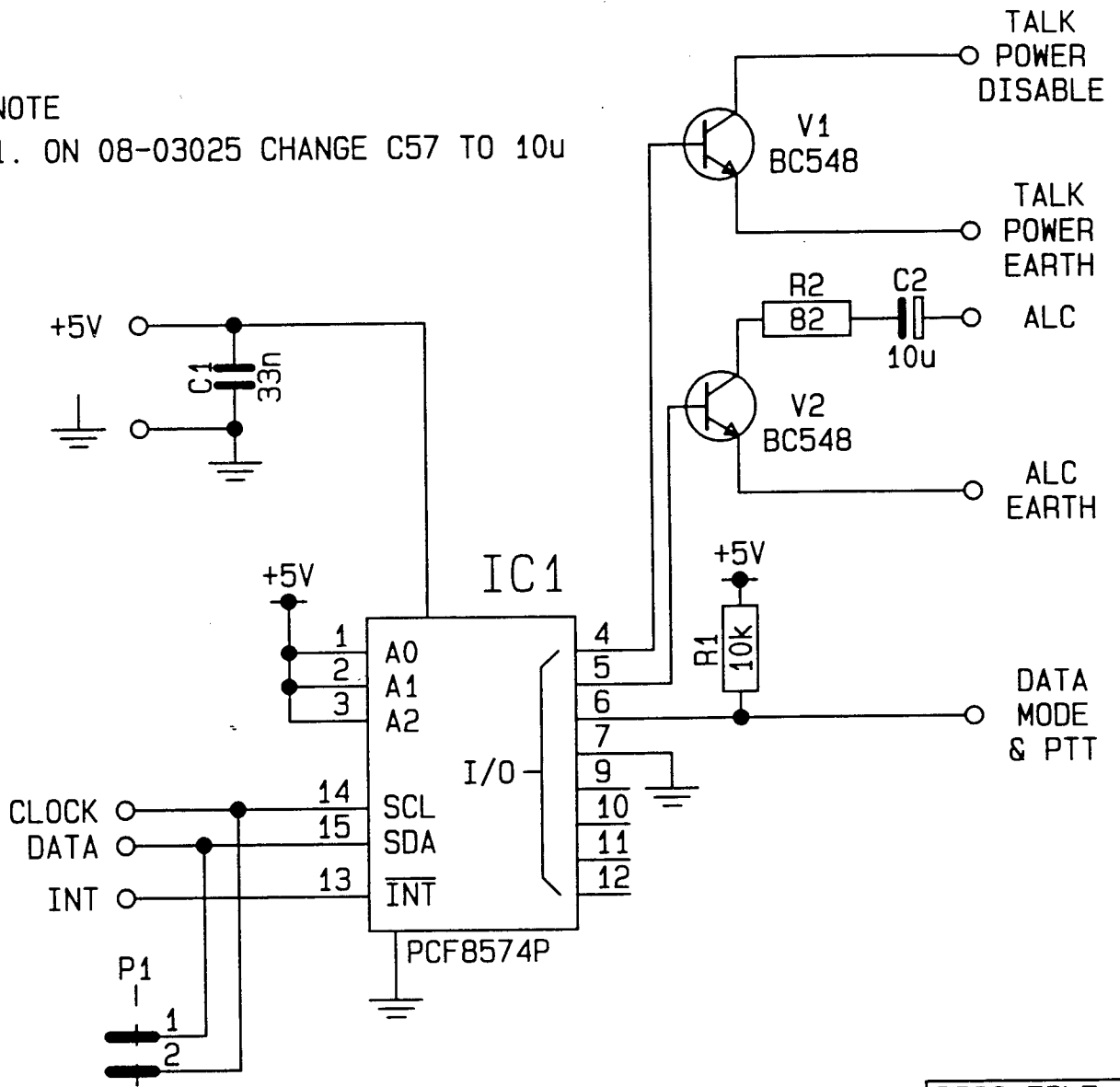


PCB 07-01606
 ASSY 08-04666-001

CODAN	DRN	CG	SCALE	© CODAN PTY. LTD. A.C.N. 007 590 605. 1994
	CHKD	NJA	DATE 11-12-90	
MATERIAL	APPD	C.M	11-1-95	TITLE
FINISH	TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. ± 1 PLACE DEC. ± ANGULAR ±			DISPLAY PCB
DRAWING/DOC. NO. 04-02875				ISS
1				SHT 1 OF 1

NOTE

1. ON 08-03025 CHANGE C57 TO 10u



PCB 07-01667
ASSY 08-05041-001

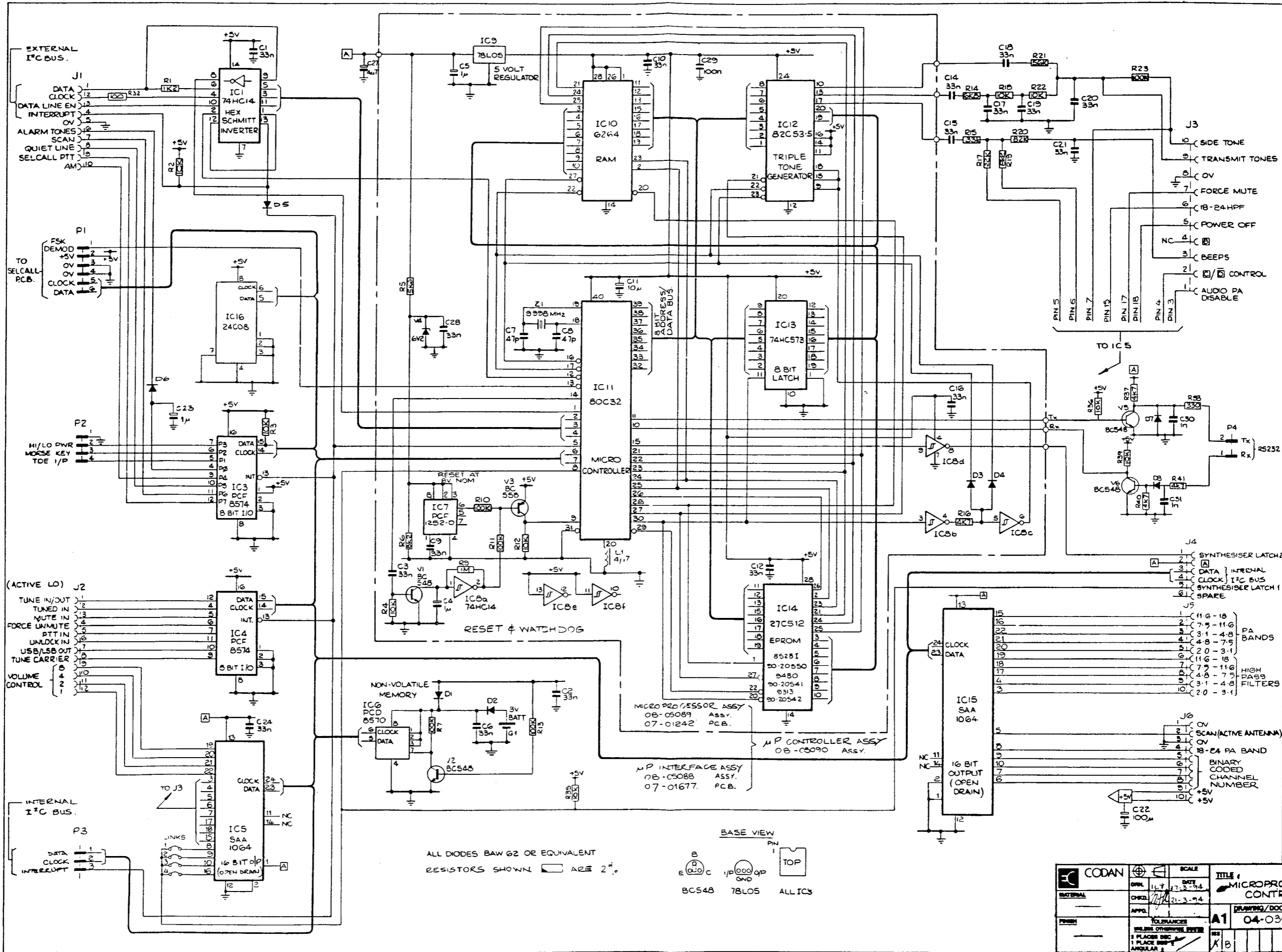
DISC FILE
3018-B.EXE

ISSUE CHANGE

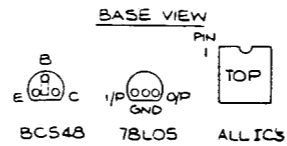
ISSUE B:
C/R 24080
R2 ADDED.
C2 WAS 47u.
P1 2/12/94

			SCALE	COPYRIGHT © CODAN PTY. LTD. A.C.N. 007 590 605	
	DRN	PJL	DATE	TITLE	
MATERIAL	CHKD	NJA	26-11-93	DATA MODE SWITCH	
FINISH	APPD			DRAWING/DOC.NO	
	TOLERANCES UNLESS OTHERWISE STATED			A4	04-03018
2 PLACES DEC. ± 1 PLACE DEC. ± ANGULAR ±			ISS		SHT 1
			A	B	OF 1

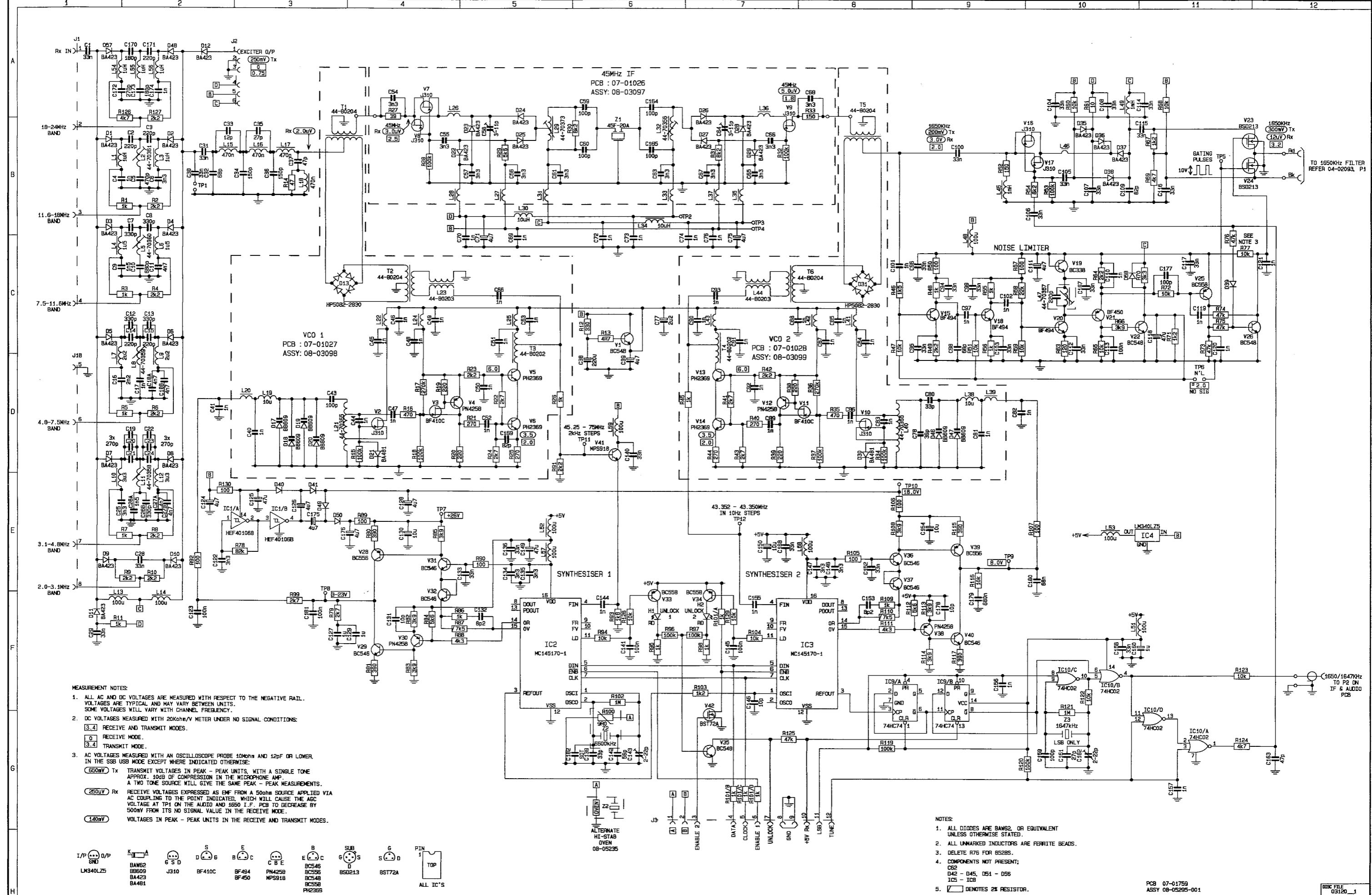
ISS. B
IC14 DETAILS
CHANGED
CIR 24211/11
19-3-95



ALL DIODES BAW 62 OR EQUIVALENT
RESISTORS SHOWN ARE 2%

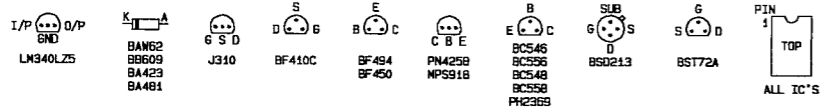


CODAN	SCALE	TITLE MICROPROCESSOR CONTROLLER	DRAWING/DOC NO. 04-03031
	DATE 17.3.94		
APPROV.	21.3.94	A1	
TOLERANCES		UNLESS OTHERWISE SPECIFIED	
1 PLACE DEC		1 PLACE IMP	
ANGULAR		ANGULAR	



MEASUREMENT NOTES:

- ALL AC AND DC VOLTAGES ARE MEASURED WITH RESPECT TO THE NEGATIVE RAIL. VOLTAGES ARE TYPICAL AND MAY VARY BETWEEN UNITS. SOME VOLTAGES WILL VARY WITH CHANNEL FREQUENCY.
- DC VOLTAGES MEASURED WITH 20Kohm/V METER UNDER NO SIGNAL CONDITIONS.
 - 3.4 RECEIVE AND TRANSMIT MODES.
 - 0 RECEIVE MODE.
 - 3.4 TRANSMIT MODE.
- AC VOLTAGES MEASURED WITH AN OSCILLOSCOPE PROBE 10Mohm AND 12pF OR LOWER, IN THE SSB USB MODE EXCEPT WHERE INDICATED OTHERWISE:
 - 650mV Tx TRANSMIT VOLTAGES IN PEAK - PEAK UNITS, WITH A SINGLE TONE APPROX. 10dB OF COMPRESSION IN THE MICROPHONE AMP. A TWO TONE SOURCE WILL GIVE THE SAME PEAK - PEAK MEASUREMENTS.
 - 250uV Rx RECEIVE VOLTAGES EXPRESSED AS EMF FROM A 500Hz SOURCE APPLIED VIA AC COUPLING TO THE POINT INDICATED, WHICH WILL CAUSE THE AGC VOLTAGE AT TP1 ON THE AUDIO AND 1650 I.F. PCB TO DECREASE BY 500mV FROM ITS NO SIGNAL VALUE IN THE RECEIVE MODE.
 - 140mV VOLTAGES IN PEAK - PEAK UNITS IN THE RECEIVE AND TRANSMIT MODES.



ALL DEVICES VIEWED FROM BASE, UNLESS SHOWN OTHERWISE.

- NOTES:**
- ALL DIODES ARE BAW22, OR EQUIVALENT UNLESS OTHERWISE STATED.
 - ALL UNMARKED INDUCTORS ARE FERRITE BEADS.
 - DELETE R76 FOR BS28S.
 - COMPONENTS NOT PRESENT:
 - C82
 - D42 - D45, D51 - D55
 - IC5 - IC8
 - DENOTES 2% RESISTOR.

PCB 07-01759
ASSY 08-05295-001

SCALE: 1:1
DATE: 11-2-96
DRAWN: MJA
CHECKED: MJA
APPD: MJA
TOLERANCES: UNLESS OTHERWISE STATED
2 PLACES DEC. #
RACES DEC. #
ANGULAR ±

FILE: 04-03120_1

CODAN
RF MIXER & DUAL SYNTHESISER PCB
A0
A1

ISS: A1
SHT 1 OF 1

ISSUE CHANGE
ISSUE 1:
CR 28020
WERE 270K
8-5-87 MJS

ISSUE 9
C54 WAS 100p
C57 ADDED
C/R 22496
20-8-90 NJA

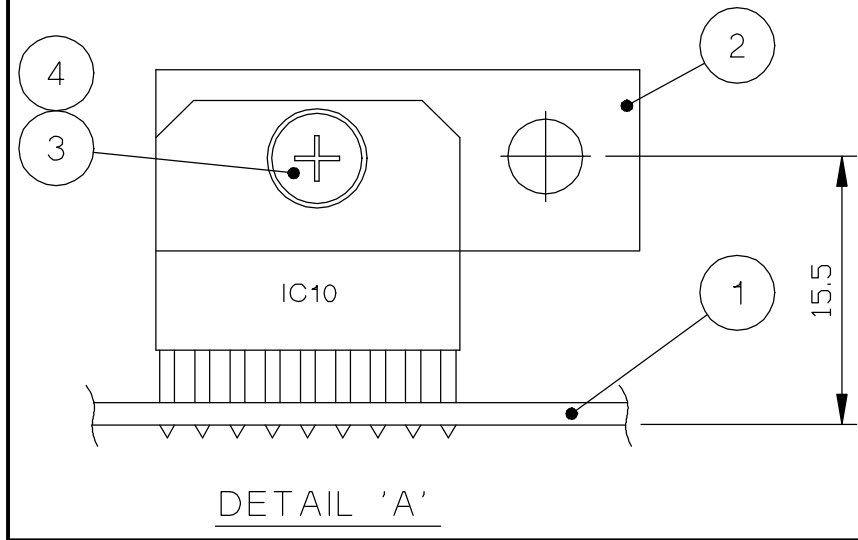
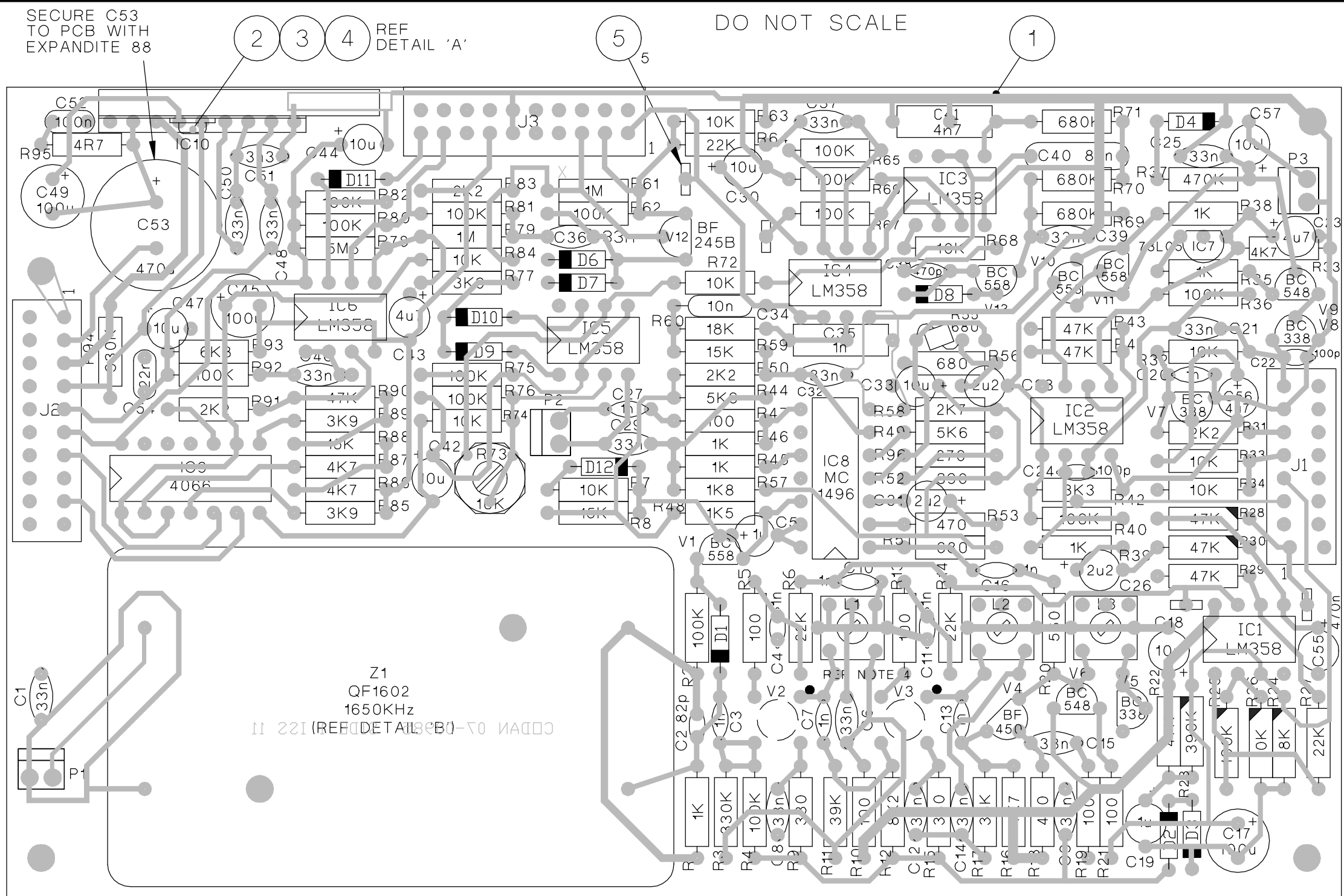
ISSUE 10
C55 WAS 100n
R28 & R30 WERE
68K
C/R 22538
29-8-90 NJA

ISSUE 11
R52 WAS 470
R96 WAS 330
C/R 23587
4-3-93 NJA

ISSUE 12
R97 ADDED
C/R 23689
29-9-93 NJA

ISSUE 13
P3 ADDED
C/R 24314
2-8-95
C57 WAS 1u
C/R 24319
7-8-95 NJA

ISSUE 14
V2 & V3 WERE
3SK85
C/R 24597
10-5-96 NJA



- NOTES:
- 1. ALL DIODES BAW62 OR EQUIVALENT.
 - 2. RESISTORS SHOWN ARE 2%
 - 3. CUT PINS OFF FILTER 4mm LONG FROM PCB AFTER SOLDERING.
 - 4. L1, L2 & L3 ARE 44-70357

B. 21096
ISSUE 2
C56 ADDED
C/R 21271
V7 WAS BC548
C/R 21257
8-4-87 NJA

ISSUE 3
ITEM 3 ADDED
BETWEEN Z1
& PCB
C/R 21289
10-6-87 NJA

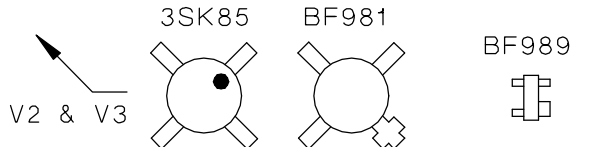
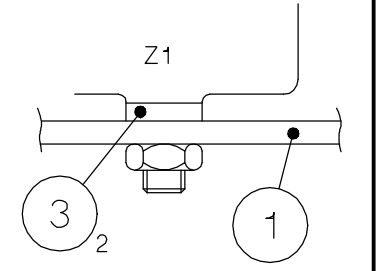
ISSUE 4
PCB WAS ISS. 4
R54 DELETED
R52 WAS 1K
R55 WAS 1K3
C/R 21339
29-9-87

ISSUE 5
R55 680 WAS
R52 820
C/R 21414
11-2-88 NJA

ISSUE 6
R36 WAS 47K
R95 ADDED
C/R 21621
22-9-88 NJA

ISSUE 7
3SK85 WAS BF981
(V2 & V3)
C/R 21999
22-6-89 NJA

ISSUE 8
C25 WAS 1u
D5 DELETED
R37 DET ADDED
C/R 22442
26-4-90 NJA

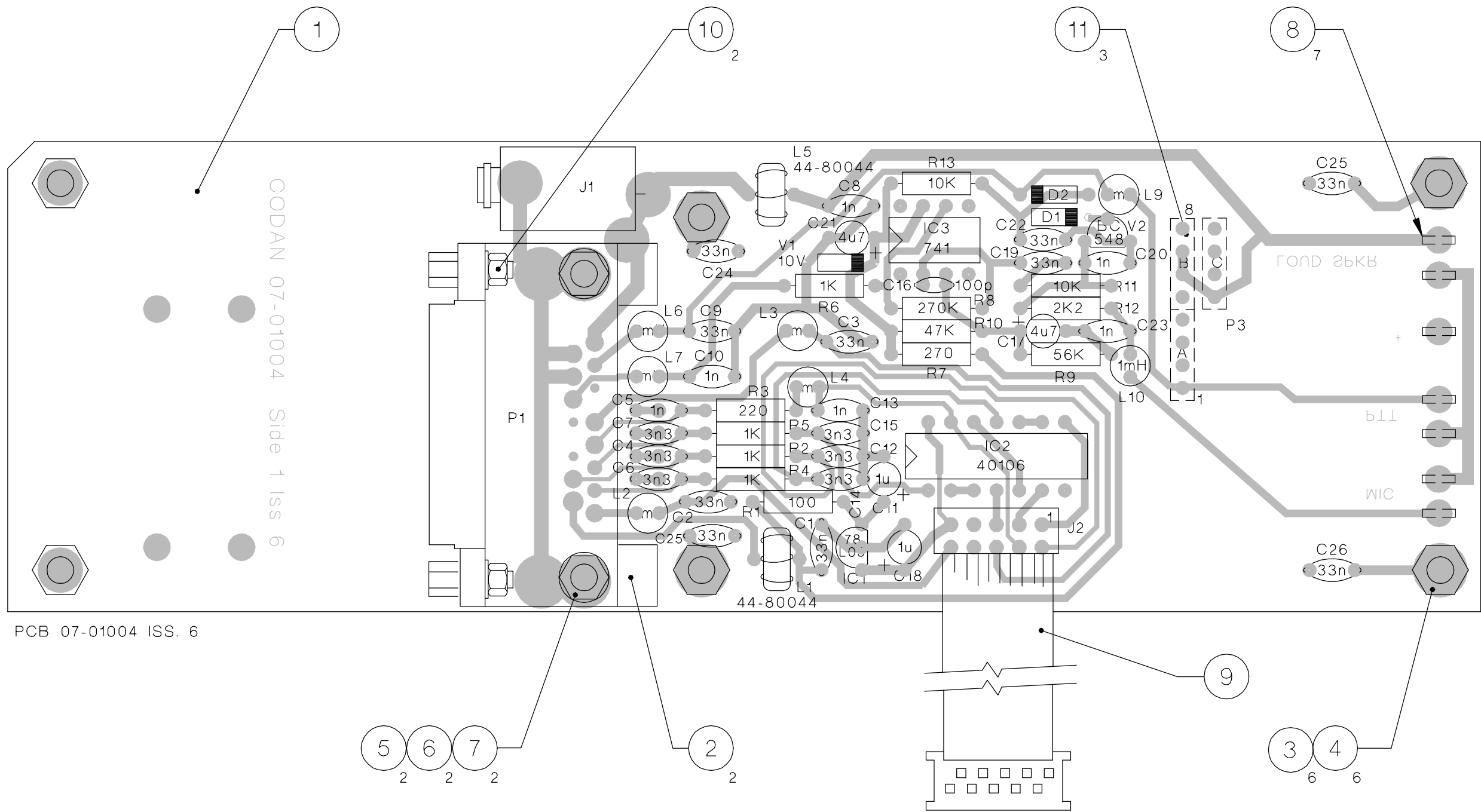


FILE NAME
08\03025_14.DWG

	SCALE 2:1		© CODAN PTY LTD, A.C.N. 007 590 605: 1997	
	DRN	MB	TITLE AUDIO & IF 1650 KHz PCB	
MATERIAL	CHKD	NJA	DRAWING/DOC NO. 08-03025	
FINISH	APPD	NJA	A3	
		TOLERANCES UNLESS OTHERWISE STATED		ISS 11 12 13 14 REDRAWN
		2 PLACES DEC.		
		1 PLACE DEC. ±0.5		
		0 PLACE DEC. ±1		
		ANGULAR ±2°		SHT. 1 OF 1

DO NOT SCALE

ITEMS SHOWN DOTTED FITTED TO UNDERSIDE OF PCB.



B. 21080

ISSUE 2
ITEMS 6 & 7
WERE 2 OFF
ITEM 10 ADDED
C/R 21434
24-3-88 NJA

ISSUE 3
P3 ADDED
PHONES & R14
DELETED
C/R 21857
10-1-89 NJA

ISSUE 4
ITEM 7 DELETED
C/R 21919
30-3-89 NJA

ISSUE 5
5 STAKES ADDED
PCB WAS ISS. 4
C/R 22156
16-11-89 NJA

ISSUE 6
ITEM 10 WAS
SCREW LOCK ASSY
C/R 22503
QTY ITEM 11 WAS 2
C/R 22530
23-8-90 NJA

ISSUE 7
4 x ITEM 8
DELETED
C/R 23004
9-8-91 NJA

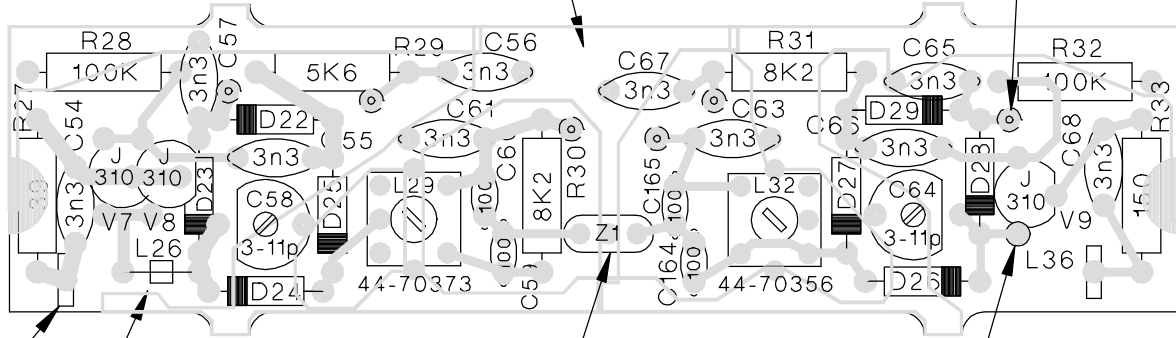
ISSUE 8
PCB WAS ISS 5
C24,C25,C26 & C27
ADDED
C/R 23377
24-7-92 NJA

FILE NAME
08\03039_8.DWG

	SCALE 2:1		© CODAN PTY LTD, A.C.N. 007 590 605: 1997																	
	DRN	APJ	TITLE MIC AMP & INTERFACE BOARD																	
	CHKD	NJA	DRAWING/DOC NO. 08-03039																	
	APPD	NJA	ISS																	
MATERIAL		TOLERANCES UNLESS OTHERWISE STATED		<table border="1"> <tr> <td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td> </tr> <tr> <td>/</td><td>/</td><td>/</td><td>/</td><td>/</td><td>/</td><td>/</td><td>/</td> </tr> </table>	1	2	3	4	5	6	7	8	/	/	/	/	/	/	/	/
1	2	3	4		5	6	7	8												
/	/	/	/	/	/	/	/													
FINISH		2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR		SHT. 1 OF 1																
		DATE 4-7-86 18-8-86 30-10-86		REDRAWN																

DO NOT SCALE

PCB 07-01026 ISS. 2



25
2

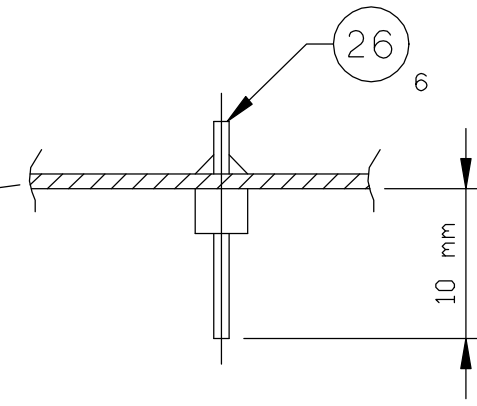
4BI BEAD ON
22 SWG TCW

4BI BEAD ON
LEG ON COMP
SIDE

22

SOLDER SEAMS
ON BOTH SIDES
OF SHIELDS

24



MOUNT 4BI BEAD
UNDERSIDE OF PCB
GLUED WITH EXPANDITE 88
ON ALL POINTS MARKED
(⊙) = 6 OFF

B. 21080
ISSUE 2
ITEM No'S CHANGED
RTV ADDED
C/R 21257
9-4-87 NJA
ISSUE 3
SCREW BLOCK
DELETED
C/R 21289
10-6-87 NJA
ISSUE 4
NOTE ADDED
RE-SOLDER SEAMS
C/R 21391
15-2-88 NJA
ISSUE 5
R27 WAS 150
C/R 23558
15-2-93 NJA

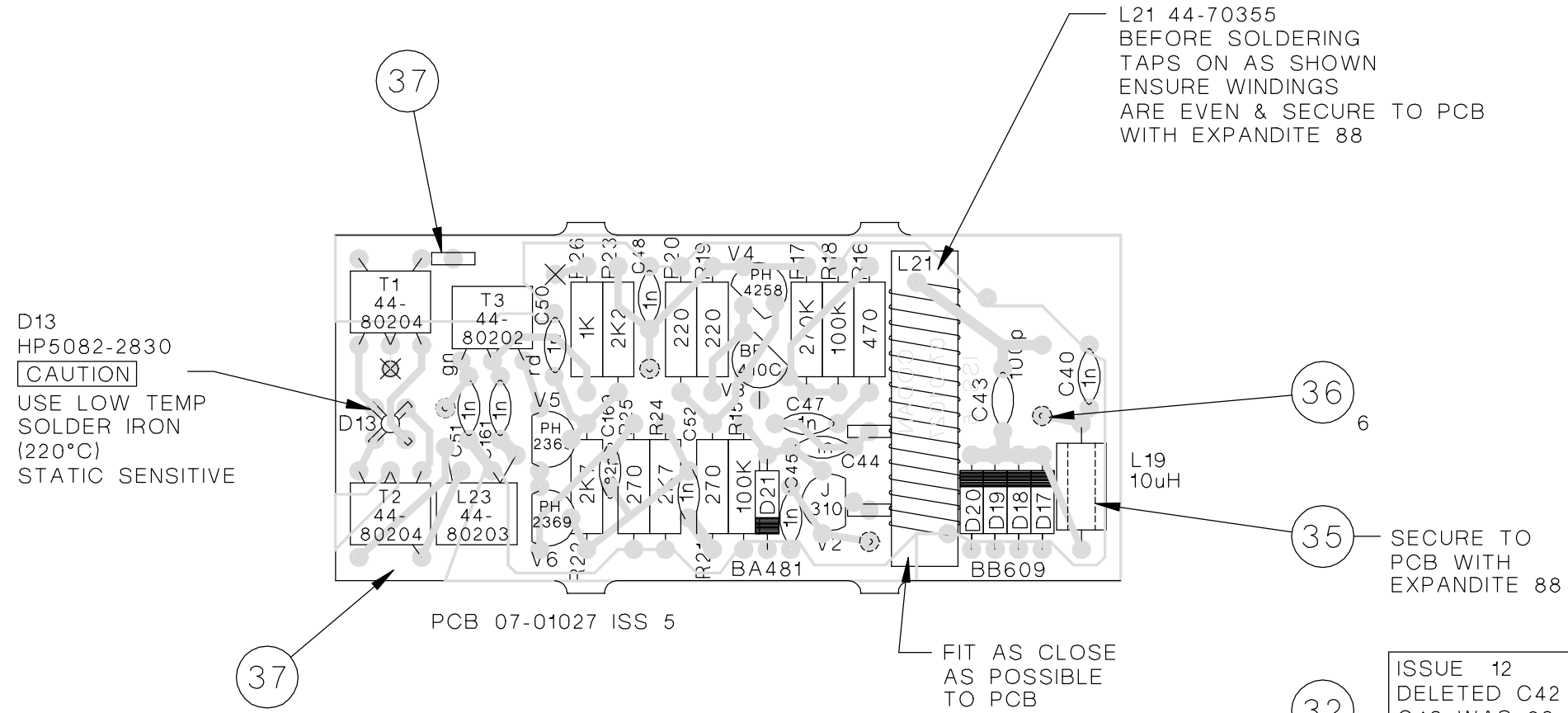
NOTES;

1. ALL DIODES BA423
2. 44-70373 - bl, rd, bl
44-70356 - bl, bk, bl
3. SECURE L26 & L36 TO
PCB USING EXPANDITE 88

FILE NAME
08\03097__5.DWG

			SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE 45 MHz I.F.	
	DRN	APJ	DATE 4-7-86		
MATERIAL	CHKD	NJA	18-8-86		
	APPD	NJA	30-10-86	DRAWING/DOC NO.	
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A3	08-03097
	2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR			ISS	SHT. 1 OF 1
	1	2	3	4	5 REDRAWN

DO NOT SCALE

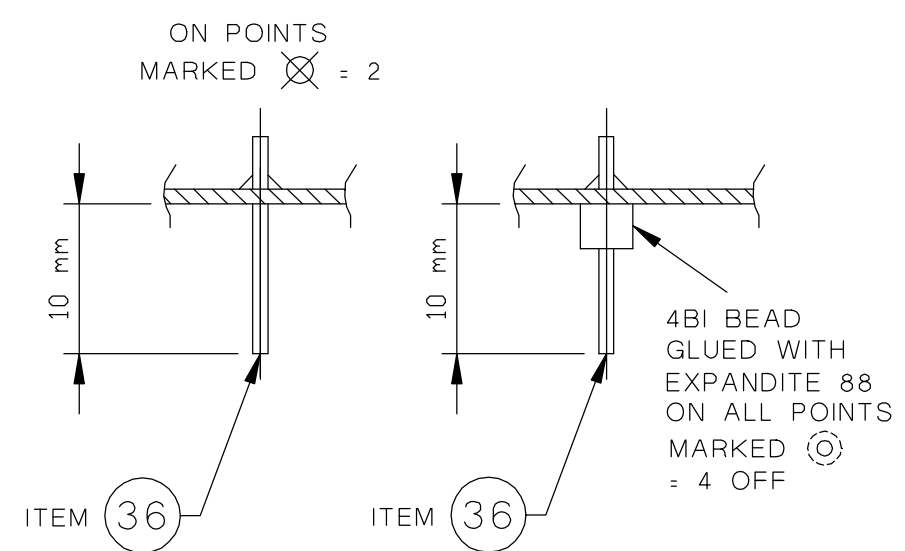
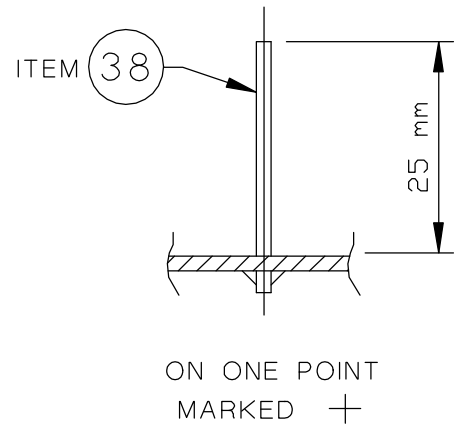


D13
HP5082-2830
CAUTION
USE LOW TEMP
SOLDER IRON
(220°C)
STATIC SENSITIVE

NOTE:
1. V2 IS 23-20006
2. 44-80202 - ye, bk, ye
44-80203 - ye, rd, ye
44-80204 - ye, gn, ye
3. SECURE T1, T2, T3
& L19 TO PCB WITH
EXPANDITE 88

SOLDER SEAMS
ON BOTH SIDES
OF SHIELDS

WARNING
THIS ASSEMBLY CONTAINS
ELECTRO-STATIC SENSITIVE DEVICES



B. 21080
ISSUE 2 C/R 21257 7-4-87 NJA
ISSUE 3 SCREW BLOCK DELETED C/R 21289 10-6-87 NJA
ISSUE 4 C42 CHANGED C/R 21374 4-12-87 NJA
ISSUE 5 NOTE ADDED RE- SOLDER SEAMS C/R 21391 15-2-88 NJA
ISSUE 6 V2 WAS J310 C/R 21600 19-8-88 NJA
ISSUE 7 C169 ADDED C/R 21621 22-9-88 NJA
ISSUE 8 V2 CHANGED TO J310 C/R 21836 20-12-88 NJA
ISSUE 9 C169 DELETED C/R 21878 2-3-89 NJA
ISSUE 10 C169 ADDED R17 WAS 390K R19 WAS 180 R26 WAS 470 C43 WAS 56p C/R 21908 28-3-89 NJA
ISSUE 11 C42 CHANGED C/R 24423 15-11-95 CM
ISSUE 12 DELETED C42 C43 WAS 68p C/R 24741 28-11-96 NJA
FILE NAME 08\03098_12.DWG

	SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1997	
	DATE 8-7-86	TITLE VCO1 & MIXER	
MATERIAL	DRN APJ	DRAWING/DOC NO. 08-03098	
FINISH	CHKD NJA 18-8-86	TOLERANCES UNLESS OTHERWISE STATED 2 PLACE DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR	A3
	APPD NJA 30-10-86		
ISS			SHT. 1 OF 1

ISSUE 11 CONT
 C79 REMOVED
 D46 ADDED
 C80 WAS 10p
 C/R 24741
 04-02-97 JB

ISSUE 12
 -001 & -002 P/No's
 ADDED,
 -002 DETAIL ADDED.
 C/R 25186
 17-12-97 PM

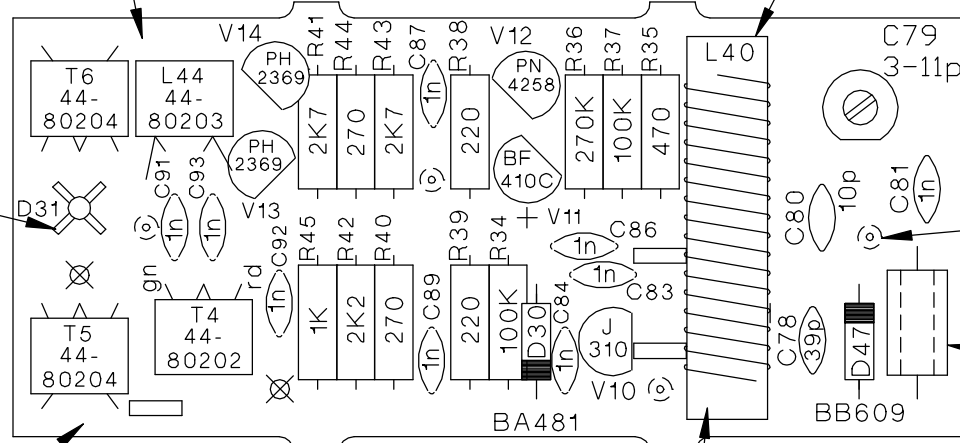
DO NOT SCALE

NOTE:

- V10 IS 23-20006
- 44-80202 - ye, bk, ye
 44-80203 - ye, rd, ye
 44-80204 - ye, gn, ye
- SECURE T4, T5, T6, L44
 & L38 TO PCB WITH
 EXPANDITE 88

D31
 HP5082-2830

CAUTION
 USE LOW TEMP
 SOLDER IRON
 (220°C)
 STATIC SENSITIVE



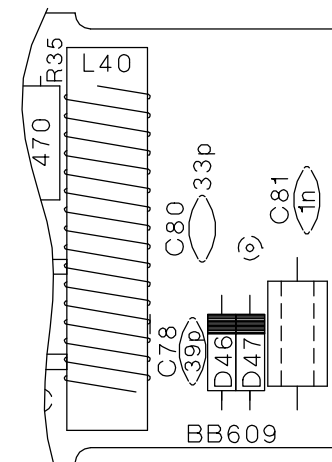
P/No 08-03099-001

PCB 07-01028 ISS 4

L40 44-70355
 BEFORE SOLDERING
 TAPS ON AS SHOWN
 ENSURE WINDINGS
 ARE EVEN & SECURE
 TO PCB WITH EXPANDITE 88

SECURE TO PCB
 WITH EXPANDITE 88

FIT AS CLOSE AS
 POSSIBLE TO PCB



P/No 08-03099-002
 ALL OTHER DETAIL
 AS PER -001.

47
 3

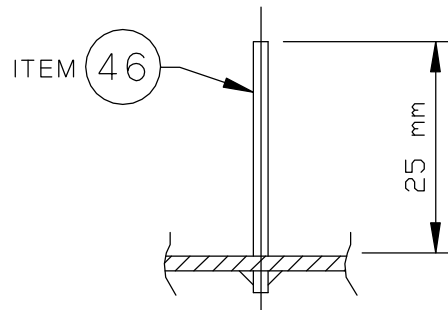
48
 6

44

43

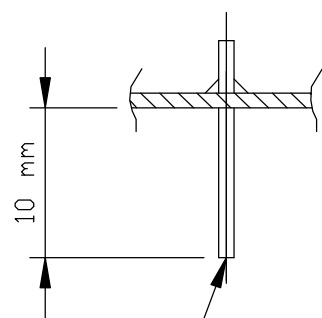
45

SOLDER SEAMS
 ON BOTH SIDES
 OF SHIELDS

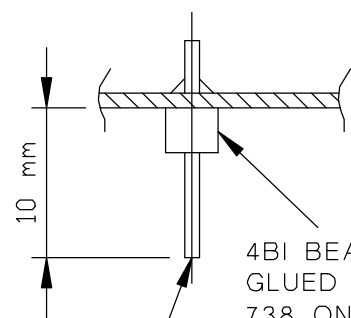


ON ONE POINT
 MARKED +

ON POINTS
 MARKED ⊗ = 2 OFF



ITEM 48



ITEM 48

4BI BEAD
 GLUED WITH
 738 ON ALL
 POINTS
 MARKED ⊙
 = 4 OFF

WARNING

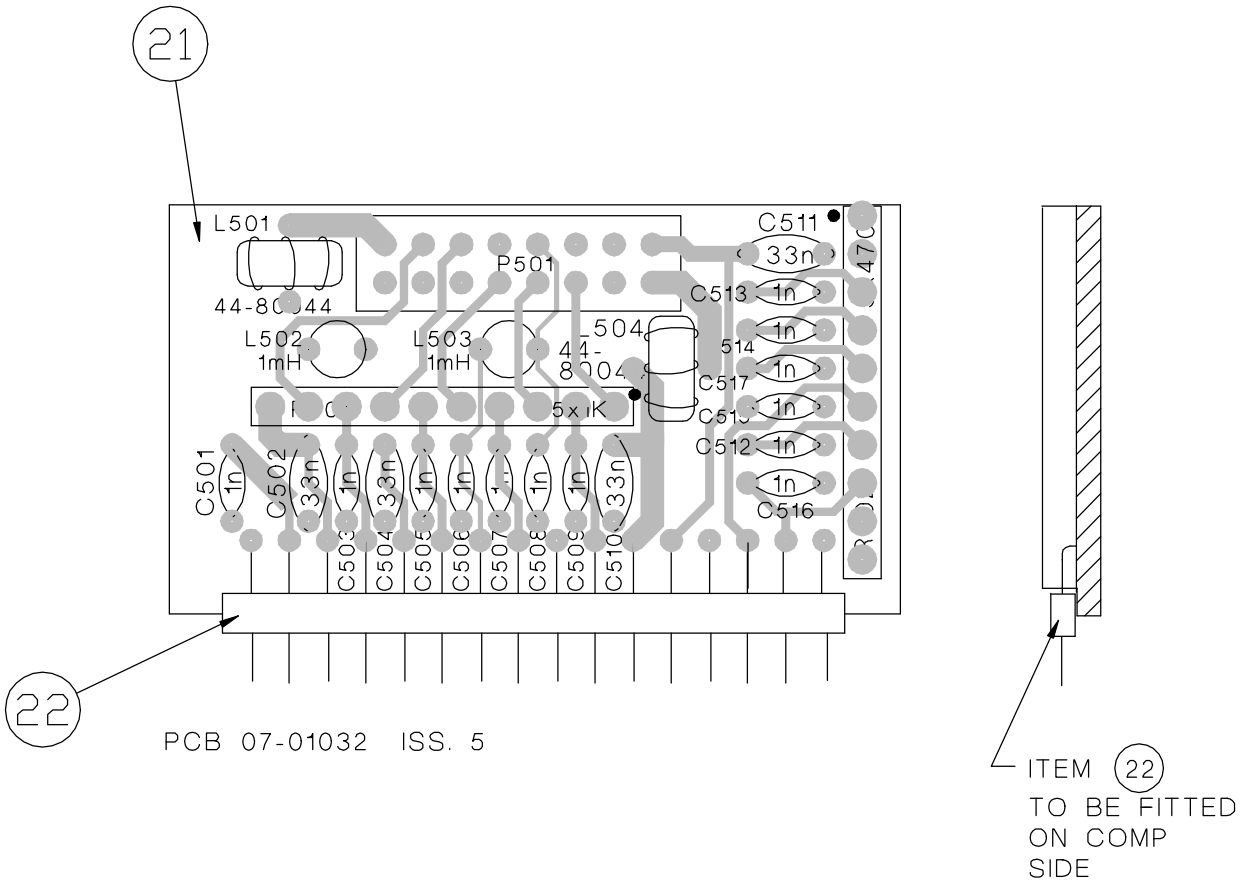
THIS ASSEMBLY CONTAINS
 ELECTRO-STATIC SENSITIVE DEVICES

- B. 21080
- ISSUE 2
 ITEM No'S CHANGED
 RTV CHANGED
 C/R 21257
 9-4-87 NJA
- ISSUE 3
 SCREW BLOCK
 DELETED
 C/R 21289
 10-6-87 NJA
- ISSUE 4
 PCB WAS ISS 1
 HOLES ADDED
 TO ACCOMMODATE
 CAP TYPE CHANGE
 C78 & C80
 C/R 21339
 29-8-87 NJA
- ISSUE 5
 C79 WAS 2-5p
 C/R 21374
 14-12-87 NJA
- ISSUE 6
 NOTE ADDED
 RE-SOLDER SEAMS
 C/R 21391
 15-2-88 NJA
- ISSUE 7
 V10 WAS J310
 C/R 21600
 19-8-88 NJA
- ISSUE 8
 V10 CHANGED
 TO J310
 C/R 21836
 20-12-88 NJA
- ISSUE 9
 R36 WAS 390K
 R38 WAS 180
 R45 WAS 470
 C/R 21908
 28-3-89 NJA
- ISSUE 10
 C79 CHANGED
 C/R 24423
 15-11-95 NJA
- ISSUE 11
 PCB NOW ISS 4
 C/R 24741
 28-11-96 JB

FILE NAME
 08\03099A12.1.DWG

			SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE	
	DRN	APJ	DATE 7-7-86	VCO2 & MIXER	
MATERIAL	CHKD	NJA	18-8-86	DRAWING/DOC NO.	
FINISH	APPD	NJA	30-10-86	08-03099	
TOLERANCES UNLESS OTHERWISE STATED			A3		
2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR			ISS		
			11 12		
			SHT. 1 OF 1		

DO NOT SCALE



PCB 07-01032 ISS. 5

ITEM 22
TO BE FITTED
ON COMP
SIDE

ISSUE 2 ITEM No'S CHANGED C/R 21257 NJA 9-4-87	ISSUE 3 IDENT SPOT ON R502 WAS ON WRONG END C/R 21280 27-5-87	ISSUE 4 C/R 21367 22-3-88	ISSUE 5 C/R 21646 BLACK SPOT MOVED 12-10-88 NJA	ISSUE 6 2x2.1 HOLES ADDED C/R 22898 NJA	ISSUE 7 IN LINE WITH PCB ISS. 3 C/R 23287 17-6-92 NJA	ISSUE 8 PCB CHANGED C/R 24450 6-3-96 CM	ISSUE 9 R502 WAS 5x1k, C512/517 TRANSPOSED. C/R 25246 2-3-98 NJA	FILE NAME 08\03127__9.DWG
---	--	---------------------------------	--	---	---	--	--	------------------------------

			SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE FILTER, REMOTE CONTROL
	DRN	APJ	DATE 10-7-86	
MATERIAL	CHKD	NJA	18-8-86	DRAWING/DOC NO. A4 08-03127
FINISH	APPD	NJA	30-10-86	
	TOLERANCES UNLESS OTHERWISE STATED			ISS 9
2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR			SHT. 1 OF 1	

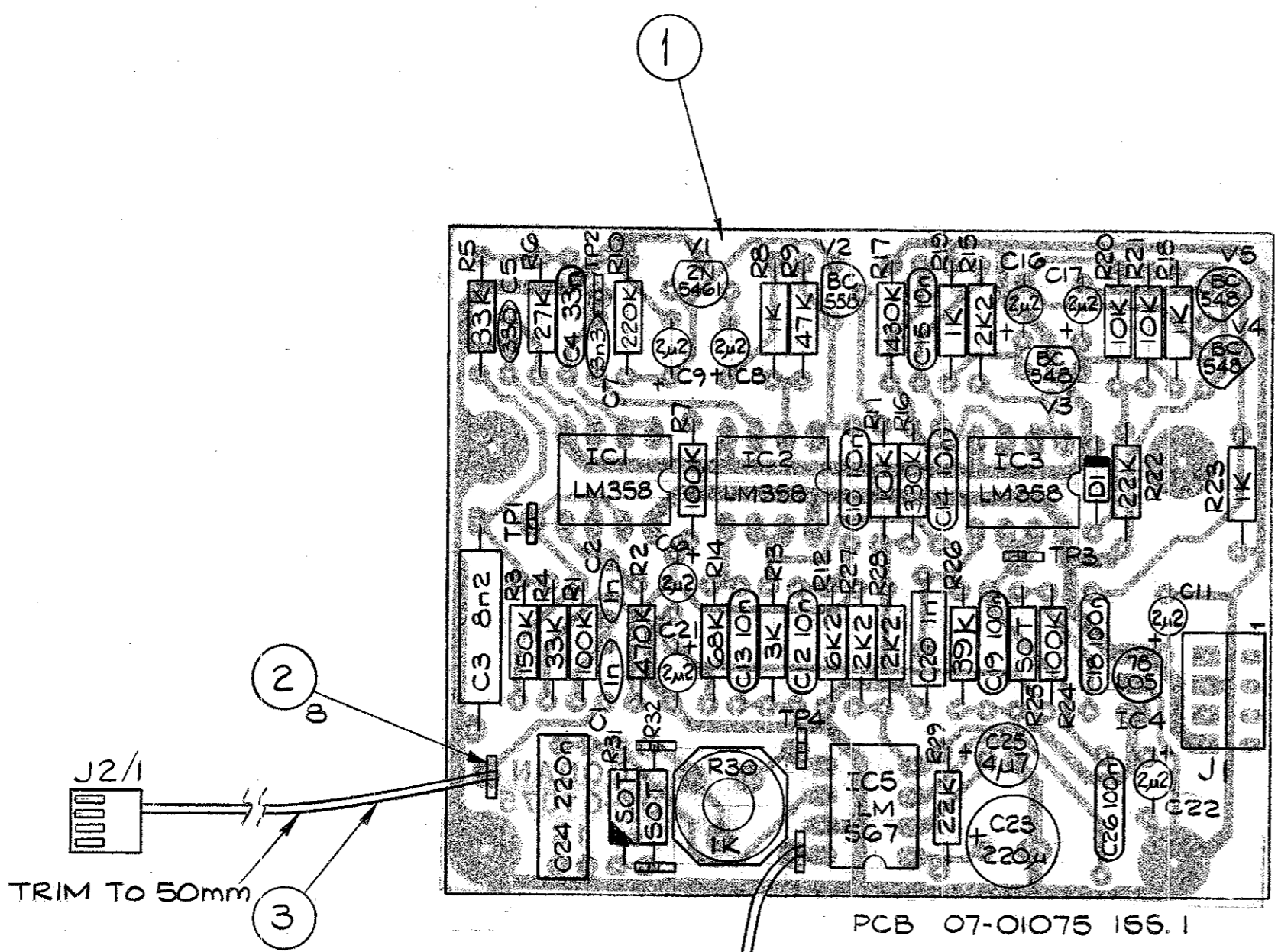
DO NOT SCALE

ISSUE 1
C/R. 21226
10-2-87 *ML*

ISSUE 2
R26 WAS SOT
R31 " CR25
R25 " 39K
C25 " 47μ
C/R. 21354
14-10-87 *ML*

ISSUE 3
R16 WAS 270K
C/R 22276
27-3-90 *ML*

ISSUE 4
C4 WAS 39n
R5 " 27K
C/R 22697
27-3-91 *ML*



FREQ.	R25	R31*
360Hz	47K	10K
440Hz	33K	8K2

* R31 MUST BE METAL FILM

DENOTES METAL FILM RESISTOR

	SCALE		TITLE		COPYRIGHT © CODAN 19	
	DRN. APJ	DATE 11-11-86	TWO-TONE DECODER PCB			
MATERIAL	CHKD. <i>ML</i>	DATE 12-11-86	DRAWING		DOC NO.	
FINISH	APPD. <i>ML</i>	DATE 10-2-87	A3		08-03273	
TOLERANCES UNLESS OTHERWISE STATED			ISS	1	2	3
2 PLACES DEC ±						
1 PLACE DEC ±						
ANGULAR ±						
			SHT			
			OF			

08-03273

283

400

DO NOT SCALE

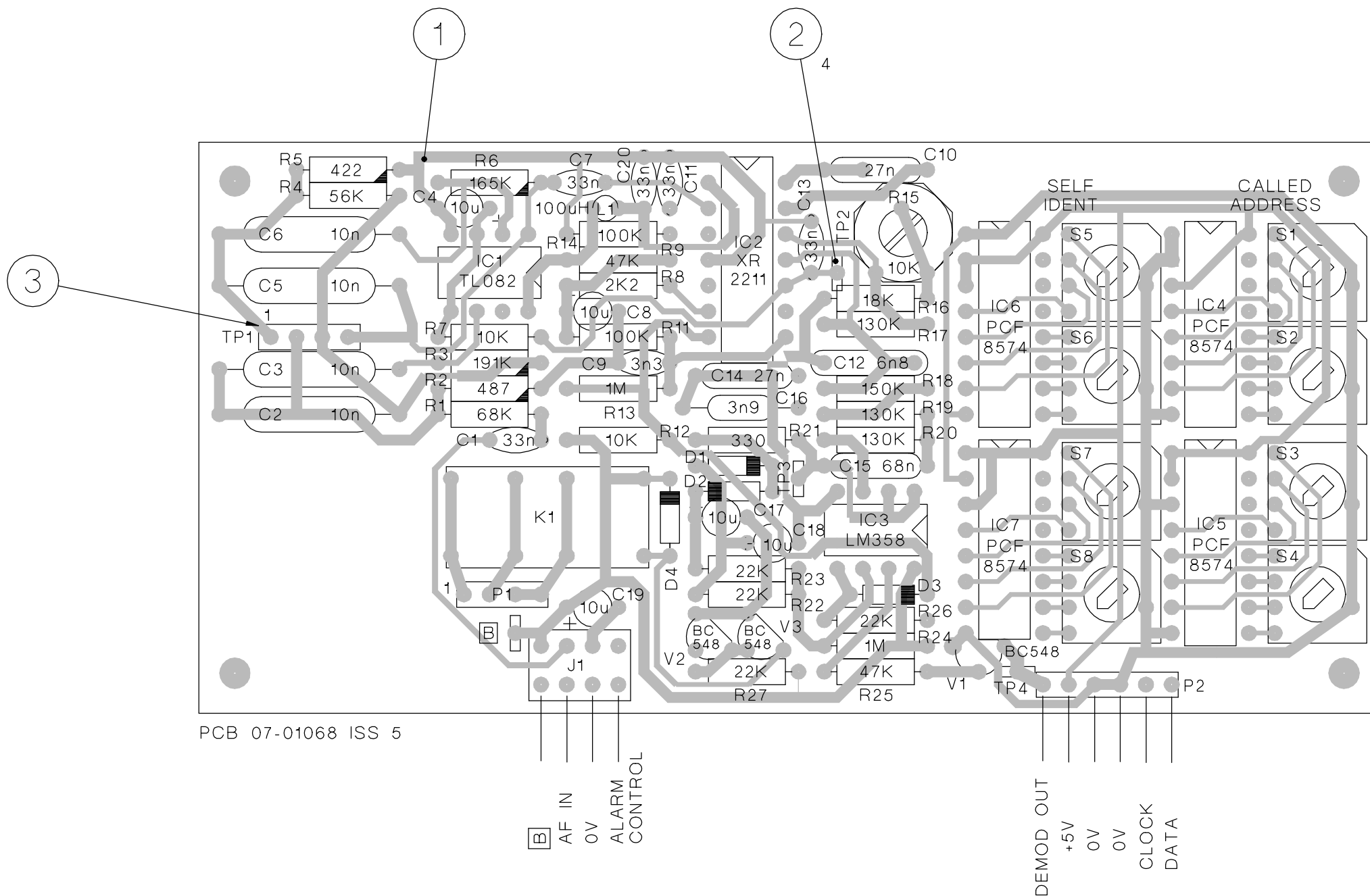
ISSUE B
C/R 21202
16-12-86 NJA

ISSUE 1
C/R 21226
10-2-87 NJA

ISSUE 2
C20 & L1 ADDED
C/R 21339
3-9-87 NJA

ISSUE 3
C/R 22128
VARIANT TABLE
ADDED
15-9-89 NJA

ISSUE 4
C/R 22812
R1 WAS 56K
R3 WAS 196K
15-4-91 NJA




PCB 07-01068 ISS 5

NOTES

1. ALL DIODES ARE BAW62 OR EQUIVALENT
2. RESISTORS SHOWN  ARE 1%

TYPE	ASSY. No	IC6	IC7	IC6	IC7	S1 - S8
SDE	08-03300	✓	✓	✓	✓	✓
SD	08-03300-000	—	—	—	—	—

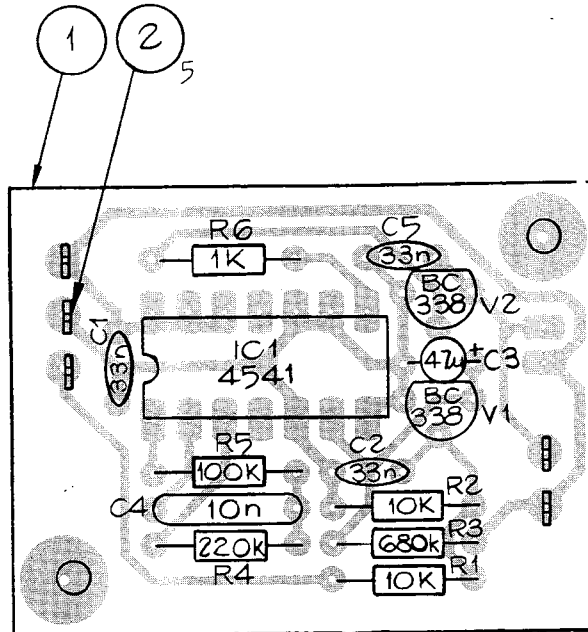
FILE NAME
08\03300_4.DWG

	SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1987 TITLE SDE, SDEM SELECTIVE CALL
	DRN APJ	
MATERIAL	CHKD NJA	12-11-86
FINISH	APPD NJA	10-2-87
TOLERANCES UNLESS OTHERWISE STATED		DRAWING/DOC NO. 08-03300
2 PLACES DEC. ±0.5		A3 ISS 4 SHT. 1 OF 1
1 PLACE DEC. ±1		
0 PLACE DEC. ±2°		
ANGULAR ±2°		


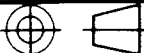
DO NOT SCALE

ISSUE B
R4 VALUE
CHGD FROM
200K
CAN 21697
24-11-88
7/6

ISSUE 2
C3 WAS 2u2
R3 WAS 470K
CIR 23584
24-2-93
M



PCB 07-01113 ISS.2

 CODAN			SCALE	TITLE PCB FAN CONTROLLER	COPYRIGHT © CODAN 19							
	DRN.	O.R.	DATE									
MATERIAL	CHKD.	<i>MJA</i>	11-10-88									
	APPD.	<i>MJA</i>	14-9-89									
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A4	DRAWING/DOC NO. 08-03334							
	2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±				ISS	1	2					SHT
											OF	1

1 2 3 4 5 6 7 8 9 10 11 12

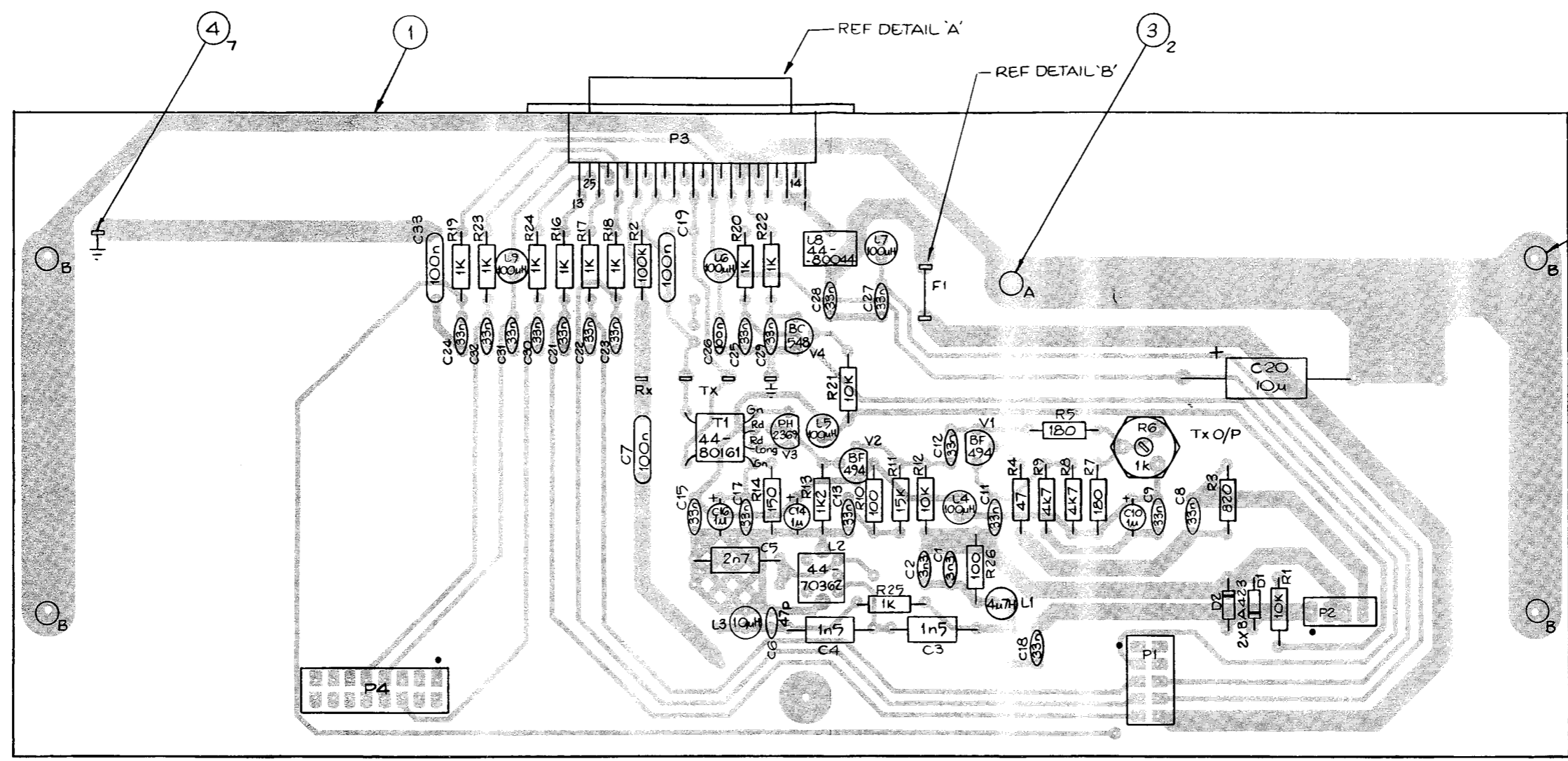
DO NOT SCALE

ISSUE B
C/R 21873
26-1-89 *ML*

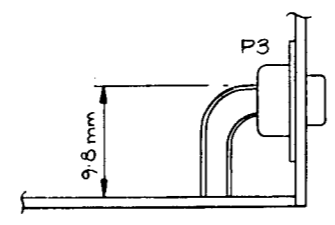
ISSUE C
L3 WAS 94u7H
C/R 21912
31-3-89 *ML*

ISSUE 2
C20 WAS 100u
C26 WAS 33n
C/R 22622
27-3-91 *ML*

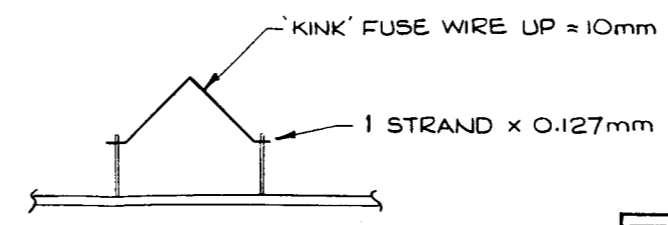
ISSUE 3
C20 LINE
DELETED
C/R 23435
1-10-92 *ML*



PCB 07-01209 155.2



DETAIL 'A'
N.T.S.



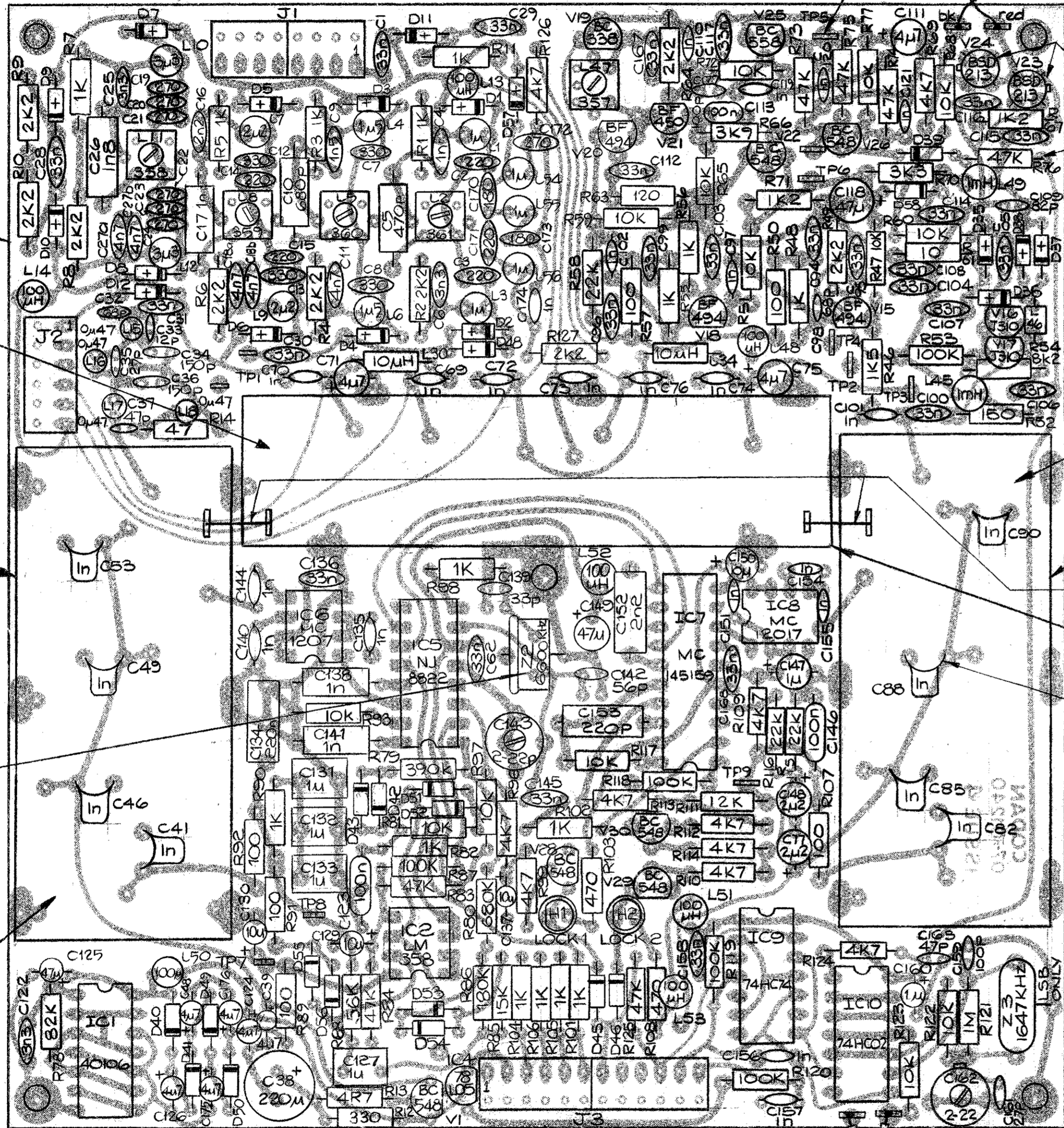
DETAIL 'B'
N.T.S.

NOTE:
ITEMS 2 & 3 FITTED TO
UNDERSIDE OF PCB.

CODAN	DRN.	O.R.	SCALE	TITLE PA/EXCITER INTERFACE	COPYRIGHT © CODAN 1993			
	CHKD.	DATE	12-9-88		DRAWING/DOC NO.	A2 08-03691		
MATERIAL	APPD.	DATE	14-9-89	TOLERANCES UNLESS OTHERWISE STATED		ISS	SHT	
FINISH	2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±					1/23	OF	

A
B
C
D
E
F
G
H

DO NOT SCALE



PCB 07-01240 155.4

screen inner

SEE NOTE 4

CAUTION

V24 & V23
STATIC SENSITIVE

FOLD WIRE
BACK FOR +VE
SUPPLY
CONNECTION

SOLDER 26 GAUGE
TCW TO BODY OF
CLIP FOR GND
CONNECTION.

DETAIL 'A'

XTAL (Z2)

25 SWG TCW TO BE
INSULATED USING
VIDAFLEX.

NOTE ALL 1n CAPACITORS SHOWN
THUS MUST BE LAYED DOWN.
CAPACITORS MAY BE FITTED ON TOP
OF P.C.B UNDER THE BOX ASSY'S OR
ON THE UNDERSIDE OF THE P.C.B.

NOTES:

1. L46 IS A FERRITE BEAD.
2. DIODES MARKED - [+] ARE BA423
ALL UNMARKED DIODES
ARE BA423 OR EQUIVALENT.
3. APPLY A LIBERAL AMOUNT OF
ISONEL 642 AIR DRY VARNISH
TO VCO 1 & 2 COILS: L21, L40
4. REMOVE FOR 8528 S
5. SOLDER ALL TABS & PINS
ON LIDS.

- ISSUE B
R79 WAS TOOK
CIR 21785
1-6-89 *MJL*
- ISSUE C
L17 WAS 0.122
C32 WAS 582P
C34 WAS 180P
C30 WAS 100P
C125 WAS 4M7
C/R 22002
6-7-89 *MJL*
- ISSUE D
C160 WAS 33n
CIR 22119
30-8-89 *MJL*
- ISSUE 2
D57 WAS D47
C150 " 33n
C142 " 68P
C/R 22151
15-11-89 *MJL*
- ISSUE 3
C/R 22284
R62 DELETED
C/R 22252
L52 DESIGN-
NATION ADDED
31-1-90 *MJL*
- ISSUE 4
L12 WAS L10
CIR 22516
21-8-90 *MJL*
- ISSUE 5
D58 ADDED
CIR 22538
30-8-90 *MJL*
- ISSUE 6
DETAIL 'A'
ADDED
C/R 22811
17-4-90 *MJL*
- ISSUE 7
R93 WAS 22K
C/R 23151
17-12-91 *MJL*

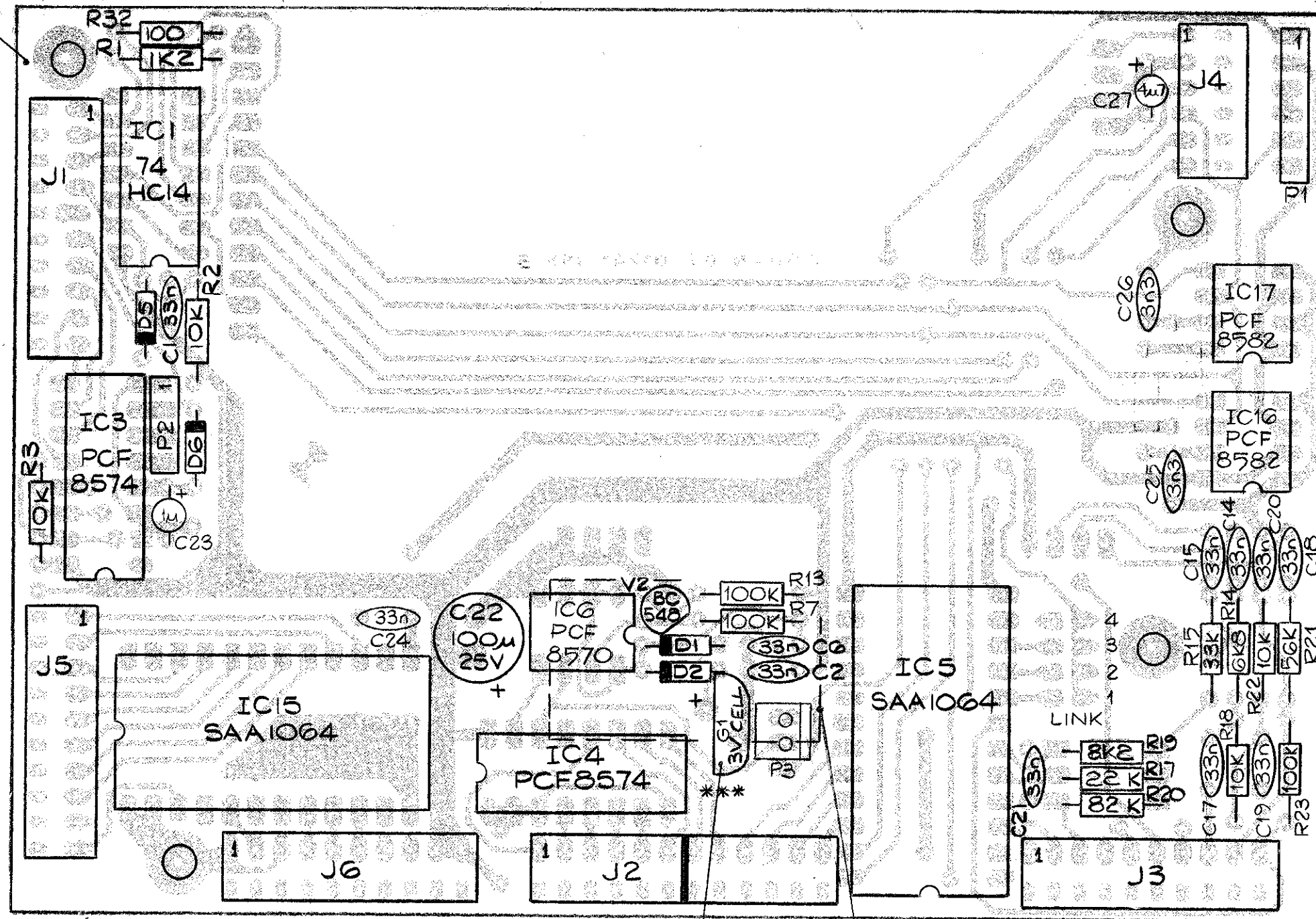
REF DETAIL 'A'

08-03740-001	AS DRAWN

	SCALE	2:1	TITLE RF, MIXER & DUAL SYNTHESISER PCB	DRAWING/DOC NO. A2 08-03740
	DATE	19-10-88		
MATERIAL	CHKD.	19-4-89	ISS	
FINISH	APPD.	14-9-89	1 2 3 4 5 6 7	
TOLERANCES			SHT	
UNLESS OTHERWISE STATED			OF	
2 PLACES DEC ±				
1 PLACE DEC ±				
ANGULAR ±				

DO NOT SCALE

21



PCB 07-01241 155.3

NOTES:

1. ALL DIODES BAW62 OR EQUIVALENT.
2. *** 3 VOLT CELL MUST BE FITTED LAST MANUALLY
3. FIT ITEM (23) OVER G1
4. FIT ITEM (22) UNDER PCB AS SHOWN

CAUTION

	SCALE		TITLE		COPYRIGHT © CODAN 1986	
	DRN.	O.R.	DATE	MICROPROCESSOR INTERFACE		
MATERIAL	CHKD.	APPD.	12-10-88	DRAWING/DOC NO.		
			14-4-89	A3 08-03741		
			14-9-89	ISS		
FINISH	TOLERANCES UNLESS OTHERWISE STATED			SHT		
	2 PLACES DEC ±			1 2 3 4		
	1 PLACE DEC ±			OF		
	ANGULAR ±					

155.B
 C27 ADDED
 CIR 21985
 20-6-89
 ISSUE 2
 C/R 22289
 R17 WAS 33K
 R19 WAS 15K
 30-1-90
 ISSUE 3
 P3 ADDED
 CIR 22538
 27-8-90
 ISSUE 4
 R33+R34 (56k)
 DELETED
 CIR 26775
 9-11-90

23

22

283

400

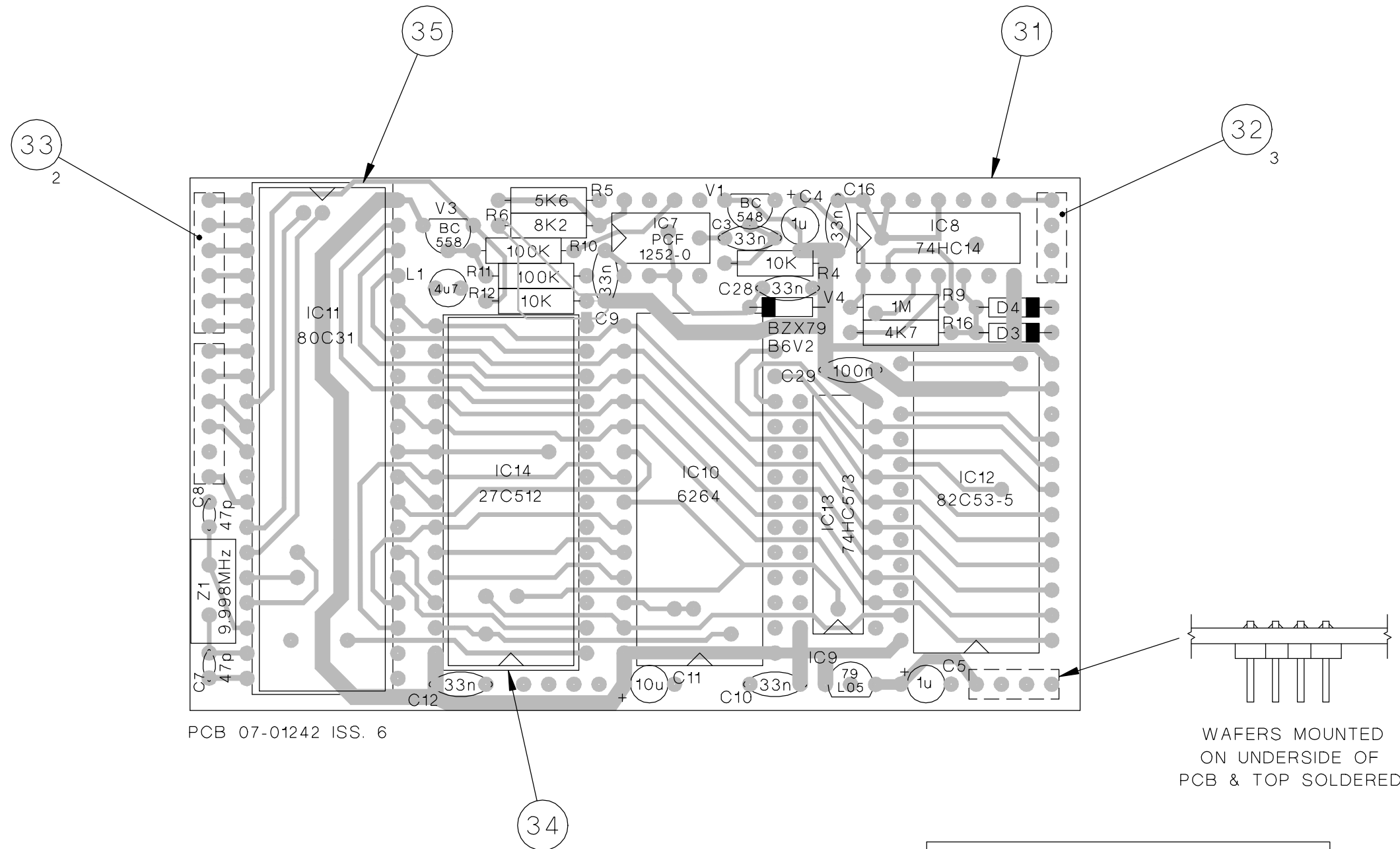
DO NOT SCALE

ISSUE 2
L1 WAS 100uH
C/R 22151
15-11-89 NJA

ISSUE 3
C/R 22252
31-01-90 NJA

ISSUE 4
C28, 29, V4 ADDED
C9 WAS 10u
R6 WAS 1K
IC7 WAS PCF1251
R8, 2K2 DELETED
C/R 22440
25-04-90 NJA

ISSUE 5
R12 WAS 100K
C/R 23422
02-09-92 CM



PCB 07-01242 ISS. 6

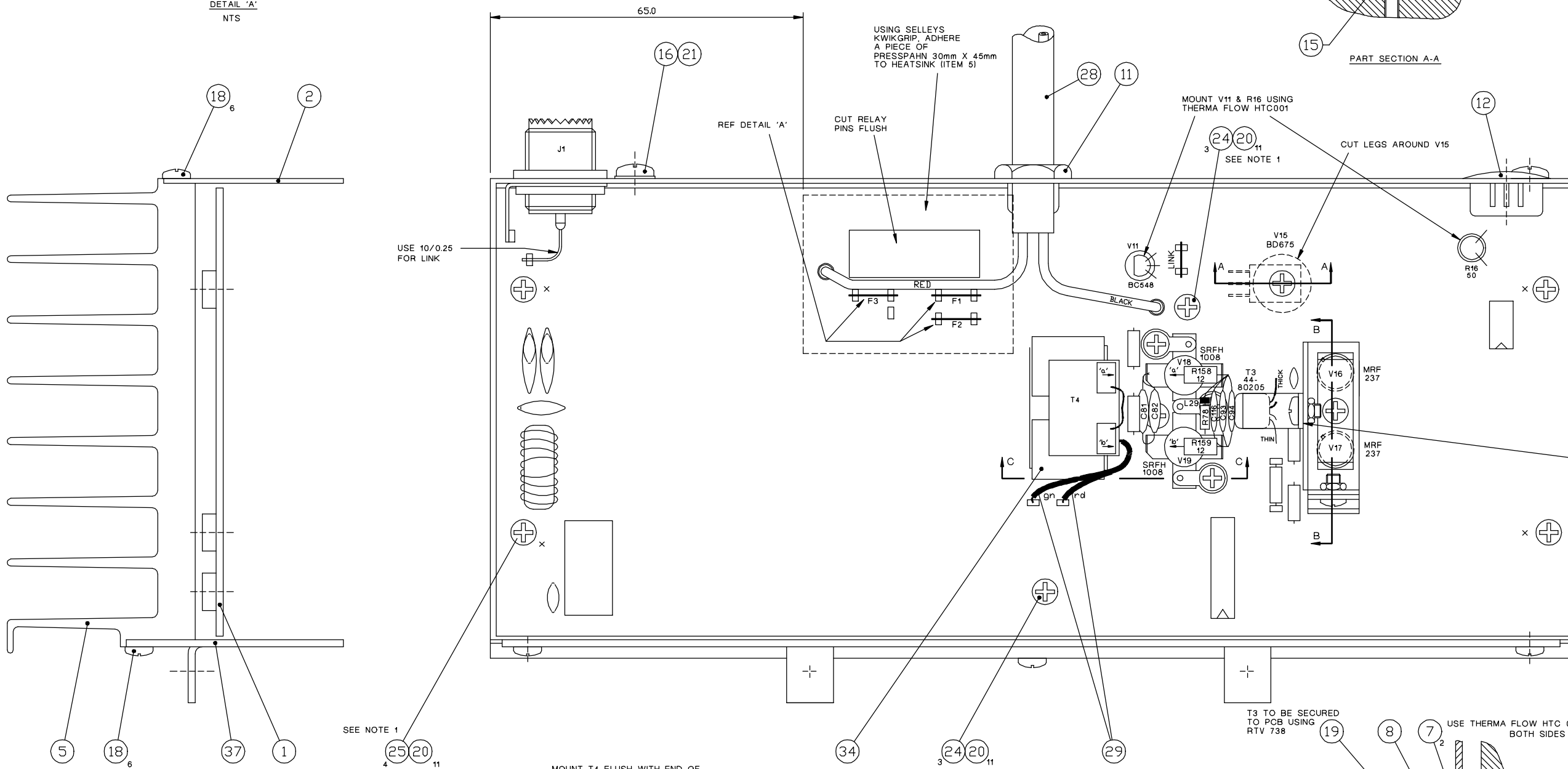
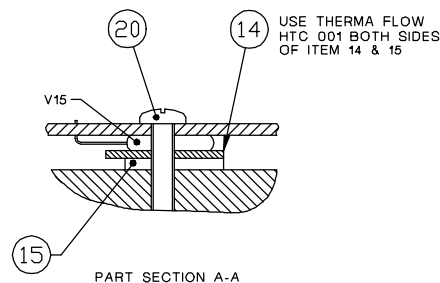
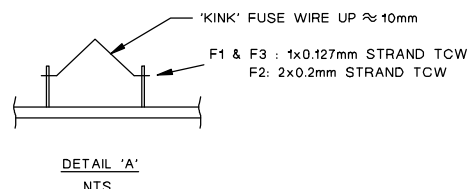
WAFERS MOUNTED
ON UNDERSIDE OF
PCB & TOP SOLDERED

WARNING
THIS ASSEMBLY CONTAINS
ELECTRO-STATIC SENSITIVE DEVICES

FILE NAME
08\03742_5.DWG

			SCALE	© CODAN PTY LTD, A.C.N. 007 590 605: 1997			
	DRN	CF	DATE	TITLE			
MATERIAL	CHKD	NJA	12-10-88	MICROPROCESSOR ASSY.			
FINISH	APPD	NJA	19-04-89	DRAWING/DOC NO.			
	TOLERANCES UNLESS OTHERWISE STATED			A3	08-03742		
2 PLACES DEC.			ISS	SHT. 1			
1 PLACE DEC.			5	OF 1			
0 PLACE DEC.			REDRAWN				
ANGULAR							

DO NOT SCALE



SEE NOTE 1
 25 20 11
 4
 ENSURE SHORT (3mm) STANDOFFS ARE FITTED IN POSITIONS SHOWN THUS X

MOUNT T4 FLUSH WITH END OF HEATSINK & AS CLOSE AS POSSIBLE TO V18 & V19.

APPLY LOCTITE 290 BETWEEN HEATSINK (ITEM 34) AND CORE

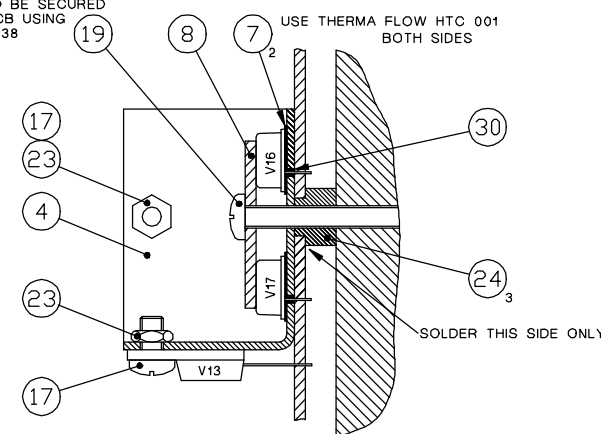
NOTE MNTG HOLE IS OFFSET. FIT T4 WITH CARE!

USE THERMA-FLOW HTC001 BOTH SIDES

BEND 2 TABS AT 90°, 1.5 mm FROM ENDS (BOTH TRANSISTORS) AS SHOWN

USE THERMA FLOW HTC 001 BOTH SIDES

T3 TO BE SECURED TO PCB USING RTV 738



PART SECTION C-C

NOTES:

1. SOLDER ITEMS 24 AND 25 ON UNDER SIDE OF PCB, WHERE POSSIBLE.
2. SECURE L29 TO WIRE USING EXPANDITE 88

ISSUE B
 REF SHT 2
 ISSUE C
 REF SHT 2
 ISSUE D
 C81 & C82 WERE 330p
 C/R 22119 NJA
 ISSUE 2
 REF SHT 2 NJA
 ISSUE 3
 C117 ADDED
 C/R 22270
 20-12-89 NJA
 ISSUE 4
 C117 REMOVED
 C/R 22304
 27/3/90 NJA
 ISSUE 5
 REF SHT 2
 ISSUE 6
 REF SHT 2
 ISSUE 7
 REF SHT 2
 ISSUE 8
 REF SHT 2
 ISSUE 9
 REF SHT 2
 ISSUE 10
 REF SHT 2
 ISSUE 11
 REF SHT 2
 ISSUE 12
 ITEM 30 WAS
 ITEM 29
 C/R 23681
 9-8-93
 ISSUE 13
 REF SHT 2
 ISSUE 14
 REF SHT 2
 ISSUE 15
 C/R 24316 &
 24317
 ITEMS 33,34
 & 36 ADDED
 REF SHT 2 ALSO
 2-11-95 NJA
 ISSUE 16
 C/R 24666
 REF SHT 2
 ISSUE 17:
 C/R 25030
 REFER SHT 2

FILE NAME
 08\03743A17.DWG

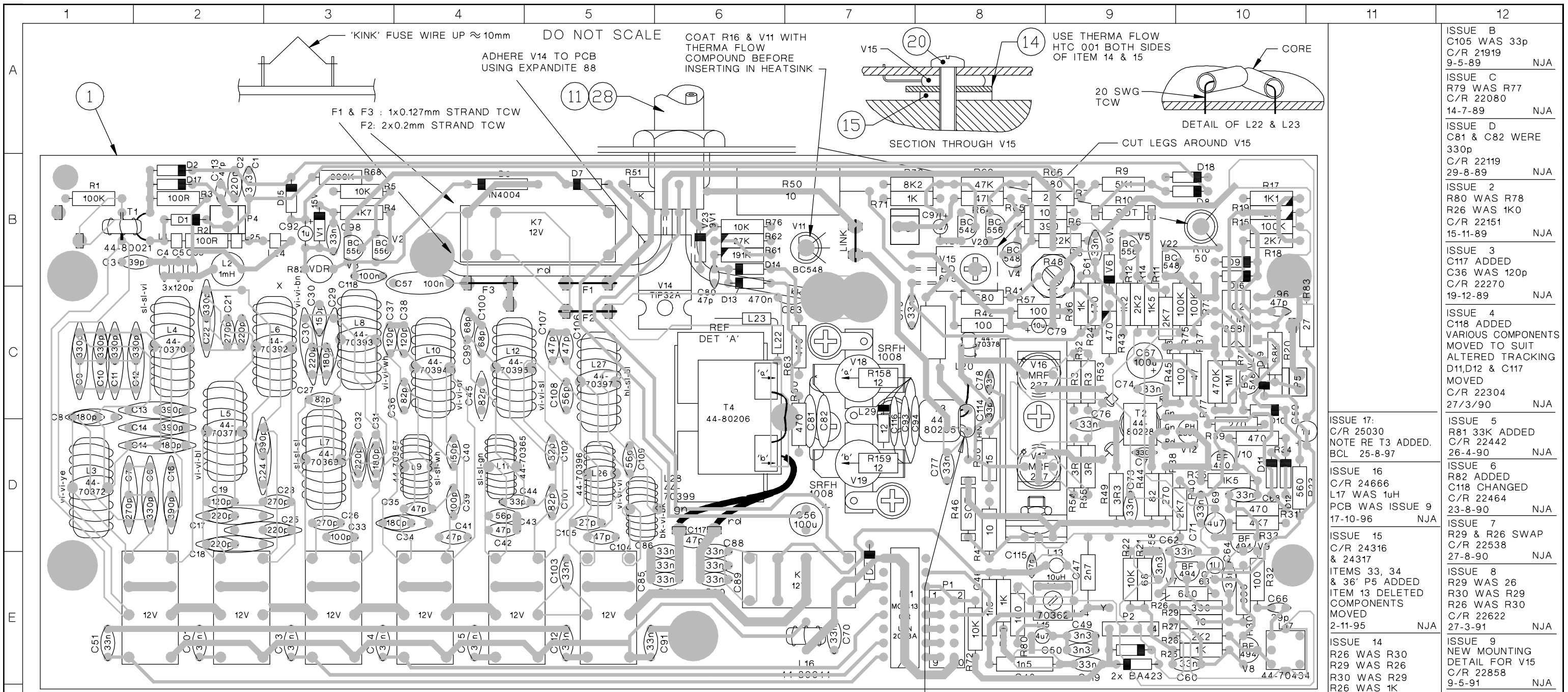
ASSY No.	TYPE
08-03743-001	8525/8528
08-03743-002	8727

CODAN

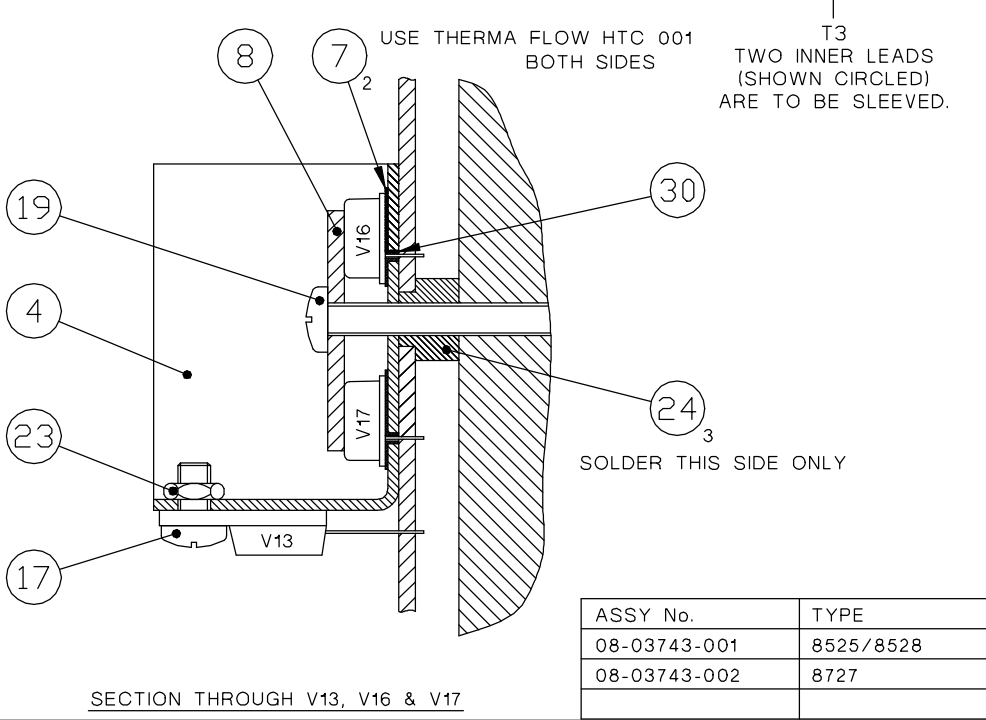
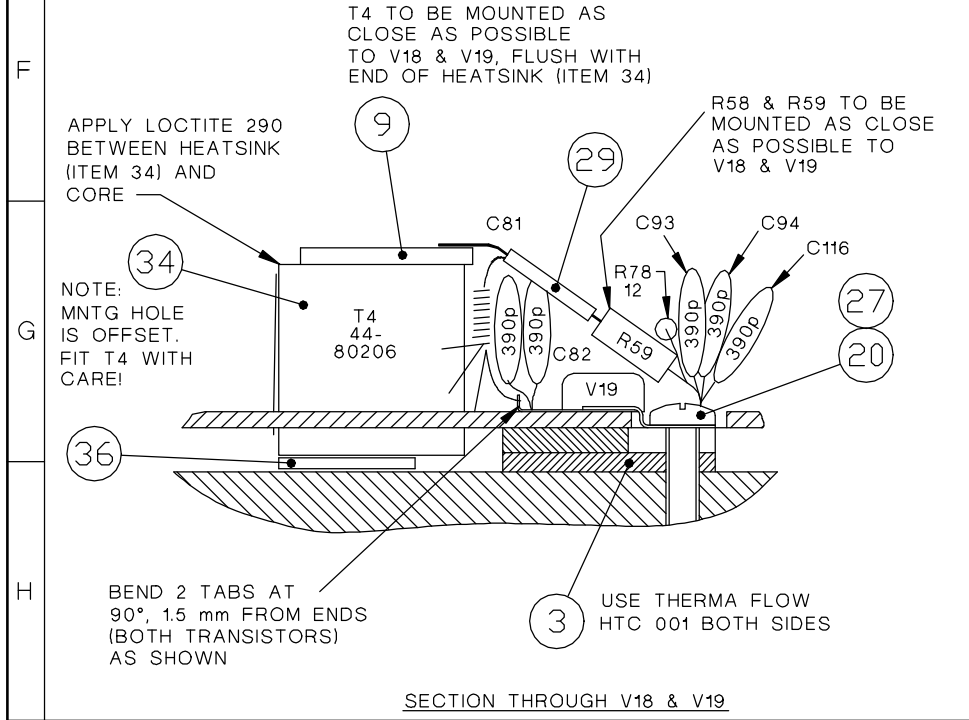
SCALE	DATE
2:1	20-10-88
DRN	CF
CHKD	NJA
APPD	NJA
TOLERANCES UNLESS OTHERWISE STATED	
2 PLACES DEC.	
1 PLACE DEC.	
0 PLACE DEC.	
ANGULAR	

TITLE	DRAWING/DOC NO.
PA ASSEMBLY C/W HEATSINK	08-03743
ISS	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
SHT. 1	OF 2

DIMENSIONS IN mm



PCB 07-01243 ISS. 10



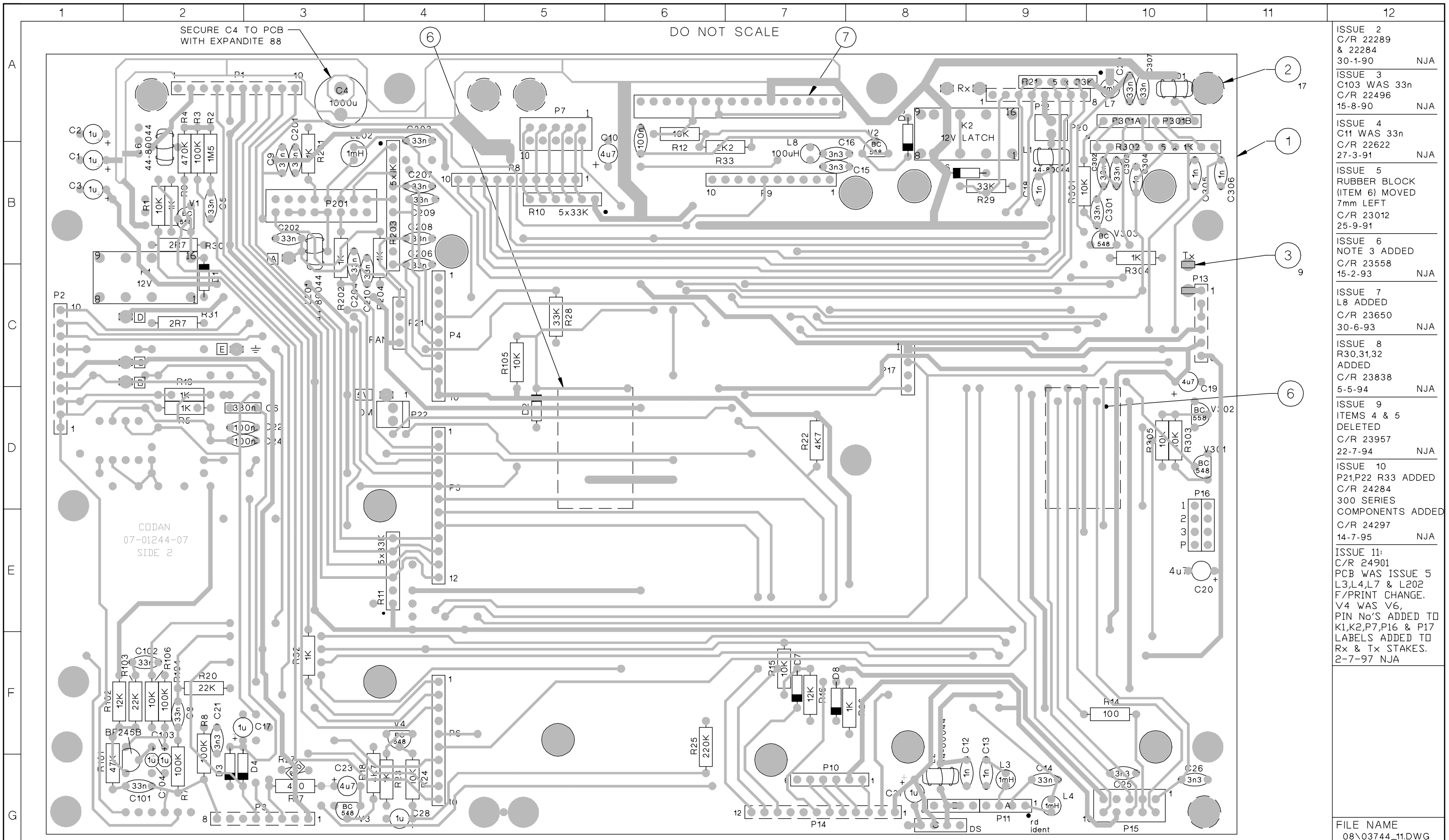
NOTES:

1. ALL DIODES ARE BAW62 OR EQUIV. UNLESS OTHERWISE STATED.
2. L1, L24, L25, L29 ARE FERRITE BEADS.
3. CAPACITORS SHOWN THIS WAY ARE FOR DIFFERENT LEAD SPACINGS AND SIZE
4. RESISTORS SHOWN WITH THIS SYMBOL ARE ±2%
5. SECURE ALL INDUCTORS & TRANSFORMERS TO PCB USING EXPANDITE 88
6. SECURE L29 TO WIRE USING EXPANDITE 88

ASSY No.	TYPE
08-03743-001	8525/8528
08-03743-002	8727

		SCALE 2:1 DATE 12-10-88		© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE PA & FILTER PCB ASSY																											
MATERIAL		DRN	CF	APPD NJA 14-9-89 TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR																											
FINISH		CHKD	NJA	DRAWING/DOC NO. A2 08-03743																											
<table border="1"> <thead> <tr> <th>ISS</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>9</th> <th>10</th> <th>11</th> <th>12</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		ISS	1	2	3	4	5	6	7	8	9	10	11	12														SHT. 2 OF 2			
ISS	1	2	3	4	5	6	7	8	9	10	11	12																			

ISSUE B C105 WAS 33p C/R 21919 9-5-89 NJA	ISSUE C R79 WAS R77 C/R 22080 14-7-89 NJA	ISSUE D C81 & C82 WERE 330p C/R 22119 29-8-89 NJA	ISSUE 2 R80 WAS R78 R26 WAS 1K0 C/R 22151 15-11-89 NJA	ISSUE 3 C117 ADDED C36 WAS 120p C/R 22270 19-12-89 NJA	ISSUE 4 C118 ADDED VARIOUS COMPONENTS MOVED TO SUIT ALTERED TRACKING D11, D12 & C117 MOVED C/R 22304 27/3/90 NJA	ISSUE 5 R81 33K ADDED C/R 22442 26-4-90 NJA	ISSUE 6 R82 ADDED C118 CHANGED C/R 22464 23-8-90 NJA	ISSUE 7 R29 & R26 SWAP C/R 22538 27-8-90 NJA	ISSUE 8 R29 WAS 26 R30 WAS R29 R26 WAS R30 C/R 22622 27-3-91 NJA	ISSUE 9 NEW MOUNTING DETAIL FOR V15 C/R 22858 9-5-91 NJA	ISSUE 10 C116 CHANGED TO C119 C/R 23227 1-7-92 NJA	ISSUE 11 D18 ADDED C/R 23558 DIA FUSE WIRE CHANGED C/R 23497 16-2-93 NJA	ISSUE 12 ITEM 30 WAS 29 C/R 23681 9-8-92 NJA	FILE NAME 08\03743B17.DWG
---	---	---	---	---	---	---	---	--	--	---	---	--	--	------------------------------



ISSUE 2
C/R 22289
& 22284
30-1-90 NJA

ISSUE 3
C103 WAS 33n
C/R 22496
15-8-90 NJA

ISSUE 4
C11 WAS 33n
C/R 22622
27-3-91 NJA

ISSUE 5
RUBBER BLOCK
(ITEM 6) MOVED
7mm LEFT
C/R 23012
25-9-91

ISSUE 6
NOTE 3 ADDED
C/R 23558
15-2-93 NJA

ISSUE 7
L8 ADDED
C/R 23650
30-6-93 NJA

ISSUE 8
R30,31,32
ADDED
C/R 23838
5-5-94 NJA

ISSUE 9
ITEMS 4 & 5
DELETED
C/R 23957
22-7-94 NJA

ISSUE 10
P21,P22 R33 ADDED
C/R 24284
300 SERIES
COMPONENTS ADDED
C/R 24297
14-7-95 NJA

ISSUE 11:
C/R 24901
PCB WAS ISSUE 5
L3,L4,L7 & L202
F/PRINT CHANGE.
V4 WAS V6,
PIN No'S ADDED TO
K1,K2,P7,P16 & P17
LABELS ADDED TO
Rx & Tx STAKES.
2-7-97 NJA

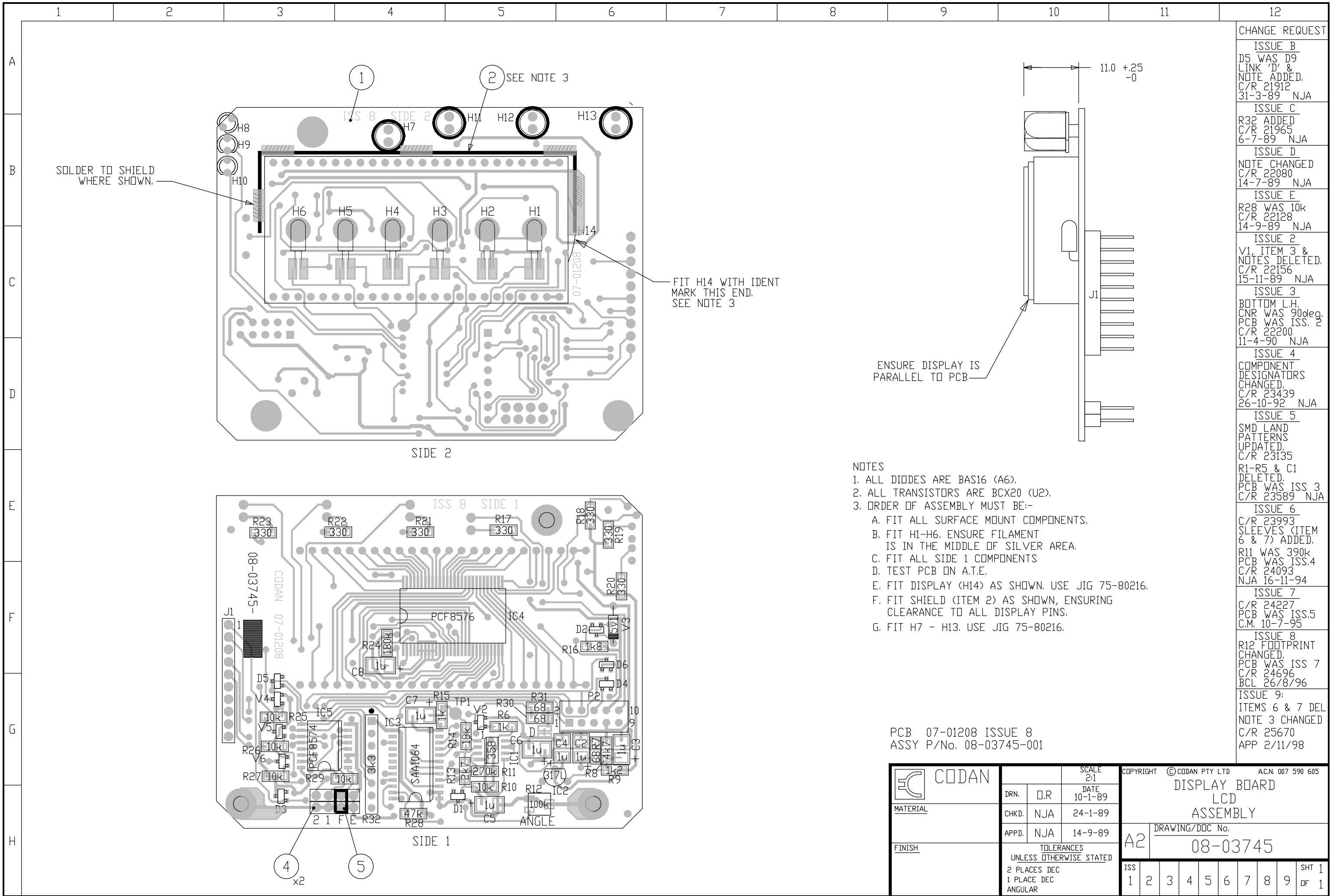
FILE NAME
08\03744_11.DWG

PCB 07-01244-07

- NOTES.
1. ALL DIODES BAW62 OR EQUIV.
 2. ADHERE ITEMS (6) TO PCB WITH KWIKGRIP IN POSITIONS SHOWN.
 3. FIT A 470 OHM RESISTOR ACROSS R17 WHEN OPTION CB IS FITTED.

08-03744-001	AS DRAWN

	SCALE	2:1	© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE MOTHER BOARD									
	DRN	CF		DATE 12-10-88								
MATERIAL	CHKD	NJA	19-4-89									
	APPD	NJA	14-9-89									
FINISH	TOLERANCES UNLESS OTHERWISE STATED		A2 08-03744									
	2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR											
DIMENSIONS IN mm			ISS									
			<table border="1"> <tr> <td>5</td> <td>6</td> <td>7</td> <td>8</td> <td>9</td> <td>10</td> <td>11</td> <td> </td> <td> </td> </tr> </table>	5	6	7	8	9	10	11		
5	6	7	8	9	10	11						
			SHT. 1 OF 1									

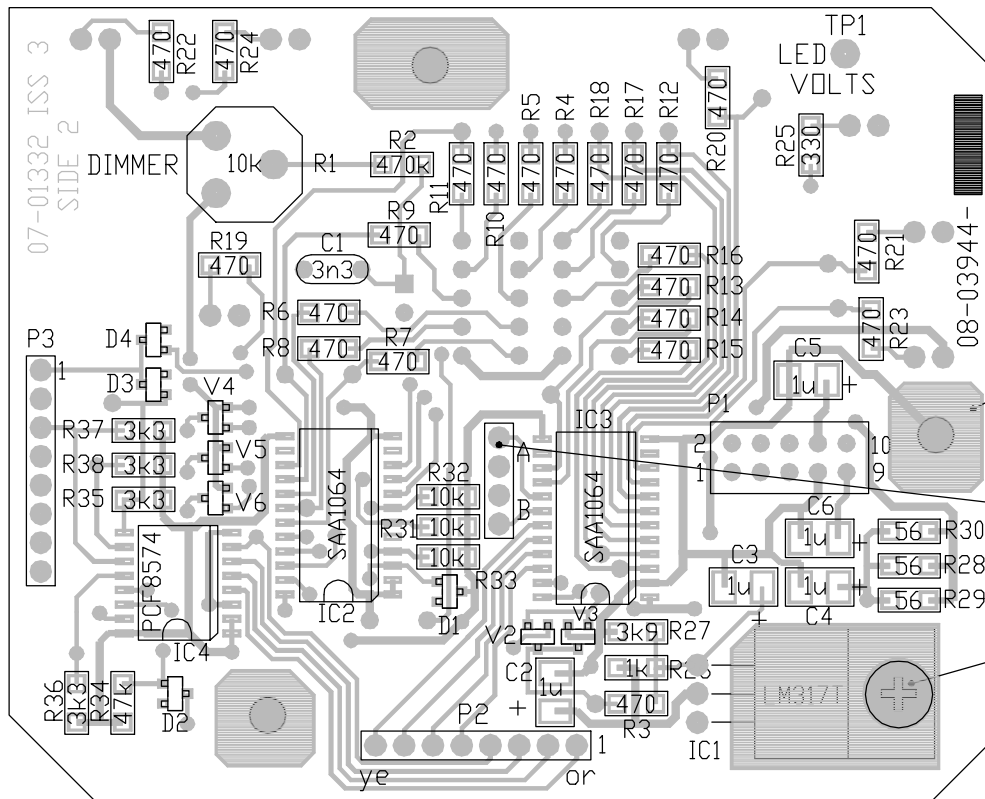
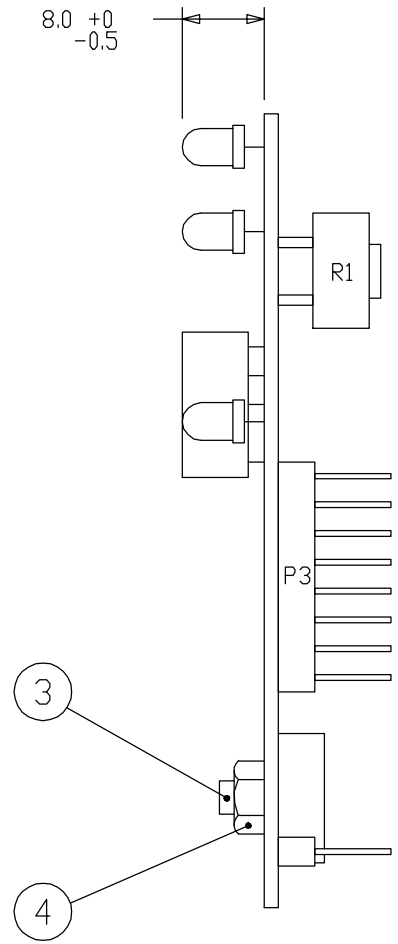
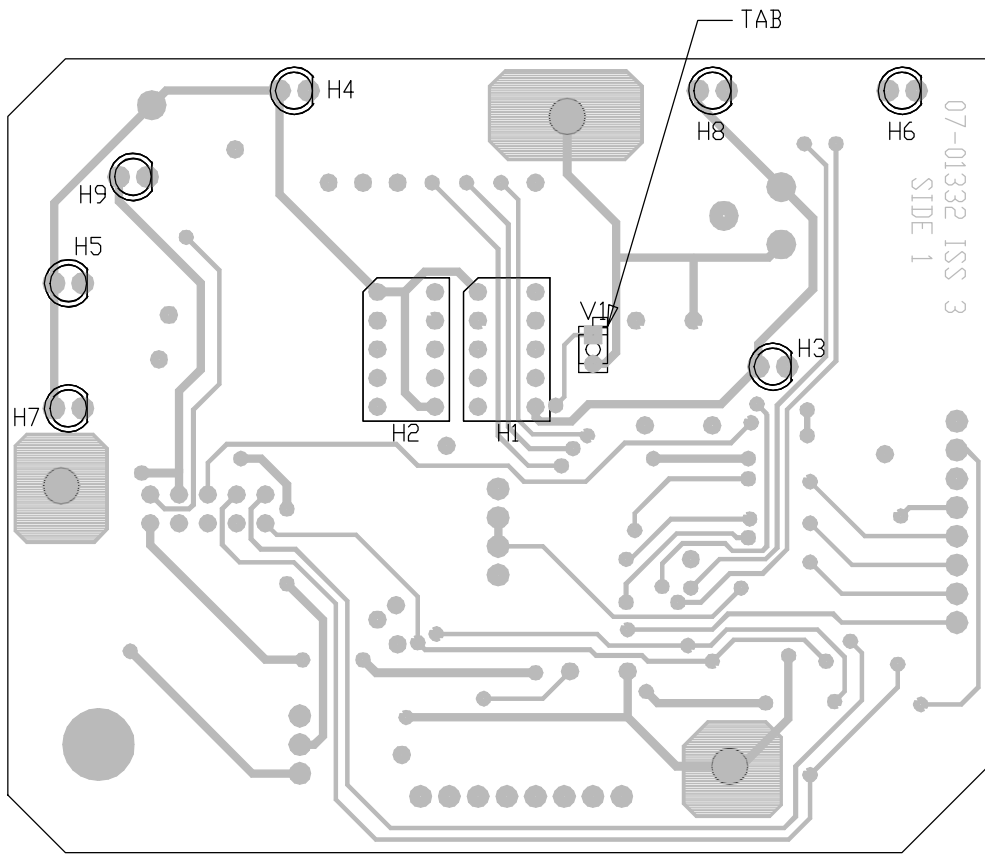


CHANGE REQUEST									
ISSUE B									
D5 WAS D9									
LINK 'D' &									
NOTE ADDED.									
C/R 21912									
31-3-89 NJA									
ISSUE C									
R32 ADDED									
C/R 21965									
6-7-89 NJA									
ISSUE D									
NOTE CHANGED									
C/R 22080									
14-7-89 NJA									
ISSUE E									
R28 WAS 10k									
C/R 22128									
14-9-89 NJA									
ISSUE 2									
V1, ITEM 3 &									
NOTES DELETED.									
C/R 22156									
15-11-89 NJA									
ISSUE 3									
BOTTOM L.H.									
CNR WAS 90deg.									
PCB WAS ISS. 2									
C/R 22200									
11-4-90 NJA									
ISSUE 4									
COMPONENT									
DESIGNATORS									
CHANGED.									
C/R 23439									
26-10-92 NJA									
ISSUE 5									
SMD LAND									
PATTERNS									
UPDATED.									
C/R 23135									
R1-R5 & C1									
DELETED.									
PCB WAS ISS. 3									
C/R 23589 NJA									
ISSUE 6									
C/R 23993									
SLEEVES (ITEM									
6 & 7) ADDED.									
R11 WAS 390k									
PCB WAS ISS.4									
C/R 24093									
NJA 16-11-94									
ISSUE 7									
C/R 24227									
PCB WAS ISS.5									
C.M. 10-7-95									
ISSUE 8									
R12 FOOTPRINT									
CHANGED.									
PCB WAS ISS 7									
C/R 24696									
BCL 26/8/96									
ISSUE 9:									
ITEMS 6 & 7 DEL									
NOTE 3 CHANGED									
C/R 25670									
APP 2/11/98									

- NOTES
- ALL DIODES ARE BAS16 (A6).
 - ALL TRANSISTORS ARE BCX20 (U2).
 - ORDER OF ASSEMBLY MUST BE:-
 - FIT ALL SURFACE MOUNT COMPONENTS.
 - FIT H1-H6. ENSURE FILAMENT IS IN THE MIDDLE OF SILVER AREA.
 - FIT ALL SIDE 1 COMPONENTS
 - TEST PCB ON A.T.E.
 - FIT DISPLAY (H14) AS SHOWN. USE JIG 75-80216.
 - FIT SHIELD (ITEM 2) AS SHOWN, ENSURING CLEARANCE TO ALL DISPLAY PINS.
 - FIT H7 - H13. USE JIG 75-80216.

PCB 07-01208 ISSUE 8
 ASSY P/No. 08-03745-001

	SCALE 2:1		COPYRIGHT ©CODAN PTY LTD ACN 007 590 605							
	DRN.	D.R	DATE	DISPLAY BOARD						
MATERIAL	CHKD.	NJA	10-1-89	LCD						
	APPD.	NJA	14-9-89	ASSEMBLY						
FINISH	TOLERANCES UNLESS OTHERWISE STATED		DRAWING/DOC No.		A2					
	2 PLACES DEC		08-03745							
	1 PLACE DEC									
	ANGULAR									
ISS	1	2	3	4	5	6	7	8	9	SHT 1 OF 1



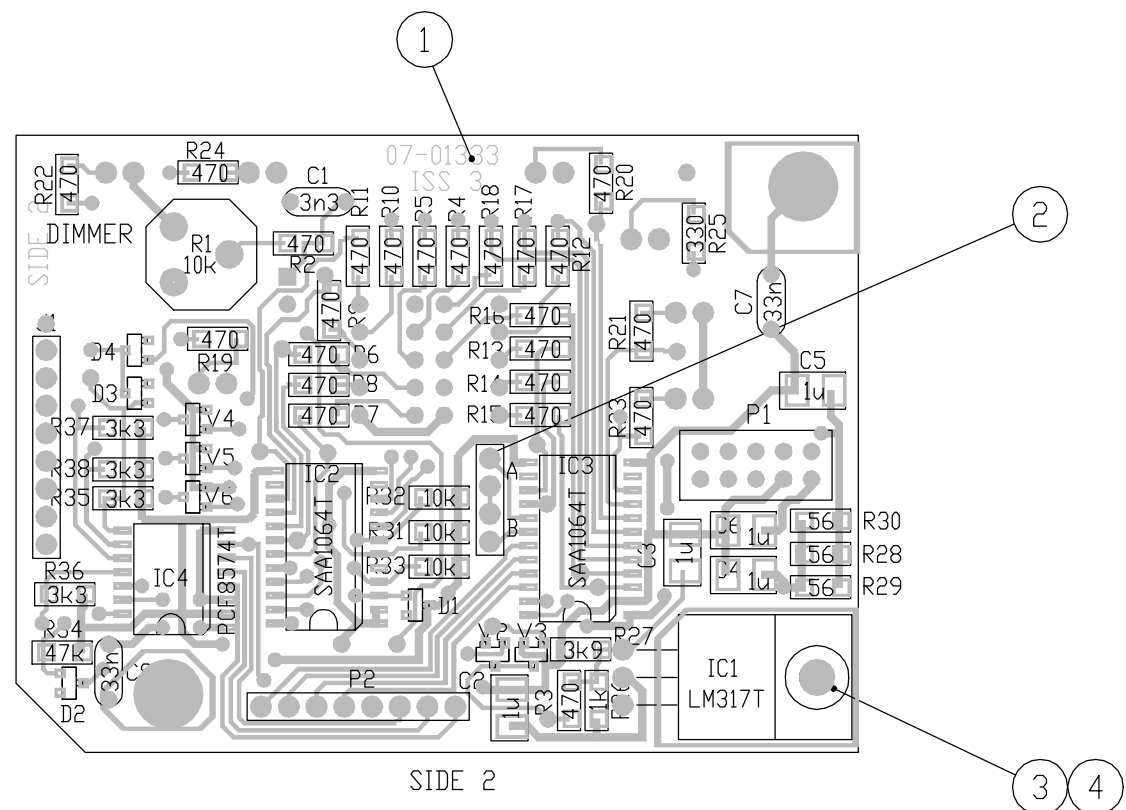
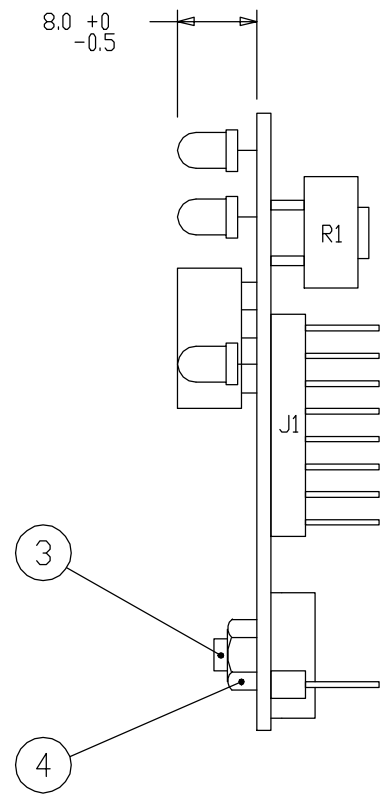
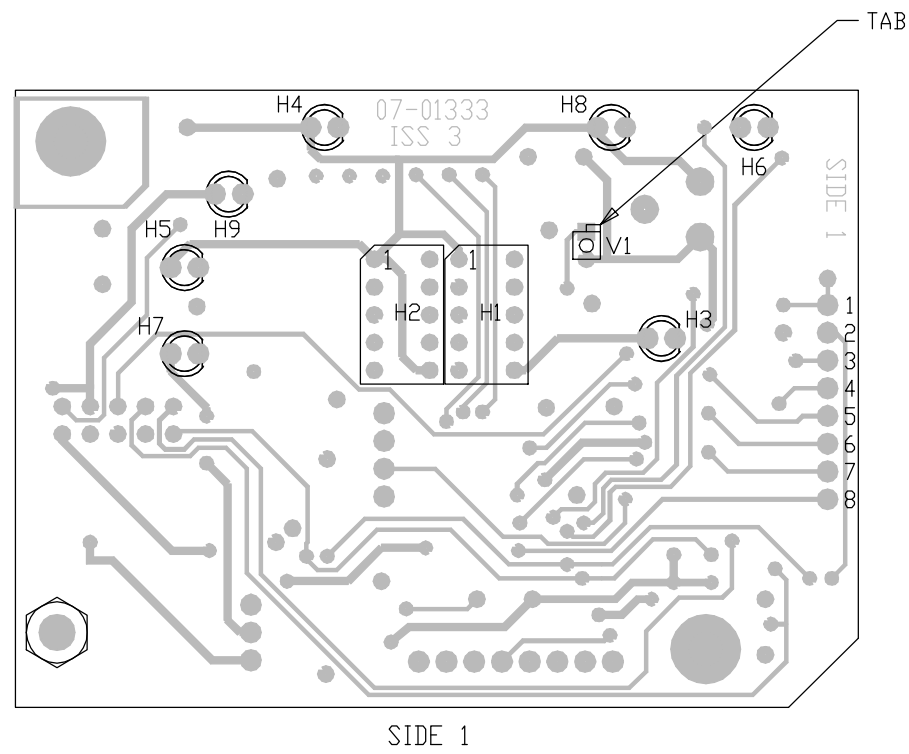
- NOTES
1. ALL DIODES ARE BAS16 (A6).
 2. ALL TRANSISTORS ARE BCX20 (U2).
 3. ORDER OF ASSEMBLY MUST BE:-
 - A. FIT ALL SURFACE MOUNT COMPONENTS.
 - B. FIT ALL OTHER COMPONENTS.

PCB 07-01332 ISSUE 3
 ASSY P/No. 08-03944-001

CHANGE REQUEST	
ISSUE B	R34 WAS 4k7
C/R 22128	14-9-89 NJA
ISSUE 2	P3 WAS J1
C/R 22142	27-10-89 NJA
ISSUE 3	H1 & H2
TRANSPOSED.	C/R 22253
20-12-89	NJA
ISSUE 4	P3 CHANGED
C/R 22300	15-3-90
PCB WAS ISS. 1	BOTTOM L/H CNR
WAS 90 deg.	C/R 22200
14-4-90	NJA
ISSUE 5	SMD LAND
PATTERNS	UPDATED.
PCB WAS ISS. 2	C/R 23135
BCL 30/4/93	

	DRN.	D.S	SCALE	COPYRIGHT © CODAN PTY LTD A.C.N. 007 590 605	
	CHKD.	NJA	DATE	DISPLAY BOARD ASSEMBLY	
MATERIAL	APPD.	NJA	4-7-89	DRAWING/DOC No.	
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A2 08-03944	
2 PLACES DEC			ISS		SHT
1 PLACE DEC			1		1
ANGULAR			2		
			3		
			4		
			5		

DO NOT SCALE



- NOTES
1. ALL DIODES ARE BAS16 (A6).
 2. ALL TRANSISTORS ARE BCX20 (U2).
 3. ORDER OF ASSEMBLY MUST BE:-
A. FIT ALL SURFACE MOUNT COMPONENTS.
B. FIT ALL OTHER COMPONENTS.

PCB 07-01333 ISSUE 3
ASSY P/NO. 08-03945-001

ISSUE B
R34 WAS 4K7
C/R 22128
14-9-89 NJA

ISSUE 2
H1 & H2
TRANSPOSED
C/R 22253
20-12-89 NJA

ISSUE 3
BOTTOM LH
CNR WAS 90 deg
R36 MOVED
PCB WAS ISSUE 1
C/R 22201
11-4-90 NJA

ISSUE 4
SMD RESISTORS &
CAP, FOOTPRINTS
MODIFIED.
C/R 23135
C7 & C8 ADDED,
PCB WAS ISSUE 2
C/R 23377
31-7-92 NJA

ISSUE 5
R2 WAS 470
C/R 23504
14-12-92 GW

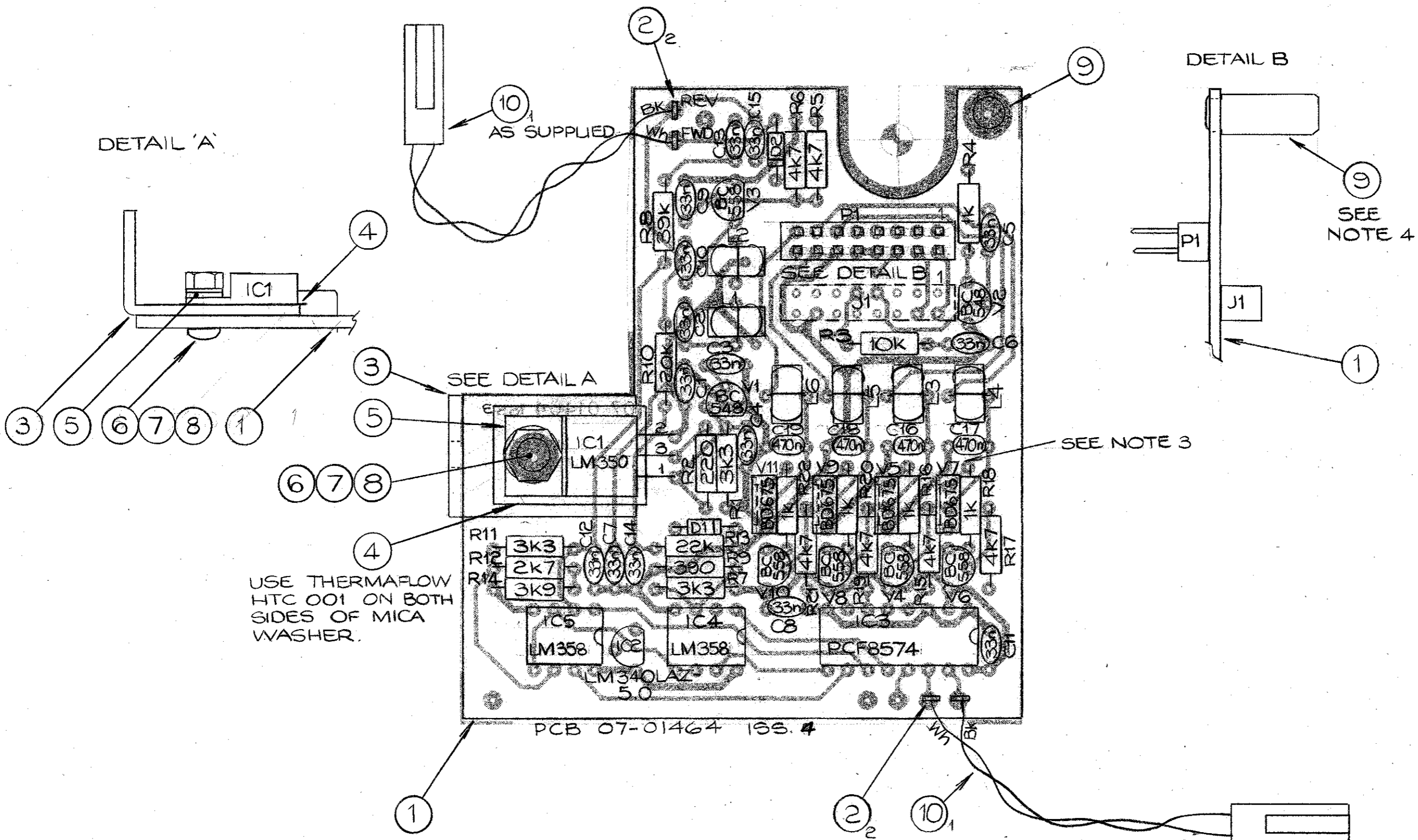
FILE No.
08\03945_5.DWG

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	DRN	OS		DATE 30-06-89
	CHKD	NJA		07-07-89
MATERIAL	APPD	NJA	14-09-89	
FINISH	TOLERANCES UNLESS OTHERWISE STATED		DRAWING/DOC NO. 08-03945	
	2 PLACES DEC.	±0.25		
	1 PLACE DEC.	±0.5		
0 PLACE DEC. ±1			A2 ISS 5 SHT. 1 OF 1	
ANGULAR ±2°				

DIMENSIONS IN mm

DO NOT SCALE

ISSUE B
PCB WAS 155.1
C/R. 22879
18-6-91 *MH*



DETAIL 'A'

DETAIL B

USE THERMAFLOW
HTC 001 ON BOTH
SIDES OF MICA
WASHER.

PCB 07-01464 155.4

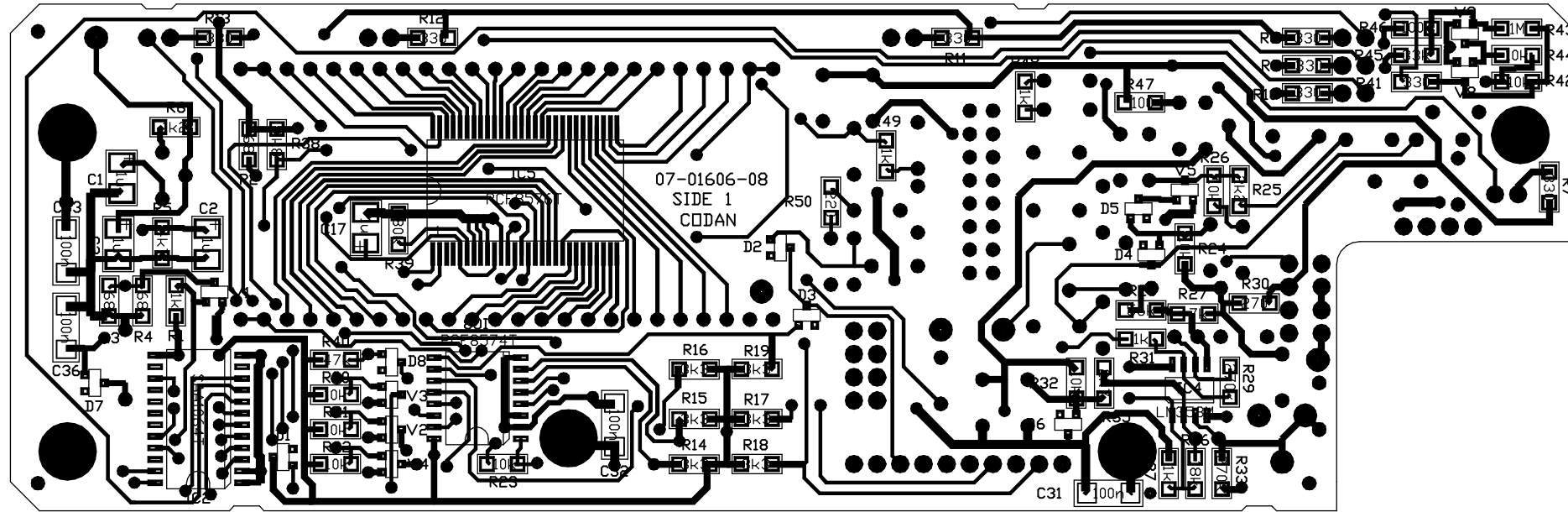
NOTES:

1. DIODES, D1 & D2, ARE BAW62 OR EQUIVALENT.
2. INDUCTORS, L1-L6, ARE 44-80044.
3. TRANSISTORS, V5, V7, V9, V11 ARE FITTED SO METAL PLATE FACES REGULATOR, IC1
4. ITEM ⑨ SWAGED WITH DIE COMBINATION 7/PA

CUT CABLE TO 70mm
BEFORE FITTING

		SCALE 2:1	TITLE ANTENNA DRIVER		COPYRIGHT © CODAN 19	
		DATE 13-9-90	DRAWING / DOC NO. 08-04285			
MATERIAL	DRN. CG	CHKD. <i>MH</i>	DATE 13-10-90	ISS A/B 1		
FINISH	APPD. <i>BH</i>	DATE 19-10-95	TOLERANCES UNLESS OTHERWISE STATED		SHT 1 OF 1	
			2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±			

08-04285-001	AS DRAWN
ASSEMBLY NO	



SIDE 1
SURFACE MOUNT COMPONENTS ONLY

- NOTES:-
 1. ALL DIODES ARE BAS16.
 2. ALL TRANSISTORS ARE BCX20.

PCB 07-01606-08
 ASSY P/No. 08-04666-001

CHANGE REQUEST

ISSUE B
 C30-C36 ADDED
 PCB WAS ISS 2
 C/R 23377
 NJA 05-08-92

ISSUE 2
 R33 WAS 390k.
 R36 WAS 10k.
 C/R 24093
 CM 11-01-95

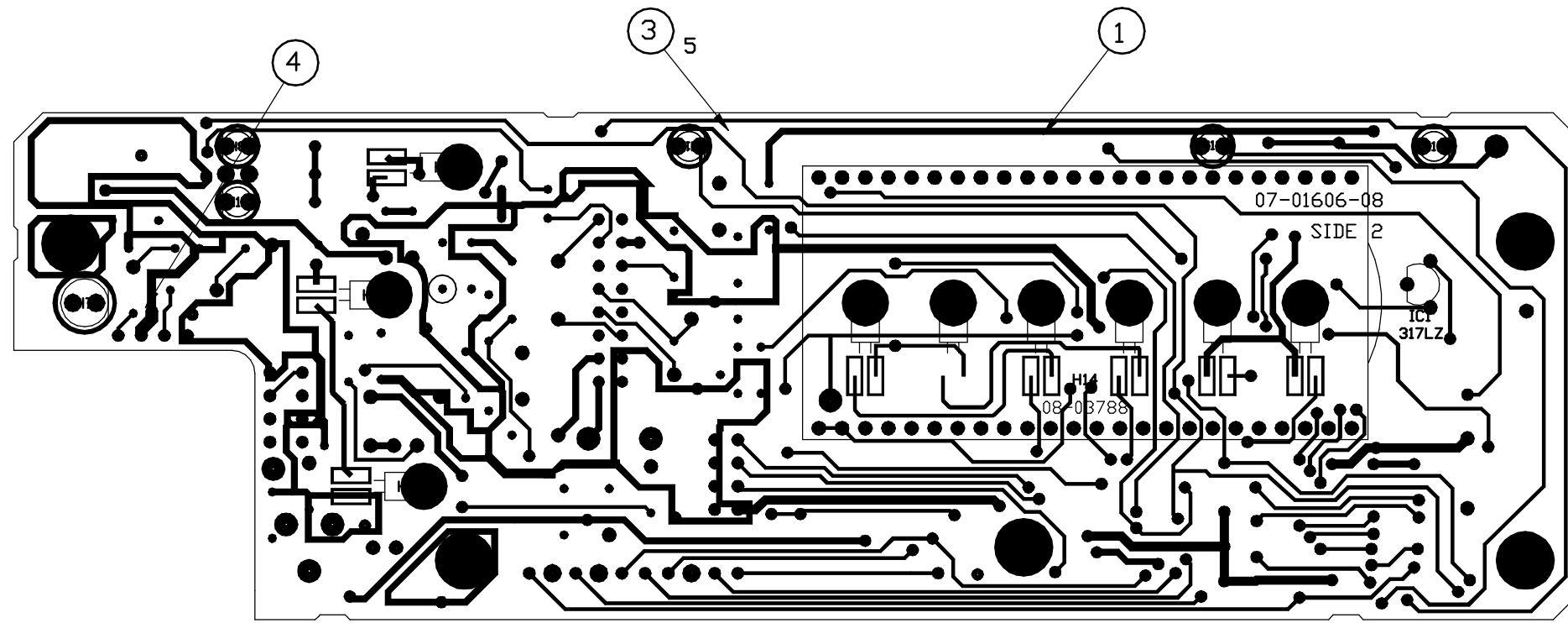
ISSUE 3
 PCB WAS ISS 5.
 C/R 24227
 CM 14-06-95

ISSUE 4
 REFER SHEET 2.
 C/R 24515
 CM 27-3-96

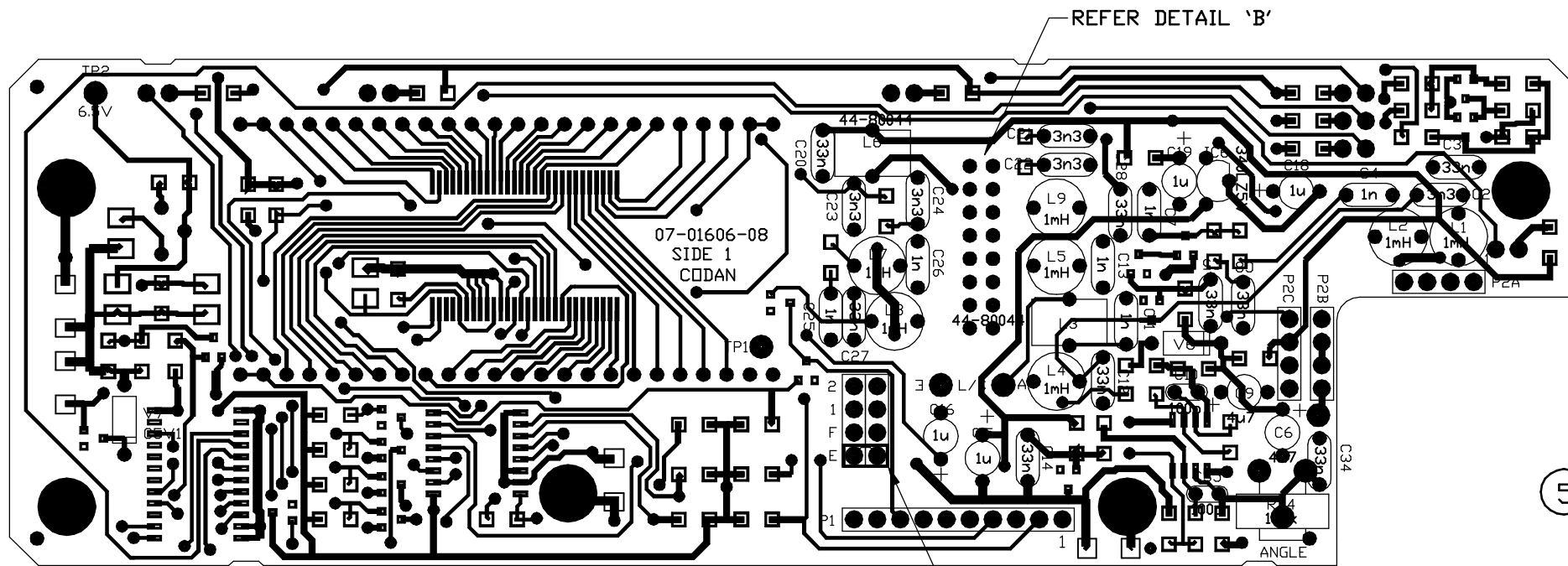
ISSUE 5
 C/R 24904
 REFER SHEET 2.

FILE No.
 08\04666_5.DWG

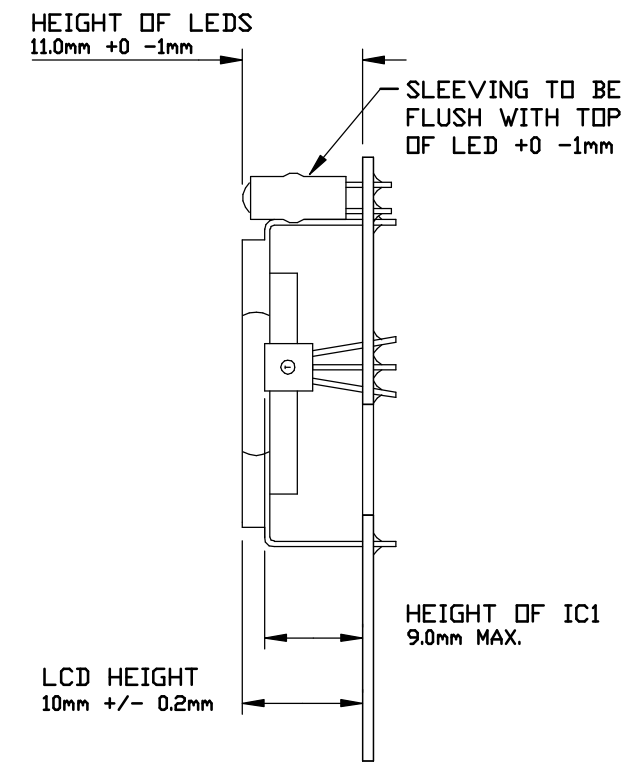
			SCALE 2:1	© CODAN PTY LTD, A.C.N. 007 590 605 1996 TITLE	
	DRN	CS/MS	DATE 19-2-91	DISPLAY PCB ASSEMBLY	
	CHKD	NJA	02-07-91	DRAWING/DOC NO. 08-04666	
MATERIAL	APPD	CM	19-10-93	A2 ISS	
FINISH			TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR		3 4 5
					SHT. 1 OF 2



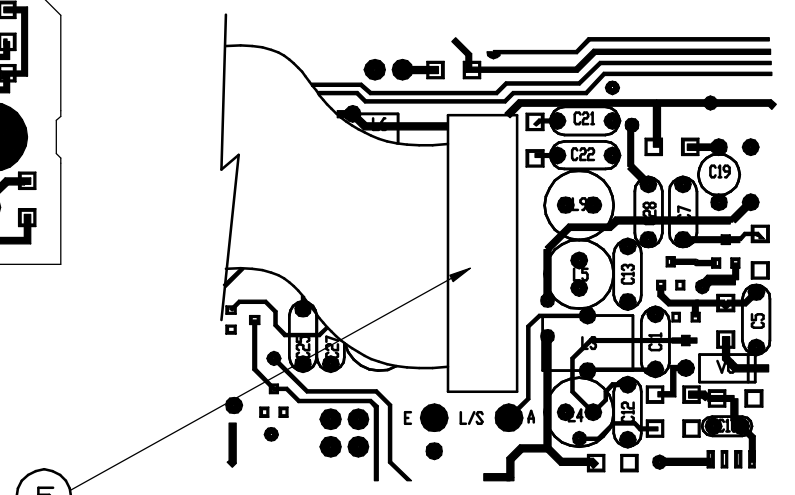
SIDE 2



SIDE 1



DETAIL 'A'



DETAIL 'B'

NOTES:
ORDER OF ASSEMBLY MUST BE:-

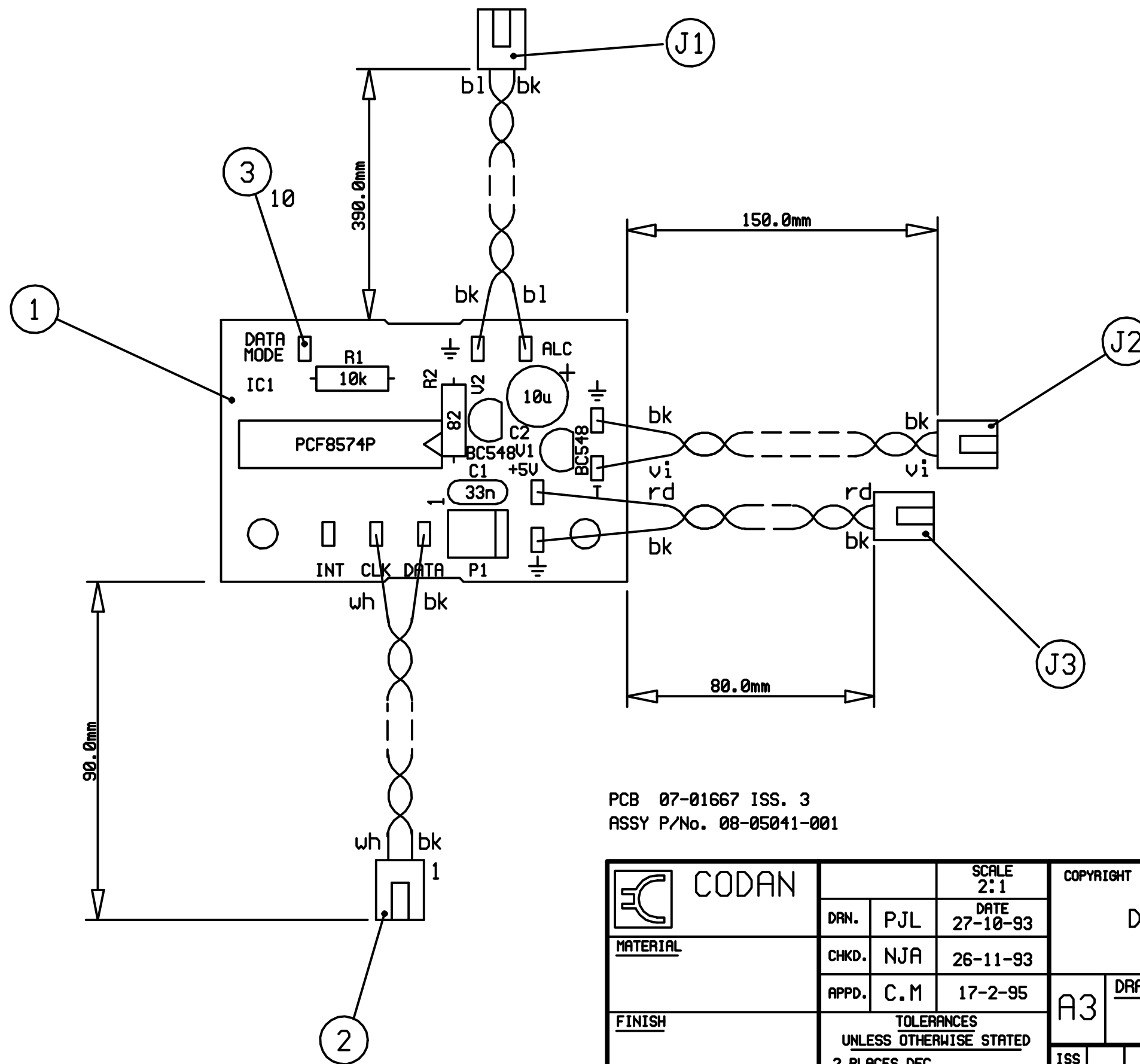
- a. FIT ALL SURFACE MOUNT COMPONENTS.
- b. FIT ALL OTHER COMPONENTS ON SIDE 1 (EXCEPT ITEM 5).
- c. FIT H1-H6, D15-17. ENSURE FILAMENT IS IN THE MIDDLE OF THE SILVER AREA AND THE LEADS DO NOT OVERHANG EDGE OF PADS.
- d. INSPECTION
- e. FIT DISPLAY H14 AS SHOWN.
- f. FIT ALL LEDS WITH SLEEVE AS SHOWN.
- g. FIT ITEM 5.
- h. INSPECT DISPLAY.

CHANGE REQUEST
ISSUE B C30-C36 ADDED PCB WAS ISS 2 C/R 23377 NJA 05-08-92
ISSUE 2 R33 WAS 390k. R36 WAS 10k. C/R 24093 CM 11-01-95
ISSUE 3 PCB WAS ISS 5. C/R 24227 CM 14-06-95
ISSUE 4 ITEM 5 ADDED. C/R 24515 20-02-96 JFB
ISSUE 5 C/R 24904 L1,L2,L4,L5,L7,L8 L9 TYPE CHANGE PCB WAS ISS. 7 17-6-97

PCB 07-01606-08
ASSY P/No. 08-04666-001

FILE NAME
08\04666_5.DWG

	DRN	CS/MS	SCALE	© CODAN PTY LTD, A.C.N. 007 590 605. 1996	
	CHKD	NJA	DATE	TITLE	
MATERIAL	APPD	CM	19-10-93	DISPLAY PCB ASSEMBLY	
FINISH	TOLERANCES UNLESS OTHERWISE STATED			DRAWING/DOC NO.	
	2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR			A2	08-04666
			ISS	3	4
				5	SHT. 2 OF 2



PCB 07-01667 ISS. 3
 ASSY P/No. 08-05041-001

CHANGE REQUEST

ISSUE B
 R2 ADDED.
 C2 WAS 47u.
 C/R 24080:
 EJ 08-12-94

ISSUE 2
 J1, J2, J3 ADDED
 C/R 24319
 4-9-95 NJA

ISSUE 3
 LENGTH INCREASED
 TO 390mm
 C/R 24421
 CM 8-11-95

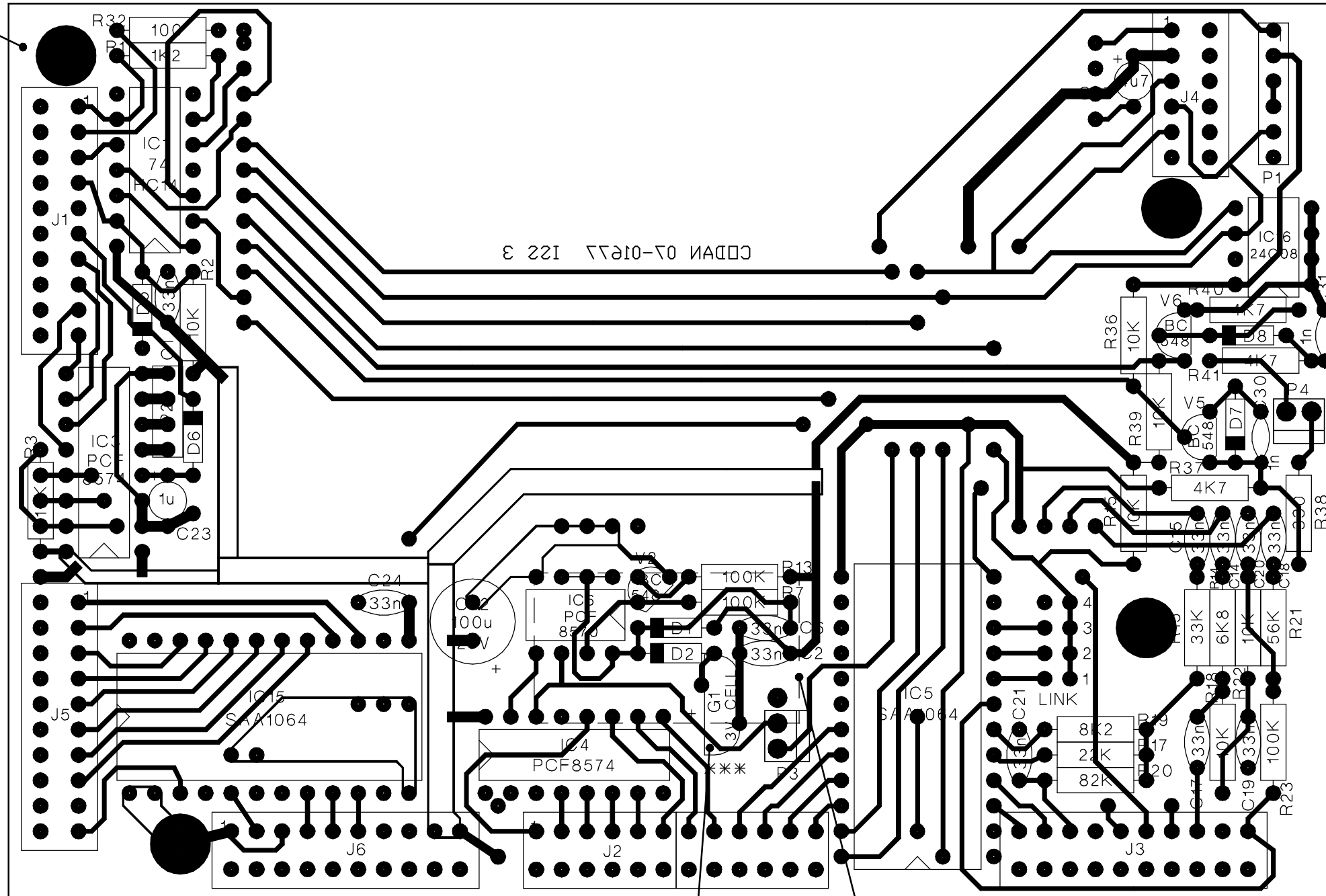
ISSUE 4
 COMPONENT VALUES
 ADDED.
 C/R 24407
 WIRE COLOURS
 TERMINATING AT
 J1 - REVERSED.
 C/R 24458
 CM 29-1-96

DISK FILE
 05041__4

	SCALE 2:1		COPYRIGHT © CODAN PTY LTD A.C.N. 007 590 605		
	DRAWN. P.J.L.	DATE 27-10-93	DATA MODE SWITCH ASSEMBLY		
	CHECKED. N.J.A.	DATE 26-11-93			
MATERIAL		APPD. C.M.	DATE 17-2-95	DRAWING/DOC No. 08-05041	
FINISH		TOLERANCES UNLESS OTHERWISE STATED		A3	ISS
		2 PLACES DEC 1 PLACE DEC ANGULAR			

DO NOT SCALE

21



PCB 07-01677 ISSUE 3

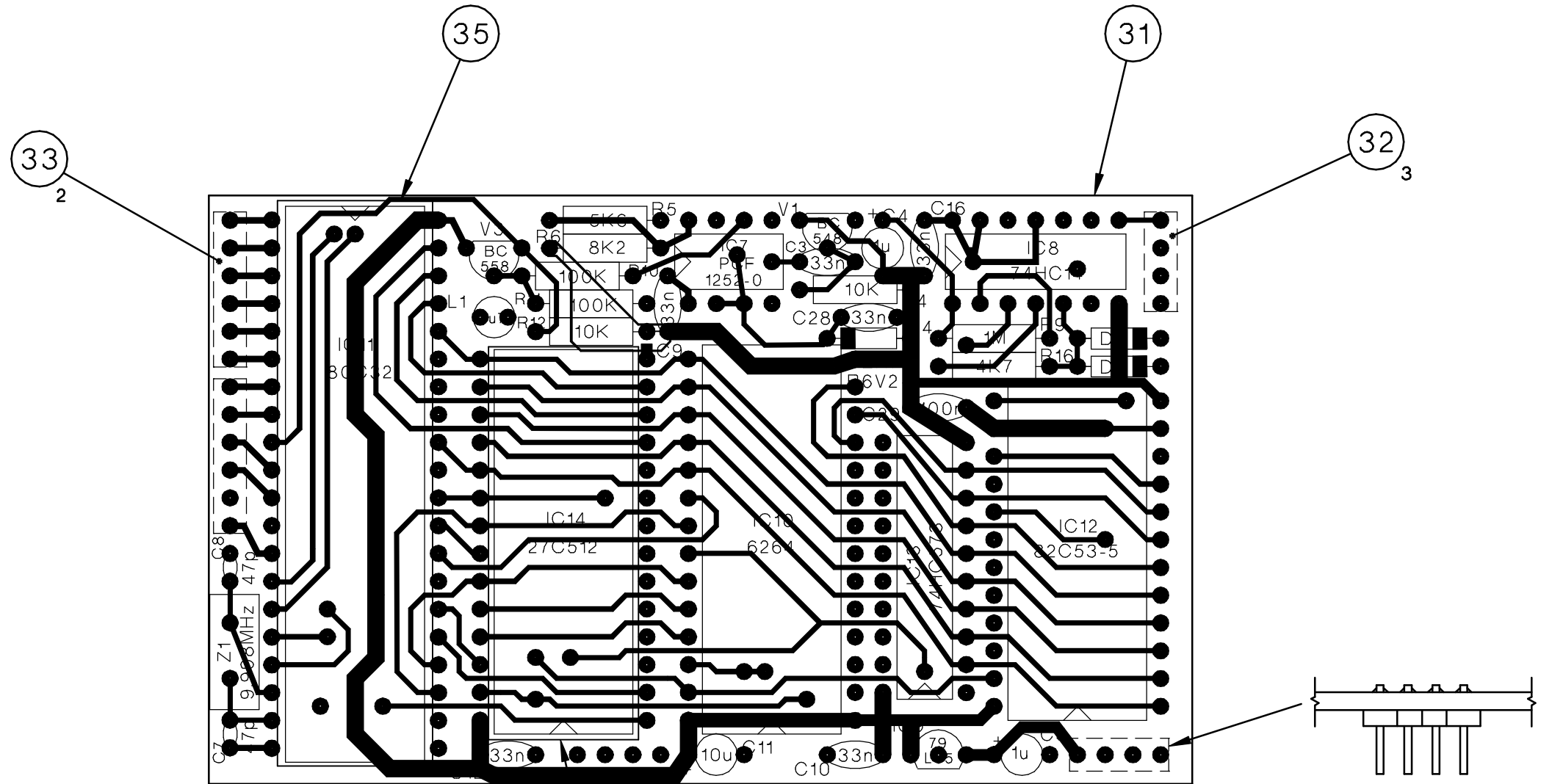
FILE NAME
08\05088_1.DWG

NOTES;

1. ALL DIODES BAW62 OR EQUIVALENT
- CAUTION** 2. xxx 3 VOLT CELL MUST BE FITTED LAST MANUALLY.
3. FIT ITEM (23) OVER G1.
4. FIT ITEM (22) UNDER PCB AS SHOWN.

	SCALE 2:1		© CODAN PTY LTD, A.C.N. 007 590 605: 1997	
	DRN	ILT	TITLE MICROPROCESSOR INTERFACE	
MATERIAL	CHKD	NJA	DRAWING/DOC NO. 08-05088	
FINISH	APPD	CM	A3	
	TOLERANCES UNLESS OTHERWISE STATED		ISS	
2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR		1		SHT. 1 OF 1

DO NOT SCALE



PCB 07-01242 ISS. 6

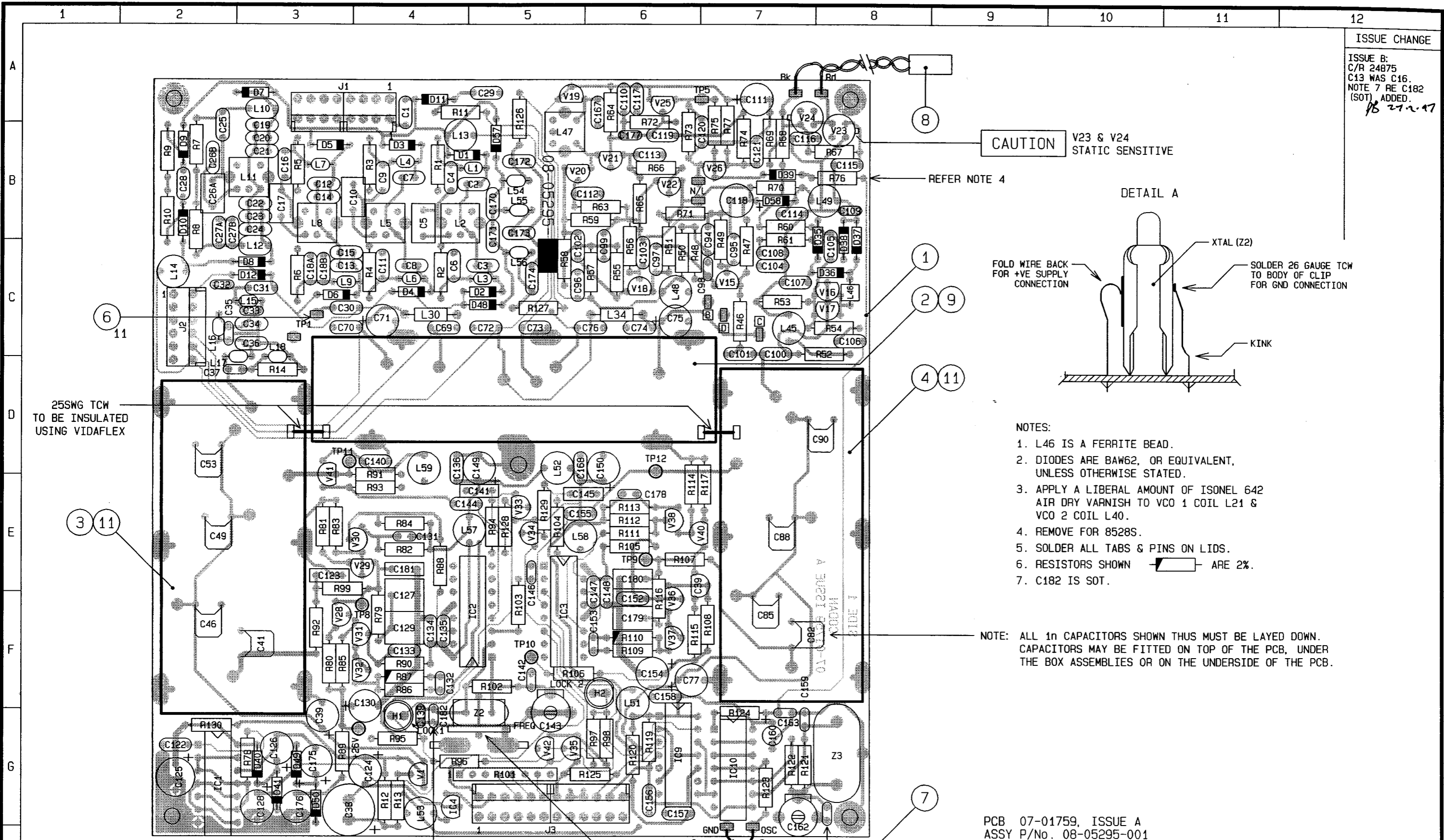
WAFERS MOUNTED
ON UNDERSIDE OF
PCB & TOP SOLDERED

WARNING
THIS ASSEMBLY CONTAINS
ELECTRO-STATIC SENSITIVE DEVICES

FILE NAME
08\05089_1.DWG

			SCALE	© CODAN PTY LTD, A.C.N. 007 590 605: 1997 TITLE MICROPROCESSOR ASSY.			
	DRN	ILT	DATE	17-3-94			
MATERIAL	CHKD	NJA	DATE	21-3-94			
	APPD	CM	DATE	1-6-94			
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A3		DRAWING/DOC NO. 08-05089	
	2 PLACES DEC. 1 PLACE DEC. 0 PLACE DEC. ANGULAR			ISS			SHT. 1
				1			OF 1

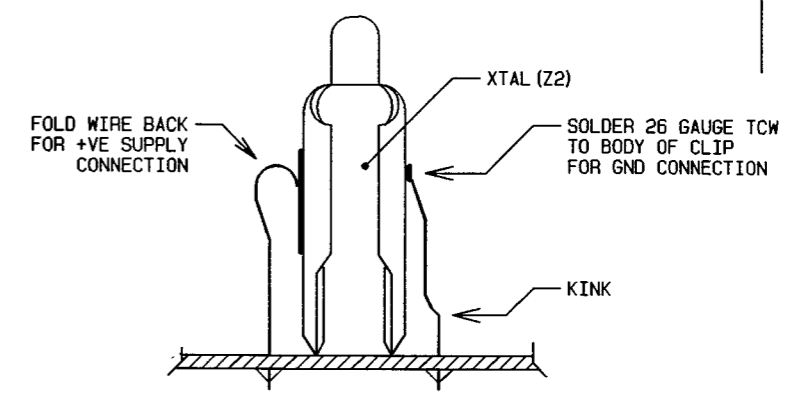
ISSUE B:
C/R 24875
C13 WAS C16.
NOTE 7 RE C182
(SOT) ADDED.
JB 27.2.97



CAUTION V23 & V24
STATIC SENSITIVE

REFER NOTE 4

DETAIL A



NOTES:

1. L46 IS A FERRITE BEAD.
2. DIODES ARE BAW62, OR EQUIVALENT, UNLESS OTHERWISE STATED.
3. APPLY A LIBERAL AMOUNT OF ISONEL 642 AIR DRY VARNISH TO VCO 1 COIL L21 & VCO 2 COIL L40.
4. REMOVE FOR 8528S.
5. SOLDER ALL TABS & PINS ON LIDS.
6. RESISTORS SHOWN ARE 2%.
7. C182 IS SOT.

NOTE: ALL 1n CAPACITORS SHOWN THUS MUST BE LAYED DOWN.
CAPACITORS MAY BE FITTED ON TOP OF THE PCB, UNDER THE BOX ASSEMBLIES OR ON THE UNDERSIDE OF THE PCB.

PCB 07-01759, ISSUE A
ASSY P/No. 08-05295-001

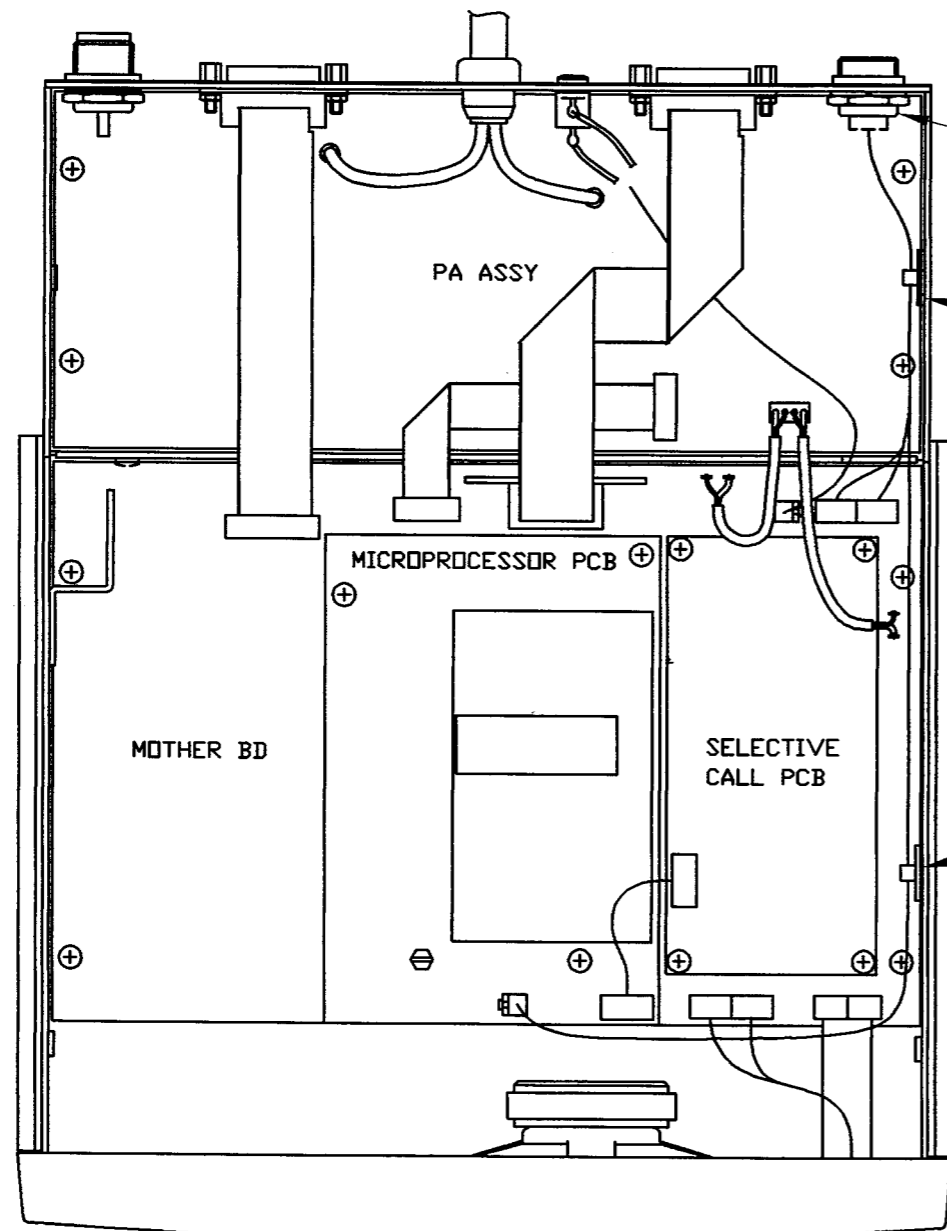
REFER NOTE 7.

REFER DETAIL A

	ORN. C G CHKD. NJA APPD. JB	SCALE 2:1 DATE 1-10-96 11-4-97	© CODAN PTY LTD, A.C.N. 007 590 605, 1996 RF MIXER & DUAL SYNTHESISER PCB ASSEMBLY - REFERENCES
	MATERIAL FINISH	TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±	DRAWING/DOC No. 08-05295
	ISS 1	SHIT 2 OF 2	

DO NOT SCALE

IF COMPONENTS ARE NOT ALREADY FITTED,
REMOVE RF MIXER & DUAL SYNTHESISER,
INSERT COMPONENTS AS SHOWN & SOLDER,
REPLACE PCB.
REF HANDBOOK CIRCUIT 04-02086 OR
04-02453.



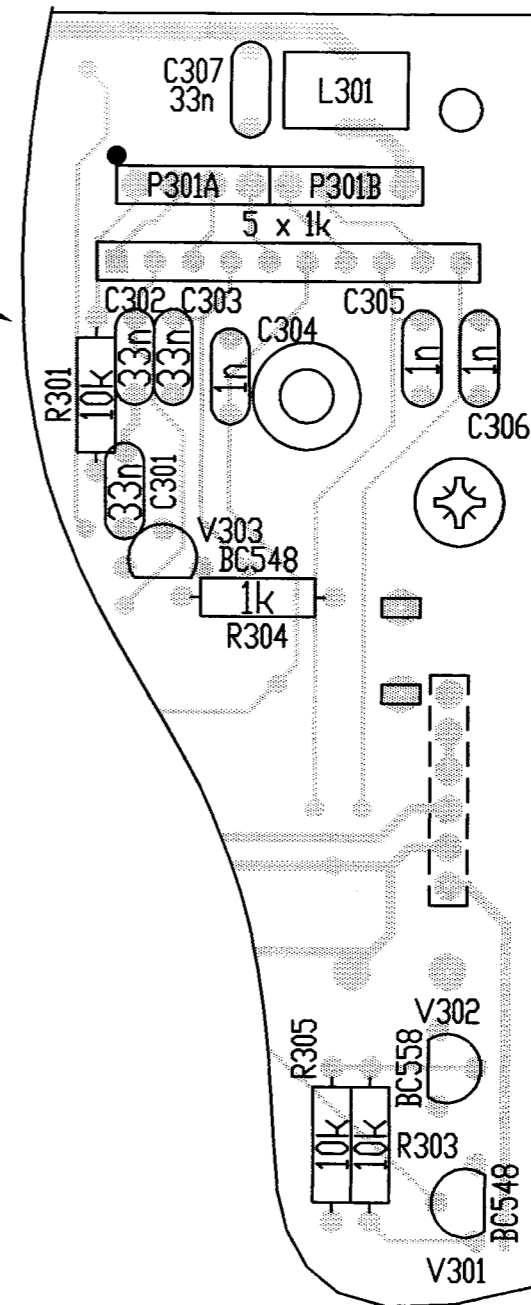
42

FIT CABLE
8 WAY: 08-03232 OR
10 WAY: 08-05091-001
AS REQ'D.

41

41

ONLY FOR
10 WAY CABLE



ISSUE B
C/R 21009

ISSUE C
C/R 21023

ISSUE D
C/R 21063

ISSUE E
21140

ISSUE 2
ITEM No's CHANGED.
C/R 21257
9-4-87 NJA

ISSUE 3
R305 ADDED.
C/R 21333
24-7-87 NJA

ISSUE 4
04 No ADDED.
C/R 21906
14-9-89 NJA

ISSUE 5
ORIENTATION OF
STAKES CHANGED.
C/R 24258
20-7-95 NJA

ISSUE 6
NOTE CHANGED.
C/R 24337
17-8-95 NJA

ISSUE 7
NOTE ADDED TO
ITEM 42.
C/R 24449
SLH 11-3-96

FILE No.
10271_7

	SCALE NTS		© CODAN PTY LTD, A.C.N. 007 590 605 1995	
	DRN	BLW	DATE 5-6-86	TITLE FITTING INSTRUCTIONS OPTION PS
MATERIAL	CHKD	NJA	6-6-86	DRAWING/DOC NO. 15-10271-001
	APPD	NJA	30-10-86	
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A3
	2 PLACES DEC.	±0.25	ISS	
1 PLACE DEC.	±0.5	7		
0 PLACE DEC.	±1			
ANGULAR	±2			

DO NOT SCALE

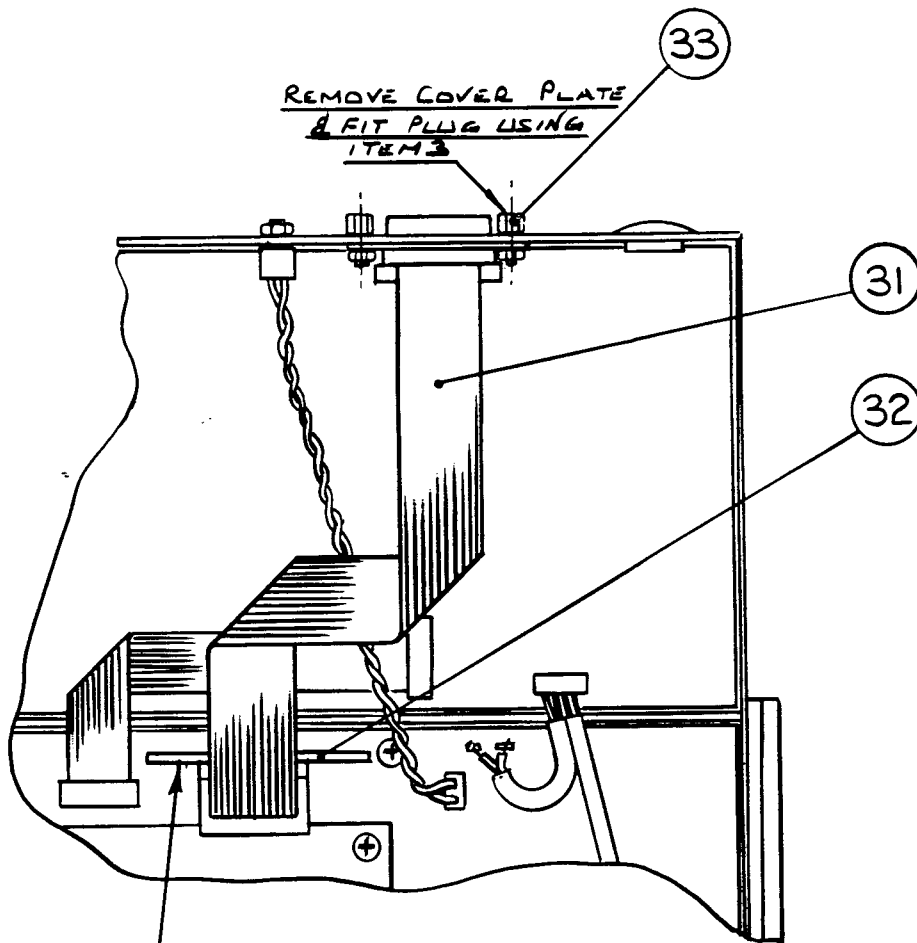
B. 21140

ISSUE 2




ITEM No's CHANGED

C/R 21257

9-4-87 *MM*

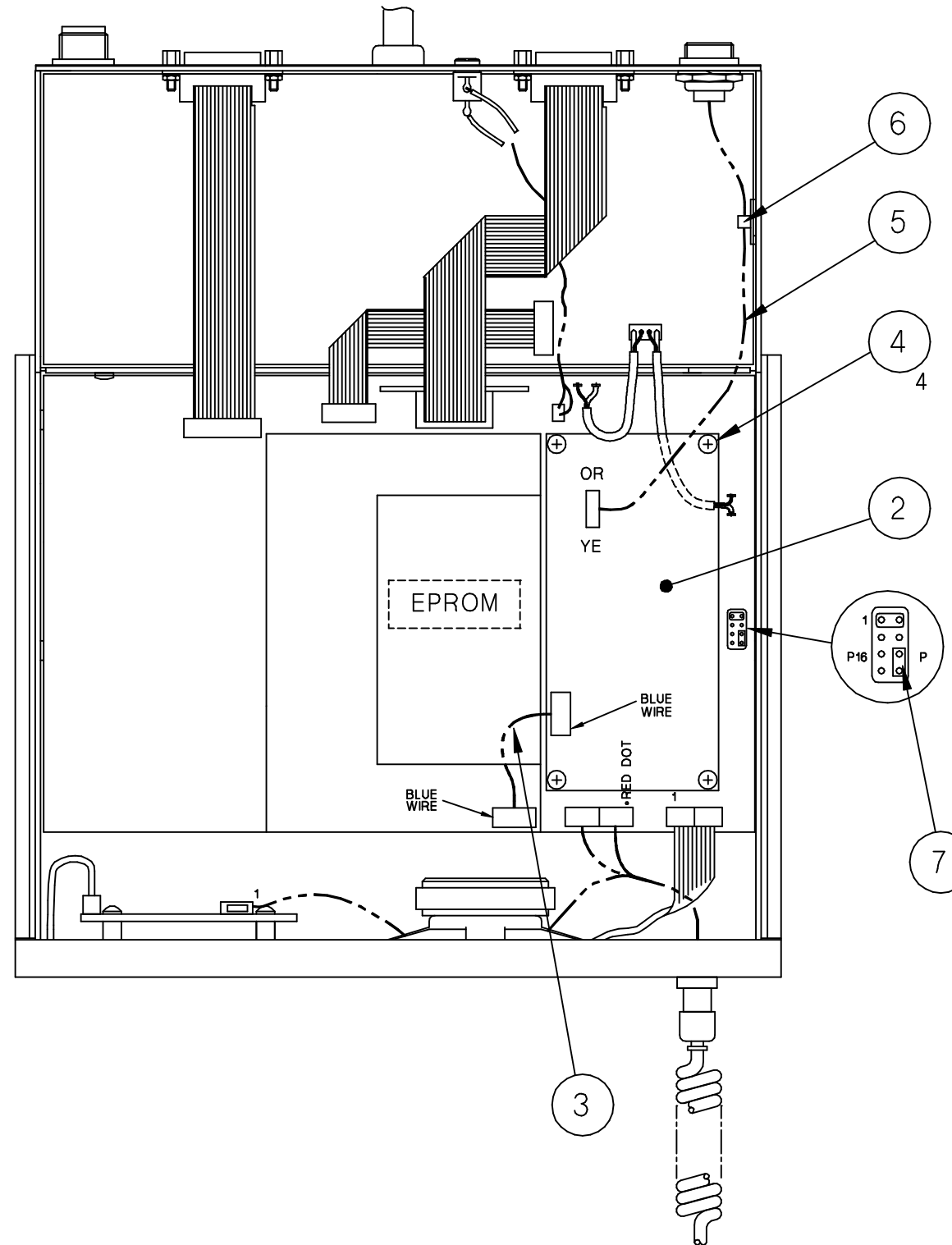


LOCATE & SOLDER PCB ITEM 2
IN POSITION SHOWN.

 CODAN	 		SCALE NTS	COPYRIGHT © CODAN 19 TITLE <u>OPTION R</u>	
	DRN. <i>BLW</i>	DATE 16-5-86	SCALE NTS		
MATERIAL _____	CHKD. <i>MM</i>	DATE 5-6-86	DRAWING/DOC NO. A4 15-10272-001		
FINISH _____	APPD. <i>MM</i>	DATE 30-10-86			
TOLERANCES UNLESS OTHERWISE STATED			ISS 12	SHT / OF 1	
2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±					

DO NOT SCALE

ITEM	PART No.	DESCRIPTION
1	15-10274-001	FITTING INSTRUCTIONS
2	08-03300	SELECTIVE CALL SDE SDEM
3	08-03331	LOOM SELECTIVE CALL
4	31-23006-501	SCREW M3x6 PAN POZI
5	08-03332	LOOM EXTERNAL ALARM
6	30-05102-001	CLAMP CABLE
7	60-90410-001	JUMPER



NOTES:

1. REMOVE BOTTOM COVER.
2. WITH THE PCB (ITEM 2) IN THE CORRECT ORIENTATION, ALIGN WITH THE PLUG ON THE MOTHERBOARD. PUSH THE PCB (ITEM 2) DOWN UNTIL IT LOCATES ON THE SPACERS. SECURE USING THE 4 SCREWS (ITEM 4).
3. CONNECT THE SELECTIVE CALL PCB (ITEM 2) TO THE MICRO PROC. PCB USING ITEM 3. ENSURE CORRECT ORIENTATION OF SOCKETS.
4. CHECK ISSUE No. OF EPROM (TO BE AT LEAST 2.2).
5. REMOVE PLUG BUTTON FROM REAR PANEL.
6. REMOVE THE NUT & WASHER FROM PLUG END OF CABLE (ITEM 5). PASS THE SOCKET END OF THIS CABLE THROUGH THE HOLE IN THE BACK PANEL & LOCATE THE PLUG IN THE HOLE, REPLACE THE NUT & WASHER. CONNECT THE CABLE TO THE SELECTIVE CALL PCB (ITEM 2) AS SHOWN. SECURE CABLE TO THE SIDE BRACKET USING ITEM 6.
7. FIT JUMPER (ITEM 7) TO P16 ON MOTHER PCB AT "P" FOR SHORT PREAMBLE OR POSITION "1" FOR LONG PREAMBLE IN SCANNING SYSTEMS.
8. TEST FOR CORRECT OPERATION (SEE HANDBOOK IF REQUIRED).
9. REPLACE BOTTOM COVER.

FILE No.
15\10274__1.DWG

DIMENSIONS IN mm

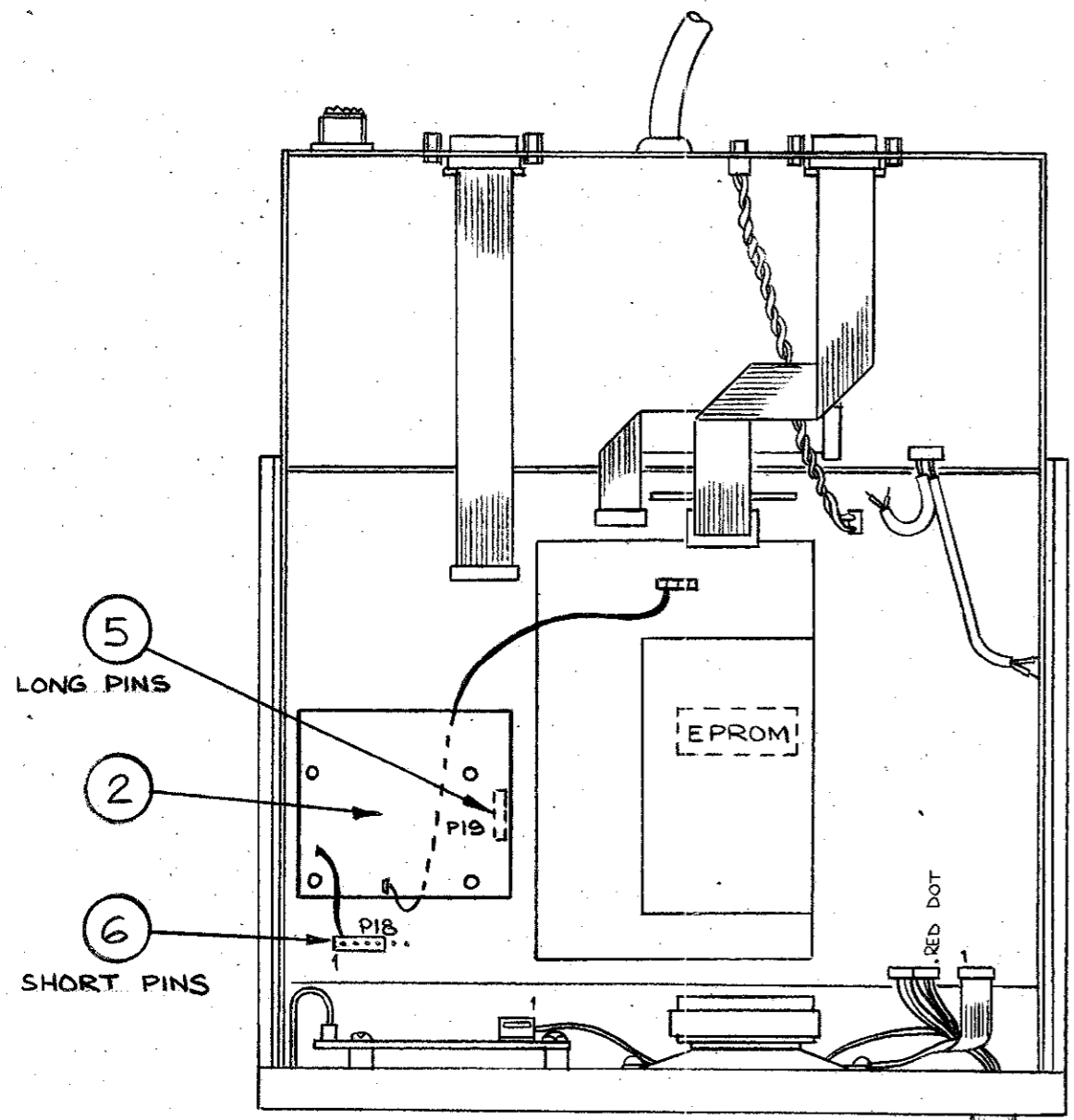
			SCALE NTS	© CODAN PTY LTD, A.C.N. 007 590 605: 2000 TITLE	
	DRN	APJ	DATE 5-2-87	OPTION SDE 8525	
MATERIAL	CHKD	NJA	DATE 9-2-87	DRAWING/DOC NO. 15-10274-001	
	APPD	NJA	DATE 10-2-87		
FINISH	TOLERANCES UNLESS OTHERWISE STATED			A3	ISS 1
	2 PLACES DEC. 1 PLACE DEC. ±0.5 0 PLACE DEC. ±1				

DO NOT SCALE

2. CIR. 21367
22-3-88 *g/b*

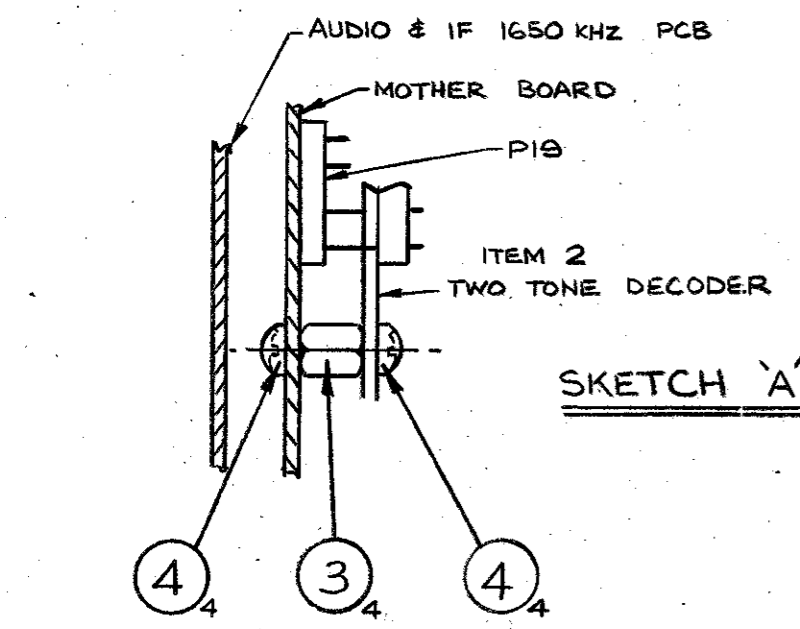
ISSUE 3
TWO UNUSED HOLES ADDED TO P18.
CIR 23793
bu 1-12-93

ITEM	PART N°	DESCRIPTION
1	15-10276-001	FITTING INSTRUCTIONS
2	08-03273	TWO TONE DECODER
3	05-03312-090	SPACER
4	31-23006-501	SCREW M3 x 6
PI9	60-00041-102	PLUG 4 WAY
PI8	60-00041-100	PLUG 4 WAY



NOTES:

1. REMOVE TOP & BOTTOM COVER.
2. DISCONNECT & REMOVE AUDIO & IF PCB (08-03025)
3. SOLDER PI8 & PI9 IN POSITION SHOWN.
4. ASSEMBLE 4 SPACERS AS SHOWN IN SKETCH 'A'
5. WITH THE PCB (ITEM 2) IN THE CORRECT ORIENTATION ALIGN WITH THE PI9 ON THE MOTHER BOARD. PUSH THE PCB (ITEM 2) DOWN UNTIL IT LOCATES ON THE SPACERS. SECURE USING THE 4 SCREWS (ITEM 4)
6. CONNECT THE TWO SOCKETS AS SHOWN ONE TO THE MOTHER BOARD, THE OTHER TO THE MICRO PROC. BOARD ENSURE CORRECT ORIENTATION OF SOCKETS.
7. REPLACE & RECONNECT THE AUDIO & IF PCB.
8. TO ENABLE TONE CALLING THE EPROM MUST BE PROGRAMMED AS REQUIRED.
9. TEST FOR CORRECT OPERATION (SEE HANDBOOK IF REQUIRED)
10. REPLACE TOP & BOTTOM COVERS.



SKETCH 'A'

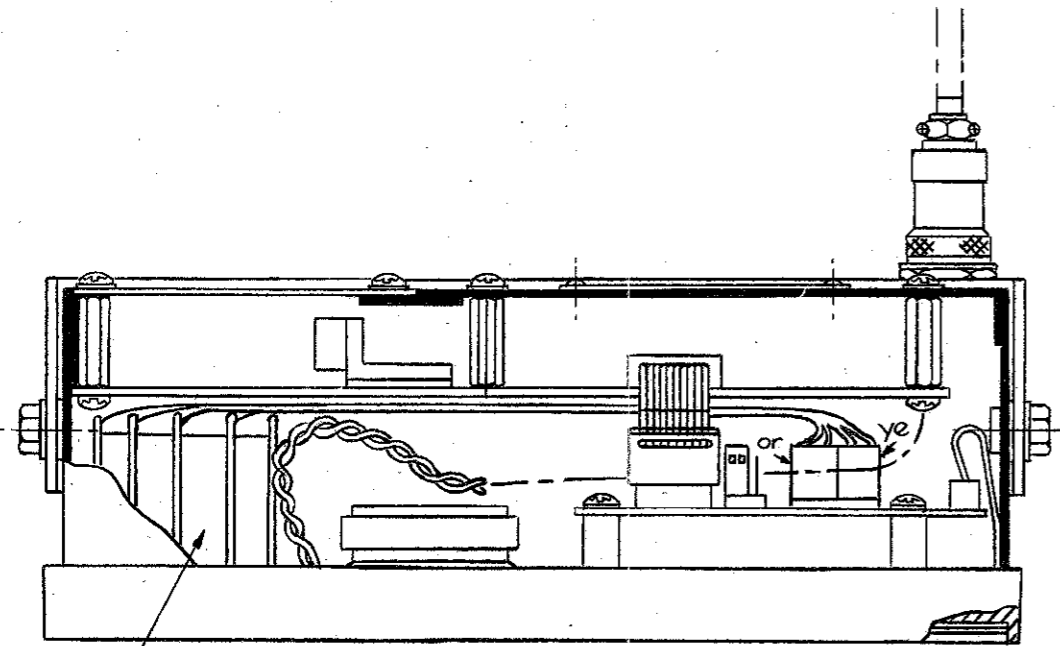
	SCALE		TITLE		COPYRIGHT © CODAN 1987
	DRN. APJ	DATE 5-2-87	OPTION TD		
MATERIAL	CHKD. <i>MM</i>	DATE 9-2-87	DRAWING DOC NO.		A3 15-10276-001
FINISH	APPD. <i>MM</i>	DATE 10-2-87	ISS		
TOLERANCES UNLESS OTHERWISE STATED			SHT		OF
2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±			X 2 3		

283

400

DO NOT SCALE

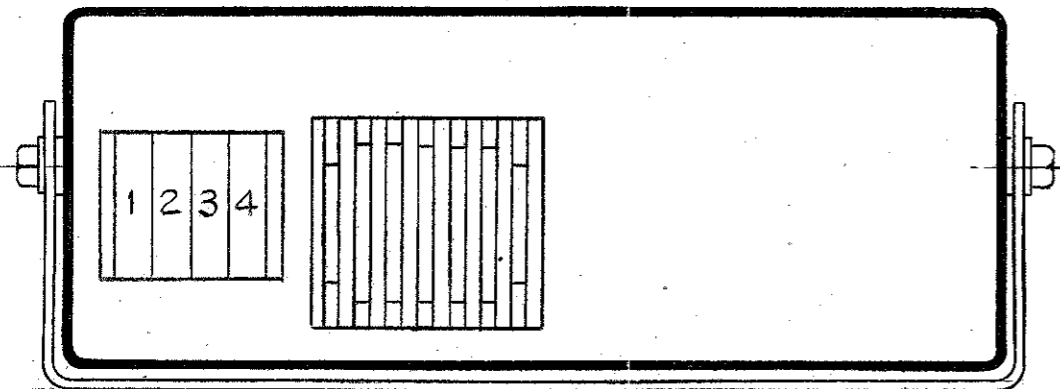
ITEM	PART No	DESCRIPTION
1	15-10282-001	FITTING INSTRUCTIONS
2	08-03301-004	SWITCH, MESH SELECTIVE CALL



2

NOTES:

1. REMOVE FRONT PANEL BY UNSCREWING THE FOUR COUNTERSUNK SCREWS IN THE SIDES.
2. DISCONNECT ALL WIRING BETWEEN FRONT PANEL & MIC AMP & INTERFACE PCB.
3. USING FLAT NOSE PLIERS BREAK OUT THE FOUR SUPPORTING BARS IN THE DIGI SWITCH HOLE AREA.
4. USING A SHARP TOOL CUT OUT THE SWITCH LAYER & ESCUTCHEON 'IMPORTANT' THIS MUST BE DONE FROM THE INSIDE.
5. FROM THE FRONT FILE USING FORWARD STROKES ONLY, CLEAN THE SWITCH LAYER ESCUTCHEON & CASTING TO THE CUTOUT SIZE IN THE CASTING. 'IMPORTANT' ENSURE THIS DOES NOT EXCEED THE CAST CUTOUT SIZE.
6. PASS THE CABLE OF THE DIGI SWITCH ASSEMBLY THROUGH THE CUTOUT AND CLIP THE SIDE PLATE INTO POSITION ENSURING THE DIGI SWITCHES CAN BE READ THE CORRECT WAY ROUND. PLUG THE CABLE FROM THE DIGI SWITCHES INTO THE DISPLAY BOARD AS SHOWN. (LOOP EXCESS CABLE)
7. RECONNECT FRONT PANEL WIRING & PLUG. REPLACE FRONT PANEL USING EXISTING SCREWS.




FRONT VIEW

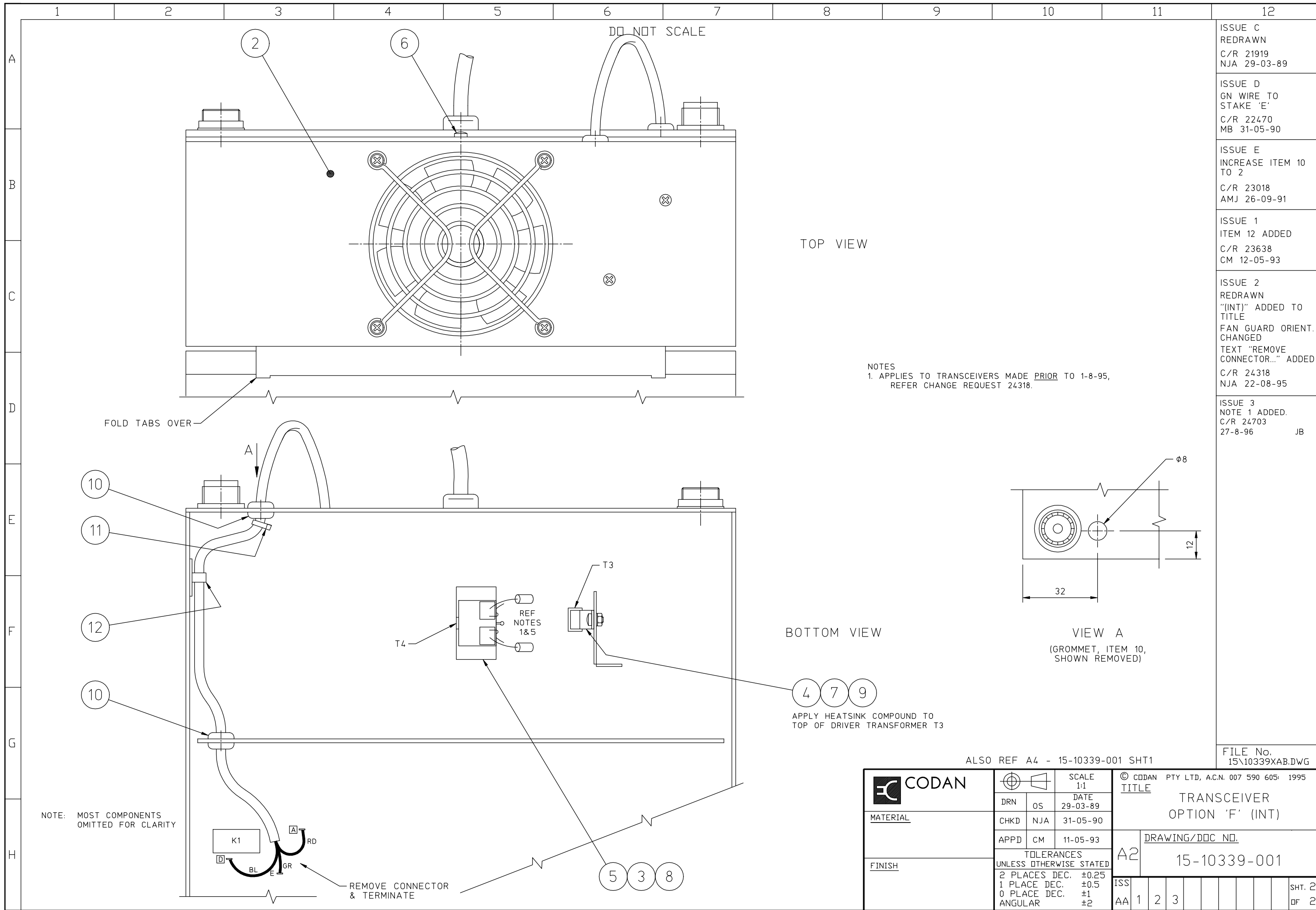
	SCALE		TITLE		COPYRIGHT © CODAN 19	
	DRN.	A.P.J	DATE	OPTION SM 8530		
MATERIAL	CHKD.	MJM	9-2-87	DRAWING DOC NO.		
FINISH	APPD.	MJM	10-2-87	A3 15-10282-001		
TOLERANCES UNLESS OTHERWISE STATED			ISS	SHT		
2 PLACES DEC ±			1	OF		
1 PLACE DEC ±						
ANGULAR ±						

FITTING INSTRUCTIONS TRANSCEIVER - OPTION F

(PA ASSEMBLY 08-03743 SERIES)

1. Obtain unfinished PA from current production batch and proceed to fit fan option as follows.
2. Secure existing resistor MTG PCB to top of O/P transformer heatsink with silastic and terminate 2 wires from T4 to PCB.
3. Drill out blind holes beneath T4 in PA heatsink $\varnothing 3.0$ (through PCB) and remove all swarf.
4. Apply heatsink compound to fully line inside surface of O/P transformer heatsink (3).
5. Fit O/P transformer (5) T4 to heatsink (3), with MTG base on underside of s/assy.
6. Place O/P transformer s/assy in position and trim wires to suit ensuring centre wire is long enough to just go through PA PCB and doesn't touch PA heatsink.
7. Remove s/assy and apply heatsink compound to base and secure to PA heatsink with screw (8).
8. Terminate wires to PA PCB and terminate 2 wire from T4 to resistor PCB.
9. Remove diode D15 for 100 watt CW operation (60 watts CW when fitted)
10. Apply heatsink compound to top of driver heatsink bracket (4).
11. Fit driver heatsink bracket (4) using screw and nut (7) and (9) ensuring bracket is placed squarely and firmly on top of T3.
12. Drill hole $\varnothing 8.0$ in rear panel as shown and fit grommet.
13. Fit fan/cover assembly (2) to top of PA heatsink using screw (6) and folding tabs over heatsink flange. Fit grommet to screen.
14. Fit cable through rear panel and screen.
15. Fit cable clamp and route cable as shown, fit cable tie, remove connector (leaving long leads) and solder ends as shown.

 CODAN	TRANSCEIVER OPTION F			DRG 15-10339-001	ISS 3	SHT 1 OF 2
	ORIG OS	DATE 11/4/89	CHKD	DATE 13/4/89	APPD CM	DATE 11/5/93



ISSUE C
REDRAWN
C/R 21919
NJA 29-03-89

ISSUE D
GN WIRE TO
STAKE 'E'
C/R 22470
MB 31-05-90

ISSUE E
INCREASE ITEM 10
TO 2
C/R 23018
AMJ 26-09-91

ISSUE 1
ITEM 12 ADDED
C/R 23638
CM 12-05-93

ISSUE 2
REDRAWN
"(INT)" ADDED TO
TITLE
FAN GUARD ORIENT.
CHANGED
TEXT "REMOVE
CONNECTOR..." ADDED
C/R 24318
NJA 22-08-95

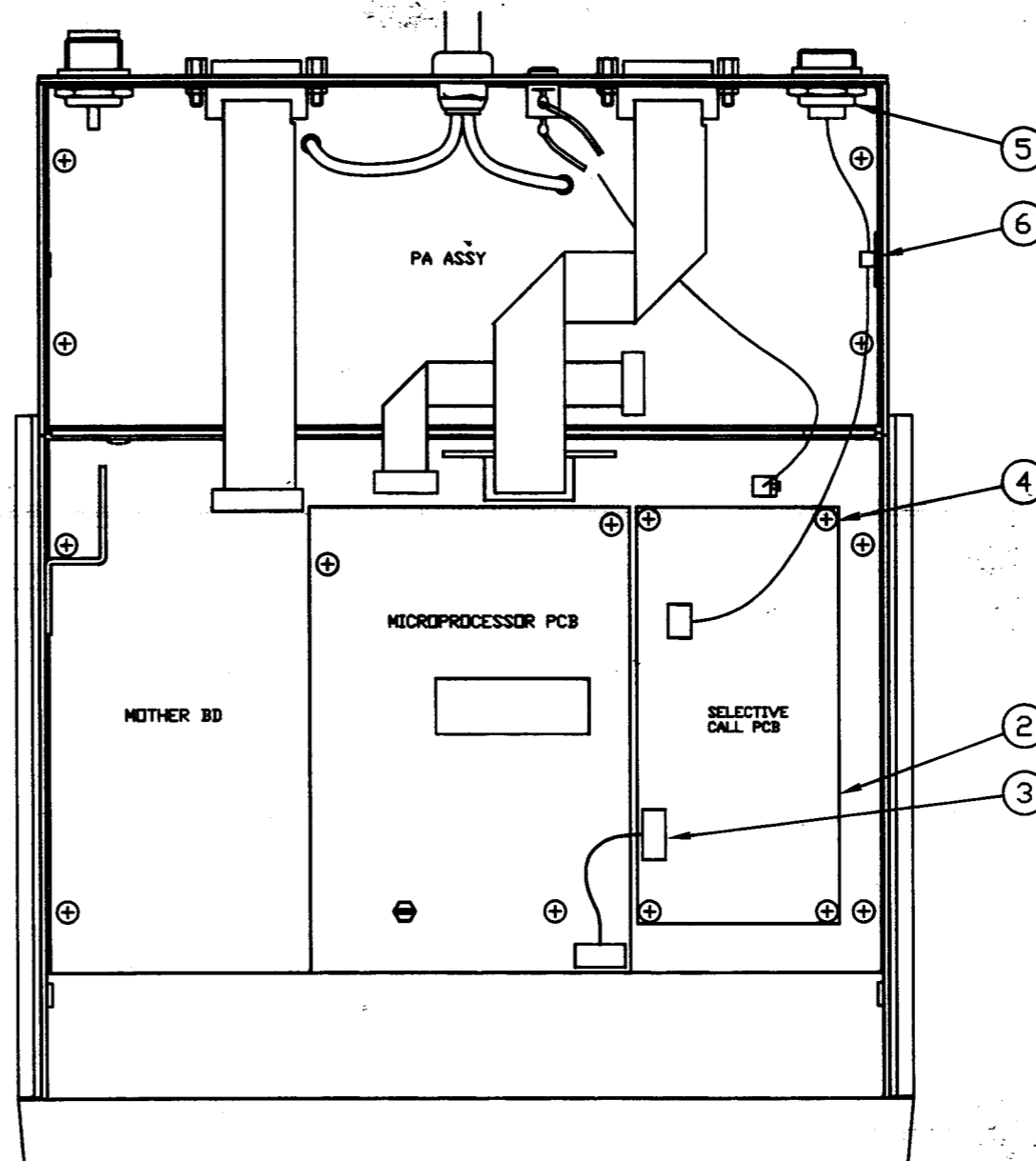
ISSUE 3
NOTE 1 ADDED.
C/R 24703
27-8-96 JB

ALSO REF A4 - 15-10339-001 SHT1

FILE No.
15\10339XAB.DWG

	SCALE 1:1		© CODAN PTY LTD, AC.N. 007 590 605 1995	
	DRN	OS	DATE 29-03-89	
	CHKD	NJA	31-05-90	
MATERIAL	APPD	CM	11-05-93	
TOLERANCES UNLESS OTHERWISE STATED			DRAWING/DOC NO.	
2 PLACES DEC. ±0.25			A2 15-10339-001	
1 PLACE DEC. ±0.5			ISS	
0 PLACE DEC. ±1			AA 1 2 3	
ANGULAR ±2			SHT. 2 OF 2	

REF	PART No	DESCRIPTION	QTY
1	15-10366-001	FITTING INSTRUCTIONS	1
2	08-03300-000	SELECTIVE CALL SD	1
3	08-03331	LOOM, SELECTIVE CALL	1
4	31-23006-501	SCREW M3x6 PAN POZI	4
5	08-03332	LOOM, EXTERNAL ALARM	1
6	30-05102-001	CLAMP, CABLE ADHESIVE BACKED	1






NOTES

1. REMOVE BOTTOM COVER.
2. WITH THE PCB (ITEM 2) IN CORRECT ORIENTATION, ALIGN WITH THE PLUG ON THE MOTHER BOARD, PUSH THE PCB (ITEM 2) DOWN UNTIL IT LOCATES ON THE SPACERS. SECURE USING THE 4 SCREWS (ITEM 4).
3. CONNECT THE SELECTIVE CALL PCB (ITEM 2) TO THE MICRO-PROCESSOR PCB USING CABLE (ITEM 3) ENSURING CORRECT ORIENTATION OF SOCKETS.
4. CHECK ISSUE No OF EPROM (TO BE AT LEAST 1.2 FOR 8528S).
5. REMOVE PLUG BUTTON FROM REAR PANEL.
6. REMOVE THE NUT & WASHER FROM PLUG END OF CABLE (ITEM 5), PASS THE SOCKET END OF THIS CABLE THROUGH THE HOLE IN THE REAR PANEL, LOCATE THE PLUG IN THE HOLE & REPLACE THE NUT & WASHER. CONNECT THE CABLE TO THE SELECTIVE CALL PCB (ITEM 2) AS SHOWN. SECURE CABLE TO THE SIDE BRACKET USING THE CABLE CLAMP (ITEM 6).
7. TEST FOR CORRECT OPERATION (SEE HANDBOOK IF REQUIRED).
8. REPLACE BOTTOM COVER.

P/No 15-10366-001 - AS DETAILED

DISC FILE
10366_1

 CODAN	 DRN	 OS	SCALE 1:1	© CODAN PTY LTD, A.C.N. 007 590 605 1993 TITLE OPTION SD - 8528 FITTING INSTRUCTIONS	
	MATERIAL	CHKD	NJA		DATE 4-8-89
	FINISH	APPD	NJA		13-8-89
TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. ±0.25 1 PLACE DEC. ±0.5 ANGULAR ±				DRAWING/DOC NO. A3 15-10366-001	
ISS 1				SHT. 1 OF 1	

DO NOT SCALE

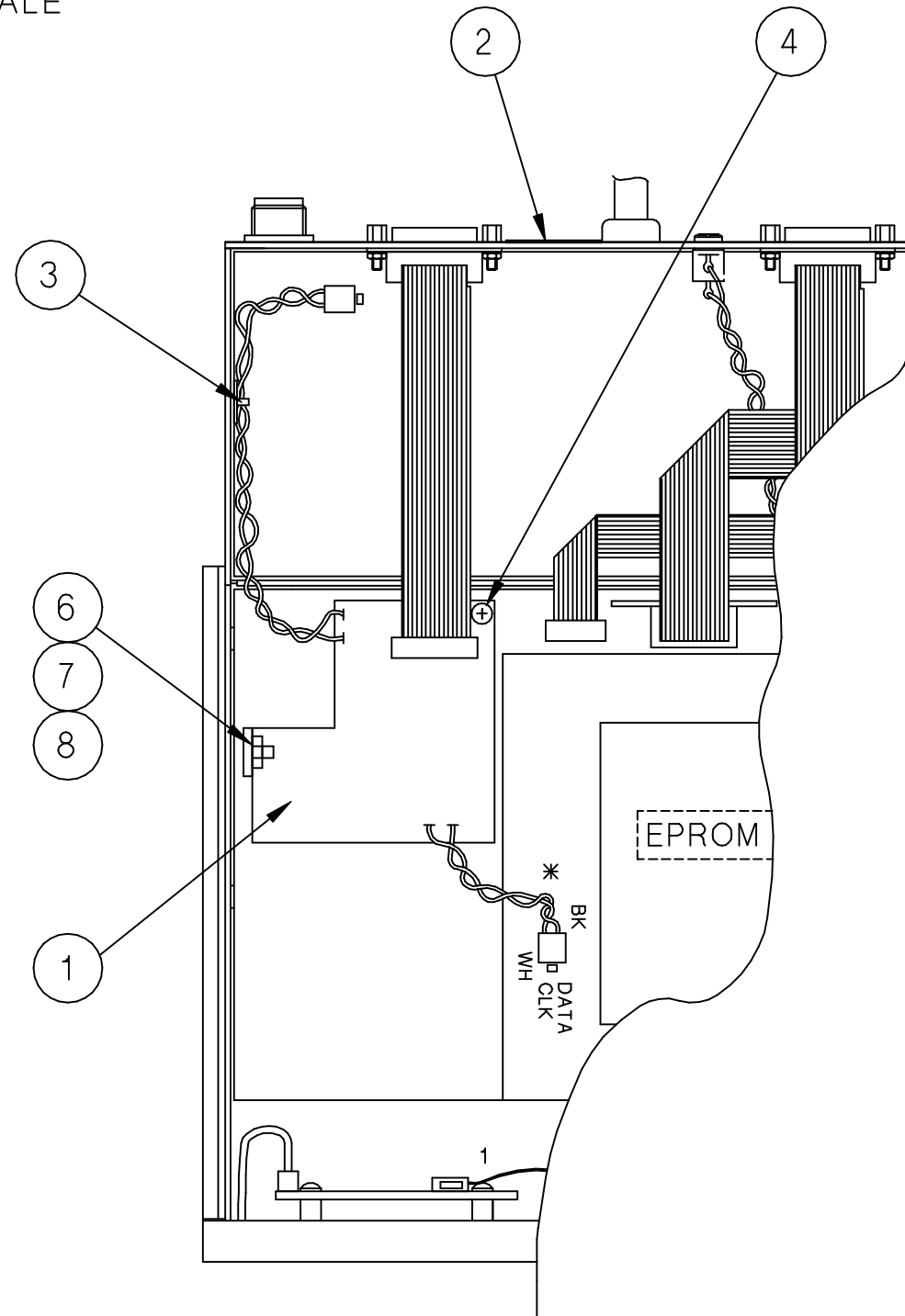
ITEM	PART No.	DESCRIPTION
1	08-04285-001	ANTENNA DRIVER PCB
2	06-01453	LABEL, WARNING
3	30-05102-001	CLAMP, CABLE ADHESIVE
4	31-23020-580	SCREW, M3x20

ISSUE 1
NOTE 2 CHANGED
ITEM 5 DELETED.
C/R 23769
CM 1-11-93

NOTES:

1. REMOVE BOTTOM COVER.
2. IF REQUIRED FIT TWO PIN CONNECTOR *(PART No. 60-00020-260 NOT SUPPLIED) TO THE μ P ASSY - NOTE CORRECT ORIENTATION.
3. REMOVE (ITEMS 6,7&8) AND UNPLUG 16 WAY RIBBON CONNECTOR FROM MOTHERBOARD. REMOVE SCREW FROM MOTHERBOARD SO (ITEM 4) MAY BE FITTED.
4. PLUG (ITEM 1) INTO P201 MAKING SURE THAT THE PINS ENGAGE CORRECTLY.
5. REPLACE (ITEMS 6,7&8) AND FIT (ITEM 4).
6. PLUG 16 WAY RIBBON CABLE INTO (ITEM 1) AND PLUG THE TWO WAY CABLES * INTO THE PA AND μ P PCB AS SHOWN.
7. FIT ADHESIVE CLIP (ITEM 3) AS SHOWN AND SECURE CABLE.
8. CHECK THAT THE SOFTWARE IS ISSUE 3 OR GREATER.
9. FIT WARNING LABEL (ITEM 2) OVER ANTENNA CONTROL ON REAR PANEL.
10. REPLACE BOTTOM COVER.

* IF NECESSARY THE WIRES OF THE SHORT TWISTED PAIR CAN BE SOLDERED DIRECTLY TO THE PCB (BK = DATA WH = CLK)

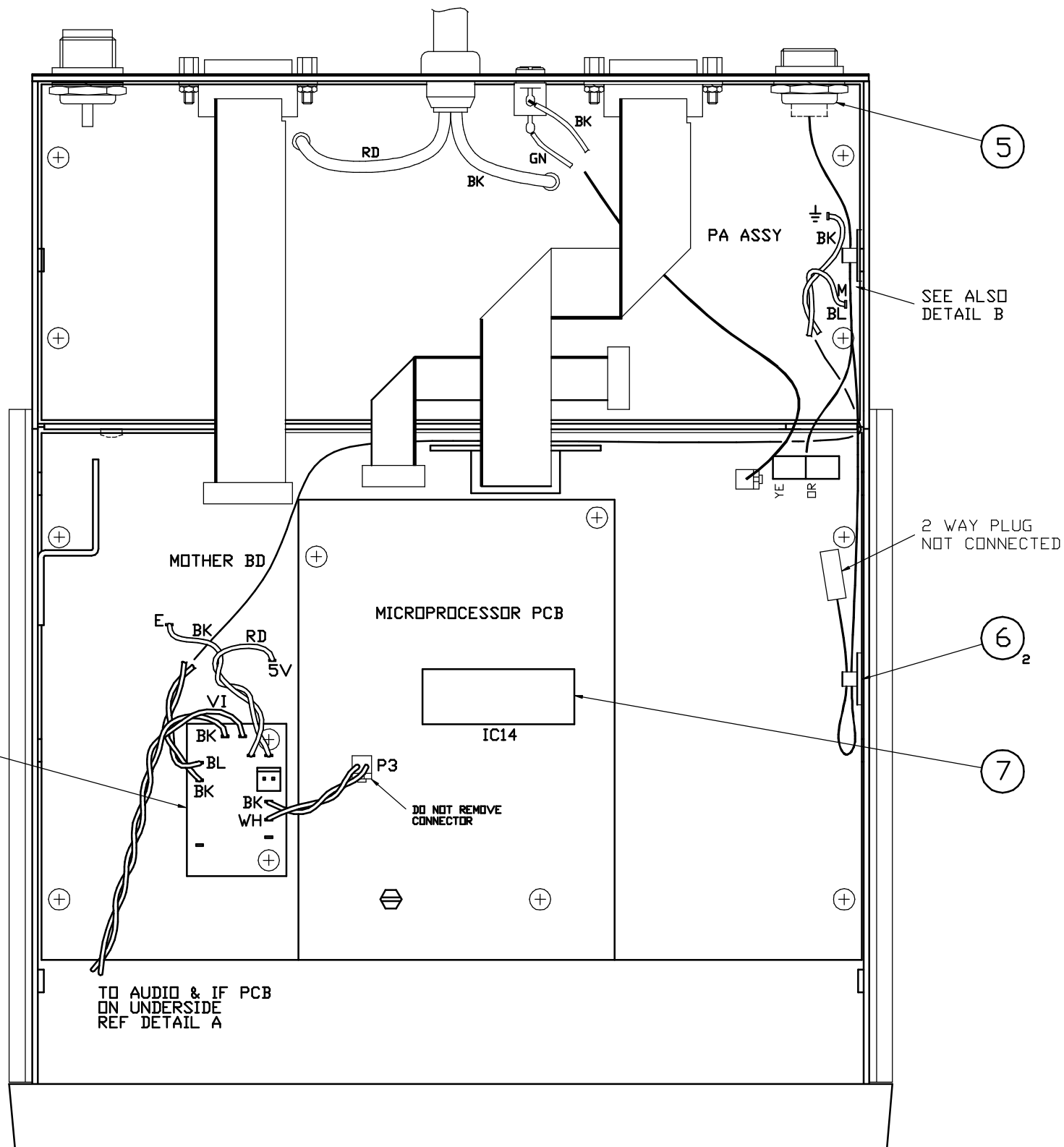
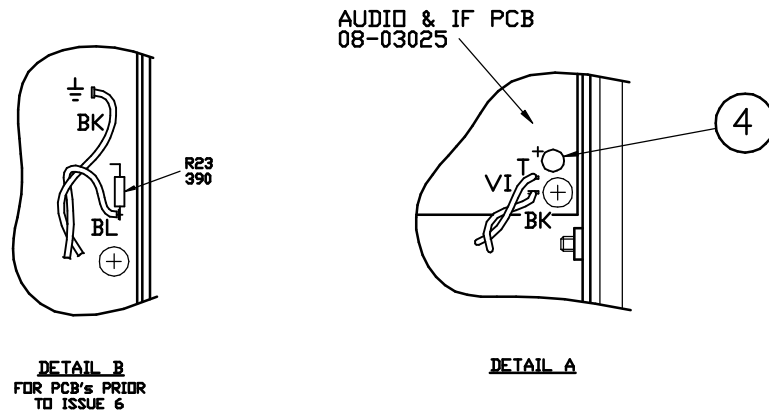


FILE No.
15\10384__1.DWG

DIMENSIONS IN mm

			SCALE NTS	© CODAN PTY LTD, A.C.N. 007 590 605: 2000				
	DRN	APJ	DATE 15-11-90	TITLE OPTION AD FITTING INSTRUCTIONS				
	CHKD	NJA	15-11-90					
MATERIAL	APPD	CM	1-11-93	DRAWING/DOC NO. A3 15-10384-001				
FINISH	TOLERANCES UNLESS OTHERWISE STATED							ISS 1
			2 PLACES DEC.					
			1 PLACE DEC. ±0.5					
			0 PLACE DEC. ±1					

REF	DESCRIPTION	QTY
1	OPTION DM PCB ASSY 08-05041	1
2	SPACER 05-03312-090	2
3	SCREW M3x5 PAN POZI	4
4	CAPACITOR 10uF/25V TAG	1
5	LOOM, 10 WAY 08-05091	1
6	CLAMP, CABLE ADHESIVE BACKED 30-05102-001	2



ISSUE B
ITEMS 5, 6, 7
ADDED,
NOTES 8, 9 & OPT
'PS' ADDED.
C/R 23930
30-5-94

ISSUE C
ITEM 6 QTY WAS 1
C/R 24101
30-11-94 CM

ISSUE 2
P3 NOTE ADDED,
ADDITION TO
NOTE 4,
SHT 2 ADDED.
C/R 24319
14-8-95 NJA

ISSUE 3
DETAIL B ADDED,
S/No NOTE ADDED,
NOTE 7 CHANGED,
MINOR NOTE
CHANGES.
C/R 24533
8-3-96 CM

IMPORTANT

SHT1 APPLIES ONLY TO 8528 TRANSCEIVERS WITH S/No's LOWER THAN B13000, 8528S LOWER THAN B4000 & 8528 INTERNATIONAL LOWER THAN K3000.

OPTION 'PS' COMPONENTS MUST BE FITTED TO MOTHERBOARD
OPTION 'PS' LOOM SHOULD BE DISCARDED IF FITTED.

NOTES

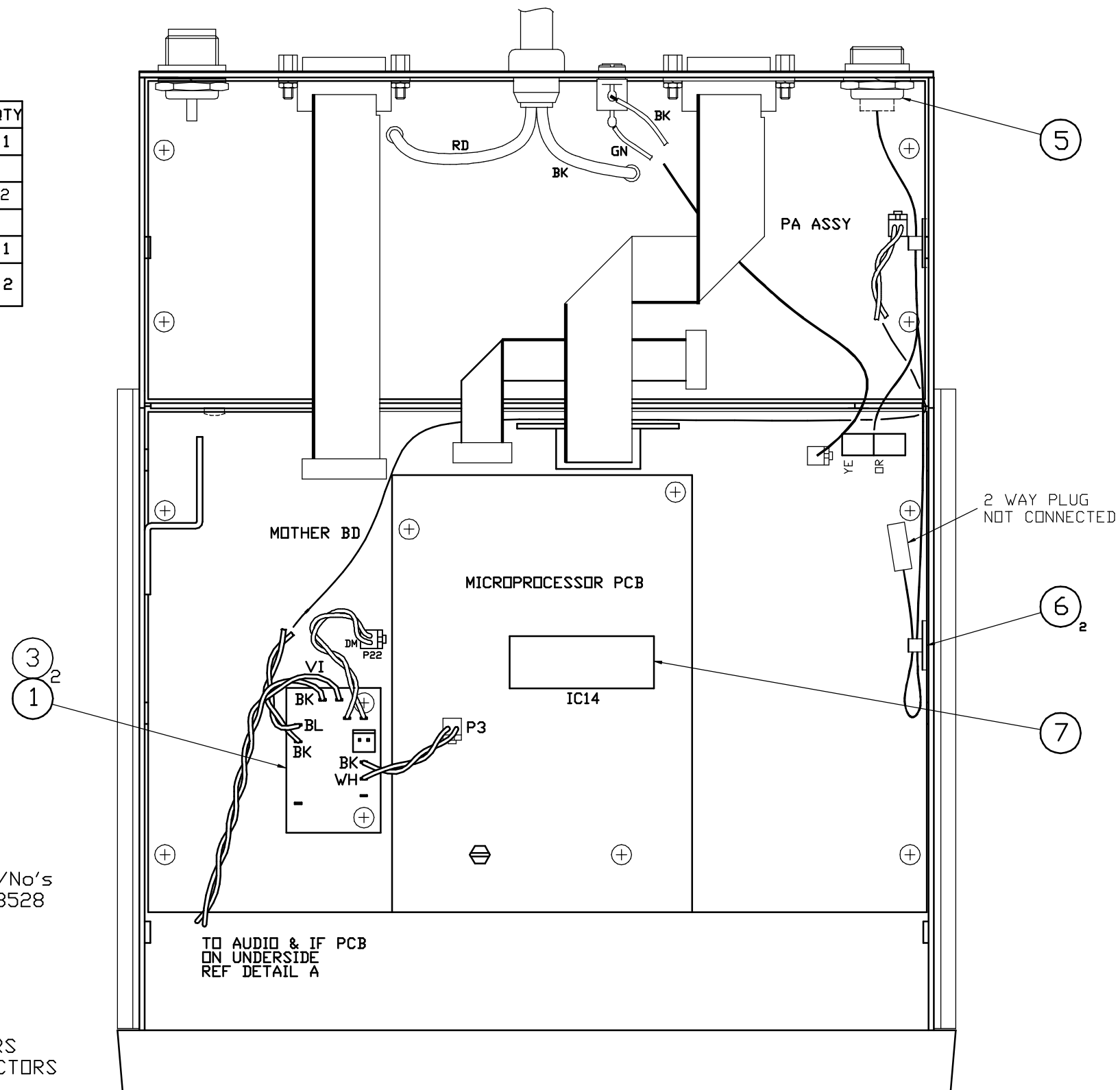
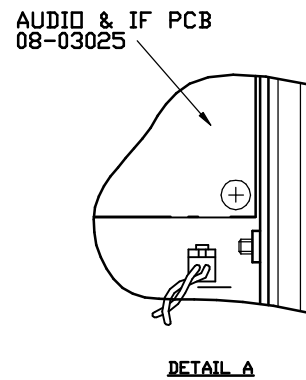
1. REMOVE AUDIO & IF PCB 08-03025.
2. FIT 2 SPACERS (ITEM 2) USING 2 M3x5 SCREWS (ITEM 3) TO MOTHER BD.
3. REPLACE AUDIO & IF PCB.
4. FIT 'OPTION DM' PCB (ITEM 1) TO SPACERS USING 2 M3x5 SCREWS (ITEM 3). CUT OFF UNWANTED CONNECTORS.
5. SOLDER WIRES AS DETAILED & FIT 2 WAY CONNECTOR TO P3 ON MICROPROCESSOR PCB.
6. IF 'OPTION AD' IS FITTED:-
REMOVE PCB ASSY TO SOLDER rd & bk WIRES TO MOTHER BD & THEN REFIT PCB.
REMOVE IT'S 2 WAY CONNECTOR FROM THE uP PCB & FIT ONTO 'OPTION DM' PCB & THEN FIT 'OPTION DM' CONNECTOR TO uP BD P3.
7. CHANGE C57 1uF ON AUDIO & IF PCB TO 10uF (ITEM 4).
8. FIT 10 WAY CONNECTOR & LOOM (ITEM 5) & ATTACH WITH CLAMP (ITEM 6) AS SHOWN.
9. ENSURE EPROM (ITEM 7) IS AT LEAST ISSUE 5.0.

P/No 15-10411-001 - AS DETAILED

	DRN	DB	SCALE 1:1	© CODAN PTY LTD, A.C.N. 007 590 605 1993 TITLE OPTION DM FITTING INSTRUCTIONS
	CHKD	NJA	DATE 28-10-93	
	APPD	CM	DATE 30-11-94	
MATERIAL			TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. ±0.25 1 PLACE DEC. ±0.5 ANGULAR ±	DRAWING/DOC NO. 15-10411-001
FINISH				ISS 2 3
				SHT. 1 OF 2

DISC FILE

REF	DESCRIPTION	QTY
1	OPTION DM PCB ASSY 08-05041	1
2	N/A	
3	SCREW M3x5 PAN PDZI	2
4	N/A	
5	LOOM, 10 WAY 08-05091	1
6	CLAMP, CABLE ADHESIVE BACKED 30-05102-001	2



ISSUE B
REF SHT 1

ISSUE C
REF SHT 1

ISSUE 2
REF SHT1
SHT 2 ADDED.
C/R 24319
14-8-95 CM

ISSUE 3
S/No NOTE ADDED,
MINOR NOTE
CHANGES.
C/R 24533
8-3-96 CM

IMPORTANT

SHT2 APPLIES ONLY TO 8528 TRANSCEIVERS WITH S/No's HIGHER THAN B12999, 8528S HIGHER THAN B3999 & 8528 INTERNATIONAL HIGHER THAN K2999.

OPTION 'PS' LOOM SHOULD BE DISCARDED IF FITTED.

NOTES

1. FIT 'OPTION DM' PCB (ITEM 1) TO EXISTING SPACERS USING 2 M3x5 SCREWS (ITEM 3) & FIT TO CONNECTORS AS SHOWN.
2. IF 'OPTION AD' IS FITTED:-
REMOVE IT'S 2 WAY CONNECTOR FROM THE uP PCB & FIT ONTO 'OPTION DM' PCB & THEN FIT 'OPTION DM' CONNECTOR TO uP BD P3.
3. FIT 10 WAY CONNECTOR & LOOM (ITEM 5) & ATTACH WITH CLAMP (ITEM 6) AS SHOWN.
4. ENSURE EPROM (ITEM 7) IS AT LEAST ISSUE 5.0.

TO AUDIO & IF PCB
ON UNDERSIDE
REF DETAIL A

P/No 15-10411-001 - AS DETAILED

	DRN	DB	SCALE 1:1	© CODAN PTY LTD, A.C.N. 007 590 605 1993 TITLE OPTION DM FITTING INSTRUCTIONS
	CHKD	NJA	DATE 11-8-95	
	APPD	CM	DATE 19-8-95	
MATERIAL			TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. ± 0.25 1 PLACE DEC. ± 0.5 ANGULAR ±	DRAWING/DOC NO. 15-10411-001
FINISH				
			ISS	A3 SHT. 2 OF 2

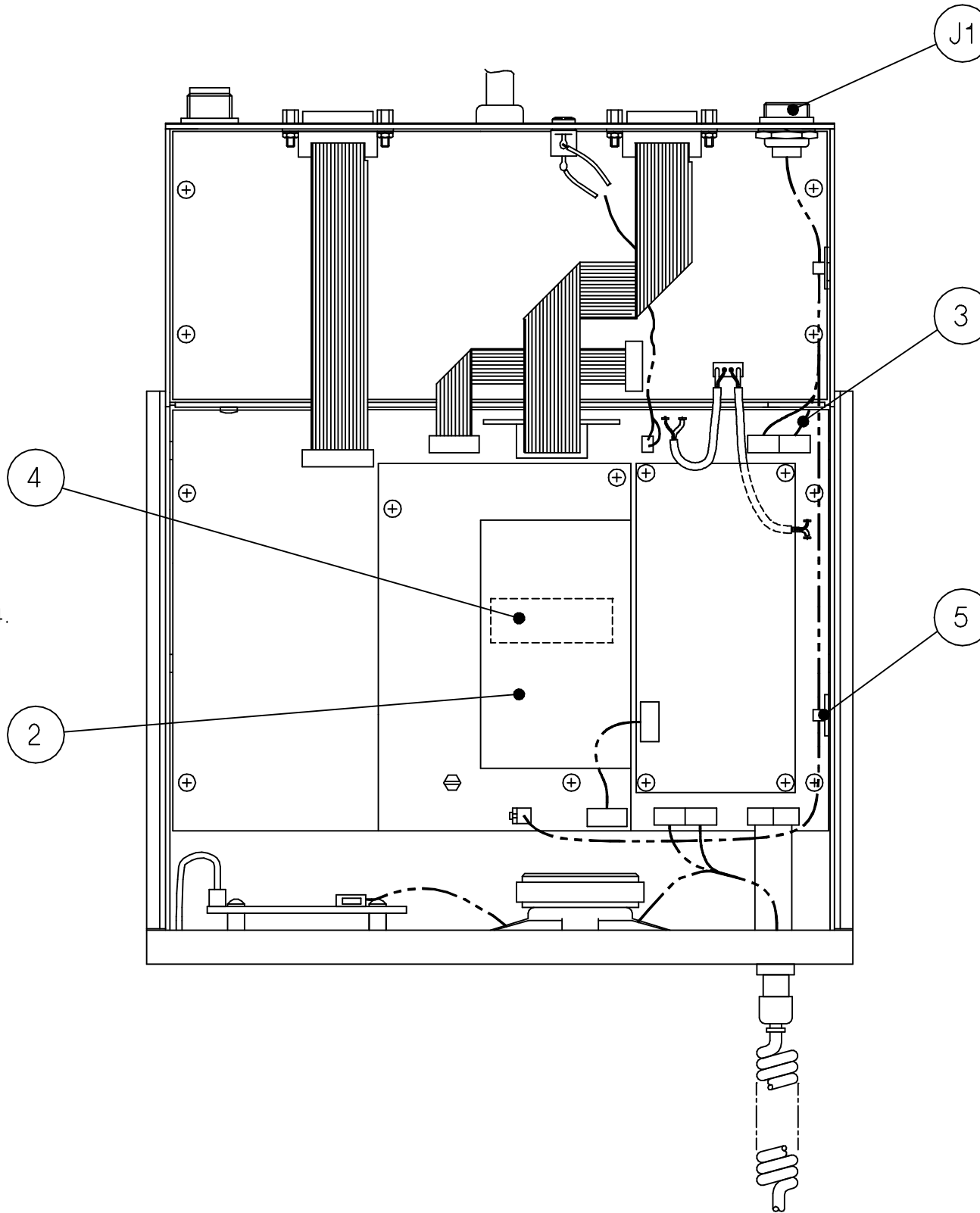
DISC FILE
10411_2

DO NOT SCALE

ITEM	PART No.	DESCRIPTION
1	15-10412-001	FITTING INSTRUCTIONS
2	08-05090-001	MICROPROCESSOR PCB
3	08-05091-001	LOOM, OPT RS
4	90-20540	EPROM
5	30-05102-001	CABLE CLAMP
6	15-10271	OPTION PS

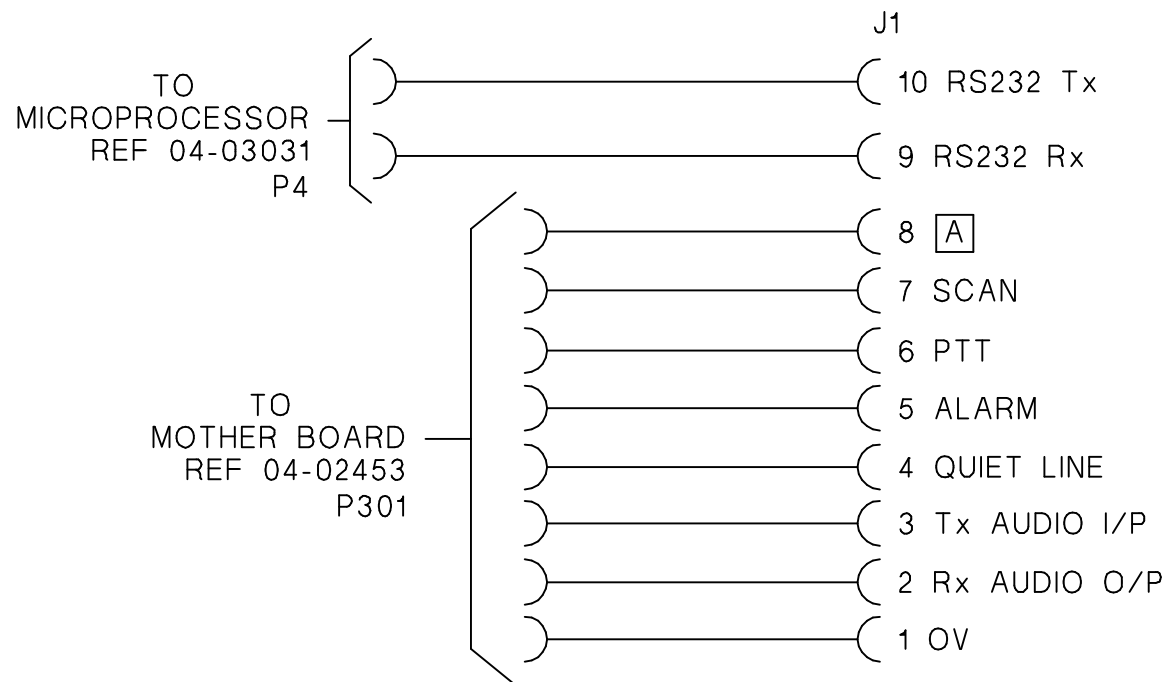
NOTES:

1. REMOVE BOTTOM COVER.
2. FIT OPTION PS COMPONENTS TO MOTHERBOARD. DO NOT FIT PS LOOM.
3. REMOVE MICROPROCESSOR PCB AND REPLACE WITH ITEM 2.
4. CHECK ISSUE NO OF EPROM - ITEM 4. IT IS TO BE AT LEAST 4-4.
5. INSTALL LOOM - ITEM 3 AND ATTACH WITH ITEM 5 AS SHOWN.
6. TEST FOR CORRECT OPERATION.
7. REPLACE BOTTOM COVER.



ISSUE B
OPTION RS ADDED.
C/R 23929
7-4-94 NJA

ISSUE C
ITEM 4 WAS 90-20278
C/R 23930
30-5-94 CAH



DIMENSIONS IN mm

FILE No.
15\10412__C.DWG

		SCALE NTS	© CODAN PTY LTD, A.C.N. 007 590 605: 2000			
	DRN CHKD APPD	ILT NJA	DATE 17-3-94 21-3-94	TITLE FITTING INSTRUCTIONS OPTIONS RS 8528		
MATERIAL	TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC. ±0.10 1 PLACE DEC. ±0.5 0 PLACE DEC. ±1		DRAWING/DOC NO. A3 15-10412-001			
FINISH	ISS A B C				SHT. 1 OF 1	

The following sections are added to the HF SSB transceiver 8525B/8528 series Technical Service Manual, Codan part number 15-02036 Issue 6, November 1995.

This information is provided in addition to that existing in Chapter 4, *Local Oscillators*. It explains the operation of the new synthesisers.

Drawings associated with this addendum are:

- RF Mixer and Dual Synthesiser Circuit Diagram 04-03120
- RF Mixer and Dual Synthesiser PCB Assembly 08-05295

Local Oscillators (04-03120)

Two synthesised oscillators are used to drive the first and second mixers. The first oscillator operates between 45.250 MHz and 75 MHz in 2 kHz steps. It converts the 250 kHz to 30 MHz receive signal to 45 MHz for the first IF. The second oscillator operates between 43.350 MHz and 43.352 MHz in 10 Hz steps. It converts the 45 MHz first IF to 1650 kHz second IF.

Each oscillator consists of a:

- voltage controlled oscillator
- phase/frequency detector
- loop amplifier
- filter
- reference crystal oscillator (common)

The division ratios required are provided in serial data form by the microprocessor from data stored in the memory.

The reference frequency crystal Z2 (6600 kHz) is held at a constant temperature by a power PTC thermistor (R100) or by a high stability temperature controlled oven (08-05235). The crystal oscillator provides the reference frequency for the two synthesisers. The reference, after being divided by four (1650 kHz), provides the local oscillator drive to the modulator/demodulator for USB operation.

A 1647 kHz (Z3) crystal oscillator drives the modulator/demodulator stages for LSB operation.

Voltage Controlled Oscillator (VCO)

As VCO1 and VCO2 are very similar, only VCO1 will be described in detail. The differences between the two VCOs are detailed in the table below.

	VCO1	VCO2
Varicaps	D17 to D20	D46 and D47
VCO output to synthesiser input pin 4	Via buffer V41 and coupling capacitor C144	Via R45 and C155
Division ratio	Divides to 2 kHz	1.1 kHz to 2 kHz in 10 Hz steps
Filter components	C127, C129, C181, R79, R99 and C123	C179, R166 and C180
Reference frequency	Reference crystal oscillator (6600 kHz)	6600 kHz obtained from IC2 pin 3 and applied to IC3 pin 1

FET V2 operates as a Hartley oscillator tuned by four varicaps D17 to D20. The output level is kept near constant frequency by a negative bias voltage applied to the V2 gate. This voltage is generated from schottky diode D21 charging capacitor C44.

Unity gain feedback amplifier V3 and V4 provides a buffer between the oscillator and the cascade connected amplifier V5 and V6. The second amplifier provides +7 dBm drive to the ring diode mixer D13. The VCO output is buffered by V41, before being applied to synthesiser IC2 pin 4.

Synthesiser for VCO1

Synthesiser IC2 generates a DC control voltage via the phase/frequency detector and control amplifier. This is applied to the varicaps to lock the VCO1 to the nominated frequency.

The 6600 kHz oscillator, part of IC2, is divided down to a 2 kHz reference frequency. The VCO signal applied to pin 4 of IC2 is also divided to produce 2 kHz when VCO1 is at the nominated frequency. Both of these signals are applied to the phase/frequency detector in IC2.

The phase/frequency detector (IC2) provides two outputs. Pin 14 provides a "go down" pulse. Pin 15 provides a "go up" pulse. These outputs are high (+5 V) when locked, except for a very narrow negative going pulse that occurs simultaneously on both outputs.

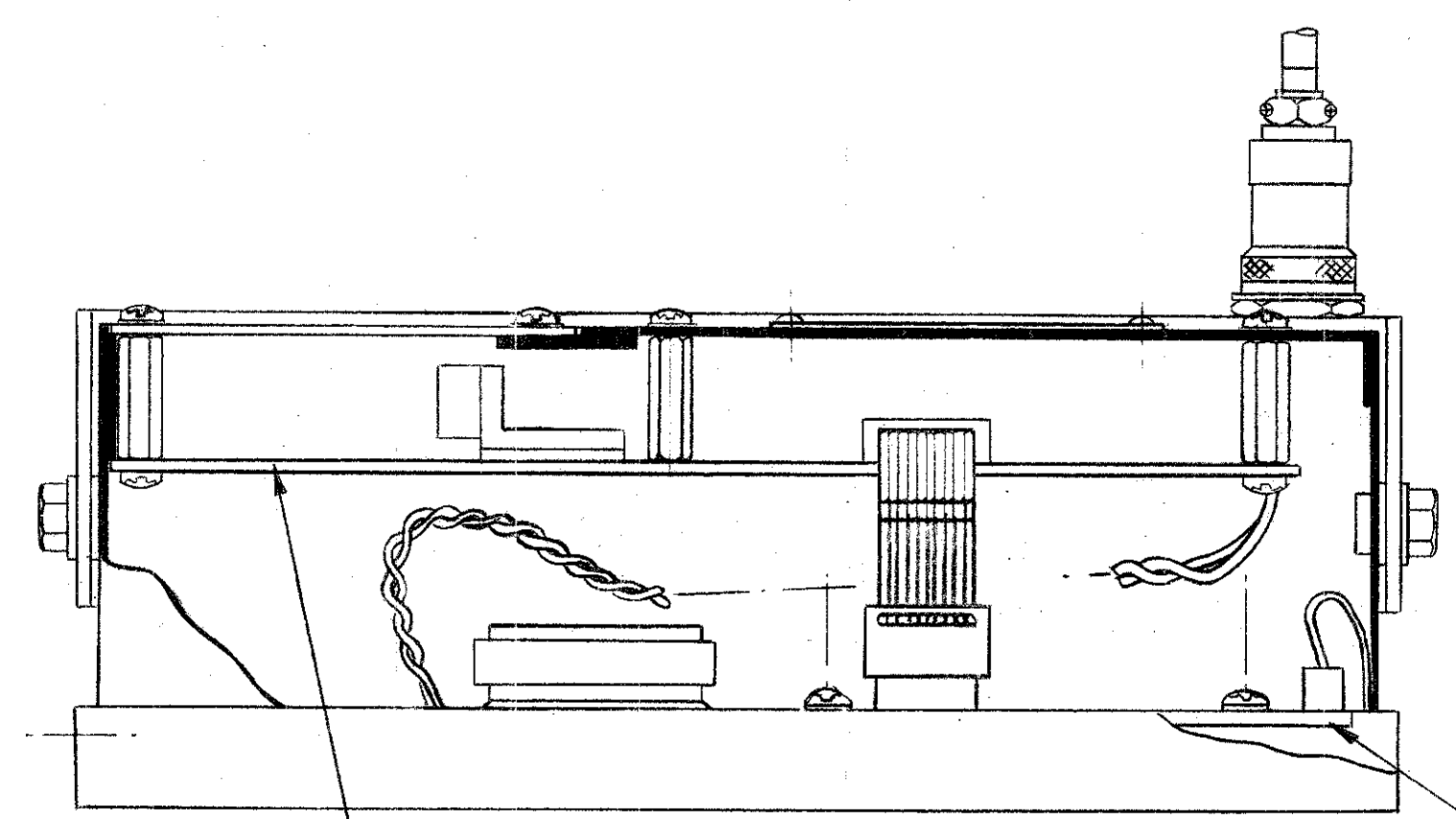
V29 and V30 provide a 3 mA discharging current pulse when pin 14 is low. V28, V31 and V32 provide a 3 mA charging current pulse when pin 15 is low.

These current pulses accumulate in the loop filter (C127, C129, C181 and R79). The resulting voltage is applied to the varicaps (D17 - D20) via a filter (R99 and C123). This filter removes any reference components from the control voltage.

1 2 3 4 5 6 7 8 9 10 11 12

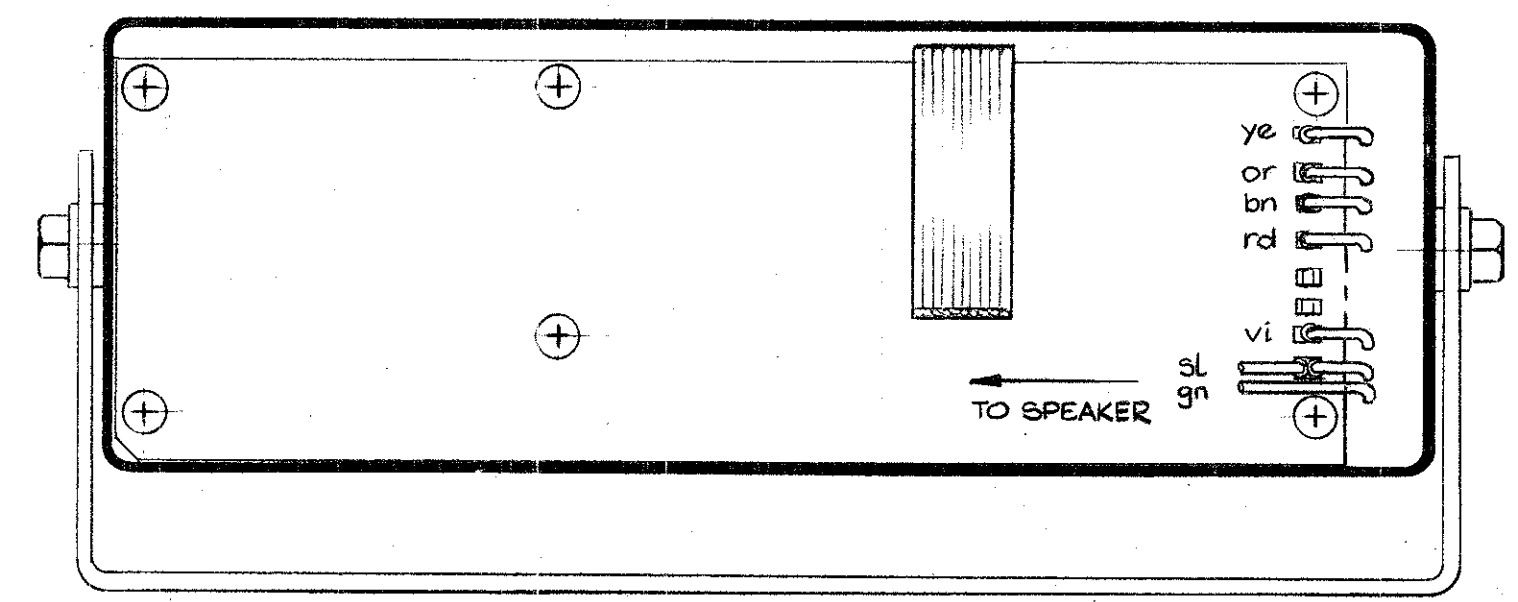
DO NOT SCALE

ISSUE 2
C/R 21219
27-1-87 *MM*



MICROPHONE AMPLIFIER
& INTERFACE P.C.B.
08-03039

DISPLAY BOARD
HEAD
08-03945



INTERNAL VIEW

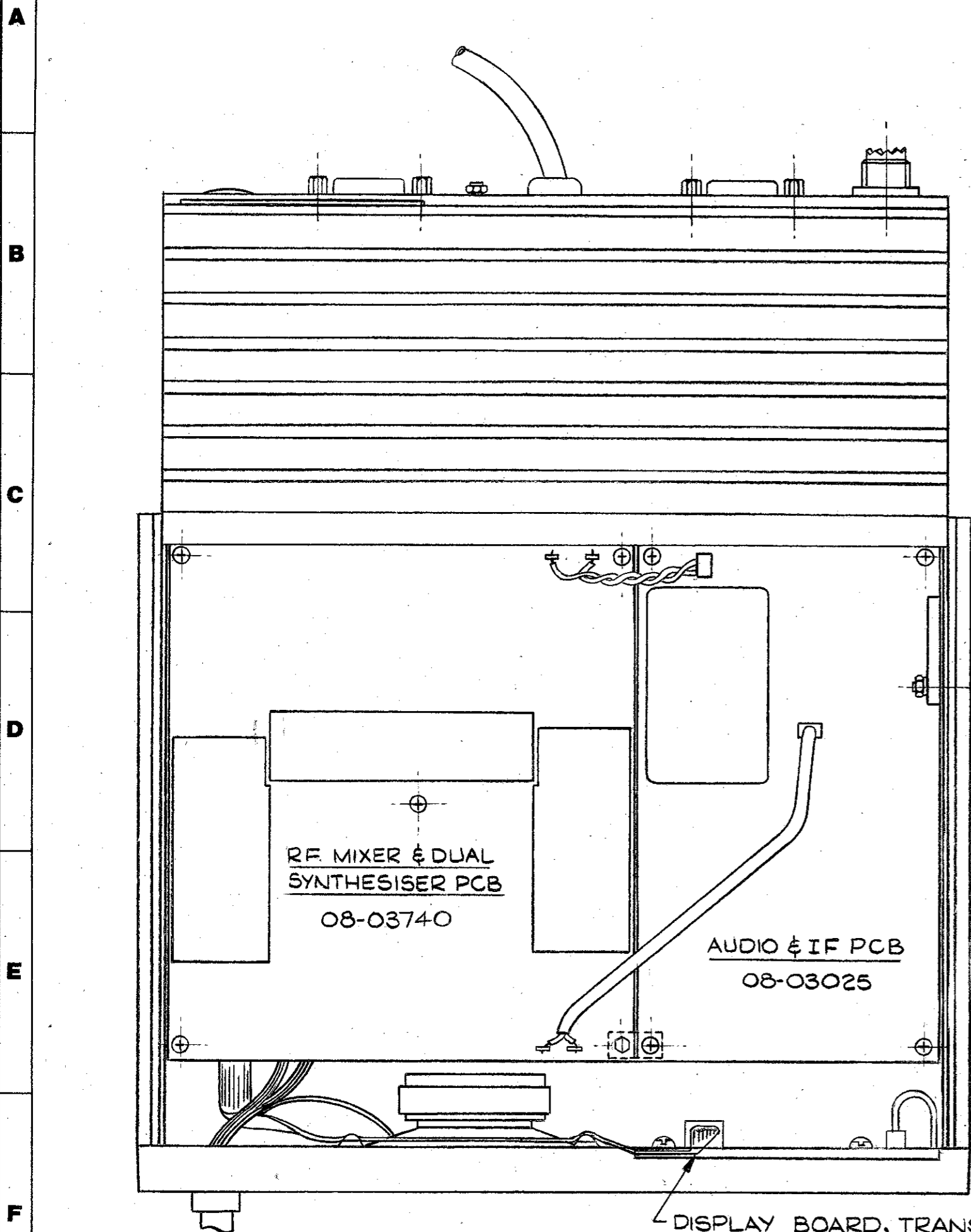
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MATERIAL	CHKD.	AKS	APPD.	MM	30-10-86
FINISH	TOLERANCES UNLESS OTHERWISE STATED		ISS	A2	DRAWING/DOC NO.
	2 PLACES DEC ± 1 PLACE DEC ± ANGULAR ±				
			SHT /		OF /

M

1 2 3 4 5 6 7 8 9 10 11 12

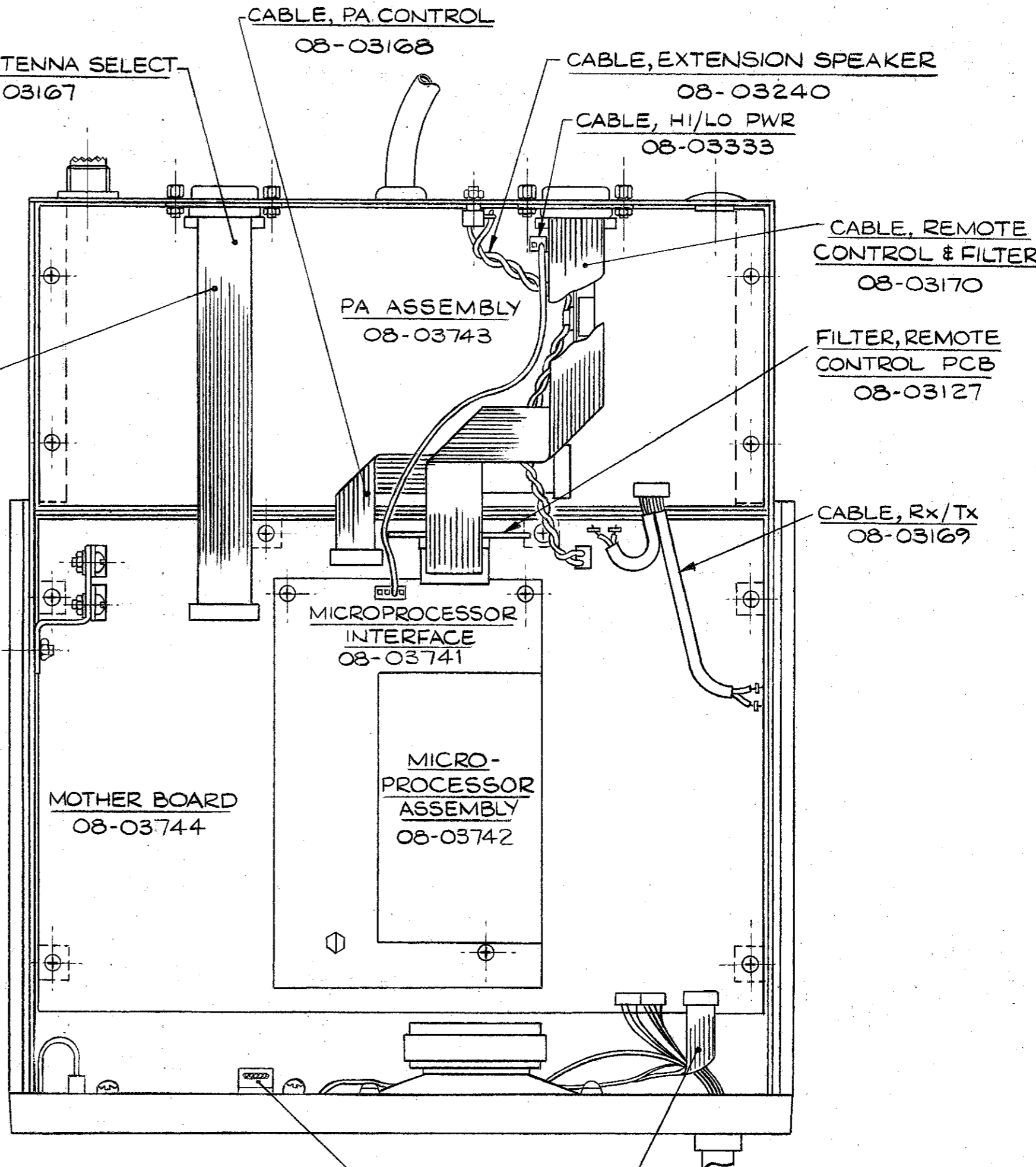
DO NOT SCALE

ISSUE 2
C/R 21219
CABLE ADDED
23-1-87 *MM*



DISPLAY BOARD, TRANSCEIVER
08-03944 8525
08-03745 8528

ENSURE THAT THE
CABLE IS CLEAR OF
RF FILTER COMPONENTS



CABLE, ANTENNA SELECT
08-03167

CABLE, PA CONTROL
08-03168

CABLE, EXTENSION SPEAKER
08-03240

CABLE, HI/LO PWR
08-03333

CABLE, REMOTE
CONTROL & FILTER
08-03170

FILTER, REMOTE
CONTROL PCB
08-03127

CABLE, Rx/Tx
08-03169

PA ASSEMBLY
08-03743

MICROPROCESSOR
INTERFACE
08-03741

MICRO-
PROCESSOR
ASSEMBLY
08-03742

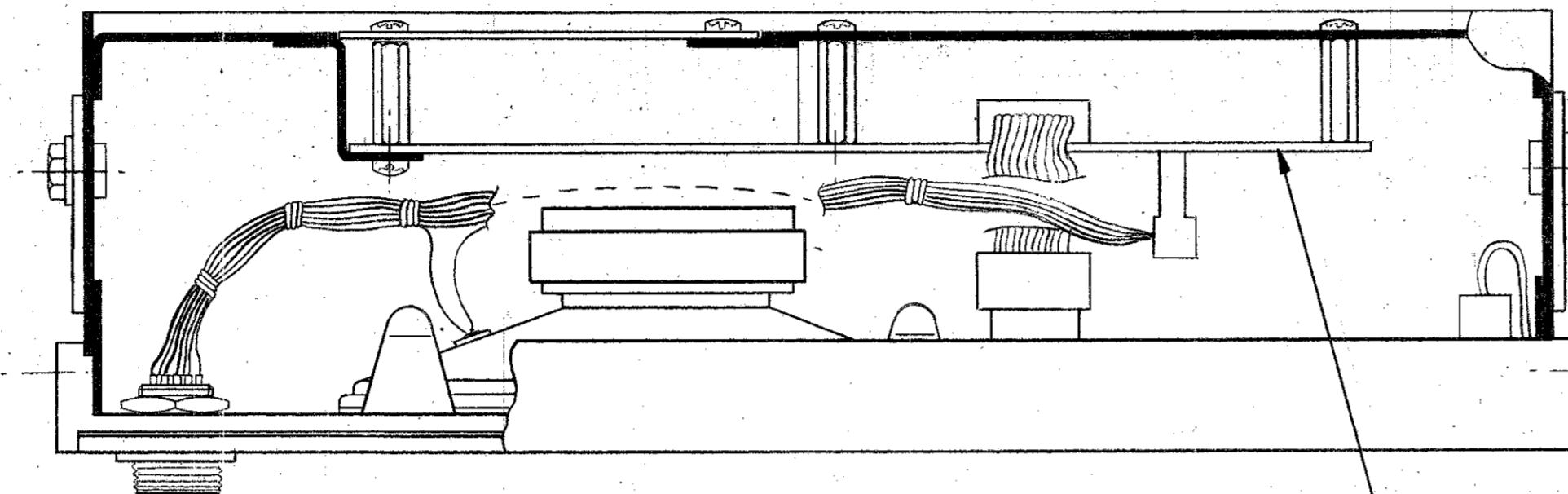
MOTHER BOARD
08-03744

CABLE, INTERFACE
08-02988

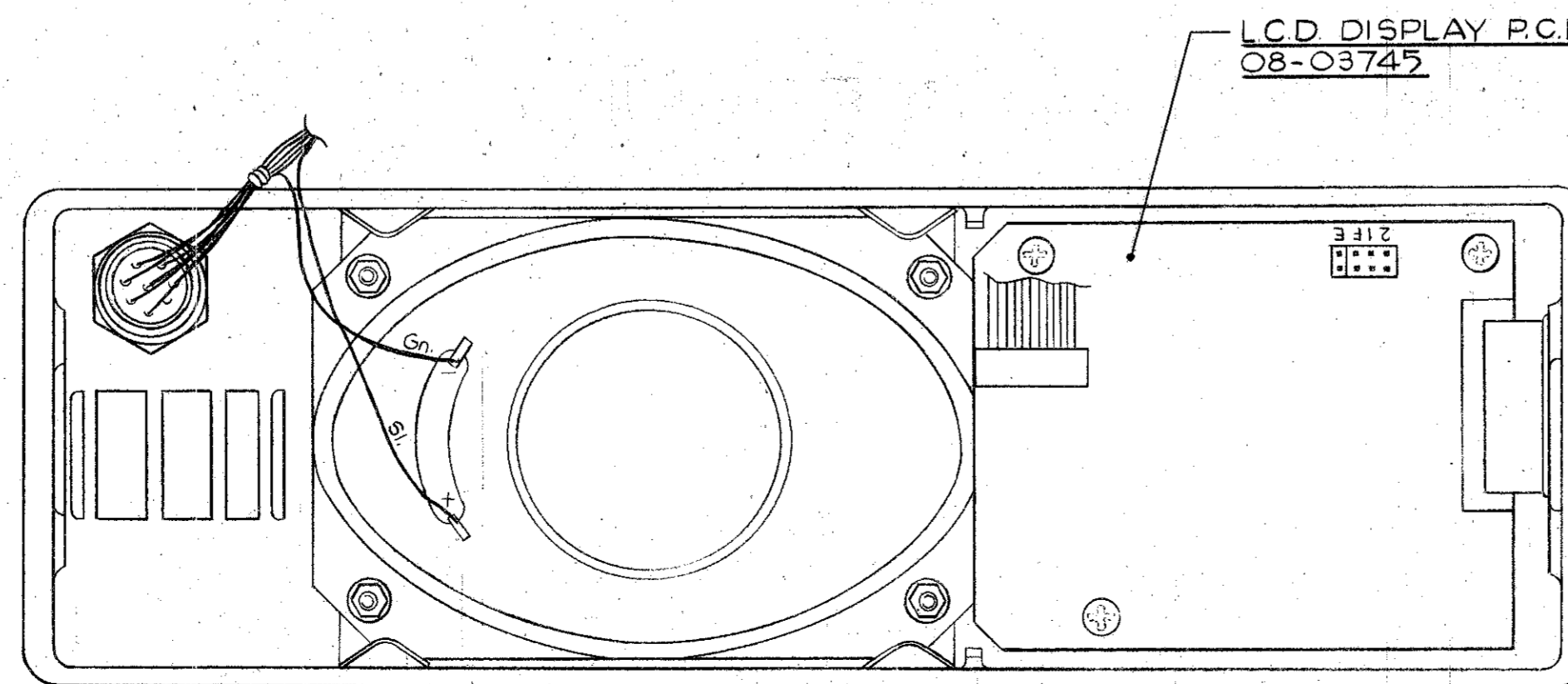
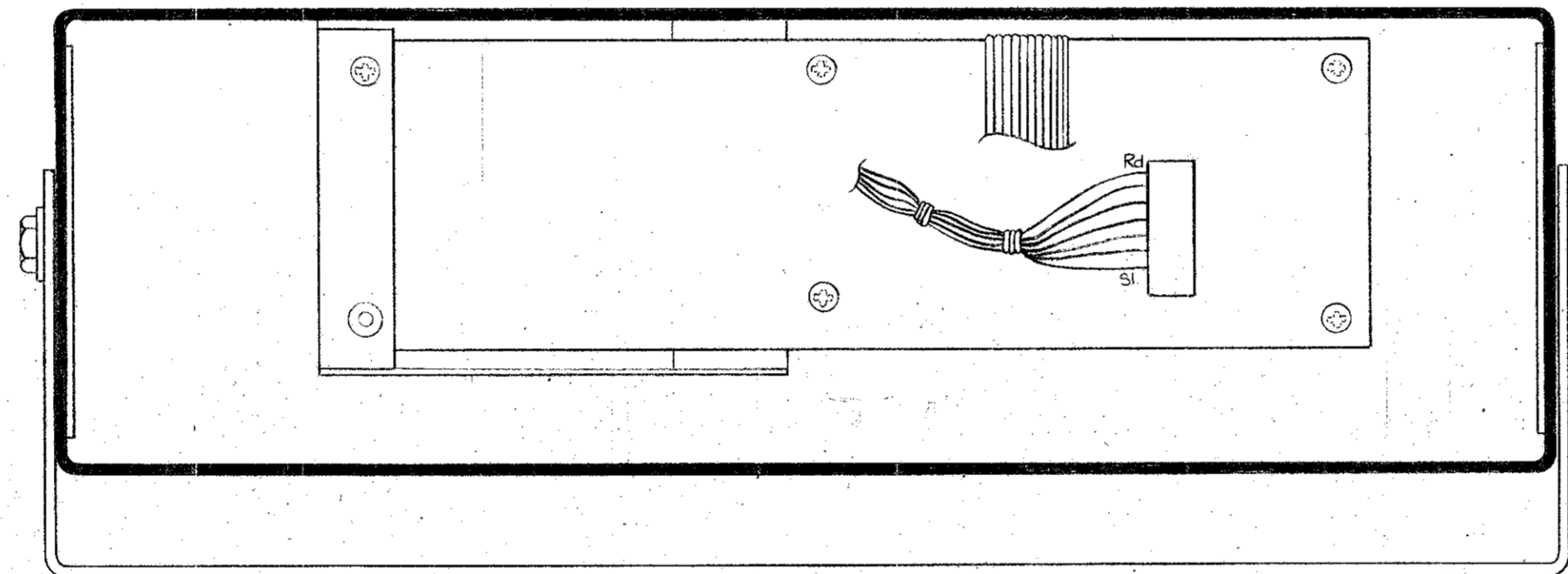
400

	DRN.	APR.	DATE	TITLE TRANSCEIVER LAYOUT
	CHKD.	<i>AWG</i>	22.10.86	
MATERIAL	APPD.	<i>MM</i>	30-10-86	DRAWING/DOC NO.
FINISH	TOLERANCES			A2 16-00035-004
	UNLESS OTHERWISE STATED			
	ISS	1	23	SHT
				OF

DO NOT SCALE



MICROPHONE AMPLIFIER AND INTERFACE P.C.B. 08-03039



L.C.D. DISPLAY P.C.B. 08-03742

	DRN. 0.S.	SCALE 1:1	TITLE CONTROL HEAD LAYOUT	COPYRIGHT CODAN 19
	CHKD. <i>[Signature]</i>	DATE 15-9-89		
MATERIAL	APPD. <i>[Signature]</i>	18-9-89	A1 16-00035-005	SHIT 1 OF 1
FINISH	TOLERANCES UNLESS OTHERWISE STATED 2 PLACES DEC ± 1 PLACE DEC ± ANGULAR +			

566



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9103 Automatic Antenna Tuner - Serial Nos A1312 - A1342

Symptom

The 9103 tuner has recently incorporated a revised Printed Circuit Board (PCB) Artwork to include components necessary for scanning when used with Coda 85... series transceivers.

An error has been discovered on the PCB silkscreen whereby Capacitor C88 (2.2 μ F) may have been inserted incorrectly. The silkscreen identifies the +ve terminal of C88 closest to capacitor C87 and is incorrect. The +ve terminal should be located closest to Resistor R64.

On units with Serial Nos greater than A1342 the error has been rectified and the incorrect identifier on the PCB removed however, the possibility exists for some units in the Serial No. range A1312 - A1342 to have had the capacitor wrongly inserted. Whilst this may not be apparent from tuner operation, the capacitor may break down over a long period of time resulting in poor scan operation.

Remedy

Owners of Tuners with Serial Nos in the above range are advised to check the orientation of capacitor C88 and replace it where incorrect. This can be accomplished by the following:

- I. Remove 10 screws securing the Tuner lid
- II. Remove 4 screws securing the shielding plate
- III. Check the orientation of Capacitor C88 as per the attached Fig 1 and if incorrect -
 - (a) Remove 4 screws securing the PCB, desolder Capacitor C88 and replace it with one correctly oriented.
 - (b) Carefully scratch off the + sign on the PCB adjacent to C88 to avoid future confusion;
 - (c) Replace the PCB
- IV. Re-assemble the Tuner

The Tuner should then be checked for correct operation.

Replacement capacitors can be made available from Codan's Service Department.

Ensure C88 has +ve terminal closest to R64

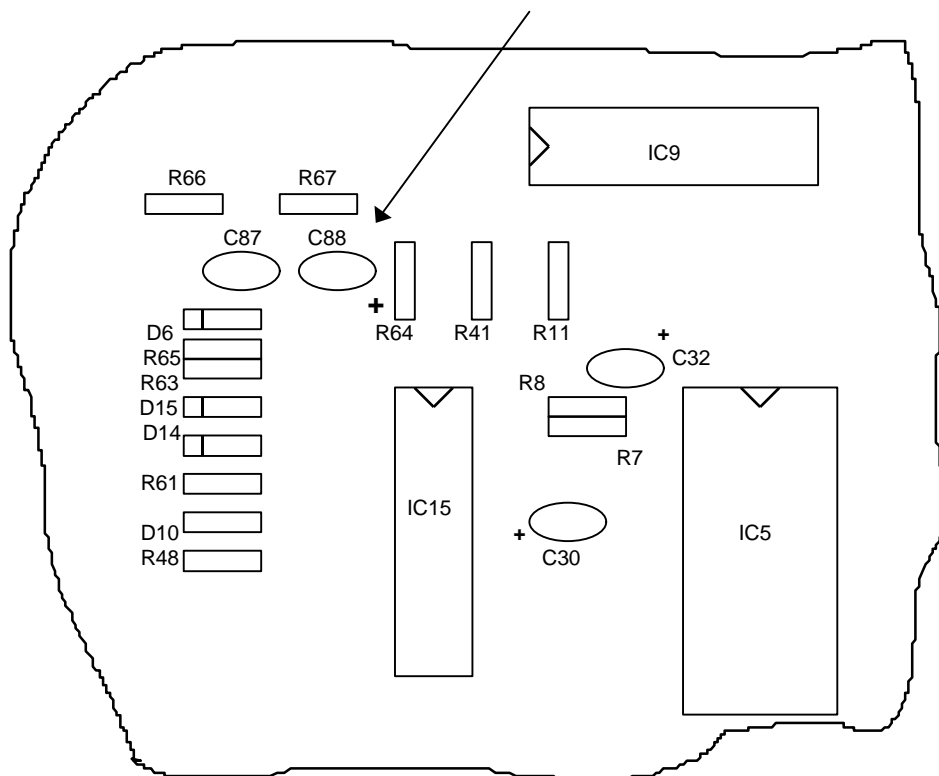


Figure 1. Part of 9103 Tuner Assembly