CODAN

HF SSB Transceiver
9323, 9360, 9390 and 9780

Technical Service Manual

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1 About this manual

This manual provides a technical description, details and drawings of the 9323, 9360, 9390 or 9780 transceiver. It should be used as a guide to the function, technical operation, fault diagnosis, dismantling, assembly, set up and adjustment of this series of transceivers.

This manual assumes that you have a technical background in electronics.

The manual contains nine chapters:

Chapter 2 provides an overview of the features of the 9323, 9360, 9390 or 9780 transceiver, including specifications.

Chapter 3 provides a brief description of the 9323, 9360, 9390 or 9780 transceiver including a general description of the major circuit functions for the control, reception and transmission of signals.

Chapter 4 provides a more detailed technical description of the operation and circuit function of the 9323, 9360, 9390 or 9780 transceiver. Read this with the associated technical drawings found in Chapter 9.

Chapter 5 provides details of maintenance, fault diagnosis procedures and general cautions and warnings associated with the 9323, 9360, 9390 or 9780 transceiver.

Chapter 6 provides programming procedures for channel additions.

Chapter 7 provides adjustments, checks and alignments to the 9323, 9360, 9390 or 9780 transceiver. A list of required test equipment is included.

Chapter 8 contains the parts lists for the 9323/9360/9390/9780.

Chapter 9 contains the circuit and layout drawings for the 9323/9360/9390/9780 transceiver.

Standards and icons

This typeface	Means
Bold	the name of a button or knob that appears on the front control panel or extended control head of the transceiver and a segment of text from the display
Italic	a cross-reference or text requiring emphasis

This icon	Means
❑	A step within a task
	Warning: It is possible that you will seriously damage yourself or the equipment
	Caution: proceed with care as your actions may lead to loss of data, privacy or signal quality
	Note: The text provided next to this icon may be of interest to you
 04-02976 Sheet 1	indicates that you should use Sheet 1 of drawing number 04-02976

Definitions

Acronyms and abbreviations

Abbreviation	Meaning
A/D	analog to digital
A/F	audio frequency
AC	alternating current
ADC	analog to digital conversion
AGC	automatic gain control
ALC	automatic level control
ALE	address latch enable automatic link establishment
AM	amplitude modulation
AND	logical AND function
ARQ	automatic repeat request
BCD	binary-coded decimal
BPF	band-pass filter
B-E	base—emitter
CB	citizen band
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
CRO	cathode-ray oscilloscope
CW	continuous wave, carrier wave
DC	direct current
DSB	double sideband
e.g.	exempli gratia, for example
EEPROM	electrically erasable programmable read-only memory
EMF	electromotive force
Emgcy	emergency
EPROM	erasable programmable read only memory
ES	emergency selcall
etc	et cetera, and so forth
EXT	external
FET	field-effect transistor
FSK	frequency shift keying

Abbreviation	Meaning
FWD-PWR	forward power
GP	general purpose
GPS	global positioning system
HF	high frequency
HPF	high-pass filter
i.e.	id est, that is
I/O	input/output
I/P	input
I^2C	inter integrated circuit
IF	intermediate frequency
IMD	intermodulation distortion
imp	impedance
ITU	International Telecommunication Union
LCD	liquid crystal display
LED	light emitting diode
LPF	low-pass filter
LSB	lower sideband
M	morse
MIC	microphone
NAND	inverted AND logic
NL	noise limiter
NOR	inverted OR logic
NPN	NPN transistor type
NTC	negative temperature coefficient
O/P	output
OC	open circuit
OR	logical OR function
P	peak
P-P	peak to peak
PA	power amplifier
PA/OP	power amplifier/output
PC	personal computer
PCB	printed circuit board
PD	potential difference
PEP	peak envelope power

Abbreviation	Meaning
PLL	phase locked loop
PNP	PNP transistor type
ppm	parts per million
PSEN	program select enable
PTC	positive temperature coefficient
PTFE	polytetra fluoro ethylene
PTT	press-to-talk
PWM	pulse width modulation
PWR	power
Q	quality factor
RAM	random access memory
REF-PWR	reference-power
RF	radio frequency
RFDS	royal flying doctor service
RMS	root mean square
ROM	read only memory
Rx	receive; receiver
SCF	suppressed carrier frequency
SCL	synchronous clock
SDA	synchronous data
SINAD	signal + noise + distortion-to-noise + distortion ratio
SOT	select on test
SSB	single sideband
TCVR	transceiver
TCW	tinned copper wire
THD	total harmonic distortion
TPE	to program enable
Tx	transmit; transmitter
USB	upper sideband
VCO	voltage controlled oscillator
VDR	voltage dependant resistor
VSWR	voltage standing wave ratio

Glossary

Term	Meaning
band-pass filter	A circuit that allows a range of frequencies to pass and attenuates all others.
comparator	Commonly, a two input operational amplifier that gives an output when one input exceeds the reference voltage of the other input.
phase/frequency detector	Any circuit or IC that gives a proportional output when a phase or frequency shift is detected with respect to a reference frequency.

Circuit reference designations

Abbreviation	Designation
A	Assembly
B	Transducer—microphone, loudspeaker etc
C	Capacitor
D	Diode—small signal and power
E	Heating device
F	Protection device—fuse etc
G	Generator—battery etc
H	Signalling/indicating device—lamp, LED, buzzer etc
IC	Integrated Circuit, thick film hybrid etc
J	Jack socket
K	Relay, key switch
L	Inductor
M	Indicating device—meter etc
P	Plug
R	Resistor
S	Switch
T	Transformer, common mode choke
TP	Test Point
U	Modem, Modulator
V	Semiconductor (not including small signal and power diodes)
X	Terminals
Z	Quartz Crystal, Crystal Filter, Frequency Network

Units

Abbreviation	Unit
A	Ampere
°C	degrees Celsius
C	Coulomb
dB	decibels
F	Farad
g	gram
h	hour
H	Henry
Hz	Hertz
J	Joule
K	Kelvin
l	litre
m	metre
min	minute
N	Newton
Pa	Pascal
S	Siemens
s	second
T	Tesla
V	Volt
W	Watt
Wb	Weber
Ω	Ohm

Unit multipliers

Abbreviation	Prefix	Numeric	Meaning
T	Tera	10^{12}	one million million
G	Giga	10^{9}	one thousand million
M	Mega	10^{6}	one million
k	kilo	10^{3}	one thousand
h	hecto	10^{2}	one hundred
da	deca	10	ten
d	deci	10^{-1}	one tenth
c	centi	10^{-2}	one hundredth
m	milli	10^{-3}	one thousandth
µ	micro	10^{-6}	one millionth
n	nano	10^{-9}	one thousand millionth
p	pico	10^{-12}	one million millionth

About this issue

This is the fourth issue of the HF SSB Transceiver 9323/9360/9390/9780 Technical Service Manual.

This manual differs from the previous issue in three significant ways:

- the RF mixer and dual synthesiser circuits have been replaced and are shown on 🗁04-03135 and 04-03096 (PA)
- Option CW has been added, details of which are shown on 🗁 04-03104, 08-05259, 04-03105 and 08-05260
- the HF SSB Transceiver 9780 has been added to the product range

Associated documents

This service manual is one of a series of publications related to the HF SSB Transceiver 9323/9360/9390/9780. Other associated documents are:

- HF SSB Transceiver User Guide (Codan part number 15-04073)
- HF SSB Transceiver Reference Manual (Codan part number 15-04076)
- HF SSB Marine Transceiver 9390 User guide (Codan part number 15-04068)
- HF SSB Marine Transceiver 9390 Reference manual (Codan part number 15-04069)
- HF SSB Transceiver 9780 User Guide (Codan part number 15-04082)
- HF SSB Transceiver 9780 Reference Manual (Codan part number 15-04083)

Other documents

If you a need to program the 9323, 9360, 9390 or 9780, refer to the XP programming guide (Codan part number 15-04035).

If you need to service the PA and Exciter Interface associated with the Codan Power Amplifier type 4404, refer to the HF 4000 series Technical Service Manual (Codan part number 15-02037).

2 General information

Overview

The 9323, 9360, 9390 and 9780 transceivers feature synthesised frequency generation. The transceiver can be controlled via the control panels or the microphone buttons. All transceiver functions are controlled by a central microprocessor, enabling facilities such as clarifier, emergency call etc, to be included as standard fit.

The transceiver can be operated from a front control panel or via a cable connected to a control head. If only a control head is required, the front control panel is replaced with a blank panel.

Transceiver type	Control head
9323	9330
9360	9366
9390	9391
9780	9782

For the 9323 or 9360, channel capacity up to 400 single or two-frequency simplex channels with limited user input channel text. For the 9390, channel capacity is up to 650 single or two-frequency simplex channels with limited user input channel text (consisting of 400 user programmable channels and 250 fixed ITU channels. For the 9780, channel capacity is up to 15 channels).

Frequencies and options are programmed via the microphone socket or 3-wire RS232 interface using XP programming software and an IBM compatible PC. Channels may be entered from the front panel by qualified personnel or, where authorised, by the operator. Channel frequencies and options can be copied from one transceiver to another via the microphone socket. Receive frequencies may be entered by the operator.

The display is a graphic super twist LCD and is back lit by LEDs. All transceiver frequencies and operating modes are shown on the display.

Front and rear panel diagrams

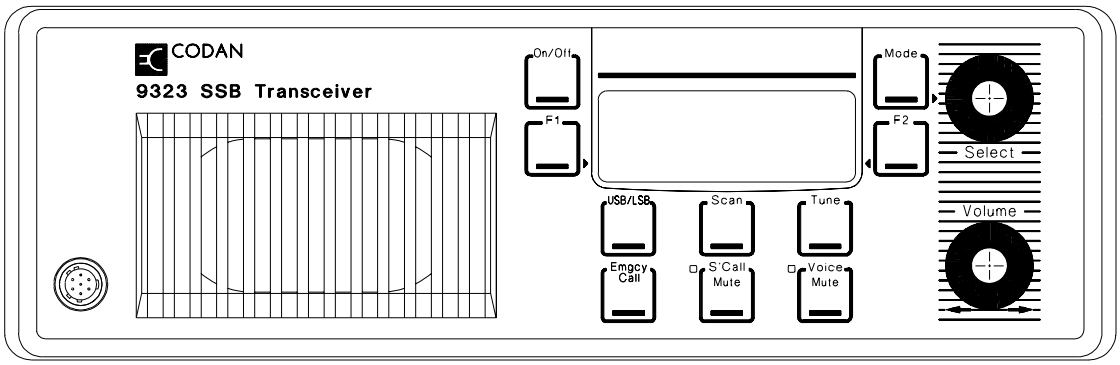

Figure 2 -1: Front panel of HF SSB Transceiver 9323

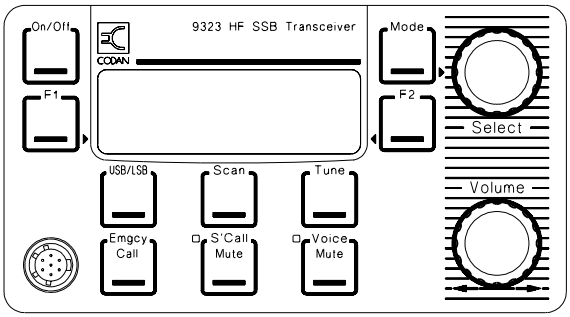

Figure 2 -2: Extended control head (9330) of HF SSB Transceiver 9323

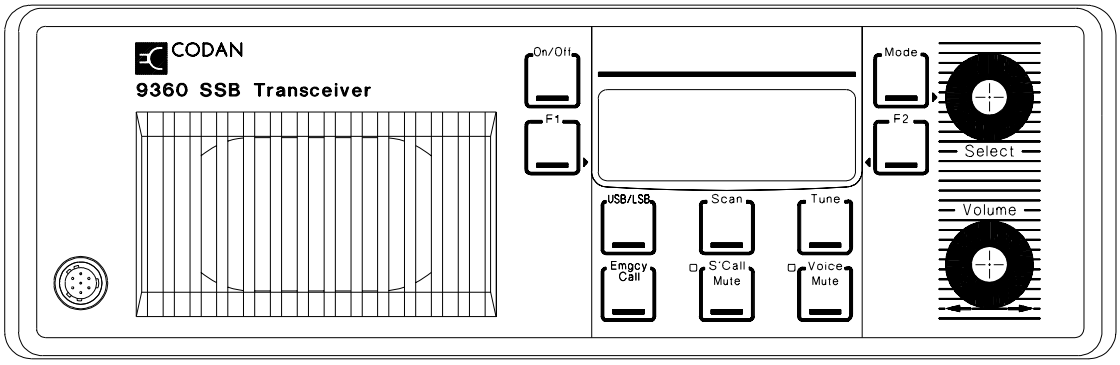

Figure 2 -3: Front panel of HF SSB Transceiver 9360

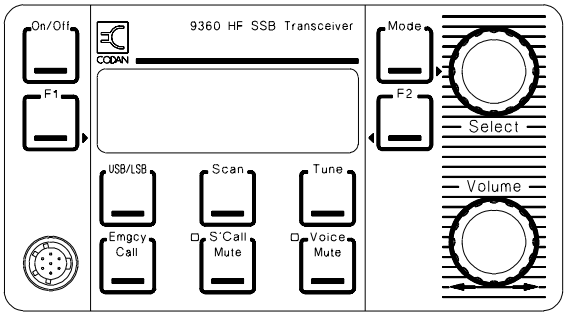

Figure 2 -4: Extended control head (9366) of HF SSB Transceiver 9360

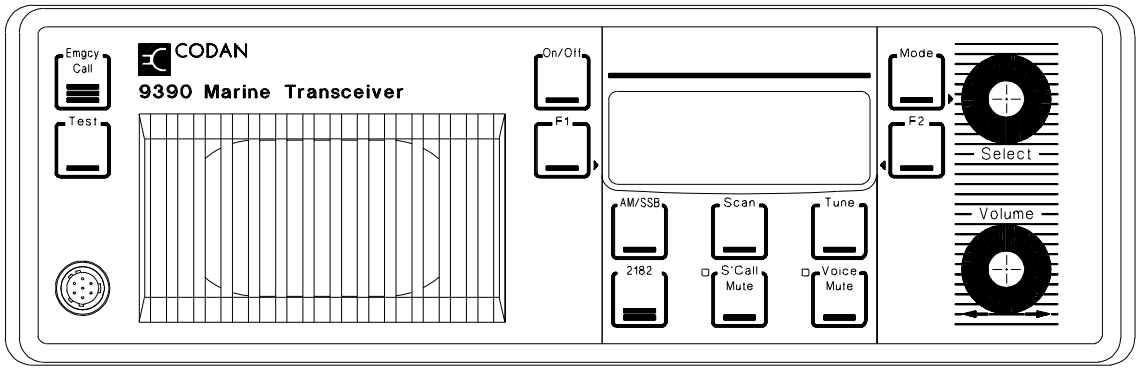

Figure 2 -5: Front panel and extended control head (9391) of HF SSB Transceiver 9390

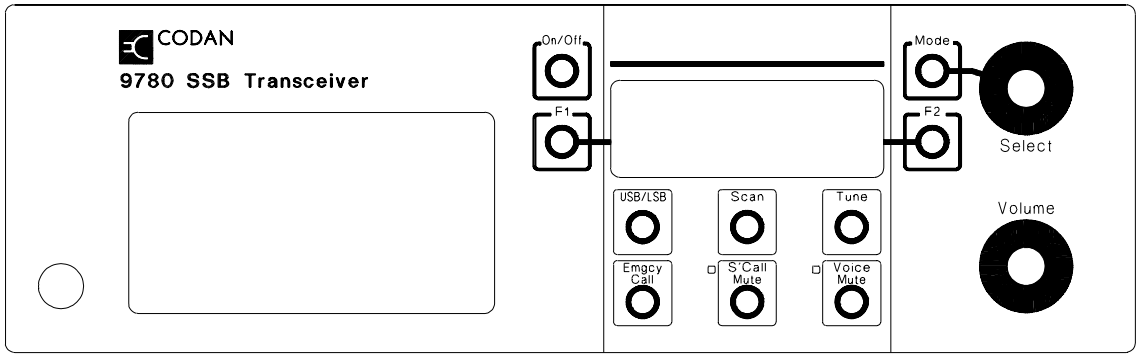

Figure 2 -6: Front panel of HF SSB Transceiver 9780

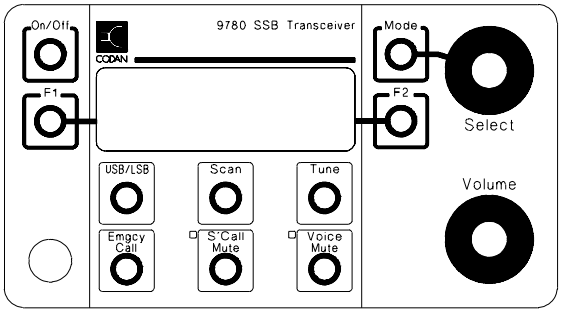

Figure 2 -7: Extended control head (9782) of HF SSB Transceiver 9780

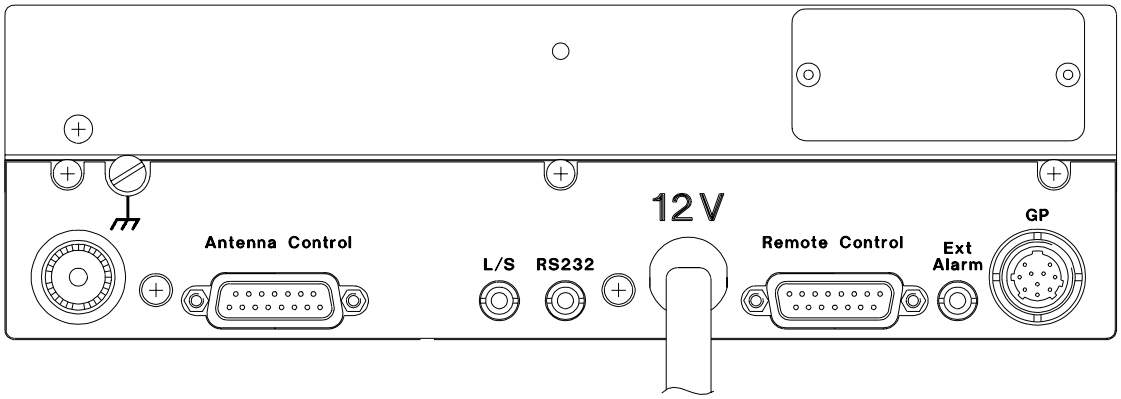

Figure 2 -8: Rear panel of HF SSB Transceivers 9323, 9360, 9390 and 9780

For an explanation of the function of knobs, buttons and connectors on these panels, see the relevant User Guide or Reference Manual. The User Guide for each transceiver type details the elements of the Liquid Crystal Display (LCD).

Specifications

Specification figures listed will normally be exceeded by production equipment. Where relevant, acceptance limits are given in brackets. All measurements are made at 13.6 V DC, with 50 Ω source and load resistances at 25°C ambient temperature (unless otherwise specified).

General specifications

Frequency range	9323 or 9390 Transmit: 2 to 26.5 MHz, (27 MHz CB band in Australia only) 9360 or 9780 Transmit: 2.25 to 30 MHz, (optional 1.6 to 30 MHz) Receive: 0.25 to 30 MHz
Channel capacity	9323 or 9360 Up to 400 single or two-frequency simplex channels 9390 Up to 650 single or two-frequency simplex channels 9780 Up to 15 single or two-frequency simplex channels
Frequency generation	All frequencies generated by synthesiser with 10 Hz resolution
Operating modes	Single sideband (J3E) USB or LSB or switched USB/LSB, (AM: H3E optional)
Frequency stability	USB: ±2 (3) ppm ⎫ -30°C to +60°C LSB: ±2 (3) ppm ±10 Hz ⎭ With high stability oven USB: ±0.5 (1) ppm LSB: ±0.5 (1) ppm ±10 Hz
Long term ageing	1 ppm per year
Oven warm up time	1 minute
Programming	Frequencies and options are programmed via the microphone socket or 3-wire RS232 interface using XP programming software and an IBM compatible PC Channels may be entered from the front panel by qualified personnel or (where authorised) by the operator
Cloning	Channel frequencies and options can be copied from one transceiver to another via the microphone socket
Controls	Sealed membrane switches on the control panel and microphone keypad Rotary controls for volume and select functions

Indicators	Refer to illustrations for details
Transmit/Receive switching	Using Option GP, 20 ms simplex operation, or 50 ms with up to 1 MHz of separation between Tx/Rx frequency
RF input/output impedance	50 Ω nominal
Supply voltage	13.6 V DC nominal, negative earth Normal operating range 10.5 to 15 V Maximum operating range 9 to 16 V
Overvoltage protection	Shut down at 16 V DC nominal for duration of overvoltage
Supply current	Receive: no signal 750 mA Transmit: see Transmit Specifications
Environment	Ambient Temperature — Relative Humidity -10°C to +30°C Head — 95% -30°C to +30°C TCVR — From 95% at +30°C +30°C to +60°C — to 30% at +60°C Note: -30°C Head to order Derate upper ambient temperature by 1°C per 330 m above sea level
Cooling	Convection or fan (Option F)
Size and weight	Transceiver only 250 mm W x 78 mm H x 350 mm D; 3.3 kg With mounting cradle 270 mm W x 90 mm H x 350 mm D Control head (9330/9366/9782) 130 mm W x 70 mm H x 40 mm D; 300 g With mounting cradle 150 mm W x 80 mm H x 40 mm D Control head (9391) 250 mm W x 78 mm H x 70 mm D; 750 g With mounting cradle 250 mm W x 90 mm H x 70 mm D Depth measurements include rear connectors/cables
Finish	Case: Silver-grey Panel surround and heat sink: Matt black Panel overlay: Lexan—Matt black (extended TCVR only) Painted surfaces are scratch-resistant textured polyester powdercoat

Receiver specifications

Type

Dual conversion,
superheterodyne

IF frequencies

45 MHz and 455 kHz

Sensitivity

Frequency	**RF Amp OFF**
0.25 to 2 MHz 2 to 26.25 MHz 26.5 to 30 MHz	Typical: 3 µV PD 0.35 (0.45) µV PD -116 (-114) dBm Typical: 0.5 µV PD -113 dBm
Frequency	**RF Amp ON**
2 to 26.25 MHz 26.5 to 30 MHz	0.12 (0.15) µV PD -125 (-123) dBm Typical: 0.18 µV PD -122 dBm

For 10 dB SINAD with greater than 50 mW audio output

Input Protection

Will withstand 50 V RMS RF from a 50 Ω source

Selectivity

Greater than 70 (65) dB at -1 kHz and +4 kHz reference SCF USB

Pass Band -6 (-8) dB
300 to 2600 Hz
Ripple 2 (4) dB PP
500 to 2500 Hz

Desensitisation

10 dB SINAD reduced to 7 dB SINAD
-1 and +4 kHz (ref SCF) 65 (60) dB

±10 kHz 80 (75) dB

±50 kHz 95 (90) dB

Blocking

As for Desensitisation

Image rejection

Better than 120 (110) dB

Spurious responses

Better than 90 (70) dB

Self generated signals > 0.35 µV PD:
7303, 9125, 10950, 12775, 14607, 18250, 20075, 21900, 23725 kHz

Cross modulation

A signal 90 (85) dB above a signal producing 10 dB SINAD, modulated 30% and removed at least 20 kHz from the wanted signal, will produce an increase in receiver noise of less than 3 dB

Intermodulation	To produce a third order intermodulation product equivalent to a wanted signal producing 10 dB SINAD, two unwanted signals greater than 30 kHz removed from the wanted signal must have a level greater than 82 (80) dB above the wanted signal
	Third order intercept (unaffected by AGC): +8 (+5) dBm with RF amp off -2 (-5) dBm with RF amp on
AGC	Less than 2 dB variation in output for input variation between 1.5 (2.5) µV and 100 mV PD
	Fast attack, slow release
AF response	Typical: −1 dB 300 Hz to 1 kHz Typical: −6 dB 1 kHz to 2.6 kHz
AF power and distortion	2.5 W into 8 Ω, 5% THD 4 W into 4 Ω, 5% THD 7 W into 2 Ω, 5% THD
Clarifier	Nominal: ±0.001%
	Clarifier is automatically reset to mid-frequency with channel change
Inband IMD	Better than 25 dB IMD with two 100 mV PD RF inputs
Signal to noise vs input signal	An increase of input level of 40 dB above the sensitivity level, increases the signal to noise at least 35 dB

Transmitter specifications

Power output 9323	100 W PEP at 2 MHz reducing with frequency to 85 W PEP at 26.5 MHz ±0.5 dB 27 MHz CB 10 W PEP
Power output 9360 and 9780	125 W PEP at 2.25 MHz reducing with frequency to 80 W PEP at 30 MHz ±1 dB CW or single tone: approximately 60% of PEP with average PEP control
Power output 9390	125 W PEP at 2 MHz reducing with frequency to 85 W PEP at 26.5 MHz ±1 dB
Duty cycle	100% normal speech over full temperature range 100% ARQ up to 30°C 25% of 16 tone continuous data mode (5 minutes on maximum) at ambient temperature up to 30°C 100% all modes up to maximum ambient of 45°C with Option F
Supply current	Output power: 100/125 W Two-tone or CW: 9 to 12 A Average speech: 6 A for battery life calculations

Protection	Safe under all load conditions by limiting reflected power to 10 W PEP and limiting PA transistor collector voltage swing Thermal protection against excessive heatsink temperature
AF response	Overall response of microphone and transmitter rises approximately 6 dB/octave 300 to 2700 Hz Electrical input -6 (-8) dB, 300 to 2600 Hz Ripple 2 (4) dB PP, 500 to 2500 Hz
Spurious and harmonic emissions	Better than 55 (45) dB below PEP
Carrier suppression	60 (50) dB below PEP
Unwanted sideband	70 (55) dB below PEP (400 Hz) 70 (65) dB below PEP (1 kHz)
Intermodulation (Two-tone test)	100 W: 30 (26) dB below each tone, 36 (32) dB below PEP 125 W: 27 (26) dB below each tone, 33 (32) dB below PEP
ALC	A 10 dB increase in signal input above compression threshold produces less than 0.5 dB increase in power output Maximum ALC range greater than 30 dB ALC attack time approximately 1 ms
Microphone	Dynamic type

Connectors

The following tables detail the pin connections and functions of the front and rear connectors. Details are also provided for the cables used for channel and cloning programming.

Microphone

Table 2 -1: Microphone connector (J3) pin function

Pin No.	Function	Signal Levels
1	Speaker Audio Output	12 V PP (max) 4 Ω (min)
2	Microphone Input	50 mV PP 12 kΩ I/P impedance
3	PTT Ground	0 V
4	Data In	0–5 V logic
5	PTT Active & Data Out	Active low, 0–12 V logic
6	"A" Rail	13.6 V nominal
7	To Front Panel Speaker	

Remote control

Table 2 -2: Remote Control connector (P204) pin function

Pin No.	Function	Signal Levels
1	Speaker	12 V PP 4 Ω min impedance
2	Remote PTT	5 V logic, Active low
3	EXT A/F I/P	Future use
4	Power On	Momentary 0 V = PWR On
5	Data I^2C	5 V logic
6	No Connection	
7	Clock I^2C	5 V logic
8	"S" & RF	4.5 to 0.25 V Rx 0 to 4.25 V Tx
9	0 V	Ground

Table 2-2 cont.

Pin No.	Function	Signal Levels
10	0 V	Ground
11	Tx A/F	250 mV threshold 10 kΩ I/P impedance
12	Rx DEMOD O/P	1.5 V PP
13	Rx A/F O/P Post Mute	1.5 V PP switched
14	INT I^2C	5 V logic
15	"A" Rail	+13.6 V nominal

Antenna control

Table 2 -3: Antenna Control connector (J202) pin function

Pin No.	Function	Signal Levels
1	Channel Number bit 4	Active low (Open Collector)
2	Channel Number bit 8	Active low (Open Collector)
3	EXT	
4	Tune In/Out	5 V logic, Active low
5	Scan Antenna	Active low (Open Collector)
6	No Connection	
7	No Connection	
8	PTT Out +10 V	1 kΩ source, Active high
9	Channel Number bit 1	Active low (Open Collector)
10	Channel Number bit 2	Active low (Open Collector)
11	Tuned In	5 V logic, Active low
12	"A" Rail	+13.6 V nominal
13	"A" Rail	+13.6 V nominal
14	Ground	0 V
15	Ground	0 V

External alarm

Table 2 -4: External Alarm connector (J305) pin function

Connections	Function	Signal Levels
Tip	External Alarm	Contacts rated 50 V, 1 A
Sleeve	Ground	Closed to ground for alarm

RS232

Table 2 -5: RS232 connector (J101) pin function

Connections	Function	Signal Levels
Tip	Data I/P	RS232 I/P
Ring	Data O/P	0–12 V O/P
Sleeve	Ground	Ground

Loudspeaker

Table 2 -6: External loudspeaker connector (J206) pin function

Connections	Function	Signal Levels
Tip	Speaker Audio Output	12 V PP max 4 Ω min impedance
Sleeve	Ground	0 V

Option GP, general purpose

Table 2 -7: Option GP connector (J304) pin function

Pin No.	Function	Signal Levels
1	0 V	Ground
2	Rx O/P	1.5 V PP
3	Tx I/P	170 mV PP Threshold
4	Q Line	+10 V I/P = On O/C = Off
5	Alarm I/P	5 V logic I/P
6	PTT	Input 0 V = PTT
7	SCAN	+10 V Output = Scan
8	"A" Rail	+13.6 V nominal
9	RS232 Rx	RS232 I/P
10	RS232 Tx	0–12 V logic O/P

Option M, morse

Table 2 -8: Morse connector (J204) pin function

Connections	Function	Signal Levels
Tip	Morse Input	5 V logic (Active low)
Sleeve	Ground	0 V

Programming cable

Codan part number 08-05137-001

Table 2 -9: Programming cable connector pin function

9-Way Computer Serial Port Socket	7-Way transceiver Microphone Socket	Pin Function
2	5	Data from transceiver
3	4	Data to transceiver
5 series Thermistor (Thermistor = 50 Ω 80°C)	3	Ground
	1/7 link	Speaker Link

Cloning cable

Codan part number 08-05138-001

Table 2 -10: Cloning cable connector pin function

7-Way Transceiver Microphone Socket	7-Way Transceiver Microphone Socket	Pin Function
4	5	Data I/O
5	4	Data I/O
3	3	Ground
1/7 link	1/7 link	Speaker Link

Options

The following options are available for 9323, 9360 and 9390:

Code	Options
ALE	Automatic Link Establishment
AM	Enable AM capability
ES*[1]	Emergency Selcall
F	Fit for continuous data transmission
GP	General Purpose interface
GPS	Global Positioning System capability
LF	Fit for 1.6 to 2.25 MHz transmit frequency range
M	Morse
PH	Headphone output
S*[2]	Selcall
SL*[1]	Selcall Lockout

*[1] Included as standard in the 9360
*[2] Included as standard in the 9323 or 9360, optional in 9390 only

The following options are available for 9780:

Code	Options
AM	Enable AM capability
LF	Fit for 1.6 to 2.25 MHz transmit frequency range
M	Morse
PH	Headphone output
S	Selcall with Selcall Lockout
ST	Selcall and Telcall capability with Selcall Lockout
D	Remote Diagnostics capability
TxD	Programming of transmit frequencies from the front panel is disabled

3 Brief description

This section of the manual provides a brief description of the major components and circuit functions of the 9323, 9360, 9390 or 9780 transceiver as follows:

- control and switching functions
- synthesiser operation
- receive path
- transmit path

For an in-depth review of these functions see chapter 4 , *Technical description*.

General

Read this description of the 9323, 9360, 9390 or 9780 transceiver in conjunction with the Block Diagram 03-00902.

The 9323, 9360, 9390 or 9780 transceiver uses the same double conversion in Receive and Transmit modes. Only the 45 MHz band-pass filter, the 455 kHz sideband filter and the local oscillators VCO1 and VCO2 are common to both modes of operation. The signal routing is determined by switching and control voltages according to the mode selected.

The circuits and functions of the 9323, 9360, 9390 or 9780 are located on four major PCBs as shown in Figure 3-1:

- Display panel PCB
- Microprocessor and audio PCB
  Micro and I/O
  Transmit audio
  Receive audio and Selective call
- Rx/Exciter PCB
  RF Mixer and synthesiser
  455 kHz IF modulator and demodulator
- PA and Filter PCB

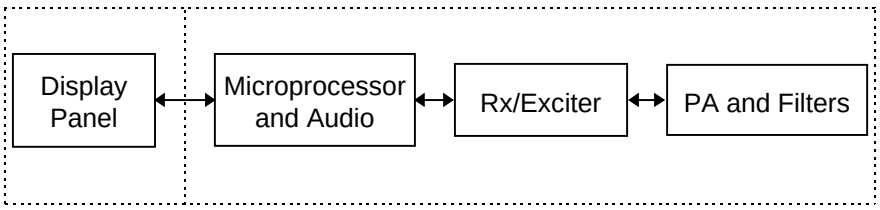

Figure 3 -1: 9323, 9360, 9390 and 9780 PCB block diagram

Control and switching

Most of the transceiver functions are microprocessor controlled. The channel frequencies are programmed via the microprocessor to the Electrically Erasable Programmable Read Only Memory (EEPROM). The remaining facilities are pre-programmed in the Erasable Programmable Read Only Memory (EPROM).

The power On function is controlled by hardware and the power Off function is controlled by software. The rotary volume control is a digital contacting encoder. It controls a 16-step attenuator in the audio signal path between the preamplifier (after the demodulator) and the amplifier. This drives the loudspeaker.

Synthesiser

The 9323, 9360, 9390 or 9780 transceivers use single loop synthesisers. The main synthesiser (VCO1) generates an oscillator frequency in 2 kHz steps. In receive, the oscillator frequency ranges from 45.250 MHz to 75 MHz. In transmit the oscillator frequency will depend on the transceiver type and the options fitted. It will be within the range of 46.6 MHz to 75 MHz.

The vernier synthesiser (VCO2) generates oscillator frequencies of 44.5435 MHz to 44.5455 MHz in 10 Hz steps.

The synthesisers are controlled by the same process that controls the remainder of the transceiver. Serial data representing the various pre-programmed channel frequencies is loaded into both synthesisers.

When upper sideband is selected, the 9323, 9360, 9390 or 9780 uses a single crystal reference oscillator of 7304 kHz. The reference oscillator is also used to provide the 456.5 kHz (7304 kHz divided by 16) signal for the audio modulator/demodulator.

For lower sideband operation a separate crystal oscillator is selected, operating at 1814 kHz to provide 453.5 kHz (1814 kHz divided by 4) to the audio modulator/demodulator.

Receive path

PA and Filter PCB

The received signal from the antenna passes through a PA low-pass filter, onto the transmit/receive relay. It is then sent to the receiver input on the Rx/Exciter PCB.

Rx/Exciter PCB

From the receive input, the signal passes through a selected high-pass filter and is fed either directly to a 30 MHz low-pass filter or via an RF amplifier. The output of the low-pass filter is fed to the input of the first balanced mixer. Here it mixes with the local oscillator VCO1 to produce an IF signal centred on 45 MHz.

The 45 MHz signal is filtered using a 15 kHz wide band-pass filter before being applied to the second balanced mixer. The signal mixes with a second local oscillator VCO2 producing an IF signal centred on 455 kHz.

The output of the second mixer divides into two paths:

- the main path passes the signal through a noise gate to a 2.5 kHz sideband filter where only the wanted sideband passes to the high gain AGC controlled IF amplifier
- the second path passes the signal through an amplifier that detects noise and controls the noise gate to remove impulse noise, such as car ignition, from the 455 kHz signal

The amplified 455 kHz signal is demodulated to produce an audio signal. It is then amplified. The amplified audio signal operates an AGC circuit. This controls the IF amplifier gain to prevent overloading when receiving strong signals. It is also used to maintain a constant audio output with changing input signals.

The amplified audio signal is fed via a mute gate to the volume control. The mute, when enabled, removes the receiver noise from the speaker. When speech is detected, the gate in the audio line closes to allow the signal to be heard.

The signal from the volume control is applied to a power amplifier IC to drive the transceiver's loudspeaker.

Transmit path

Microprocessor and Audio PCB

The microphone audio is amplified and levelled in the microphone amplifier/compressor, then fed to a balanced modulator.

Rx/Exciter PCB

When mixed with the local oscillator, the double sideband output of the modulator is applied to a 2.5 kHz sideband filter centred on 455 kHz, passing only the wanted sideband to the first mixer. Here it mixes with the local oscillator VCO2 to produce an IF signal centred on 45 MHz.

The transmit signal is filtered by the 15 kHz wide band-pass filter before being fed to the input of the second mixer.

At the second mixer, the signal mixes with the output of oscillator VCO1 to produce the required channel frequency. It passes through a 30 MHz low-pass filter to the PA and Filter PCB.

PA and Filter PCB

On the PA assembly, the signal is amplified, then it is passed through the transmit/receive relay to the selected band filter. The output from the filter is fed via the VSWR detector to the antenna output connector. From here it is connected by coaxial cable to the antenna.

The VSWR detector monitors the forward and reflected power and controls the power output of the transmitter. If a high VSWR is detected, the power output is reduced to protect the PA.

4 Technical description

This section of the manual contains a technical description of the 9323, 9360, 9390 or 9780 transceiver and 9330, 9366, 9391 or 9782 control head. It should be read together with the drawings in chapter 9, *Drawings*.

Control and supply voltages

All switching, except power On, is controlled either directly or indirectly by the microprocessor IC101 (located on the Microprocessor and Audio PCB) in conjunction with the microprocessor IC2 in the control head.

Power on

🗁 04-02974
When the **On/Off** button on the control panel is pressed, the PWR ON line (P4 pin 3) is pulled low via the series circuit consisting of diode D1 on the **On/Off** button and D3.

The cathode of D3 is at 0 V prior to switch on, permitting the PWR ON line to momentarily be held low by discharged capacitors on the 5 V rail.

🗁 04-02976 Sheet 2
The PWR ON line on the front panel is connected via a short cable to P201 pin 3 located on the Microprocessor and Audio PCB. From there it is fed via R222 to the base of transistor V203.

🗁 04-02976 Sheet 2
The PWR ON line from the extended control head is connected by a control cable to the transceiver rear panel connector P204 pin 4, then via a ribbon cable to the Microprocessor and Audio PCB (P203 pin 7). From there it is fed through an RF suppression network (L205 and C236) then connected in parallel to the front PWR ON line, then via R222 to the base of V203.

With the PWR ON line low, V203 conducts and energises the ON coil of latching relay K201 resulting in contacts K201 closing and applying a ground to the TCVR ON line.

The TCVR ON line is connected from the Microprocessor and Audio PCB via P101 pin 3 (see Sheet 1) to P1 pin 3 on the PA assembly [🗁 04-02973 and 04-03096] and finally to the negative side of relay K8.

If the polarity of the DC supply is correct and below 16 V, V4 will conduct and relay K8 will energise, closing contacts K8-1 and connecting the DC supply to the transceiver. The PWR ON line is disabled on start up when D3 on the control head is reverse biased by the 5 V supply.

If the DC supply voltage exceeds 16 V, zener diode V2 conducts causing V3 to also conduct and switch off V4, thus preventing K8 from energising.

Diode D7 prevents relay K8 from operating if the DC supply is reverse polarised.

The power input circuit is protected from high voltage transients by Voltage Dependent Resistor (VDR) R8.

Power off

If the **On/Off** button on the control panel is pressed [🗁 04-02974] when the transceiver is operational, a scanning active low pulse from the microprocessor IC2 pin 11 is applied to the input port of IC1. The interrupt line (pin 13) momentarily goes low, indicating to the microprocessor IC2 to read the input ports of IC1 and to switch off the transceiver.

The switch off command is sent from IC2 (pins 22 and 23) via the external I^2C bus to microprocessor IC101 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1] pins 22 and 23.

Microprocessor IC101 outputs data on the local I^2C bus to IC109 pins 23 and 24, latching pin 5 on the PWR OFF line low. The OFF coil of latching relay K201 (see Sheet 2) energises, opening K201 contacts and releasing the power relay K8 on the PA assembly, thus switching off the transceiver.

Supply voltages

The supply voltages on the Display Panel PCB [🗁 04-02974] are shown in Table 4-11.

Table 4 -11: Display Panel PCB supply voltages

Supply	Description	Regulator
"A" rail	unregulated battery supply	
"B" rail	10 V regulated supply	IC9
+5 V	5 V regulated supply	IC11
-7 V	-7 V from charge pump supply	IC7

The supply voltages on the Microprocessor and Audio PCB [🗁 04-02976] are shown in Table 4-12.

Table 4 -12: Microprocessor and Audio PCB supply voltages

Supply	Description	Regulator
"A" rail	unregulated battery supply	
"B" rail	10 V regulated supply	IC201
+5 VA	5 V regulated supply	IC202
+5 VB	5 V regulated supply	IC203

The supply voltages used on the Rx/Exciter PCB [🗁 04-02972] are shown in Table 4-13.

Table 4 -13: Rx/Exciter PCB supply voltages

Supply	Description	Regulator
"A" rail	unregulated battery supply (supplies the crystal oven only)	
"B" rail	+10 V regulated supply	IC201*
+5 VB	5 V regulated supply	IC203*
+18/26 V	18 & 26 V from the charge pump supply	IC11

* Regulator is located on the Microprocessor and Audio PCB [🗁 04-02976]

The supply voltages on the PA and Filter PCB [🗁 04-02973 and 04-03096] are shown in Table 4-14.

Table 4 -14: PA and Filter PCB supply voltages

Supply	Description	Regulator
"A" rail	unregulated battery supply	
+5 V	5 V regulated supply selected in transmit only	IC2
+5 V	5 V supply (supplies IC1 only)	V1

Receive/Transmit switching

The main transmit/receive DC switching circuit originates from the latched output of IC209 pin 6 located on the Rx/Exciter PCB [🗁 04-02972 and 04-03135 Sheet 2]. IC209 pin 6 is connected to two transistors V209 and V212. V209 governs the AGC function. V212 forms part of the circuit controlling the transmit and receive mixer circuits.

When the Receive mode is selected, the output of IC209 pin 6 is latched to 0 V, switching V209 off and allowing the AGC to function normally. V212 is also switched off, allowing the first NAND gate of IC6/D to be pulled high by resistor R42. This sets the output of IC6/D pin 11 low, switching on V2 and V6, thus enabling the receive mixers IC4 and IC7. The output of the second NAND gate IC6/C will go high, switching V3 and V7 off and inhibiting the transmit mixers IC5 and IC8.

When the PTT inputs are detected by the microprocessor IC101 [🗁 04-02976 Sheet 1] it sends a command via the local I^2C bus to IC209 [🗁 04-02972 and 04-03135 Sheet 2] to latch the output pin 6 high (+5 V). This causes V209 in the AGC circuit to conduct, setting the AGC to 0 V and disabling the 455 kHz IF amplifier. Resistor R255 provides a small DC offset to IC205/A to ensure the AGC always switches to 0 V.

With IC209 pin 6 latched high, V212 conducts, setting the input of IC6/D pin 13 low. This in turn sets the output of IC6/D pin 11 high, thus switching off V2 and V6, disabling the receive mixers IC4 and IC7 and providing the DC voltage to enable the transmit mixers IC5 and IC8.

The noise limiter in Transmit mode is disabled by V7 conducting, thus applying a DC level via D201 and R203 (see Sheet 2) to the AGC input pin of noise amplifier IC201 pin 5.

DC from V7 has two other functions. It provides bias via R238 to IC202 pin 5 to enable the modulator. It also biases V5 (see Sheet 1) on, clamping the base of V4 to 0 V, thus preventing D19 from conducting and attenuating the transmit signal.

Serial data from the microprocessor IC101 [🗁 04-02976 Sheet 1] is also applied to IC1 on the PA assembly. When transmit is selected, a ground on pin 12 energises the transmit/receive relay K7. The path is now completed from the PA output to the antenna.

In Transmit mode, the microprocessor IC101 outputs a low from pin 28. This is applied to the input of inverter buffer IC207 pin 12 (see Sheet 2). The high at the output pin 14 is connected to:

- the antenna control connector P202 pin 15
- the optional PCB output P204 pin 12
- the mute squaring amplifier IC307/B via R365 and D307 (see Sheet 3)

The DC applied to IC307/B applies a small offset to disable the squaring amplifier during transmission.

Receiver

Input low-pass filters

🗁 04-02973 and 04-03096
The receiver input signal is fed through one of six relay-selected, PA Low-Pass Filters (LPF) K1–K6. The signal is then fed via the transmit/receive relay K7 and signal clamping diodes D3–D6 to connector J3.

High-pass filters

🗁 04-02972 and 04-03135 Sheet 1
From J3 on the PA assembly, the High-Pass Filter (HPF) is connected by a coaxial cable to J2 located on the Rx/Exciter PCB. Six HPFs are used to complete the band-pass filter (BPF) characteristics. These are diode switched according to the frequency band in use, by grounding the appropriate select line from IC1. For broadcast channels below 2 MHz, a 14 dB resistive attenuator is selected instead of a filter.

This is an example of how the HPF works. If the HPF 2-3.1 is selected, IC1 pin 10 switches from 10 V to 0 V. This completes the input DC switching current path from the "B" rail via R2, L1, D11, L18 and R14 to 0 V. Diode D11 is forward biased and passes the receive signal to the input of the selected HPF.

The output DC switching current path from the "B" rail consists of R3, L2, D12, L20 and R15 to 0 V. With D12 forward biased, the receive signal at the output of the 2-3.1 HPF can either be fed directly via D15 and C57 to the following 29 MHz low-pass filter (LPF) or via D16 to the input of the RF amplifier.

RF amplifier

🗁 04-02972 and 04-03135 Sheet 1
The RF amplifier (consisting of V1 and its associated components) has a nominal gain of 12 dB. It can be selected from the front panel on the control head. When the RF amplifier is selected, IC2 pin 12 goes high, switching the output of IC3/A and B (in parallel) from 0 V to approximately 10 V. This action applies DC volts via RF filter inductor L27 to the primary of T2, then to the series inductors of the LPF L26-L24 to the collector of V1. The DC volts also forward biases V1 via feedback resistor R24.

With the RF amplifier selected, the voltage on the base of V1 is positive with respect to the output of the HPF network, thus forward biasing D16. This allows the signal to pass to the input of the RF amplifier. At the same time, D15 is switched off, as the cathode is held approximately 2 V positive with respect to the anode.

LPF and first mixer

🗁 04-02972 and 04-03135 Sheet 1
The output from the HPF is fed direct, or via the RF amplifier, to a 29 MHz LPF (C59, L24, C60/61, L25, C62, & L26) and then via transformer T2 to the balanced input of the first mixer IC4 pins 12 and 13.

Mixer IC4 is a combined amplifier/balanced mixer with a gain of approximately 20 dB. The received signal is mixed with the output of the Voltage Controlled Oscillator (VCO1), then applied to pin 5. This operates between 45.250 MHz and 75 MHz to produce a balanced IF output (pins 3 and 14) centred at 45 MHz.

DC is applied to the mixer IC4 pins 3 and 14 via the filtered "B" rail and the centre tap of the mixer output transformer T3. In Receive mode, V2 is conducting and supplies the filtered "B" rail to IC4 pin 4 and 11, via R34 and R36 respectively.

45 MHz band-pass filter

🗁 04-02972 and 04-03135 Sheet 1
The 45 MHz IF signal is filtered through a 15 kHz BPF (centred on 45 MHz) consisting of T3, Z1, L30, Z2 and T4. This removes unwanted signals produced by the first mixer. The filtered output is applied via coupling capacitors C84 and C85 to the balanced input of the second mixer IC7 pins 12 and 13.

Second mixer

🗁 04-02972 and 04-03135 Sheet 1
Mixer IC7 is a combined amplifier/balanced mixer and identical to mixer IC4. The 45 MHz signal is mixed with the output of the second Voltage Controlled Oscillator (VCO2), then applied to pin 5. This operates between 44.5435 MHz and 44.5455 MHz to produce a second IF centred at 455 kHz.

DC to the mixer output is provided by the filtered "B" rail, which is connected to the centre tap of the 455 kHz output transformer T201 (Sheet 2). It is then fed to the mixer output transformer T3. In Receive mode when V6 is conducting, the "B" rail provides DC via R45 to IC7 pin 4 and bias via R47 to pin 11.

Noise limiter

🗁 04-02972 and 04-03135
The 455 kHz output of IC7 pins 3 and 14 is applied via C201, R201, C202 and R202 to the balanced input of a high gain amplifier IC201 pins 4 and 6.

The balanced outputs at pins 1 and 8 are connected to a tuned auto transformer T202 (455 kHz). The output of T202 is applied to the base of V201, which is an active rectifier. Noise bursts produce positive going pulses at the collector of V201 and trigger, via V202, the monostable flip-flop IC6A/B. The pulse width is determined by C208 and R210 (nominally 250 μs).

The outputs of the flip-flop pins 3 and 4 produce complimentary pulses that are connected to the FET gates of V204 and V205. These gate out the noise bursts from the 455 kHz signal. With V204 on and V205 off, the IF signal is passed to the sideband filter Z202. When a noise burst is present, V204 is switched off and V205 is switched on, blocking the IF signal for the period of the gate pulse.

The average DC component of V201's collector current is used as an automatic gain control to IC201. It is applied via R206 to pin 5. This ensures that only the noise burst signal triggers the monostable. The AGC decay constant is set by the components C204 and R205.

In transmit, IC201 is disabled (see page 4-4, *Receive/Transmit switching*).

455 kHz filter and IF amplifier

🗁 04-02972 and 04-03135 Sheet 2
The IF signal from the noise blanker gate V204 is applied to a 2.5 kHz ceramic filter Z202. The filter removes the unwanted sideband, adjacent channels and other unwanted products generated by the second mixer. The wanted sideband, centred at 455 kHz, is passed by the filter to a two-stage gain controlled amplifier, consisting of V207, V208, and its associated components.

The IF amplifier is broadly tuned to 455 kHz by the tuned circuits L202/C219 and L203/C223.

Demodulator

🗁 04-02972 and 04-03135 Sheet 2
The output of the 455 kHz IF amplifier is passed via coupling capacitor C224 to the input of a double balanced mixer IC203 pin 1. The IF signal is mixed with the local oscillator that is applied to pins 8 and 10 to produce an audio output at IC203 pin 6. The local oscillator operates at 456.5 kHz for USB conversion and 453.5 kHz for LSB. For details of operation of the local oscillator see page 4-18, *455 kHz local oscillator for USB/LSB.*

Local oscillators VCO1 and VCO2 shift by a total of 3 kHz when switching from USB to LSB. This enables filter Z202 to be used for either sideband.

Automatic gain control

🗁 04-02972 Sheets 1 and 2
An Automatic Gain Control (AGC) is applied to a number of stages in the receiver. This is used to increase the dynamic range of the receiver and to maintain an almost constant audio output level for a large variation of input signals.

When the receiver is at maximum gain, the AGC at the output of IC205/A pin 1 (TP205) (see Sheet 2) is nominally 5.5 V. This is set by the resistor divider R257 and R258 in conjunction with the gain setting resistors R254 and R259.

The demodulated audio output from IC203 is first amplified by IC204/A then passed via a resistive attenuator (R263 and R264) to a full wave active peak rectifier circuit V210 and V211.

Under no signal conditions, IC204/A output, V210 and V211 bases and emitters are all at the same potential of 5 V. When the audio swing at the output of IC204 exceeds approximately ±0.75 V (from 5 V), it causes V210 to conduct during the positive peaks and V211 during the negative peaks. The common collector output charges capacitor C237 during the transistor's conducting period. The resulting DC is applied to inverting amplifier IC205/A causing the AGC output to drop to a level determined by the strength of the received signal. This lowers the voltage applied to gate 2 of both FETs V207 and V208, reducing the overall gain of the 455 kHz IF amplifier.

AGC is applied to a second inverting amplifier IC204/B to extend the dynamic range of the receiver. Its output produces an inverted AGC, nominally 0 V under a no signal condition, but starts to rise once the input to IC204/B falls below 3.2 V (set by R249 and R250).

The inverted AGC from IC204/B is divided into two paths:

- one path is connected via R223 to gate 1 of V207, improving the gain control of the 455 kHz IF amplifier
- the second path is via a delay and damping network (R221/V206, R220, C215, D203, and R41) to the base of V4 (see Sheet 1)

The pin diodes D19 across the first mixer output act as variable resistors. The resistance falls as V4 collector current increases with a rise in AGC, thus reducing the mixer output gain at high signal levels.

Another AGC circuit is incorporated at the output of the second mixer. It is used for signals that are out of the 2.5 kHz sideband frequency, but within the 15 kHz BPF bandwidth (see Sheet 1). V15 is connected between one side of the balanced output and the "B" rail. When the output swing from the mixer IC7 exceeds 0.7 V between the base and the rail, V15 conducts and reduces the gain of the first mixer by increasing the current through the pin diodes D19.

The AGC fast attack time is set by R262, R263 and R264 in the emitter circuit of the peak rectifiers V210 and V211 (see Sheet 2). Capacitor C237 charges and the resultant slow decay time of C237 is through the resistor network R260 and R259. The attack and decay time will vary at different signal strengths, but nominally are about 2 ms and 0.5 s respectively. Resistor/diode networks R276/D207 and R277/D208 are connected to outputs on IC209 (pins 4 and 5) and can be grounded, under software control. This reduces the AGC decay time constant when required for special applications.

Voice mute

🗁 04-02976 Sheets 1, 2 and 3
The audio at the output of IC204/A on the Rx/Exciter PCB [🗁 04-02972 Sheet 2] is connected via P201 pin 9 (Rx Audio) to the Microprocessor and Audio PCB pin 9 (see Sheet 2). It is then coupled via C206 to the input of IC307A (see Sheet 3), which operates as a squaring amplifier. At the open collector output, the squared signal across load resistor R352 charges C343 via D308 during the negative excursions. The charge is transferred to C344 by V303 during the positive excursions. The resultant DC voltage on C344 is proportional to the frequency of the audio (i.e. voltage rises as frequency increases). The squaring amplifier is disabled in transmit by applying a DC offset from IC207 pin 14 (Sheet 2) via D307 and R365 to IC307/B pin 5.

IC304/B and its associated components function as an LPF with a cut-off frequency of approximately 10 Hz. The output from IC304/B is a DC voltage varying at the syllabic rate of the received speech.

IC307/C and IC307/D form a window comparator. The window width is adjusted by the mute sensitivity preset R357. The divider network R359 and R360 together with C348 averages the output of IC304/B to provide the reference voltage for the window comparator. If the output from IC304/B rises or falls below this reference by the amount set by R357, then the open collector outputs of IC307/C and IC307/D will discharge C349, applying a low to the input of comparator IC307/B pin 6.

The second input of comparator IC307/B pin 7 is set to 4 V by resistor divider R363 and R364. When input pin 6 falls below 4 V, the comparator output at pin 1 goes high (MUTE DET line). This indicates to the microprocessor IC101, via IC111 pin 5 (see Sheet 1), that speech has been detected.

Mute detection timing is controlled by discharging C349 through R361 for a fast attack and charging C349 via R362 for a slow release (about 3 seconds).

When Voice Mute mode is selected by the **Voice Mute** button on the control panel [🗁 04-02974], the microprocessor IC2 on the control head sends a signal via the external I^2C bus to the microprocessor IC101 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1]. The microprocessor IC101/A sends a command via the local I^2C bus to IC114 to latch the mute switch pin 19 low. This applies a low to IC206/D pin 12 (see Sheet 3), which opens the mute gate and only allows a very low level of audio to pass via R330 (when fitted) to the volume control circuit.

When voice is detected by the mute circuit, a high is applied to IC111 pin 5 (MUTE DET line). The interrupt pin (pin 13) momentarily goes low, informing the microprocessor to read the input ports of IC111. This will indicate to the microprocessor that the mute detect line is high. The microprocessor then sets the mute switch IC114 pin 19 high and closes the mute gate IC206/D (see Sheet 3). The audio is then passed to the volume control circuit.

Volume control and audio output amplifier

🗁 04-02974, 04-02976 Sheets 1 and 3
The volume control circuit is a 16-step attenuator and consists of R334–R340. Each step has ≈4 dB of attenuation, giving a total of 64 dB.

The rotary volume control is a digital contacting encoder. When this control is rotated in either direction, the microprocessor IC2 on the Display Panel PCB [🗁 04-02974] reads each position change. It sends commands via the external I^2C bus to the microprocessor IC101 on the Microprocessor and Audio PCB (see Sheet 1) to select the appropriate audio attenuators. The microprocessor IC101 then sends data via the local I^2C bus to change the output ports of IC114 pins 3–6. This action controls the analogue switches that switch the step attenuator in and out.

The audio is passed from the buffer amplifier IC304/A, through a resistor attenuator R342 and R343, to the input of the loudspeaker amplifier IC306.

The maximum output of the audio amplifier is either:

- 2.5 W into an 8 Ω speaker
- 8 W into a 2 Ω speaker

Warning beeps are heard if the maximum or minimum limits of the volume control are reached. The warning beeps are generated from the tone generator IC106 pin 10 [🗁 04-02976 Sheet 1]. The tone is fed via a resistor attenuator network to the input of the loudspeaker amplifier IC306 (BEEPS I/P line). The beep audio level is varied by the volume control. The level is controlled by the microprocessor, which selects the appropriate attenuator shunt resistors (R138, R140 and R142) to ground (IC109 pins 8, 9 and 10).

Low voltage Tx inhibit

🗁 04-02972 and 04-03135 Sheet 2
The comparator IC211A on the Rx/Exciter PCB monitors the "A" rail. When the supply voltage drops to 9 V, the output of IC211A is pulled low thus disabling the PTT line connected from IC209 pin 6 via R275 to transistor switch V212. This function prevents the transceiver latching in Tune mode when the supply voltage drops below 9 V.

Transmitter exciter

Microphone amplifier/compressor

🗁 04-02974 and 04-02976
The microphone insert is a moving coil device and is active when the **PTT** button is pressed. This removes the short circuit across the microphone, and at the same time, applying a ground to the PTT line on J1 pin 5.

The microphone is connected to the control panel via J3 pins 2 and 3 [🗁 04-02974] and to the PCB via P3 pins 1 (ground) and 5. From there, the microphone audio is passed through an RF filter network R24 and C21 to the input of the preamplifier IC10/B.

When the microphone is not in use, the input switch (consisting of transistor V10 and associated components) disables the audio by applying a short across the input.

The audio output of amplifier IC10/B is fed through an RF decoupling network (R40, C41 and R44) to connector P4 pin 2. In the front panel control version, the audio is connected to P201 pin 2 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 2). From there it is fed via capacitor C219 and analogue switch IC206/A to the combining amplifier IC204/A.

For the control head version, the Tx audio at connector P4 pin 2 is fed via a control cable to P204 pin 11 on the transceiver. From there the output is connected via a ribbon cable to P203 pin 6 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 2]. The audio path continues from pin 6 via a second RF suppression network (R229/B and C242), through C218 and analogue switch IC206/C to the combining amplifier IC204/A.

Additional audio inputs are applied to the combining amplifier IC204/A from:

- the tone generator IC106 via R213
- the optional PCB (P204 pin 3) via R214
- the option PS input (P303 pin 5) via C217, analogue switch IC206/B and R216

The microphone audio at the output of IC204/A is applied to the input of a microphone compressor amplifier consisting of IC204/B, IC205/A and B, V202 and associated components. This provides a constant output for a large variation in speech levels applied to the input (≈30 dB range).

When there is no speech present, the amplifier IC204/B is set to the maximum gain. This is determined by the feedback resistor R208 and the shunt FET V202, which functions as a variable resistor (minimum resistance is ≈150 Ω for maximum gain).

The output of amplifier IC204/B is connected to the inputs of IC205/A and IC205/B forming a window comparator. The window is set by the divider chain R204–R207 to be centred at 5 ±0.25 V.

When the level of the speech input applied to the microphone amplifier is greater than ≈3.5 mV P (compression threshold), the output swing will exceed the comparator window (±0.25 V). This produces negative going output pulses from the comparator IC205/A and B pins 1 and 7. These pulses lower the DC charge on capacitor C212. The effect is that the voltage will be reduced on the FET gate of V202. This increases the resistance of the FET and lowers the gain of the microphone. This puts the microphone amplifier into compression. The output level remains constant for a further 30 dB increase in input level before overloading occurs.

Under normal speech conditions, the time constant (consisting of C212 and R211), sets the talk power ratio and produces a high average transmission power level. When data transmission is required, the time constant is extended by switching in capacitor C213 in parallel to C212 (TALK PWR OFF line). This is achieved by a command from the microprocessor IC101 [🗁 04-02976 Sheet 1] to set the output port of IC114 pin 10 low, thus grounding the negative side of C213.

When lower power is required for CB channels, the drive level to the PA is reduced by the microprocessor IC101 setting IC114 pin 9 low. This causes FET V201 (see Sheet 2) to switch on and apply R203 in parallel to resistors R205 and R206. This action reduces the comparator window to ±0.125 V, resulting in a reduction of 6 dB in the audio output from the microphone compressor amplifier IC204/B.

Modulator

🗁 04-02972 and 04-03135 Sheet 2
The transmitter audio output of IC204/B is passed via P102 pin 4 to the RF/Exciter PCB P201 pin 4. The output is then fed to the input of the balanced modulator IC202 pin 1. The modulator is enabled when DC is applied via the transistor switch V7 and R238 (Sheet 1) to the bias input pin 5.

The audio is mixed with the local oscillator of 456.5 kHz (453.5 kHz for LSB) and is applied to pin 8 and 10 (see page 4-18, *455 kHz local oscillator for USB/LSB*). This produces a DSB output at pin 6. From there it is passed via D204 to the 455 kHz sideband ceramic filter Z202 pin 1.

455 kHz filter and first mixer

Filter Z202, with a bandwidth of 2.5 kHz, filters out the unwanted sideband leaving only the wanted sideband at pin 3. From there it is fed via the noise limiter gate V204 (disabled in transmit) to a tuned auto transformer T201. It is fed from T201 via a resistor matching attenuator network R48 and R49 [🗁 04-02972 and 04-03135 Sheet 1] to the input of the first balanced amplifier/mixer IC8 pins 12 and 13.

The first mixer IC8 (see Sheet 1) is enabled by operating transistor switch V7, applying DC via R46 to pin 4 and bias current via R50 to pin 11. The filtered "B" rail is applied to the mixer output pins 3 and 14 via the centre tap of output transformer T4.

In the first mixer IC8, the 455 kHz transmit signal is mixed with the output of the local oscillator VCO2. This is applied to pin 5 to produce a second IF output signal centred on 45 MHz (pins 3 and 14). The gain of the mixer/amplifier is approximately 20 dB.

45 MHz band-pass filter

The 45 MHz IF signal is filtered through a 15 kHz BPF consisting of T4, Z2, L30, Z1 and T3. This removes unwanted signals produced by the first mixer. The filtered output is applied to the balanced input of the second mixer IC5 pins 12 and 13.

Second mixer and exciter output filter

The second mixer IC5 is enabled by operating the transistor switch V3. This applies DC through R35 to pin 4 and bias current via R38 to pin 11. The filtered "B" rail is applied via preset resistor R22 and transformer T1 to the mixer output pin 3 and 14.

The 45 MHz transmit signal is mixed with the output of local oscillator VCO1 then applied to IC5 pin 5 to produce the selected channel frequency at the mixer output (pins 3 and 14). The gain of the mixer/amplifier is approximately 20 dB.

The balanced network, consisting of components R22, C55 and C56, is adjusted to remove unwanted spurious signals.

The mixer output is fed via a 29 MHz low-pass filter (consisting of L23, C53, C51/52, L21 and C50) to the transmit exciter output connector J1. From there it is coupled via a coaxial cable to the PA assembly.

Tune

When the **Tune** button is pressed [🗁 04-02974], a low is applied to the input port of IC1. The interrupt pin (pin 13) momentarily goes low indicating that the microprocessor IC2 has to read the input port of IC1. It also detects that the **Tune** button has been pressed. The tune command will be sent via the external I^2C bus to the microprocessor IC101 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1].

The microprocessor IC101 outputs data on the local I^2C bus to IC209 on the Rx/Exciter PCB [🗁 04-02972 and 04-03135 Sheet 2] to latch output at pin 6 high and pin 10 low.

The high on IC209 pin 6 enables the transmit mixers and disables all of the receive functions (see page 4-4, *Receive/Transmit switching*).

The output pin of IC209 pin 10 is connected to a NOR gate IC206/A pin 2. When pin 2 is low, the 456.5 kHz carrier (453.5 kHz for LSB), which is always present at IC206/A pin 3, then appears at the output (pin 1). This applies the carrier signal via the driver transistor V203 to the input transformer T201 of the first transmitter mixer IC8.

The output pin of IC209 pin 10 (see Sheet 2) is also connected to the input of the NOR gate IC206/D pin 11. When pin 11 is low, the output (pin 13) is set high, biasing V202 into saturation. The output of the second cascade NAND gate IC6/B pin 4 goes low, opening the FET gate V204. This stops the re-inserted carrier from being loaded by the sideband filter Z202.

The carrier appearing at the output of the second mixer IC5 will be at the frequency of the selected channel (SCF) and is used for tuning automatic and manual antennas.

Local oscillators

General

🗁 04-02972 and 04-03135 Sheet 1
Two digitally controlled synthesised local oscillators are used to drive both the transmit and receive functions of the first and second mixers. VCO1 operates between 45.25 MHz and 75 MHz, moving in 2 kHz steps. VCO2 operates in the range of 44.5435 MHz to 44.5455 MHz, moving in 10 Hz steps.

The synthesisers IC10 and IC13 are programmed in serial data format from the microprocessor IC101 [🗁04-02976 Sheet 1], which accesses the channel data stored in the E^2PROM memory.

Each synthesiser is locked to the reference oscillator. This consists of a 7.304 MHz crystal (Z3) held at a constant temperature by an oven, which is one of the following:

- a PTC thermistor (E1) at 60°C
- a high stability oven [🗁 04-03095] where the R3 NTC resistor measures the temperature of the crystal and causes the op-amp comparator IC1 to vary the current in the heating element V2 to maintain the temperature of 65°C to within ±1°C

The temperature of the high stability oven is set by R4. V1, R12 and R13 limit the maximum current through V2 to approximately 400 mA.

VCO1 and phase lock loop (04–02972)

🗁 04-02972 Sheet 1
The oscillator VCO1 is designed around a differential amplifier consisting of FETs V8 and V9. The frequency of oscillation is determined by the tuned circuit L33, C94 and the capacitance of the varicaps D20 to D23. The oscillator output power is set by source resistors R55 and R58. The resistor R54 assists in maintaining a constant output level over the operating frequency range.

The oscillator output at the tap of the tuned inductor L33 is coupled via C101 to an emitter follower V10. The output drives the two mixers IC4 and IC5 and the prescaler IC9 (all pin 5).

The high frequency output from VCO1 is divided by a 64/65 prescaler IC9, down to a frequency range of 706 kHz to 1.17 MHz (pins 2 and 3). A high or low on pin 1 sets the division ratio.

IC10 is a complex chip that contains two programmable dividers and a phase comparator. The phase comparator compares two input signals of the same frequency and outputs a voltage that is dependent on their relative phase.

The input to comparator pin 4 is from the prescaler IC9. This is divided down to 2 kHz by one of the programmable dividers. The quartz crystal (Z3) connected between pins 7 and 8 forms the reference oscillator. It is set to a frequency of 7304 kHz. The second divider is programmed to always divide the reference frequency down to 2 kHz.

The two divided signals are applied to the phase comparator internal to IC10. When the two signals are "locked" in phase, the comparator output (pin 1) is at mid-rail (2.5 V). These two frequencies are locked together by the action of the loop, e.g. changing the first programmable divider will change the VCO frequency.

Two separate outputs are available from the phase comparator. The output of IC10 pin 2 (PDB line) is a course control that outputs a mark:space ratio proportional to the frequency difference between the divided signals. The output of IC10 pin 1 (PDA line) is the fine control. It gives an analogue output that takes over from the PDB output when the two signals are close to phase lock.

The transistors V11, V12, V13 and associated components form the loop filter. The input at the base of V13 is biased to 2.5 V by H1 (functioning as a zener diode). The output DC, which can swing between ground and the positive rail (26 V), is applied via L32 to the varicaps D20 to D23.

The components L32 and C95 provide an LPF to the control DC while presenting a high impedance to the oscillator circuit. The control DC level changes the capacity of the varicaps to set the VCO to the required frequency. As the control voltage rises so does the frequency of the VCO.

When a new channel is selected, the microprocessor changes the value of the programmable divider IC10, which is fed by the prescaler IC9. As the two signals driving the phase comparator are now no longer at the same frequency, the phase comparator outputs pulses to the loop filter. The output of the loop filter ramps in the direction necessary to re-establish lock.

VCO1 and phase lock loop (04-03135)

🗁 04-03135 Sheet 1

The oscillator VCO1 is designed around a differential amplifier consisting of FETs V8 and V9. The frequency of oscillation is determined by the tuned circuit L33, C94 and the capacitance of the varicaps D20 to D23. The oscillator output power is set by source resistors, R55 and R58. The resistor R54 assists in maintaining a constant output level over the operating frequency range.

The oscillator output at the tap of the tuned inductor L33 is coupled via C101 to an emitter follower V10. The output of V10 drives two mixers IC4 and IC5 via C76 and C78 and a second emitter follower V11. The output of V11 is applied via C104 and R66 to the input of synthesiser IC9 pin 4.

Synthesiser IC9 generates a DC control voltage via the phase/frequency detector and control amplifier. This is applied to the varicaps to lock VCO1 to the nominated frequency.

The 7304 kHz oscillator (part of IC9) is divided down to a 2 kHz reference frequency. The VCO signal applied to IC9 pin 4 is also divided to produce 2 kHz when at the nominated frequency. Both of these signals are applied to the phase/frequency detector in IC9.

The phase/frequency detector provides two outputs. Pin 15 provides a "go down" pulse. Pin 14 provides a "go up" pulse. When locked, these outputs are high (+5 V) except for a very narrow low pulse that occurs simultaneously on both outputs.

V13 and V16 provide a 3 mA discharging current pulse whilst IC9 pin 15 is low. V12, V18, and V17 provide a 3 mA charging current pulse whilst pin 14 is low.

These current pulses accumulate in the loop filter (C106, C107, C151 and R70). The resulting voltage is applied to the varicaps (D20 - D23) via a filter (R51 and C96). This filter removes any reference signals from the control voltage.

VCO2 and phase lock loop (04-02972)

🗁 04-02972 Sheet 1

The tuned circuit L40, C130/131, C132 and C133 sets the appropriate frequency of operation. The network (consisting of C128, Z4, D31 and L39) is equivalent to a voltage controlled, very high Q series tuned circuit. This network effectively grounds the gate of V14 at the series resonant frequency. This determines the final frequency of oscillation.

The oscillator drive output from capacitor divider C132 and C133 is applied to mixers IC7 and IC8 and the prescaler IC12 (all pin 5).

The phase locked loop (PLL) incorporates VCO2. It works in a similar manner to the phase locked loop that incorporates VCO1. The only exceptions are that the phase detector output (IC13 pin 17) is required to drive the loop amplifier IC14/A and that the phase comparator varies from 1.1 kHz to 2 kHz. This allows the phase comparator frequency to vary, enabling the loop to move in 10 Hz steps while still having a relatively high phase comparator frequency.

The 7304 kHz reference oscillator output from IC10 pin 8 is applied to the PLL IC13 pin 2.

The DC output of the loop filter IC14/A pin 1 is applied via L36 to the varicap D31. It controls the frequency of the VCO. Components L36, R80 and C127, form an LPF to control the DC, while presenting a high impedance to the oscillator circuit. Component IC14 is powered from the 18 V output of the charge pump power supply IC11 and associated components.

VCO2 and phase lock loop (04-03135)

🗁 04-03135 Sheet 1
VCO2 is a crystal controlled Colpitts oscillator. The tuned circuit L40, C130/131, C132 and C133 sets the appropriate frequency of operation. The network (consisting of C128, Z4, D31 and L39) is equivalent to a voltage controlled, very high Q series tuned circuit. This network effectively grounds the gate of V14 at the series resonant frequency. This determines the final frequency of oscillation.

The oscillator drive output, from capacitor divider C132 and C133 is applied to mixers IC7 and IC8. It is also applied via emitter follower V19 to the input of synthesiser IC10 pin 4.

Synthesiser IC10 is almost identical to VCO1 synthesiser IC9 except for the following:

- The programmed division ratio of both the VCO and the reference frequencies vary between 1.1 kHz to 2 kHz. A look up table contained on the Microprocessor and Audio PCB allows for 10 Hz steps over the frequency range.
- Different filter components are used (C142, R110 and C141) because of the narrower operating frequency range.
- The control voltage at the output of V23 and V24 are connected via source follower V25 to varicap D31 of VCO2.
- The reference frequency is obtained from IC9 pin 2 via a buffer amplifier V26 to IC10 pin 1.

455 kHz local oscillator for USB/LSB (04-02972)

In USB mode, the 7304 kHz reference oscillator is taken from the second PLL IC13 pin 3 [🗁 04-02972 Sheet 1]. It is then applied via a harmonic filter network (R268, C244, L205 and C245) [🗁 04-02972 Sheet 2] to the input of a "divide by two" divider IC208/A pin 3. The output (pin 6) is applied to a second "divide by two" divider IC208/B pin 11.

The enable line of dividers IC208/A and IC208/B pins 4 and 10 and the gate input of IC206/C pin 8 are all connected to the output port of IC209 pin 9. In USB mode, the microprocessor IC101 [🗁 04-02976] latches the output of IC209 pin 9 high, via the local I^2C bus to IC209. This enables the dividers and disables the 1814 kHz oscillator NOR gate IC206/C.

The 1826 kHz reference signal (7304 kHz divided by 4) of IC208/B pin 8 is fed via NOR gate IC206/B to two more cascade "divide by two" dividers IC207/A and B. This produces a balanced output signal of 456.5 kHz signal at pin 8.

From here it is applied via the attenuator network (R269, R270, R271 and R272) to the balanced local oscillator inputs of modulator IC202 and demodulator IC203 pins 8 and 10.

In LSB mode, the microprocessor IC101 latches the output of IC209 pin 9 low. This disables the dividers IC208/A and B and enables the 1814 kHz crystal oscillator IC206/C . The signal is then fed via the NOR gate IC206/B and the dividers IC207/A and B (used for USB) to the modulator and demodulator. This produces the required local oscillator frequency of 453.5 kHz.

455 kHz local oscillator for USB/LSB (04-03135)

In USB mode, the 7304 kHz reference oscillator is taken from the second synthesiser IC10 pin 3 [🗁 04-03135 Sheet 1]. It is then applied via a harmonic filter network (R268, C244, L205 and C245 [🗁 04-03135 Sheet 2]) to the input of the first "divide by two" divider IC208/A pin 3. The output (pin 6) is applied to the second "divide by two" divider IC208/B pin 11.

The enable line of dividers IC208/A and IC208/B pins 4 and 10 and the gate input of IC206/C pin 8 are all connected to the output port of IC209 pin 9. In USB mode, the microprocessor IC101 [🗁 04-02976] latches the output of IC209 pin 9 high, via the local I^2C bus. This enables the dividers and disables the 1814 kHz oscillator NOR gate IC206/C.

The 1826 kHz reference signal (7304 kHz divided by 4) of IC208/B pin 8 is fed via NOR gate IC206/B to two more cascade "divide by two" dividers IC207/A and B. This produces a balanced output signal of 456.5 kHz at pin 8.

From here it is applied via the attenuator network (R269, R270, R271 and R272) to the balanced local oscillator inputs of modulator IC202 and demodulator IC203 pins 8 and 10.

In LSB mode, the microprocessor IC101 latches the output of IC209 pin 9 low. This disables the dividers IC208/A and B and enables the 1814 kHz crystal oscillator IC206/C. The signal is then fed via the NOR gate IC206/B and the dividers IC207/A and B (used for USB) to the modulator and demodulator to produce the required local oscillator frequency of 453.5 kHz.

Clarifier

The operation of the clarifier control, when selected on the front panel of the control head, is read by microprocessor IC2 via IC1 [🗁 04-02974]. The information is then sent via the external I^2C bus [🗁 04-02976 Sheets 1 and 2]. For each clarifier step detected, the microprocessor IC101 [🗁 04-02976] reprograms synthesiser IC13 [🗁 04-02972 Sheet 1] or IC10 [🗁 04-03135 Sheet 1], shifting VCO2 in 10 Hz steps from the nominal frequency. The clarifier has a range of ±50 Hz for channels 2 MHz to 5 MHz and then increases with frequency at a rate of ±10 ppm above 5 MHz.

The operation of the clarifier is achieved by varying both VCO2 and the reference frequency dividers according to the "look-up" table in the transceiver's operating system. Thus the phase comparison frequency is not constant, but varies from 1.1 to 2.0 kHz.

An audible indication is given when the clarifier reaches its upper or lower limit. The clarifier automatically resets to the mid frequency when another channel is selected or the transceiver power is interrupted.

Microprocessor and peripherals—transceiver

Microprocessor

🗁 04-02976 Sheets 1 and 2
The microprocessor IC101 on the Microprocessor and Audio PCB is an 80C552, a member of the Intel 80C51 8–bit microprocessor family. The microprocessor has:

- 256 bytes of RAM
- no internal program memory
- two counter/timers
- eight 8–bit ADC inputs
- a watchdog timer
- I^2C Bus
- an internal clock oscillator

The microprocessor operates in a conventional 8–bit data, 16–bit address configuration. To minimise the pin count, the low-order address bits are multiplexed with the data on pins 50 to 57 to produce a common 8–bit bus. The chip IC102 is used to latch the low order address bits to facilitate access to the external non-multiplexed devices.

The Address Latch Enable (ALE) signal IC101 pin 48 indicates to the latch when the address is present on the bus. The high order address bits are provided directly from IC101 pins 39 to 46.

The external devices that are connected to the bus are:

- IC103—an EPROM containing control software and the 9390 Radphone channels; selected via the Program Store Enable ($\overline{PSEN}$) signal pin 47
- IC104—a RAM device supplementing the microprocessor's internal RAM; selected via the Read ($\overline{RD}$) or Write ($\overline{WR}$) signals from IC101 pins 30 and 31
- IC105—E^2PROM containing the programmed channels
- IC106—a triple-tone generator used to generate control tones (see page 4-23, *Tone generation*)

The microprocessor is reset if the supply voltage ("A" rail) falls below 9 V. The reset circuit consists of a voltage detector and power up reset circuit IC107B and associated components.

I²C buses

There are three I²C bus lines:

- **EXT I²C bus**—This provides two-way serial data communication between the microprocessor IC2 pins 22 and 23 in the control head [🗁 04-02974] and the microprocessor IC101 pins 22 and 23 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1]. The data line, SDL, conveys information and the transfer is synchronised by transitions on the clock line, SCL.

- **Local I²C bus**—(shared with the PA Serial Bus) allows the microprocessor IC101 pins 7 and 8 to communicate to:

  IC108 E²PROM—16 kbit memory device used to contain general function commands such as Selcall Ident, tone frequencies, etc.

  IC109 and IC114—two 16–bit output ports that have different addresses set by pin 1. Serial data is read by both ICs but only the one that matches the address portion of the data stream will latch the selected IC's 16–bit parallel output. The two ICs provide a total of 32 open drain outputs to various control circuits throughout the transceiver.

  IC209 and IC111—two 8–bit In/Out integrated circuits. IC111 [🗁 04-02976 Sheet 1] and IC209 [🗁 04-02972 and 04-03135 Sheet 2] convert their eight ports to serial data for application to the bus. They convert serial data from the bus to parallel at their ports. They have different addresses and are set by the address pins 1, 2 and 3.

  When a data transfer is required, the microprocessor IC101 outputs the address of the required IC on the data line, followed by a Read/Write command. Data is read from, or written to, the selected IC. When a change at the input ports occur, the IC with the change sends an interrupt to the microprocessor IC101 pin 27. The microprocessor interrogates each IC in turn until the changed data is read. The selected IC removes the interrupt and the microprocessor is then able to continue with other operations.

  IC2—8–bit output port located on the Rx/Exciter PCB[🗁 04-02972 Sheet 1]. This IC selects the appropriate HPF, and when required, the RF filter.

  IC110—The real time clock.

- **Synthesiser I²C bus**—(shared with the synthesiser bus)

  IC112—[🗁 04-02976] battery backup RAM stores the latest operator commands such as current selected channel, volume level, mute on/off, selcall information etc. It retains this information when the transceiver is switched off. When powered up again, the microprocessor reads the information stored in IC112 and resets the transceiver to the last settings before it was switched off.

  IC210—E²PROM is a 2 kbit memory device located on the Rx/Exciter PCB [🗁 04-02972 and 04-03135 Sheet 2] and is not used at present. It will be available for future applications.

Synthesiser bus

(Shared with synthesiser I^2C bus.)

The synthesiser bus allows the microprocessor IC101 pins 10 and 11, to communicate to two synthesisers IC10 and IC13, located on the Rx/Exciter PCB [🗁 04-02972 Sheet 1 or IC9 and IC10 🗁 04-03135 Sheet 1]. These set the frequencies of VCO1 and VCO2.

PA serial bus

(Shared with the local I^2C bus.)

The 8–bit output port IC1, which is located on the PA and Filter PCB [🗁 04-02973 and 04-03096], reads the serial data and only latches its 8–bit parallel outputs when a strobe signal is received on pin 7 from the microprocessor IC101 pin 9. The open collector output controls:

- PA LPFs
- PTT line (within the PA)
- high/low power select

RS232 bus

The RS232 provides serial data communication between the microprocessor IC101 pins 24 and 25 and external equipment using the RS232 format. The DATA OUT line is buffered by V103 and associated components. The DATA IN line is buffered by IC113/F.

Tone generation

The tone generator IC106 has three audio outputs at pins 10, 13 and 17 [🗁 04-02976 Sheet 1]. The various tones are generated within the IC by dividing the common clock input to pins 9, 15 and 18 by factors programmed into the data input (pins 19 and 20). The tone generator is enabled by a low from the microprocessor pin 29 applied to IC106 pin 21.

The three audio outputs pins 10, 13 and 17, are filtered by a resistor/capacitor network and provides the audible signals required for emergency call, selcall and warning beeps etc.

A/D inputs

The microprocessor IC101 [🗁 04-02976 Sheet 1] monitors the supply voltage and VSWR signals applied to the A/D input:

- The supply voltage ("A" rail) is applied via resistor divider R107 and R111 to IC101 pin 1. The microprocessor provides a low alarm tone when the supply drops below 10 V.
- The transmit forward power detector output from D1 (FWD–PWR line) on the PA assembly [🗁 04-02973 and 04-03096] is applied via a coupling cable to resistor divider R108 and R112. It is then applied to IC101 pin 68.

  The transmit reflected power detector output from D2 (REFL–PWR line) on the PA assembly is applied via a coupling cable to resistor divider R109 and R113. It is then applied to IC101 pin 67.

  The microprocessor IC101 compares the forward and reflected power when in the Tune mode. It also provides a visual indication on the LCD of the measured VSWR when the special Test mode is enabled.

Applications that will be available in the future are:

- AGC voltage derived from the Rx/Exciter PCB will be connected via a coupling cable to a resistor divider R110 and R114, then to IC101 pin 66
- temperature measuring circuit R72, R73 and R74, shown on the Rx/Exciter circuit [🗁 04-02972 Sheet 1], is to be fitted on the PCB

Antenna control

The connector J202 [🗁 04-02976 Sheet 2] provides an interface to automatic antenna tuning systems, antenna selectors or band select for external power amplifiers.

The antenna control has a 4–bit binary output (pins 1, 2, 9 and 10). Three of these bits (pins 1, 9 and 10) can be programmed to provide information on the selected channels or bands. Pin 2 is used for special functions, e.g. detection of an external LPF.

The channel number is obtained by decoding the binary code. When the binary code is decoded, binary one is channel 1 then it follows the channel numbers up to channel 8. It then starts a zero for channel 9, a one for channel 10 and so on.

In band selection, the binary numbers are decoded as follows:

Table 4 -15: Frequency band and number

Band Number	Frequency Band
1	Less than 2.0 MHz
2	2.0 MHz to 2.99 MHz
3	3.0 MHz to 4.99 MHz
4	5.0 MHz to 7.99 MHz
5	8.0 MHz to 12.99 MHz
6	13.0 MHz to 19.99 MHz
7	20 MHz and above

The TUNE IN/TUNE OUT line (pin 4) and TUNED IN line (pin 11) are two control lines required by some automatic antenna systems. The TUNE IN/TUNE OUT line, once activated, is held low by the automatic antenna control network. It maintains the Tune mode while the automatic antenna completes the tune process. The microprocessor IC101 checks the TUNED IN line for a high or low on completion of the tuning sequence. A high indicates to the microprocessor that the tune has been successful. A low indicates that the tune has failed. This information is displayed on the LCD. Audio beeps are also provided to the speaker.

The SCAN line (pin 5) goes low when in Scan mode and selects the scan amplifier in the automatic antenna.

When the **PTT** is initiated, pin 8 provides an active high and can be used by some tuners in their logic circuits.

To enable the tuners to be powered from the transceiver, a fused switched supply from the transceiver's battery power is provided by pins 12 and 13 (positive) and pins 14 and 15 (ground).

E^2PROM write protect

Output of the microprocessor IC101 pin 21 [🗁 04-02976 Sheet 1] is connected via inverter IC113/E and R156 to the base of switching transistor V106. Except during programming, IC101 pin 21 is high resulting in V106 conducting, which in turn sets IC105 pin 27 high (write protect).

Microprocessor and peripherals—control panel

Microprocessor

The microprocessor IC2 contained on the Display Panel PCB [🗁 04-02974] is identical to the microprocessor IC101 on the Microprocessor and Audio PCB. For details of operation see page 4-21, *Microprocessor*. To facilitate access to the external non-multiplexed devices, IC3 is used by latching the lower order address bits.

The following devices are connected to the bus:

- IC5—an EPROM containing an LCD display and control information. The microprocessor selects the EPROM via the Program Store Enable signal IC2 pin 47.
- IC6—a RAM device supplementing the microprocessor's internal RAM. It is selected via the Read or Write signals IC2 pins 30 and 31.

A voltage detector and reset circuit (IC10/A and associated components) resets the microprocessor if the supply voltage ("A" rail) falls below 9 V.

I^2C buses

There are two I^2C bus lines:

- **EXT I^2C bus**—this bus is used to communicate between the Display Panel PCB IC2 pins 22 and 23 and the transceiver's microprocessor IC101 [🗁 04-02976] (see page 4-22, *I2C buses*).
- **Local I^2C bus—**allows the microprocessor IC2 pins 20 and 21 to communicate to an 8–bit In/Out port IC1 and E^2PROM IC4. The In/Out port IC1 allows communications from the keypad. IC4 contains the contrast and back light settings for the control panel.

Keypad

The keypad consists of switches on a panel overlay (substrate) forming a 3×4 matrix. The rows and columns are connected to the Display Panel PCB [🗁 04-02974] via P1.

The columns are held low. One line is driven direct from IC2 pin 11. The remaining three lines are buffered by open collector transistors V1, V2 and V3, which are driven from pins 14, 13 and 12 respectively.

When a button is pressed, it applies a low to one of six input ports of IC1. This causes the interrupt line to go low, forcing the microprocessor to read the ports. The microprocessor identifies the row that is low and then polls each column in turn to identify the actual button that has been pressed. When the microprocessor has identified which button has been pressed, it performs the function for that button.

An additional diode D1, is connected to the cathode of D2 and forms part of the Power On circuit (see page 4-1, *Power on*).

Select control

The **Select** knob is a 360°, 16 position, binary encoder. It is continuously rotatable in either direction. It can be selected to carry out many functions such as changing the channel, clarifying the received signal, free tuning the transceiver etc. The microprocessor IC2 detects each step of the control, then increments either forward or back, in its selected function.

Volume control

The **Volume** knob is a rotary, digital encoder and its main purpose is to control the level of audio to the speaker amplifier (see page 4-10, *Volume control and audio output amplifier*). It also has other functions in the Setup and Program modes such as adjusting the LCD back lighting, moving the cursor etc.

Display

The Liquid Crystal Display (LCD) H1 consists of a 122 × 32 character dot matrix with LED back lighting. It has its own decoder and drive network. The data from the microprocessor IC2 is sent via the 8–bit data lines to the display.

The back lighting to the LCD is achieved by a bank of LEDs mounted at the back of the display. The normal intensity of the back lighting is set by the parallel resistors R16, R17 and R20 with transistors V6 and V13 switched on in series with the LEDs connected between the "B" rail and ground. When the back lighting is reduced by the **Volume** knob on the front panel, the microprocessor IC2 switches off transistors V6 and V13 in sequence to give a total of four levels of intensity.

The LCD viewing angle is adjustable by the **Select** knob on the front panel. The **Select** knob is controlled by the Pulse Width Modulation Output from the microprocessor IC2 pin 4 and via a DC filter R13/C13 to IC8/A pin 3. The DC average of the Pulse Width Modulation appearing across C13 determines the DC output of IC8/A pin 1. This sets the VEE level to the LCD for the required viewing angle. It has a control range between –3 and –4 V.

The temperature compensating components IC8/A, D8 and D9 ensure that the set viewing angle remains constant over the operating temperature range. To enable the output of IC8 to be negative with respect to reference ground, it is connected to the +5 V and the −7 V supplies.

A second temperature sensor R53 monitors the temperature and reduces the back light by switching off V13 at 60°C followed by V6 at 65°C. The back light returns to its normal setting for a period of two minutes when any control function is initiated.

Microphone keypad

The microphone assembly incorporates a microphone, a **PTT** button, a keypad and an encoder.

The keypad can be used to control most of the transceiver's functions. It consists of a panel overlay forming a 3×4 matrix. The three columns and four rows are connected to encoder IC1 [🗁04-02975]. When each button is pressed, it outputs serial data from IC1 pin 1. This is fed to the control head via J1 pin 4. From here, it is passed via a buffer/inverter IC7/A to the RXD input of the microprocessor IC2 pin 24. The microprocessor reads the data and performs the appropriate function for the particular button that was pressed.

The encoder IC1 receives its 5 V supply from the "A" rail via shunt zener diode V1 through series resistor R1.

The back lighting to the buttons is provided by four LEDs, which are connected via two 470 Ω current limiting resistors to the "A" rail.

Data input/output

The connector J3 on the front of the control panel provides input from the microphone assembly (see page 4-28, *Microphone keypad*). It also has a secondary function when connected to a computer with XP software. It provides an input/output data facility for channel programming and set up.

When set up in Program mode, data from the computer is applied to J3 pin 4. This is the same data input path used by the microphone and follows the same path to the RXD input of the microprocessor IC2 pin 4. The data from the microprocessor IC2 pin 25 (TxD line) is passed to the buffer/inverter V7. From here the data goes via P3 pin 3 to J3 pin 5 and then to the computer input.

"S"+ RF indicator

An approximate indication of the receive signal strength and transmit output power is displayed in the form of a bar graph on the LCD. These two signals are derived from the AGC in receive and the forward power detector in transmit.

The AGC voltage from the RX/Exciter PCB enters the Microprocessor and Audio PCB at P102 pin 5 [🗁 04-02976 Sheet 1]. This is connected via D101 and R101 to the load resistor R104.

The forward power detector is derived from the PA assembly and enters the Microprocessor and Audio PCB at P101 pin 10. It is then connected via R102, D102 and R103 to the load resistor R104.

The receive signal strength and the transmit output power signals do not appear at the same time. Therefore they can share the same path and are OR gated across R104 ("S" + RF). The signals are available from P201 pin 4 [🗁04-02976] via a coupling cable to the front panel P4 pin 4 [🗁04-02974] and to the Remote Control connector P204 pin 8 [🗁04-02976] for the control head. The signals are then passed through an RF filter (R43 and C37) to microprocessor IC2 pin 1.

The microprocessor IC2 measures the analogue level of the AGC in receive and the forward power detector in transmit [🗁04-02974]. The resulting digital information is passed to the LCD display H1. The microprocessor in the LCD assembly translates the information to produce the appropriate signal levels on the bar graph.

In receive, the analogue level of the AGC is measured by IC2. The minimum signal commences at 4.5 V and falls to 0.25 V for maximum signal strength. In transmit the measurement is reversed—it begins at 0 V for a zero output and rises to 4.25 V for maximum output power.

Mute indicators

The **S'Call Mute** and **Voice Mute** buttons incorporate LED indicators and are lit when one of the mute functions is selected. These are controlled by the microprocessor IC2 setting the appropriate output port of IC1 pin 11 or 12 high, via the I^2C bus. This causes either V4 or V5 to conduct and to light the respective LED.

Front panel back light

The front panel back lights help locate the buttons and control knobs for night-time operation. The panel consists of 16 LEDs divided into four groups. They are connected between the "A" rail and transistor switch V11 to ground. Each group of four LEDs has its own 390 Ω current limiting resistor. When the back lighting to the LCD is set to minimum, transistor V11 is switched off reducing the intensity of the front panel back light.

PA and filters

PTT and PA filter control

🗁 04-02973 and 04-03096
The drivers, output stages and part of the output bias circuit are permanently connected to the supply voltage when the Power On relay K8 is energised. They draw no current until transmit is selected. When the **PTT** is enabled, power is supplied via V5 to the remaining circuits of the PA.

The PA LPFs are controlled by the microprocessor IC101 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1]. Serial data on the local I^2C bus from the microprocessor IC101 is applied to IC1 pin 3 (serial data input 8–bit output driver) on the PA and Filter PCB.

Depending on the channel frequency, the microprocessor IC101 will select one of the six filters by grounding one of IC1**'**s outputs (pins 13–18).

When the **PTT** is selected, the microprocessor IC101 sends serial data to IC1 (on the PA and Filter PCB), which latches pin 12 to ground. This energises K7 (transmit/receive change over relay) and also forward-biases V5. As a result DC is provided to the input, pre-driver stages and the 5 V regulator IC2.

The 5 V regulator supplies bias for the ALC and input amplifier. It also enables the output transistor's bias circuit.

Gain control stage

The RF input from the exciter is terminated by R20 and drives the common base, long-tail pair V13 and V14. This is achieved through R41 and R44 being connected in parallel for signal currents. The resistor R43 sets the DC condition of the long-tail pair and is RF bypassed by C90.

The gain of the input amplifier is controlled by the difference of emitter DC currents in V13 and V14. The RF input is split between the emitters of V13 and V14 in inverse proportion to their input impedance. The gain of V14 is reduced when the ALC increases the current in V13. The collector load of V14 consists of components L19 and R45. These components are frequency compensating components and reduce the low frequency gain.

Pre-driver stages

The collector output of V14 is coupled via C94 to the emitter follower V15. The output of V15 drives the pre driver stage V16. The components R51, L20 and C97 (in the emitter circuit) provide high frequency peaking. The output of V16 is coupled to the driver stage via transformer T2.

Driver stage

The push–pull, class B, driver stage V21 and V22 is voltage driven from the secondary of T2. The transformer T3 provides the current drive to the output stage.

The bias for the driver stage is applied to the centre tap of T2. This is provided by the total current of the emitter follower and pre-driver stages (V15 and V16) via transistor V17, which is connected as a diode. The bias is set by the SOT resistor R54 and changes the voltage drop across the collector-emitter of V17.

Output stage and bias regulator

The push–pull, class B, output stage V23 and V24 is driven from the centre tapped secondary winding of transformer T3. The centre tap provides the bias feed from the bias regulator.

The bias regulator V19 and V20 provides a constant voltage to the bases of V23 and V24. The transistors V19 and V20 form a feedback voltage regulator. The output voltage is the base-emitter voltage of V19 and is adjustable by the preset potentiometer R59. The transistor V19 is mounted on the PA heatsink and provides temperature compensation to the bias network.

When low power is selected, the microprocessor (via the serial bus) latches IC1 pin 11 low. This energises the transistor V25 and changes the current through V19. The result is an increase in standing current to the output transistors V23 and V24. This increase in bias improves the intermodulation distortion at low power.

The zener diode V18 and resistor R61 increase the bias for a low DC supply voltage (< 11 V). This, in conjunction with the power output reduction circuit in the ALC (see page 4-32, *ALC control*), reduces the intermodulation distortion when operating from a low DC supply.

The balanced/unbalanced impedance matching output transformer T4 couples the power amplifier output to the band filters via the transmit/receive relay K7.

Output filters

The transmit frequency range is dependent on the PA assembly fitted and uses six LPFs, which are selected by relays K1 to K6. These are operated from IC1 and are selected to remove the harmonics generated by the PA.

The output of the filter circuit passes through the ALC RF bridge to the antenna output J1.

PA assembly 2.25 to 30 MHz has an optional external filter to increase the lower range to 1.6 MHz. The filter is attached to the rear of the heatsink and is relay selected by a low on IC114 pin 18 [🗁04-02976] via the antenna control connector J202/2.

ALC control

The Automatic Level Control is provided from:

- forward power
- reflected power
- output stage collector swing
- battery voltage
- heatsink over temperature
- transmit/receive and filter relay failure

All the ALC control inputs, except for relay failure detection (detailed later), are applied to V8 to V11. The ORed output is connected via R30 to the positive input pin of the ALC level comparator IC3/B pin 5. The reference voltage to pin 6 is software controlled by the microprocessor IC101.

The PA-PWM line from the microprocessor IC101 pin 5 [🗁 04-02976 Sheet 1] outputs a programmed mark:space ratio. This is applied via a filter network (R106, C104, R105 and C103) to the buffer amplifier IC107/A pin 3.

The DC level at the output represents the average mark:space ratio set by the microprocessor. This is applied via R36 to the reference input of IC3/B pin 6 on the PA and Filter PCB [🗁 04-02973 and 04-03096]. The control voltage ranges between 2 to 5 V. This is limited by the resistor divider network R32, R33 and R34 (NTC) to between 3.0 to 3.8 V at the reference input of IC3/B pin 6. This allows the microprocessor to reduce the PA output at the higher operating frequencies and ensures that the intermodulation distortion remains within the specified limits.

In the absence of any ALC inputs, the output of IC3/B holds the base of V13 to the reference voltage on pin 6 (3.0 to 3.8 V). With the base of V14 referenced to 5 V, V13 will be cut off, setting V14 to maximum gain. If an ALC control signal causes any of the transistors V8 to V11 to conduct, it will result in the rise of the output of IC3/B. This reduces the gain of V14 and thereby controls the gain of the PA.

The output voltage of the RF bridge (T1, L3 and R2) and capacitor divider (C6, C3, C4 and C5) is rectified by D1 for the forward power and by D2 for the reflected power.

The output of the forward rectifier D1 is applied via R22 to the input of V8. The resistor R22 and the sum of the resistors between the base of V8 and ground, form a resistor divider network. This determines the nominal PEP output level when matched to a 50 Ω load.

For high power, the sum of the lower section of the divider chain consists of R21, the parallel value of R15 and R16 (SOT), and R19. The resistors R17 (SOT) and R18 are shorted out by the FET switch V7 (+5 V on gate) and do not contribute to the chain. The nominal high power output, which is measured at low frequency, is set by R16 (SOT).

For low power, the sum of the lower section of the divider chain uses the same components as used for high power, as well as V7 off (i.e. gate at 0 V), resistors R17 (SOT) and R18. The resistor R17 is selected for low power when the power is <12 W PEP.

The output of the forward detector D1 is also applied to V9 via an averaging detector circuit consisting of R23 and C83. When the average of the signal exceeds the peak detector circuit (this occurs when in Tune mode, CW (morse) and in some data transmissions), V9 takes control and reduces the output power.

The output of the reflected rectifier D2 is applied via resistor divider R26 and R25 to the input of V10. The rectifier D2 takes control of the ALC when the reflected power exceeds 10 W (> 2:1 VSWR).

The peak output collector swing is monitored by R70 and D10 for V24, and R73 and D11 for V23. The diode cathodes are ORed and applied via resistor divider R71 and R72 to V11. The transistor V11 will conduct and limit the collector peak to 42 V to prevent damage to the output transistors.

The battery voltage is monitored by V6. When the supply voltage ("A" rail) drops to about 12 V, the voltage at the base of V6 (set by the resistor divider R11 and R12) will fall to 4.3 V and cause V6 to conduct. This will start to raise the voltage across R19 (part of the forward detector resistor chain) and change the threshold of the forward ALC detector. The ALC detector will start to reduce the output power and, as the control is linear, a further reduction in supply voltage will continue to lower the output power.

If the heatsink exceeds 80°C, PTC resistor R34 rapidly increases in value, reducing the reference ALC threshold level to the comparator IC3/B. This lowers the output power and prevents the heatsink from exceeding 90°C.

The protection circuit consists of IC3/A and associated components. It simultaneously monitors the output transistors, collector swing (applied to IC3/A pin 3) and the forward detector output of D1 (applied via R27 to IC3/A pin 2). In the event of a relay failure, which results in no signal at the antenna output, the output of IC3/A (coupled via D9 into the ALC control circuit) will go high. This will reduce the drive to the output transistors to a safe level by lowering the gain of the input amplifier V14.

Selective calling

All the selective calls are sent as Frequency Shift Keying (FSK) signals and normally use 1700 Hz and 1870 Hz at a rate of 100 baud.

Calibration

The phase lock loop Selcall FSK Decoder IC302 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 3] has a Voltage Controlled Oscillator (VCO) whose frequency is set by C310, R315 and the DC volts across R317.

The Pulse Width Modulation Output (S-PWM line) from the microprocessor IC101 pin 4 [🗁 04-02976 Sheet 1], is filtered by R155 and C314 (see Sheet 3) to produce a DC voltage across R317. The level of the voltage is set by the mark:space ratio of the Pulse Width Modulation Output from the microprocessor and will determine the final frequency of the VCO.

For the Selcall FSK Decoder IC302 to perform correctly, it is necessary for the two selcall frequencies to be centred on the VCO frequency (e.g. for 1700 Hz and 1870 Hz the centre frequency = 1785 Hz). This is automatically checked and calibrated every time the power is applied to the transceiver.

The procedure for FSK is:

- At switch on, the microprocessor IC101 [🗁 04-02976 Sheet 1] programs a test tone from the tone generator IC106 pin 17 at the centre frequency of the two selcall working frequencies. The microprocessor also provides a Pulse Width Modulation Output (S-PWM line on pin 4) to produce a predetermined DC voltage across R317 [🗁 04-02976 Sheet 3]. This sets the VCO to within the operating frequency band.
- The test tone is applied via R135A, C120 and R136 to the input of the dual active BPF network IC301A/B and associated components [🗁 04-02976 Sheet 3]. The filter has a 3 dB bandwidth of 400 Hz centred on 1785 Hz. The filtered output (pin 7) is applied to the FSK Decoder IC302 pin 2.
- The loop phase detector output (pin 11) produces an AC output with a DC offset. This is applied to an active data filter IC303/A to remove the AC component. The remaining DC voltage at the output (pin 1 FSK"V" line) is connected via divider R120 and R122 to an A/D input of the microprocessor IC101 pin 62. There is also a reference voltage derived from IC302 pin 10 (REF"V" line). This is connected via resistor divider R119 and R121 to a second A/D input of the microprocessor IC101 pin 63.
- The microprocessor IC101 compares the two DC levels FSK"V" and REF"V". IC101 adjusts the mark:space ratio of the Pulse Width Modulation Output (S-PWM line) until the difference voltage equals zero. This sets the VCO to half way between the two operating FSK tones. For fast calibration on power up, the microprocessor retains this setting in the E^2PROM IC108.

Selective calling

The selective calling facility is fitted as standard in the transceiver (it is optional for the 9390). To use it, it must be enabled.

A call is initiated by pressing the **Call** button on the microphone, or **F1** on the front control panel. On recognising the request for a call, the microprocessor IC101 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 1] checks that the channel selected has selcall enabled. If it is enabled, the microprocessor generates the required data for the selective call from the Call Address and Self Ident code configured in the transceiver.

The microprocessor IC101 [🗁 04-02976 Sheet 1] sets the dividers in the tone generator IC106 to produce the correct FSK tones before applying the generated data. The resulting FSK tones from IC106 pin 17 are filtered by R135/A, C120, R136 and C117. This is applied via R213 and C215 to the input of the combining amplifier IC204/A (see Sheet 2). The transistor V204 is switched off. This removes the short circuit during transmission and enables the FSK tones to be applied to the combining amplifier IC204/A. The FSK tones are also attenuated by R131 and R132 (see Sheet 1) and are applied as side tone to the input of the speaker audio amplifier IC306 (beeps input). At the same time, the microprocessor IC101 generates a PTT command so that the FSK tones are transmitted. On completion of the coded transmission, the PTT signal is removed and the transceiver returns to the Receive mode.

In Receive mode, the FSK audio appears at the output of the audio preamplifier IC204/A on the Rx/Exciter PCB [🗁 04-02972 and 04-03135 Sheet 2]. The audio is passed by ribbon cable from P201 pin 9 to P102 pin 9 on the Microprocessor and Audio PCB [🗁 04-02976 Sheet 2]. It is then applied via C206, C302 and R302 to the input of the dual BPF IC301/A and IC301/B (see Sheet 3). The audio from the filter output (pin 7) is fed to the input of the FSK decoder IC302 pin 2.

The voltage controlled oscillator (part of IC302) is automatically calibrated on power up (see page 4-34, *Calibration*). In the absence of FSK signals, the lock detect output from pin 6 will fluctuate and the resulting charge on C312 will be less than half the supply voltage. The voltage is applied via R312 to the comparator input (pin 8) resulting in a low output from pin 7. Some of the output is fed back via R313 to the input to provide hysteresis. The comparator output is taken via D303 to the non-inverting input of IC303/B. This results in a low output from IC303/B, which effectively cuts off V302. When the FSK signals are detected, the lock detect output goes high. The resulting high comparator output reverse biases D303, thus enabling IC303/B.

When FSK signals are received, data appears on the phase detector output (pin 11). This is applied to the data filter IC303/A and associated components. This is an LPF at approximately 80 Hz, which passes the resulting data to the input of IC303/B. The data filter output is also peak rectified by D301, D302, C320 and C321. The voltages on the two capacitors are summed at the inverting input of IC303/B to give a reference voltage equal to the main frequency of the FSK signal. The result is that IC303/B regenerates the data and ignores any frequency shift in the RF path.

The demodulated FSK signals are applied via V302 to the microprocessor IC101 pin 26 (see Sheet 1). The microprocessor decodes the addresses contained in the data. If the selective call is found to be addressed to the transceiver, the microprocessor sends a revertive message to the caller. The microprocessor simultaneously produces outputs to activate the necessary audio and visual indications that a selective call has been received.

If the transceiver **PTT** is not pressed on completion of the audio alarm period, the microprocessor IC101 sends a command for IC109 to open-circuit the output (pin 6 open collector). This allows the line connected to pin 6 to forward bias V301 via pull up resistor R328. The transistor V301 energises relay K301 for two minutes, operating an external alarm (if fitted). The relay K301 contacts are rated at 50 V at 1 A. The operation of **PTT** cancels the alarm.

Emergency call (RFDS) and two-tone calling

The two-tone calling system consists of the transmission of two simultaneous audio tones. The frequency difference of the two tones provides a narrow bandwidth independent of frequency shifts in the RF transmission path.

The Australian Royal Flying Doctor Service (RFDS) uses the two-tone audio transmission to alert the RFDS stations of an emergency call. The activation of the station's emergency detection system requires the transmission of two audio frequencies of 1320 Hz and 880 Hz for a minimum period of 10 seconds. This facility (designated E) must be enabled on the selected channel before it can be used.

The emergency call function is activated by pressing the **Emgcy Call** button on the front panel. The microprocessor IC2 in the control head recognises the request. It then sends the command via the I^2C bus to the microprocessor IC101 to initiate the emergency call [🗁 04-02976 Sheet 1]. If the selected channel has been enabled for the emergency call, the microprocessor IC101 programs the tone generator IC106 to output 880 Hz from pin 13 and 1320 Hz from pin 17. This generates the PTT command.

The two tones are filtered by a resistor/capacitor network and mixed across the final filter capacitor C117. They are then sent via R213 and C215 to the input of the combining amplifier IC204/A (see Sheet 2). As in the Selcall mode, the shunt transistor V204 is switched off for the period of the transmission.

The mixed tones are also attenuated by R131 and R132 and applied as side tone to the input of the speaker amplifier IC306 (see Sheet 3).

When the **Emgcy Call** button is pressed for a minimum of two seconds, an emergency call will be transmitted for a duration of 45 seconds. The transmission may be cancelled anytime by:

- pressing **Tune**
- pressing **PTT** on the microphone
- switching off the transceiver

There are also four programmable, two-tone frequency combinations available (T1 to T4). When enabled on the selected channel, they can be activated by pressing the **Call** button on the microphone or control head. Unlike the emergency call, the transmission ceases and the transceiver returns to Receive mode when the button is released.

Emergency alarm (marine)

The marine emergency alarm in the 9390 consists of two alternatively produced tones of 1300 Hz and 2200 Hz.

The tone generation is the same as the emergency tone (see page 4-36, *Emergency call (RFDS) and two-tone calling*) except that only one tone is generated at a time.

The alarm is activated by pressing the **Emgcy call** button for two seconds. It transmits the alarm for 45 seconds. The alarm can be cancelled at any time by pressing **Emgcy Call** again or by operating **PTT** on the microphone.

The alarm process is started when the **Test** button is pressed for two seconds. It continues for 45 seconds but does not transmit the tones. The test alarm can be cancelled at any time by pressing **Test** again or by operating **PTT** on the microphone.

The marine emergency alarm is available on all channels and does not have to be enabled as with emergency calls (RFDS) and tone calls.

PA Exciter Interface

🗁08-05226 and 04-03092
The 9323, 9360, 9390 or 9780 series transceivers may be fitted with a PA Exciter Interface assembly replacing the 100/125 W PA assembly.

Transceivers fitted with the PA/Exciter Interface assembly are identified by a letter H suffixed to their type number, which is located on the rear of the panel. This assembly is designed for use with Codan Power Amplifier type 4404.

The microprocessor detects when the PA/Exciter Interface assembly is fitted and provides the necessary control commands to operate the PA/Exciter Interface PCB.

Filter and PTT control

[🗁 04-03092]
The band filters, **PTT** and high/medium/low power on the Power Amplifier type 4404 are selected by the microprocessor in the transceiver.

Serial data from the microprocessor IC101 [🗁 04-02976] is applied via the local I^2C bus to IC2 (serial data input 8-bit output driver) on the PA/Exciter Interface PCB (P1/14, 15 and 16). The outputs of IC2 pins 11, 12, and 13 provide the BCD switching lines to select the filters. Pins 14 and 15 select the high, medium and low transmit power levels to the Power Amplifier type 4404.

When **PTT** is selected, the microprocessor IC101 [🗁 04-02976] sends serial data to IC2, which latches pin 16 to ground. This grounds the PTT line to the 4404 and at the same time forward biases V1, providing the DC supply to the transmit amplifier V3, V4 and V5.

Power On/Off

In the power off state, contacts K1/C and D are in the open position. The 24 V DC supply connected to the Power Amplifier type 4404 is fed via the two series connected power relays K8 and 9, and D10 on the Filter PCB [🗁 04-01817 (HF 4000 series)], through the connecting cable to P2/6 on the PA/Exciter Interface PCB [🗁 04-03092] . From here it passes through RF filter network L5 and C6 to charge C1 to about 13 V. The remaining volts are dropped across V7 and D6.

At the moment of switch on, the POWER ON line (P1/3) from the transceiver goes low applying the charged voltage across C1. This energises the ON coil of the latching relay K1. This results in the contacts of the latching relay K1/C and D closing and grounding the POWER ON line to the Power Amplifier type 4404. With this line low, relays K8 and 9 energise, applying 24 V to all circuits in the Power Amplifier type 4404.

When the power is switched on, a 13.6 V regulated supply IC2 on the Power Amplifier [🗁 04-01817 (HF 4000 series)] is connected via the interconnecting cable to P2/1 and 2 on the PA/Exciter Interface PCB. From here it is fed through L4, F1, L1 and P1/5, 6, 7 and 8 to the Microprocessor and Audio PCB. At the same time it provides 13.6 V to IC2 and switching transistor V1 on the PA/Exciter PCB. V1 provides the supply to power the transmit amplifier during transmit only.

At the moment of switch off the POWER ON line P1/3 goes high (12 V approximately) and forward biases transistor V8. This energises the OFF coil of the latching relay K1, causing contacts K1/C and D to open and remove the ground on the POWER ON line to the Power Amplifier type 4404 (P2/6). This de-energises relays K8 and 9, switching off the 24 V and 13.6 V regulated to the transceiver.

Transmit Amplifier

The RF input to the PA/Exciter Interface PCB is applied to J2. From here it is fed via a common mode transformer T2 through R17/C15 and R18 to a common base amplifier V3. R19 preset provides a range of approximately 8 dB of gain control. The signal at the collector of V3 is passed to an emitter follower V4, the output of which drives V5.

In combination with T3, V5 forms a fixed gain feedback amplifier. The secondary of T3 is adjusted for 2.0 V PP output by R19. This occurs when the exciter is modulated with a single tone into compression while connected to the 4404 PA assembly.

The output of T3 must be terminated into 50 Ω if it is not connected to the Power Amplifier type 4404 when adjusting R19.

Receiver Path

The received signal from the PA assembly is applied via the connecting cable to Rx I/P between P2/10 and 9 (AC ground). It is fed via C14, input protection diodes D1 to D4 and common mode transformer T1 to J1. From here it is coupled by a coaxial cable to the receiver input on the Rx/Exciter PCB [🗁 04-02972 and 04-03135].

Antenna Control

The Antenna control cable connected between P202 on the Microprocessor and Audio PCB [🗁 04-02976] and J201 mounted on the rear panel is also connected via P3/6, 7 and 9 to the PA/Exciter Interface PCB [🗁 04-03092]. This enables the SCAN, TUNE and TUNED IN control lines to be connected to the PA assembly 4404 via the connecting cable between the two units.

PA assembly 4404

Details on the Codan PA assembly 4404 are available in a separate Technical Service Manual, Codan part number 15-02037.

Options

Option AM

Option AM allows AM (H3E) users to select and transmit on AM for any channel.

When AM is selected, IC114 pin 9 [🗁 04-02976 Sheet 1] goes high and controls two circuits. It switches on V201 [🗁 04-02976 Sheet 2] and halves the audio output from the microphone amplifier IC204 pin 7. It reinserts the carrier signal by switching on IC206/A and V203 [🗁 04-02972 and 04-03135 Sheet 2]. R284 sets the level of the reinserted carrier.

The 9390 has AM transmission as standard on the 2182 distress channel.

Option CW

Option CW is used in the 9360 range of transceivers that have the 500 Hz CW filter fitted. When this option is fitted, the standard SSB filter (Z202) [🗁 04-03135] is removed and an extra PCB [🗁08-05259] with two filters is added.

The 1814 kHz crystal Z201 is also removed and replaced with a PCB [🗁08-05260] with three switchable crystal oscillators.

In normal USB/LSB operation, the signal is filtered by Z1, which is 2.5 kHz wide. When **UCW** or **LCW** is selected, the 500 Hz filter Z2 is switched in series with Z1 by relay K1. K1 is controlled by the software via IC209 pin 7 [🗁04-03135].

The local oscillator switch activates one of three oscillators depending on the mode selected.

Mode	**Oscillator**
LSB	Z1 is on
UCW	Z2 is on
LCW	Z3 is on

This signal is divided by 2 in IC3/A, then connected to the input of IC206/C [🗁04-03135].

Option F

Option F consists of an axial fan mounted in a shroud and clamped to the PA heatsink. The operation of the fan provides additional heat dissipation to the PA when transmitting continuous data.

After two minutes of transmission, with less than 20 seconds break in between, the microprocessor IC101 [🗁 04-02976 Sheet 1] open-circuits the output of IC114 pin 15. This causes switch V105 to conduct via the pull up resistor R153.

The power is then applied to the fan, which is connected between the parallel pins 1–2/3–4.

When transmitting for up to 5 minutes and on release of the **PTT**, the fan continues to operate for a further 30 seconds. However, if the transmission exceeds 5 minutes, the fan will continue to run for a further 5 minutes, after returning to Receive mode.

Option GP

Option GP is available to operate equipment such as teletype, modems etc. The connector J303 provides the following facilities:

Table 4 -16: Connector J303 functions

Pin No.	Function	Remarks
1	0 V	
2	Receive audio output	
3	Transmit audio input	
4	Quiet line input	Selects selcall mute
5	Alarm input	Active low for warning beeps
6	PTT	Selects transmit—no time out
7	Scan	High when scan selected
8	Battery supply	Nominal 13.6 V
9	RS232 Rx	Data to TCVR
10	RS232 Tx	Data from TCVR

Option M

Option M is available for the transmission of morse code. There is an external morse key connected to J204 [🗁 04-02976 Sheet 2]. When keyed, it transmits an 800 Hz tone from IC106 pin 13 on the selected channel.

Option PH

Option PH provides the connection for a headset. A 6.4 mm switched jack socket can be fitted to the transceiver front panel and connected to the loudspeaker circuit [🗁 04-02971]. Insertion of the jack in the socket mutes the loudspeaker by breaking the loudspeaker circuit.

The headset signal is slightly attenuated by two 330 Ω resistors in the line. This makes volume adjustment unnecessary when changing to or from headset operation. This option is only applicable to front control transceivers.

Option STE (9390 only)

Option STE allows 9390 users to send selective calls to a single transceiver or a group of transceivers. If this option is fitted, see page 4-34, *Selective calling*.

Accessories

RS232/I²C Interface

🗁 04-03068

General description

The RS232/I²C Interface unit is used to provide an additional two serial ports for transceivers 9323, 9360 and 9390 or remote control console 8570. The unit would normally be located at the transceiver end of the "Option R" cable. It can be located next to an extended control head but requires a special cable between the Interface unit and the control head.

Serial Port 1 must be used as a computer interface and Serial Port 2 must be used for a GPS receiver. The maximum of two RS232/I²C Interface units may be connected to the transceiver or remote control console.

Set up

Before using the RS232/I²C Interface unit, it is necessary to configure each port for the GPS and Computer. This is achieved by setting the dip switches located within the box, as applicable.

To gain access to the dip switches located on the PCB it is necessary to remove the single screw securing the back cover (identified by the silk screened title RS232/I²C Interface) and remove the cover.

Each RS232 port may be configured with a number of baud rates using dip switches as shown in the tables below.

Table 4 -17: Baud rate (GPS)

S1-dip 5 switch	S1-dip 4 switch	Setting
on	on	9600 baud no parity 1 stop
on	off	4800 baud no parity 1 stop
off	on	2400 baud no parity 1 stop
off	off	1200 baud no parity 1 stop

Table 4 -18: Baud rate (Computer)

S1-dip 7 switch	S1-dip 6 switch	Setting
on	on	9600 baud no parity 1 stop
on	off	4800 baud no parity 1 stop
off	on	2400 baud no parity 1 stop
off	off	1200 baud no parity 1 stop

Table 4 -19: Enabling ports

S1 dip 1 switch	GPS	S1 dip 2 switch	Computer
off	enabled	off	enabled
on	disabled	on	disabled

Disabling unused ports will reduce data processing time.

RS232/I²C Interface address

If you have two RS232/I²C Interface units connected to one transceiver or control console, then each unit must be set to a different address. To do this you set S1 dip 3 switch as detailed in the table below.

Table 4 -20: RS232/I²C Interface addresses

RS232/I²C	S1 dip 3 switch
First unit	off
second unit	on

Either RS232/ I²C Interface can be identified as the first unit.

Technical description

🗁 04-03086
The RS232/ I²C Serial Interface unit is used to interface transceivers 9323, 9360 and 9390 or the remote control console 8570 via the I²C bus of the "Option R" connector. The 87C654 microprocessor controls the I²C bus protocols and data exchanges to the transceiver or control console. The I²C line levels are driven by IC5. LC filters on the I²C minimise microprocessor noise into the transceiver.

Each serial port is driven by the same microprocessor with RS232 line level conversion using a MAX231 driver IC4. Signal levels on the microprocessor side of IC4 are TTL compatible, while signals on the line side are at true RS232 levels.

5 Maintenance

This chapter provides maintenance and fault finding procedures that can be carried out on the 9323, 9360, 9390 or 9780 transceiver. It covers general warnings and cautions to be observed when working with electronic equipment.

This chapter also outlines fault finding steps when receive and transmit failures occur and provides removal and installation procedures.

General

CMOS devices

A number of Complementary Metal Oxide Semiconductor (CMOS) devices are used in the transceiver and most of them have built-in protection. However, their extremely high open-circuit impedance makes them susceptible to damage from static charges. Care must therefore be used when shipping and handling the devices and servicing the equipment in which they are installed.

Packaging

Replacement CMOS devices are supplied in special conductive packaging. They should remain in this packaging until required for use.

Switching off

Ensure that power supplies are switched off before making connections or disconnections between circuit boards.

Handling

Handle circuit boards and touch conductive parts as little as possible.

Grounding

Anything connected to or touching the circuit board tracks should be grounded as follows:

- Ground test equipment connected to a board through its mains lead.
- Discharge static charges, which may build up on a person, by touching a grounded metal surface with both hands. This should be done before working on, and at frequent intervals while working on circuit boards.
- Wear a suitably grounded conductive wrist strap. This will minimise the build up of static on you.

Circuit boards

Excessive heat

Excessive heat may lift the track from the circuit boards. This will cause serious damage. Avoid the use of high-powered soldering irons. A soldering iron rated at a maximum of 60 W, preferably temperature controlled at approximately 370°C, is sufficient for most tasks. A soldering iron, rated at a slightly higher temperature of 425°C, may be required for heavier components such as PA transistors. Only apply the soldering iron long enough to unsolder an existing joint or to solder a new one.

Unsoldering

When unsoldering, use a solder-sucker or Solder wick to remove solder.

Do not use sharp metal tools such as screwdrivers or twist drills as these may damage the printed circuit track and plated through-holes.

Component substitution

Avoid unnecessary component substitution as this may damage the component, the circuit track or adjacent components.

Component replacement

When a component is diagnosed as defective, or the fault cannot be diagnosed in any other way than by substitution, observe the following when replacing components:

- Axial leads—Components with axial leads, such as resistors and capacitors, can often be replaced without unsoldering the joints on the boards. The defective component can be removed by clipping its leads close to the component, leaving the leads soldered to the board. These leads should be straightened, so that the leads of the replacement component can be wrapped around and soldered to them. After soldering, the excess lead should be clipped off.
- Remove solder—When a component has been unsoldered from the board, ensure the holes are clear of solder before inserting the leads of the replacement.

Never force the leads through the holes as this will damage the circuit track, particularly where plated through–holes are used.

- Observe orientation—Before replacing defective diodes, transistors, electrolytic capacitors or integrated circuits, observe any markings that indicate polarity or orientation. It is essential that these types of components are installed correctly. If necessary, consult the manufacturer's data for indications of the polarity of diodes, capacitors and transistors.

- Heatsinking—When soldering heat sensitive components to the circuit board, where possible use long-nosed pliers or some other form of heatsinking on the leads of the components.
- Thermal conduction—When replacing transistors that are mounted on heatsinks, ensure there is thermal conduction between the heatsink and the component being replaced. This can be achieved by cleaning the mounting surfaces then re-coating them with a thermal conduction compound such as Jermyn Thermaflow A30.

Track repair

Broken or burnt sections of printed circuit track may be repaired by bridging the damaged section with tinned copper wire. The section where the repair is to be made must be cleaned before soldering (observe the precautions detailed on page 5-2, *Unsoldering*).

Integrated circuit replacement

It is often possible to unsolder and remove components from the board without damage to the component or the tracks on the board. However, integrated circuits with many connections, mounted on double-sided circuit boards with plated-through holes, are almost impossible to remove intact and the operation is likely to damage the circuit boards. To replace these components, their leads must be cut individually until the body of the component can be removed. Individual leads must be unsoldered and removed. The excess solder must be removed before inserting the replacement component (see page 5-2, *Component replacement*).

Transmitter precautions

When making measurements of the low level stages of the exciter, it is advisable to remove the drive to the PA and Filter PCB. The supply voltage is applied to the PA at all times when the transceiver is switched on. Caution should be exercised when connecting probes.

Probe precautions

Observe the following when connecting CRO probes to the transceiver:

- When connecting probes to the PA assembly, the earth clip lead should be wound around the body of the probe so that the earth clip just reaches the probe tip. This reduces stray RF pick-up.
- The earth clip should be connected to the ground plane, adjacent to the point of measurement.
- It is not advisable to connect two probes at the same time, particularly when one is earthed to the PA ground plane and the other is earthed to the Exciter. This may cause earth loop problems.
- Probes should be connected after power has been applied to the transceiver and the test equipment. The earth connection should be made first and disconnected last.

Surface mounted components

In the control head, surface mounted components are used extensively on the printed circuit board. There are also a few fitted on other PCBs in the transceiver.

The removal or replacement of these components should only be attempted by a skilled technician experienced in handling surface mounted components.

Dismantling and assembling

Sometimes it is necessary to remove printed circuit boards from the transceiver in order to carry out repairs. The paragraphs that follow provide the technician with instructions on the removal and assembly of the circuit boards. While carrying out these instructions observe the following:

- Screwdriver—Screws with pozidrive heads are used in almost all locations. Use the appropriate and correct size screwdriver.
- Connectors—The ribbon cable header and multi-way connectors that are used can be incorrectly mated with their corresponding connectors. Care must be taken when re–installing the connectors to ensure they are correctly mated.
- To remove the screws securing the driver transistors (V21 and V22) and bias transistor (V17) on the PA assembly, use a 1/16 inch Allen key.

Top and bottom covers

To gain access to the printed circuit boards, the top and bottom covers must be removed from the transceiver. The process is the same for the removal of both covers.

Removing the covers

- ❑ Unscrew the two retaining screws, one on either side of the cover.
- ❑ Unscrew the two screws that secure the relevant cover to the front surround.
- ❑ Face the front of the transceiver towards you.
- ❑ Lift the rear of the cover up and slide the cover back, withdrawing it from the front panel.

Replacing the covers

- ❑ Face the front of the transceiver towards you.
- ❑ Slide the cover into the front surround and lower the back of the cover on to the frame.
- ❑ Replace the two screws that secure the cover to the front surround and the two retaining screws.

Rx/Exciter PCB

Removing the Rx/Exciter PCB

- ❑ Disconnect the ribbon cable connector P201.
- ❑ Disconnect the Tx/Rx coaxial connectors J1 and J2.
- ❑ Remove the seven retaining screws and take out the PCB.

Re-installing the Rx/Exciter PCB

- ❑ Locate the PCB in its correct position and orientation.
- ❑ Replace the seven retaining screws.
- ❑ Connect the Tx/Rx coaxial connectors J1 and J2.
- ❑ Connect the ribbon cable connector P201.

Microprocessor and Audio PCB

Removing the Microprocessor and Audio PCB

- ❑ Disconnect all cable connectors to the PCB.
- ❑ Remove the screw securing the heatsink block to the side panel.
- ❑ Remove the seven retaining screws and take out the PCB.

Re-installing the Microprocessor and Audio PCB

- ❑ Locate the PCB in its correct position and orientation.
- ❑ Replace the seven retaining screws.
- ❑ Replace the screw used to secure the heatsink block to the side panel.
- ❑ Connect all cable connectors to the PCB, ensuring correct orientation.

PA and Filter assembly

Accessing the PA and Filter PCB

- ❑ Remove the bottom cover (see page 5-2, *Circuit boards*).
- ❑ Remove the eight screws securing the screen cover to the PA assembly and remove the cover.

The PA output transistors can be replaced without removing the PCB from the heatsink (see page 5-15, *Replacement of PA transistors*).

Removing the PA assembly from the chassis

- ❑ Remove the covers (see page 5-5, *Removing the covers*).
- ❑ Disconnect the ribbon connector P1 and the two coaxial connectors J2 and J3.
- ❑ Disconnect all cables between the rear connectors and the Microprocessor and Audio PCB.
- ❑ Turn the unit over (heatsink facing up) and remove the three screws that secure the PA heatsink screen to the septum panel. Turn the unit over again (heatsink facing down).
- ❑ Remove the three screws and the one stand-off screw located at the four corners of the PA PCB.
- ❑ Carefully slide the PA assembly, complete with the heatsink, to the rear and clear of the main frame.

Removing the PA PCB

- ❑ Remove the four screws that secure the PA transistors to the heatsink.

  One of the PA transistor's retaining screws is concealed by capacitors C107 and C108. Remove these capacitors to gain access to the screw.
- ❑ Remove the screws securing the PCB to the heatsink.

  The 12 mm long screw removed from the driver heatsink must be returned to this position when re-assembling.
- ❑ Remove the earth screw and the three screws securing the rear panel to the heatsink.
- ❑ Lift the PCB clear of the heatsink. Remove the existing Thermaflow compound from the components before proceeding with any repairs. Take care not to damage the mica insulator located under the bias transistor V20.

Re-installing the PA PCB

- ❑ Ensure that all the surfaces that touch the heatsink are coated with a thermal conduction compound before installing the PCB.
- ❑ Replace the earth screw and the three screws that hold the rear panel to the heatsink.
- ❑ Replace the screws that hold the PCB to the heatsink.
- ❑ Replace the four screws that hold the PA transistors to the heatsink.
- ❑ Replace capacitors C107 and C108.

Observe the following:

- Take care to align the thermistor R34 and transistor V19 in their appropriate hole locations in the heatsink.
- Check the mica washer is under the transistor V20.
- Ensure the screws that were removed when the PCB was being disassembled, are installed in their correct locations.
- The screws should not be tightened until all the assembly is complete. The screws that secure the PA transistors should be tightened last to avoid straining the connections.

Front panel

Accessing the Display Panel PCB

- ❑ Remove the top and bottom covers (see to page 5-5, *Removing the covers*).
- ❑ Remove the four countersunk screws located at the sides of the front panel (two each side).
- ❑ Disconnect the cable connector to P201 on the Microphone and Audio PCB.
- ❑ Remove the two screws securing the back screen, then remove the screen.

The PCB contains surface mounted components. These can be accessed without removing the PCB.

Accessing the reverse side of the Display Panel PCB, microphone connector or keypad

- ❑ Remove the two control knobs (secured by nuts under the removable caps).
- ❑ Remove the three fixing screws (the screw that secures the voltage regulator IC9 is longer and includes an insulator).
- ❑ Carefully disconnect the three connectors and remove the PCB.

The replacement of the surface mounted components should not be attempted except by a technician experienced in handling surface mounted components.

Re-installing the Display Panel PCB

- ❑ Replace the Display Panel PCB.
- ❑ Connect the three connectors to the Display Panel PCB.

- ❑ Replace the three fixing screws. Remember to replace the insulator beneath voltage regulator IC9.
- ❑ Replace the two control knobs.

Control head

Accessing the Display Panel PCB

- ❑ Remove the two screws securing the back and lift out.
- ❑ Disconnect the cable connector from P4 and remove the cover.
- ❑ If you need to operate the control head while the cover is off, remove the P-clip clamping the cable before refitting the connector.

Removing the Display Panel PCB

- ❑ Follow the procedure on page 5-8, *Front panel*.

Fault diagnosis

General

The removal and substitution of components may damage the components and/or the printed circuit boards. In some cases, it is impossible to remove components without destroying them. It is important therefore, to carry out as much diagnosis as possible without removing components. Specific tests are described later in this section. The following general points should also be of assistance:

- Spare boards—If spare boards are held in stock, they may be substituted to localise the fault to one board.
- Transistor tests (static)—Transistor failures are most often due to open circuit base-emitter or base-collector junctions, or a short circuit between emitter and collector.

These types of faults can often be detected without removing the transistor, using the ohms range of an analogue multimeter or diode test on a digital multimeter.

The two junctions should both give the appearance of a diode, that is high resistance with the multimeter leads one way round and low resistance when the leads are reversed. Polarity depends on whether a PNP or NPN transistor is being tested. The resistance between collector and emitter should be high with the multimeter leads either way round. The circuit diagram should be examined for parallel paths before you remove a transistor that fails the following tests:

- Transistor tests (dynamic)—Some transistor faults can be diagnosed by measuring voltages within the circuit. One of the most significant voltage measurements is the base-emitter voltage. The polarity of this will depend on the type of the transistor (PNP or NPN). A base-emitter voltage between 0.6 to 0.8V should be measured on a forward-biased base-emitter junction (double this voltage for a Darlington transistor). With its base-emitter junction forward-biased the transistor should conduct. Some indication of satisfactory operation of the transistor can be obtained by measuring the voltage drop across its collector or emitter resistor and short circuiting its base to the emitter. The short circuit removes the forward bias cutting off the transistor, so that the voltage across the resistor is considerably reduced.
- Integrated circuits—If there appears to be no output from an integrated circuit, before replacing the device, it should be ascertained whether the failure is due to the IC or its load. As a general rule, if changes in the input cause absolutely no changes in the corresponding output, the IC should be suspected. If however, a very small change in output can be detected, the load is more likely to be the cause. Depending upon the circuit, make further tests by disconnecting resistors, capacitors etc to verify the diagnosis before removing the IC.

Reading the technical description and understanding how the transceiver functions will assist in diagnosing any possible faults that may occur.

Voltage measurements

On the circuit diagrams and relevant circuits, note that voltages are shown at various points under different conditions to enable the faulty section of the transceiver to be located.

Always check first the parameters listed in the tables below.

Table 5 -1: Display Panel PCB supply voltages

[🗁 04-02974]

Supply	Description	Regulator
"A" rail	+13.6 V nominal unregulated supply	
"B" rail	+10 V ±0.2 V regulated supply	IC9
+5 VA	+5 V ±0.2 V regulated supply	IC11
–7 V	–7 V ±1 V from charge pump supply	IC7

Table 5 -2: Microprocessor and Audio PCB supply voltages

[🗁 04-02976]

Supply	Description	Regulator
"A" rail	+13.6 V nominal unregulated supply	
"B" rail	+10 V ±0.2 V regulated supply	IC201
+5 VA	+5 V ±0.2 V regulated supply	IC202
+5 VB	+5 V ±0.2 V regulated supply	IC203

Table 5 -3: Rx/Exciter PCB supply voltages

[🗁 04-02972 and 04-03135]

Supply	Description	Regulator
"A" rail	+13.6 V nominal unregulated supply (supplies the crystal oven only)	
"B" rail	+10 V ±0.2 V regulated (supplied from Microprocessor & Audio PCB)	IC201
+5 VB	+5 V ±0.2 V regulated (supplied from Microprocessor & Audio PCB)	IC203
+18 V	+18 V ±1 V charge pump supply	IC11
+26 V	+26 V ±1 V charge pump supply	IC11

Table 5 -4: PA & Filter PCB supply voltages

[🗁 04-02973 and 04-03096]

Supply	Description	Regulator
"A" rail	+13.6 V nominal unregulated supply	
+5 V	+5 V ±0.2 V regulated supply (selected in transmit only)	IC2
+5 V	+5 V ±0.25 V zener diode supply	V1

No reception

- ❑ Check the Mute gate is closed (IC206 pin 12, +10 V) [🗁 04-02976].
- ❑ Check the supply voltages are correct (see page 5-11, *Voltage measurements*).
- ❑ Check the AGC measures 5.5 V ±0.3 V on the Rx/Exciter PCB [🗁 04-02972 Sheet 2]. If the AGC = 0 V, then check if IC209 pin 6 = 5 V when in Transmit mode.
- ❑ Use a signal generator and a series capacitor (about 100 nF) to apply a signal to the test points shown on the circuit diagrams. The receive levels and frequencies, shown on the RF and IF circuit diagrams, should cause the AGC to fall by about 0.5 V from its no signal level of approximately 5.5 V (under no fault conditions).

  Start at the 455 kHz IF amplifier and proceed back through the receive path towards the antenna. When the injected signal can not be heard any more or the AGC stops falling by 0.5 V (when applying levels shown on the circuit diagram), a close examination between the satisfactory and failed check points should indicate where the fault lies.
- ❑ In the case of an audio fault, apply a signal from the Signal Generator to the receiver input at a frequency set to approximately 1 kHz above the channel frequency (1 kHz below for LSB). With the aid of an oscilloscope, trace the audio signal path from the demodulator output to the loudspeaker.

  If the AGC is operating satisfactorily, the audio signal should be present at the output of pre-amplifier IC204/A test point TP206 (Rx DEMOD) [🗁 04-02972 and 04-03135]. This point provides the audio to the AGC circuit.
- ❑ If the receive fault shows as an oscillation or instability, check that the transmit mixers IC5 and IC8 do not have DC on pins 4 or 11 (< 0.5 V) [🗁 04-02972 and 04-03135]. Check the modulator IC202 has no DC applied to pin 5.

- ❑ If DC is measured at any of the points indicated:

  Check the base-emitter voltage of switching transistors V3 and V7. If it measures 0.5 V or more, check that the output voltages of NAND gates IC6/C and IC6/D are correct as shown on the circuit diagram.

  Check if DC can be measured on the mixer IC5 pins 4 and 11. If so, then unsolder and lift one side of resistor R35. Check if the voltage still appears at the collector of transistor V3. If so, suspect collector-emitter leakage of the transistor and replace the transistor. If DC still remains on pins 4 and 11 of the mixer, replace IC5.

  Check if DC can be measured on mixer IC8 pins 4 and 11. If so, then unsolder and lift one side of resistor R46. If the DC still remains on pins 4 and 11, replace IC8. If the voltage is only on the collector of V7 (with R46 lifted), apply a short circuit between IC202 pin 5 and ground. If the voltage goes from the collector of V7, then replace modulator IC202. If the voltage remains on the collector with pin 5 shorted, then replace V7 (collector-emitter leakage).

No transmit

- ❑ Check the supply voltages are correct (see page 5-11, *Voltage measurements*).

- ❑ Apply an audio signal of about 1 kHz at a level of 10 mV RMS to the microphone input connector J3 pin 2 and ground pin 3 on the control panel/head. Select Transmit mode (pin 5 to ground). With the aid of an oscilloscope, trace the audio, IF and RF signals through the transmit path. Check that the measured levels correspond approximately to the levels shown on the circuit diagrams. A reduction of signal or complete failure at any of the check points should indicate the approximate location of the fault.

Unlocked synthesiser

If VCO1 or VCO2 lose lock (H101 and/or H102 illuminate on the Microprocessor and Audio PCB [🗁 04-02976]):

- ❑ Check the 26 V supply is present and connected to the oscillator VCO1 (V8 and V9) and the control amplifier V11 and V13 [🗁 04-02972] or V12 and V18 [🗁 04-03135].

  If VCO2 has failed, check that 18 V is present at the control amplifier IC14/A pin 8 [🗁 04-02972 only].

- ❑ Check that VCO1 and VCO2 are oscillating.

  The frequencies at TP4 (VCO1) and TP8 (VCO2) should be within the range indicated on the diagram.

- ❑ Check the output levels of the prescalers IC9 pin 3 and IC12 pin 3. The frequency should be approximately the VCO frequency divided by 64 [🗁 04-02972 only].
- ❑ Check IC9 and IC10 pin 11 are high (approximately 5 V) when locked.
- ❑ Check that the VCO control voltages on TP1 and TP5 are within the limits as indicated on the circuit diagram (or TP1 and TP9 [🗁 04-03135]).
- ❑ Check that the Enable, Data and Clock pulses are present at the input of synthesiser integrated circuits IC10 pins 10, 11 and 12 and IC13 pins 11, 12 and 13 when changing channels (or IC9 and IC10 pins 5, 6, and 7 [🗁 04-03135 and 08-05332]).
- ❑ If only VCO2 is unlocked and the previous checks appear correct, alignment may be the cause of the failure. Re-set VCO2 (see page 7-11, *VCO2 adjust*).

PA failure

To optimise the amplifier performance, the PA output transistors are matched in pairs by a letter code. Measurements in this area depend upon the matched pair of transistors fitted and the frequency of transmission.

Table 5-5 is a guide to the peak-to-peak voltages expected at the specified points in the PA circuit. They are given for 100 W PEP full power output when driven with a two-tone input. For these tests the supply voltage should be 13.6 V and the output terminated into a 50 Ω load.

Table 5 -5: Peak to peak voltages

Frequency (MHz)	**Battery (Amps)**	**V15 (V PP)**	**V16 (V PP)**		**V21/V22 (V PP)**		**V23/V24 (V PP)**	
		E	C	E	C	B	C	B
2.5	9.0	0.15	1.5	0.15	11.0	0.25	30	2.2
3.5	9.0	0.20	1.5	0.20	12.0	0.28	30	2.5
5.5	9.5	0.30	1.7	0.30	12.0	0.40	32	2.8
8.5	9.5	0.35	2.0	0.35	12.0	0.50	36	3.0
15.5	10.0	0.45	3.5	0.45	18.0	0.80	35	4.5
17.9	12.0	0.50	3.5	0.50	20.0	1.30	30	4.8
26.5*	10.0	0.40	3.3	0.40	12.0	1.00	36	3.5

***** Measured at 80 W PEP.

Replacement of PA transistors

The PA output transistors V23 and V24 should only be replaced as matched pairs. The gain groupings of the SRFH1008 (selected MRF455) transistors are identified by a letter code and should be the same.

The PA output transistors can be replaced without removing the PA and Filter PCB from the heatsink. It is necessary to release only the screws securing the transistors.

- ❑ Unsolder and remove the capacitors C107 and C108 located between the collectors of the transistors.
- ❑ Unsolder and lift the driver transformer T3 secondary winding from the transistor bases.
- ❑ Remove the screw located between the heatsink fins that secures the output transformer to the heatsink.
- ❑ Unsolder and lift the output transformer T4 from the transistor collectors.
- ❑ Remove the flange fixing screws.
- ❑ Use a de-soldering tool or "solder wick" to remove the bulk of the solder at each connection. Remove the solder lugs from the emitters of the transistors. Gently pull the transistor legs away from the PCB while heating the joints.
- ❑ Clean away excess solder from transistor pads on the PCB.
- ❑ Clean the transistor mating surface on the heatsink with a cloth or tissue.
- ❑ Coat the transistor flange with a thin film of thermal compound (e.g. Jermyn Thermaflow). Note that you must not use too much thermal compound. Check the orientation and fit the new transistors.
- ❑ Refit the four flange mounting screws complete with the three solder lugs. Tighten the screws evenly.
- ❑ Carefully solder the transistor connections. This should be carried out quickly using a very hot soldering iron.
- ❑ Replace the screw that secures the output transformer to the heatsink.
- ❑ Solder the output transformer primary to the collectors and solder in capacitors C107 and C108.
- ❑ Re-adjust the bias current (see page 7-23, *PA adjustments*).

Control keypad

If there is a lack of response to button selections, it may be due to the malfunction of one or more of the sealed membrane switches. To test the switches, disassemble the control head and disconnect J1 [🗁 04-02974] and remove the Display Panel PCB. Connect a meter between each pair of pins as indicated in Table 5-6. An open circuit should appear if the switch is not operated and continuity (less than 100 Ω) when the switch is pressed.

Table 5 -6: Keypad connections

J1 Connector	Switch PCB	Button Function
1 - 5	1 - 6	On–Off
1 - 6	1 - 4	F1
1 - 7	1 - 2	Mode
2 - 5	3 - 6	Emgcy Call
2 - 6	3 - 4	USB/LSB
2 - 7	3 - 2	F2
3 - 5	5 - 6	Voice Mute
3 - 6	5 - 4	Tune
3 - 7	5 - 2	–
4 - 5	7 - 6	S'Call Mute
4 - 6	7 - 4	Scan
4 - 7	7 - 2	–

If any of these switches are faulty you need to replace the entire keypad.

Displayed error messages

Message	Description
ALE ACK timeout	Failure to communicate with ALE Controller 9300/9600.
ALE not initialised	The transceiver has not downloaded its information to the ALE Controller 9300/9600.
BAD ALE ACK	Failure to communicate with ALE Controller 9300/9600.
Bad record type XX	Data was corrupted during XP programming.
Bad type/inst XX/XX	The transceiver detected an internal data fault.

Message	Description
BBRAM Ck/Sum Err	Data corrupted in Battery Backup RAM IC112 [🗁 04-02976 Sheet 1].
BBRAM Update Failed	Cannot write data to Battery Backup RAM IC112 [🗁 04-02976 Sheet 1].
Disconnect Err	Transceiver received a "disconnect call" when not operating with an IPC–500.
External RAM Bad	On power up, unable to write to Parallel RAM IC104 [🗁 04-02976 Sheet 1].
FSK calibration fail	The selcall decoder is not calibrated.
I2C Bus Error XXXX:XXXX	Major hardware fault on one of the internal I^2C bus lines.
Intrnl Tmr Alloc Err	The transceiver detected an internal timer allocation error.
Loading ALE data	This should be displayed on power up for a short period when the ALE Controller is connected.
Low Battery	Battery supply is below 10 V.
No Channels Fitted	Cannot find any programmed channels. If programmed channels exist but cannot be located, the Parallel E^2PROM IC105 is corrupted [🗁 04-02976 Sheet 1].
No deflt rec for XX	The transceiver could not read a default record.
Parallel EEPROM Bad	Unreliable data from IC105 [🗁 04-02976 Sheet 1].
RAM Fault	Cannot read data from Parallel RAM IC104 [🗁 04-02976 Sheet 1].
RTC Ck/Sum Err	The transceiver detected a real time clock checksum error.
SEEPROM Ck/Sum Err	Data corrupted in Serial E^2PROM IC108 [🗁 04-02976 Sheet 1].
Serial BBRAM Bad	On power up cannot write reliably to Battery Backup RAM IC112 [🗁 04-02976 Sheet 1].
Serial EEPROM Bad	On power up cannot write reliably to Serial E^2PROM IC108 [🗁 04-02976 Sheet 1].
Serial EEPROM Fail XX	Detected error in writing data to Serial E^2PROM IC108 [🗁 04-02976 Sheet 1].
Unknown error: XX	The transceiver detected an unknown data error.
Unlock Error VCO1	VCO1 unlocked.

Message	Description
Unlock Error VCO1 and 2	VCO1 and VCO2 unlocked.
Unlock Error VCO2	VCO2 unlocked.
Writing SEE defaults	Now reprogramming serial E^2PROM with default settings.

7 Adjustments

Introduction

Preset adjustments, which are normally factory-set, will require attention only if components that affect their settings are replaced.

The 9323, 9360, 9390 or 9780 transceiver is provided with a special Test mode (see page 7-5, *Test mode*) that assists you to:

- align the receiver HPFs
- align the 45 MHz band-pass filter using only an oscilloscope, signal generator and a simple jig, made from an 820 Ω resistor and a 100 µF capacitor attached to clip leads
- align T201 and T202 in the 455 kHz IF filter
- check VCO1 (not adjustable)
- check and adjust VCO2
- adjust the USB channel frequency
- adjust the LSB channel frequency
- check the PA for band switching and intermodulation distortion at the top, bottom and centre of each filter band
- check receiver sensitivity at 22 selected frequencies between 1.6 MHz and 30 MHz

Test equipment required

The following test equipment is required:

- oscilloscope 50 MHz, complete with a 10X probe with a 10 MΩ and less than 20 pF input impedance
- RF dummy load 50 Ω and power meter rated at a minimum of 100 W RMS
- RF signal generator covering the range of 400 kHz to 30 MHz, with a calibrated output of 0.2 µV to 10 mV from a source impedance of 50 Ω
- frequency counter 50 MHz with a resolution of 1 Hz
- regulated power supply of 13.6 V ±0.2 V at 20 A peak
- two-tone audio generator operating at 700 Hz and 2300 Hz complete with 3 dB balance control and adjustable output 0–100 mV RMS
- digital multimeter 10 MΩ input impedance
- transceiver test unit to Codan drawing 04-03190

The microphone isolating transformer should be fitted with a mu-metal screen to prevent the 50 Hz mains from being picked up.

- resistance box fitted with E12 series resistor range 10 Ω to 1 MΩ to assist in the selection of the SOT resistors
- spectrum analyser for intermodulation measurements

Voltage regulators

None of the voltage regulators are adjustable. Only the output voltages can be checked.

Table 7 -1: Microprocessor and Audio PCB voltages

Test Point	Description
B	+10 V ±0.2 V regulated DC IC201
+5 VA	+5 V ±0.2 V regulated DC IC202
+5 VB	+5 V ±0.2 V regulated DC IC203

Table 7 -2: Rx/Exciter PCB voltages

Test Point	Description
+26 V	+26 V ±1.0 V charge pump supply
+18 V	+18 V ±1.0 V charge pump supply
TP2	Switched DC supply (IC6/C), B rail voltage in receive, 0 V in transmit
TP3	Switched DC supply (IC6/D), B rail voltage in transmit, 0 V in receive

Table 7 -3: PA and Filter PCB voltages

Test Point	Description
+5 V Switched	Regulated DC supply selected in transmit only (IC2) +5 V ±0.2 V No test point provided but can be checked at a number of places, for example, R43 or PTC R34
V1 Zener	DC supply to IC1 (V1) +5 V ±0.25 V Can be checked at IC1 pin 5

Crystal oven

The crystal oven (E1) on the Rx/Exciter PCB [🗁08-04962 and 08-05322] is attached to the reference crystal Z3. The oven should be checked after allowing a five minute warm up period. The temperature operates between 55°C and 65°C and is not adjustable. Replace the crystal oven if the results are outside the specified limits.

The high stability oven operates at a temperature of 65°C ±5°C. If measured externally, it will indicate approximately 5°C lower than the operating temperature. The oven is not adjustable and should be replaced if found to be faulty.

Test mode

The Test mode provides eleven test set-up procedures and 23 special channels. They enable the service technician to check the transceiver's performance and when necessary, carry out minor adjustments to ensure the equipment meets the specifications.

Table 7-4 details the eleven test facilities and the specific area targeted for the test. Table 7-5 and Table 7-6 detail the test channels.

Table 7 -4: Test facilities

Test	Details of Test	Checks
1	Sets VCO1 to 60 MHz Sets VCO2 to 44.5445 MHz	For checking VCO1 and VCO2 at centre frequency, see page 7-10, *VCO1 check* and page 7-10, *VCO2 check*.
2	Sets VCO1 to 75 MHz Sets VCO2 to 44.5485 MHz	For checking VCO1 and VCO2 at top frequency, see page 7-10, *VCO1 check* and page 7-10, *VCO2 check*.
3	Sets VCO1 to 45.25 MHz Sets VCO2 to 44.5405 MHz	For checking VCO1 and VCO2 at bottom frequency, see page 7-10, *VCO1 check* and page 7-10, *VCO2 check*.
4	Programs VCO1 between two frequencies centred at 8.4 MHz	Used for aligning the 45 MHz BPF with a CRO and Signal Generator.
5	Programs VCO1 and VCO2 to 44.544 MHz	Used for aligning the 45 MHz BPF using a spectrum analyser.
6	Sets Rx frequency to 1.40 MHz* Selects HPF 2–3.1	For aligning L19 in 2–3.1 HPF, see page 7-12, *HPF/LPF filter alignment*.
7	Sets Rx frequency to 2.18 MHz Selects HPF 3.1–4.8	For aligning L16 in 3.1–4.8 HPF, see page 7-12, *HPF/LPF filter alignment.*
8	Sets Rx frequency to 3.48 MHz Selects HPF 4.8–7.47	For aligning L13 in 4.8–7.47 HPF, see page 7-12, *HPF/LPF filter alignment.*
9	Sets Rx frequency to 5.30 MHz Selects HPF 7.47–11.6	For aligning L10 in 7.47–11.6 HPF, see page 7-12, *HPF/LPF filter alignment.*
10	Sets Rx frequency to 8.26 MHz Selects HPF 11.6–18	For aligning L7 in 11.6–18 HPF, see page 7-12, *HPF/LPF filter alignment*.
11	Sets Rx frequency to 12.6 MHz Selects HPF 18–30	For aligning L4 in 18–30 HPF, see page 7-12, *HPF/LPF filter alignment*.

* For 1.6 MHz Option LF fit 1.6 link on Rx/Exciter PCB after this test.

Accessing Test mode

Selecting the Test mode

- ❑ Switch off the transceiver.
- ❑ On the Microprocessor and Audio PCB [🗁08-04966], remove the shorting link parked on the two ground pins and fit to Link 1 (test).

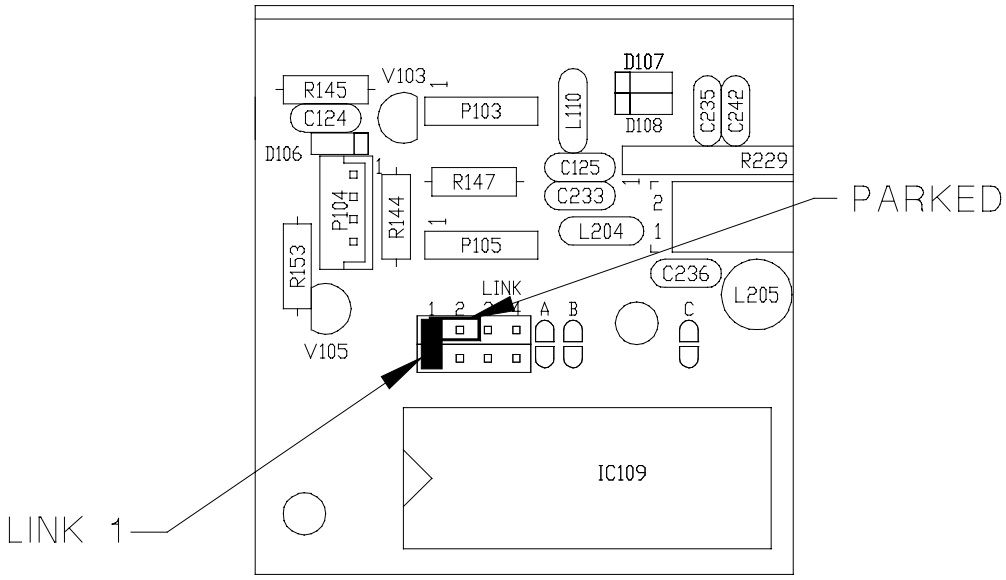

Figure 7 -1: Link 1 position

- ❑ Switch on the transceiver, which is now in the Test mode. In the Test mode the transceiver is fitted with a number of test channels specifically to check the performance of the transceiver.

Returning to Normal mode

- ❑ Switch off the transceiver.
- ❑ Remove the shorting link from Link 1.
- ❑ Replace the shorting link to its normal parked position. The transceiver will return to its normal operating mode.

Test channels for 2.0 to 26.5 MHz PA assembly

Table 7 -5: Test channels for 2.0 to 26.5 MHz PA assembly

🗁08-04963

Channel	Frequency MHz	PA LPF range	Receiver HPF	RF Amp	Talk Power Select	Remarks
1	2.0	2.0-3.1	2.0-3.1	On	Off	
2	2.5					
3	3.0					
4	3.1	3.1-4.8	3.1-4.8	On	Off	
5	3.5					
6	4.7					
7	4.8	4.8-7.47	4.8-7.47	On	Off	
8	5.5					
9	7.4					
10	7.5	7.47-11.6	7.47-11.6	On	Off	
11	8.5					
12	11.5					
13	11.6	11.6-18.0	11.6-18.0	On	Off	
14	15.5					
15	17.9					
16	18.0	18.0-27.0	18.0-27.0	On	Off	
17	22.0					
18	26.5					
19	27.0					
20	2.0	2.0-3.1	2.0-3.1	Off	On	See Note
40	19.999	18.0-27.0	18.0-27.0	On	Off	90-20523-XXX
41	20.001					Ver 4.2 onwards

Channel 20 (2.0 MHz) checks the transmit power with talk power on. Also the receiver sensitivity can be measured with the RF amplifier off. All remaining channels (1 to 19) have the talk power off. This allows the two-tone transmit signal to be viewed on the oscilloscope without the ripple being displayed.

All channels have the following enabled:

- USB/LSB/AM
- Emergency Call
- Selcall
- Two-tone

Test channels for 2.25 to 30 MHz PA assembly (1.6 to 30 MHz with Option LF fitted)

Table 7 -6: Test channels for 2.25 to 30 MHz PA assembly

08-05237

Channel	Frequency MHz	PA LPF range	Receiver HPF	RF Amp	Talk Power Select	Remarks
1	1.6	1.6-2.25	1.6-3.1	On	Off	Only with option LF fitted
2	2.0					
3	2.2					
4	2.3	2.25-3.45	2.0-3.1	On	Off	
5	2.8					
6	3.4		3.1-4.8	On	Off	
7	3.5	3.45-5.35				
8	4.5					
9	5.3		4.8-7.47	On	Off	
10	5.4	5.35-8.2				
11	7.0					
12	8.1		7.47-11.6	On	Off	
13	8.2	8.2-12.65				
14	10.2					
15	12.6		11.6-18.0	On	Off	
16	12.7	12.65-19.5				
17	16.5					
18	19.4		18.0-30.0	On	Off	
19	19.5	19.5-30				
20	27					
21	29.8					

Table 7-6 cont.

Channel	Frequency MHz	PA LPF range	Receiver HPF	RF Amp	Talk Power Select	Remarks
22	1.6		1.6-3.1	On	Off	Receiver
23	3.1		3.1-4.8			HPF
24	4.8		4.8-7.47			check
25	7.5		7.47-11.6			
26	11.6		11.6-18.0			
27	18		18.0-30.0			
28	26.5					
29	2.3		1.6-3.1	Off	On	See note
40	19.999		18.0-30.0	On	Off	90-20523-XXX
41	20.001					Ver 4.2 onward

Channel 29 (2.3 MHz) checks the transmit power with talk power on. Also the receiver sensitivity can be measured with the RF amplifier off. All remaining channels (1 to 28) have the talk power off. This allows the two-tone transmit signal to be viewed on the oscilloscope without the ripple being displayed.

All channels have the following enabled:

- USB/LSB/AM
- Emergency Call
- Selcall
- Two-tone

VCO checks and adjustments

VCO1 check

🗁08-04962
There is no adjustment for VCO1, which is located on the Rx/Exciter PCB. To check VCO1 is operating correctly perform the following in Test mode.

- ❑ Select Test 1.
- ❑ Ensure the screening can is over VCO1 and Mixer 1 for the test.
- ❑ Connect a DC voltmeter to TP1 and check for a reading between 9.0-11.5 V. The frequency at TP4 should measure 60 MHz ±100 Hz.
- ❑ Select Test 2.
- ❑ Check the voltage at TP1 reads 19-25 V. The frequency at TP4 should measure 75 MHz ±100 Hz.
- ❑ Select Test 3.
- ❑ Check the voltage at TP1 reads 2-4 V. The frequency at TP4 should measure 45.25 MHz ±100 Hz.

VCO2 check

🗁08-04962 and 08-05322
VCO2 is located on the Rx/Exciter PCB and can be checked in Test mode. The test point and measurement results for 🗁08-05322 are given in brackets.

- ❑ Select Test 1.
- ❑ Connect a DC voltmeter to TP5 (TP9) and check for a reading between 7.8-8.2 V. The frequency at TP8 should measure 44.5445 MHz ±100 Hz (44.5455 MHz ±100 Hz).
- ❑ Select Test 2.
- ❑ Check the voltage at TP5 (TP9) reads between 11-17 V. The frequency at TP8 should measure 44.5485 MHz ±100 Hz (44.5495 MHz ±100 Hz).
- ❑ Select Test 3.
- ❑ Check the voltage at TP5 (TP9) reads between 2-5 V. The frequency at TP8 should measure 44.5405 MHz ±100 Hz (44.54145 MHz ±100 Hz).
- ❑ If the measurements are not within the stated limits, adjust VCO2 (see page 7-11, *VCO2 adjust*).

VCO2 adjust

🗁08-04962 and 08-05322
The test point and measurement results for 🗁08-05322 are given in brackets.

Adjusting VCO2 in Test mode

- ❑ Select Test 1.
- ❑ Connect an oscilloscope to TP5 (TP9) and set up for 5 V per division and timebase to 2 ms per division.
- ❑ Short TP6 and TP7 together.
- ❑ Starting from the bottom of the coil, adjust L40 tuning core for a minimum repetition rate. Remove the short from TP6 and TP7.

✋ Great care must be taken to use the correct trimming tool to prevent damage to the tuning core.

- ❑ Connect a DC voltmeter to TP5 (TP9). Starting from the bottom of inductor L39, adjust the tuning core for a reading between 7.8-8.2 V. The frequency at TP8 should measure 44.5445 MHz ±100 Hz (44.5455 MHz ±100 Hz).
- ❑ Select Test 2.
- ❑ Check the voltage at TP5 (TP9) reads 11-15 V. The frequency at TP8 should measure 44.5485 MHz ±100 Hz (44.5495 MHz ±100 Hz).
- ❑ Select Test 3.
- ❑ Check the voltage at TP5 (TP9) reads 2-4 V. The frequency at TP8 should measure 44.5405 MHz ±100 Hz (44.5415 MHz ±100 Hz).

HPF/LPF filter alignment

HPF filter

The six high-pass filters are located on the Rx/Exciter PCB [🗁08-04962 and 08-05322]. Each filter contains an adjustable inductor in series with a capacitor to form a series tuned circuit. You will need to set up the following before checking the alignment of the inductors.

- ❑ Connect an audio voltmeter to the audio output (across the speaker).
- ❑ Adjust the volume control for a suitable noise reference point on the audio meter (about ¼ scale).
- ❑ Connect a signal generator to the receiver input.

It is important that the signal generator output level is always kept below the AGC threshold to ensure the optimum tuning point can be seen on the audio meter.

Checking the alignment of the inductors in Test mode

- ❑ Select the required test, signal generator frequency and the inductor number from the list for test numbers below.

Test		Signal generator frequency	Inductor
6	1.40 MHz	1.401 MHz ±100 Hz	L19
7	2.18 MHz	2.181 MHz ±100 Hz	L16
8	3.48 MHz	3.481 MHz ±100 Hz	L13
9	5.30 MHz	5.301 MHz ±100 Hz	L10
10	8.26 MHz	8.261 MHz ±100 Hz	L7
11	12.6 MHz	12.601 MHz ±100 Hz	L4

Test 6, L19 is adjusted with link 1.6 removed. Link 1.6 to be refitted after adjustment if used with 1.6 to 30 MHz PA assembly [🗁08-05237].

- ❑ Set the signal generator frequency to the correct frequency according to the list above.
- ❑ Adjust the output level for approximately +10 dB above the noise level indicated on the audio meter (1 kHz tone should be heard in the speaker).

- ❑ Adjust the required inductor for a minimum signal. If necessary, increase the signal generator output to maintain the audio above the noise level, while adjusting the inductor for a minimum tuning point.

LPF filter

There are two 30 MHz LPFs. Both are located on the Rx/Exciter PCB [🗁 08-04962 and 08-05322]. One is located in the Receiver input and the other is located in the Exciter output.

Alignment of the LPFs is not necessary, as each coil is pre-aligned.

The following is provided for information only:

Coil	**Frequency**
L21, L24	55 MHz
L22, L25	45 MHz
L23, L26	100 MHz

45 MHz filter alignment (08-04962)

🗁08-04962
There are two methods of aligning the 45 MHz BPF located on the Rx/Exciter PCB:

- using an oscilloscope and a signal generator
- using a spectrum analyser with a tracking generator

Both methods are detailed in the following two sections.

Alignment—method 1

The following steps detail the alignment procedure using an oscilloscope and a signal generator in Test mode.

❑ Select Test 4.

❑ Connect a 100 µF, 25 V electrolytic capacitor in series with an 820 Ω resistor between TP1 and 0 V (negative of capacitor to 0 V).

❑ Unsolder sweep link S—D24/D25 and R69 (coarse lock VCO1). Sweep link S is located below the VCO1 shield and below the yellow LED H1.

❑ Remove the shorting link parked on the two ground pins of link E–E and fit to B–E of noise limiter TP202.

Fitting the link to B–E opens the noise limiter gate.

❑ Connect the signal generator, which is set to a frequency of 8.4 MHz ± 100 Hz and an output of 0.7 mV PD to the receiver input.

❑ Connect an oscilloscope with a 10X probe to TP201.

❑ Connect External Trigger input to TRIG Test Point on the PCB. Set the oscilloscope to:

Channel one	20 mV per division using a 10X probe
Timebase	2 ms per division
Trigger External	Adjust the trigger for a constant sweep

❑ Adjust transformers T3 and T4 and inductor L30 for a minimum ripple response (see Figure 7-2).

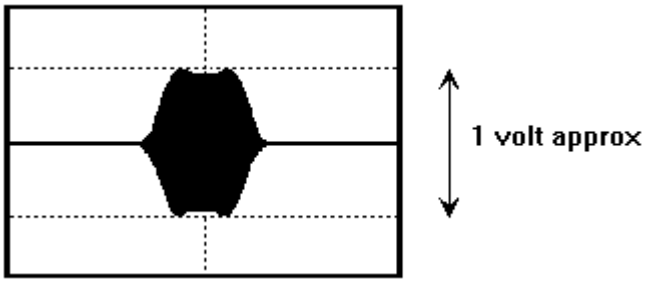

Figure 7 -2: Ripple response

- ❑ Remove the shorting link to B–E and return it to its parking position (ground pins of link E–E).
- ❑ Solder sweep link S.

Alignment—method 2

The following steps detail the alignment procedure using a spectrum analyser and tracking generator in Test mode.

- ❑ Select Test 5.
- ❑ Remove the shorting link parked on the two ground pins of link E–E and fit the link to B–E of noise limiter TP202.

  Fitting the shorting link to B–E opens the noise limiter gate.
- ❑ Connect the tracking generator set to an output of 7 mV RMS (–30 dBm) direct to the receiver input.
- ❑ Connect the spectrum analyser input to TP201 (50 Ω input is permitted). Set up the spectrum analyser as follows:

Centre frequency	455 kHz
Frequency span	100 kHz (10 kHz per division)
Vertical level	10 dB per division

- ❑ Adjust the spectrum analyser sensitivity to about −50 dBm to display the frequency response of the 45 MHz BPF.
- ❑ Adjust transformers T3 and T4 and inductor L30 for less than 2 dB ripple over 15 kHz span centred at 455 kHz. If desired, the vertical level can be changed to 2 dB per division to improve the resolution.

In this Test 5, VCO1 and VCO2 are set to 44.544 MHz allowing the receive frequency to equal the 455 kHz IF frequency. This allows the spectrum analyser and tracking generator to be used to align the BPF at a frequency of 455 kHz.

- ❑ Remove the shorting link to B–E and return it to its parking position (ground pins of link E–E).

45 MHz filter alignment (08-05322)

🗁08-05322
There are two methods of aligning the 45 MHz BPF located on the 08-05322 Rx/Exciter PCB. The two methods are:

- using an oscilloscope, a signal generator and a simple jig
- using a spectrum analyser with a tracking generator

These methods are detailed in the following two sections.

Alignment—method 1

The following steps details the alignment procedure using an oscilloscope, a signal generator and a simple jig. The circuit for the test jig is shown in Figure 7-3.

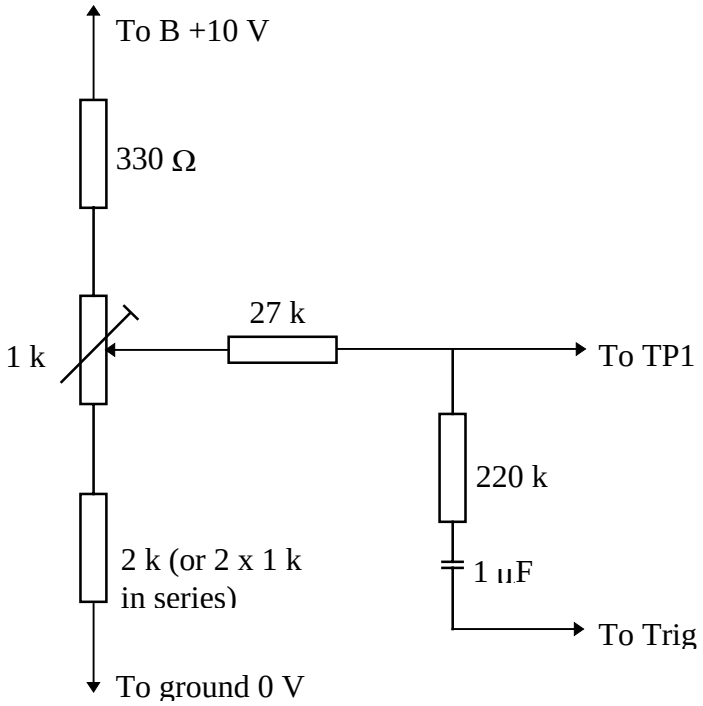

Figure 7 -3: Circuit for test jig

- ❑ Connect the test jig to the Rx/Exciter PCB [🗁08-05322] as shown in Figure 7-3.
- ❑ Unsolder sweep link S adjacent to TP1.

  This opens the synthesiser control loop by disconnecting the DC control line to the varicaps D20-D23.
- ❑ Remove the shorting link parked on the two ground pins E-E and fit to B-E of noise limiter TP202.

This opens the noise limiter gate and prevents the AGC from operating during the alignment.

- ❑ Set the signal generator output to 0.7 mV PD at a frequency of 8.4 MHz ±0.4 MHz.
- ❑ Connect the signal generator to the receiver input.
- ❑ Connect an oscilloscope with a 10X probe to TP201.
- ❑ Connect the external trigger input to TRIG Test Point on the PCB.
- ❑ Set the oscilloscope as follows:

Channel One	20 mV/division using the 10X probe
Timebase	2 ms/division
Trigger	External trigger

- ❑ Select Test mode by fitting the shorting link to Link 1 as shown in Figure 7-1.
- ❑ Switch on the transceiver, then select Test 4.
- ❑ Adjust the oscilloscope's trigger control for a constant sweep (positive trigger).
- ❑ Slowly adjust the potentiometer on the jig for a display on the oscilloscope similar to that show in Figure 7-2.
- ❑ Adjust transformers T3, T4 and inductor L30 for minimum ripple response.
- ❑ Switch off the transceiver.
- ❑ Remove the jig from the PCB.
- ❑ Remove the shorting link from B-E and return it to its parking position (ground pins E-E).
- ❑ Solder sweep link S.
- ❑ If you do not want to perform any other testing, remove the Test mode link on the Microprocessor PCB and return it to its parking position (see Figure 7-1).

Alignment—method 2

This alignment method is the same as given for 45 MHz filter alignment for assembly 08-04962 (see page 7-15, *Alignment—method 2*).

455 kHz IF and noise limiter alignment

🗁08-04962 and 08-05322
There are two tuned transformers in the 455 kHz IF circuit located on the Rx/Exciter PCB. T201 is located in the IF path to the sideband filter. T202 is located at the output of the noise limiter 455 kHz amplifier.

The alignment may be carried out either in the Test mode or normal operating mode.

Aligning the transformers in the 455 kHz IF circuit on the Rx/Exciter PCB

- ❑ Select any receive channel.
- ❑ Connect a signal generator to the receiver input. It should be set to 1 kHz above the selected channel frequency (1 kHz below for LSB) at an output of about 10 mV EMF.
- ❑ Fit a shorting link to B–E to disable the noise limiter gate.
- ❑ Connect an oscilloscope using a 10X probe to TP201. Set the oscilloscope as follows:

Timebase	50 µs per division
Channel One	50 mV per division (equals 0.5 V per division with the attenuation of the 10X probe)
Trigger	Auto

- ❑ Adjust T201 for maximum amplitude.

  Only a small change in amplitude will be seen due to the low Q of the tuned circuit.
- ❑ Remove the 10X probe from TP201.
- ❑ Connect a 1X probe to position A (part of noise limiter TP202).
- ❑ Set the oscilloscope to a sensitivity of 10 mV per division.
- ❑ Adjust T202 for maximum amplitude.
- ❑ Remove the shorting link to B–E and return it to its parking position (link E–E).

Exciter output transformer balance

🗁 08-04962

Alignment should only be necessary if the mixer IC5 or transformer T1 on the Rx/Exciter PCB have been replaced. To perform the alignment use a spectrum analyser. (For 08-05322 assemblies, R22 should be set to its mid-range position.)

- ❑ Select test channel 21 (27 MHz).
- ❑ Connect a 50 Ω dummy load to the antenna connector complete with a power meter.
- ❑ Connect a spectrum analyser via a 47 kΩ resistor to the antenna connector.
- ❑ Set up the spectrum analyser as follows:

Centre frequency	27 MHz
Frequency span	20 kHz
Vertical level	10 dB/div
Trigger	Continuous sweep
Video bandwidth	300 Hz

- ❑ Apply a two-tone audio signal of 700 Hz and 2300 Hz at a level of 20 mV RMS to the microphone input connector and select **PTT** (Transmit mode).
- ❑ Adjust the two-tone 27 MHz signal displayed on the spectrum analyser to the top of the screen.
- ❑ Remove the 2300 Hz tone and adjust the remaining 700 Hz tone for the same level produced by the two tones.
- ❑ Reset the spectrum analyser centre frequency to 18 MHz.
- ❑ Adjust R22 for a minimum 18 MHz signal.

  It may be necessary to solder link to C55 or C56 (never both together) to improve the balance. The unwanted 18 MHz product should be greater than 60 dB below the 27 MHz signal.

- ❑ Re-seal R22.

Frequency adjustment

🗁 08-04962 and 08-05322
All the channels are synthesised and locked to the 7304 kHz reference crystal (Z3) oscillator. The divided reference crystal oscillator (7304 kHz divided by 16) provides the local oscillator to the modulator and demodulator in USB mode. Therefore, it is only necessary to adjust the reference frequency for all channels on USB.

An additional divided crystal oscillator (1814 kHz divided by 4) provides the local oscillator to the modulator and demodulator in LSB mode.

Frequency adjust USB

Adjusting the frequency of the USB

- ❑ Select test channel 18 (2.0 to 26.5 MHz PA) or test channel 28 (2.25 to 30 MHz PA). Both channels are 26.5 MHz.
- ❑ Remove the coaxial connector from J1 on the Rx/Exciter PCB (removing the exciter output to the PA).
- ❑ Connect a frequency counter to Exciter output J1.
- ❑ Press the **Tune** button on the control panel.
- ❑ Adjust trimmer C116 [🗁 08-04962] or C115 [🗁 08-05322] (reference crystal adjust) to a frequency of 26.5 MHz ±5 Hz.

Allow at least five minutes from switch on before adjusting the frequency.

Frequency adjust LSB

Adjusting the frequency of the LSB

- ❑ Adjust frequency in the USB (see page 7-21, *Frequency adjust USB*).

  Remain on the same channel and leave the frequency counter connected.
- ❑ Select LSB.
- ❑ Press the **Tune** button on the control panel.
- ❑ Adjust C243 for 26.5 MHz ±5 Hz.

Mute adjustment

🗁08-04966
Mute is located on the Microprocessor and Audio PCB.

Adjusting the Mute

- ❑ Connect the transceiver to an antenna (a short length of wire will do).
- ❑ Select an unoccupied channel.
- ❑ Press **Voice Mute** to enable the audio mute.
- ❑ Commence with preset potentiometer R357 fully clockwise. Slowly rotate the control counter–clockwise until the mute gate closes and the receiver noise is heard in the loudspeaker (mute threshold).
- ❑ Rotate the control back in a clockwise direction a quarter turn.

  The mute should now be sensitive enough to operate on the weakest signal without false triggering on noise pulses. The sensitivity may be varied from this setting to suit individual requirements (counter–clockwise to increase sensitivity).

PA adjustments

🗁08-04963 and 08-05237

Driver bias

Adjusting the driver bias

- ❑ Disconnect exciter output to the PA by removing the connector from J2 on the PA and Filter PCB assembly.
- ❑ With the transceiver switched off and the DC supply disconnected, unsolder LINK (DC supply to the driver transistors V21 and V22) next to the black negative battery lead.
- ❑ Connect a multimeter, set to DC 100 mA range, in place of the removed link (+ positive to the left as viewed from the front).
- ❑ Connect the DC supply and switch on the transceiver.
- ❑ Select any transmit channel and operate the **PTT** (Transmit mode). Check the driver current measures 18 mA ±3 mA.

  If the current is out of the specified limit stated above it can be changed by selecting an alternative SOT resistor R54.
- ❑ Switch off the transceiver, disconnect multimeter and replace LINK with a length of TCW.

PA bias

Adjusting the bias of the output PA transistors

- ❑ Disconnect exciter output to the PA by removing the connector from J2 on the PA and Filter PCB assembly.
- ❑ With the transceiver switched off and the DC supply disconnected, unsolder fuse PA O/P (DC supply to the output transistors V23 and V24) next to the red positive battery lead.
- ❑ Connect a multimeter, set to DC 1 A range, in place of the removed fuse (positive to the left as viewed from the front).
- ❑ Connect the DC supply and switch on the transceiver.
- ❑ Select any transmit channel and operate the **PTT** (Transmit mode). Check the output transistor current measures 300 mA ±30 mA.
- ❑ If the current is out of the specified limits stated above, adjust preset potentiometer R59 to 300 mA ±30 mA.

❑ Switch off the transceiver and disconnect the DC supply and resolder fuse PA O/P.

If the fuse is broken, replace it with two strands (2 × 0.2 mm TCW) taken from a piece of 7 × 0.2 mm cable. Solder the wire to the two stakes. Extend the centre of the wire up to form an inverted Vee. Only solder at the wire ends attached to the stakes.

Output power

For PA assembly 08-04963 (2 to 26.5 MHz), link X1 is located above P1. You must check the following on link X1 before setting the output power.

- Soldered—required when setting the output power to 100 W PEP and reducing to 85 W PEP at 26 MHz. This complies with the licensing regulations in Australia.
- Unsoldered—required when setting the output power to 125 W PEP and reducing to 85 W PEP at 26.5 MHz.

For PA assembly 08-05237 (2.25 to 30.0 MHz or 1.6 to 30 MHz with option LF fitted), link X1 must remain fitted.

Setting the output power

❑ Ensure the Exciter output is connected to J2 on the PA and Filter PCB Assembly.

❑ Select any channel frequency between 4–6 MHz (test channel 8).

❑ Connect an average or PEP power meter with a 50 Ω dummy load to antenna connector J1.

❑ Connect the oscilloscope via a 47 kΩ resistor to antenna connector J1.

❑ Set the oscilloscope as follows:

Timebase	500µs per division
Trigger	Auto

❑ Connect the signal generator to provide two-tone audio signals (700 Hz and 2300 Hz) via the test unit to the microphone socket.

❑ Select transmit (**PTT**) and adjust the two-tone level (use the level adjust on the test unit) for microphone compression.

❑ Adjust the Oscilloscope "Y" sensitivity for on-screen display and adjust the trigger for a stationary waveform.

❑ Adjust the two-tone balance control for good crossover display.

- ❑ Select a value for the HIGH PWR SOT resistor R16 (nominally 8k2 to 12k) on the PA PCB for the following output power.

PA assembly 08-04963 (2 to 26.5 MHz)	100 watts PEP, link X fitted 125 watts PEP, link X should **not** be fitted.
PA assembly 08-05237 (2.25 to 30.0 MHz or 1.6 to 30 MHz with option LF fitted)	125 watts PEP, link X fitted

↳ The indicated PEP level with two-tone modulation will depend upon the type of measuring instrument as shown in Table 7-7.

Table 7 -7: Power output PEP vs measuring instrument

Power output PEP	**100 Watt**	**125 Watt**
Peak reading meter	100 W	125 W
RMS reading meter	50 W	62.5 W
Average reading meter (e.g. Bird Model 43)	40.5 W	50.6 W
Oscilloscope	200 V PP	224 V PP

- ❑ Check the two-tone waveform is clean and undistorted.
- ❑ The output power is factory set and not likely to be outside the specified limits. Check that there are no faults with the transmitter circuits before attempting to adjust the power output.

Output power 27 MHz band (9323 only)

Before setting the lower power required for the CB channels, set the high power (see page 7-24, *Output power*).

Setting the output power for the 27 MHz band

- ❑ Select test channel 19 [🗁 08-04963] or test channel 20 [🗁 08-05237]. Both channels are 27 MHz.
- ❑ Proceed as detailed on page 7-24, *Output power*.
- ❑ Select a value for SOT R17 for less than 12 W PEP (5 W average).
- ❑ Check the two-tone waveform is clean and undistorted.

Intermodulation

To check for high power, a range of test channel frequencies are provided. The test channels 2 to 20 can be used to check the six bands for Intermodulation Distortion (IMD) on the 2 to 26.5 MHz PA assembly. The test channels 4 to 29 can be used to check the six bans for IMD on the 2.25 to 30 MHz PA assembly (1 to 29 if the LF option is fitted). To check each band, there is a test channel allocated near the bottom, top and centre of each band.

To check for low power of the 27 MHz CB channels (9323 only) the 27 MHz test channel is used to check the IMD of the PA.

Use a spectrum analyser to test the IMD.

- ❑ Ensure the Exciter output is connected to the input J2 on the PA and Filter PCB Assembly.
- ❑ Connect a 50 Ω dummy load to the antenna output J1.
- ❑ Connect the spectrum analyser via a 47 kΩ resistor to the antenna output J1. This provides a low level output for the spectrum analyser.

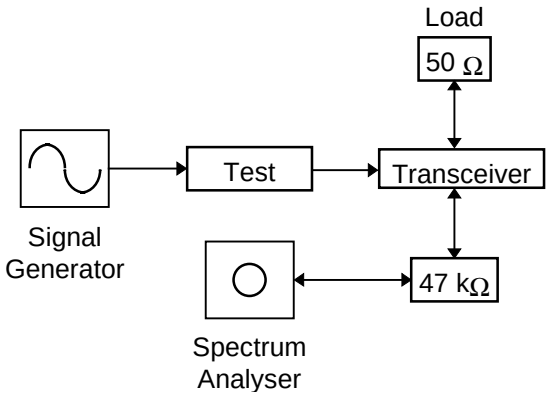

Figure 7 -4: Test set up

- ❑ Select the lowest frequency in the test channel (i.e. test channel 2 for the 2 to 26.5 MHz PA).
- ❑ Connect the signal generator to provide two-tone audio (700 Hz and 2300 Hz) via the test unit to the microphone socket.

- ❑ Set up the spectrum analyser as follows:

Centre frequency	Set to frequency of the selected test channel
Frequency span	20 kHz (2 kHz per division)
Vertical level	10 dB/div
Video bandwidth	300 Hz
Sensitivity	Depends on the signal level applied to the analyser and will require adjusting when transmitting

- ❑ Select **PTT** (Transmit mode) and adjust the two tones for compression.

  If the compression level is unknown, use an oscilloscope to check the output of the microphone amplifier at test point TX–AF [🗁 08-04966]. Adjust the output for a signal level of 500 mV PP.

- ❑ Adjust the two tones displayed on the spectrum analyser for equal amplitude by operating the balance control on the two-tone signal generator.

- ❑ Adjust the sensitivity control on the spectrum analyser to set the two tones at the top of the screen.

- ❑ Measure the intermodulation distortion levels at 2.5 MHz with respect to each tone. Add 6 dB to the reading if referenced to PEP (refer to transmit specifications for limits).

- ❑ Check the intermodulation distortion on the remaining frequencies including the 27 MHz channel for the 9323 (see Table 7-4). The centre frequency of the spectrum analyser must be set to the channel frequency selected.

To check for spurious and harmonic components during the IMD checks, adjust the frequency span of the spectrum analyser.

Receiver performance checks

Sensitivity and (S+N)/N ratio

- ❑ Connect an AC voltmeter across the audio output (loudspeaker).
- ❑ Select RF gain on test channel 3.
- ❑ Set the signal generator frequency 1 kHz above the SCF of the selected channel (1 kHz below for LSB).
- ❑ Connect the output, set to 0.15 µV PD (–123 dBm), to the antenna socket J1.
- ❑ Adjust the volume control for a suitable near full scale dB reading on the AC voltmeter. Take note of the reading.
- ❑ Switch off or adjust the signal generator output to a frequency outside the receiver band-pass. Check that the audio output drops by at least 10 dB.
- ❑ Repeat the above test with the RF gain off (test channel 20 for 2 to 26.5 MHz PA [🗁 08-04963] or test channel 29 for 2.25 to 30 MHz PA [🗁 08-05237]) and with the signal generator output set to 0.4 µV PD (-115 dBm).
- ❑ Check the audio output drops by at least 10 dB when the signal generator is switched off or tuned out of the band-pass.

AGC check

- ❑ Set up the equipment as for the sensitivity test (see page 7-28, *Sensitivity and (S+N)/N ratio*) but with the signal generator output set to 50 mV PD (-13 dBm).
- ❑ Adjust the volume control for a suitable, near full-scale dB reading on the AC voltmeter.
- ❑ Take note of the reading.
- ❑ Reduce the signal generator output until the receiver output drops by 6 dB. The signal generator level should be less than 2.5 µV PD (–99 dBm).

Audio output

- ❑ Set up the equipment as for the sensitivity test (see page 7-28, *Sensitivity and (S+N)/N ratio*).
- ❑ Connect an oscilloscope in parallel to the AC voltmeter across the audio output (loudspeaker).
- ❑ Increase the volume control and check the audio output exceeds 12 V PP at the onset of clipping displayed on the oscilloscope.

For this test it is advisable to replace the loudspeaker with an 8 Ω, 5 W resistor.

Selectivity (USB operation)

- ❑ Set up the equipment as for the sensitivity test (see page 7-28, *Sensitivity and (S+N)/N ratio*) but with the RF gain off (test channel 20 for 2 to 26.5 MHz PA [🗁 08-04963] or test channel 29 for 2.25 to 30 MHz PA [🗁 08-05237]).
- ❑ Set the signal generator output to 0.5 µV PD (−113 dBm).
- ❑ Take note of the audio output reference level on the AC meter.
- ❑ Monitor the signal generator using a frequency counter and adjust the frequency to −1 kHz and then to +4 kHz from SCF (USB).
- ❑ Increase the signal generator to 0.5 mV (−53 dBm) and check that the audio output is less than the reference level at both frequencies.

Clarifier operation

- ❑ Set the signal generator frequency 1 kHz above the SCF of the selected channel (1 kHz below for LSB).
- ❑ Connect the output to the antenna socket.
- ❑ Set the output to any level between 0.4-10 µV PD. The RF gain can be on or off.
- ❑ Select Clarifier mode and check the audio frequency changes with rotation of the **Select** knob in a clockwise and counter-clockwise direction.
- ❑ Check that the marker on the display moves left and right, and that pips are heard at the limits of each end of the control.

Noise limiter operation

- ❑ Check the RF gain is off (test channel 20 for 2 to 26.5 MHz PA [🗁 08-04963] or test channel 29 for 2.25 to 30 MHz PA [🗁 08-05237]).
- ❑ Set the signal generator frequency 1 kHz above the SCF of the selected channel (1 kHz below for LSB).
- ❑ Connect the output via a tee piece to the antenna socket J1.
- ❑ Set the signal generator to 0.4 µV PD.
- ❑ Connect a BNC to a two-terminal adaptor. Connect this to the other end of the tee piece.
- ❑ Connect the output of a square-wave generator to the adaptor via a 100 pF capacitor.
- ❑ Set the square-wave generator frequency to a 100 Hz and the output to 5 V PP.

  When the noise limiter is on**,** the signal produced by the signal generator should be clearly heard over the interfering signal from the square-wave generator.
- ❑ Switch the noise limiter off by shorting A–E on noise limiter test point TP202 located on the Rx/Exciter PCB [🗁 08-04962 and 08-05322].

  The noise from the square-wave generator should swamp the wanted signal from the signal generator. This test will verify the noise limiter is functioning correctly.

Transmitter performance checks

Frequency check

Check as detailed on page 7-21, *Frequency adjustment*.

ALC

- ❑ Use the transceiver test unit with the two-tone audio source (700 Hz and 2300 Hz) to modulate the transmitter.
- ❑ Increase the audio output slowly, in Transmit mode, until the output power just ceases to increase (ALC threshold).
- ❑ Note the PEP output and increase the audio input by 10 dB.

  The increase in output should be less than 0.5 dB above the ALC threshold.

Power output and intermodulation

PA assembly 08-04963, 2 to 26.5 MHz with 100 W PEP selected

Power output should be 100 W PEP at 2 MHz reducing to 85 W at 26.5 MHz (link X1 soldered on the PA PCB fitted). Intermodulation distortion (using 700 Hz and 2300 Hz two-tone modulation) should be better than –32 dB below PEP (–26 dB below each tone) as measured with a spectrum analyser (see page 7-26, *Intermodulation*).

PA assembly 08-04963, 2 to 26.5 MHz with 125 W PEP selected

Power output should be 125 W PEP at 2 MHz reducing to 85 W at 26.5 MHz (Link X1 **not** fitted). Intermodulation distortion (using 700 Hz and 2300 Hz two-tone modulation) should be better than –32 dB below PEP (–26 dB below each tone) as measured with a spectrum analyser (see page 7-26, *Intermodulation*).

PA assembly 08-05237, 2.25 to 30 MHz (1.6 to 30 MHz if option LF fitted)

Power output should be 125 W PEP at 2.25 MHz reducing to 80 W at 30 MHz. Intermodulation distortion (using 700 Hz and 2300 Hz two-tone modulation) should be better than –32 dB below PEP (–26 dB below each tone) as measured with a spectrum analyser (see page 7-26, *Intermodulation*).

The indicated PEP level with two-tone modulation will depend upon the type of measuring instrument used (see Table 7-8).

Table 7 -8: Power output PEP vs measuring instrument

Power output PEP	**100 W**	**125 W**
Peak reading meter	100 W	125 W
RMS reading meter	50 W	62.5 W
Average reading meter (e.g. Bird Model 43)	40.5 W	50.6 W

Emergency call (9323 only)

The Emergency Call facility is for use with the Australian Royal Flying Doctor Service (RFDS).

The two-tone modulation frequencies of 880 Hz and 1320 Hz are determined by the software. Therefore it is only necessary to carry out a function check as follows.

- ❑ Connect a 50 Ω dummy load and power meter to the antenna connector.
- ❑ Connect an oscilloscope via a 47 kΩ resistor to the antenna connector.
- ❑ Select a test channel.
- ❑ Operate the **Emgcy Call** and check the following:

Output power	Approximately 100 W PEP
Modulating tones	Approximately of equal amplitude (viewed on the oscilloscope)
	Heard in the loudspeaker

8 Parts list

General information

The parts lists for the PCB assemblies contain:

- circuit reference number
- descriptions, giving the value and type of component
- manufacturer and manufacturer's part number
- Codan part number

Items having numeric references identifying specific components or subassemblies may be encountered in the parts lists included in this manual. These items, selected from master manufacturing information, identify parts that are either useful for maintenance purposes or relate to other items and may be cross-referenced in the remarks column.

Table 8 -1: Resistor and capacitor abbreviations

Resistors	**Capacitors**
CC: carbon composition	AS: solid aluminium electrolytic
CF: carbon film	CC: ceramic multilayer chip
MF: metal film	CE: ceramic
MG: metal glaze	EL: wet aluminium electrolytic
MO: metal oxide	M: stacked mica
WW: wire wound	PC: polycarbonate
	PE: polyester
	PP: polypropylene
	PS: polystyrene
	PT: PTFE
	TA: solid tantalum

Ordering information

Orders for replacement components must include the following information. This will ensure that the correct parts are supplied and help speed up delivery times.

- equipment type (e.g. Type 9323, 9360, 9390 or 9780 transceiver)
- component location (e.g. Rx/Exciter PCB, 08-04962)
- component circuit reference number (e.g. R74)
- full component description (e.g. Resistor 1kΩ 5% 0.33W CF Res)
- manufacturer (e.g. Philips)
- manufacturer's part number (e.g. 2322 211 13102)
- Codan part number (e.g. 40-31000-020)

Component substitution

When replacing general purpose components (resistors, capacitors etc.), equivalent parts from other manufacturers may be used provided they have similar tolerances, voltage/power rating and temperature coefficients to the specified part.

Substituting components that do not exactly match those listed in the parts list will not adversely affect equipment performance.

Parts list

Table 8 -2: Parts list index

Title	Assembly No
Sundry Parts	08-04956-001
Display Panel	08-04964-001
Microphone Keyboard Encoder	08-04965-001
Microprocessor and Audio	08-04966-001
Rx/Exciter	08-04962-001 08-05322-001
PA Assembly c/w Heatsink	08-04963-001
PA Assembly c/w Heatsink (30 MHz)	08-05237-001
Filter, Low-pass (1.6 MHz)	08-05227-001
PA Exciter Interface S/assy	08-05226-001
RS232/ I^2C Interface	08-05181-001
500 Hz Filter Switch	08-05259-001
500 Hz Filter LO SW (900 Hz cf)	08-05260-002

9 Drawings

The drawings in this chapter consist of the mechanical and electrical diagrams required to maintain the 9323, 9360, 9390 or 9780 transceiver.

Table 9 -1: List of drawings

Title	Drawing	Drawing No
Control Head Layout		16-00109-001
Transceiver Layout		16-00109-002
9323, 9360, 9390 & 9780 Block Diagram		03-00902
Interconnection Diagram		04-02971
Display Panel	Circuit Diagram	04-02974
	PCB Assembly	08-04964
Microphone & Keyboard Encoder	Circuit Diagram	04-02975
	PCB Assembly	08-04965
Microprocessor & Audio		
Micro & I/O	Circuit Diagram	04-02976 Sht 1
Tx Audio	Circuit Diagram	04-02976 Sht 2
Rx Audio & S'Call	Circuit Diagram	04-02976 Sht 3
Microprocessor & Audio Assembly	PCB Assembly	08-04966
Rx/Exciter		
RF Mixer and Synthesiser	Circuit Diagram	04-02972 Sht 1
455 kHz IF Mod & Demod	Circuit Diagram	04-02972 Sht 2
Receiver/Exciter Assembly	PCB Assembly	08-04962
RF Mixer and Synthesiser	Circuit Diagram	04-03135 Sht 1
455 kHz IF Mod & Demod	Circuit Diagram	04-03135 Sht 2
Receiver/Exciter Assembly	PCB Assembly	08-05322
PA & Filter	Circuit Diagram	04-02973
	PCB Assembly	08-04963
PA & Filter (30 MHz)	Circuit Diagram	04-03096
	PCB Assembly	08-05237
Filter, Low-pass (1.6 MHz)	Circuit Diagram	04-03093
	PCB Assembly	08-05227

Table 9-1 cont.

Title	Drawing	Drawing No
PA Exciter Interface	Circuit Diagram	04-03092
	PCB Assembly	08-05226
500 Hz Filter Switch	Circuit Diagram	04-03104
	PCB Assembly	08-05259
500 Hz Filter Local Osc. Switch	Circuit Diagram	04-03105
	PCB Assembly	08-05260
Options		
F	Fitting instructions	15-10413-001
GP	Fitting instructions	15-10414-001
M	Fitting instructions	15-10415-001
PH	Fitting instructions	15-10434-001
RS232/I^2C	Circuit Diagram PCB Fitting instructions	04-03068 08-05181 15-00752-001