SECTION IV
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

Section IV describes the theory of operation for the RA6790/GM HF Receiver. The theory traces primary signal flow as it progresses through the various components of the Receiver and details the functional relationships of each component to the signal flow. This section is divided into two main discussions: (1) Functional, detailing, the primary signal flow as related to the Receiver's operation; and (2) a detailed circuit description of each assembly and the components included on each card. Simplified functional block diagrams, timing diagrams and tables are used throughout the text to aid the technician in understanding the theory of operation to the circuit level. (Refer to Figure 4-1.)

4.2 FUNCTIONAL THEORY OF OPERATION

The primary signal from the antenna input, through the Receiver, to the audio output and secondary functions as they are related to that primary signal flow are traced. For simplification and a basic understanding of receiver operation, the functions are divided into five major divisions (Figure 4-2): Primary Signal (RF, IF and AF), Oscillator Synthesizers, Automatic Gain Control (AGC), Receiver Control, and Power Supply. Additionally, while not a major signal processing section, a functional description of BITE is provided.

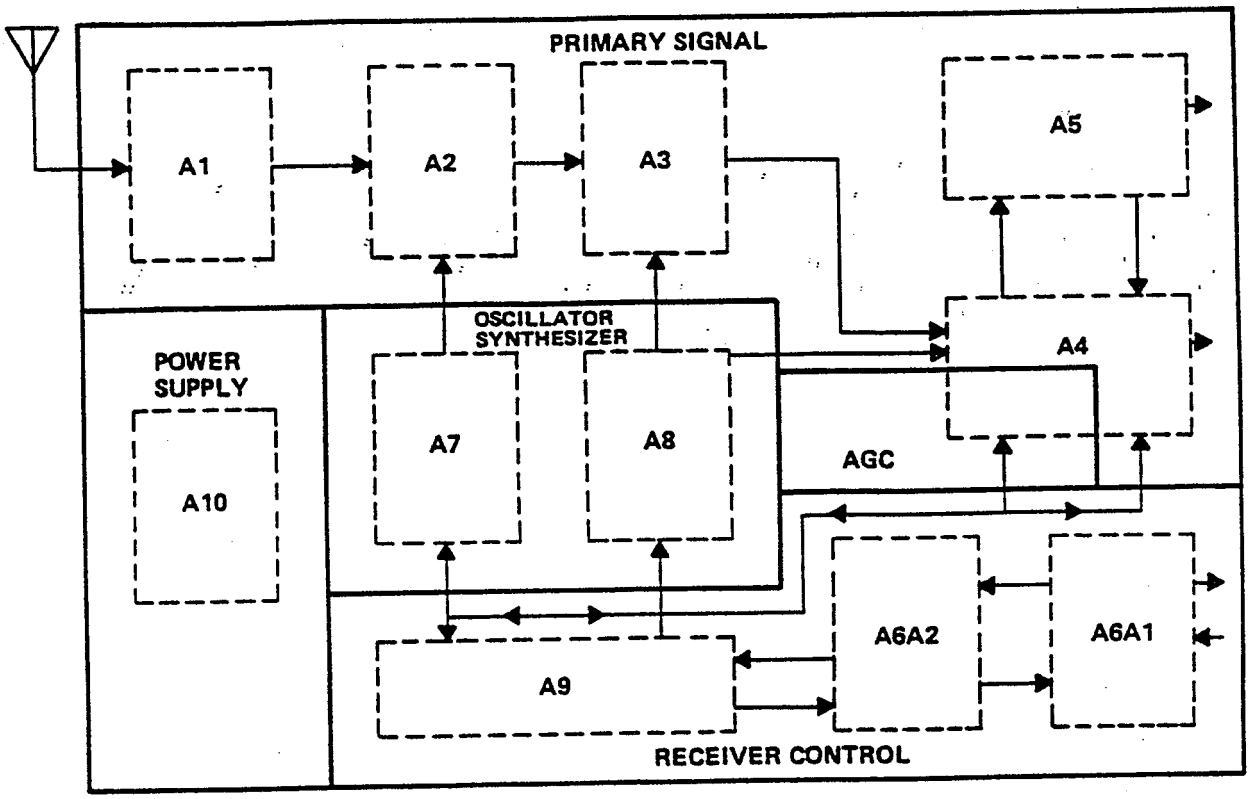
The circuit card assemblies associated with the primary signal flow include: A1, A2, A3, A4 and A5. The second major division describes the operation of the oscillator synthesizers (circuit card assemblies A7 and A8) from the first local oscillator signal to the first mixer, the second local oscillator to the second mixer and the beat frequency oscillator function for CW operation. The third division is the operation of the Automatic Gain Control (AGC) which is contained primarily on circuit card assembly A4 along with IF and AF components. Some other AGC circuitry is located on A3 and A5. The fourth division, Receiver Control circuitry which is contained on the front panel and circuit card assembly A6A1, A6A2, and A9, is described. The fifth major functional division of the Receiver is the power supply contained in assembly A10. Figure 4-1 shows an overall functional block diagram of the Receiver and should be followed in reading the description.

4.2.1 Primary Signal – RF/IF/AF Section

The primary signal consists of the Radio Frequency (RF) signal, the Intermediate Frequency (IF) signal, and the Audio Frequency (AF) signal.

4.2.1.1 RF Signal

The antenna signal is connected through the rear panel of the Receiver to a low pass filter located on assembly A1. The four section elliptical low pass filter rejects frequencies above 35 MHz and at the same time prevents local oscillator and IF frequencies from being radiated back through to the antenna. Each section of the filter contains a coil-capacitor tank circuit, with the coil of each stage adjustable for peaking the tank circuit. This provides optimum rejection at its designed frequency. The output of this first low pass filter is routed to another filter located on circuit card assembly A2. This filter operates much in the same manner as the one just described but also provides



Circuit Card Assembly	Nomenclature	Function
A1	RF Low Pass Filter	Primary Signal
A2	First IF Mixer	Primary Signal
A3	Second IF Mixer	Primary Signal
A4	Main IF/AF	Primary Signal/AGC
A5 (optional)	ISB IF/AF	ISB-Primary Signal
A7	First LO Synthesizer	Oscillator Synthesizer
A8	Second LO/BFO Synthesizer	Oscillator Synthesizer
A6A1 (optional)	Serial Asynchronous Interface	Receiver Control
A6A2	Microcomputer	Receiver Control
A9	Front Panel Control	Receiver Control
A10	Power Supply	Receiver Power

Figure 4-2. Basic Receiver Functional Breakdown

for impedance matching to the first mixer stage and to reduce peak to peak ripple on the carrier signal. The output of this filter is connected directly to the first mixer where the RF signal is mixed with the variable frequency from the first local oscillator to form the first IF signal.

4.2.1.2 IF Signal

The first IF signal is developed in the first mixer stage where the RF signal is mixed with the variable output frequency of the first local oscillator. The first local oscillator frequency is varied in direct relation to the RF frequency selected from the control section and varies between 40.955 (0.5 MHz selected) and 70.455 MHz (30 MHz selected). This variable frequency produces a different frequency in the mixer of 40.455 MHz. This difference frequency along with all other resultant frequencies is routed to a filter which rejects all other frequencies except the desired 40.455 MHz carrier with intelligence. The filter has a 20 kHz bandwidth and is coupled to a linear buffer amplifier. This amplifier stage is controlled by a control signal from the AGC circuit to maintain a constant amplitude output.

The AGC controlled IF signal is routed to circuit card assembly A3, where it is connected to a two stage IF amplifier, with additional between stage filtering. These two stages provide additional level control of the IF signal. This AGC controlled IF signal is impedance coupled to a band pass filter consisting of four stages of tuned filter traps. An adjustable amplifier just prior to the filters provides for adjusting the gain through the filters. The IF output from the filter is connected to the second mixer where the IF is mixed with the second local oscillator to form the second IF signal. The second local oscillator output of 40 MHz is mixed with the 40.455 MHz first IF, which provides a difference frequency of 455 kHz. This difference frequency is transformer coupled to a filter network which rejects all frequencies except the desired 455 kHz second IF signal. The output of the filter network is coupled to an IF amplifier to restore gain and for coupling to the plug-in band pass filters, contained on circuit card assembly A4.

The IF signal from A3 is coupled directly to seven bandwidth filter slots. The number of filters plugged in and the bandwidth of each filter depends on the option procured. Any number, up to seven, may be plugged into the card at any one time if optional filters were specified. The filter bandwidth desired for operation is then automatically switched into the IF circuit when it is selected from the front panel or remotely. When the optional independent sideband (ISB) is used, filter slot FL1 must contain a lower sideband filter. All bandpass filter slots are permanently connected to a diode switch, including FL1. This filter may be connected, through a movable link, from the diode switch to a bus that leads directly to the ISB circuit card assembly A5.

In all modes of operation, including ISB, the diode switch selects the desired filter slot. The control circuitry automatically selects the filters in an ascending bandwidth order regardless of the order in which they are plugged into the sockets; that is, bandwidth 1 (BW1) selects the narrowest bandwidth and so on with BW5 selecting the widest bandwidth. Two slots are generally reserved for upper sideband (USB) and lower sideband (LSB) which are also automatically selected when that mode is directed from the control section. The IF signal output of the selected bandwidth filter is impedance coupled to a two stage AGC controlled amplifier. The output of this amplifier is then coupled to a bandpass filter for additional filtering of the IF signal. A portion of this signal is routed through a buffer amplifier to J2-IF OUT, on the rear panel, as the IF output signal.

The IF signal is also coupled through a buffer amplifier to one input of an RF switch and to the product and synchronous AM detector. The RF switch also has the beat frequency oscillator (BFO) as an input with the output of the switch coupled directly to the FM detector. The switch has two modes of operation and is switched through the control circuitry. In the AM and FM modes the switch selects the IF signal, in all other modes, the switch automatically couples the BFO to the

FM detector and limiting amplifier. Two outputs of the FM detector is then coupled to a detector select switch and to the carrier input of the product and synchronous detector. The output to the product and synchronous detector will be either the demodulated AM signal or BFO depending on the mode selected. The detector select switch is also controlled by the function modes of the control section. In the FM mode the select switch passes only the FM detected signal to an audio filter. In all other modes the detector select switch passes the output of the product and synchronous detector to the same audio filter.

When the ISB is selected from the control section, the LSB portion of the IF signal is linked directly to circuit card assembly A5. The flow of the IF signal through the ISB circuit is very similar to that just described; except that the BFO is connected directly to the ISB detector. The USB portion of the IF signal is routed through the A4 circuit card in the ISB mode.

4.2.1.3 AF Signal

The detected audio signal from either the FM detector or the product detector is selected by the detector select switch through receiver control. The selected audio is routed through a lowpass filter to a crosspoint switch. Through receiver control the crosspoint switch selects the various audio modes available as outputs from the Receiver. When the ISB option is installed the audio output from that circuit card is also coupled to the switch. In non ISB modes the main audio (A4 card) is selected and routed to two separate audio amplifiers. The first amplifier is volume controlled through the AF GAIN control on the front panel. The output of this amplifier is routed both to the rear panel for loudspeaker output and to the phones jack on the front panel. The second amplifier is level controlled through a variable attenuator placed in the line to the second amplifier by the crosspoint switch. Attenuation is varied through a screwdriver adjustment on the front panel. This amplifier then drives an output transformer which provides the monitor line output to the rear panel. If the ISB circuit card is installed in this non ISB mode the output of the attenuator will also be routed through circuits on the ISB card and appear on Line 1 output on the rear panel. This circuit is described in the ISB mode which follows.

In the ISB mode either the main (USB) or the ISB (LSB) is selected and routed to the same circuits as described in non ISB mode. In addition the crosspoint switch couples both the LSB and USB through variable attenuators to their respective amplifiers on the ISB circuit card. The two amplifiers drive output transformers which couple the USB (Line 1 output) and LSB (Line 2 output) to the rear panel. Level control of Line 1 output is through front panel screwdriver adjustment MAIN-LINE LEVEL. Line 2 output is controlled through I-LSB LINE LEVEL. These two adjustments vary the attenuators connected in their respective lines.

4.2.2 Oscillator Synthesizers Section

The oscillator synthesizers consist of the first local oscillator (LO) synthesizer, the second LO synthesizer and the beat frequency oscillator (BFO) synthesizer. The three oscillator synthesizers are each independent separate oscillators except that the 1 MHz signal derived from circuitry in the second LO is used as a reference frequency to the other two oscillators.

4.2.2.1 First Local Oscillator Synthesizer

The first local oscillator provides the oscillator frequency to the first mixer where it is mixed with the RF signal to produce the first IF signal. This variable oscillator, located on circuit card assembly A7, is controlled from the receiver control frequency select. It is a voltage controlled single loop synthesizer oscillator with an output frequency variable between 40.955 and 70.455 MHz in 1 Hz increments.

A voltage controlled oscillator (VCO) generates the basic frequency which is applied to a drive amplifier located on circuit card assembly A2. This same output frequency is applied to the divide-by-N circuit. The value of N is determined by the digital control logic, which is also coupled to the divide-by-N circuit. This digital control logic depends on the RF frequency selection inputs. The output of the divide-by-N circuit is coupled to a phase comparator to which a 100 kHz reference signal and the digital logic is also connected. The basic output of the phase comparator depends on the phase difference between the reference signal and the divide by N signal. This basic output is combined with the digital control logic, filtered and applied to the dc control amplifier. The output of this dc amplifier controls the frequency of the VCO. The output of the VCO is transformer coupled to a high pass filter, located on circuit card assembly A2, which rejects frequencies below the oscillator range. This filter output is applied to a transistor drive amplifier which routes the signal through an RF wideband transformer to the mixer. The VCO is varied between 40.955 MHz (RF selection of 0.5 MHz) and 70.454999 MHz (RF selection of 30 MHz). When this oscillator frequency is applied to the mixer and mixed with the RF signal a difference frequency of 40.455 MHz is obtained. It is this difference frequency that is used for the first IF signal.

4.2.2.2 Second Local Oscillator Synthesizer

The second local oscillator provides the oscillator frequency to the second mixer where it is mixed with the first IF signal to produce the second IF signal. The oscillator, located on circuit card assembly A8, is a constant frequency phase locked oscillator driven from a reference signal. The output of the oscillator is 20 MHz which is frequency doubled to provide the 40 MHz signal to the second mixer. A reference signal, internal or external, is required for operation of the synthesizer. The internal reference signal comes from a crystal oscillator which has an output frequency of 5 MHz. An external reference signal may be applied through the REF IN/OUT connector on the rear panel. The INT/EXT slide switch S2, also located on the rear panel, must be in the appropriate position for the reference selected. With the switch in the EXT position, the internal reference oscillator is turned off and the external reference signal is applied through a transistor switch and shaper circuit to a phase comparator. With the switch in the INT position, access to any external reference is turned off, the internal oscillator is turned on and applied through the transistor switch in the same manner as the external reference.

The heart of the oscillator synthesizer is a 20 MHz crystal reference oscillator whose output is coupled through a buffer amplifier to a divide-by-2, divide-by-2, and divide-by-10 circuit. The resultant 10 MHz, 5 MHz and 1 MHz output of the circuit is coupled to a data select circuit. The 1 MHz signal is also routed to the BFO oscillator and to circuit card assembly A7, where it is used as a reference signal to the first local oscillator. The reference frequency output of the data select circuit is applied to the phase comparator which phase compares this signal to the internal or external reference. The phase difference signal (if any) is then applied through a digital to analog converter to the 20 MHz oscillator. If the oscillator tends to drift off frequency, the phase difference between the reference signal and oscillator signal will be detected by the phase detector and the phase difference, applied through the digital to analog converter, will readjust the oscillator.

The output of the oscillator is also coupled through another buffer amplifier to a frequency doubler. The 40 MHz output signal from this doubler is routed to circuit card assembly A3 and capacitor coupled to the second mixer. The difference frequency between this 40 MHz signal and the 40.455 MHz first IF signal is the second IF signal of 455 kHz.

4.2.2.3 BFO Synthesizer

The BFO provides the fixed and variable beat frequency for reinsertion of the carrier in the sideband and CW modes. The oscillator operates at the second IF signal frequency of 455 kHz and can be varied 8 kHz in either direction. The BFO oscillator, located on circuit card assembly A8, is a

voltage controlled variable oscillator with a center frequency of 22.75 MHz. The oscillator output frequency is filtered and applied through a buffer amplifier to a divide-by-50 circuit. The output of this divide-by-50 circuit provides the variable 447 to 463 kHz BFO signal for reinsertion at the product detectors on circuit card assemblies A4 and A5.

A digital control circuit is used to vary the basic oscillator frequency of 22.75 MHz. The output of this circuit is coupled to a phase comparator, along with a 500 Hz reference signal. This 500 Hz reference signal is derived by applying the 1 MHz reference signal, from the second local oscillator, to a divide-by-2000 circuit. The phase comparator compares the output of the digital control circuit and the 500 Hz reference signal and applies the difference signal through a digital to analog converter to the VCO. The oscillator may be varied between 22.35 and 23.15 MHz in 500 Hz increments, which when applied to the divide-by-50 circuitry, provides a BFO frequency between 447 and 463 kHz variable in 10 Hz increments. The BFO frequency is filtered before being routed to the product detectors.

4.2.3 Automatic Gain Control (AGC) Section

The AGC circuits provide the Receiver with constant level AF output signal with large variations in the incoming RF signal. For example, the change in IF or AF output levels is less than 6 dB for a change in the input level of −100 dBm to −10 dBm. This automatic gain control is accomplished through AGC circuitry, located mainly on circuit card assembly A4. The optional ISB circuit card assembly A5 contains its own AGC for signal gain control in the ISB mode of operation.

The Receiver may be operated in any one of three different gain control modes: manual, automatic, and automatic with a manually set threshold. In the manual mode, the gain is set through a front panel control. In the automatic mode, the AGC circuits will compensate for changes in the receiver input signal level. In the automatic/manual mode, the front panel control is used to set the operating threshold of the AGC circuits.

The AGC operates from a portion of the IF signal taken after the gain control IF amplifier stage, thus maintaining a closed AGC loop. The AGC detects the IF signal, provides three different decay times, and provides for automatic threshold control of the output signal or manual threshold control. The output of the AGC circuit is routed to the second IF amplifier on circuit card assembly A4 to a current amplifier on circuit card assembly A3. The current amplifier controls the first IF signal by controlling the gain of two IF amplifier stages; one located on circuit card assembly A3 and the other located on circuit card assembly A2.

4.2.4 Receiver Control Section

Signals that control the receiver's operational parameters (such as operational mode, receiver frequency, BFO frequency, bandwidth, AGC and BITE sequence) are produced by the microcomputer (A6A2) and routed by the front panel receiver control circuit card assembly (A9). The microcomputer under program control follows instructions it receives from the front panel in LOCAL operation and from the remote controller in REMOTE operation. In both LOCAL and REMOTE, the microprocessor functions essentially the same; however, when being operated from a remote location, the power must be turned on at the front panel and the optional serial asynchronous interface assembly (A6A1) must be installed. The serial asynchronous interface circuit card assembly (A6A1) interfaces the external remote controller (when used) with the microcomputer.

Figure 4-1 shows the receiver control circuits and shows the signal flow between the front panel receiver control assembly (A9), the microcomputer circuit card assembly (A6A2) and the serial asynchronous interface circuit card assembly (A6A1). The front panel receiver control assembly (A9) contains the Liquid Crystal Displays (LCD), connects to both sets of keyboard switches

and the receiver control circuits and routes data between these units and the microcomputer. The RA6790/GM interconnections diagram contained in Section VII show all connections to and from these modules.

As shown in Figure 4-1, the microcomputer (A6A2) directs receiver operations by interfacing with circuits on the receiver control assembly (A9) and serial asynchronous interface (A6A1) and sending control signals to various receiver circuits. The receiver control assembly (A9) contains the tuning mode and frequency displays and the tuning control circuits and connects to the frequency select and the modes select keypads. The strobes and selection circuits that route data under microprocessor control are also on the receiver control assembly. The strobe and selection circuits control the transfer of information between the front panel and the microcomputer as well as between the microcomputer and the receiver circuitry.

The basic functions performed by the microcomputer (A6A2) include:

1. Initialize circuits following power application.
2. Read local input signals from front panel controls.
3. Update front panel displays.
4. Compute and send receiver tuning and operating data to the appropriate receiver circuits.
5. Receive commands from the remote controller and upon request, return receiver status.
6. Retain memory of receiver setting at power failure or turn-off and restore receiver to the operational modes when power is reapplied.

The microcomputer directs receiver operations by executing the control program that it obtains from the Erasable Program Read Only Memory (EPROM). During local operation, the receiver is controlled by the microcomputer as follows:

a. The frequency and mode setting established by the front panel switches and the tuning control are continuously read at 25 ms intervals by the microcomputer. The actual scanning function of the microcomputer is under program control. As the microcomputer scans the front panel switch and controls, it also stores the current status of each control parameter in the memory (RAM).

b. The microcomputer, again under program control, uses the stored control parameters that it placed in memory to compute the control signals that it sends to the receiver circuits (1st LO Synthesizer, 2nd LO and BFO, and main IF/AF). These digital control signals are then sent to the receiver circuits through the receiver control assembly (A9) to generate the desired operation.

c. Periodically, as established by the control program, the microcomputer reads the receiver status that it has stored in memory (RAM) and sends this information to control the front panel displays.

d. When the microcomputer senses a BITE (Built In Test Equipment) request from the front panel switches, it is directed to perform the BITE test sequence and follows the BITE program which is also contained in memory. During BITE sequence the processor disables all external and local controls.

NOTE

The receiver control program and the BITE program have been developed by the manufacturer as part of the receiver design and cannot be changed or updated by the customer for either operational control or maintenance.

During remote operation, the receiver is controlled by the microcomputer, but in place of instructions from the front panel, the instructions to the microprocessor are obtained from the remote controller:

1. During the front panel scan, the microprocessor monitors the position of the LOCAL-REMOTE switch. When this switch is in REMOTE, the microprocessor will branch to the remote mode portion of the program so that instead of responding to front panel switches, it will look for command words from the remote interface card (A6A1).

2. Commands from the remote controller are received by the Serial Asynchronous Interface Assembly A6A1. As each command is received, an interrupt is sent to the microcomputer which directs the microcomputer to branch to specific portions of the program (or subroutine) to carry out the command. After responding to the command instructions, the microcomputer returns to the normal remote mode program until a new set of commands or requests are received from the remote controller.

3. When the remote controller contains data for receiver control (such as frequency, AGC, or mode selection) the microcomputer stores the data in memory (RAM), and on completion of remote data interrogation transfers the information to the receiver circuits.

4. When the remote controller command contains a request for receiver status, the microprocessor accesses the corresponding receiver status information stored in memory (RAM) and sends it via the Serial Synchronous Interface Assembly (A6A1) to the Remote Controller.

5. In addition, the microcomputer under program control periodically (every 25 ms) reads the receiver parameters from memory (RAM) and continually updates the front panel displays.

When a request is received from the remote controller during LOCAL operation, the microprocessor will respond and return the status of the receiver as described in the above paragraphs. Remote commands received during LOCAL operation will be stored in memory but they will not be acted upon unless the receiver is placed in REMOTE operation.

The microcomputer directs all operations and communicates with other receiver control circuits through its 8 bit bi-directional data bus and the write/read and clock (ROMC) lines. The ROMC lines indicate the type of instructions to be performed with the write and clock lines providing the necessary information. The 8-bit bus provides both bi-directional data and unidirectional address capability (to the Receiver). The operating control program is contained in the program memory EPROMS (Erasable Program Read Only Memory). Temporary storage for receiver settings and for data computations is provided by the Working Random Access Memory (RAMs), which can be written into and read out of by the CPU. These memories are addressed by the CPU, through the static memory interface (SMI). The CPU sends the ROMC, write and clock signals to the SMI. The SMI recognizes the ROMC code calling for a Memory Address operation. The SMI, in sequence, addresses the ROM or RAM over the memory address bus. Then it sends a read signal to the EPROM (if it is addressed) or sends a read or write signal to the RAM (if it is addressed). The CPU places the data to be read by the RAM on the data bus or reads the data placed on the data bus by the ROM or RAM, as appropriate.

The microcomputer (A6A2) also contains the RESET and RAM data retention circuitry. The RESET circuitry generates reset signals when power is applied and turned off. This reset signal is applied to the CPU. When power comes on, the CPU initializes all circuitry to its starting condition and causes the program to start at its initial program address. When power is removed, due to power turn-off or power failure, the reset signal to the CPU goes low. The CPU now causes the system to

come to an orderly halt. In addition, the memory data retention circuitry (at power turn-off) connects an internal battery to the RAMs so that the receiver settings are retained in this memory. Thus when power is reapplied, the receiver will be reset to its last operational condition when power was interrupted. Also, at power turn off, the memory retention circuitry places the RAM in a lower power drain mode which retains memory but draws a minimal amount of power from the internal battery. When external power is applied, the internal battery is charged by the external power supply.

The CPU, in programmed sequence, receives and sends data from and to the front panel displays and controls, and the receiver control circuitry (through A9) via the CPU data bus. The data is directed between the CPU data bus and the receiver control and front panel circuitry, in the correct program sequence, by the bi-directional, tri-state switch. This switch is controlled by the strobe logic which is driven by the ROMC, write and clock signals from the CPU. The addressing of the various receiver and front panel circuitry, to accept or supply data from or to the data bus, in the prescribed program sequence, is done by the strobe logic and tri-state latched switch. This switch is driven by the CPU data bus and its outputs latched to the input data from the bus, at the prescribed program times, by the strobe logic.

The CPU receives and sends data from and to the remote controller via the Serial Asynchronous Interface (module A6A1). Data to and from the CPU and module A6A1 is sent directly over the CPU data bus. Additional control signals between the CPU and the module A6A1 are sent via the CPU I/O (input-output) ports. A UART (Universal Asynchronous Receiver Transmitter) in the A6A1 module interfaces the parallel 8-bit data word on the CPU bus to the serial data streams in and out from and to the remote controller. The UART also generates and sends to the CPU an interrupt request whenever the remote controller sends commands or data. This requests the microcomputer to orderly stop its present program and jump to a program routine which will service the remote controller commands and data. The UART and interrupt logic on the A6A1 module will supply the CPU with the interrupt routine starting address by placing this interrupt vector address on the CPU data bus when the CPU acknowledges that it will service the interrupt request. The reset signal from the microcomputer module is also sent to the interface module to initialize its circuitry at power turn-on.

As indicated in the block diagram, Figure 4-1, the front panel receiver control, module A9, connects to the keyboard switch panels 1 and 2. These switches are continually read. in program sequence, by the CPU. The switches are read in groups, with the switches being selected by enabling their associated data select buffers. The data select and strobes circuitry selects the buffers, in the programmed sequence, as directed by the strobe logic and tri-state latched switch outputs from the microcomputer A6A2. The read data goes on to the buffered data bus and then through the data buffers and the bi-directional, tri-state switch to the CPU bus. It should be noted that the digital outputs from the tuning knob encoder and digital data outputs from the IF/AF (A4 module) are read out here as if they were additional switches.

Both the tuning mode and frequency indicating front panel Liquid Crystal Displays (LCD) are contained on module A9. These displays are continually updated by the microcomputer CPU. The displays are driven by decoder-drivers which are enabled by their respective data select and strobes. The data from the CPU bus is applied to this circuitry, at the correct times in the program sequence, through the data buffers and bi-directional tri-state switch. The operating and tuning data developed by the microprocessor is relayed to the appropriate receiver circuitry through module A9. The buffered data bus goes directly to the main IF/AF module, A4, with the data select and strobes circuitry supplying the strobes to the various circuits in this module. Data to the 1st LO and 2nd LO/BFO modules are generated, in the proper program sequence, through the data select and strobes circuitry in the A9 module. Data to the 1st LO consist of a strobed and clocked serial data stream. The 2nd LO/BFO data consist of a binary coded digital word for the BFO frequency and an ON-OFF signal for the BFO. It should be noted that OOL (Out of Lock) signals from the 1st LO, REF and BFO drive

the OOL indicators located on the A9 card. The OOL overall signal, generated by the microcomputer, is sent to the front panel OOL indicator through A9.

The serial asynchronous interface module, A6A1, in addition to the UART and interrupt circuitry described earlier, contains circuitry for selecting and generating serial data mode and baud rates and for setting the receiver address when the receiver is used in the remote mode.

4.2.5 Power Supply Section

The power supply provides the various dc voltages required throughout the receiver. The unit, located on assembly A10, contains a step-down transformer, diode rectifiers, filter capacitors and regulators. Primary input power is controlled through a POWER ON switch located on the front panel. This primary input power may be either 100, 120, 220 or 240 volts from 43 to 420 Hz. The proper voltage is selected through a pc wafer and voltage selector located on the rear panel of the receiver. The step-down transformer provides three different voltages for rectification, filtering and regulation. Six different dc voltages are provided at the output of the power supply. These voltages are +20 Vdc regulated, +15 Vdc regulated, +15 Vdc unregulated, −15 Vdc regulated, +5 Vdc regulated and +5 Vdc unregulated.

4.2.6 Built In Test Equipment (BITE) Functional Description

The BITE system of the receiver has the ability to perform two major functions. First, it determines, organizes and displays the bandwidth of the IF filters installed in the receiver. This allows the installation of these filters in any slot, with minimum limitations. Secondly, the BITE performs tests of functionality of the receiver modules. These tests provide overall verification of the operation of the receiver, and specific verification of the operation of selected modules. The BITE performs the following functional tests in the receiver: Readability of the RAM in the microcomputer; lock condition and timing of all phase locked loops; settling time in the frequency synthesizers; operation of the IF AGC; operation of the ISB AGC detector if it is installed; and measuring the bandwidth of all of the IF filters. In order for the receiver to pass the above tests, all modules must have been operating properly. However, A1, A6A1, A4 and A5 are not interrogated.

BITE may be controlled by the operator from the front panel of the receiver through the simultaneous use of two controls, one on each keypad. This minimizes the likelihood of accidental interruption of an operating receiver. To initiate BITE from the front panel, the operator must press both the LOCK and the AM pushbutton switches, then release AM and then LOCK for initialization. The microcomputer then begins the full BITE sequence. As the microcomputer is executing the BITE program, the front panel display indicates what the receiver is actually doing. For instance, frequency, BFO and mode data are displayed. Should an error be discovered the front panel frequency display is blanked except for a two digit error code which contains the number of the test that failed. The operator writes down the number of the test that failed then pushes both LOCK and CW and then releases CW and then LOCK, which tells the microcomputer to continue to the next test. The displays are reinstated and the testing proceeds. The displays remain active throughout the tests since the process takes approximately one minute to complete, and if the displays are moving, the operator has confidence that the tests are proceeding. When the test is finished, the receiver will return to the signal it was monitoring prior to being told to perform the BITE test sequence. Should the operator wish to terminate the BITE cycle at any time, he may press and hold LOCK and LSB then release LSB then LOCK and the receiver will revert to its normal pretest operation at a point in the sequence where disabling the process is allowed. In addition to being able to originate the test, to continue the test, and to stop the test, there is (for maintenance purposes) a loop facility which can be invoked by using both LOCK and USB pushbuttons. In this mode, the front panel controls, with the exception of LOCK and USB, are disabled but the microcomputer will continuously supply the signals required to perform the failed test so that additional fault isolation procedures, using external test equipment, may be employed.

The BITE sequence may also be initiated by a remote device. The remote control device sends a message to the receiver telling it to initiate BITE. BITE will then report up to a maximum of five errors and then report a test complete code upon request. If the test complete code is received with no fault numbers, then the receiver passed the BITE tests. The control device may send a message to the receiver asking for the installed IF filter bandwidths. The receiver would then send the measured bandwidths to the controller showing the filter slot positions in which each filter is installed.

During initialization, BITE is initiated if the microcomputer determines that the memory has been corrupted for some reason. This automatically initiated BITE will determine the receiver filter complement, organize a filter assignment table, and return the receiver to operation. When performing this test, the receiver does not stop on errors but completes the testing and restores receiver operation. The receiver also does not stop on errors when BITE is initiated under remote control, but completes the sequence and stores the fault numbers for remote interrogation. The following discussion describes the actual tests conducted to verify the proper operation of each module.

a. Microcomputer. All 256 bytes of the Random Access Memory (RAM) in the microcomputer are tested to ensure that the memory may be written into and read out of properly. A ones and zeroes memory pattern is used to perform this test.

b. Second Local Oscillator and BFO. The lock status of both the BFO and the second local oscillator synthesizers is tested. The second local oscillator synthesizer should be locked at all times. The BFO is enabled by placing the receiver in the CW mode. The BFO synthesizer is then tested for a lock condition both at 455 kHz and all 500 Hz steps between and including plus and minus 8 kHz offsets. This dynamic program also checks the switching times of the BFO synthesizer as indicated by the out-of-lock circuitry on the BFO board. A failure in any of these tests is indicated as an error code to the operator or to the remote controller, on request.

c. First Local Oscillator. Testing of lock, in 500 kHz intervals from 30 MHz to 0 MHz, is performed, and the switching time of the synthesizer throughout the band is tested utilizing out-of-lock signals as the indication for reaching lock after each step.

d. IF Module. The IF module (A4) is checked to determine whether or not the AGC circuits operate properly on signals. The test routine enables the CW detector and BFO, and checks that an audio output is present during the initial filter tests. The manual IF gain attenuation system is tested by observing its control effects on the audio output level during the filter tests.

e. ISB Module. When the optional ISB board (A5) is installed it is checked for proper AGC action along with the IF gain and the manual IF gain control, in the same way that the main IF board (A4) was checked.

f. IF Filters. One of the major functions of the BITE is to determine the bandwidths of the IF bandwidth filters installed in the receiver, and assign them to bandwidth selection switches BW1 through BW5. The filters are assigned in order of increasing bandwidth and allow the operator to select a desired bandwidth. In addition, two different types of single-sideband detection filters may be used and the bandwidth determination routines verify their correct installation. Two sideband filters may be installed in the receiver for independent or normal sideband operation. one for upper sideband, the other for lower. (When ISB is installed these two filters are required.) If one symmetrical sideband filter is to be used for both sidebands it may be installed in filter slot FL1. Then for lower or upper sideband, the first and second local oscillators are offset by 1.8 kHz to accommodate the symmetrical filter. There is one restriction on the filter complement in the receiver; the FL1 slot must contain the filter to be used for lower sideband. It may be either the independent offset sideband filter or a symmetrical filter, but in either case it must be the filter used for lower

sideband. The BITE bandwidth routine checks the filter in the FL1 slot to determine whether or not it is a center-tuned filter or an offset filter. If center tuned, it uses the filter for both sidebands by putting a 1.8 kHz offset in the first and second local oscillator. If it is an offset filter, the filter slot that the filter is in is labeled for the lower sideband and the rest of the filter complement is searched for the matching USB filter. If a symmetrical filter is found to be installed in the FL1 slot, the offset for the first and second local oscillators is set to 1.8 kHz; however, if an offset sideband filter is found with a symmetrical filter in FL1 slot an error will occur. If there are less than 5 symmetrical filters installed in the remaining slots of the receiver, the symmetrical filter in FL1 is used as a center tuned filter which may be used for the AM, FM, or CW detection mode. If five other filters are present in the system, the symmetrical sideband filter will be used only for sideband reception. The remaining filter slots, FL2 through FL7, are checked for presence of a filter, except for a slot which has previously been identified as the USB slot. If there is a filter present in a slot, its bandwidth is measured. The first LO is scanned, in frequency, from a 10 kHz maximum offset back to the 3 dB point, based on a previously measured center frequency reference level. (NOTE: This reference level can vary from filter to filter.) The frequency difference between the center referenced level and the 3 dB point is designated as half the actual bandwidth. Having measured the bandwidth of all the filters installed. the filters are sorted in order of increasing bandwidth so that when the BW1 pushbutton switch on the front panel of the receiver is pressed, the narrowest bandwidth available is selected. When the BW2 pushbutton switch is pressed, the next narrowest progressing to the widest at BW5 (if there are less than 5 symmetrical filters installed in slots FL1-FL7 the widest one is assigned a number corresponding to the maximum number of symmetrical filters installed). Future filters which may have different bandwidths from the filters presently defined may be used in this system without any change. The bandwidths of the filters installed in the receiver can be reported to the remote controller upon command. In the remote operating mode, if the remote controller asks for a specific bandwidth, the receiver selects the bandwidth that is nearest to the bandwidth requested. The Receiver reports the actual bandwidth used to the remote controller. This is an indirect check on the filters.

4.3 DETAILED CIRCUIT DESCRIPTION

This section provides a detailed description of all electronic circuits contained in the receiver. Refer to Figure 4-1 for an overall functional block diagram. Figure 4-2 lists the circuit card assemblies in the order that they are described in the following paragraphs. Simplified functional block diagrams along with timing diagrams and tables are used throughout the text to aid in simplifying the description. Components referred to throughout the text are referenced by their last two reference designators. Block diagrams referred to throughout the text should be used in conjunction with applicable schematic diagrams in Section VII.

4.3.1 RF Low Pass Filter, A1

The incoming RF signal is passed from the RF IN connector J1 to a 50 ohm, 4 section elliptical lowpass filter which has a cut-off frequency of 35 MHz (refer to schematic diagram, Figure 7-1). This filter provides the necessary protection to the Receiver from image signals at frequencies between 81.4 and 111.4 MHz; and from signals at the first intermediate frequency of 40.455 MHz. The filter also prevents first local oscillator reradiation from the antenna connection. Each section of filter consists of a tank circuit, consisting of a tunable coil (L1 through L4) and capacitor (C2, C4, C6 and C8), connected sequentially in the receiver line with a second capacitor (C1, C3, C5, C7 and C9) connected from each tank circuit parallel to the signal flow. Each tank circuit is tuned to provide a high resistance to a particular frequency while other frequencies are reflected in the parallel capacitor which in turn reflects this signal to the next stage and so on.

4.3.2 First Mixer, A2

Figure 4-3 is a simplified block diagram of the first mixer module A2. It consists of a signal lowpass filter, first mixer, bandpass filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the first local oscillator frequency of 40.955 to 70.455 MHz. The schematic diagram for the first mixer is shown in Figure 7-2.

4.3.2.1 RF Signal Lowpass Filter and Mixer

The output of the A1 module is connected to the first mixer through a two section elliptical lowpass filter (L15-C23, L11-C24-C25 and L12-C26-C27), which has a cut off frequency of 35 MHz and serves to present a defined impedance to the mixer, U1, RF input port. This filter operates much in the same manner as the RF input filter, except the first input coil L15 is non-adjustable. It offers a very low impedance to the incoming wanted RF signal, but an increasingly higher impedance to frequencies above 30 MHz. The mixer U1, is used for mixing both the incoming RF signal (0.5 to 30 MHz) and the first local oscillator signal (40.955 to 70.455 MHz). The resultant frequencies are taken from the mixer, and filtered to provide a difference frequency of 40.455 MHz to form the first IF signal.

4.3.2.2 First Local Oscillator Input Filter and Drive Amplifier

The filter for the incoming first local oscillator signal is comprised of four sections of a tunable coil (L1 to L4), connected in series with a capacitor (C2, C4, C6 and C8) and with the combination of the two connected parallel to signal flow. A second capacitor (C1, C3, C5 and C7), connected in series with signal flow separates each coil capacitor. Each coil is tuned for maximum impedance for a desired frequency. The series capacitance acts as a high impedance to undesired frequenices below 40 MHz. The output of this filter is coupled to a common emitter amplifier Q2 through capacitor C9 and resistor R3. The mixer drive amplifier is comprised of transistors Q1, Q2, Q3 and Q4. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of common emitter amplifier, Q2, whose current is regulated by transistor Q1. The voltage at the base of Q1 is set by divider R1 and R2 which in turn sets the potential at the emitter of Q1. Thus the current through R6 is regulated by bias control of Q2 via R6 and L6. The output of Q2 is capacitance-coupled (C21 and C22) to a complementary pair amplifier made up of PNP transistor Q3 and NPN transistor Q4. The output of this pair is applied directly to transformer T1 to drive the LO input to mixer U1. The mixer also receives the RF input from A1 as described above.

4.3.2.3 AGC Controlled IF Amplifier

The output of the mixer is coupled to a bandpass filter FL1. This crystal bandpass filter is designed to reject all the resultant mixer frequencies, except the difference frequency of 40.455 MHz with a bandwidth of 16 kHz. This 16 kHz bandwidth provides an additional option in the AM, FM, or CW modes of operation. This first IF signal is coupled through C44 to an impedance matching network of L16, C32 and R14, and to a linear amplifier consisting of field effect transistor Q5. A dual tapped transformer T3, makes up part of the load circuit of Q5, to which is connected a current controlled AGC signal. This AGC signal, in effect, varies the impedance of the load transformer which in turn varies the gain of Q5. A second signal from the AGC circuit is applied to the gate of Q5 which varies its bias in relation to the AGC signal strength. This results in a high linear AGC controlled first IF signal, for output to the second mixer circuit card assembly A3.

4.3.3 Second Mixer, A3

Figure 4-4 shows a simplified functional block diagram of the second mixer circuit card assembly A3. It consists of a three stage AGC controlled first IF amplifier, a bandpass filter, a mixer

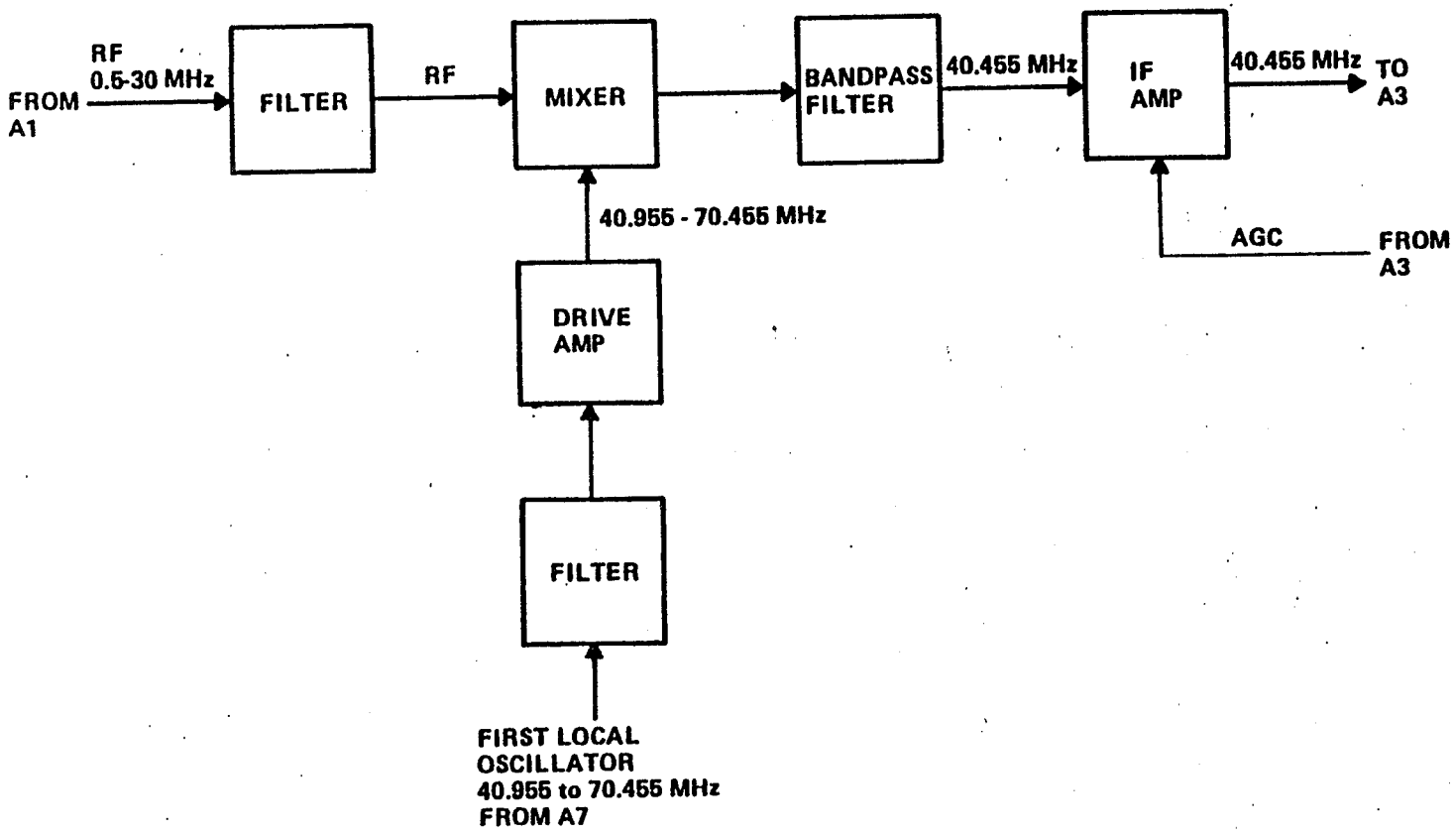


Figure 4-3. First Mixer, Functional Block Diagram

and output second IF amplifier. Input signals to the circuit card include; the first IF signal from A2, AGC signal from A4, and the second local oscillator signal from A8. The output signals consist of AGC output to A2 and the second IF signal to A4. Figure 7-3 shows the schematic diagram for the second mixer, A3.

4.3.3.1 First IF Amplifier

The first IF amplifier consists of three stages with the second stage gain controlled from the AGC signal. The third stage drives the signal for input to the bandpass filter. The 40.455 MHz signal routed from A2 is coupled to the drain of field effect transistor Q1, through capacitor C1. The grounded gate of this stage provides high gain for input to filter FL1 through capacitor C5. Filter FL1 provides for rejection of all frequencies other than the 40.455 IF signal. The output of the filter is connected through capacitor C6 to the drain of field effect transistor Q2, which also has a grounded gate. The load circuit of Q2 consists of resistors R16 and R18 and a dual tapped transformer T1. The AGC signal is connected to one tap of the transformer and, in effect, varies the impedance of the load transformer. This action varies the gain of the amplifier in relation to the AGC signal. The output of this stage is taken from the second tap on the transformer and coupled to the base of NPN transistor Q3, through capacitor C11 and resistor R20. A variable coil that forms part of the first section of a four section bandpass filter is connected into the load circuit of Q3. The output of Q3 is, therefore, reflected directly into the bandpass filter. A variable resistor R26 in the emitter circuit of Q3 provides for gain adjustment of this stage.

4.3.3.2 Bandpass Filter, Mixer and Second IF Amplifier

The bandpass filter consists of four tunable tank circuits (C15-L5, C16-L6, C17-L7, and C14-C19-L8), each made up of a tunable coil and a capacitor. Each stage is tuned to resonate at the first IF signal frequency and reflects its output to the next section for finer tuning and so on. The output of this filter is coupled directly to the input of integrated circuit mixer U3. A 40 MHz signal from the second local oscillator is connected to a second input of the same mixer. It is this difference frequency that is used as the carrier for the second IF signal. All other frequencies are rejected through the filter consisting of capacitors C31 and C32 and coil L9. The output of the mixer, U3, is connected to a tapped load transformer T2. The output is taken from that transformer tap and coupled through C24 and the filter, just described, to an integrated amplifier U4. This stage provides amplification for the second IF signal output from A3.

4.3.3.3 AGC Amplifier

A two section AGC amplifier is contained on circuit card assembly A3 which provides for both voltage and current control of a signal from AGC circuits on A4. This controlled AGC signal is applied to two IF signal stages for level control. One of the IF stages controlled is located on circuit card assembly A2 and described in paragraph 4.3.2.3. The second AGC controlled IF amplifier is on A3 and is described in Paragraph 4.3.3.1. An AGC signal from the AGC circuit on A4 is routed through resistor R2 to two separate amplifiers. The first amplifier is a two stage feedback amplifier consisting of integrated operational amplifiers U2B and U2C. The highly regulated output of this amplifier is routed to circuit card assembly A2 and used as the bias control to the gate of that output IF amplifier. The same AGC signal through resistor R2 is routed to an integrated operational amplifier U2A. This amplifier has both its negative and positive inputs regulated through voltage regulating transistors U1A (positive) and U1B (negative). The action of these transistors control the bias voltage to the operational amplifier which in turn controls its output current flow. The output of this amplifier stage is then coupled to transistor U1C which amplifies the signal and applies it to the IF amplifier through resistor R19 and diode CR1. The diode prevents IF signal feedback to the amplifier. This signal then controls the gain of that IF amplifier in relation to the AGC signal from A4. The output of the operational amplifier U2A is also coupled to the base of transistor U1D which buffers the signal for application to the IF amplifier stage on A2.

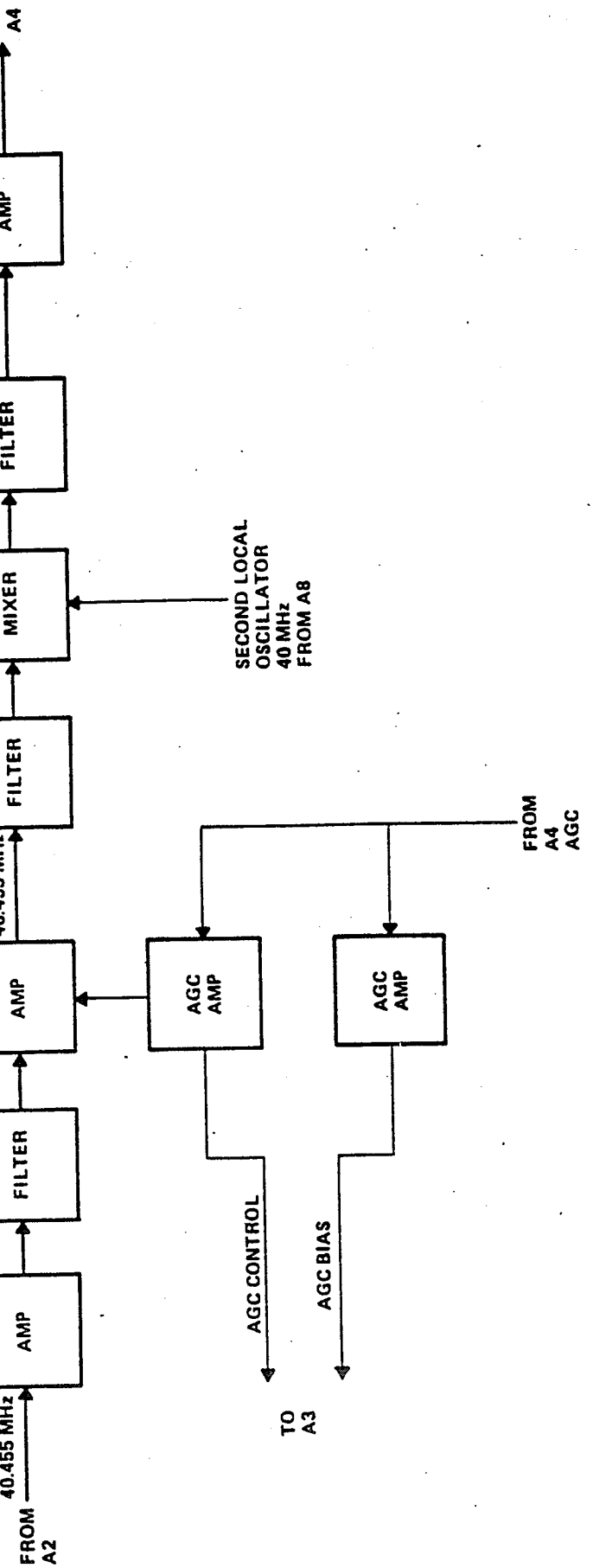


Figure 4-4. Second Mixer, Functional Block Diagram

4.3.4 Main IF/AF, A4

The Main IF/AF circuit card assembly A4 contains IF circuits, AF circuits, and AGC circuits. The description of these circuits are divided into those three basic functions and shown in three separate simplified block diagrams in Figures 4-5, 4-6, and 4-7. Receiver control circuits are also contained on A4 and are described under the A9 circuit card. Input signals to the circuit card include: the second IF signal from A3, the BFO signal from A8, audio and AGC signals from A5 and control signals from A9. Output signals from the board include: second IF signal to A5, BFO, audio and AGC signals to A5, audio signals to A9 and to the rear panel, AGC signals to A3, and control signals to A9. The schematic diagram for the A4 circuit card is shown in Figure 7-4.

4.3.4.1 IF Circuits

Figure 4-5 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4. This circuitry consists of the bandpass filters, their switching circuitry. a four stage IF amplifier, an IF output amplifier, an RF switch, a limiting amplifier and FM detector, and a product and synchronous AM detector. The second IF signal routed from A3 is connected directly to seven 455 kHz bandpass filter sockets FL1-FL7. These sockets provide for plugging in up to seven optional preselected filters of various bandwidths. These filters optionally available in bandwidths from 0.4 kHz to 16 kHz, may be changed at the customer's discretion, (refer to Section 1). Selection of a particular installed filter is then accomplished automatically through the receiver control system. Each filter socket is connected to a diode switch which is controlled from the receiver control circuits. The output of the diode switch for filter FL1 must be linked to the common output of all the other filter switches, if it is used in A4 operation. If it is to be used for the ISB operation, then it must be linked to the output for that circuit card assembly A5. The receiver control is programmed to select and switch into the circuit the filters in ascending order of bandwidths, regardless of the order in which they are plugged into the sockets; that is, when BW1 is selected, from receiver control, the narrowest bandwidth contained in the seven sockets (six if ISB is installed) will automatically be selected. BW2 will select the next widest bandwidth and so on with BW5 selecting the widest bandwidth. Two filters are generally reserved for USB and LSB operation, which are also selected automatically when those modes of operation are called for through receiver control.

The common output of the diode switch which consists of CR1 through CR14, R9 through R22 and C21 through C27, is connected through resistor R25 to the base of transistor Q1. This emitter follower stage acts as a buffer between the diode switch and the input to a two stage IF amplifier U8 with AGC control. An incoming AGC signal is applied to each stage of the integrated circuit amplifier and provides for level control of the IF signal. A variable resistor R39 connected between the output of the first stage and the input of the second stage provides for manual adjustment of the gain of the IF signal. Variable resistor R47 is used for adjusting the AGC signal level. The output of the two stage IF amplifier is connected to a filter consisting of capacitors C44, C46 and C47, resistor R50 and tunable coils L1 and L2. This double tank circuit provides for rejecting unwanted spurious signals. The output of the filter is routed through capacitor C49 to two separate functions; a three stage IF output amplifier and an emitter follower amplifier Q6. The first stage, Q7, of the IF amplifier is an emitter follower which provides buffering between the incoming signal and the second stage Q8. This second stage amplifies the signal and connects it to still another emitter follower stage Q9 for buffering to the IF OUT connector J2, located on the rear panel.

The emitter follower amplifier Q6 acts as a buffer in the same manner as Q7 above but its output is routed to three separate functions; the AGC detector circuit, the product detector and the FM detector through the RF switch. The signal routed to the AGC detector is described under AGC control circuits. The IF signal routed to the FM detector U18 through the RF switch

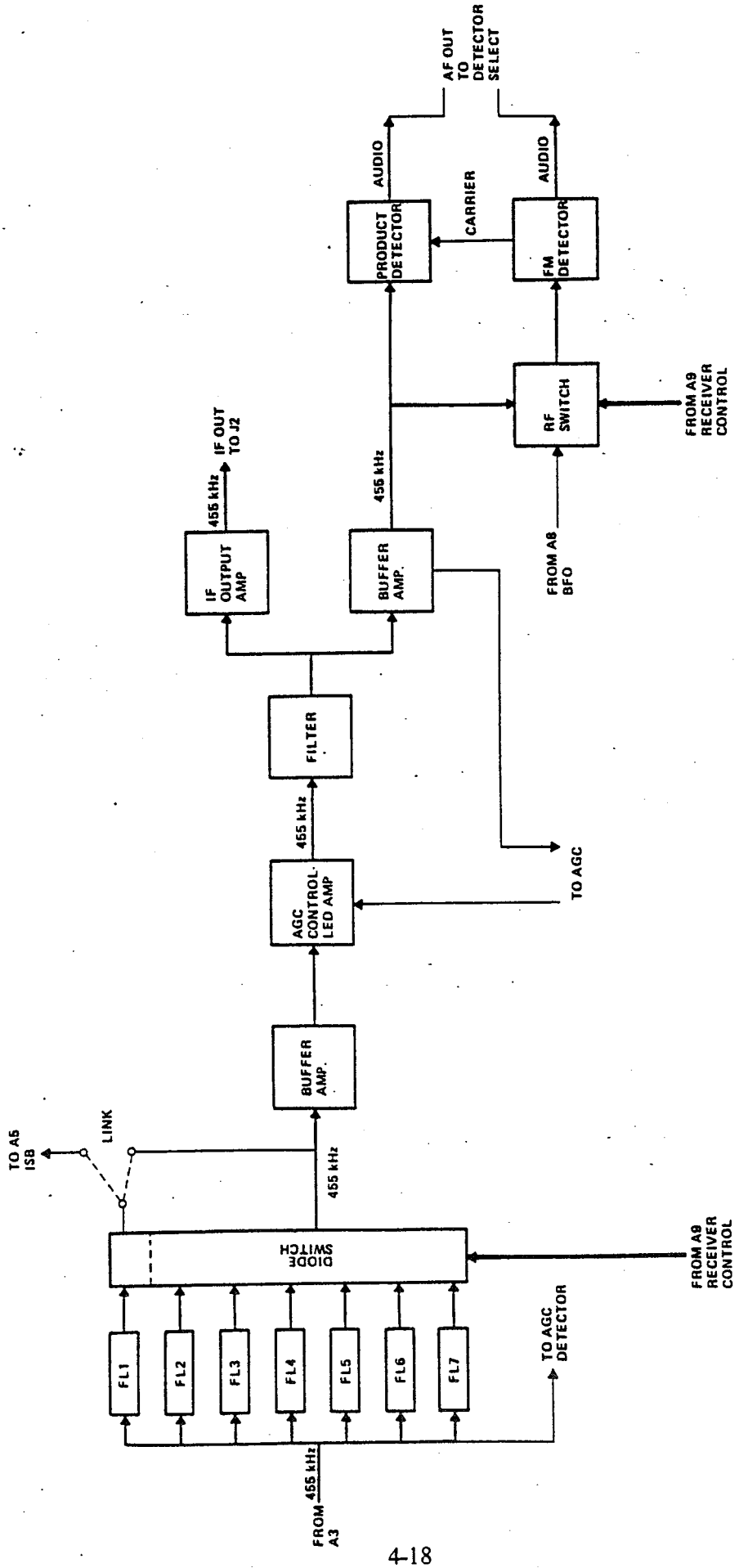


Figure 4-5. A4 IF Circuits, Functional Block Diagram

CR22-CR25 is (a diode switch) operated by Receiver control. Receiver control directs the switch to connect the IF signal to the detector in the AM and FM modes only. In all other modes of operation, the RF switch connects the BFO signal to the FM detector U18. The IF signal routed to the product detector is connected to its signal port. All signals applied to the FM detector; AM, FM or BFO are connected to a limiting amplifier which removes modulation from the AM carrier and passes it or BFO through the output carrier of the FM detector to the carrier input of the product detector. In the FM mode the signal is detected, its carrier rejected, and an audio signal, from the detector audio output, is connected to the detector select switch. This switch, an integrated circuit transistor gate U19A will select the detected FM audio, only in the FM mode, as directed by receiver control. In all modes except FM, a carrier frequency (AM or BFO) is applied to the carrier input of the product detector. In all modes of operation the signal selected, through receiver control, appears on the signal input of the detector. The detector removes the carrier and routes the audio, through its output, to the detector select switch U19A described above. Receiver control directs this switch to select that audio in all modes except FM.

4.3.4.2 AF Circuits

Figure 4-6 shows a functional block diagram of the audio circuits contained on circuit card assembly A4. This circuit consists of an audio lowpass filter stage, a crosspoint switch, two attenuators and two output amplifiers. The audio signal from detector select U19A is connected, through capacitor C85, to a lowpass filter and amplifier U28. The filter rejects any unwanted frequencies above the audio frequency that might have passed through the detector. The amplifier U28 operates in two different modes. In the AM and FM modes transistor switch U19B disconnects capacitor C113 from the circuit while in all other modes the capacitor is connected across R128 effectively shunting this resistor; thus reducing the signal level in these modes. The output of amplifier U28 is connected to an audio crosspoint switch U25. This switch, through Receiver control, controls audio switching from A4 circuits described above and from the optional A5 circuit card when installed. In non ISB modes the switch routes the A4 signal to the AF GAIN input and to variable attenuator U30. The signal through the AF GAIN control is coupled through capacitor C96 to an audio output amplifier U26. The output of this amplifier is coupled through C108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal through the AF GAIN control is coupled through capacitor C 108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal through variable attenuator U30 is routed to connector J8 for output to the ISB circuit card and is also routed back to the crosspoint switch. The switch, in this non ISB mode, connects the attenuated signal through capacitor C95 to a second audio output amplifier on integrated circuit U26. This amplifier drives transformer T1 through C107 and is coupled to the Monitor Line output on connector J3 on the rear panel. The variable attenuator is controlled through screwdriver adjust MAIN-LINE LEVEL located on the front panel and provides level control of the main (A4) audio signal to the Monitor Line output in the non ISB mode.

In the ISB mode either main (USB) or ISB (LSB) is selected and routed to the same circuits described in non ISB mode. In addition the crosspoint switch couples both the USB and LSB through variable attenuators to their respective amplifiers on the ISB circuit card. The USB is routed through attenuator U30 and controls the signal as described in non ISB mode. The LSB signal is routed through attenuator U31 to J8 and back to the crosspoint switch in the same manner as USB. Attenuator U31 is controlled through screwdriver adjust I-LSB LINE LEVEL located on the front panel and provides level control of the LSB (A5) audio signal. The LSB and USB are routed through connector J8 to their respective amplifiers on circuit card A5 and returns through circuit card A4 to Line 1 Output (USB) and Line 2 output (LSB) on AF OUT Connector J3 on the rear panel.

Two audio signals are routed to the AF metering circuit contained on circuit card A4. One signal is tapped from the AF GAIN control input and the second signal from the monitor output

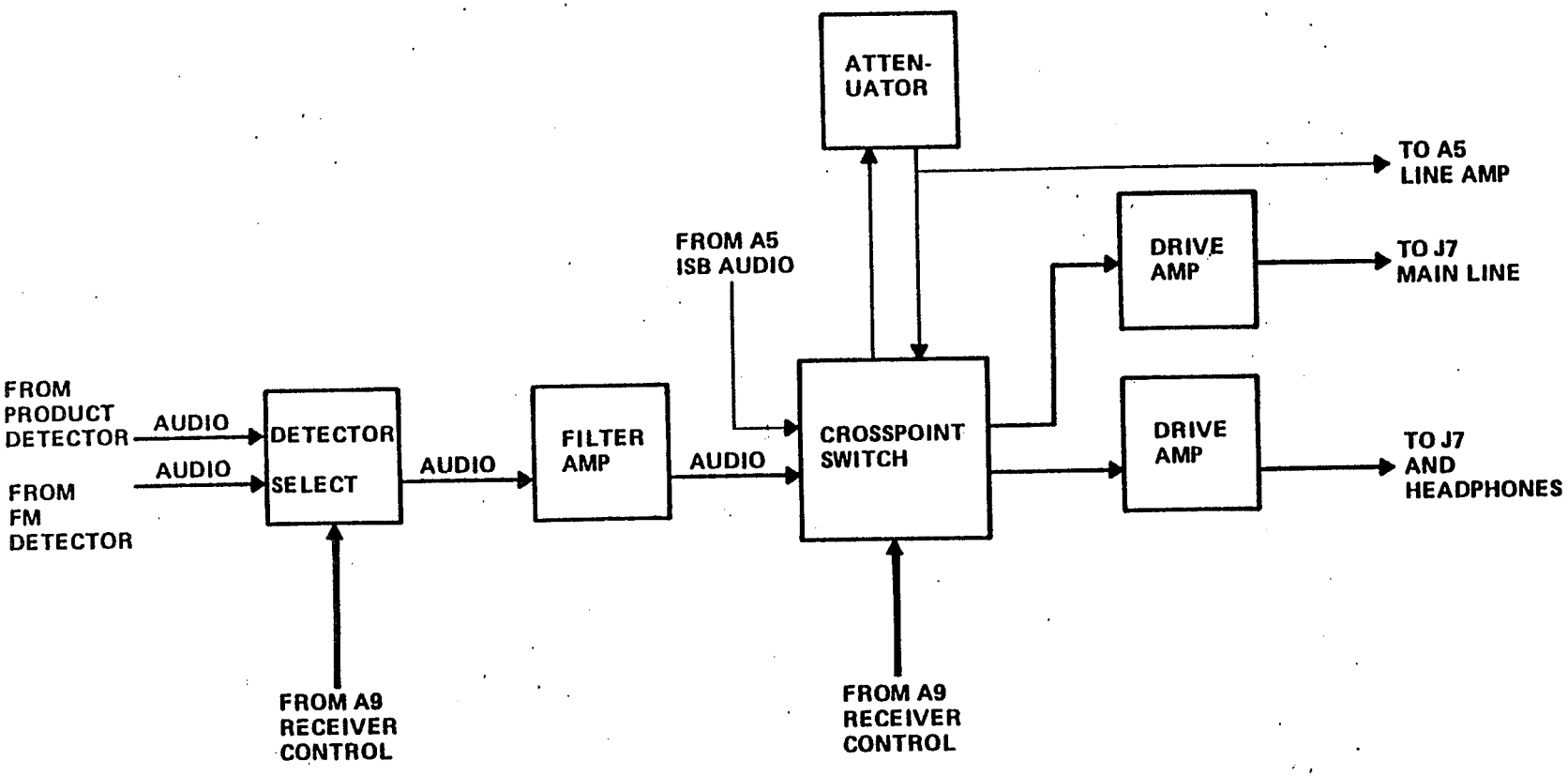


Figure 4-6. A4 AF Circuits Functional Block Diagram

amplifier. These two signals are connected to transistor gate U19C which selects between the two signals on direction from Receiver control. In all modes except BITE the signal from the monitor output amplifier is selected and routed to the AF metering circuit. This circuit is described under AGC circuits.

4.3.4.3 AGC Control Circuits

Figure 4-7 illustrates a functional block diagram of the AGC circuitry contained on circuit card assembly A4. The circuits consist of an AGC detector, AGC decay, peak signal detector, decay time constants, an integrator, filter, a gain control distribution amplifier, a digital to analog converter and various electronic switches controlled from receiver control circuits. The description also includes the AF/RF meter comparator circuit.

The AGC circuitry is designed to provide three modes or techniques for controlling the gain of the Receiver; Manual, Automatic and Automatic with a selectable threshold. In the automatic mode the level of the IF amplifier U8 is controlled automatically with three selectable decay times; SHORT, MEDIUM and LONG. In the manual mode the IF GAIN control is used to control the level of the AGC signal applied to the IF amplifier U8. The IF GAIN control is used to select the threshold in the automatic with selectable threshold mode. The same decay times as in automatic are selectable in this mode.

An IF signal taken from IF emitter follower Q6 is coupled through capacitor C31 to U10A for detection. The three transistor array U10 acts as a detector to the IF signal with U10C connected as an emitter for buffering the DC signal to two circuits; AGC decay and peak signal amplifier. Peak signal amplifier U7C couples the signal, across a decay time select circuit, to integrator amplifier U14A. The signal routed to the hang circuit which consists of amplifier U7A and U7B is time controlled through capacitor C42, resistors R45 and R146 and transistors Q2 and Q10. When short time decay is selected, Receiver control turns on transistor Q2 and transistor gate U12A. Capacitor C42 is shorted to ground through transistor Q2 which turns on transistor U10D and a short delay is asserted using combination resistors R52 and R55. When medium time decay is selected transistor Q10 and transistor gate U11Ais asserted. Capacitor C42 discharges through the parallel resistance of R45 and R146 providing a short hang time, after which U10 is turned on and a medium delay is asserted through R52 and R53. When long time decay is selected capacitor C42 discharges through R45 providing a long hang time, after which U10 is turned on, decay time is through R52.

The AGC applied to integrator amplifier U14A is mixed with signals from diversity AGC through amplifier U14B and gain control or threshold from amplifier U14C when AGC mode dictates. In the manual mode both transistor gates U11C and U12B are enabled through receiver control and the gain control voltage is asserted directly to the input of U14A. In the manual with automatic threshold mode U12B is turned off and the voltage from the IF GAIN control asserts itself through diode CR20 only when that level is higher than the AGC signal at the input of U14A. The digital to analog converter is coupled through U11D and is used to insert threshold level from a remote location through receiver control. Diversity AGC applied through transistor gate U11C to the input of U14C and to amplifier U14B influences the AGC signal only when its level is higher. When AGC dump is enabled (during certain BITE modes and local/remote operations that require dumping of AGC) receiver control enables flip-flop U9A which turns on transistor U10E. This rapidly discharges capacitor C52 thereby preventing U14A from acting as integrator.

The integrator amplifier is coupled to AGC filtering; consisting of capacitor C59, resistors R76, R77, R81 and R83, diode CR21 and amplifier U17A. If AGC dump is asserted (in certain BITE modes) transistor gate U12D is turned on providing a much faster charge patch for C59 through resistor R78. The output of the filter amplifier U17A is coupled to amplifier U17B. This amplifier provides the AGC signal to IF amplifier U8. At the same time U17B provides one input to A3 AGC drive amplifier U17D through diode CR26. If ISB is installed and enabled a second AGC signal

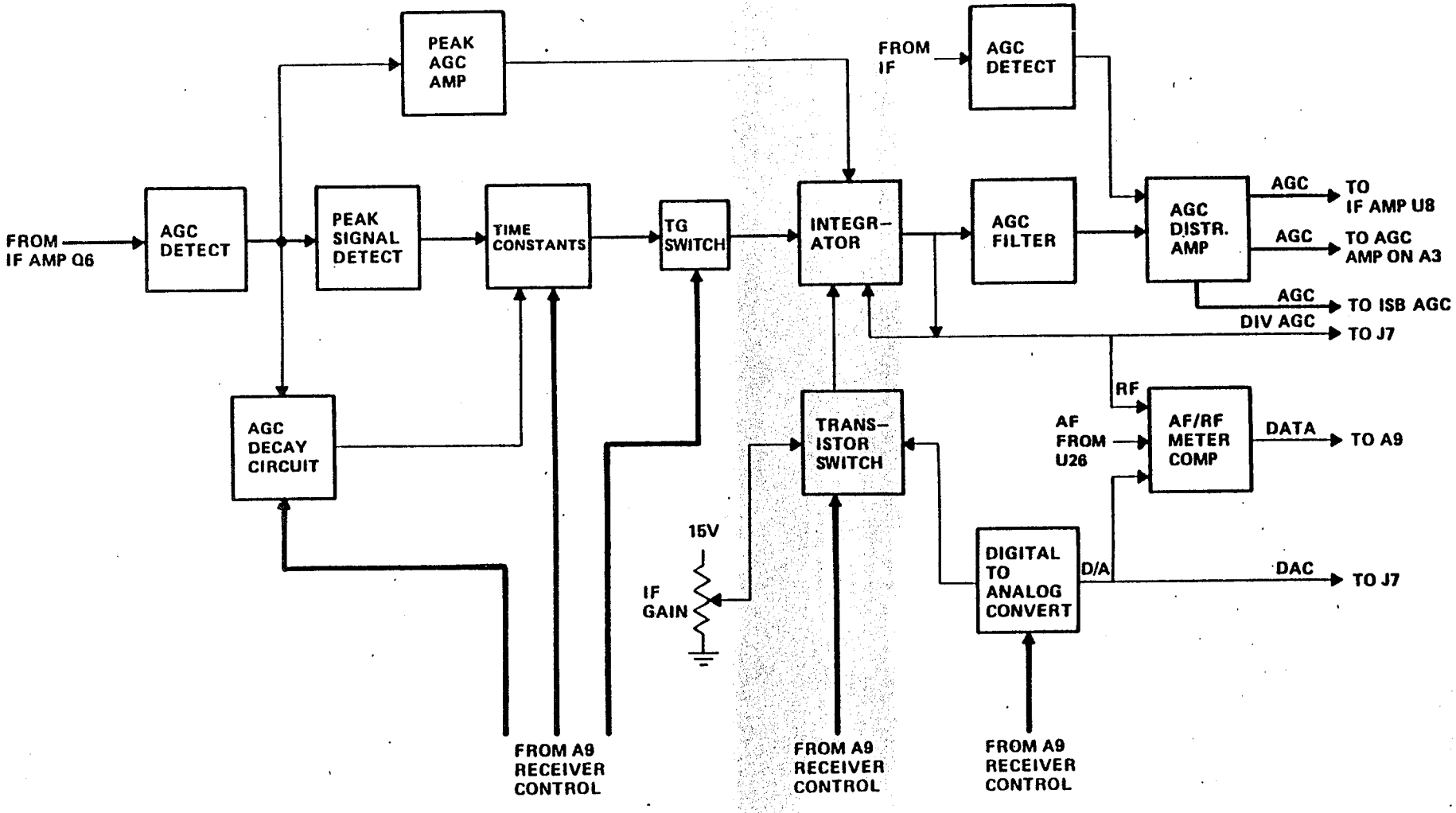


Figure 4-7. A4 AGC Circuits Functional Block Diagram

from that circuit card is coupled to U17D through diode CR27. The two diodes biases the strongest of the two signals to the input of U17D. The output of this amplifier is coupled through J2 to AGC circuits on circuit card assembly A3.

An AF/RF meter comparator circuit is contained on circuit card assembly A4. This circuit monitors the main RF, the ISB RF and the AF that may be input from either the main or the ISB signal. The circuits consist mainly of comparator amplifiers U24A (AF), U24B (ISB-RF) and U24C (main-RF). All three amplifiers operate in the same manner with their negative inputs accepting the AF or RF reference while the positive input is referenced from the digital to analog converter U21. The output of each amplifier is output through connector J2 to Receiver control. From this information the microprocessor adjusts the input to U21 which in turn adjusts the converter signal to the AGC in all modes except manual. The output of the three comparators are also processed to the front panel meter readout where the RF or AF signal level can be monitored.

4.3.5 Independent Sideband (ISB), A5

The Independent Sideband (ISB) circuit card assembly A5 contains IF circuits, AF circuits and AGC circuits. The description of these basic circuits are divided into those three basic functions and shown in two separate functional block diagrams in Figures 4-7 and 4-8. Input signals to the circuit card include; IF signal, BFO signal, AGC, and audio signals from A4. Output signals include; AGC and audio to A4, and AGC and audio to AF OUT-J3 on the rear panel, but through circuit card assembly A4. The ISB circuit card assembly schematic diagram is shown in Figure 7-5.

4.3.5.1 IF Circuits

Figure 4-8 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4 along with the AF function. This circuitry consists of a four stage IF amplifier, a BFO amplifier, a product detector, an audio amplifier, two audio line drive amplifiers, and AGC circuits. The IF signal is routed from bandpass filter FL1 by the filter selection switch, located on circuit card assembly A4 to the IF amplifier on A5. This filter is selected in the ISB mode of operation, so that an IF signal is routed to A5 only in that mode. The IF amplifier is identical to the one located on A4 and is described in Paragraph 4.3.4.1. The IF signal from the AGC controlled IF amplifier is routed both to the AGC circuits and to the signal input port of a product detector U11. A BFO signal from A4 is applied to the base of transistor Q7 through capacitor C30, amplified and applied to the carrier input port of the same detector. The detector removes the carrier and applies, through its audio output port, the audio signal, through capacitor C43, to an audio amplifier.

4.3.5.2 AF Circuits

Figure 4-8 shows a functional block diagram of the AF circuitry, along with the IF circuits, as they function on circuit card assembly A5. This circuitry consists of an audio amplifier and two audio line driver amplifiers. The audio signal, as received from the product detector, is connected, through capacitor C43 and resistors R78 and R79, to the base of emitter follower amplifier Q8. The output of this amplifier is then routed to circuit card assembly A4. Refer to 4.3.4.2 for a description of the ISB audio on A4. The attenuated audio signal is routed back to A5 and applied to the input of one line driver amplifier integrated in U12. The output of this amplifier drives transformer T2 with a center tapped 600 ohm output. This output is routed to AF OUT-J3 on the rear panel. The main audio signal from the A4 audio is connected to the second amplifier U12 and processed in the same manner as the ISB audio except through transformer T1.

4.3.5.3 AGC Circuits

Figure 4-7 shows a functional block diagram of the AGC circuits for circuit card assembly A4. These circuits are identical to ISB AGC circuits and are described in Paragraph 4.3.4.3.

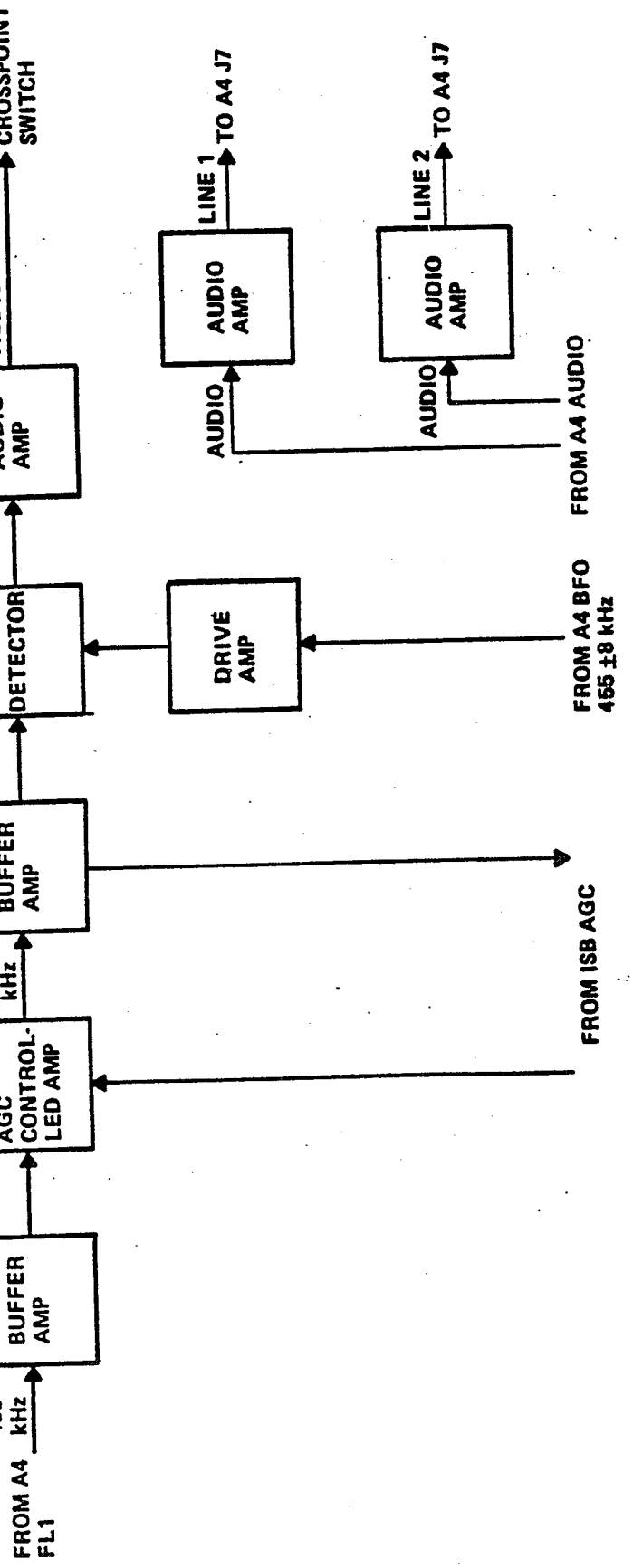


Figure 4-8. ISB Functional Block Diagram

4.3.6 First Local Oscillator Synthesizer, A7

The first local oscillator synthesizer circuit card assembly A7 contains circuits to produce the first oscillator frequency of 40.955 to 70.454999 MHz for the first mixer which in turn produces the first IF signal of 40.455 MHz. The description of this circuitry is divided into three basic groups; operation of phase lock loops, the digital control circuitry and the oscillator control circuitry. Figures 4-9 through 4-11 respectively, show simplified block diagrams of the three basic circuit divisions. Input signals to the circuit card assembly include receiver control and a 1 MHz reference frequency. The only output signal from the assembly is the 40.955 to 70.454999 MHz oscillator signal.

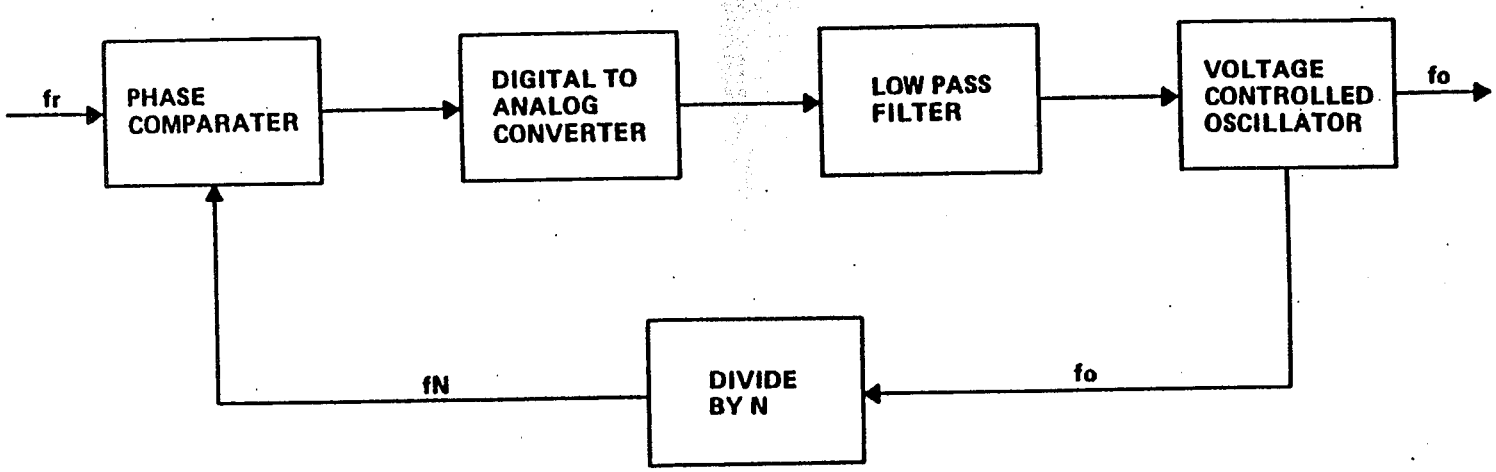
4.3.6.1 Operation of Phase Lock Loops

A basic phase lock loop consists of essentially four main blocks. These are shown in Figure 4-9 and are a Voltage Controlled Oscillator (VCO), a divider capable of dividing the output of the VCO by an integer number ($\div$N), a phase detector ($\emptyset$) and a Loop Filter Amplifier (LFA). A phase lock loop configured in this manner is capable of locking to the incoming reference frequency (F ref) and in discrete steps, each frequency step being the same as the incoming reference frequency (F ref). This is derived from the fundamental formula for this type of loop which is Fo = F ref x N; therefore, to vary the main VCO Frequency (Fo) either Freq or N would have to be changed. Most loops perform frequency change by modification of N, the integer divide ratio. It is noted, however, that this type of simple single loop can only vary in frequency steps as small as the reference frequency (F ref). However, it is assumed that a system is possible whereby the main oscillator (Fo) frequency can effectively divide a fractional number, then it is possible to achieve a much finer resolution given the same higher frequency reference. Assume that Fo is 50.123467 MHz and the reference frequency is 100 kHz, then using the above formula the result is with n as the ratio, a non-integer number: 50.123467 = 0.1 x n; therefore, n = 501.23467. If we split this number into its integer part and its decimal part, the result is a three decade integer and a five-decade decimal number. Generating the non-integer part as an actual frequency is done by considering a portion of the frequency spectrum of interest between 50.1 MHz and 50.2 MHz where this finally generated frequency will occur. Thus, it is possible to generate any signal between these two frequencies by an averaging technique, that is to say (see Figure 4-12) if the signal at 50.2 MHz is sampled, 23,467 times and the signal at 50.1 MHz, 76,533 (100,000-23,467) times then the average or apparent signal produced by this sampling would occur at the frequency of interest at 50.123467 MHz. This type of sampling produces a large number of sampling sidebands on the main output frequency. These can be removed, however, by producing a signal equal and opposite to these predictable sidebands and adding this to the oscillator control signal and effectively nullifying the production of these sidebands.

In the synthesizer used in the receiver the circuitry can be split into two; for the operating analysis, those circuits involved in the generation of the digital signals to control the generation of the 5-decade decimal part of the divide ratio number (n) which in turn controls the sampling technique and the signal to sum with the oscillator control signal, and those circuits including an oscillator, 3-decade integer divider, phase detector, summing amplifier and lowpass filter making up the components of a simple phase lock loop. These two parts in further discussions will be referred to as the Digital Control and the Oscillator Control circuitry. A separate section is included for auxiliary circuitry which is provided to produce large frequency step control and out-of-lock indications for the receiver.

4.3.6.2 Digital Control

Figure 4-10 illustrates a simplified block diagram of the digital control circuitry. The circuitry associated with the time control, the incoming 1 MHz reference signal from A7J2, is used as the clock for accumulator and registers through the NOR gate U4D which drives U20, U21 and



NOTE:
FOR NORMAL OPERATION
$f_o = f_r \times N$
WHERE:
f_o = OSCILLATOR FREQUENCY
f_r = REFERENCE FREQUENCY
N = DIVIDE BY NUMBER

Figure 4-9. Typical Phase Lock Loop Functional Block Diagram.

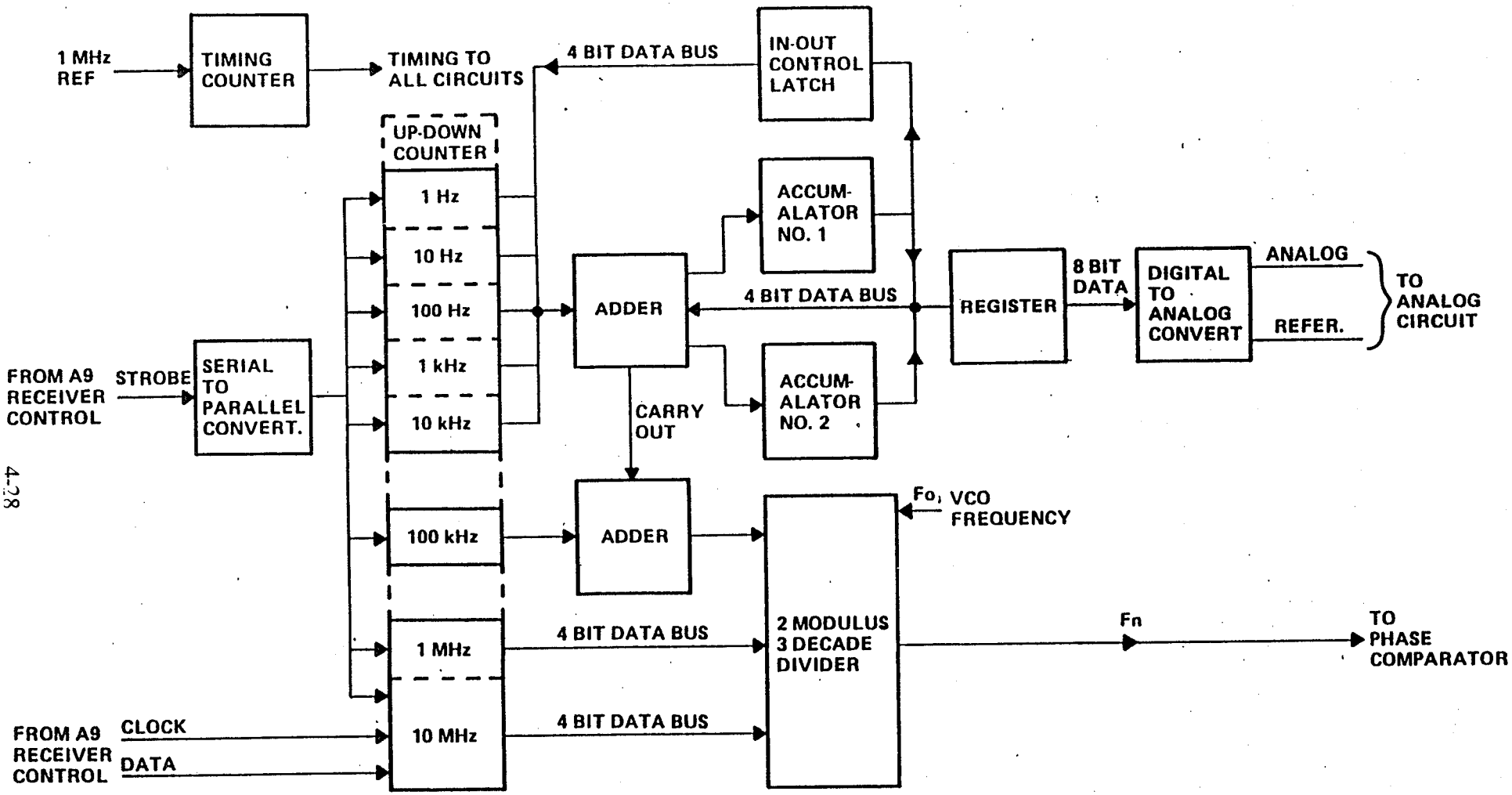
U22, and is routed directly to U3, U5 and U18. The Hex D flip-flops U3 and U5 with U1A and U1B provide a 10-level, ring counter. This counter is used to provide timed pulses to clock the accumulator from first accumulation to second accumulation and sequentially clock out the data in the latches U8 through U12 to the full adder U15. Flip-flop U3 provides a pulse 1 clock pulse wide but delayed 5 pulses from DØ the input, to Q1 the output. The output at U3Q4 is connected to the input DØ of U5. U5 also provides 1 clock pulse wide pulses but each output QØ through Q4 is used to drive the incoming data latches. U4A and U4B convert the narrow pulses from U3 QØ and U5 QØ into a 50% duty cycle square wave with a period of 10 clock pulses (each half cycle 5 clock pulses long). The 180° out-of-phase outputs at U4A pin 1 and U4B pin 4 provide control to U2, U22 and U19 to ensure that these devices are enabled during the correct half cycle. The 100 kHz reference for the reference side of the phase comparator is taken from U5 output Q4. U5 output QØ is provided to U4C via U7C to reclock the CARRY IN to U15 and also to U6 to provide the clock for alignment of signals out of the HEX D flip-flop U6.

In serial-to-parallel conversion, the incoming serial data stream from the A9 Receiver control assembly consists of DATA, CLOCK and STROBE signals. The strobe is routed to U6 input D1 where its output is reclocked. This output at U6 Q1 is fed back to D2 and its output Q2 provides a strobe input to U13 and U14 one clock pulse delayed. The incoming CLOCK is fed to U14 through U8 in parallel. The serial DATA is fed first into U14 which from its output on U14 pin 10 to U12 and U13 shift registers. The output from U12 at pin 10 is fed to U10 and U11, and so on to U9 and U8 to complete the data load and forming the serial-to-parallel conversion of synthesizer data into the data registers. The data registers U8 through U14 hold the data for the synthesizer frequency, the U8 register holding the 4-bit BCD data for the 1 Hz digit and each register the next decade so the U9 register holds the 10 Hz data and so on to the U14 register which holds the 1 MHz and 10 MHz data.

If the front panel RF frequency is set to 10.426800 MHz then the actual loaded data is 39.255 MHz above this frequency which is 49.680800. The first IF frequency is 40.455 MHz so we can see that a further offset of 1.2 MHz less than the main LO frequency of 50.881800 is introduced by the microcomputer into the serial data stream sent to A7. This is accounted for in the actual mathematical process in the first and second accumulator circuitry, which replaces this offset before generating the final VCO control voltage to the local oscillator.

With accumulator operation, the data loaded into the registers U8 through U12 is fed in 4 parallel boards under control of the ring counter U5 during the first half cycle of the tuning as discussed in the tuning section to the Full NBCD Adder U15. As the accumulation proceeds, the accumulating sum is passed from the sum outputs of U15 to the 4-bit wide latch U18. The Carry Out signal from U15 is also stored in U18 and is clocked out to U7A and then under control of U7C from the tuning circuits through U4C back into the Carry-In port of U15 deriving the first accumulation the outputs from U18 will be propagated through into the 4 stage shift registers contained in U20 and U21. U20 and U21 are 18 stage registers divided each into 2 four stage registers and 2 five stage registers. The four outputs from U18 are fed into the 4-stage registers in each half of each U20 and U21 and then the output of these 4-stage registers is fed back to the 5-stage register in each half of U20 and U21 At the end of the first accumulation the data at the output of the 4-stage register appears at the input to the tri-state 4-bit buffer U2A.

As the second accumulation begins U2A is enabled, under control of U4A, and the data at its inputs is transferred to the B inputs of U15 the NBCD Adder. During the five clock periods of the second accumulation the data in U20 and U21 is shifted back to the B inputs of U15. During this period, the data in U8 through U12 is held as the tri-state output enable of these registers is not enabled ensuring the results of the first accumulation is added again in the second accumulation. At the end of the second accumulation the results of the first accumulation will be propagated through the 5-stage register in each half of U20 and U21 and will appear at the inputs DØ through D3 of the



UK and US Patents have been applied for covering the synthesizer circuits described on this page. This information is subject to limited rights in technical data (DAR 7-109(A)).

Figure 4-10. First Local Oscillator Digital Circuits Functional Block Diagram

4 x 4 Multiport Register U22, and at the A1 through A8 inputs to U15. If no new data is loaded into U8 through U12 from the serial input data stream, then the two cycles of accumulation will continue; first accumulating the contents of U8 through U12 on one half cycle with the data at A1 through A8 in U15, and on the second half cycle adding the results from the first accumulation back into the B inputs of U15. Temporary storage for the results of each accumulation is provided by U18, U20 and U21.

If the result of adding numbers in U15 is a terminal count, the adder will produce a Carry-Out pulse at U15 pin 6 and reset to zero and start counting again. In a real situation this process is on going and the adder is continually providing Carry-Out pulses. (See Figure 4-12, line B.) This Carry-Out pulse is fed to U6 to be reclocked. The reclocked output at U6 pin 7 is routed through U1C to a further adder U17. The carry out is also clocked by U19A so that if it occurs on one edge of the accumulating half cycle controlled from U4B, it will appear at the Q output of U19A and after reclocking in U6 through the fifth latch it is applied to the carry input of the 4-bit full adder U17. (See Figure 4-12, line C.) The adder U17 continually updates,by addition, based on the carry out information from U15, the 100 kHz frequency information, provided by the input storage register U13. The addition in this adder is continuous so that the outputs at U17 pins 10 through 13 are constantly changing to provide the averaging action previously discussed.

For DAC control, a 4 x 4 multiport register U22 provides storage for the results of the constant accumulations and provides the information to the digital-to-analog converter U23. U19B divides the accumulator control signal by two so that all four registers in U22 can be loaded. The read cycles to these registers are controlled by the RØA, RØB, R1A and R1B inputs of U22. The RØA and RØB inputs are fixed and the R1A and R1B inputs are controlled by the output of U19B so that during two accumulations R1 is loaded, each register RØ and R1 consisting of two 4-bit data storage areas. The data stored is that which appears at the data inputs of U22, DØ through D3. This stored information is transferred to the register A outputs and register B outputs when W Enable is high and either WØ is high transferring RØA and RØB contents or W1 is high transferring the contents of R1A and R1B.

The digital-to-analog converter provides an output based on the changing data at its inputs as a voltage ramp whose amplitude and DC offset is modified by the adjustment of R5. The D/A also provides a reference source for the pulse to voltage converter U33.

NOTE

The pulses demonstrated in Figure 4-12 can be reproduced in circuit if the RF front panel frequency is set to 1.046000 MHz and the test points TP1 and TP2 temporarily shorted. This ensures that the accumulations start from a zero condition. B will then be at TP3, C at TP4 and E at U23, pin 2 (the D/A output).

4.3.6.3 Oscillator Control

Figure 4-11 presents a simplified block diagram of the oscillator control circuits. To more fully understand the operation, the following description is divided into four principal areas; 1) Main Division, 2) Phase Comparator and Pulse-to-Voltage Converter, 3) VCO and Analog Control Circuitry, and 4) Speed-Up and Out-of-Lock Operation:

1. Main Division. The BCD data outputs for 100 kHz, 1 MHz and 10 MHz provided by U17 and U14 are applied to a 2-modulus, 3-decade divider consisting of U27, U29, U30 and U31. This form of division ensures that by using a 2-modulus high speed control device U27 that can divide by 10 or 11 under control of its M1 and M2 input control can divide a high frequency input by an

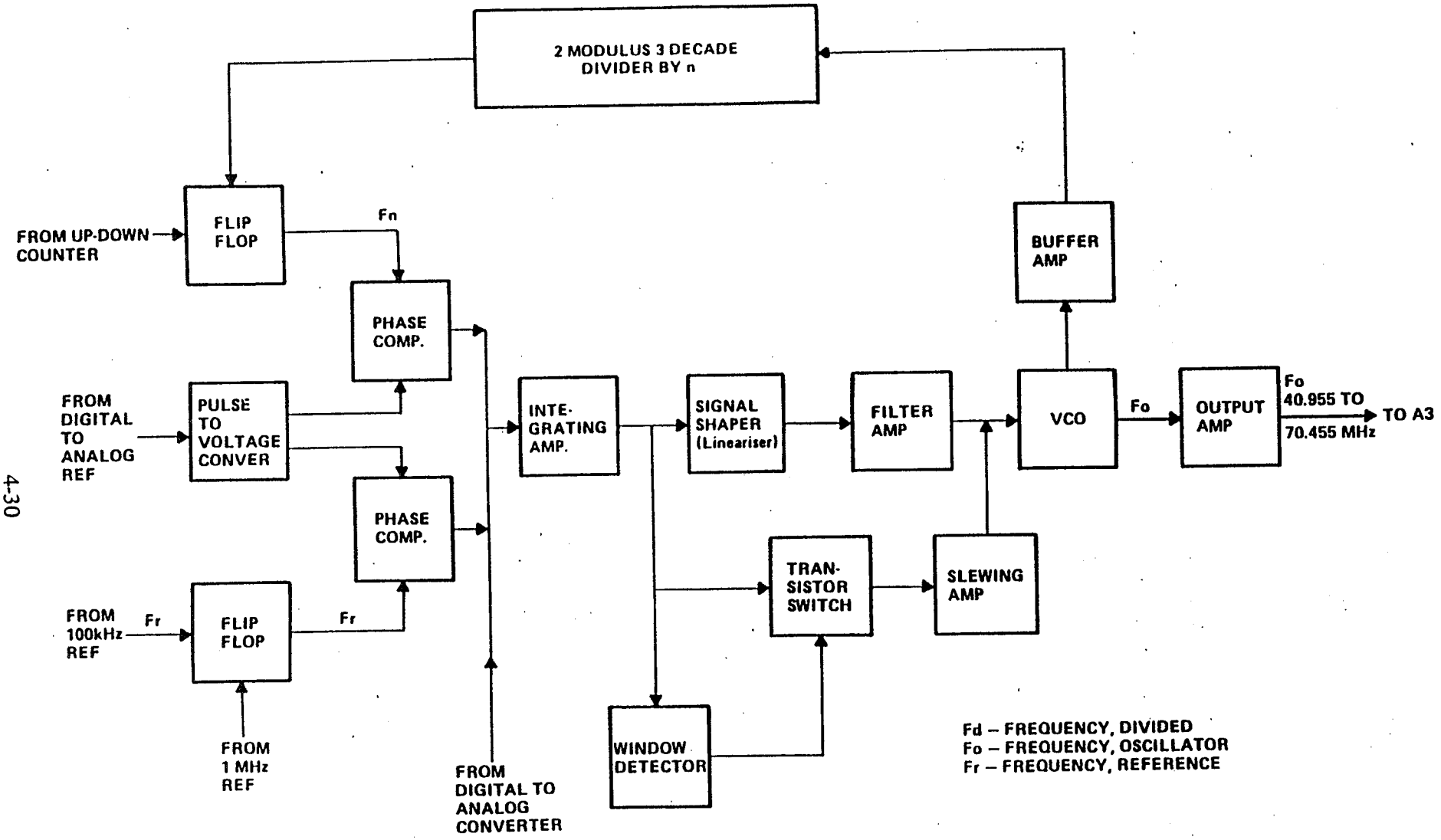


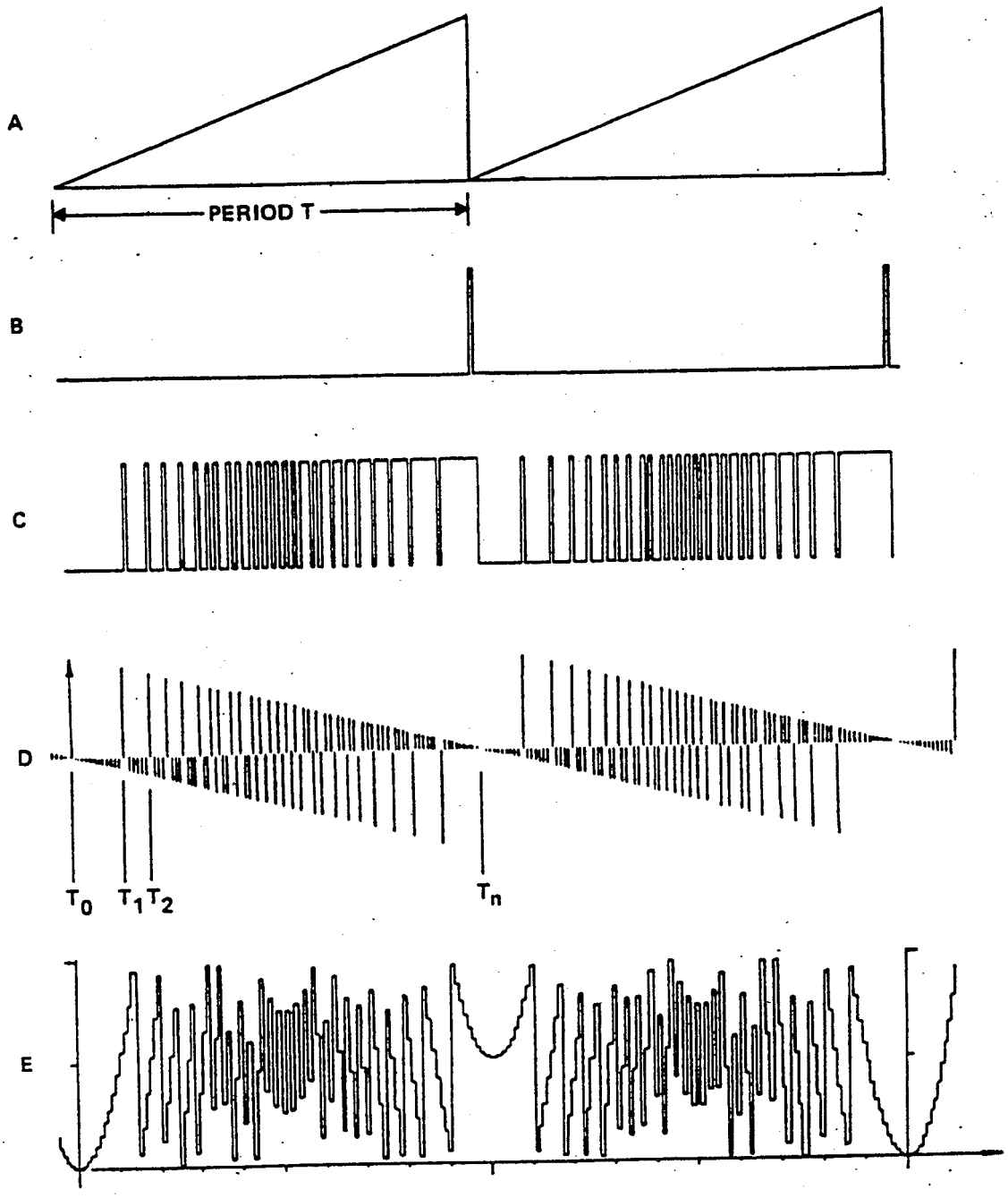
Figure 4-11. First Local Oscillator Analog Circuits Functional Block Diagram

integer value. The terminal count from U29 is applied inverted by Q5 to this control input of U27. The resultant divided signal at pin 9 of U29, U30 and U31 is applied to a TTL to ECL converter network consisting of R30, R31 and CR7 to a flip-flop U28A. This flip-flop reclocks the divided output under control of the clock signal on U28A pin 6 from the ECL output U27 pin 8, and then applied to one side of the phase comparator from its quadrature outputs on pins 2 and 3.

2. Phase Comparator and Pulse-to-Voltage Converter. The phase comparator reference is derived from the 100 kHz signal from U5 pin 12, reclocked against the 1 MHz reference in U26A. The reference output at U26A pin 2 is applied to the other side of the phase comparator consisting of U28B, U26B and U32. The ECL comparator provides phase comparator outputs at TP7 and TP8. The variable input from U28A pin is applied to a pulse-width detector consisting of CR9, CR10, Q6 and U33B. As the pulse width changes as the frequency varies from 40.455 MHz to 70.454999 MHz the voltage at the emitter of Q6 varies continuously and linearly over a range of approximately 1 volt. The DC offset of this voltage is determined by the D/A ref from U23. U33A and Q8 from one-half of a current source to CR12 and CR14 and Q7 and Q9 from the bottom half of this current drive through CR13 and CR15. Phase compared outputs at TP7 and TP8 are fed into the diode network formed by CR12, CR13, CR14 and CR15 and an output from this pulse-to-current converter is fed to R60.

3. VCO and Analog Control Circuitry. The current output of the phase comparator is combined with the voltage ramp from the D/A through C80. This combined signal is then applied to an integrating amplifier U35. In normal operation, the output of U35 is sent to a signal linearizing/ inverter circuit U37A and to the out-of-lock window detector comprising U34C and U34D. This is described in more detail in the speed-up and out-of-lock circuit operation. The output of U37A at TP10 is a DC voltage that can vary from a high voltage up to 18 volts and a low voltage equal to 1 volt, it will be high voltage when the selected frequency is at 30 MHz and low when the system requires 0.5 MHz. This DC voltage is then passed through U37B which along with its associated resistors and capacitors forms a low-pass filter. This output is then buffered from the VCO by 120K resistor R88 between TP11 and TP12. A further lead-lag network is then in the VCO control line between TP12 and ground formed by R92, R93, R94 and C98. This voltage is then applied to the VCO control varactors CR3 and CR4 through R85 and L4. A voltage applied to CR3 and CR4 will vary the capacitance across the main VCO coil L5 and thus vary the frequency generated. Q1 is the main LO active device and an output from its drain is capacitively coupled to a buffer amplifier of the cascade type formed by Q12 and Q13. The output of this feeds the 2-modulus divider controller U27. A further output from the oscillator coil is tapped off and provides the main LO output through Q2 and Q3 with step down transformer T1.

4. Speed-Up and Out-of-Lock Operation. When a large step of frequency is introduced on the front panel or from remote the window detector U34C and U34D comparators, compares the inputs on pins 9 and 10 from the VCO control circuitry with fixed high and low references on pins 11 and 8. If the voltage goes higher or lower (frequency step up or down) than these references a pulse will appear at the comparator outputs on pins 13 and 14. This pulse is applied through an RC network to a voltage converter consisting of U34B and CR19 and CR20. This voltage off set pulse is then used to drive three switches U36B, U36C and U36D. These switches by- pass the lowpass filter U37B and increase the integrating bandwidth of U35 and one switch, provides a feed forward from TP10 to the positive input of U40. U40 provides an integrated drive to push-pull drivers Q10 and Q11, the action of these drivers is to high-speed charge or discharge C98 through R91, C97 and R94. When the control voltage is at approximately the correct voltage for the frequency selected this circuit becomes operative. U34A provides the Out-of-Lock signal for feeding to the A9 Receiver control board and then to A6A2 for processing. If a pulse or a constant low level is applied to pin 6 of U34A then its output will go low indicating OOL.



UK and US Patents have been applied for covering the synthesizer circuits described on this page. This information is subject to limited rights in technical data (DAR 7-109(A)).

Figure 4-12. Detailed Timing Diagram

UK and US patents have been applied for covering the synthesizer circuits described on this page.

4.3.7 Second LO and BFO Generator A8

The second local oscillator and beat frequency oscillator circuit card assembly contains the circuitry for these two oscillators. An internal/external frequency reference circuit is also contained on this circuit card. The second local oscillator develops the fixed 40 MHz signals for the second mixer that in turn provides the 455 kHz second IF signal. The BFO is a variable oscillator that provides both the 455 kHz second IF signal and the basic 455 kHz beat frequency for sideband and CW modes of operation. The oscillator, through receiver control, may be either set at 455 kHz or varied plus or minus 8 kHz either side of its basic frequency for CW operation. The internal/external frequency reference circuit provides a reference frequency for both oscillators phase lock loops as well as the first LO contained on A7. In addition, the circuit includes an internal temperature controlled crystal oscillator which supplies a selectable 1 MHz, 5 MHz or 10 MHz reference frequency output at the rear panel. An external reference frequency can be used in place of the internal reference. The circuit description for the internal/external reference, the second LO and BFO are described under their respective headings with functional block diagrams shown in Figures 4-13 and 4-15. Schematic diagrams of these circuits are shown in Figure 7-10.

4.3.7.1 Internal/External Reference Frequency

The A8 circuit card contains circuitry that permits either an internal or external reference frequency. This reference frequency is required for the operation of all three oscillator synthesizers. A reference in/out connector and switch on the rear panel in addition to linkage on the A8 circuit card provide for the selection of either internal or external frequency and for selecting the proper divide by N frequency for the Phase Comparator.

4.3.7.2 Internal Mode

A 5 MHz crystal oscillator Y1, located on A8 is used as the internal reference frequency. With the rear panel REF INT/EXT switch in the INT position, the base of Q1 is grounded through R7 which turns voltage regulator U1 on. The voltage from this regulator enables the temperature controlled crystal oscillator. Approximately 30 minutes are required for maximum stability. The oscillator output is coupled through capacitor C5 to the base of transistor switch Q5. With the ground applied through the INT/EXT switch, the base of Q5 is held high through inverter U2A and diode CR3 while the base of transistor switch Q4 is held low through diode CR2. Transistor Q5 conducts, transferring the 5 MHz signal through a TTL square wave shaper Q6 to one clock input of the phase comparator. See 4.3.7.4, item 3. The 20 MHz voltage controlled oscillator, described in 4.3.7.4, item 2, is stabilized through the use of this reference frequency. The 20 MHz output of the oscillator is divided by three dividers (two $\div 2$, U7B + U7A and a $\div 10$, U6). The two dividers ($\div 2$) are contained in a single dual D flip-flop. The clock signal (20 MHz) is applied to the clock input of U7A. With the Q output connected to the D input, the Q output provides the 10 MHz reference. The 10 MHz is also connected to the clock input of the second flip-flop and to the divide by 10 circuit. The second flip-flops Q output provides the 5 MHz reference signal. The divide by 10 circuit is a two stage divider ($\div 2$ and $\div 5$). The 10 MHz drives the clock input for the divide by 5 at B input pin 1. The output of this divider (QD pin 11) is connected back to the clock of the second divider ($\div 2$) at A input pin 14. Dividing by 5 first then by 2 provides a more symmetrical 1 MHz reference. The 1 MHz signal is output from the divider ($\div 2$) at QA output pin 12. The 1 MHz, 5 MHz and 10 MHz frequencies derived from these dividers are available for reference through data select switches U4 and U5. The 1 MHz reference is routed directly to the BFO synthesizer and to the first local oscillator synthesizer through NAND gate U11C and connector J2. One of the three frequencies will be selected by data select U5 and routed to rear panel connector J7. Either one of the three frequencies may be selected by proper connection of links LK1 and LK2. In this internal mode, data select C of both U4 and U5 is held low through the INT/EXT switch. Linking LK1 makes data

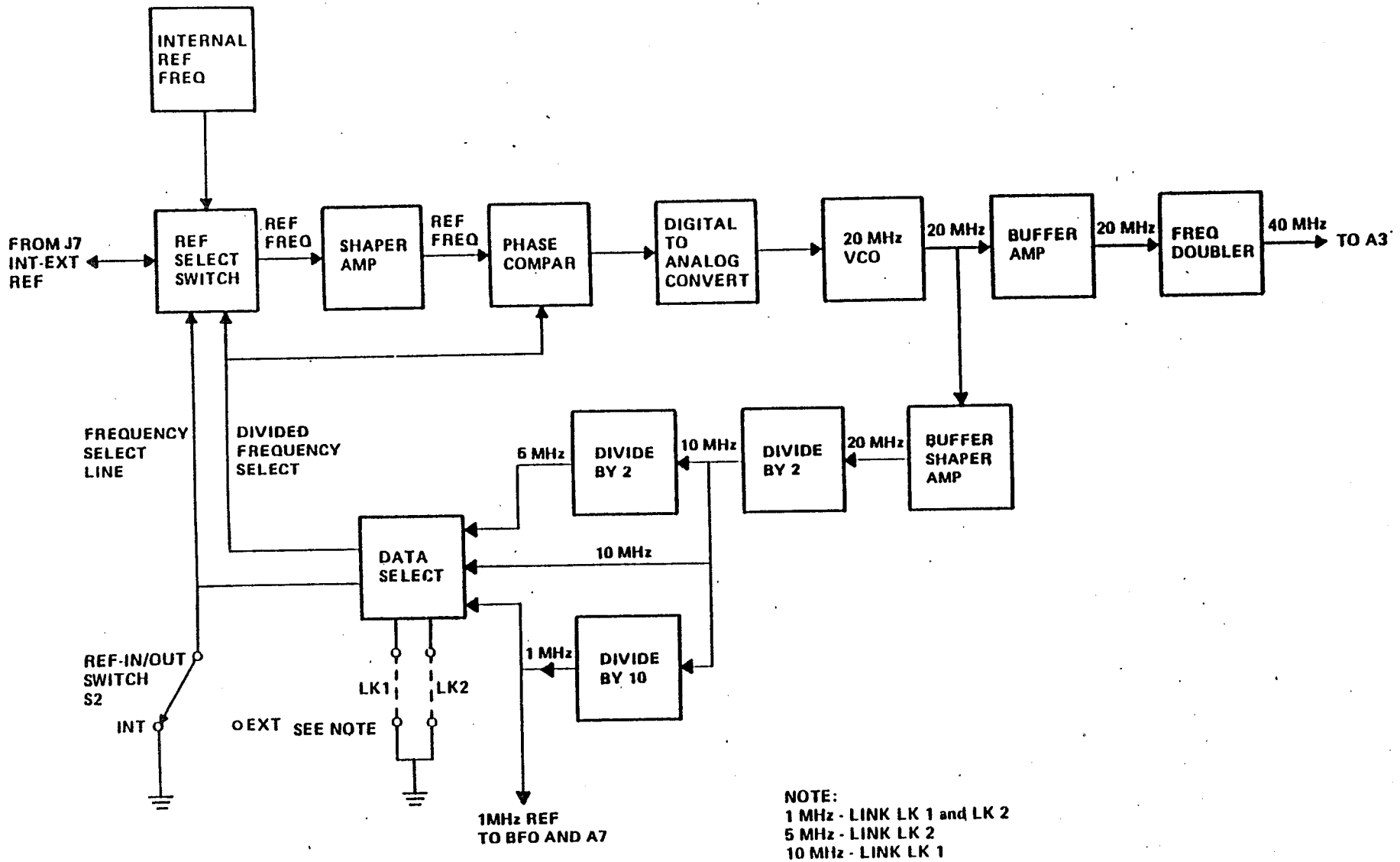


Figure 4-13. Second Local Oscillator Fun nal Block Diagram

select A low which outputs D0 input of both U4 and U5 to their respective Y outputs. For U4 this is 5 MHz, for U5 it is 1 MHz. When only LK2 is linked data select A will be high and B low which connects both D1 inputs to their respective Y outputs (U4-5 MHz, U5-5 MHz). When both LK1 and LK2 is linked both data select A and B are held low which outputs D3 of both U4 and U5 (U4-5 MHz, U5-10MHz). As noted in this internal mode, U4 always selects the 5 MHz. It is then routed to the phase comparator as the oscillator reference signal. The output frequency selected by U5 is routed through resistor R13 to buffer amplifier stages Q3 and Q2. These stages provide for output into 50 ohms through a high pass filter, L1, C6 and C7, and connector J7 on the rear panel. The high pass filter also provides filtering for reference frequencies applied externally through J7 while resistors R8 and R9 provide a 50 ohm impedance to the incoming reference frequency.

4.3.7.3 External Mode

In this mode of operation the INT/EXT switch is set to EXT and this line goes high from the +5 volts through resistor R78. This causes transistor Q1 to turn voltage regulator U1 off which in turn turns off the internal crystal oscillator Y1. When an external oscillator is connected to connector J7 on the rear panel, the input is routed through the high pass filter, and capacitor C8 to the base of transistor switch Q4. The input of NOR gate U2A is now high which in turn keeps the base of Q5 low through diode CR3. Transistor Q4, whose base is no longer low, conducts which applies the external reference through the TTL shaper to the same clock input of the phase comparator that the 5 MHz reference was applied in the internal mode. The appropriate reference frequency for application to the second clock input to the phase comparator can be selected through LK1 and LK2 as in the internal mode; however, data select C is now high. Linking LK1 selects D6 (10 MHz), LK2 selects D5 (5 MHz) or both LK1 and LK2 select D4 (1 MHz). The D0, D1, and D2 inputs to U5 cannot be selected when data select C is high (external mode) and no output appears on the Y output of U5.

4.3.7.4 Second Local Oscillator

Figure 4-13 shows a simplified functional block diagram of the second local oscillator. The circuit consists mainly of a crystal referenced, voltage controlled oscillator, a frequency doubler output circuit and a phase lock loop includes amplifiers, an ECL to TTL buffer, three frequency dividers (two $\div 2$ and a $\div 10$), reference frequency select circuit, a phase comparator and a digital to analog converter. The three dividers are used to provide a choice of reference frequencies for internal or external reference.

1. Phase Lock Loop. The 20 MHz oscillator frequency is kept on frequency through a phase locked loop (See Figure 4-9). The oscillator output is routed through a divide by N circuit that provides an oscillator reference frequency. This divided oscillator frequency is coupled to the second clock input of a phase comparator. The phase comparator, described below, detects any phase shift between the oscillator frequency and a reference frequency also connected to the phase comparator. The phase comparator then changes the digital to analog converter output voltage which is connected to the oscillator varactor and crystal. This then causes the oscillator frequency to change. This loop action will continue until the oscillator frequency is brought into phase (same frequency) with the reference frequency.

2. Voltage Controlled Oscillator. The 20 MHz oscillator consists of ECL OR gate U22D, 20 MHz crystal Y2, varactor CR4, resistors R47, R48, R49 and R50 and capacitors C34 through C38. Oscillation frequency is derived from the parallel combination of crystal Y2 in series with C37 and with varactor CR4 in series with C34. The dc voltage applied at the junction of CR4 and Y2 controls the reactance of the parallel circuit, mainly through CR4. This dc voltage, controlled

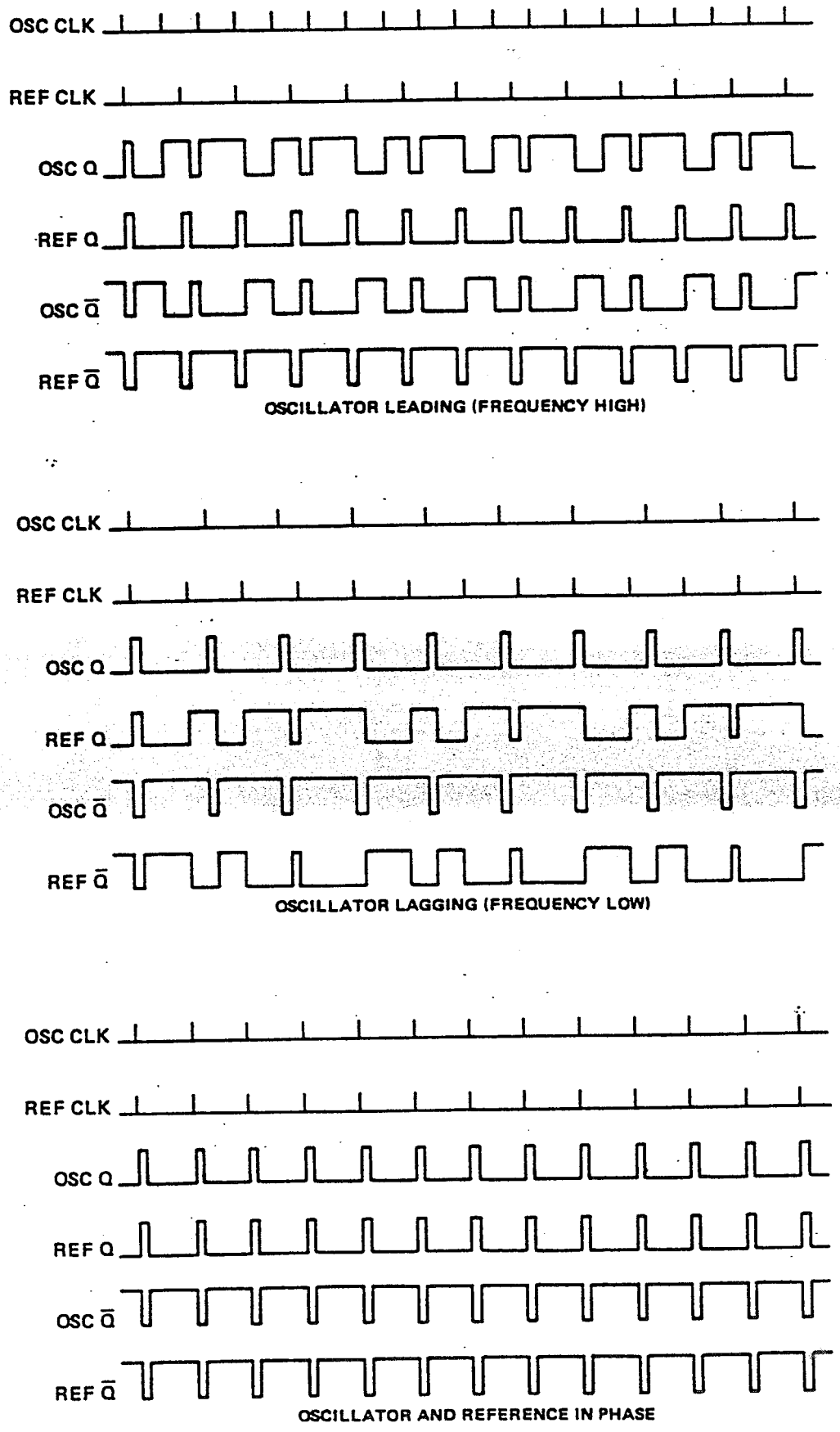


Figure 4-14. Waveform Diagram: Phase Comparator

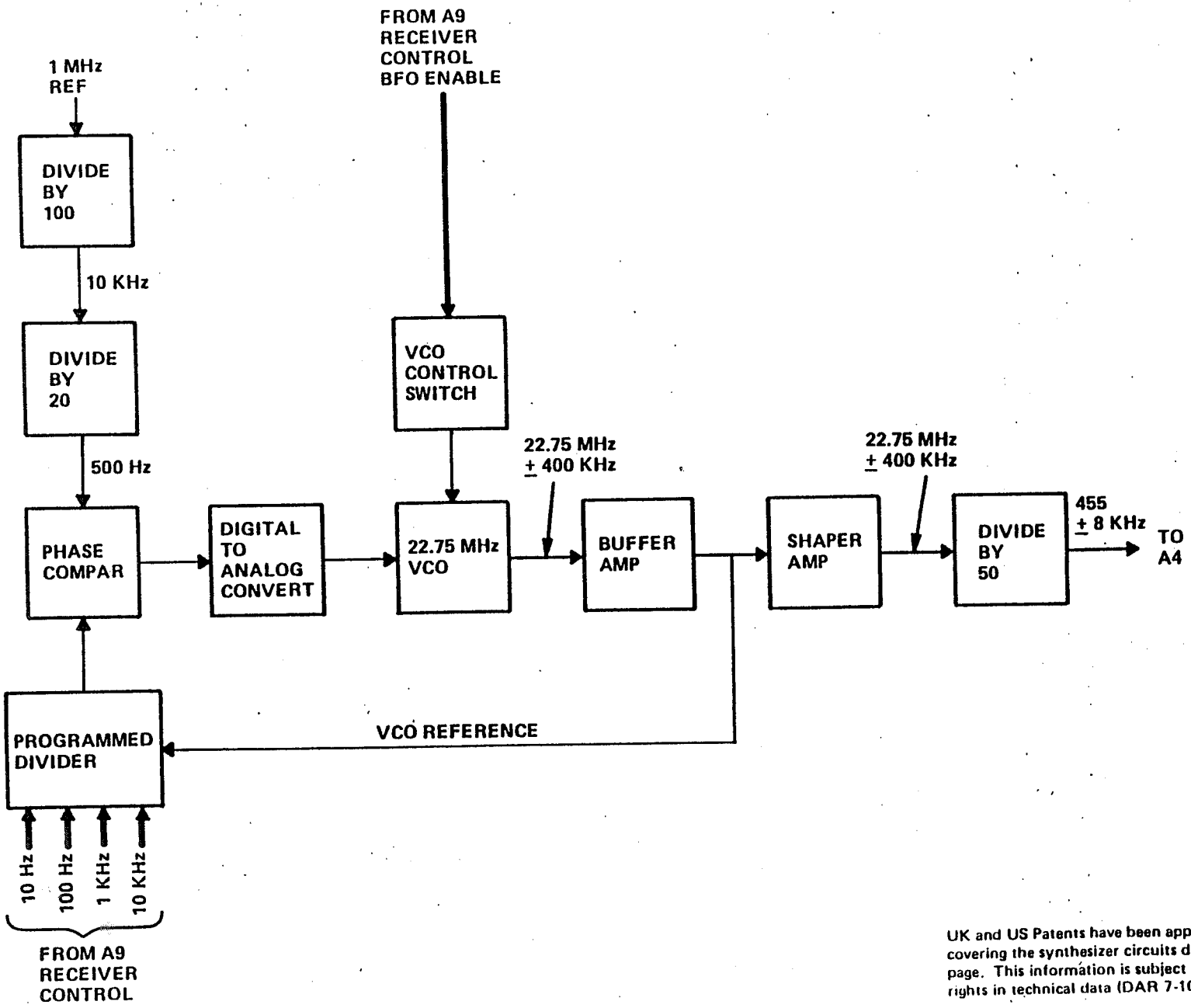
through the phase lock loop described in Paragraph (1) compensates for any frequency shift of the oscillator. The oscillator output is coupled to two buffer amplifiers U22A and U22B. Buffer U22A is used to drive a TTL shaper buffer amplifier, Q10, which shapes the oscillator output into a square wave for input to the divider. These circuits are described in Paragraph a. Buffer U22B drives a frequency doubler circuit, Q11, and associated components. This tuned circuit selects the 40 MHz component of the signal and outputs it through J3 to circuit card A3 as the second oscillator frequency.

3. Phase Comparator and Digital to Analog Converter. The phase comparator is used to detect the phase shift between the reference frequency and the oscillator frequency and to apply control to the digital to analog converter in relation to that phase shift. The comparator consists of dual flip-flop U3A and U3B and NAND gate U2B. Flip-flop U3A is clocked from the reference frequency while U3B is clocked from the divided oscillator frequency. The D inputs to both flip-flops are held high through the +5 volts. When both Q outputs are high the output of NAND gate U2B goes low, resetting both flip-flops with a delay through R32 and C20. Thus when the positive edge of a clock signal clocks a flip-flop, Q goes high while $\overline{Q}$ goes low. If the two clock signals to the flip-flops are in phase, the $\overline{Q}$ outputs then will go high from the reset action through NAND gate U2B, initiated from the leading edge of both clock pulses. The $\overline{Q}$ outputs will remain high through the on-off period of that particular clock pulse. Except for a small delay time introduced by the flip-flops the $\overline{Q}$ outputs will be high most of the time when the two clock signals are in phase. (See Figure 4-14). When the oscillator frequency leads the reference signal (frequency high), the $\overline{Q}$ output of U3B remains on less than the $\overline{Q}$ output of U3A because the leading pulse sets back to Q on U3B before the lagging pulse of the reference signal sets back to Q on U3A. The reverse of this is true when the oscillator frequency lags the reference signal (frequency low). The two $\overline{Q}$ outputs of the phase comparator are coupled to a digital to analog converter which consists of transistors Q7, Q8 and Q9, resistors R33 through R39 and capacitors C24 through C26. The $\overline{Q}$ output of reference flip-flop U3A is connected to the emitter of Q7 through R33 while the $\overline{Q}$ output of the oscillator flip-flop U3B is connected to the emitter of Q9 through R34. When the oscillator and reference signal are in phase, the two outputs are the same and transistors Q7 and Q9 conduct at a rate dependent on the amplitude and time period of the pulse. With the amplitude always constant, the amount of conduction then depends only on the time period. When the pulse goes high, the emitters of Q7 and Q9 go more positive causing them to conduct less and when the pulse goes low, they conduct more. The voltage output at the common collectors of Q8 and Q9 would tend to follow this rise and fall in the pulse; however, the inverted signal at the base of Q8 also causes it to conduct less when the pulse is high and more when the pulse goes low. This action converts the pulse signals into a dc level sawtooth waveform at the Q8-Q9 common collectors. The low pass filter, C25, C26 and R39 smooths this waveform and dampens sudden changes caused from changes in the phase comparator pulse rates and in turn stabilizes the phase lock loop. When oscillator frequency increases, the pulse rate increases, the pulse rate increases at Q7 and decreases at Q9, causing a reduction of the dc level output. When oscillator frequency decreases the reverse action takes place. This analog dc output is coupled through R47 to the oscillator for frequency control.

4. Out of Lock Detector. The out of lock (OOL) detector consists of NAND gate U2C, resistors R43 and R44 and capacitors C29 and C31. The NAND gate output is held low (phase loop in lock) by the $\overline{Q}$ outputs of the phase comparator. The resistor capacitor combinations R43-C29 and R44-C31 integrate the square wave signal to provide a constant high on the two NAND gate inputs. If either or both of the two $\overline{Q}$ outputs from the phase comparator remains low the output of the NAND gate will go high. The OOL output from this circuit is routed to A9 front panel control for processing.

4.3.7.5 Beat Frequency Oscillator (BFO)

Figure 4-15 is a simplified block diagram of the beat frequency oscillator. This circuit provides the variable 455 kHz BFO for receiver CW and sideband operation. The BFO is varied plus



UK and US Patents have been applied for covering the synthesizer circuits described on this page. This information is subject to limited rights in technical data (DAR 7-109(A)).

Figure 4-15. BFO Functional Block Diagram

or minus 8 kHz through receiver control. The oscillator operates in a phase locked loop which consists of a voltage controlled oscillator (VCO), a buffer amplifier, a programmed divider, a phase comparator and a digital to analog converter. A divide by 2000 circuit is included to provide a 500 Hz reference signal for the phase comparator. The VCO operates at a center frequency of 22.75 MHz which is 50 times the BFO center frequency of 455 kHz. The oscillator output is routed through a buffer amplifier, TTL shaper, divide by 50 circuit and filter to provide the 455 kHz BFO to the A4 circuit card. An out of lock (OOL) circuit is also included to detect any out of lock condition of the phase lock loop.

1. Phase Lock Loop. The phase lock loop for the BFO oscillator functions in the same way as the circuit described for the second local oscillator except the divide by N is made variable through BFO input data to the divide by N circuit.

2. Voltage Controlled Oscillator. The VCO consists of field effect transistor Q18 opto isolator U21, coils L4 and L5, resistors R66 and R67, capacitors C52 through C56 and C59 and varactors CR6 and CR7. The capacitive reactance of the two varactors in conjunctions with L4 determines the frequency at which the circuit will oscillate. Since varactors change capacitance in relation to the level of the dc voltage applied, the frequency of the oscillator is controlled from the output of the digital to analog converter that is applied to varactors CR6 and CR7 through coil L3. Opto isolator U21, connected to the source of Q18 through resistor R67, provides for on-off control of the oscillator by isolated control of the oscillator source bias. When BFO is enabled in the CW and sideband modes, U21 is enabled through pin 2 which in turn completes the bias path for Q18 through R67. The output of the oscillator is coupled through capacitor C57 to the gate of field effect transistor Q19 which acts as a buffer amplifier between the oscillator and two output circuits. One output of the buffer amplifier provides the oscillator reference frequency through capacitor C72 to the programmed dividers. This circuit is described in Paragraph 3. The second output is coupled through capacitor C60 to a shaper circuit, Q20, R72, R73, R74 and C61. This circuit shapes the waveform into a square-wave for the TTL logic of the divide by circuit U20. The dual decade counter U20 is externally strapped to provide a division of 50 on its QD output, pin 9. The variable 22.35 to 23.15 MHz oscillator signal is reduced in frequency by the division of 50 which provides the 447 to 463 kHz BFO. This output is filtered through the filter network consisting of C63, C64, C65, L6, R75, R76 and R77. This filter shapes the digital waveform from U20 into an approximate sine wave signal before being routed to circuit card A4 through connector J4.

3. Programmed Dividers. The programmed dividers determine the divide by N number by which the oscillator frequency will be divided for a variable reference to the phase comparator. The program dividers consist of presettable BCD decade counters U14 through U18, divide by 10 or 11 2-modulus controller U19, NOR gates U12A through U12D and AND gates U13A through U13C. The program divider has two reference inputs; the oscillator frequency coupled through C72 to the V reference and clock inputs of U19 at pins 15 and 16 and the BFO data control inputs to U15 through U18. It is the BFO data inputs in conjunction with U19 that sets the divide by N number for dividing the VCO frequency. To divide the 22.75 MHz to 500 Hz, for the second clock input to the phase comparator, would require a division of 45500. The five decade counters are externally strapped to count down from a maximum count of 100000 (99999 + 1). The actual data then that would be set on the BFO inputs would be 100000 – 45500 = 54500; however due to gating restrictions between the decade counters the actual number set at the BCD inputs is 54509 at center frequency (455 kHz). The BFO is adjustable plus or minus 8 kHz so that the swing in the BCD inputs must be from 53709 (54509 – 800) to 55309 (54509 + 800) with 54509 as center. At center frequency counter U18 receives the 10 Hz BCD digits on its parallel inputs P0 through P3 with P0 and P3 ($2^0 + 2^4 = 9$) high. Counter U17 receives the 100 Hz digits with all input low (0), U16 receives the 1 kHz digits with P0 and P2 ($2^0 + 2^2 = 5$) high, and U15 receives the 10 kHz digits with only P2 ($2^2 = 4$) high. Counter U14 is strapped P0 and P2 ($2^0 + 2^2 = 5$) to the +5 volts (high)

and P1 and P3 to ground (low). This supplies the 100 kHz digit which is always 5. Counter U15 receives only the 2^0, 2^1 and 2^2 BCD digits since the 10 kHz swing is never greater than 7. The counter is a two modulus divide by 10 or 11 controller and will divide by 10 or 11 for different periods in the clock signal. The TC output of U18 coupled to the M1-M2 inputs of U19 determine the periods at which it will divide with either 10 or 11. NOR gate U12C ensures that the count enable input of U18 goes low when TC goes high. This assures that the TC output will be retained long enough for action on the M1-M2 inputs of U19. The QTTL output (pin 11) is used to clock the decade counters U14 through U18 and as a reclocking source for NOR gate U12A. Four control inputs, parallel enable (PE), count enable parallel (CEP), count enable trickle (CET) and reset (R) select the counters mode of operation. The R and CET of all counters is held high through the +5 volts connected to all counter CET and R inputs. The CEP input of counter U17 (100 Hz) is also held high from the same +5 volts since this counter does not receive a carry out from previous counters. The CEP of counter U16 is high only when the TC output of U17 is high, the CEP of U15 is high only when the TC output of both C16 and C17 through AND gate U13A are high and the CEP input of U14 is high only when the TC output of both U15 and U16 through AND gate U13B are high. This AND gating of the TC outputs help prevent extra pulses from occurring that are caused from delays in the counters. The PE of all counters are alternately low and high as the TC output to inverter U12B is alternately high and low. With the R and CET of all counters held high (counter resets when R is low) the count mode is enabled when CEP and PE goes high. When PE goes low the counters will synchronously load the data from the BFO inputs into the counters with the count occurring each 500 Hz. The counters output on TC only when PE is held high; however when CEP is held low the TC output will be retained until the next clock pulse. The TC output of the programmed dividers is connected to one input of a two input NOR gate U12A. The clock signal is connected to the second input so that any unwanted pulses, created by delay in the counters and not in sequence with the clock pulse will be rejected. The output of U12A is routed through inverter U12D to one clock input of the phase comparator as the oscillator reference frequency.

4. Reference Frequency. The 1 MHz reference frequency supplied from internal/external reference circuits is divided by 2000 to provide a 500 Hz reference frequency to the phase comparator. This division of 2000 is accomplished with two dual decade counters U8 and U9. Counter U8 provides a division by 100 while counter U9 provides division by 20. Each counter has two divide by 2 circuits and two divide by 5 circuits and are externally strapped to provide the divisions by 100 and 20. The division by 100 is accomplished by using all four dividers in the order shown ($\div 2$ = 500 kHz. $\div 5$ = 100 kHz, $\div 5$ = 20 kHz and $\div 2$ = 10 kHz). The divide by 20 is accomplished in the same manner except its input is the 10 kHz output of the $\div 100$ and the second $\div 5$ is bypassed ($\div 2$ = 5 kHz, $\div 5$ = 1 kHz, and $\div 2$ = 500 Hz). The resultant 500 Hz output is coupled to the clock input of D flip-flop U10A. This flip-flop is contained in a dual flip-flop package which together with NOR gate U11A make up the phase comparator.

5. Phase Comparator and Digital to Analog Converter. As described previously, the 500 Hz reference frequency is connected to flip-flop U10A. The second flip-flop U10B receives its clock signal from the programmed dividers. The D inputs of both flip-flops are tied to the +5 volts (logic 1) while both Q outputs are connected through 2 input AND gate U11A and resistor R83 to the reset of both flip-flops. Both flip-flops will reset each time that both Q's go high, causing a logic 0 at the resets of both flip-flops. The clock input signal to U10A (reference) consists of positive going pulses while the signal from the programmed divider (oscillator reference) also contains positive going pulses and is connected to the clock input of U10B. Each flip-flop triggers Q on (high) the positive going pulse of its respective clock signal and at the same time triggers $\overline{Q}$ to zero (low). Previously as described, when both Q outputs are high the output from AND gate U11A is low clearing both flip-flops through R83. This resets the Q outputs to low and the $\overline{Q}$ outputs to high. Refer to Figure 4-14. The two $\overline{Q}$ outputs are connected to the digital to analog converter which consists of transistors Q15, Q16 and Q17 and their associated components. This circuit operates in the same manner as the digital to analog converter

described in Paragraph b (3) except that adjustments in the BFO frequency provide a different setting of the dc control voltage. This causes the VCO to change frequency in relation to the BFO setting.

6. Out of Lock Detector. The out of lock detector consists of NAND gate U11B, resistors R57, R58 and R84 and capacitors C83 and C86. This circuit operates in the same manner as the second local oscillator OOL circuit.

4.3.8 Receiver Control Section

The front panel Receiver control circuit card A9 provides for the in and out flow of Receiver control data, both from local (front panel) and remote locations. The front panel contains controls and indicators for local operation of the Receiver which includes: two - sixteen keypad switch sets, a tuning knob, two Liquid Crystal Displays (LCD), a fault indicator, an IF and AF GAIN control, two audio line level controls, an audio phones jack and a POWER-ON switch. All of these controls, except POWER-ON switch S1, are interfaced to Receiver circuits through the A9 circuit card. The IF and AF GAIN controls, two audio level controls and phones jack are routed directly through the A9 circuit card to their respective Receiver functions. The keypads, tuning encoder, LCD's and fault indicator connect through various interface circuits on the A9 circuit card to the microprocessor (A6A2). The data is processed by the microcomputer and routed back through interface circuits (A9) to various Receiver functions (A4, A5, A7 and A8). Receiver control data entered from a remote location is routed through interface circuits (A6A1) to the microprocessor (A6A2). This data is processed and routed through A9 in the same way as front panel data. Figure 4-16 shows a functional block diagram while the schematic diagram is shown on three sheets in Figure 7-11.

1. Front Panel Switches. Two sets of switch panels, each containing 16 pushbutton switches, are used to enter Receiver control data from the front panel. Switch panel 1 is used for Receiver tuning, BFO tuning and for selecting remote or local control. Switch panel 2 is used to select Receiver mode, AGC mode, bandwidth and RF/AF meter indication. Each pushbutton switch is a single pole, single throw switch with normally open momentary contacts. One contact of each switch is commonly connected to ground within each keypad set. The other contact of each switch is connected to an input of six hex buffers U7, U8, U9, U23, U24 and U25 (two inputs of U8 and U24 are unused) and to +5 volts through a 10K ohm resistor supplied through resistor array U1, U2, U5 and U6. When any particular switch is open (not pushed), its input to the buffer is held high through the 10K ohm resistor to the +5 volts. When the switch is closed (pushed), the input line to the buffer goes low. The high or low condition of any switch is passed through the respective buffers to the data bus when that particular buffer is enabled from the address multiplexer U29. The 32 outputs (four are unused) of the six hex buffers are strapped to the 8-line data bus in groups of eight with each group controlled from a separate address enable signal from U29. This assures that the status of two or more switches will not be transferred through the buffers to the same data line at the same time. The enable signals from U29 are controlled from in/out read and address control signals generated by the microprocessor in order to regularly scan the switch pads for new data. Data on these lines are transferred to the microprocessor as described in 5.

2. Tuning Encoder. The tuning encoder, operated from the front panel tuning knob, is used to adjust, in fine frequency increments, either Receiver frequency or BFO frequency. Pushbuttons, on the right keypad, select the mode of the tuning encoder and the rate at which frequency data may be entered. The TUNE RATE pushbutton selects one of three rates of change for main Receiver frequency that the tuning encoder will respond; fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments). The BFO pushbutton selects BFO frequency tuning in one rate only (10 Hz increments). The LOCK pushbutton disables the encoder while the TUNE RATE or BFO pushbutton enables the encoder from a locked condition. The tuning encoder consists of a 25 segmented disk operating in conjunction with two offset reflective object sensors U59 and U60 with the sensors being mounted on the A9 circuit card. The light from the sensor is reflected from the alternately reflective and non-reflective segments of the disk to the detectors as the disk is rotated.

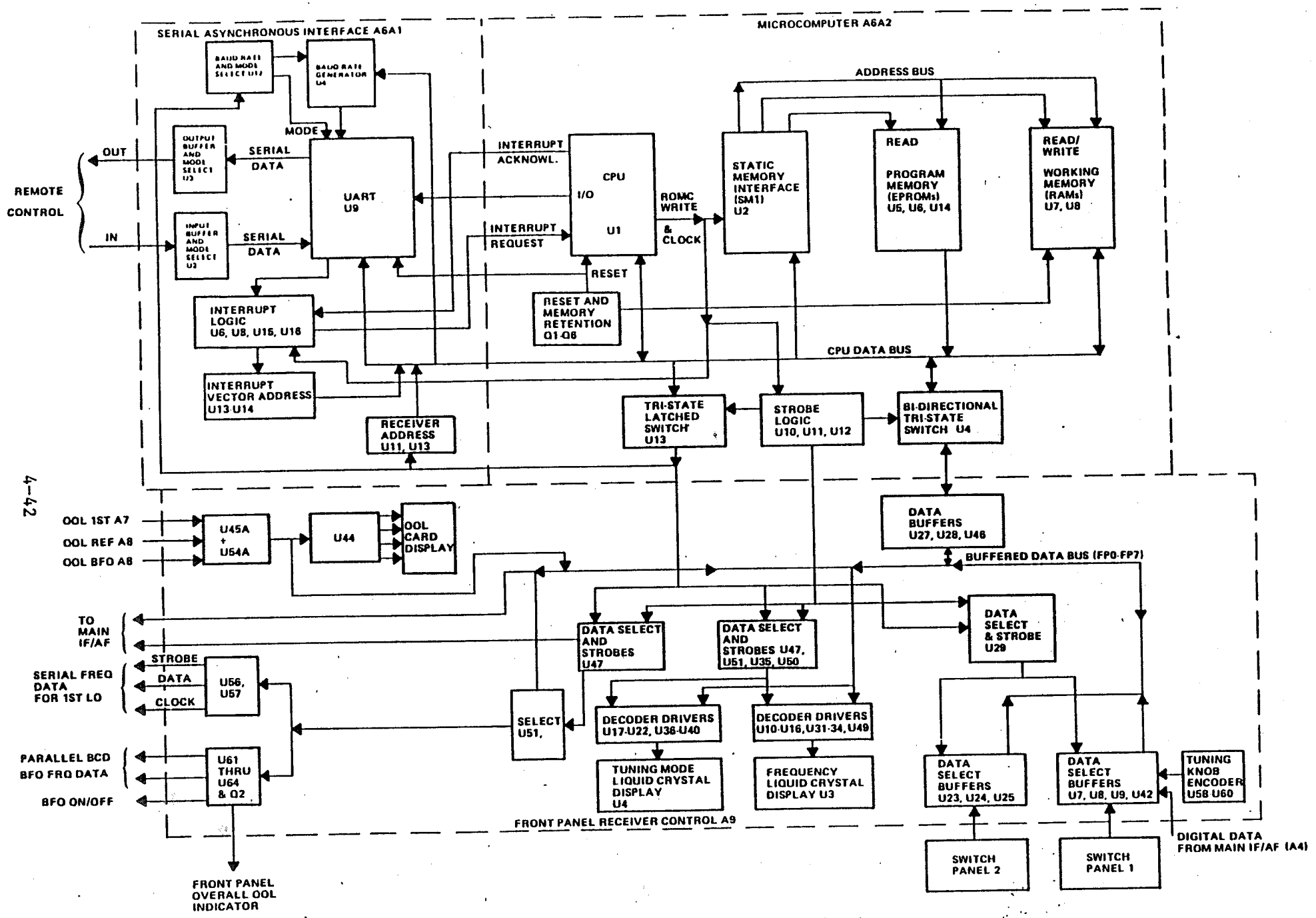


Figure 4-16. Front Panel Control, Block Diagram

This produces two pulse waveforms (see Figure 4-17). The two detectors are physically positioned, in relation to the disk segments, so that one waveform either leads or lags the other by 90 degrees. Clockwise rotation of the tuning knob causes the output of U59 to lead that of U60 causing frequency entered to increase. Counter-clockwise rotation causes the waveform of U60 to lead that of U59 causing frequency to decrease. The outputs of the object sensors are coupled, through resistors R16 and R17, to a comparator U58A and U58B. The two inputs to this circuit are compared to a fixed dc voltage input to the comparator from resistor combinations (R8 and R10 for U58A and R9 and R11 for U58B) which control the comparator switching point. The square wave outputs of the comparator are routed to buffer U42B. This data buffer is enabled, from multiplexer U29, in program sequence to transfer the encoder data to data lines FP0 and FP1 for processing as described in item 5.

3. Audio and IF. Audio and IF controls and an audio phones jack are contained on the front panel for control and monitoring of these functions. Control and audio to and from these components are routed through the A9 circuit card from the A4 circuit card with no connection to the in-out digital control hardware on A9. A complete description of their function can be found in Paragraph 4.3.4.

4. Liquid Crystal Displays. Two Liquid Crystal Displays (LCD) are contained on the front panel for displaying Receiver status. Receiver frequency and BFO frequency are displayed on LCD U3 while Receiver mode, AGC mode, tuning mode, remote/local mode, bandwidth and AF/RF metering are displayed on LCD U4. The 8-line data bus is routed directly to ten 4-line LCD drivers (U19-U22, U36-U40 and U49) and to thirteen BCD to seven segment decoder/drivers (U10-U18 and U31-U34). The ten line drivers provide decoding and drive for all annunciator displays while the thirteen 7-segment drivers provide decoding and drive for all numerical displays. Multivibrator U26, timed by R1 and C8, provides a 100 Hz signal to the DF (display frequency) inputs of the line drivers, the BP (backplane) inputs of the 7-segment drivers and the two LCD's. This signal is used to drive the LCD's display.

NOTE

LCD displays operate from low frequency square wave pulse trains. The contrast of the display being a function of the frequency.

Timing to the line drivers is provided by strobe signals from BCD to decimal decoder U50 while the 7-segment drivers receive timing from 4-bit latch and decoder U35. These two decoders receive their input from binary counter U51. The clock pulse (CP) for U51 is derived from three strobes S7, S11 and S15 combined by NOR gate U48A. Decoder U35 is controlled by inversion of strobe S7 through U48B while U50 is timed by strobe S15 through inverter U56. When a strobe signal in program time enables a line driver or 7-segment driver, the data at its input port is latched into the driver. The 100 Hz signal on the DF or BP input of the drivers is applied to the display segments and is inverted or not inverted through control of the data input to each driver. This in turn controls whether the segment is turned on or off. Any segment of an LCD is turned on by a 180 degree difference of phase between segment input and the main backplane drive to the LCD (Figure 4-18). To turn the display segment off the phase difference between these two signals must be zero degrees; that is, the two signals must be in phase (see Figure 4-18).

5. Receiver Control Circuit Card A9. This circuitry routes data entered at the front panel, to the microprocessor bus and routes processed data from A6A2 to various receiver functions on A4, A5, A7 and A8 circuit cards. This data flow in the data bus I0D0 through I0D7 is controlled by read, write and address controls (I0C0 through I0C7) signals from the microprocessor. All data entered from the front panel except audio and IF functions described in item 3, is transferred to the

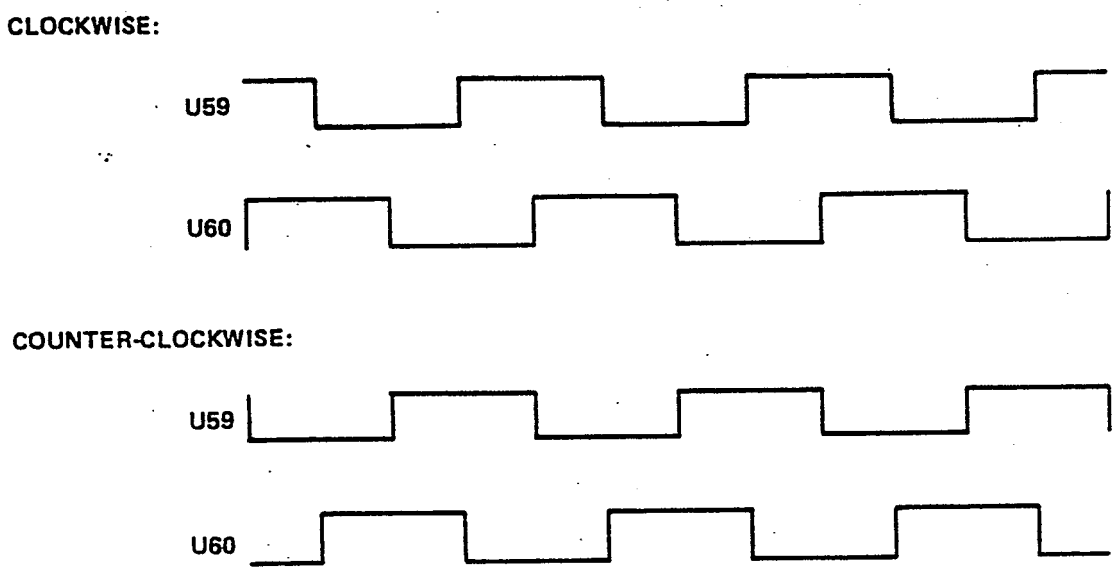


Figure 4-17. Encoder Output Signals

microprocessor for processing, then routed back through A9 to various Receiver functions. Data entered from a remote location is routed to the microprocessor, then the processed data is routed to various Receiver functions through A9 in the same manner as processed front panel data.

a. Data In/Out Control. Data flow between the A9 circuit card and the microprocessor is via their respective 8 bi-directional data lines. The flow of data from A9 to A6A2 and vice versa is buffered and controlled by U27, U28 and U46. The bi-directional switches U27 and U28 are configured to transfer data from A9 to A6A2 when enabled in a READ cycle via inverter U56. The tri-state, 8-bit latch U46 is used to transfer data from A6A2 to A9 during a WRITE cycle under the control of the WSTB signal. Control signals (I0C0 through I0C3) from the microprocessor are used to generate strobe signals are timed through the WSTB signal to the strobe input of U47 and from multivibrator U55A and U55B. The multivibrator, controlled from the WSTB signal and inverted I0C5 signal through NOR gate U48, provides timing to the inhibit input of U47. The strobe signals (U47 outputs) are then latched in proper timed sequence and are used to time latches, decoders, gates, etc., that in turn control data flow to various receiver control functions or displays. The data flow through these components and the strobe signal functions are described in the various receiver functions that follow.

b. Receiver Frequency. Processed receiver frequency data from the microprocessor is routed through data line FPO to one input of two input AND gate U57A. The second input to the AND gate comes from the Q0 output of decoder U64 which receives its input from presettable binary counter U51. Strobes S5 and S7, S11 and S15 through NOR gate U48 time U51, strobe S11 through inverter U56 time U64. The frequency data in proper timed sequence is serially routed through AND gate U57A to the A7 circuit card. Strobe signal S12 and the Q0 output of U64 are connected to two input AND gate U57B whose output is routed to A7 as a clock signal for circuits on that card. The Q0 output of U64 is also routed to A7 through inverter U56 as a strobe signal to those same circuits. These circuits on the A7 circuit card further process the serial frequency data in conjunction with the clock and strobe signals, and adjust the oscillator frequency as first directed from the front panel or remote location.

c. BFO Frequency. BFO frequency data after being processed by the microprocessor (A6A2) is routed through data lines FP0, FP1 and FP3 to the same binary counter (U51) as the Receiver frequency data. Outputs (Q1, Q2 and Q3) of the binary counter are connected to the three binary inputs of four 8-bit addressable latches U61 through U64. These latches supply the BCD inputs to a programmed divider circuit on the A8 circuit card for BFO frequency control. Timing for the latches is supplied by strobe S11 through inverter U56. The Q4 output of latch U61 provides a signal through transistor Q2 that enables the BFO synthesizer on A8 in CW and SSB/ISB modes.

d. Circuit Card A4 Functions. All eight data lines along with six strobe signals are routed to control circuits on the A4 circuit card for control of various receiver functions operating on this circuit card. The control circuits (located on A4) are a direct function of the A9 interface circuits; therefore, a description of their operation is included in this paragraph. All references to components in this paragraph (unless otherwise noted) refer to components on the A4 circuit card. Refer to Figure 7-4 for the schematic diagram. The eight data lines of A9 are routed to 2-level translators (U3 and U5) on the A4 circuit card. Six strobe signals (STB10 through STB15) are also routed to A4 with strobes STB12 through STB15 connected to the input of level translator U16. These level translators provide a new voltage level to the incoming data for operation of circuits on the A4 card. The strobe outputs from translator U16 are used to clock data latches U2, U4, U13, U15 and U23, the digital-to-analog converter U21, and the crosspoint switch U25. The data bus output from translators U3 and U5 is routed to these components and applied to the various A4 functions as directed by the strobe signals. Data latch U2 is used to select the bandpass filters, but through

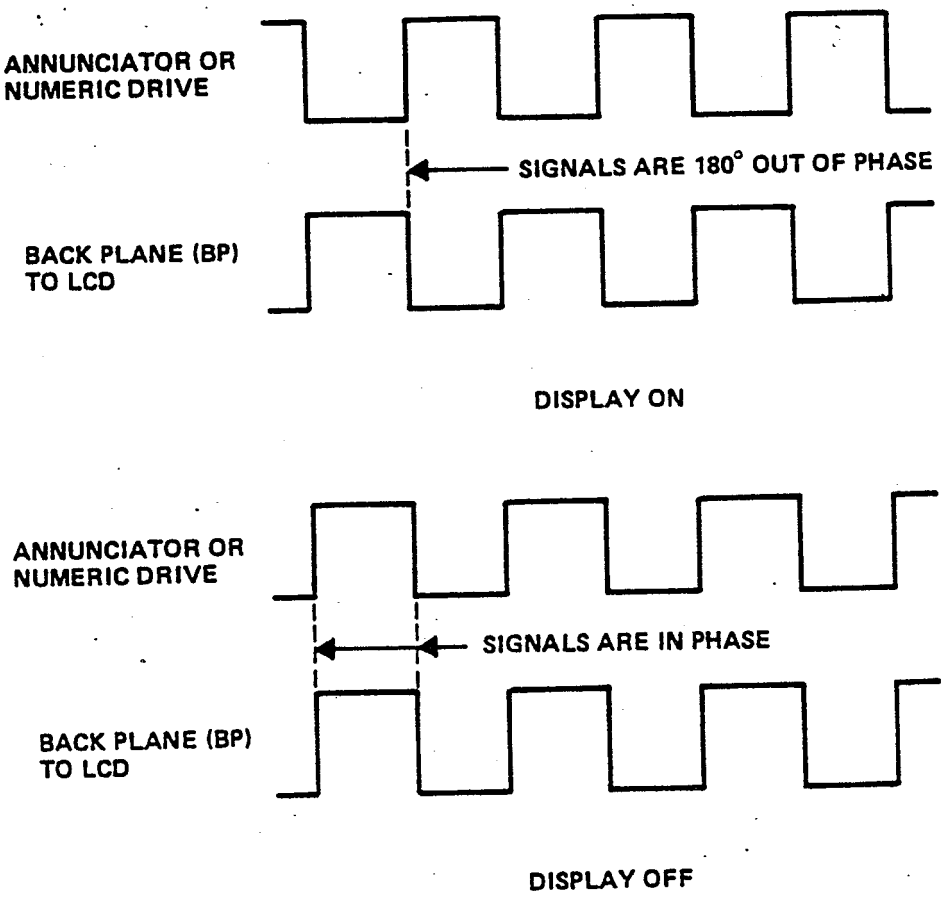


Figure 4-18. Liquid Crystal Display Control Signals.

BCD to 1 of 10 decoder U1. This decoder has only one output high at a time as directed by the BCD input. This allows selection of filter slots FL2 through FL7 in accordance with the three digit BCD on the data line as clocked by strobe 12 on the clock input of U2. The Q4 output of U2 is routed directly to the diode switch of FL1 which is used to select that filter slot at the appropriate program time. Data through data latch U4 is used to control the RF switch that selects between BFO and the IF signal for input to the limiting amplifier and FM detector and D flip-flop U9A. This flip-flop controls the AGC dump line. Data latch U4 is also timed by strobe 12. Data through data latches U13 and U15 control switches in the AGC circuits for various AGC modes. These latches are timed through strobe 13. The output of data latch U23, timed by strobe 15, controls the detector select switch U19A, an audio filter level control switch U19B and an AF meter audio select switch U19C. All eight data lines are connected to the digital-to-analog converter for digital control of its analog output. This unit is timed through strobe 14 and is used to provide analog-to-digital conversion of the DIV AGC line and audio line by peak detector U22A using a successive approximation technique. The digital information gathered by the microprocessor is used for front panel metering. Five data lines are routed to crosspoint switch U25 which is timed by strobe S15. The audio function of the crosspoint switch along with other A4 functions controlled through A9 are described under the A4 circuit card in Paragraph 4.3.4.

e. Circuit Card A5 Functions. Two data latches on the A5 circuit card are used to control AGC circuit functions on this circuit card. The two latches U7 and U8 have A5 reference designators and are shown on the A5 schematic diagram in Figure 7-5. The 8-line data bus from translators (described in Paragraph d) on the A4 circuit card are routed to the data latches with strobe 10 timing both latches through transistor Q6, also located on A5. The data output from the latches is used to control the AGC circuits described under the A5 circuit card in Paragraph 4.3.5.

f. Out of Lock (OOL) Functions. Three out of lock circuits, that monitor the condition of the phase lock loops of the three oscillators, drive OOL indicators on the A9 circuit card and supply their output data to the microprocessor. This data is routed through circuits on the A9 card that drive a fault indicator on the front panel and also a fault indicating circuit that provides a TTL level related to the FAULT condition to connector J3 on the rear panel via A4 circuit card. The three OOL circuit outputs from the three oscillator phase lock loops are connected to the S inputs of dual D flip-flops U45 and U54. These flip-flops are clocked from address multiplexer U29. With the data and reset inputs tied to ground (low) and the S inputs low (phase lock loop in lock) the Q outputs of the flip-flops will be low. If an S input goes high (out of lock) its Q output will go high causing a low through its respective inverter U44A, U44B or U53A. This in turn will enable the applicable LED indicator DS1, DS2 or DS3. These LED indicators are located on the A9 circuit card for accurate determination of the OOL circuit. The Q outputs of the flip-flops are also connected to the inputs of buffer U43 which is also timed by multiplexer U29. The buffer, in program sequence, outputs the status of the OOL circuits on the data bus which is then routed to the microprocessor. The processed FAULT data is routed through binary counter U51 and decoders U63 and U64. The Q5 (FAULT) output of decoder U63 is routed through inverter U52B to the rear panel while the Q5 (FAULT) output of U64 drives the front panel fault indicator through inverter U52A.

g. AF/RF Meter Comparator Functions. The main RF, ISB RF, and AF comparator circuits along with an ISB fitted circuit from the A4 circuit card are connected to four inputs of non-inverting buffer U42A. The inputs are strapped to +5 volts through 22K ohm resistors in resistor array U41. When the optional A5 circuit card is installed, input I1 is strapped low through a grounding circuit on that card. The three comparator input (I2, I3 and I4) levels depend on the comparator outputs. Buffer U42 is timed from multiplexer U29 and in program sequence transfers the comparator data as used by A6A2 in a successive approximation technique to generate a bar graph for front panel display to data lines FP0, FP1 and FP2 and the ISB fitted status to data line FP4.

h. Power Supply Distribution. The A9 circuit card provides a distribution path for dc power, generated from the A10 power supply module directly to circuit cards A4, A6A2, A7 and A8. This dc power through A9 is further distributed through the A4 circuit card to the optional A5 circuit card and through A6A2 circuit card to optional A6A1 circuit card. The +15 volts dc is also routed to the front panel for operation of the LCD back lighting. The distribution of this dc power is as shown below.

DC Power	From A10 To A9J4 Pin Number	Output To A4 from A9J5 Pin Numbers	A6A2 from A9W1 Pin Numbers	A7 from A9J6 Pin Numbers	A8 from A9J7 Pin Numbers
+5 Volts	3, 4, 7 and 8	1	23 and 24	20	26
+5 Volts (unregulated)	9 and 10		15 and 16	15 and 16	
+5 Volts	13, 15, 19, 21 and 22	2 and 4	19 and 20	17 and 18	24
+ 15 Volts (unregulated)	5 and 6	8			
−15 Volts	18 and 20	6	21 and 22	14	22
+20 Volts	1 and 2				

4.3.8.1 Microcomputer Board A6A2

A functional description of the microcomputer board A6A2 is given in Paragraph 4.2.4 with a functional block diagram shown in Figure 4-20.

As shown on the electrical schematic diagram, Figure 7-8, the microcomputer board A6A2 makes use of a type 3850 CPU (U1). The 3850 CPU is from the Fairchild F8 microcomputer component family. A detailed description of the microcomputer family operation, including timing and instruction set, is given in the F8 Users Guide. This guide is available from the Fairchild Camera and Instrument Corporation, Mountain View, California.

The CPU (U1) controls receiver operation by reading the operating program and routing data and control signals throughout the receiver based on the procedures and algorithms of this program. The CPU 8-bit data word bi-directional ports (DB0-DB7) connect to an 8-line data bus. This bus is common to major receiver control circuitry (directly or through buffers) and is the primary means of communication between the CPU and other parts of the receiver. The CPU clock is provided by the 2.0 MHz crystal Y1 which is connected across pins 38 and 39 of the CPU. The Φ and Write pulse outputs (shown in Figure 4-19) are clock outputs which provide timing drive for all microcomputer circuitry. The ROMC-0-4 outputs from the CPU connect to other circuits in the receiver and identify operations which these circuits must perform during any instruction cycle. Interrupt requests are received through the /INT REQ port while the acknowledgement that the CPU will respond to the interrupt requests is routed through the /ICB port. The Input/Output (I/O) ports 00-07 and 10-17 are ports through which the CPU communicates with logic external to the microprocessor. Here, seven of these ports are used and are connected to the serial asynchronous interface module A6A1 (when it is installed in the receiver).

Figure 4-20 is a functional block diagram of the CPU. The inputs and outputs, described previously, are shown as well as the basic functions performed by the CPU. The CPU performs

instructions which are obtained from the control program contained in the program memory (EPROMs, U5, U6 and U14). These instructions are routed to the instruction register of the CPU and then carried out during instruction cycles. The control unit logic of the CPU sends out the ROMC signals to other parts of the Receiver during each instruction cycle. These specify the functions to be performed for each instruction. There are four or six clock periods (Figure 4-19) in an instruction cycle (dependent upon the number of 8-bit instruction words required), which are determined by the ROMC signals generated by the CPU. The CPU performs computations, when required by the program, in its ALU (Arithmetic Logic Unit) making use of the accumulator, status register and scratch pad memory registers. The ISAR (Information Storage Address Register) is the address register for the scratch pad memory.

The CPU receives and follows the program (sequence of instructions) which is stored in the erasable/programmable read only memory (EPROMs) contained in U5, U6 and U14 (Figure 7-8). These are type 2716 EPROMs. Each of these units contains 2K 8-bit words for a total of 6K 8-bit words of programmable memory. The CPU also uses the temporary Random Access Memory (RAMs) contained in U7 and U8. These are type 5101L RAMs and provide 256 8-bit words of working memory (temporary data storage). U7 provides 4 bits of each 8-bit word and U8 provides the remaining 4 bits of each word.

The memories are addressed by the CPU through U2, the Static Memory Interface (SMI) type 3853 (Figure 7-8). The CPU sends the ROMC-0-4, Write and Φ signals to the SMI. The SMI, in timed sequence, recognizes the ROMC-0-4 code for a memory access operation, and addresses the appropriate memory, program (EPROM) or working (RAM), over the address bus A0-A10. The SMI (U2) address outputs A11 and A12, through decoders U3A and U3B are also used in addressing by enabling the appropriate memory chip U5-U8 and U14. Directed by the ROMC-0-4 code and write signals from the CPU, the SMI also directs reading or writing through its CPU READ and /MEM W outputs. Thus, the memory units (when addressed and directed place data on the CPU data bus or accept data from the CPU data bus (DB0-DB7). The EPROMs place 8-bit instruction words on the bus and the RAMs supply data to or read data from the bus when addressed and directed by the CPU under program control.

Figure 4-21 is a functional block diagram of the System Memory Interface (SMI). The inputs and outputs, described previously, are shown. The SMI contains the program counter which contains the program memory address (at which instructions are located) and the data counters which contain the working memory (RAM) addresses. The program counter is either incremented as each instruction in the program is executed or new addresses are inserted by the program or by the interrupt address vector. The working memory addresses are generated by the program. The SMI also contains a timer which is used to generate internal interrupts for initiating program subroutines at required times during the program cycle.

As described previously, the CPU (under program control) writes and reads data to and from the front panel controls and displays and the receiver circuitry. This data consists of front panel control settings, display readouts and receiver circuit control and status signals in the form of 8-bit digital words. The CPU data bus (D00-D07) connects to these units via the tri-state bi-directional switch U4 (Figure 7-8) and then through the bi-directional data bus (I0D0-I0D7). The direction of data flow and timing of switch openings are controlled through pins 1 and 19 of U4. Signals to these pins are generated by the strobe logic gates U10-U12 and the Q7 output from the tri-state latched switch U13 at the appropriate times in the program. The strobe logic inputs consist of the ROMC-0-4 and write signals. Thus, at appropriate program times, the CPU data bus connects through U4 and through pins 1-8 of connector J2 to the front panel and receiver control circuitry. Also, outputs /IO READ and /WSTB from pins 25 and 27 of J1 go to the front panel and receiver control circuitry to direct reading or writing data from or to the bus at the appropriate times in the program. The U13 latched outputs (I0C0-E0C7) provide the programmed codes

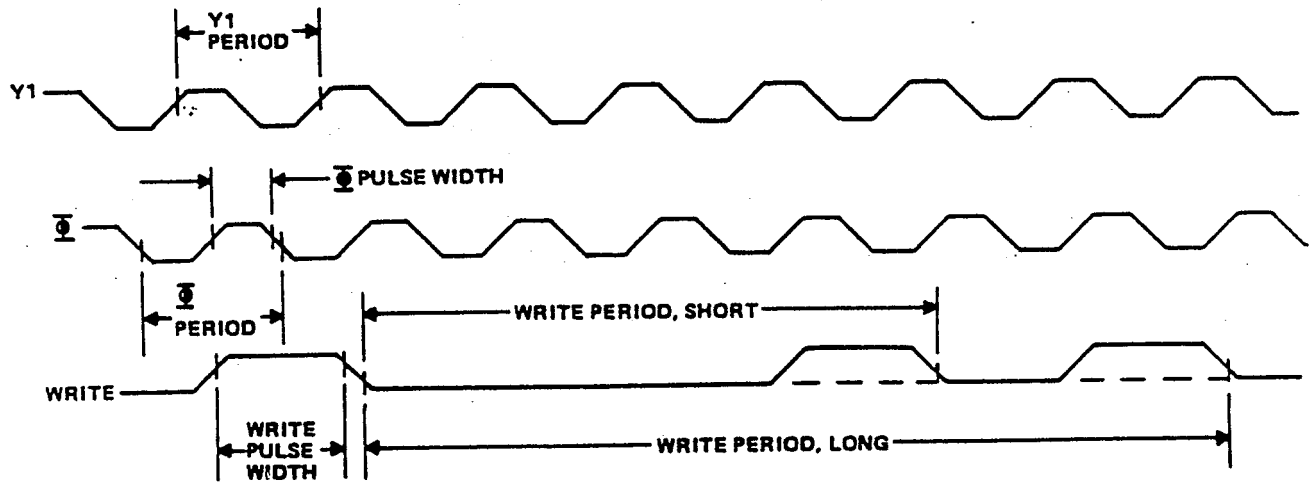


Figure 4-19. Central Processor Unit Timing Signal Diagram

for the selection (or addressing) of the various elements in the front panel and receiver control circuitry (to accept or supply data from or to the common data bus) at appropriate times in the program. These addresses (I0C0-E0C7) are latched into the U13 outputs from the CPU data bus (D00-D07) at the proper times in the program through the U13 OE (output enable) and CP clock inputs. The OE and CP inputs are generated by the ROMC-0-4 and write outputs from the CPU through gates U10 and U12. The CPU also receives and sends data from and to the Serial Asynchronous Interface modules (A6A1) via the data bus. This data consists of commands and receiver settings to the CPU and receiver status to the remote controller in the form of 8-bit digital words. Connections between these units are made through connector J2. The data bus to the Serial Asynchronous Interface module is labeled PB0-PB7. The microcomputer receives the interrupt request (/INT REQ) signal from the Serial Asynchronous Interface module. The CPU also sends the WRITE, Φ timing signal, strobe logic outputs /IO READ and /WSTB, the tri-state latched outputs I0C0-I0C7, the ROMC-0-4 outputs, the CPU 00-07 and 10-17 outputs and the interrupt acknowledge /ICB signal. These signals are used to direct operations of the interface module and to synchronize operations between the CPU and the remote controller, as will be described later.

The reset and memory retention system is composed of stages Q1 through Q7, the 2.0 volt internal power source BT1, R9, CR3 and C16, and the battery charging circuitry, CR6, R9. At Power On, the +5 Volt unregulated line (from pins 15 and 16 of J1) switches Q1 and Q2, bringing the /RESET line high. Also at Power On/RESET turns Q4 and Q5 on, C15 is charged, the gate of Q6 is taken negative and CE2 of the RAMs (U7 and U8) is asserted. This activates the RAMs in their normal operating, higher power drain, mode. Also, the gate of Q7 goes negative taking the low off the CPU RESET. The CPU now starts the initialization process. During the turn on cycle the +12V through R8 quickly turns on Q3, charging C16, which supplies Vcc to the RAMs. CR2 limits the voltage to Vcc while R11 limits the current. CR3 is back biased and the +5 volt supply through CR6 and R9 charges the internal battery BT1.

The Schmidt trigger, Q1 and Q2, detects voltage variations in the +5 volt unregulated line. The collector of Q2 will go to ground when the power supply +5 volt unregulated line decreases (such as at power turn off or failure) past the trigger levels set by CR1 and R2-R5-R6. When this occurs, the /RESET line goes low. Also, the voltage at D of Q7 going low, instructs the CPU to come to a stop at the end of the next execution cycle. At power down, Q3 will stop conducting. Initially, the voltage across C16 still supplies sufficient VDD voltage to the RAMs for the CPU to complete its cycle. When the voltage across C16 falls to approximately 2.4 volts the internal battery BT1, through R9 and CR3 supplies the memory retention power to the RAMs. The voltage out at D of Q6, now low, sets the RAMs at their lower power drain memory retention mode. The battery leakage is greater than the retention memory current drawn by the RAMs; therefore, several months of memory retention is available.

The CPU may receive an interrupt request (/INT REQ) into its pin 23 from the SMI (internal interrupt) or from the Remote Controller Serial Asynchronous Interface (when used) through J2. During an interrupt routine, the CPU will assert its /ICB output (from pin 22), thus not accepting any further interrupts until it has completed the routine. When a Remote Controller Serial Asynchronous Interface is not used, with no J2 connection and with LINK 1 installed (see Figure 7-8),the /ICB output from the CPU connects directly to the /PRI IN input of the SMI. This prevents an internal interrupt from being generated by the SMI until any previously accepted interrupt has been serviced by the CPU. When a Remote Controller Serial Asynchronous Interface is used with the interface connected to J2 and LINK 1 removed, the /ICB output goes directly to the Serial Asynchronous Interface circuitry. As will be described in more detail later, this prevents the interface from generating an external interrupt until any previously accepted interrupt has been serviced by the CPU. In addition, the PRI input (into pin 24 of J2) from the Serial Asynchronous Interface goes to the /PRI IN of the SMI. The Serial Asynchronous Interface is waiting to request an interrupt. Thus, the SMI cannot generate an

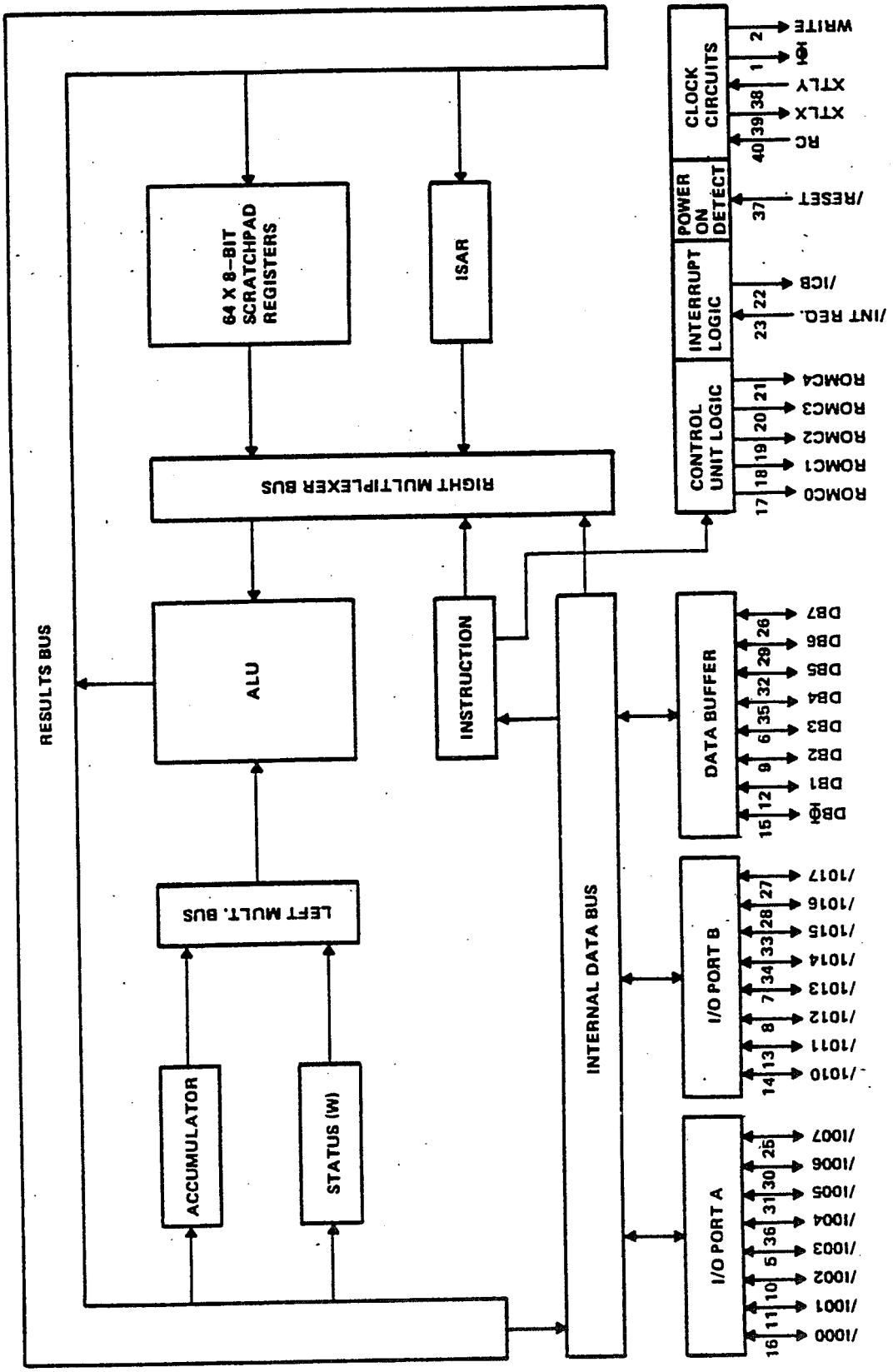


Figure 4-20. Central Processor Unit Functional Block Diagram

internal interrupt while either of these conditions exist. It will be noted that the DR and TBRE outputs from the UART (in the Serial Asynchronous Interface, see Figure 7-7) are sent out through connector P1, pins 37 and 36, to the CPU I/O terminals 11 and 10. These are used by the microcomputer to determine whether the interrupt request was for a receive or transmit routine.

The error outputs from the UART; PE (parity error), OE (overload error) and FE (framing error) are sent to the CPU I/O ports 14, 13 and 12 through connectors P1 pins 5, 43 and 42.

4.3.8.2 Serial Asynchronous Interface Module A6A1

A functional description of the Serial Asynchronous Interface Module is given in Paragraph 4.2.4 in conjunction with the functional block diagrams, Figure 4-16 and 4-21.

Figure 7-7 is the electrical schematic diagram of the Serial Asynchronous Interface Module A6A1. This module interfaces an external remote controller (when used) through a serial data line to the microcomputer through an 8-bit data bus. The Universal Asynchronous Receiver transmitter, UART (U9), provides the interface between the serial data lines to and from the remote controller and the microcomputer parallel data bus (PB0-PB7).

The UART contains a transmit and a receive station. A block diagram for each of these sections is shown in Figures 4-22 and 4-23. The receive section converts the incoming serial stream (from the remote controller into the pin 20 RR1 input) to 8-bit parallel words and places them on the microcomputer bus through output pins 5 through 12. The transmit section, when directed by the microcomputer (through pin 23, data strobe TBRL) takes the 8-bit parallel words from the microcomputer data bus (through pins 26-33) and puts them in a serial format for serial transmission to the remote controller (through pin 25). The serial format,Section III, Paragraph 3.3.3.2, is an 11-bit word containing one start bit, the 7-bit ASCII Code data word, a parity bit followed by two stop bits. Coding for the data word is described in Section III, Paragraph 3.3.3.2. The UART parallel inputs and outputs are tied together and onto the common microcomputer data bus (Figure 7-7). The UART receiver inputs and outputs are tri-state, with only inputs or outputs activated at one time.

The UART is initialized by the /RESET line from the microcomputer, through pin 2 of connected P1 and inverter U6A, into its MR (pin 21) input. Transmit and receive clock signals, TRC and RRC (pins 40 and 17), which determine the rate of data transfer, are supplied by the programmable Baud Rate generator U4. This generator divides the frequency of crystal, Y1, down to the programmed transmit and receive clock rates. Both the receive and transmit clock rates are set at 16 times the baud rate. The frequency generated by U4 is obtained from the data bus, upon initialization by the microcomputer program from information supplied by the configuration set on the rear panel cover into its input RA-RD and TA-TD. This data is strobed into U4 by the strobing signal from output VO (pin 14) of decoder U19. This decoder is driven by microcomputer address and strobing signals I0C0-I0C1, I0 READ and /WSTB. As indicated by Table III on the A6A1 schematic diagram, the baud rate is set by connecting the appropriate A6A1W1J1 external connector terminals W, X, Y and Z to common. Terminals not connected to common will have +5V connected through U1. These terminals connect to inputs of tri-state buffer U12. The inputs are strobed onto the data bus (to go to the baud generator inputs, at the appropriate times), by the strobe signal out of X1 (pin 4) of decoder U19. The baud rate is set to match that of the Remote controller. Table 2-7 gives information for setting the baud rate.

Also strobed, upon initialization, from output Y1 of decoder U19 is the CRL (pin 34) input to the UART. This loads the UART control register with the EPE, CLS1, CLS2, SBS and P1 inputs at that time. This sets whether parity is used (P1) odd or even parity (EPE), number of bits in a data word (CL1, CL2) and number of stop bits (SBS) used. As described previously, the

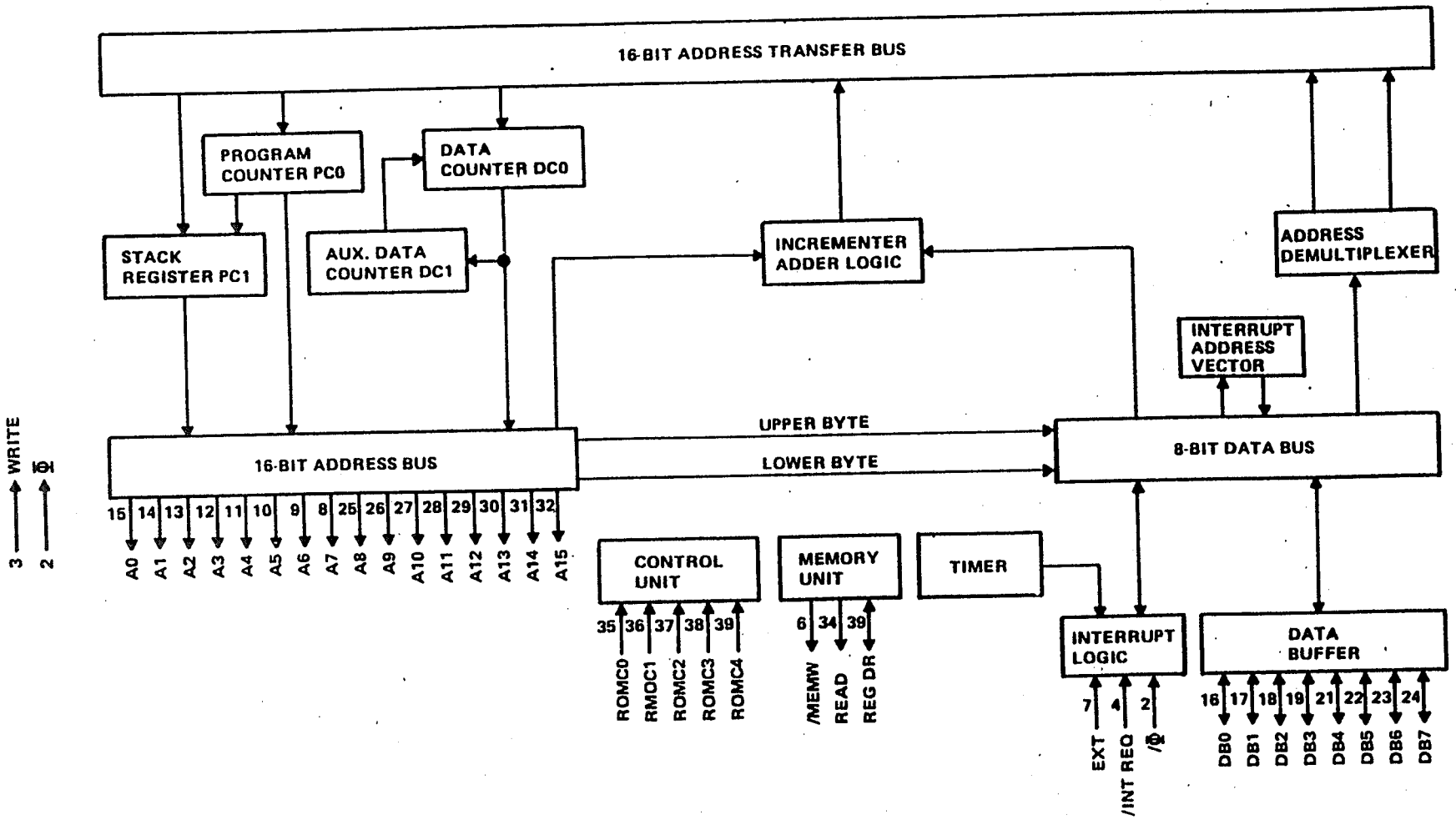


Figure 4-21. System Memory Interface Functional Block Diagram

word length is fixed at 8 and the number of stop bits is fixed at 2. Table I on the schematic shows that the parity (ON or OFF) and even or odd parity are set through terminals U and V of external connector A6A1W1J1. These are also set by connecting the appropriate terminals to common ground. The unconnected terminals will have +5V connected through U1. These terminals also connect to tri-state buffer U12 and are strobed on to the data bus (and to P1 and EPE) at the appropriate time by the strobe signal out of X2 (pin 4) of decoder U19.

The receiver number for remote addressing is selected by connecting the appropriate terminals K, L, M, N, P, R, S, T of connector A6A1W1J1 (See Table I on schematic) to common. This setting through tri-state buffers U11 and U13B and Pull-up resistors U10 and U1 is strobed onto the data bus, for readout by the microprocessor, by the strobe from X1 (pin 3) of decoder U19.

Figure 4-23 is a block diagram of the receive station of the UART. When data is received from the remote controller, it comes through the external connector A6A1W1J1 to Receiver U2. Receiver U2 yields signals that are compatible to the Receiver circuits of the UART (U9) through its RR1 input (pin 20). The UART receiver section converts the incoming serial data stream from the remote controller to 8-bit parallel words and places them on the microcomputer bus (PB0 through PB7) through outputs RBR1 through RBR8. The serial format, as described previously, is an 11-bit word containing a start bit, a 7-bit ASCII code, a parity bit followed by two stop bits. Instruction word codes are also described in Section III. When data is available from the remote controller, an interrupt request is made by asserting the DR output, indicating data is available to the microcomputer. The DR output will go through gate U8A, if not inhibited by computer outputs 00 and 01 (microcomputer not accepting these interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D, and U17B) to drive flip-flop U16A. The outputs of this flip-flop drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. If the CPU is currently blocking, thus ignoring interrupt requests, /ICB will be high. Under this condition U15B and C gates are inhibited. When /ICB is not high (microcomputer accepting interrupts), gates U15B and C are enabled. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its normal Receiver monitoring functions as directed by the control program (from EPROM) and start the interrupt routine to accept data from the remote controller.

During the interrupt routine the microcomputer asserts its /ICB output, thus not accepting any further interrupts until it has completed the routine. It will be noted that the DR output from the UART are routed through connector P1, pin 37 to the microprocessor I/O terminal 11. This input enables the microcomputer to determine that the interrupt request was for a receive routine.

Figure 4-22 is a block diagram of the transmit section of the UART. When the remote controller has requested data (status) and the transmit buffers of the UART are empty, so that it can accept data from the microcomputer for transmission to the remote controller, the TBRE output is asserted. The TBRE signal will go through gate U8A, if it is not inhibited by microcomputer outputs 00 and 01 (microcomputer not accepting interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D and U17B) to drive flip-flop U16A. The outputs of these flip-flops drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. When the CPU in the microcomputer is busy and ignoring interrupt requests, /ICB will be high. Under this condition, U15B and C gates are inhibited. When /ICB is not high these gates (U15B and C) are enabled and the /PRI output from U15C is output through pin 24 of P1. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its present program and start the interrupt routine to send

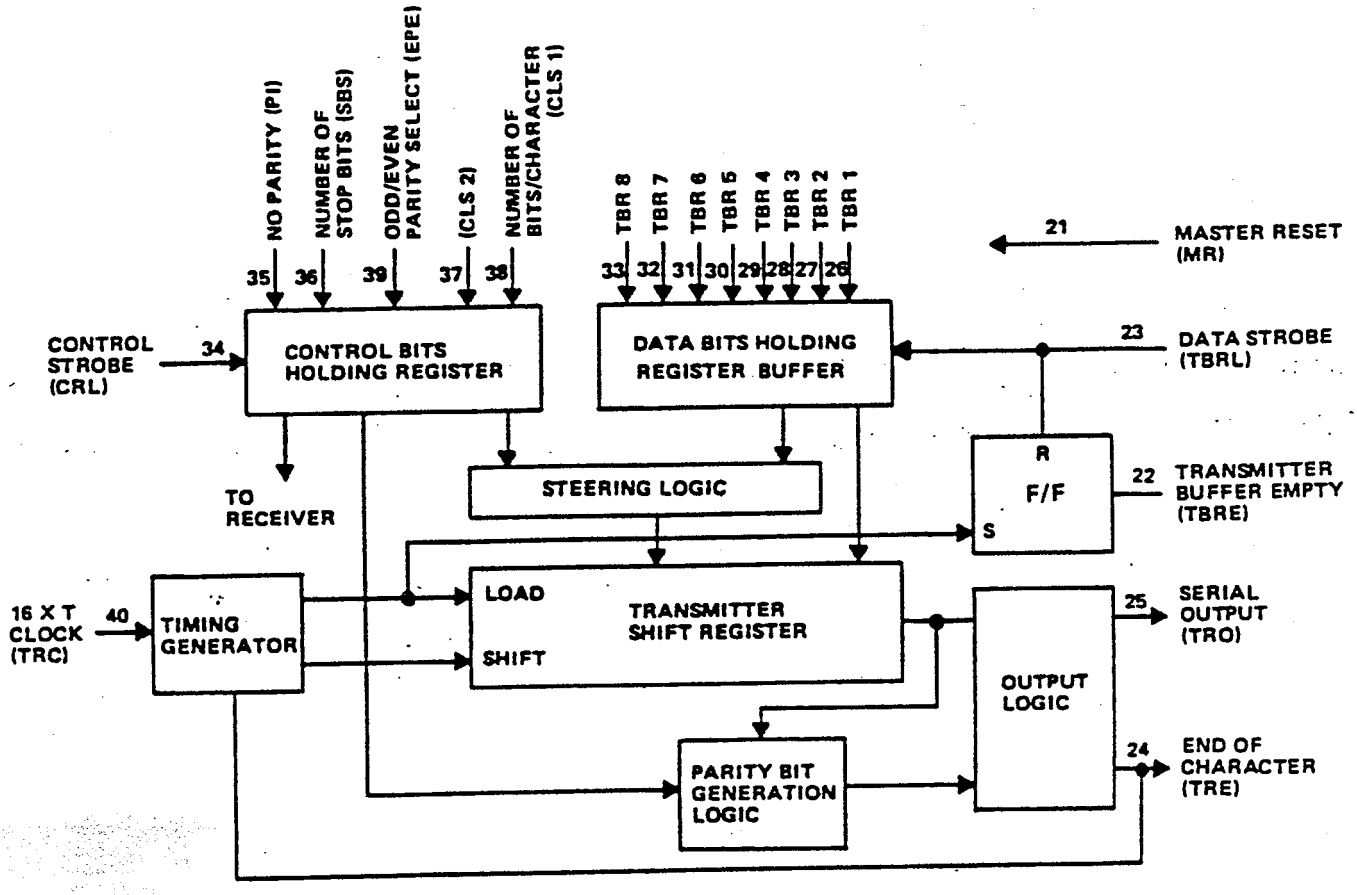


Figure 4-22. UART Transmitter Functional Block Diagram

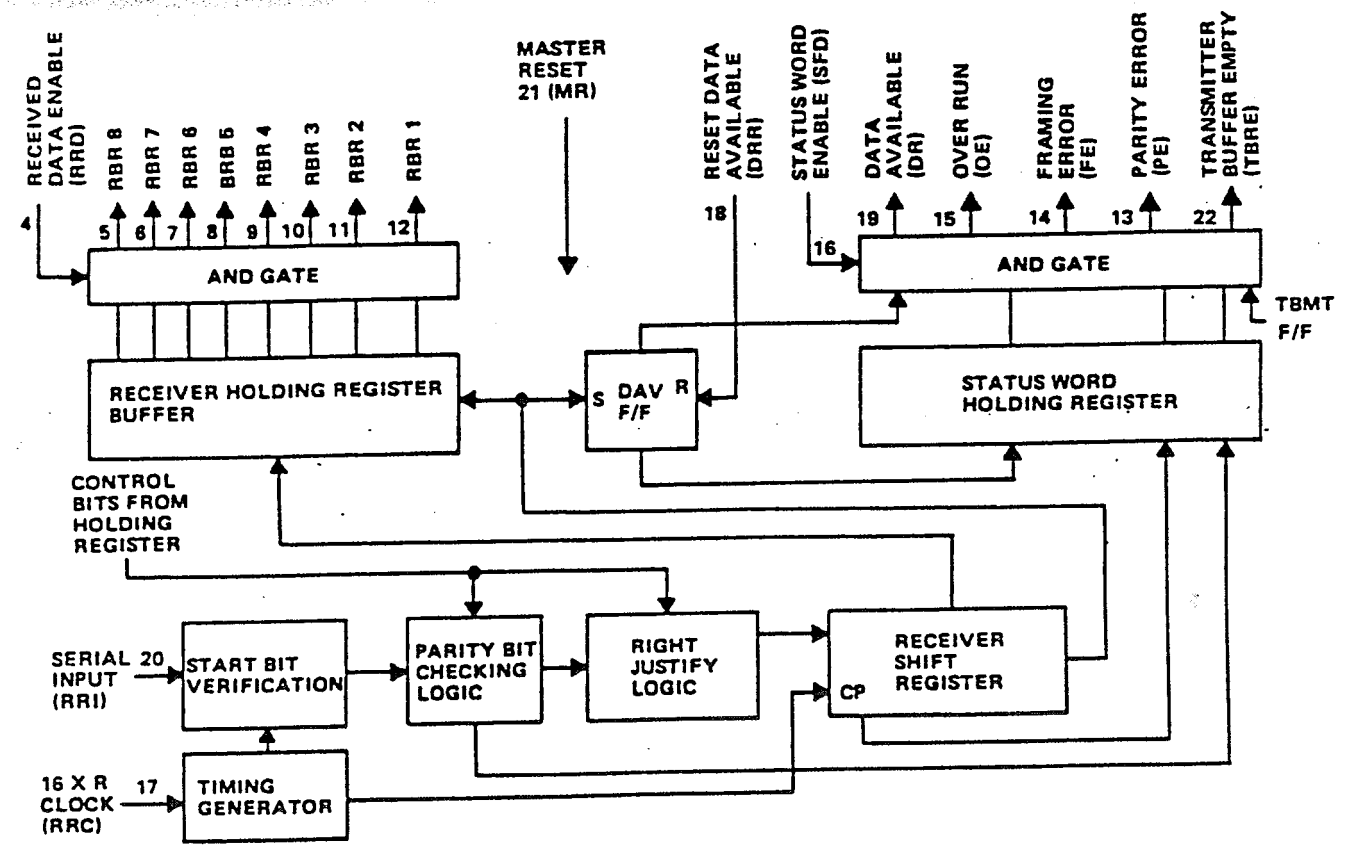


Figure 4-23. UART Receiver Functional Block Diagram

receiver status to the remote controller. During the transmit interrupt routine the microcomputer asserts its /ICB output, and will not accept any further interrupts until it has sent the status data to the remote controller. The TBRE output from the UART is routed through connector P1 pin 36 to the microcomputer I/O terminal 10 to identify the interrupt as a transmit routine. The serial output from the UART is output TR0 (pin 25) and is routed through line driver U3 to the remote controller through external connector A6A1W1J1.

Connections between the serial asynchronous interface module and the remote controller may be selected to accommodate signals compatible with MIL-188C/RS-232C, RS-423 and RS-422. The selection is made by connecting the remote controller to the interface external connector A6A1W1J1 in accordance with Table II (shown on the schematic) and using the links (on the Serial Asynchronous Interface module) in accordance with Table IV (shown on the schematic).

The interrupt circuitry on the A6A1 module not only generates the interrupt request, but it also provides the microcomputer with the interrupt vector. This is the program memory address at which the interrupt routine starts. A specific sequence of ROMC signals (put out when the CPU expects the interrupt vector address) is detected by gates U15D, U15A and flip-flops U16C, U16D and U16A. When these signals are received, gate U15A enables switches U13A and U14A to output the interrupt vector on the data bus to be read by the microprocessor.

4.3.9 Power Supply, A10

The receiver contains a power supply module that provides the power required for operation of the receiver. Refer to schematic diagram, Figure 7-12. The module operates from an ac line input, steps down the voltage, rectifies the ac, filters and regulates the various divided voltages. The unit contains a circuit card switch which provides for switching the transformer input for 100, 120, 220 or 240 volts ±10% operation from the input power line. This line frequency can be between 43 and 420 Hz and is controlled through the POWER-ON toggle switch located on the front panel. The input power is also fused through F1, located on the rear panel for easy access. The 100 or 120 volt input must be fused differently than the 220 or 240 volt input. The alternate fuse is contained in a fuse holder located inside the power supply.

4.3.9.1 DC Power Output

The secondary of transformer T1 contains three separate windings that provide the six different dc outputs for receiver operation. These six dc outputs, along with their tolerances are listed below:

+20 ±1 volt
+15 ±0.5 volt
+15 volts unregulated (nominally +22 volts)
−15 ±0.5 volt
+5 +0.5 −0.2 volts
+5 volts unregulated (nominally +10 volts)

Conventional bridge rectifiers CR1, CR2 and CR3 provide ac to dc rectification while capacitors C1, C4, C7 and C10 provide filtering and to smooth the pulsating dc. Capacitors C1 through C9 are connected adjacent to the three voltage regulators to suppress possible oscillations. The rectified and filtered dc from one winding 12 to 13 of the transformer is coupled to dc regulator A10A2, which provides the regulated +20 volts to pins 1 and 14 of A10J3. Winding 6 to 8 provides the +15 volts unregulated to pins 3 and 16, the +15 volts regulated through regulator U2 to pins 7, 8, 10, 11 and 24 and the −15 volts regulated through regulator U3 to pins 22 and 23. Winding 9 to 11 provides the +5 volts unregulated to pins 5 and 18 and the +5 volts regulated through regulator U1 to pins 2, 4, 15 and 17 of A10J3. The six dc outputs from A10J3 are routed to various applications throughout the receiver circuitry.