INSTRUCTION MANUAL

DIGITAL RECEIVER

FR-101

(DIGITAL COUNTER UNIT)

YAESU MUSEN CO., LTD.

TOKYO JAPAN

DIGITAL FREQUENCY READOUT
FOR
FR-101 DIGITAL RECEIVER

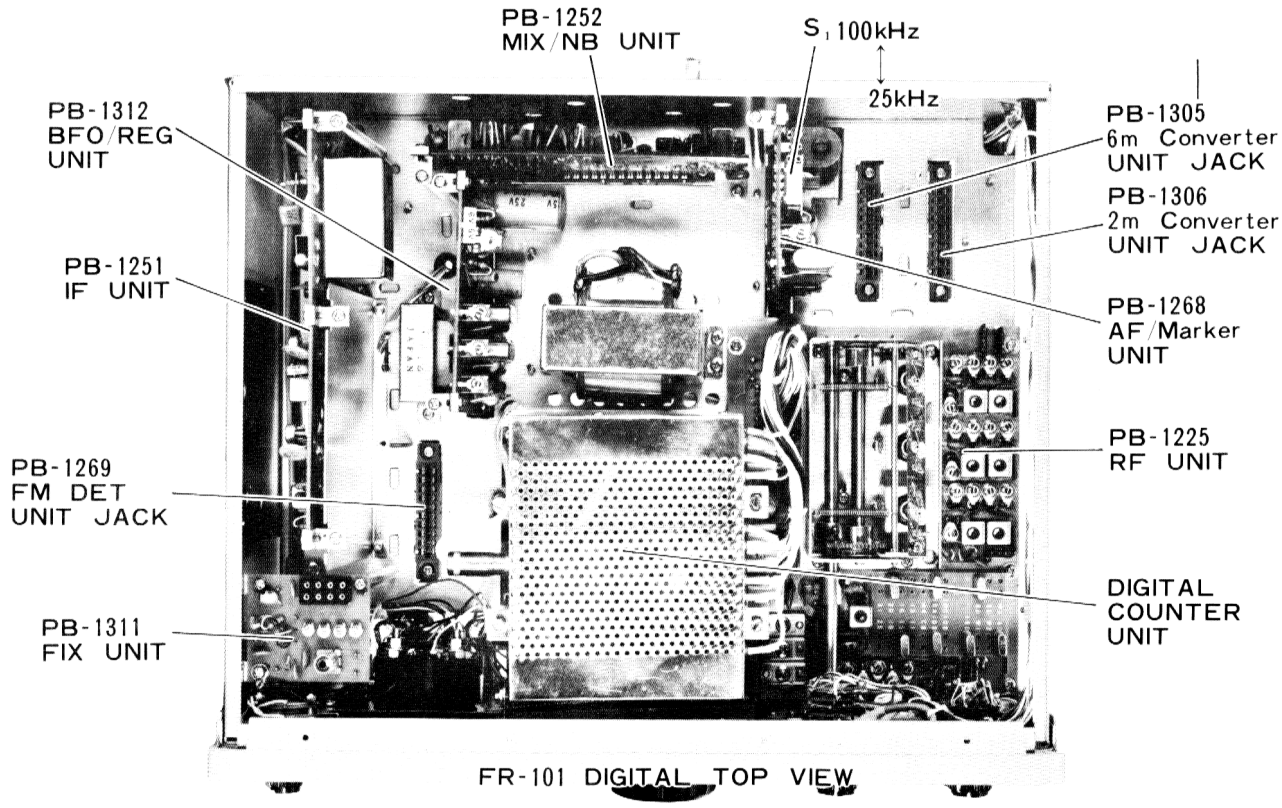
GENERAL DESCRIPTION

In the FR-101 digital receiver, a frequency counter is incorporated for accurate frequency readout by the display tubes. The frequency counter unit contains all elements including display tubes and frequency counter to display received frequencies.

The VFO frequency of 8.7 to 9.2 MHz is converted to 13.0 to 13.5 MHz. The diode matrix circuit, consisting of D1 through D49, converts this frequency into the actual received frequency which corresponds to the setting of the BAND switch.

When the VFO frequency is outside of its range, the display tubes flicker showing out of band operation. When the blue button switch on the front panel of the receiver is depressed, the last digit, 100 Hz display tube, is disappeared to avoid the annoyance of flicker.

The display does not function when the DC voltage is used for power source.



FR-101 DIGITAL TOP VIEW

CIRCUIT DESCRIPTION

The heterodyne oscillator, Q16, oscillates at 22.2 MHz, the second harmonic of the crystal frequency. The heterodyne mixer, Q15, produces a 13.0 to 13.5 MHz signal when the heterodyne oscillator signal is mixed with the VFO signal.

This frequency is shifted approximately ±3.7 kHz with a varicap diode connected between the crystal and ground in order to calibrate the tolerance of the receiver heterodyne oscillator. The control voltage to the varicap diode is supplied through the potentiometer marked CALIB on the front panel.

The 13.0 to 13.5 MHz signal is fed through a wave shaper Q1-1, time gate Q2-1, inverter Q2-2, and 10 Hz counter Q4, to the counter IC Q5 where 100Hz, 1 kHz, 10 kHz and 100 kHz BCD output signals are produced.

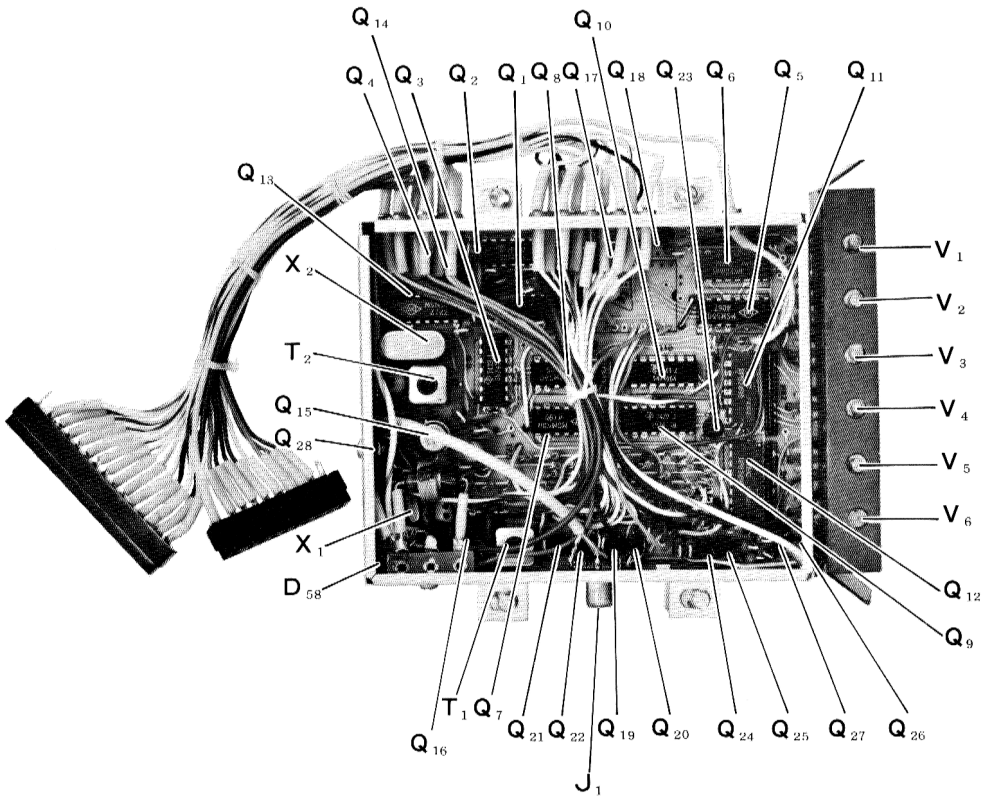
The standard frequency oscillator (clock) is composed of the 1.31072 MHz crystal controlled oscillator. The 1.31072 MHz output signal is divided by a binary counter, Q13, into a 5 Hz signal which is used as gate signal for Q2-1 and as blanking signal for Q3-2. The memory and reset pulses are produced by Q1-2, Q1-3, Q2-3, Q1-4, Q1-5 and Q1-6. The BCD output signal supplies an 8 segment output through the driver, Q6, to the display tubes, V1, V2 and V3. Q7, Q8, Q9 and Q10 add 500 kHz to the counter reading when the BAND switch is set to the band that starts from 500 kHz, such as 1.5, 3.5, 28.5, etc. Mega-Hertz indicators V5 and V6 are controlled by Q12 and Q24 through Q27. They select the proper cathode with the BAND switch position.

When the VFO frequency is outside its range, the output from Q14 controls Q10, D52, D53 and Q3-2 to produce the blanking pulses that flicker the display tubes.

The 13.5 volt DC voltage is regulated to 5 volts for the IC's and transistors by voltage regulator IC, Q28.

The display tube filament voltage is supplied through a 2.2 ohm resistor from the receiver AC voltage supply.

The display does not function when the DC voltage is used for power source.



DIAL CALIBRATION

For accurate frequency readout, when the receiving band is changed, it may be necessary to recalibrate the dial to compensate for the tolerance of the heterodyne crystals. Please refer to the "DIAL CALIBRATION" on page 8.

SSB MODE

(1) Set the BAND switch and the PRESELECTOR to the desired band, and the CLARIFIER switch to the OFF posotion.
(2) Push the CALIB switch on, and zero beat the main tuning dial against the 100 kHz or 25 kHz marker signal.
(3) Adjust the CALIB control until the counter shows an exact marker frequency. The CALIB control moves the counter frequency approximately ±3.7 kHz.

CW MODE

Follow the procedures described in the SSB MODE above, and then adjust the CALIB control until the counter reads 800 Hz higher than the actual zero beated marker signal frequency. For example, when the dial is zero beated to 21,025 kHz, the counter should be set to 21,025.8 kHz with the CALIB control.

AM-FM MODE

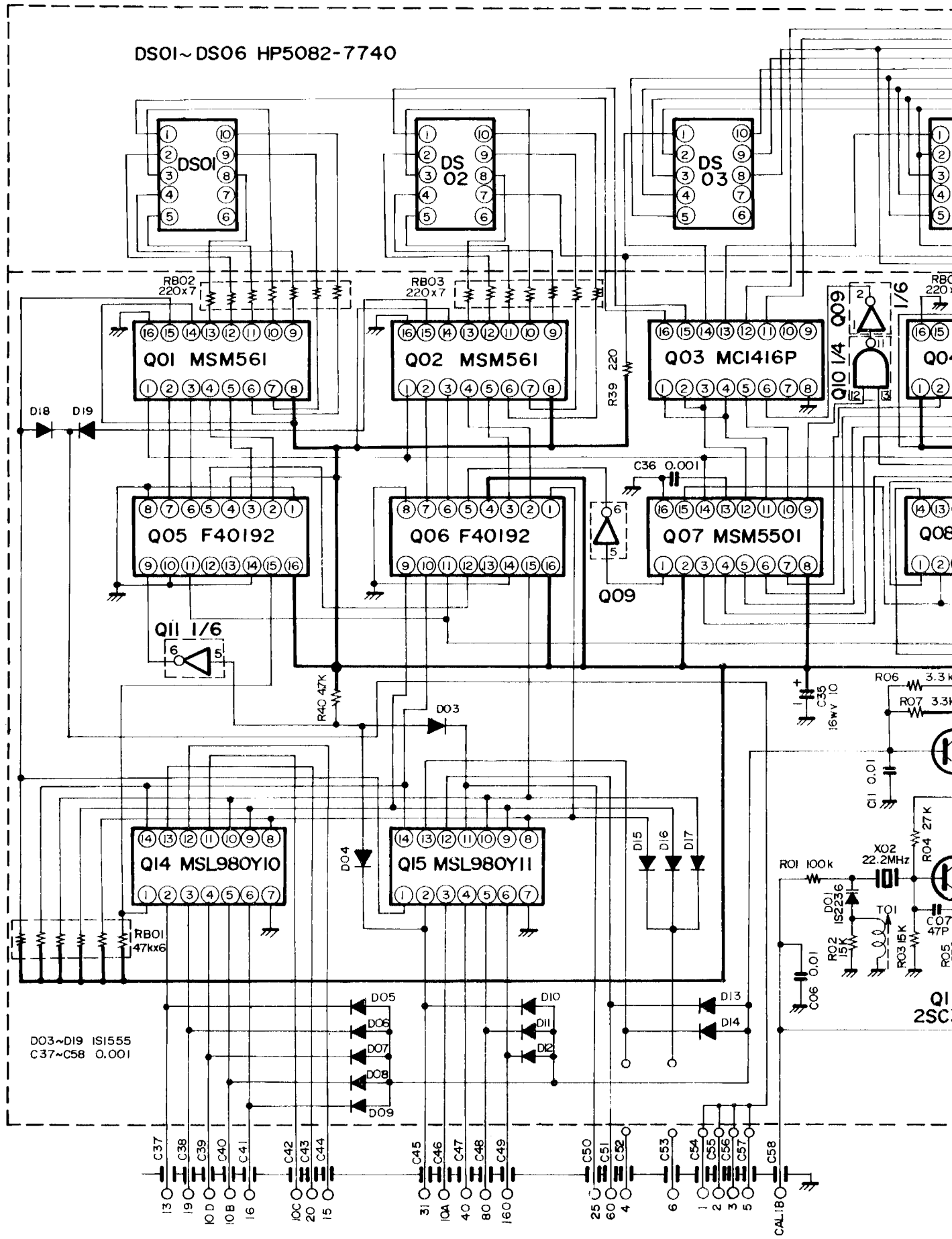
Since the zero beat method can not be used for the AM and FM modes, a maximum S-meter reading is used as described on page 8.

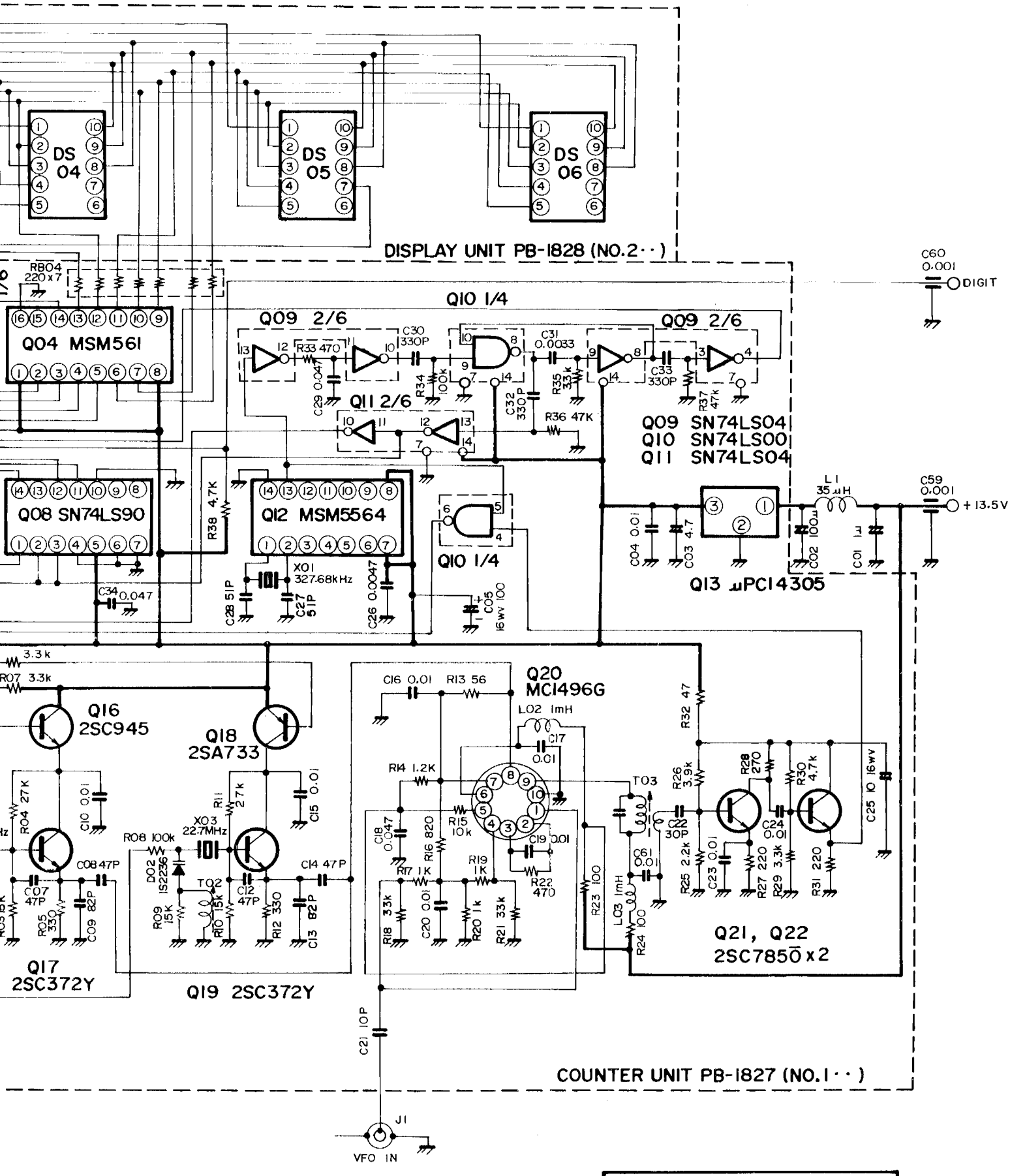
IMPORTANT NOTE

When the FR-101 digital receiver is used in transceive operation in conjunction with our FT-101/277 transceiver or FL-101 transmitter, the frequency counter reads the VFO frequency of either the receiver or transmitter. In other words, the counter shows the received frequency in the receive mode and the transmitted frequency in the transmit mode, regardless of the VFO in use. When the clarifier is used in transceive operation, the counter shows both your transmitting and receiving frequencies.

FR101 COUNTER UNIT PARTS LIST

PB PRINTED CIRCUIT BOARD		
1426(A~Z)	COUNTER CIRCUIT	
V	**DISPLAY TUBE**	
1~6	DIGITRON	LD-8062
Q	**IC & TRANSISTOR**	
2,3	TTL	SN7400N
1.	〃	SN7404N
9	〃	SN7475N
10	〃	SN7486N
4	〃	SN7490N
6,11,12	〃	μPB249D
7,8	C-MOS	MSM580
5	〃	MSM5502
13	〃	MSM5564
15	LINEAR	MC1496G
28	REGULATOR	MC7805P
14,16,17,19,21 23,25,27,29	TR	2SC373
18,20,22,24,26	〃	2SA564A(R)
D	**DIODE**	
1~50	Ge	1N60AM
56, 57	Si	1S1555
58	Varactor (FET)	2SK30A
X	**CRYSTAL**	
1	HC-18/U	11.100MHz
2	HC-6/U	1.31072MHz
R	**RESISTOR**	
	CARBON FILM	
42	¼W	56Ω
29,40,41	〃	100Ω
27	〃	180Ω
4,5	〃	220Ω
39	〃	470Ω
10	〃	560Ω
33	〃	820Ω
1,7,34,36,37	〃	1KΩ
31	〃	1.2KΩ
13,16,19,22,24,30	〃	2.2KΩ
2	〃	5.6KΩ
6,8,9,11,21,23,32	〃	10KΩ
3,12,15,18	〃	22KΩ
35,38	〃	33KΩ
14,17,2,,25,26,28 20	〃	100KΩ
	CARBON COMPOSITION	
43	½W	2.2Ω
RB	**BLOCK RESISTOR**	
1,2,3	CENTER COMMON	8×100KΩ
C	**CAPACITOR**	
	DIPPED MICA	
1,2,13	50WV	50PF
50	〃	60PF
9	〃	100PF
10	〃	150PF
4	〃	200PF
7	〃	300PF
6	〃	350PF
	CERAMIC DISC	
8,11,14,16,17	50WV	0.01μF
18,19,20,21,48		
3,12,15,22,24,46	50WV	0.047μF
	CERAMIC FEED THRU	
25~45,49	500WV	1000PF
	MYLAR	
5	50WV	0.003μF
	ELECTROLYTIC	
47	16WV	1μF
23	16WV	100μF
TC	**TRIMMER CAPACITOR**	
1	ECV 1ZW	20P50
L	**INDUTOR**	
1	TV-245	250μH
2		10μH
3,4		1mH
5	10K80T	35μH
T	**TRANSFORMER**	
1	OSC	
2	OUT PUT	
P	**PLUG**	
1	128-15-10-281S	
2	128-10-10-281S	
3	US PIN PLUG	SQ 4052
J	**JACK**	
1	US PIN JACK	SQ 3052


DS01~DS06 HP5082-7740
DS01
DS 02
DS 03
RB02 220x7
RB03 220x7
Q01 MSM561
Q02 MSM561
Q03 MCI416P
Q10 1/4
Q09 1/6
R39 220
D18
D19
C36 0.001
Q05 F40192
Q06 F40192
Q07 MSM5501
Q09
Q11 1/6
R40 47K
D03
C35 16wv 10
R06 3.3K
R07 3.3K
C11 0.01
Q14 MSL980Y10
Q15 MSL980Y11
D04
D15
D16
D17
R04 27K
R01 100k
XO2 22.2MHz
D01 IS2236
T01
C07 47P
R02 15K
R03 15K
C06 0.01
RB01 47kx6
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D03~D19 IS1555
C37~C58 0.001
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
C57
C58
13
19
10D
10B
16
10C
20
15
31
10A
40
80
160
25
60
4
6
1
2
3
5
CAL18



FR-101

COUNTER UNIT DIAGRAM


YAESU