

Figure 7

133.30 ~ 137.29 MHz

PB-1757 (PLL UNIT)

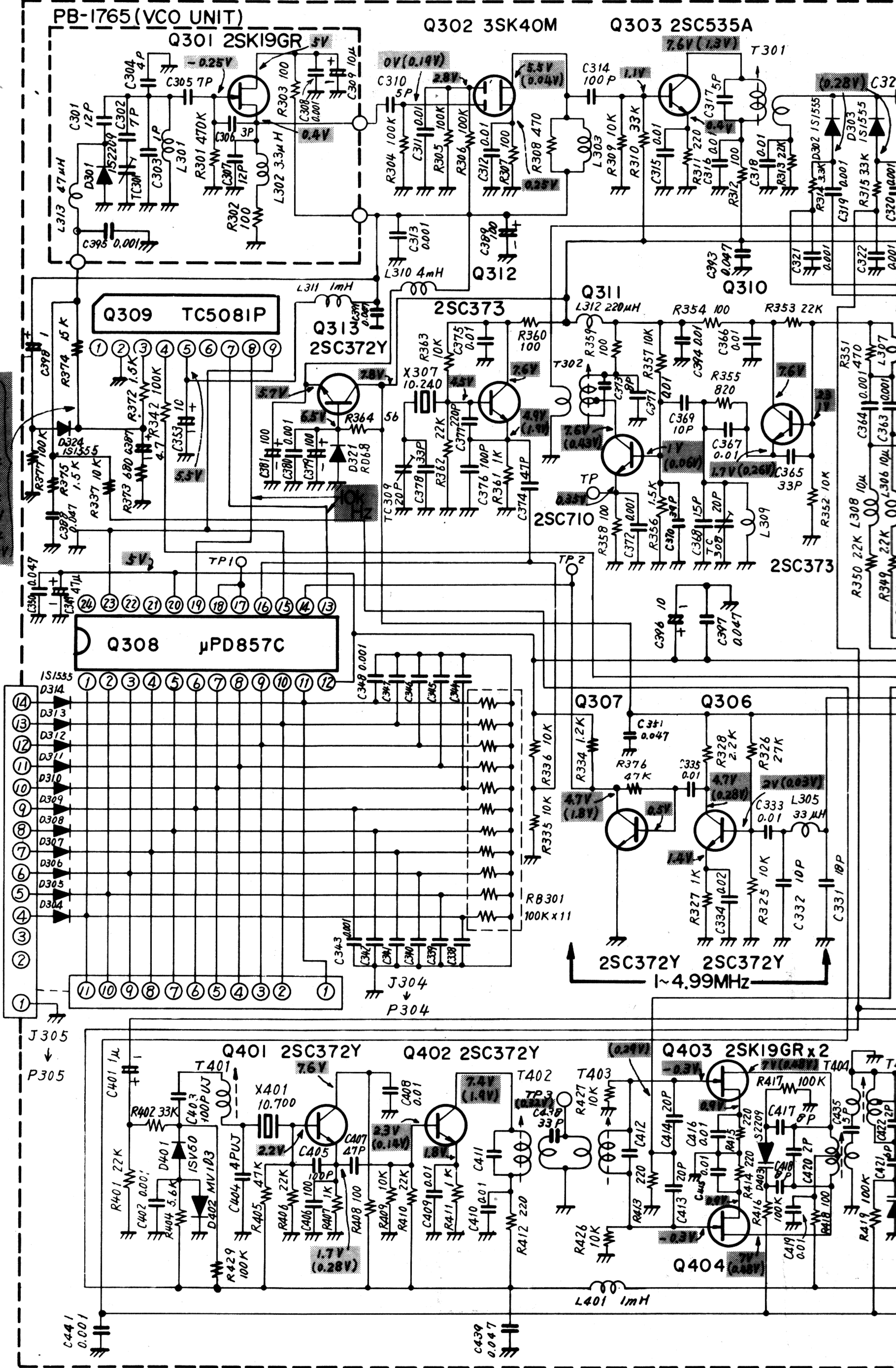
PB-1765 (VCO UNIT)

Q302 3SK40M

Q303 2SC535A

Q301 2SK19GR

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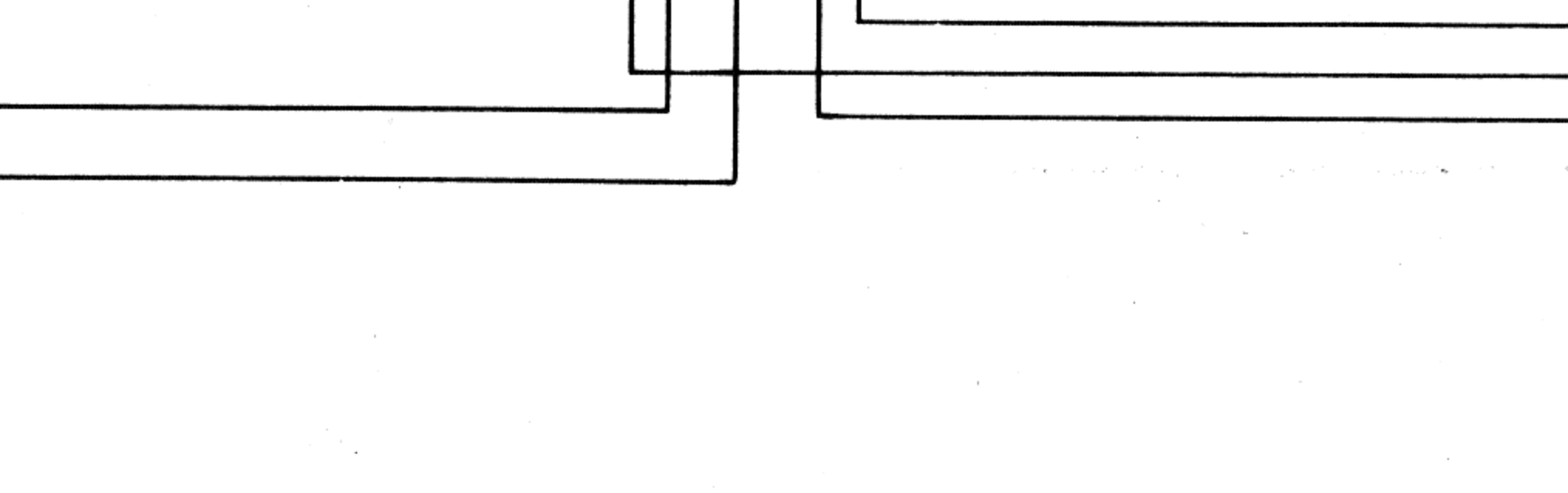
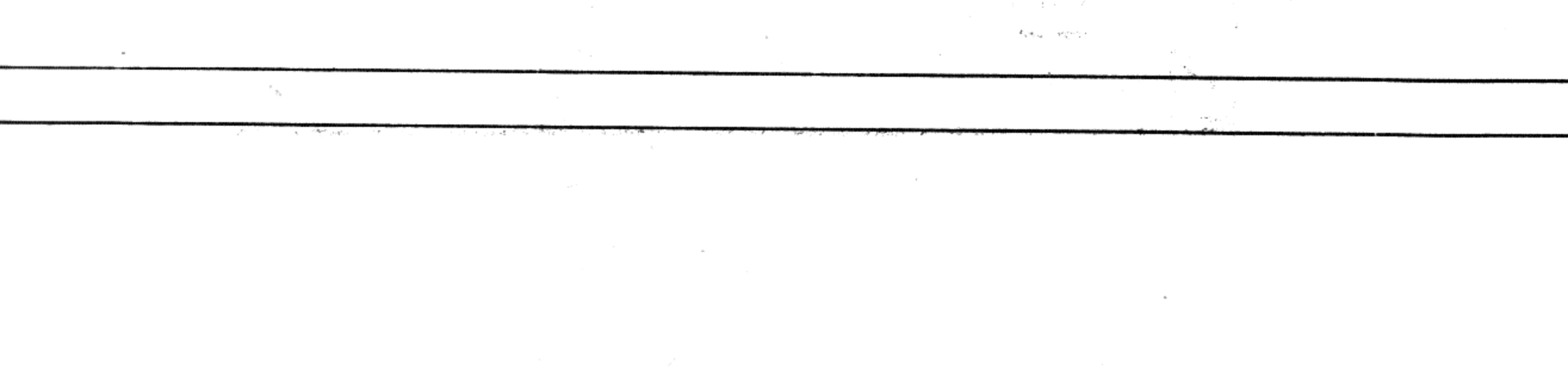
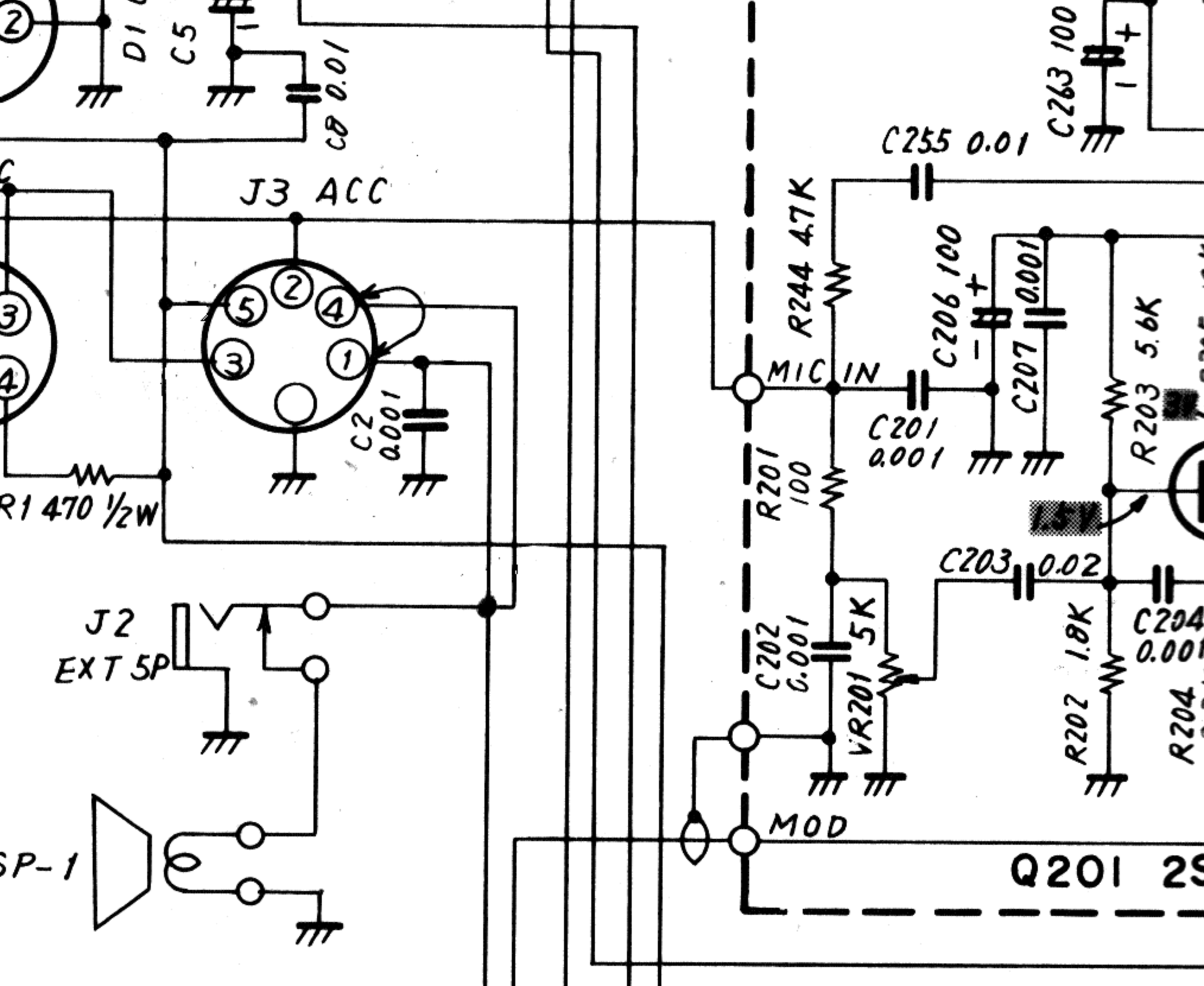
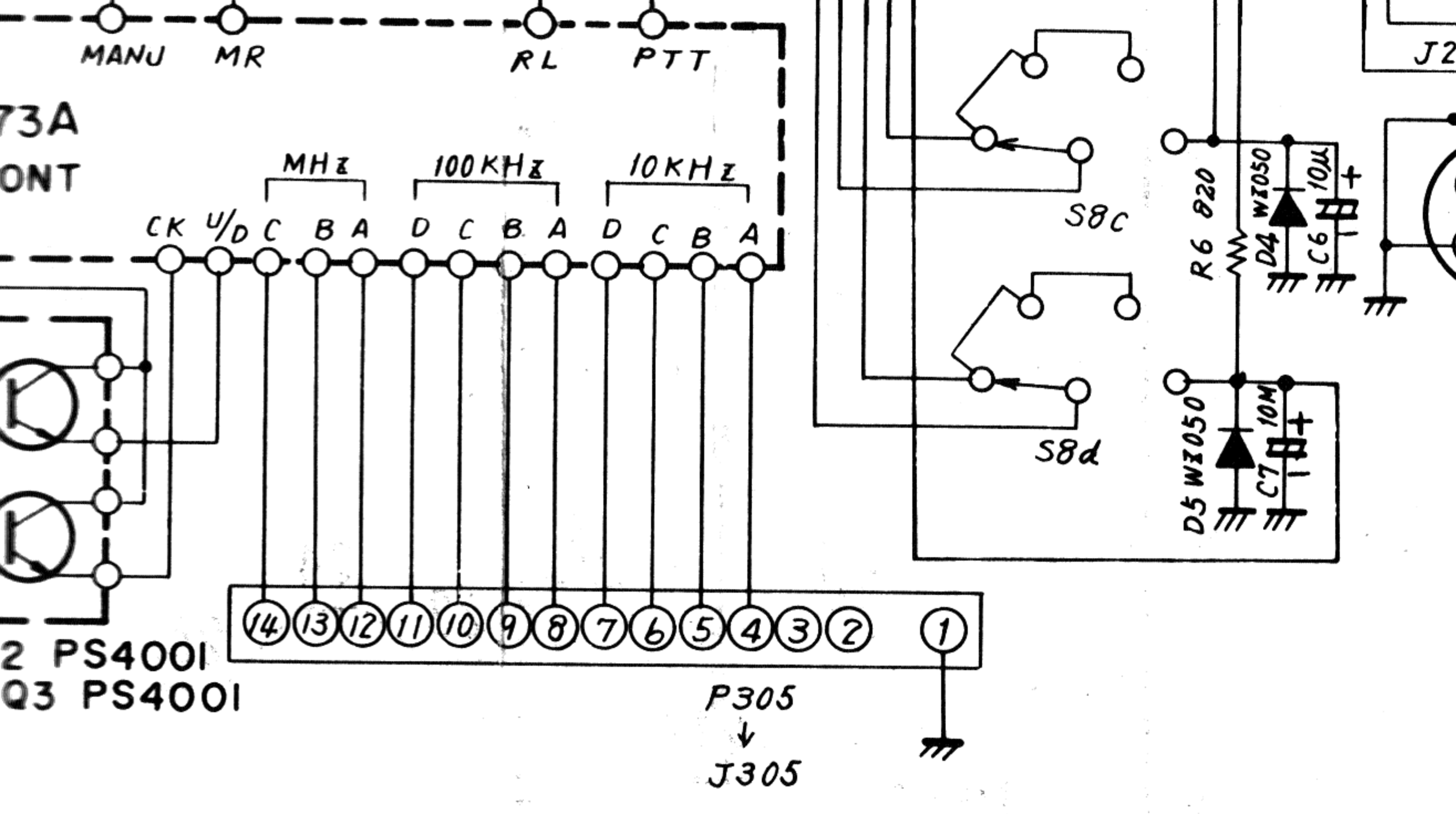
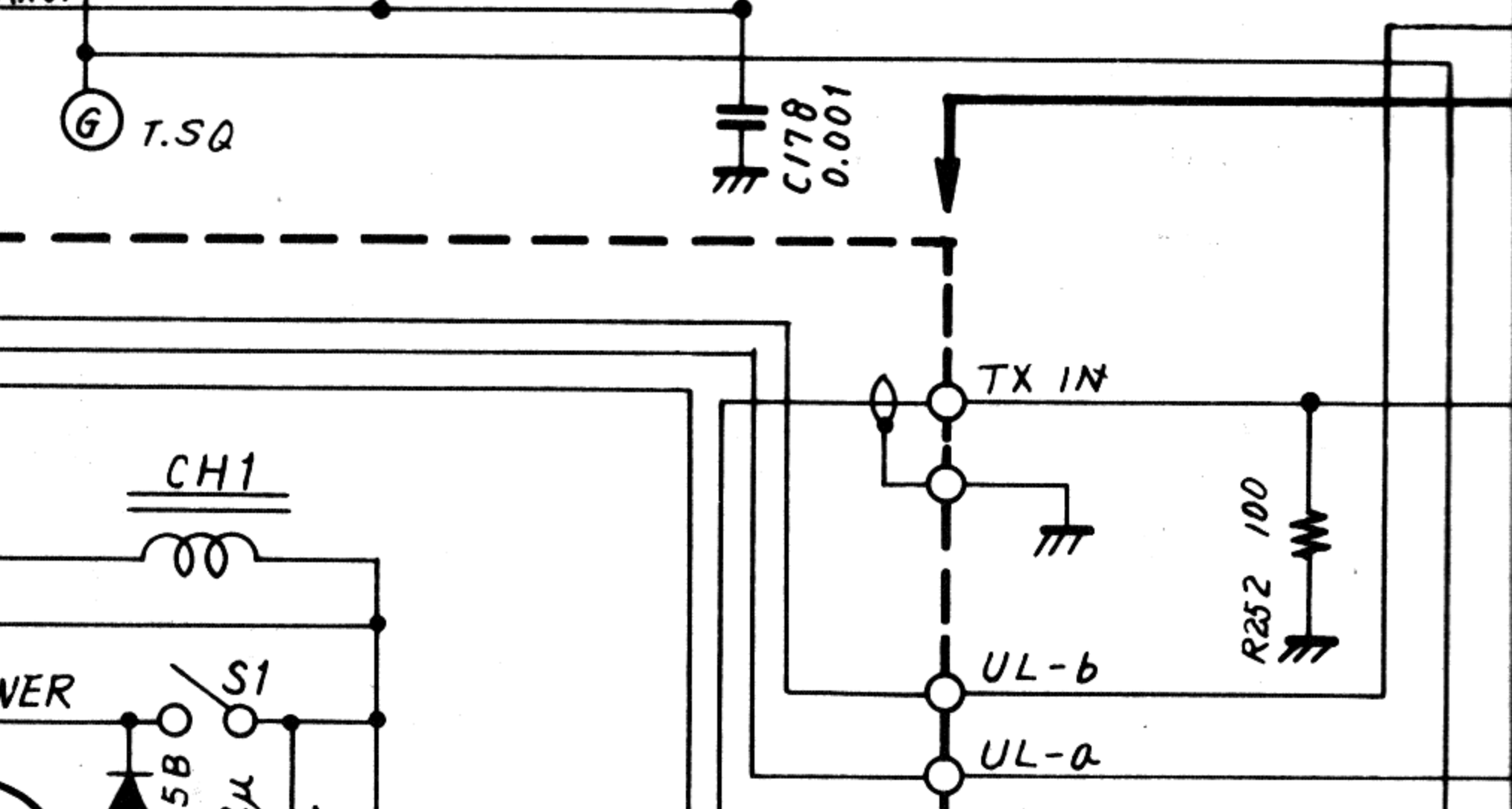
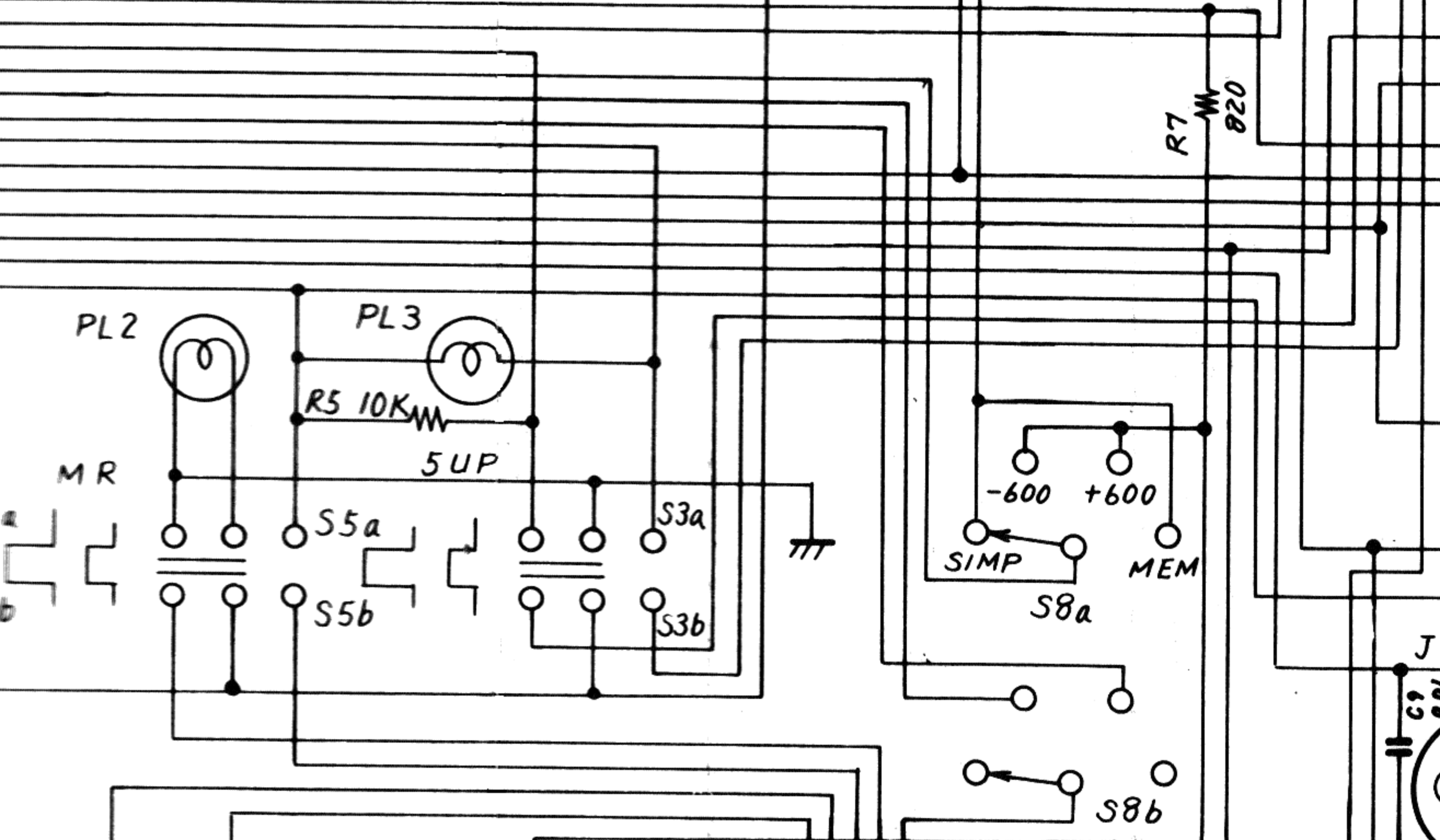
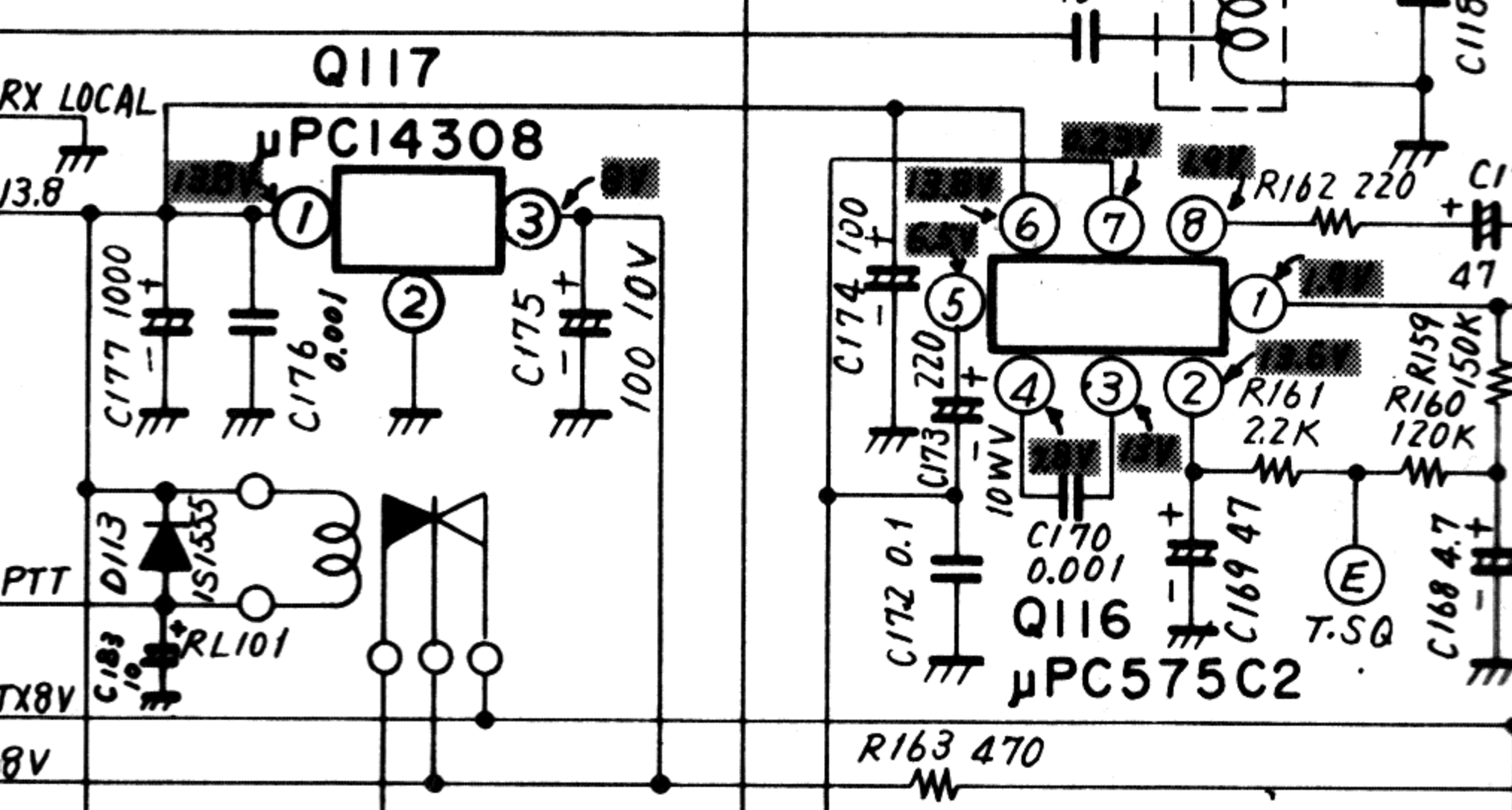
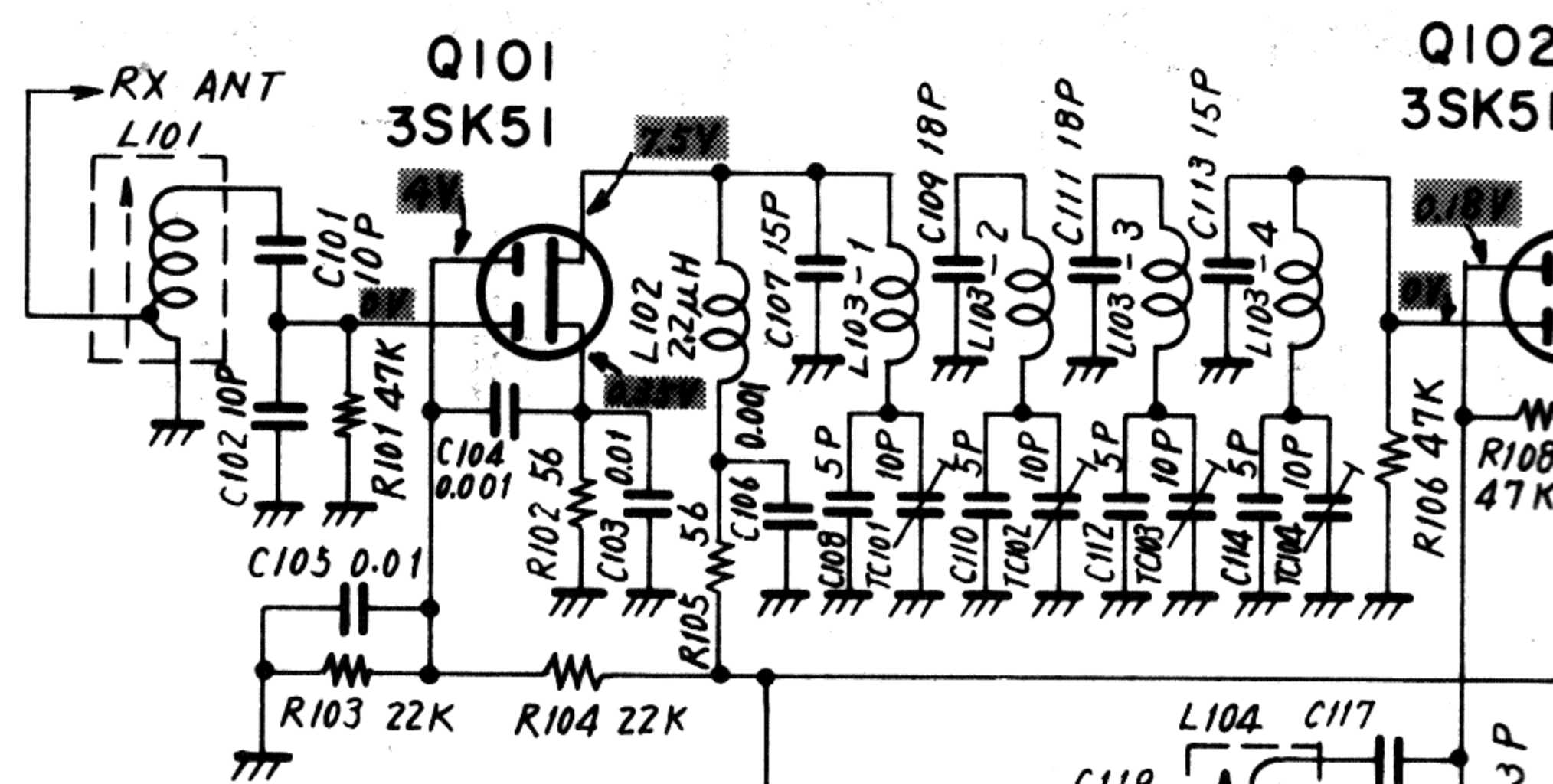
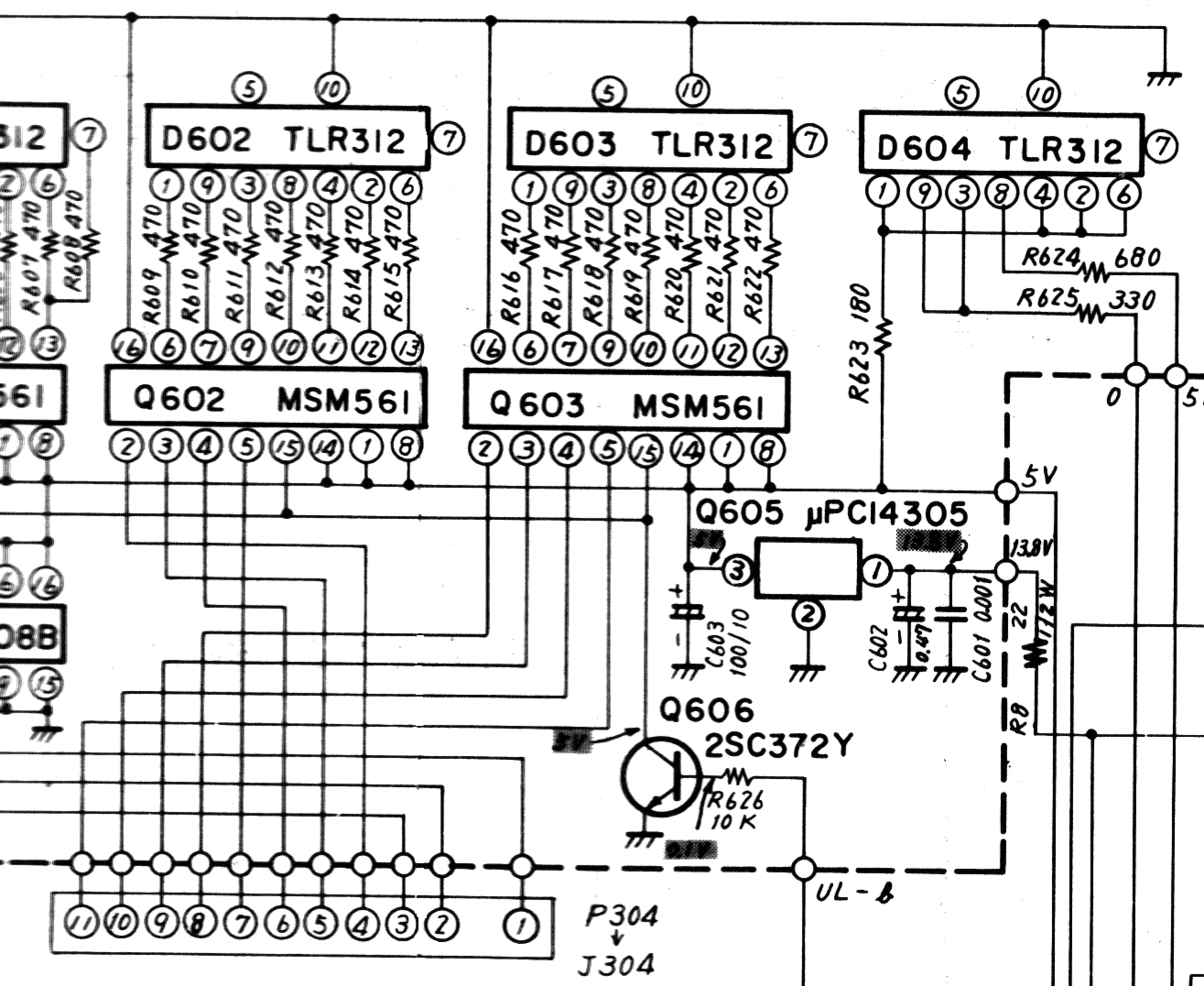
133.30 MHz
134.00 MHz
134.70 MHz
135.40 MHz
136.10 MHz
136.80 MHz
137.29 MHz

10.7 MHz

-1759 (DISPLAY UNIT)

144.00MHz ~ 147.99MHz

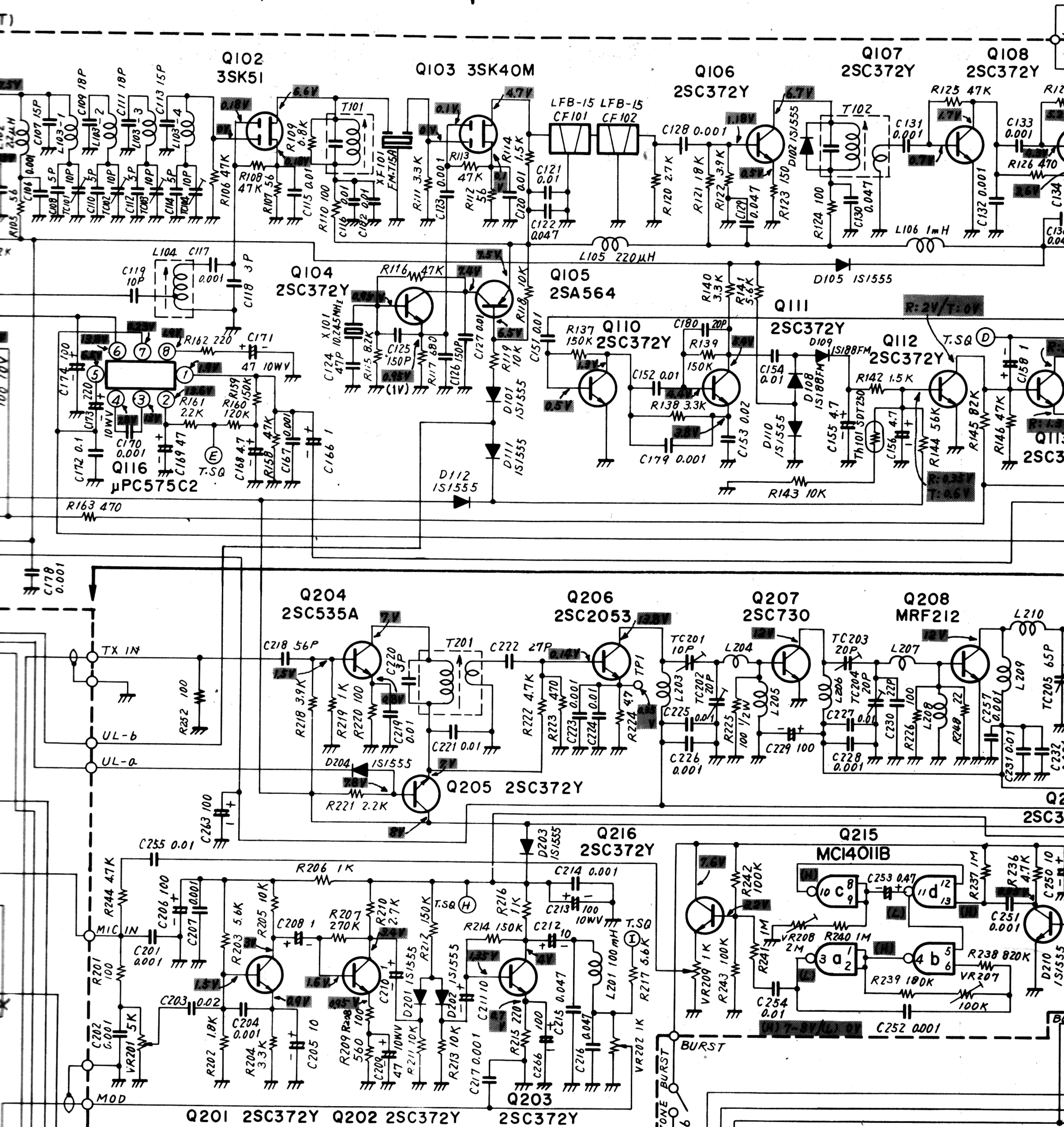
PB-1659 (MAIN UNIT)



Hz ~ 147.99MHz

10.7MHz

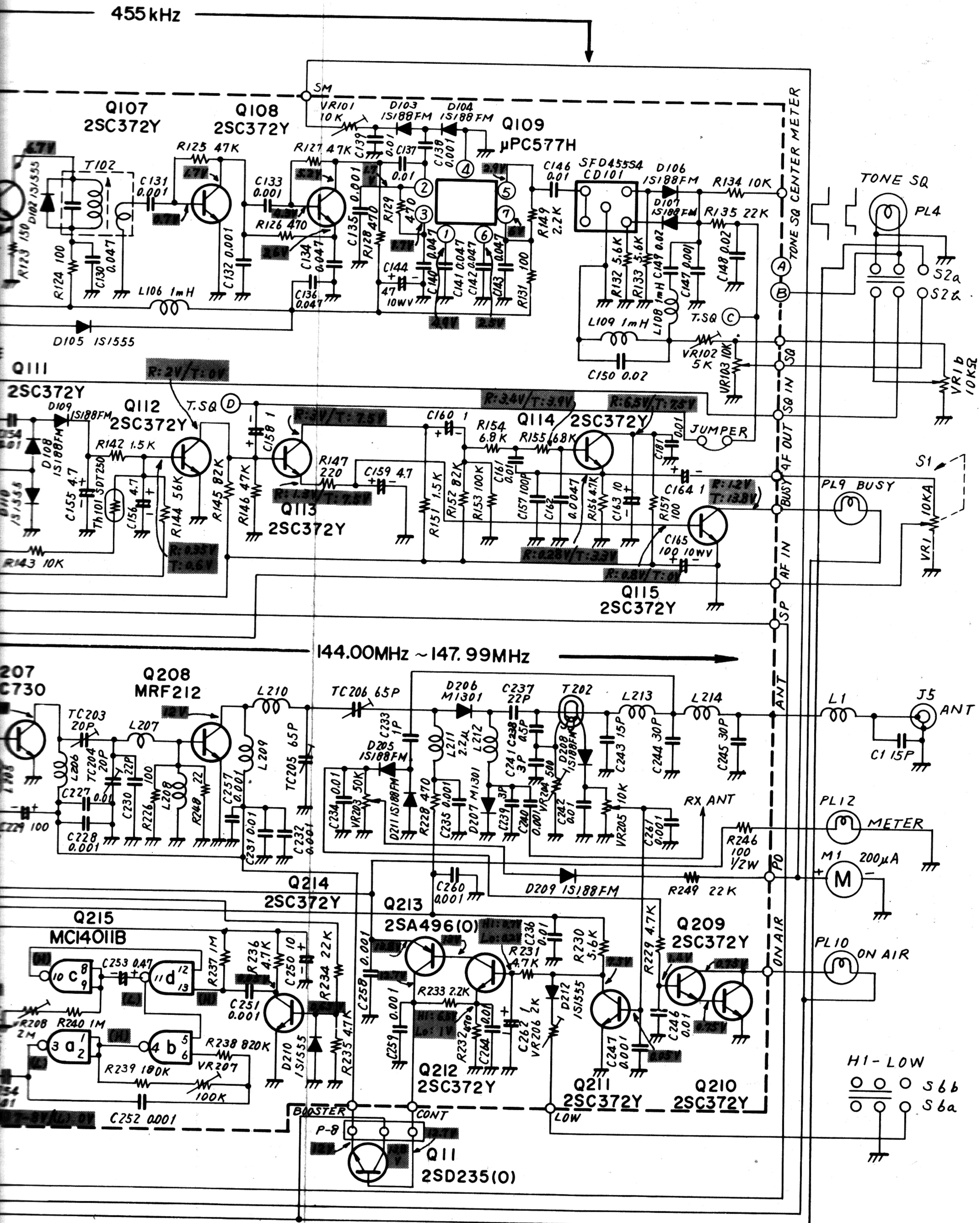
455 kHz



NOTES

- 1. ALL RESISTORS ARE IN 1/4W UNLESS NOTED OTHERWISE
- 2. ALL CAPACITORS ARE IN μF UNLESS NOTED OTHERWISE
- 3. ALL ELECTROLYTIC CAPACITORS ARE OTHERWISE NOTED
- 4. * VALUE IS NOMINAL.

— V DC VOLTAGE
 (—V) rms SIGNAL LEVEL
 MEASURED WITH VTVM.



- NOTES**
1. ALL RESISTORS ARE IN 1/4W UNLESS OTHERWISE NOTED.
 2. ALL CAPACITORS ARE IN µF UNLESS OTHERWISE NOTED.
 3. ALL ELECTROLYTIC CAPACITORS ARE 16WV UNLESS OTHERWISE NOTED
 4. * VALUE IS NOMINAL.

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FT-227R
CIRCUIT DIAGRAM

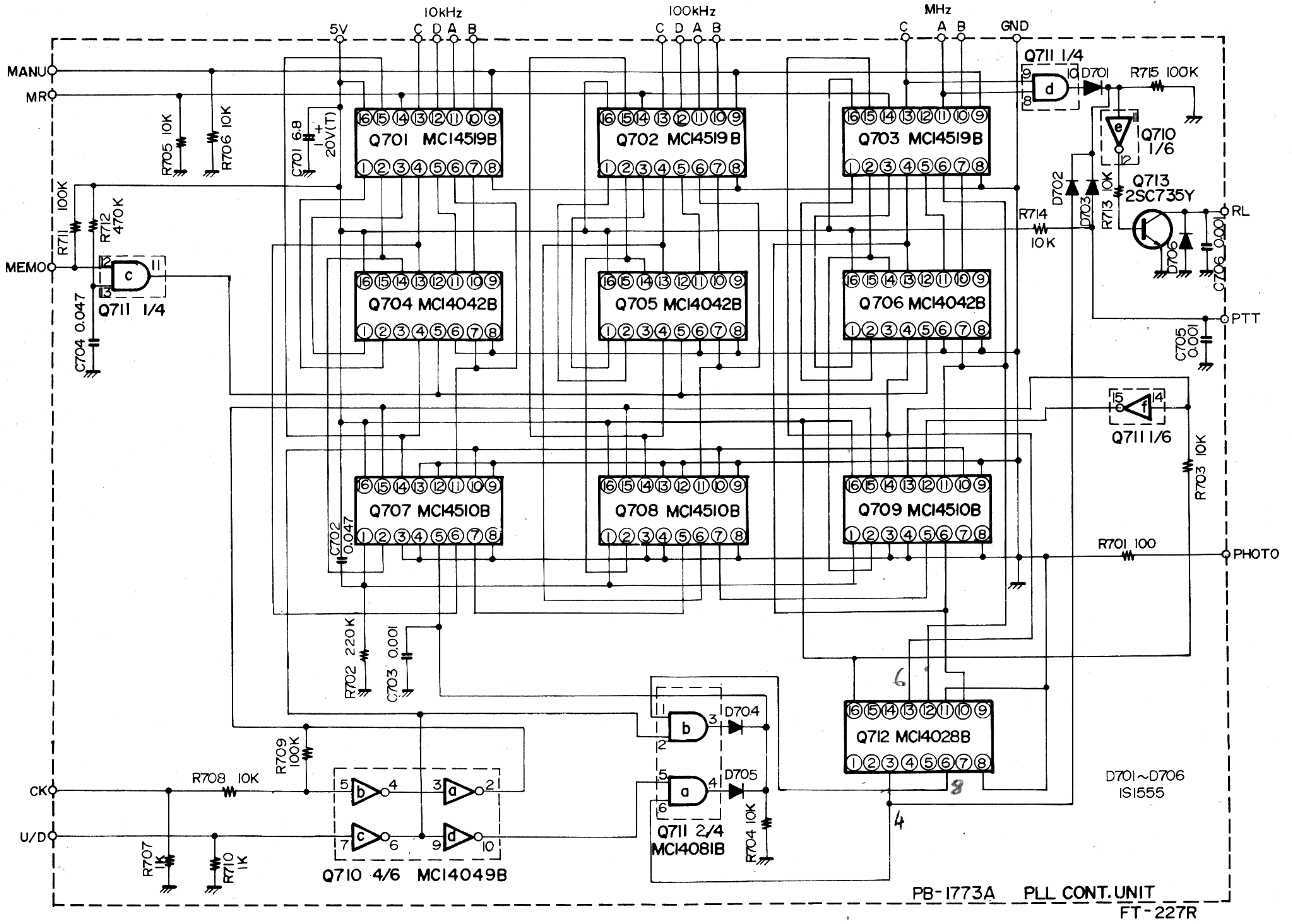
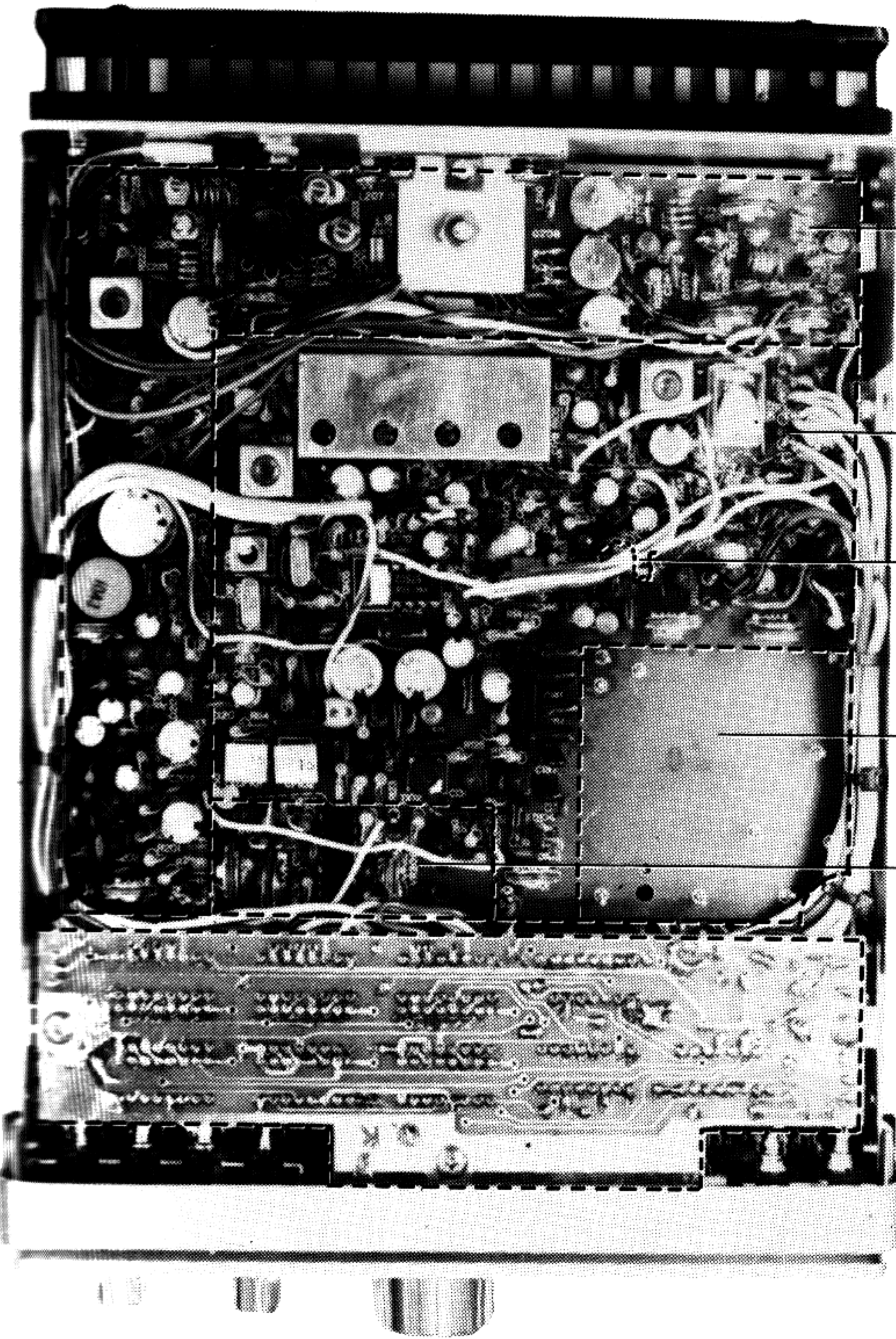


Figure 8

Q308 (μ PD857C) PROGRAMMABLE DIVIDER CODE

Q308 PROGRAMMABLE INPUT PIN →			1	2	3	4	5	6	7	8	9	10	11
P/J305 →			4	5	6	7	8	9	10	11	12	13	14
P/J304 →			11	10	9	8	7	6	5	4	3	2	1
FREQUENCY ↓	DIAL DISPLAY ↓	PROGRAMMABLE DIVIDER RATIO ↓	P ₁	P ₂	P ₃	P ₄	P ₅	P ₆	P ₇	P ₈	P ₉	P ₁₀	P ₁₁
144.00	4.000	1/100	0	0	0	0	0	0	0	0	1	0	0
4.01	4.010	1/101	1	0	0	0	0	0	0	0	1	0	0
4.02	4.020	1/102	0	1	0	0	0	0	0	0	1	0	0
4.03	4.030	1/103	1	1	0	0	0	0	0	0	1	0	0
4.04	4.040	1/104	0	0	1	0	0	0	0	0	1	0	0
4.05	4.050	1/105	1	0	1	0	0	0	0	0	1	0	0
4.06	4.060	1/106	0	1	1	0	0	0	0	0	1	0	0
4.07	4.070	1/107	1	1	1	0	0	0	0	0	1	0	0
4.08	4.080	1/108	0	0	0	1	0	0	0	0	1	0	0
4.09	4.090	1/109	1	0	0	1	0	0	0	0	1	0	0
144.10	4.100	1/110	0	0	0	0	1	0	0	0	1	0	0
4.11	4.110	1/111	1	0	0	0	1	0	0	0	1	0	0
4.12	4.120	1/112	0	1	0	0	1	0	0	0	1	0	0
4.13	4.130	1/113	1	1	0	0	1	0	0	0	1	0	0
4.14	4.140	1/114	0	0	1	0	1	0	0	0	1	0	0
4.15	4.150	1/115	1	0	1	0	1	0	0	0	1	0	0
4.16	4.160	1/116	0	1	1	0	1	0	0	0	1	0	0
4.17	4.170	1/117	1	1	1	0	1	0	0	0	1	0	0
4.18	4.180	1/118	0	0	0	1	1	0	0	0	1	0	0
4.19	4.190	1/119	1	0	0	1	1	0	0	0	1	0	0
144.20	4.200	1/120	0	0	0	0	0	1	0	0	1	0	0
4.30	4.300	1/130	0	0	0	0	1	1	0	0	1	0	0
4.40	4.400	1/140	0	0	0	0	0	0	1	0	1	0	0
4.50	4.500	1/150	0	0	0	0	1	0	1	0	1	0	0
4.60	4.600	1/160	0	0	0	0	0	1	1	0	1	0	0
4.70	4.700	1/170	0	0	0	0	1	1	1	0	1	0	0
4.80	4.800	1/180	0	0	0	0	0	0	0	1	1	0	0
4.90	4.900	1/190	0	0	0	0	1	0	0	1	1	0	0
145.00	5.000	1/200	0	0	0	0	0	0	0	0	0	1	0
145.01	5.010	1/201	1	0	0	0	0	0	0	0	0	1	0
145.02	5.020	1/202	0	1	0	0	0	0	0	0	0	1	0
145.03	5.030	1/203	1	1	0	0	0	0	0	0	0	1	0
145.04	5.040	1/204	0	0	1	0	0	0	0	0	0	1	0
145.05	5.050	1/205	1	0	1	0	0	0	0	0	0	1	0
145.06	5.060	1/206	0	1	1	0	0	0	0	0	0	1	0
145.07	5.070	1/207	1	1	1	0	0	0	0	0	0	1	0
145.08	5.080	1/208	0	0	0	1	0	0	0	0	0	1	0
145.09	5.090	1/209	1	0	0	1	0	0	0	0	0	1	0
145.10	5.100	1/210	0	0	0	0	1	0	0	0	0	1	0
145.20	5.200	1/220	0	0	0	0	0	1	0	0	0	1	0
145.30	5.300	1/230	0	0	0	0	1	1	0	0	0	1	0
145.40	5.400	1/240	0	0	0	0	0	0	1	0	0	1	0
145.50	5.500	1/250	0	0	0	0	1	0	1	0	0	1	0
145.60	5.600	1/260	0	0	0	0	0	1	1	0	0	1	0
145.70	5.700	1/270	0	0	0	0	1	1	1	0	0	1	0
145.80	5.800	1/280	0	0	0	0	0	0	0	1	0	1	0
145.90	5.900	1/290	0	0	0	0	1	0	0	1	0	1	0
146.00	6.000	1/300	0	0	0	0	0	0	0	0	1	1	0
147.00	7.000	1/400	0	0	0	0	0	0	0	0	0	0	1
147.99	7.990	1/499	1	0	0	1	1	0	0	1	0	0	1

※ 1 HIGH LEVEL (5V)
※ 0 LOW LEVEL (0V)



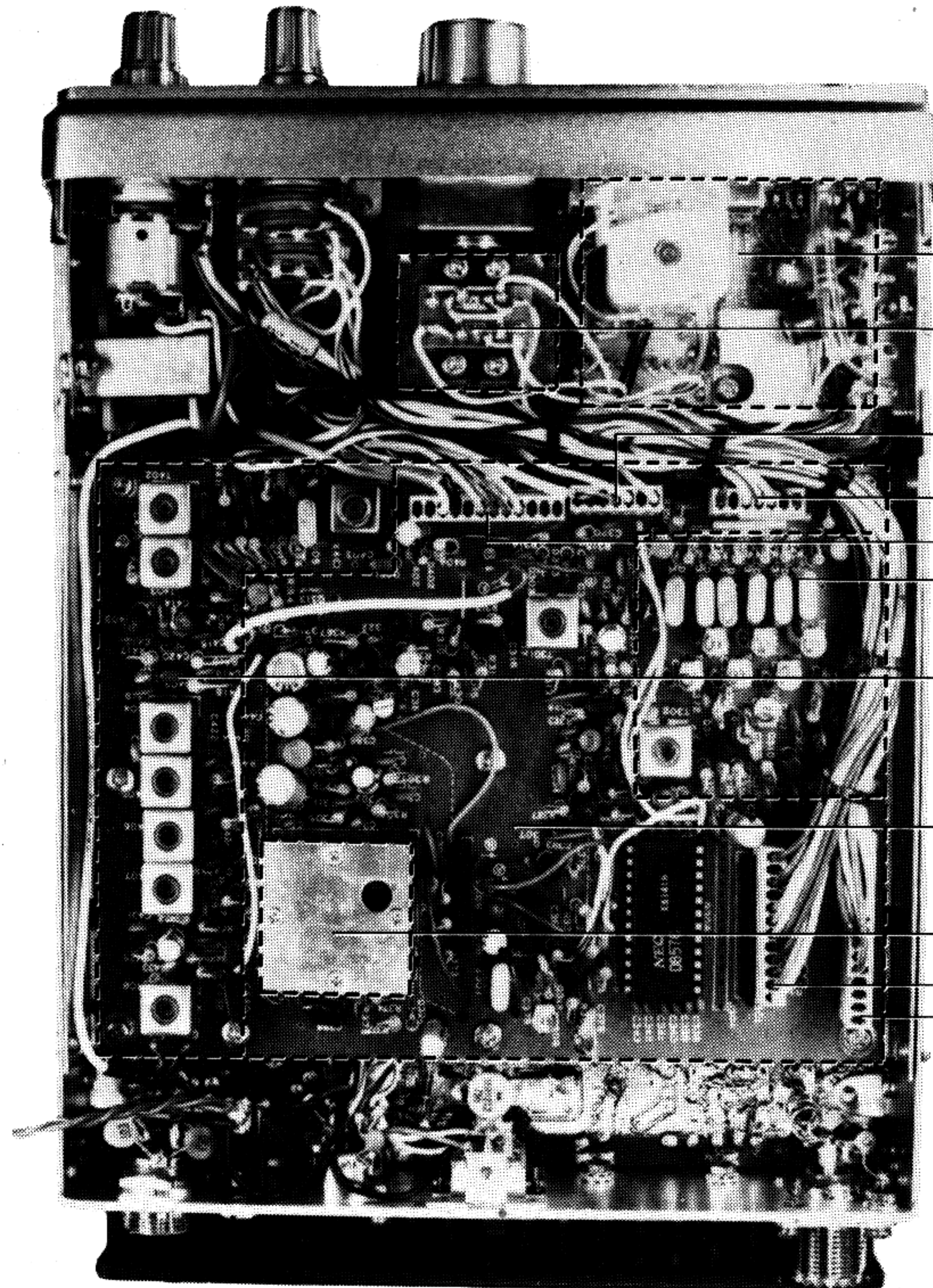
MAIN UNIT
TRANSMITTER
SECTION

MAIN UNIT
RECEIVER
SECTION

RED WIRE MUST BE CUT
WHEN TONE SQUELCH UNIT
IS INSTALLED.

TONE SQUELCH UNIT
(WHEN INSTALLED)

TONE BURST
SECTION



DISPLAY UNIT

CHANNEL SELECTOR
PHOTO INTERRUPTER
UNIT

P/J₃₀₁

P/J₃₀₂

P/J₃₀₃

PLL LOCAL
SECTION

MODULATOR
CONVERTER } SECTION

PLL SECTION

VCO SECTION

P/J₃₀₄

P/J₃₀₅

Figure 10 TOP VIEW

Figure 11 BOTTOM VIEW

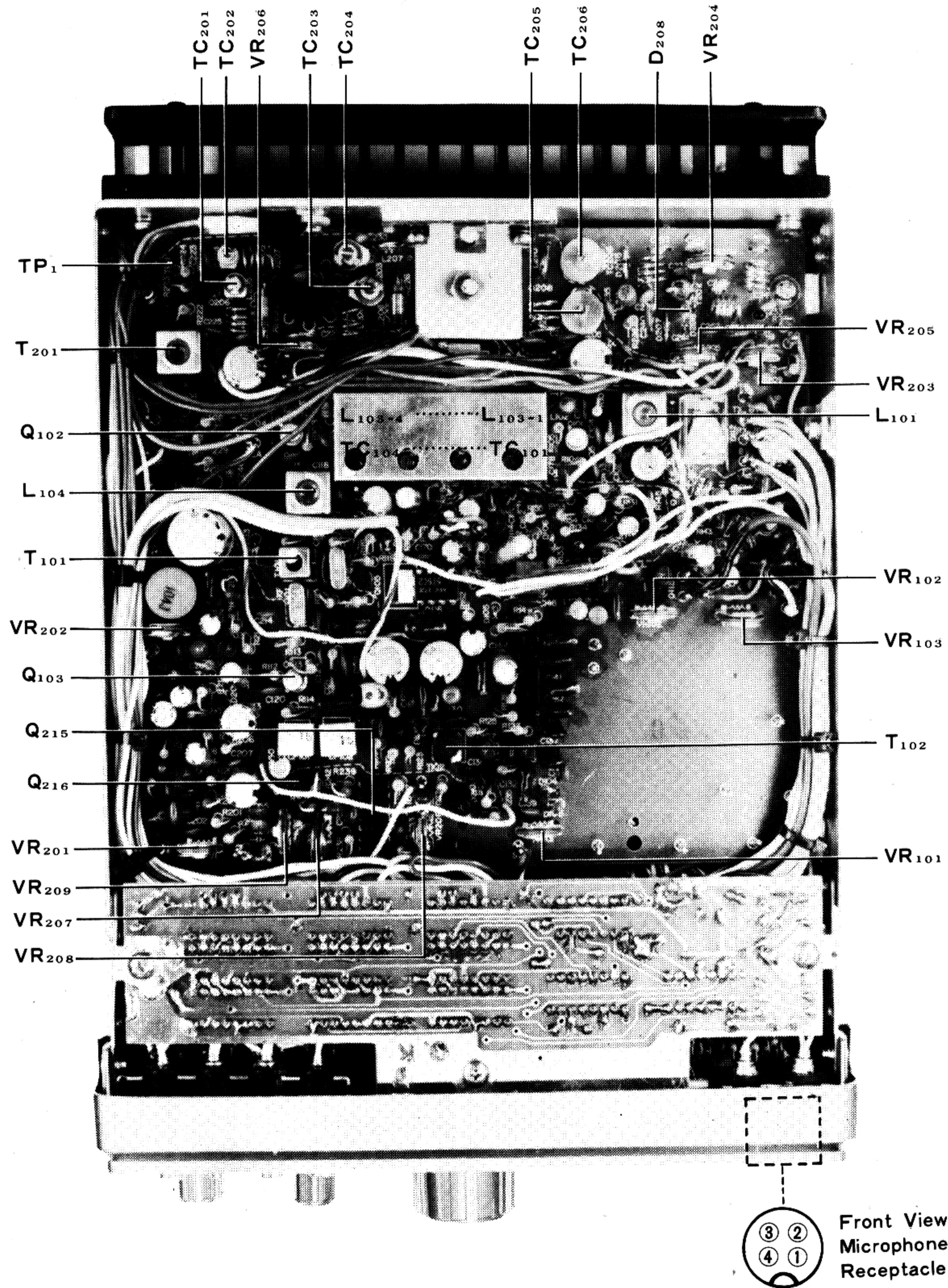


Figure 12

ALIGNMENT POINT

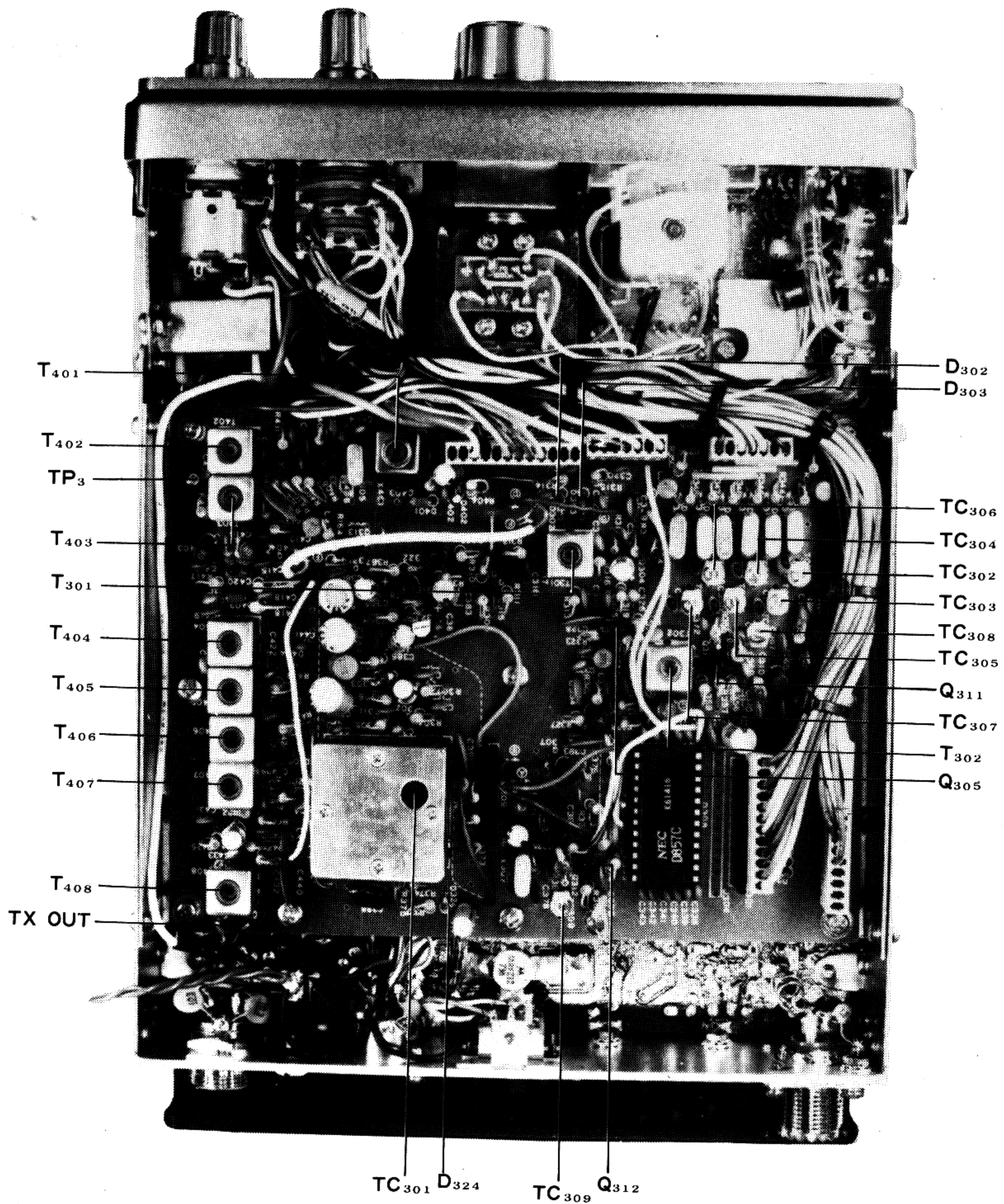


Figure 16 ALIGNMENT POINT

Optional tone squelch

The optional tone squelch unit has been set to 77 Hz operation at the factory, however, the tone squelch frequency can be chosen to any frequency between 70 Hz to 160 Hz by the setting of VR502. The transmitting level of the tone signal is set by VR504.

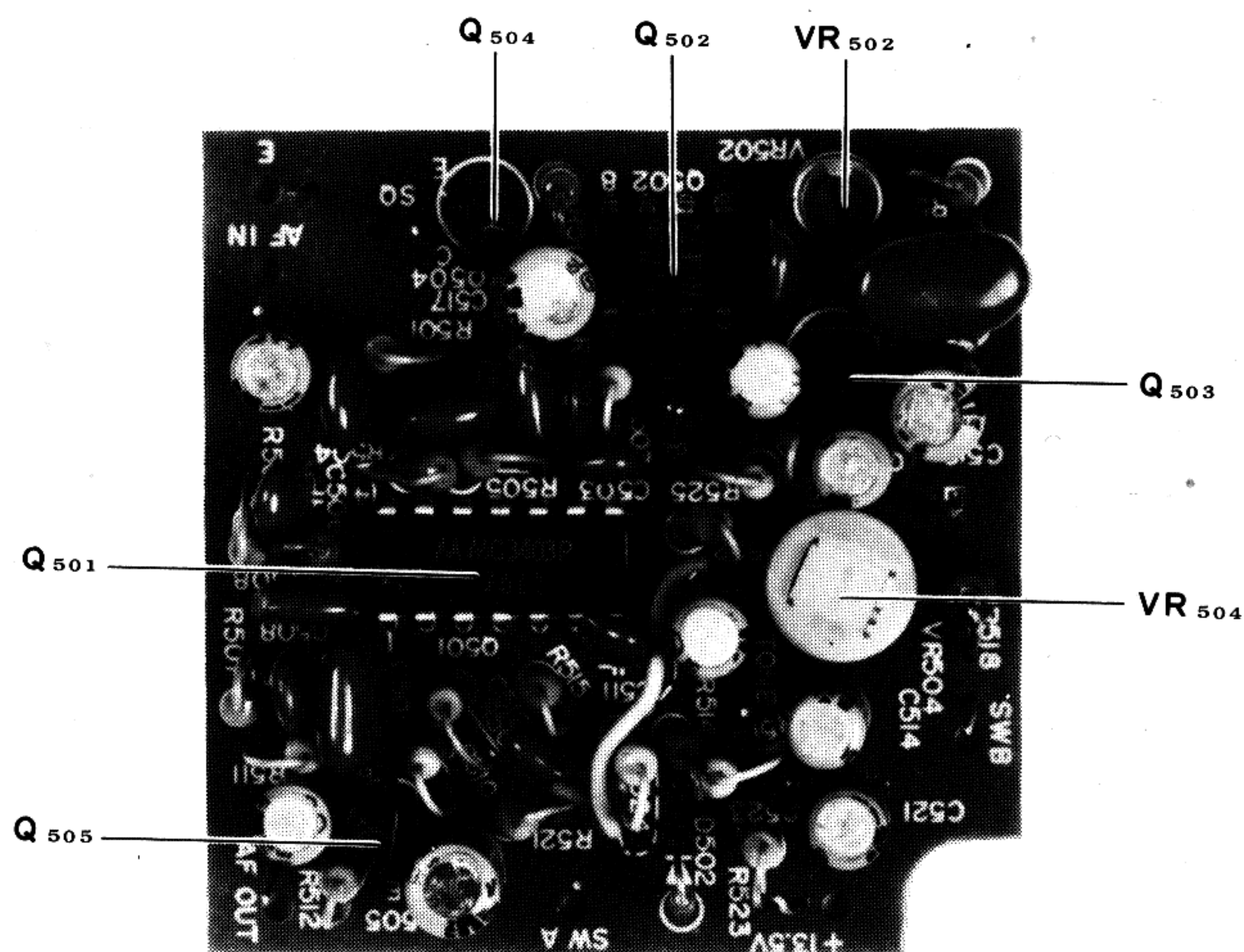
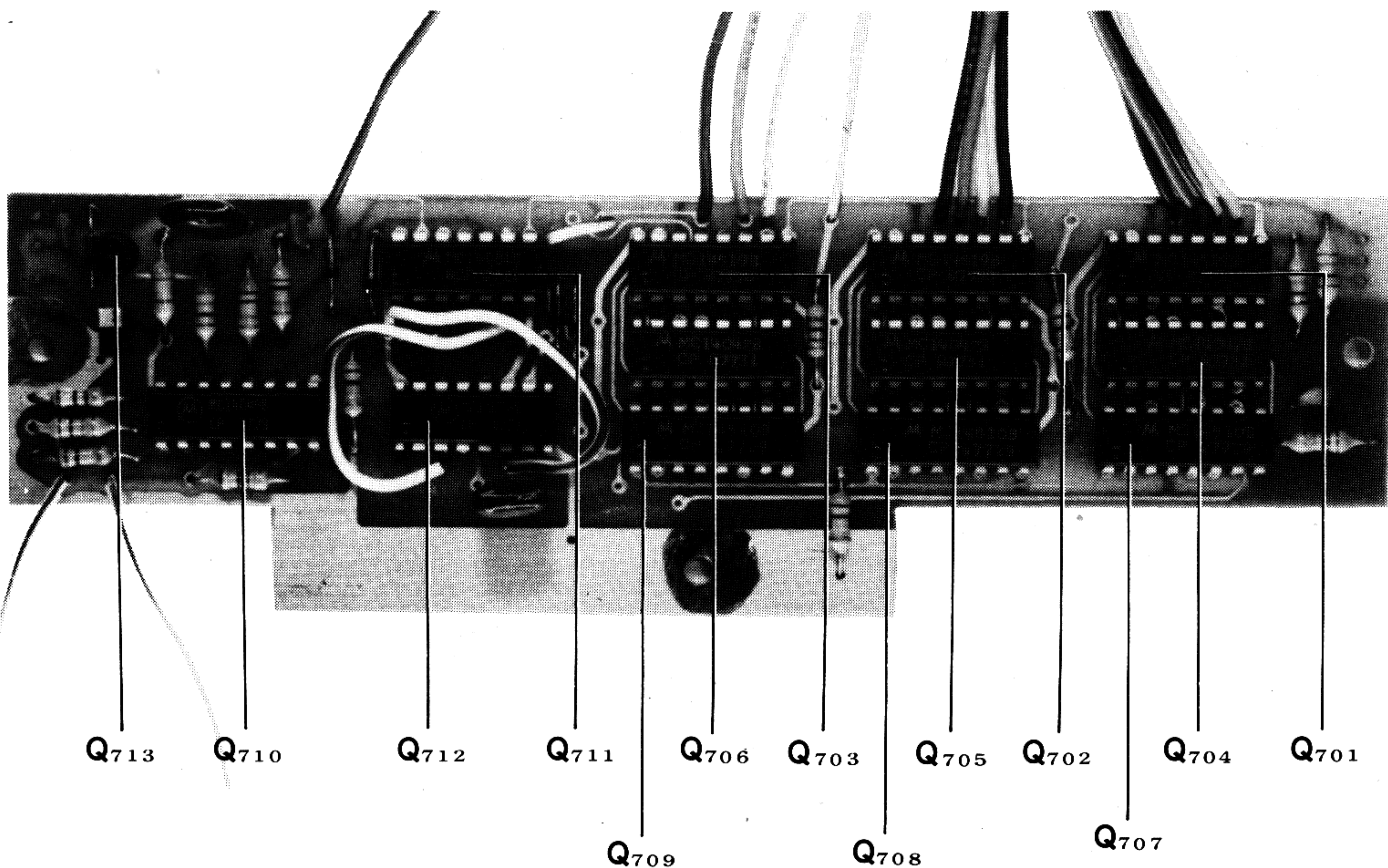
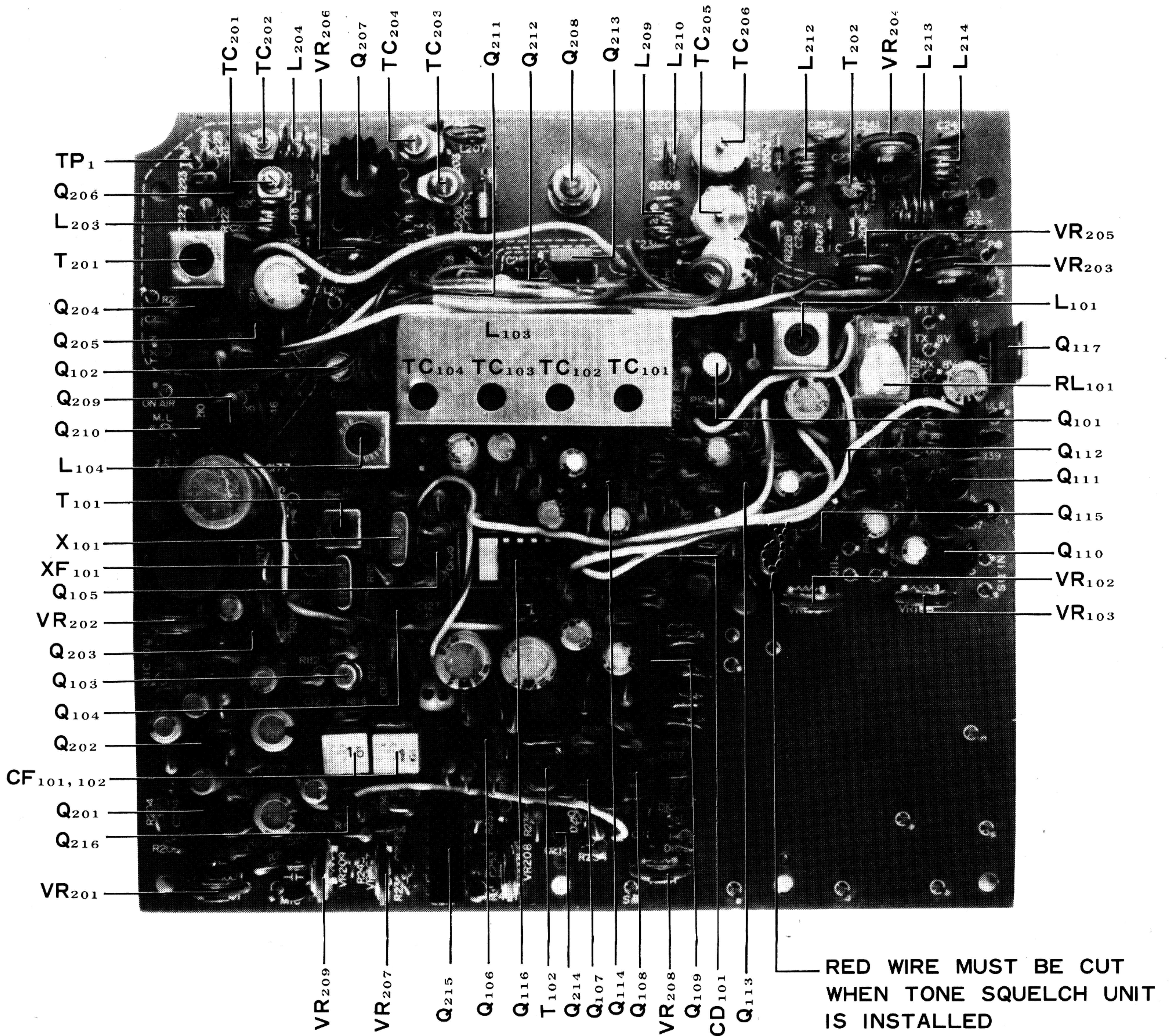
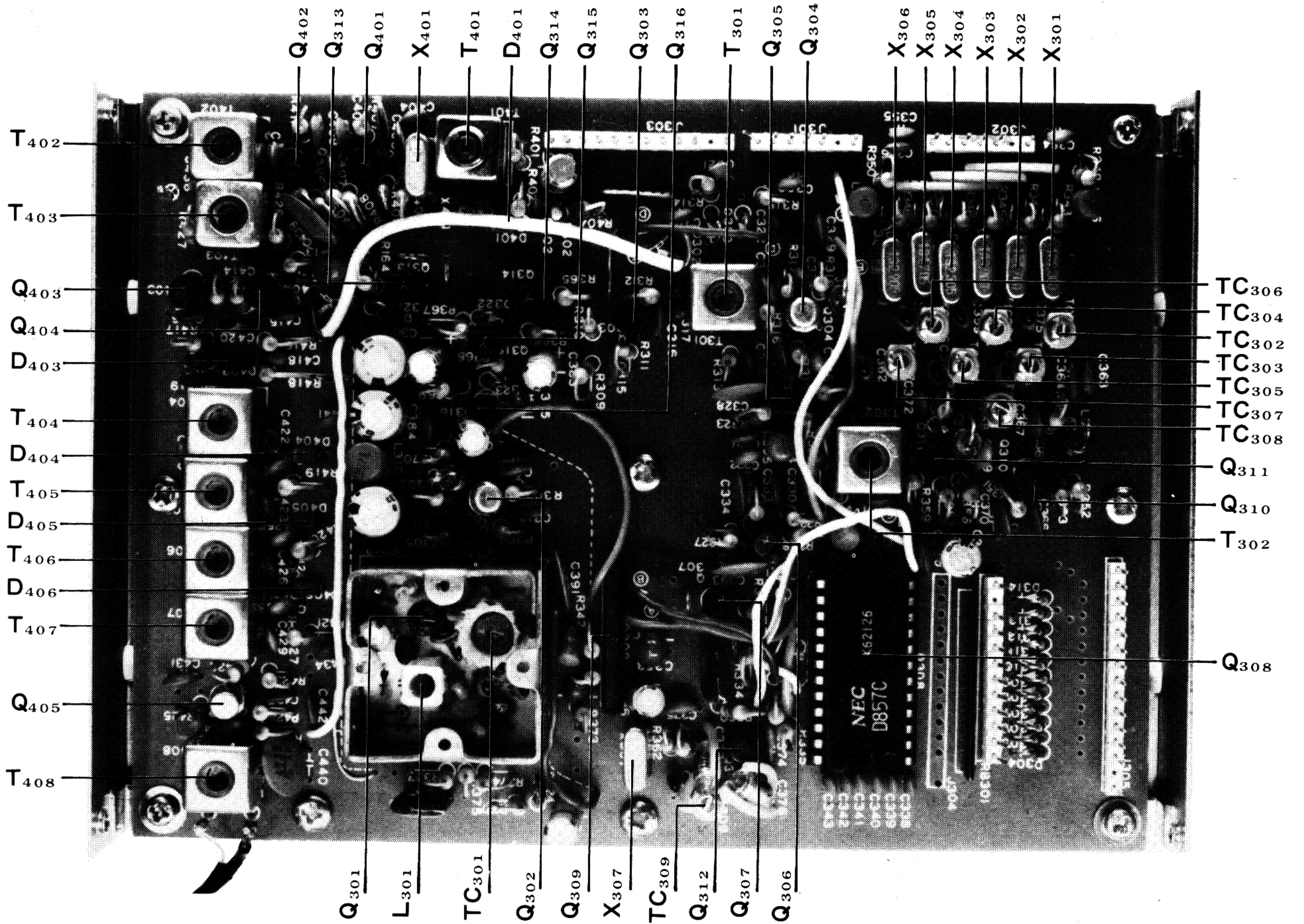


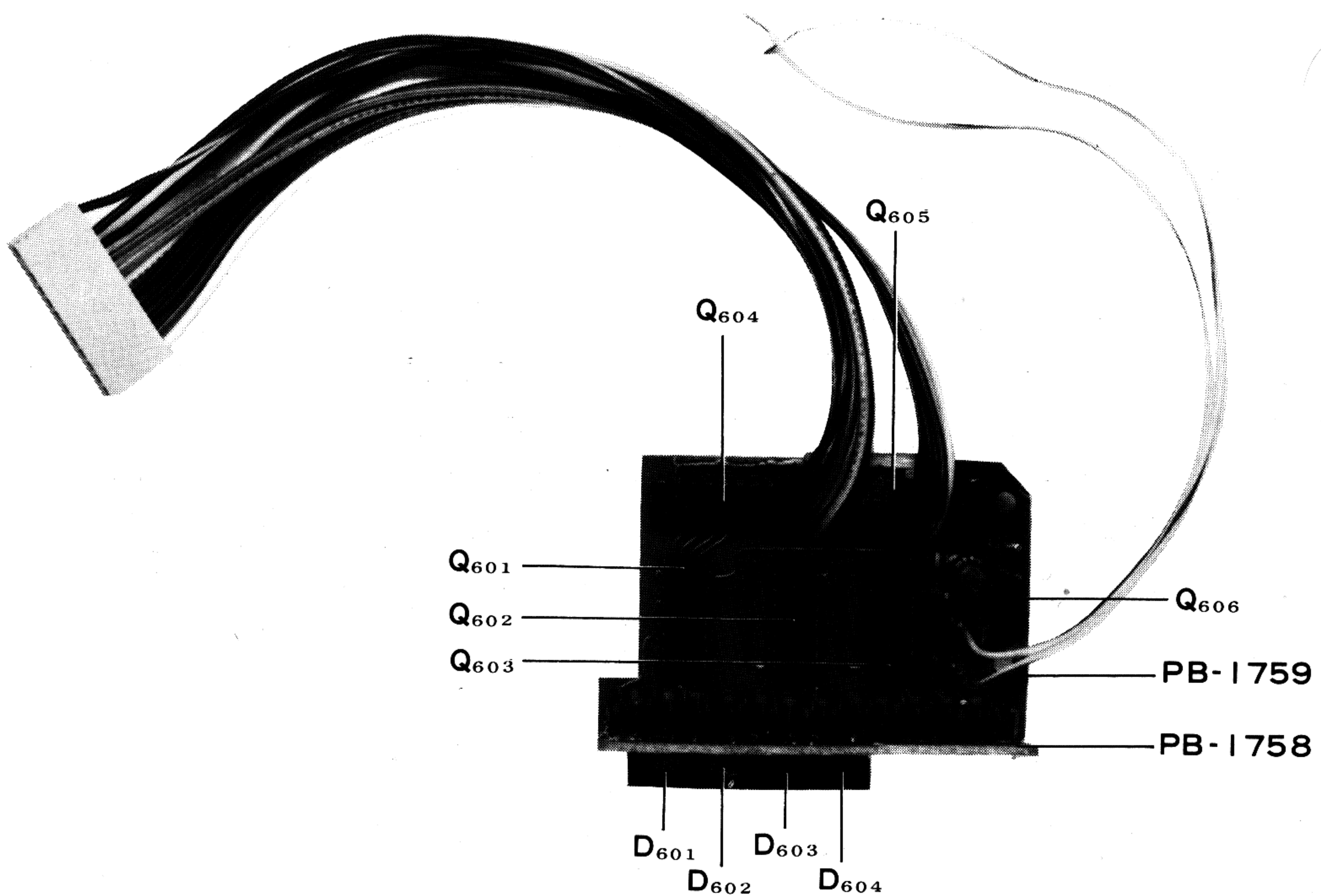
Figure 17



PLL CONTROL UNIT



PLL UNIT



DISPLAY UNIT