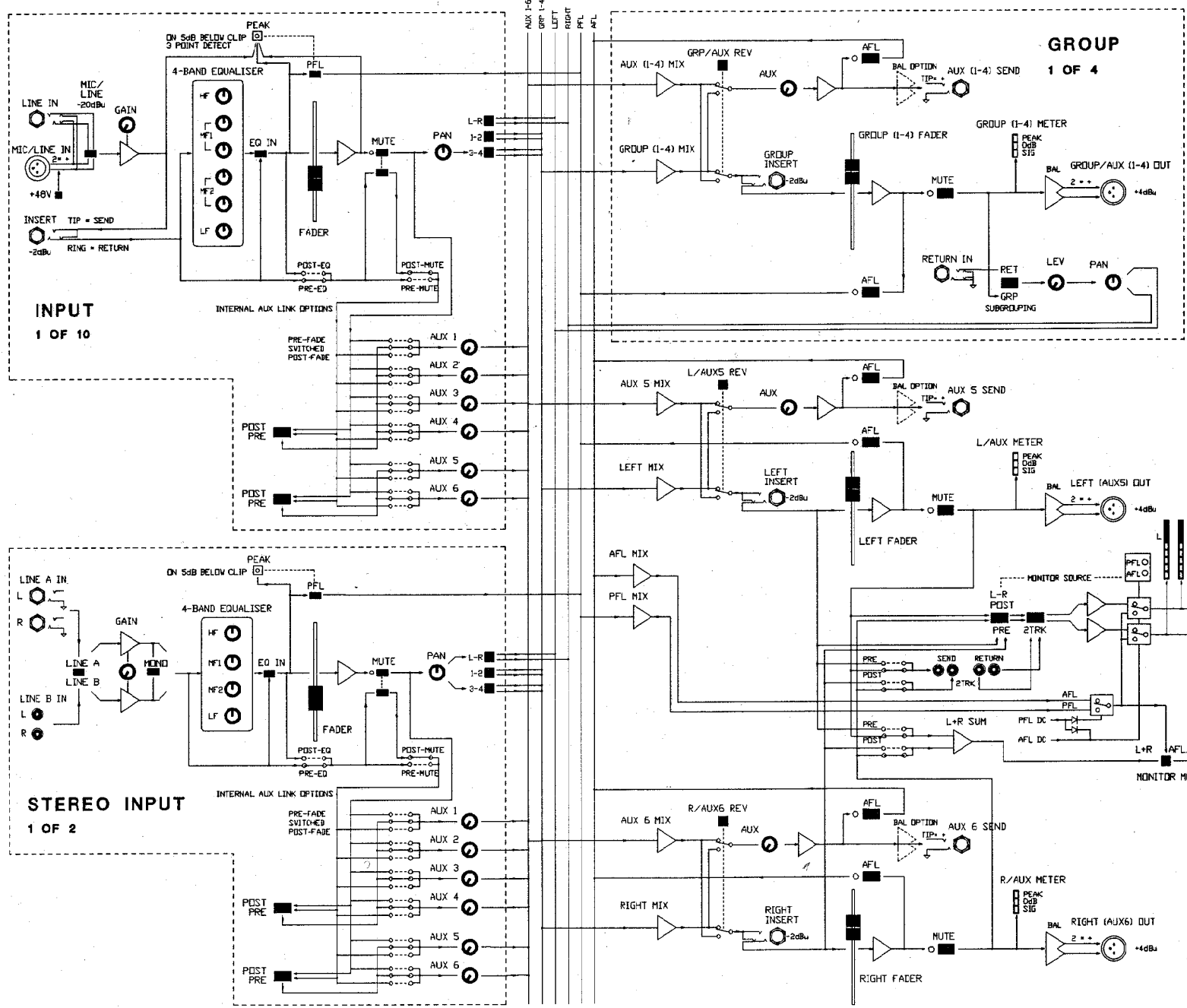


# GL2

## BLOCK DIAGRAM



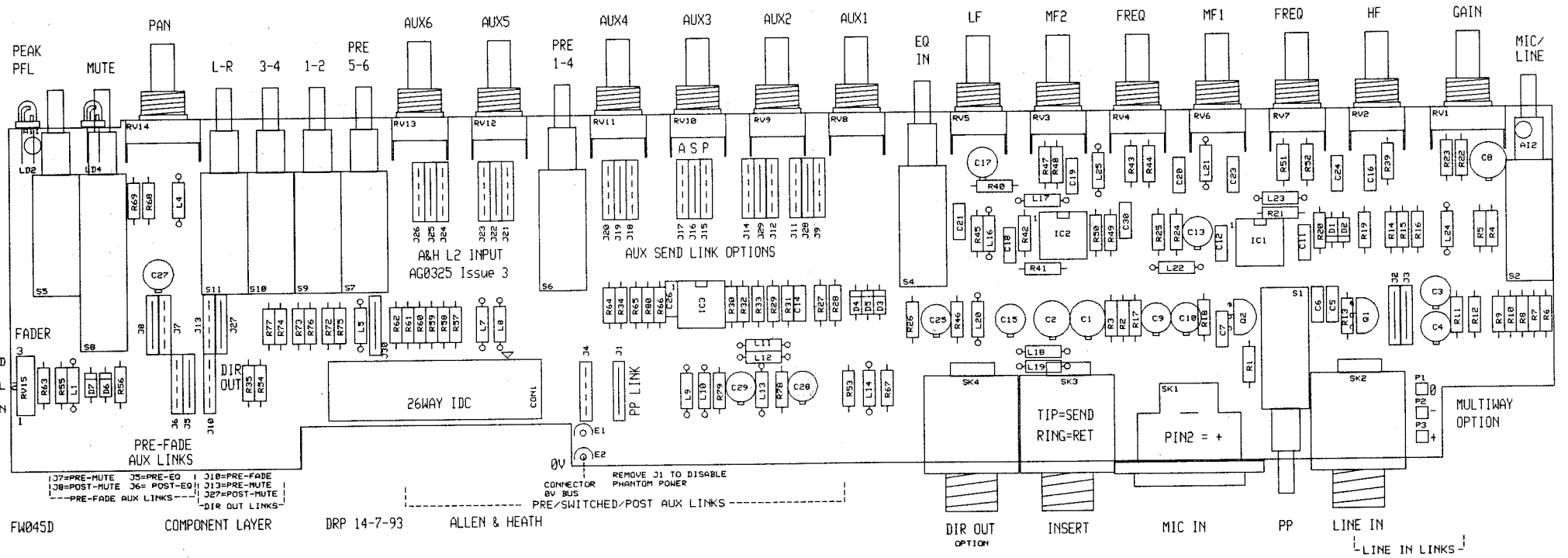
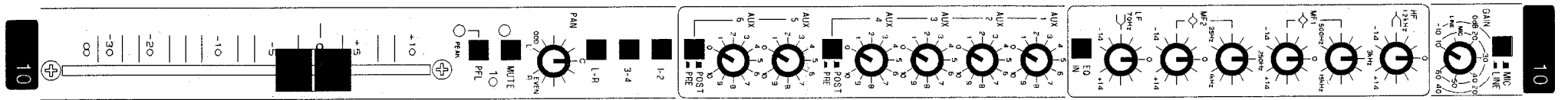
INPUT  
1 OF 10

STEREO INPUT  
1 OF 2

GROUP  
1 OF 4

MASTER

# INPUT CHANNEL



FW045D

COMPONENT LAYER

DRP 14-7-93

ALLEN & HEATH

DIR OUT OPTION

INSERT

MIC IN

PP

LINE IN

LINE IN LINKS

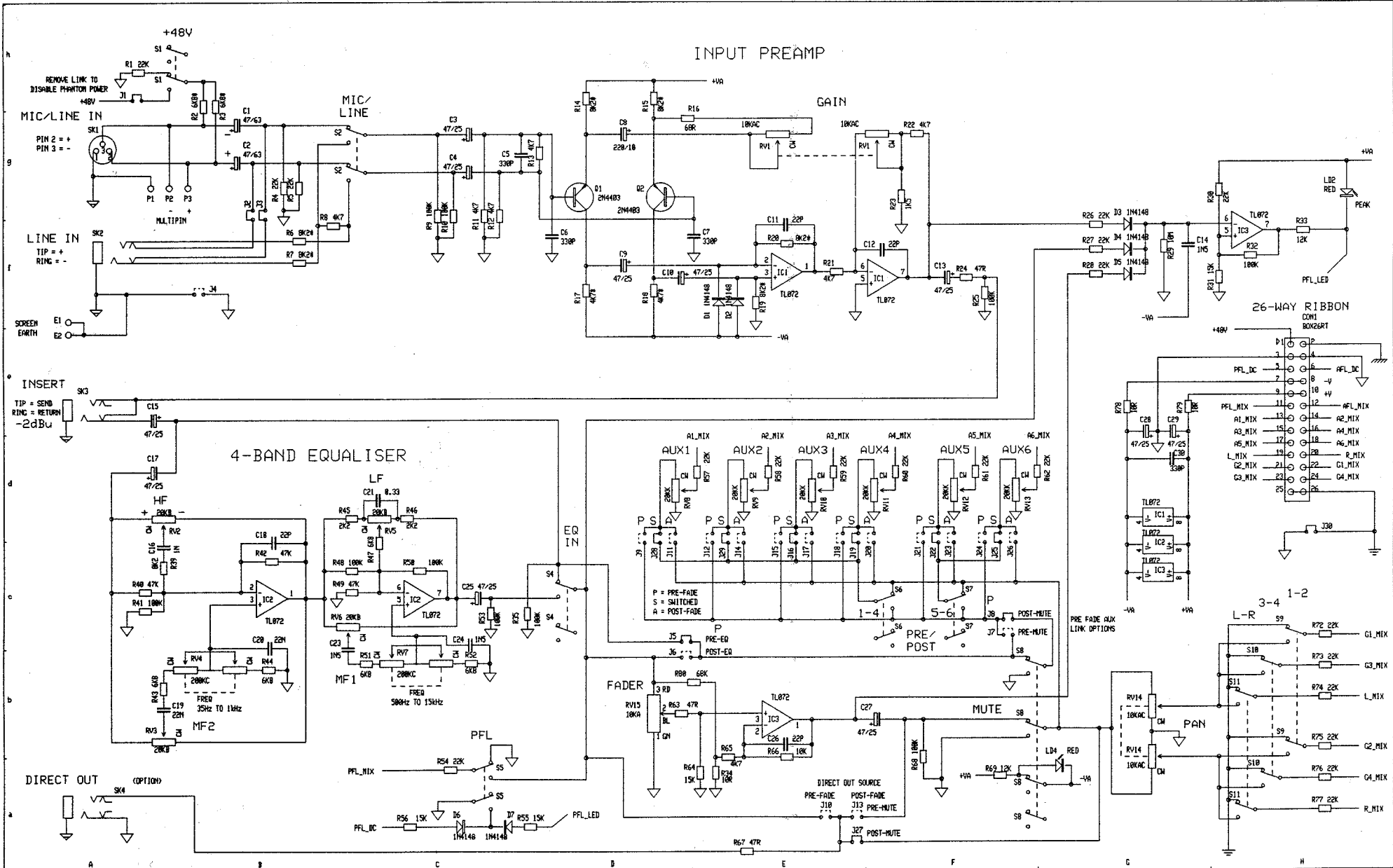
J7=PRE-MUTE    J5=PRE-EQ    J10=PRE-FADE  
 J8=POST-MUTE    J6=POST-EQ    J13=PRE-MUTE  
 J9=POST-MUTE    J12=POST-EQ    J14=POST-MUTE  
 PRE-FADE AUX LINKS    DIR OUT LINKS

REMOVE J1 TO DISABLE  
 CONNECTOR PHANTOM POWER  
 BY BUS  
 PRE/SWITCHED/POST AUX LINKS

A&H L2 INPUT  
AG0325 Issue 3

AUX SEND LINK OPTIONS

MULTIWAY OPTION



ISS.	REVISION	BY DATE	NOTES
P1	ORIGIN	CD 12-5-93 DRP 21-7-93	1. RESISTORS MARKED A ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE μF/VOLTS

UNIT TITLE  
GL2

DRAWING TITLE  
INPUT CIRCUIT DIAGRAM  
PCB TYPE AG0325

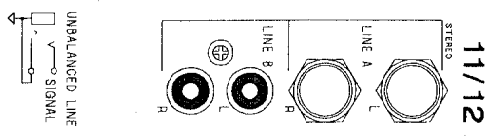
MANUFACTURED IN ENGLAND BY  
ALLEN & HEATH

DRAWING No. D222 ISSUE 1

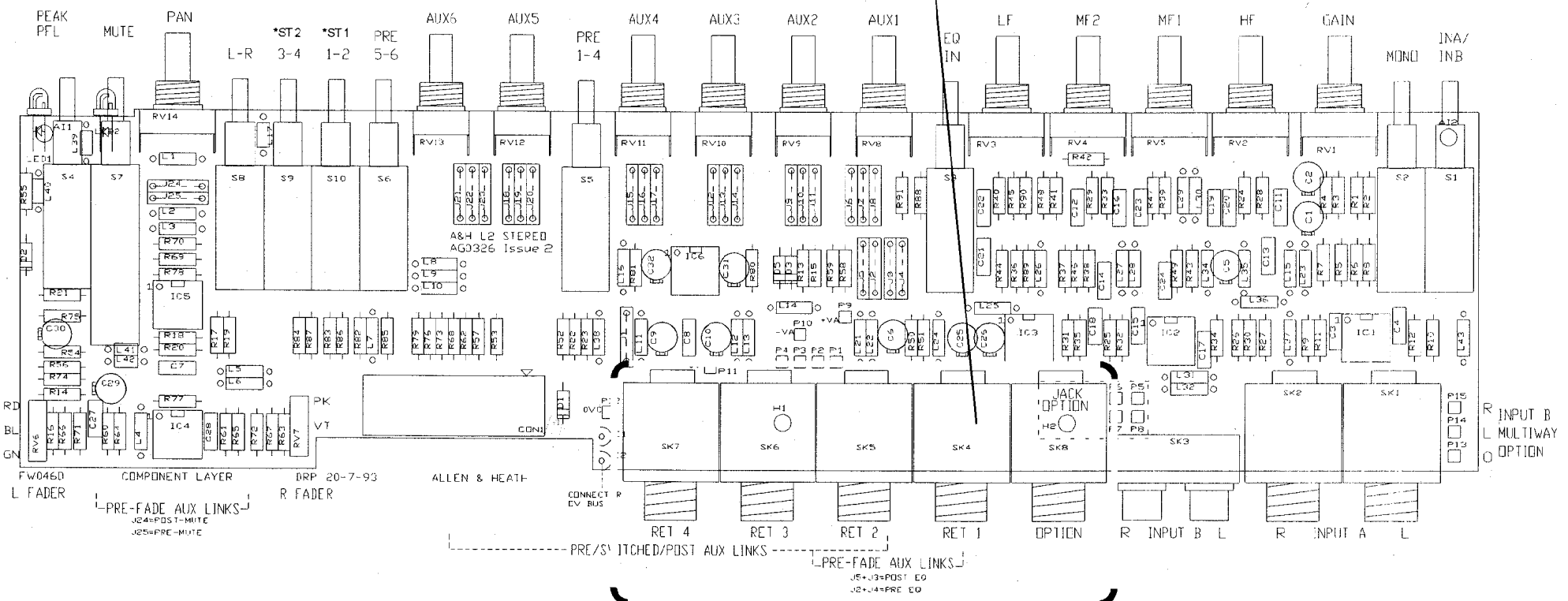
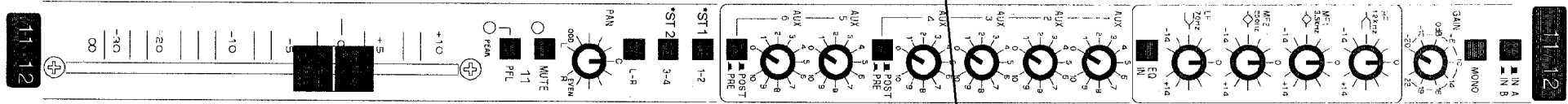
# STEREO CHANNEL

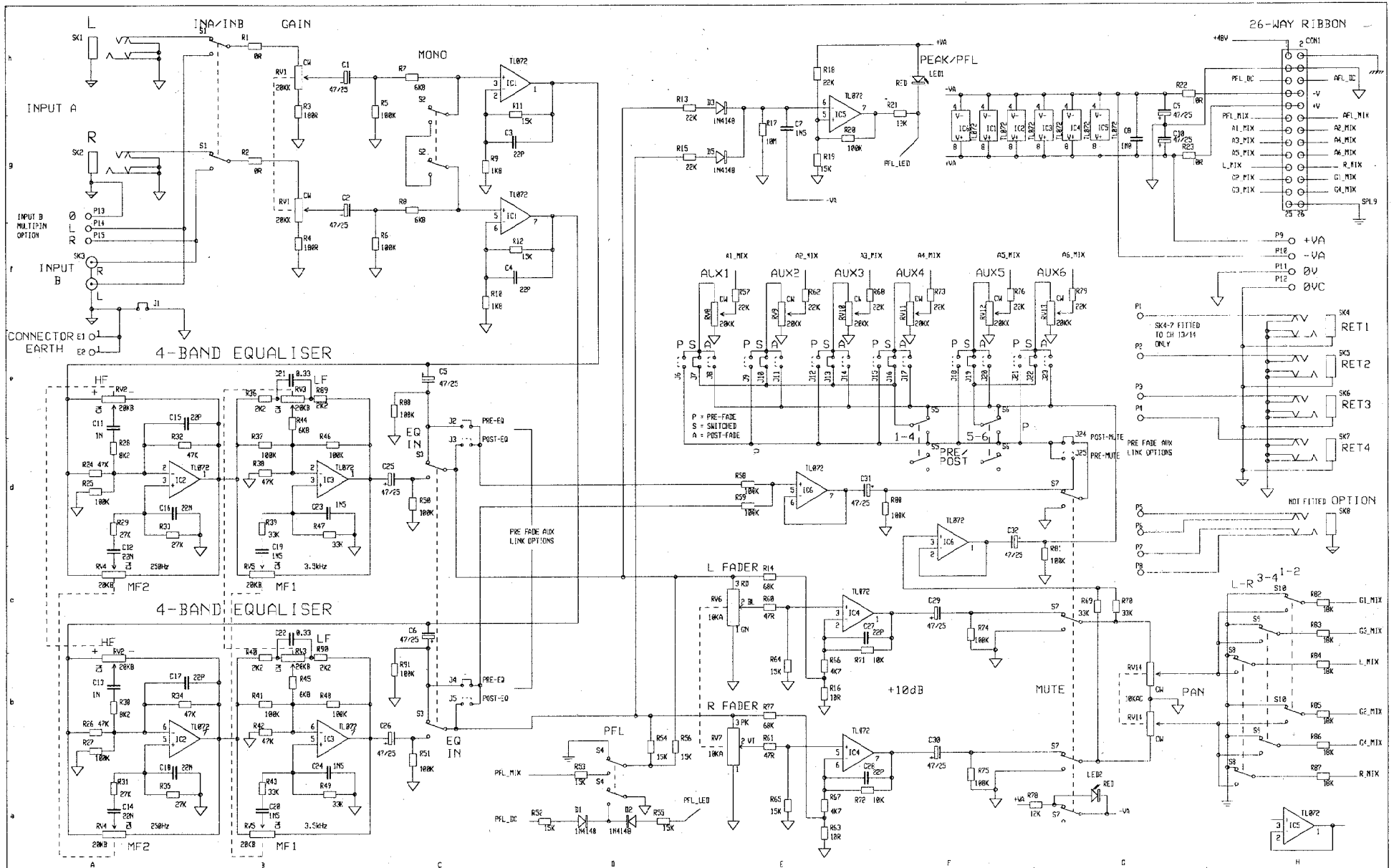
SK4, 5, 6, 7, 8 NOT FITTED ON GL2-S

\* = GL2-S



11/12





ISS.	REVISION	BY	DATE	NOTES
P1	ORIGIN	DRP	2-6-93	1. RESISTORS MARKED * ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE WAF-VOLTS
1		DRP	21-7-93	

UNIT TITLE  
GL2

DRAWING TITLE  
STEREO CIRCUIT DIAGRAM  
PCB TYPE AG0326

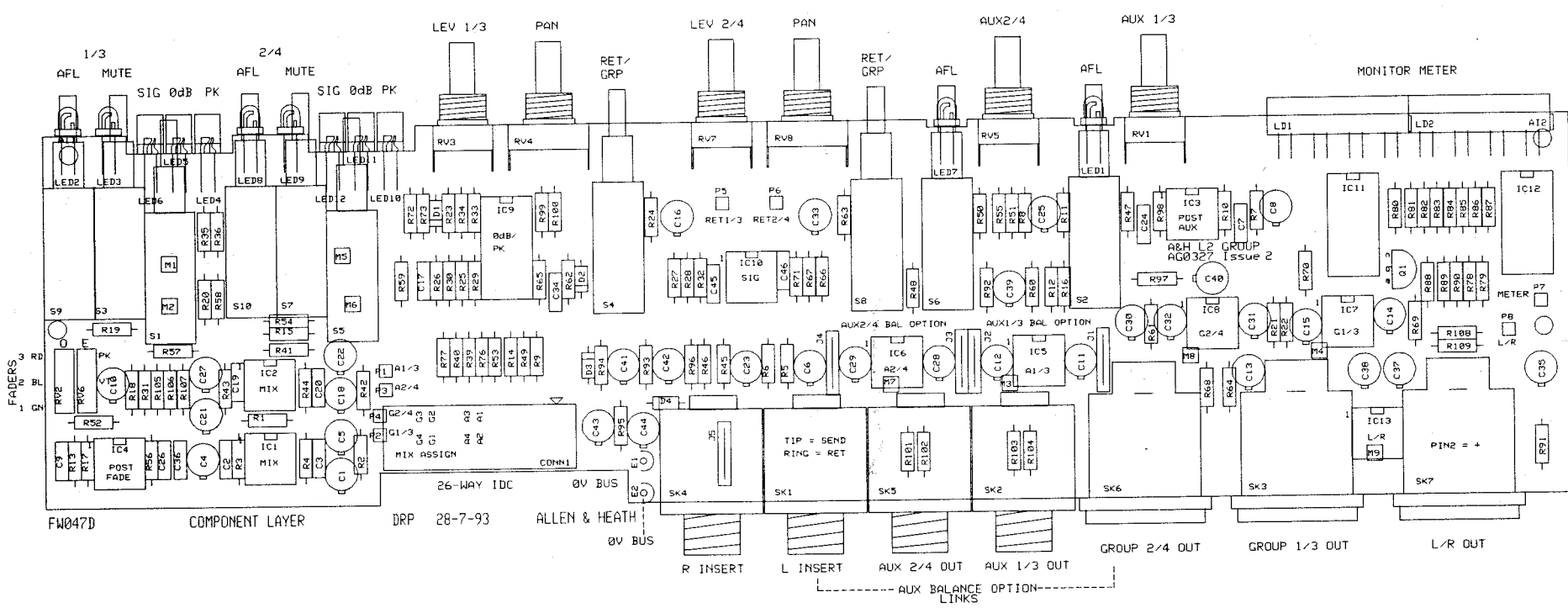
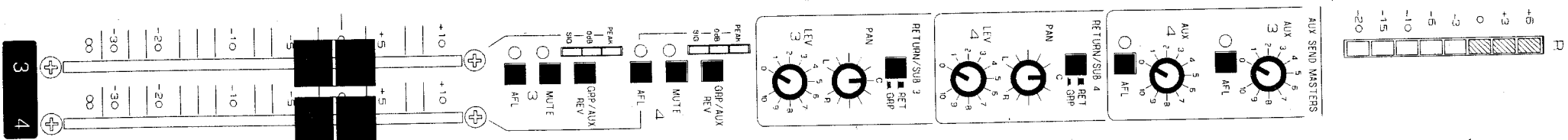
MANUFACTURED IN ENGLAND BY  
ALLEN & HEATH

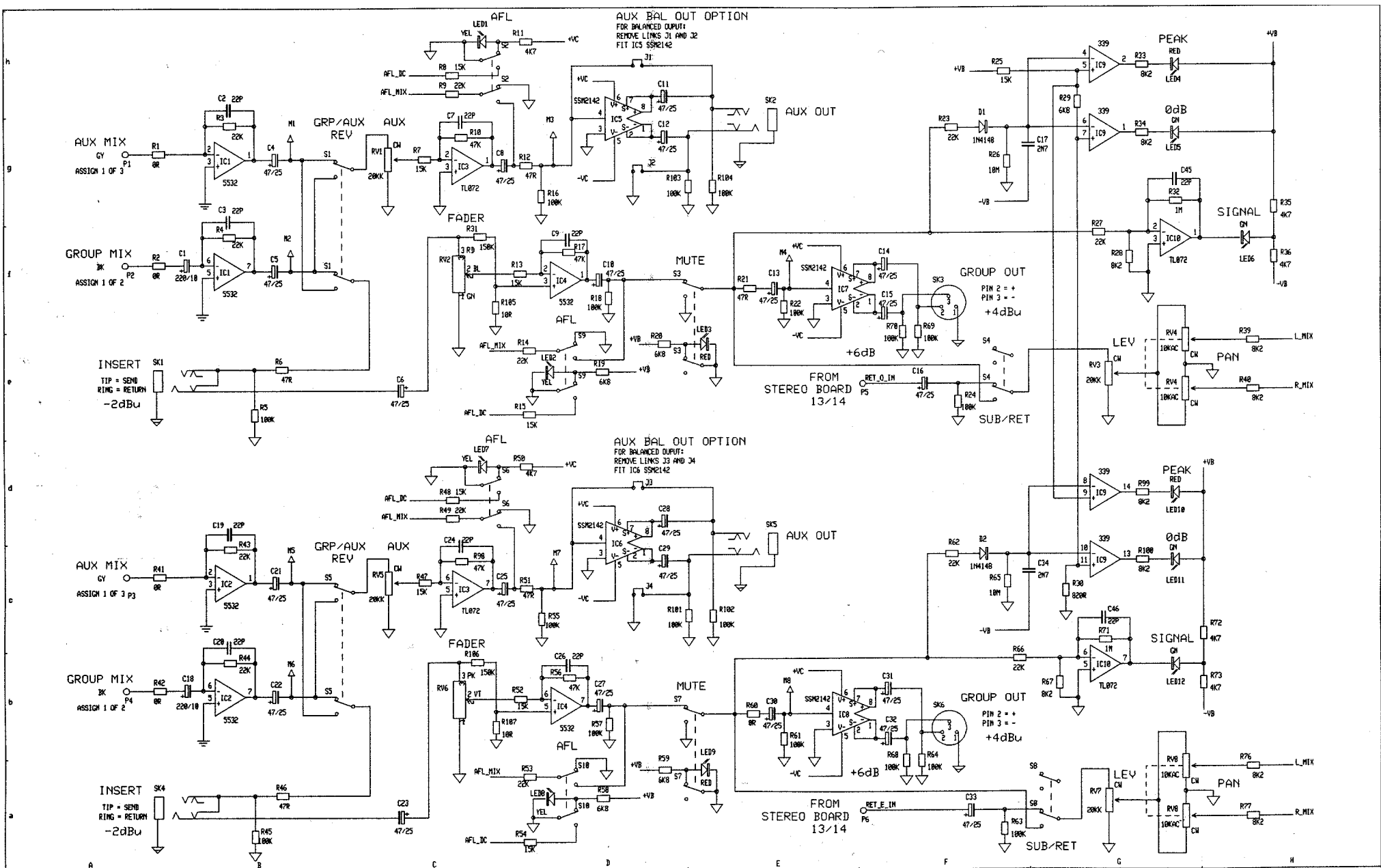
DRAWING No. D223 ISSUE 1

MANUFACTURED IN ENGLAND BY  
ALLEN & HEATH

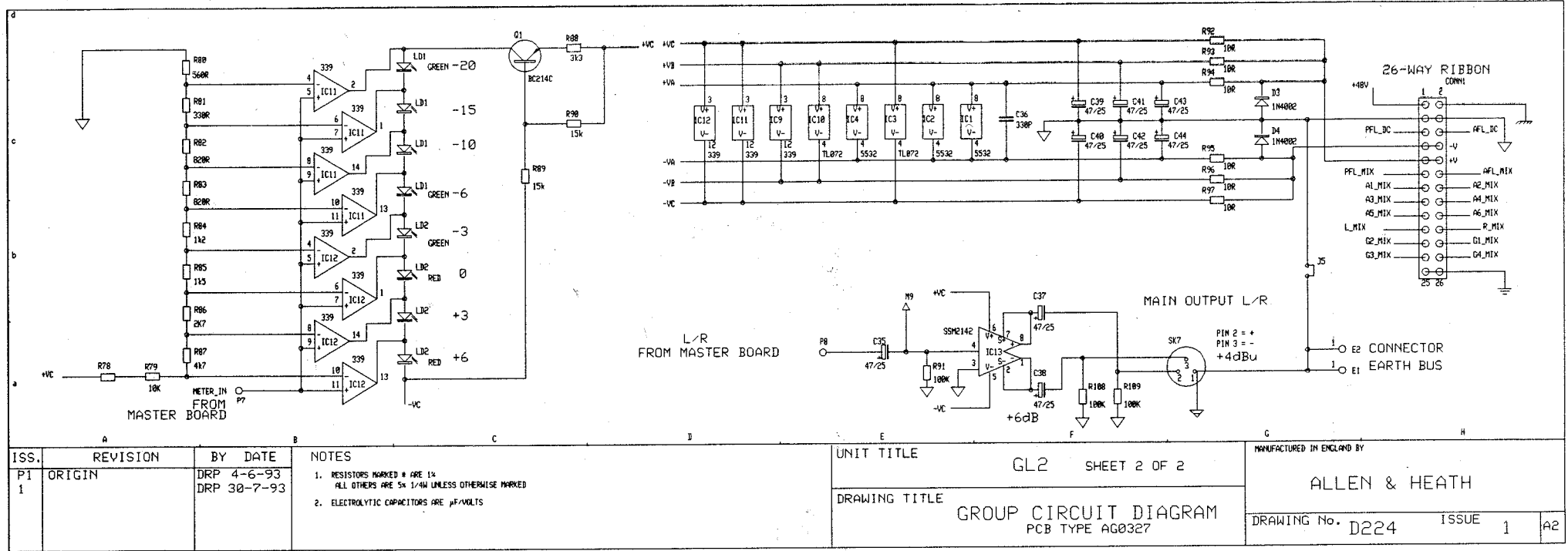
DRAWING No. D223 ISSUE 1

# GROUP SECTION



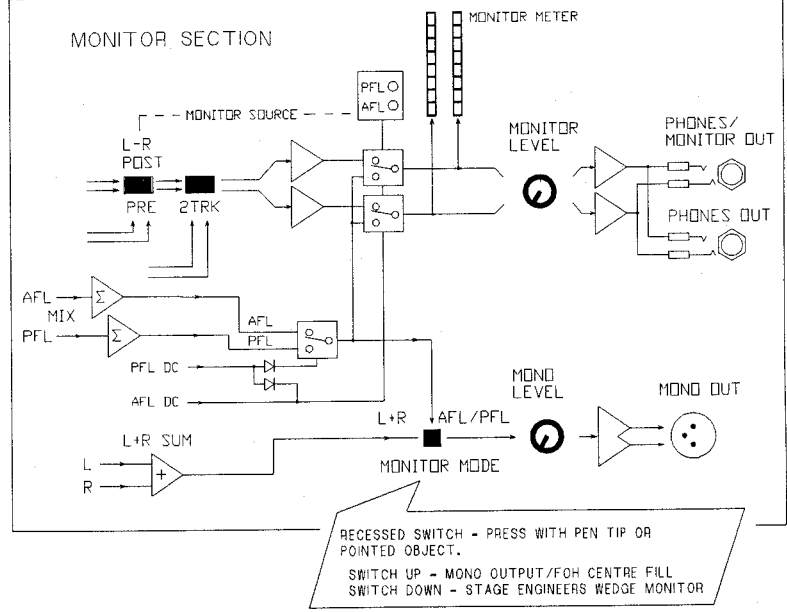
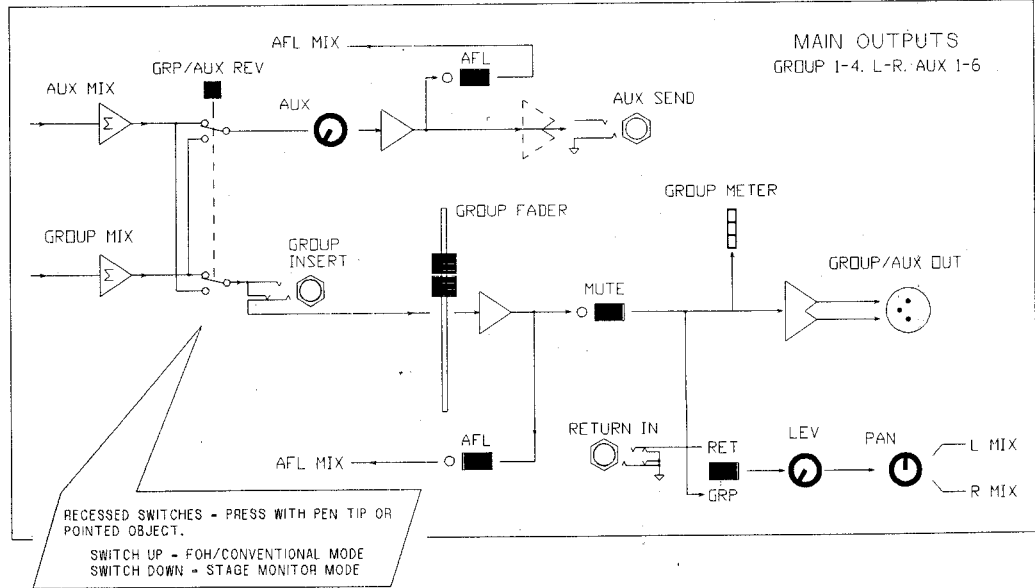


ISS.	REVISION	BY DATE	NOTES	UNIT TITLE	GL2 SHEET 1 OF 2	MANUFACTURED IN ENGLAND BY
P1	ORIGIN	DRP 4-6-93 DRP 30-7-93	1. RESISTORS MARKED # ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE µF-VOLTS	DRAWING TITLE	GROUP CIRCUIT DIAGRAM PCB TYPE AG0327	ALLEN & HEATH
1						DRAWING No. D224 ISSUE 1 A2



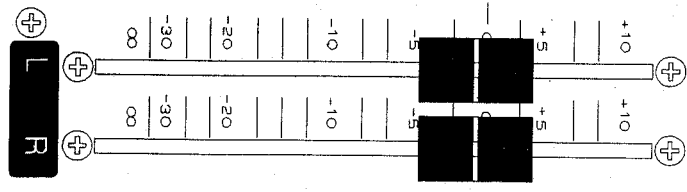
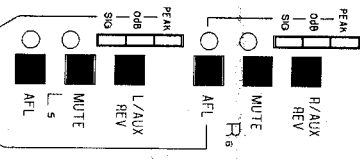
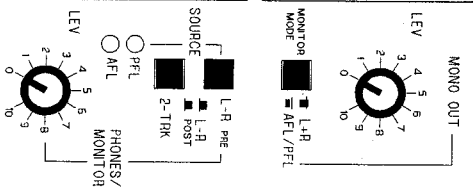
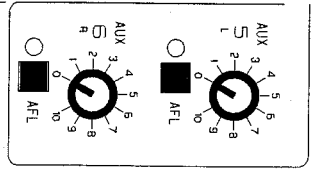
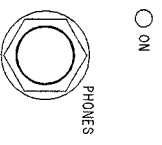
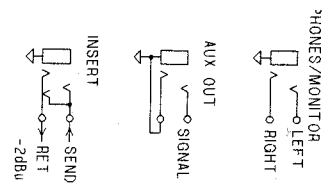
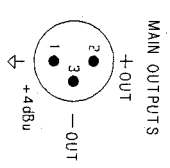
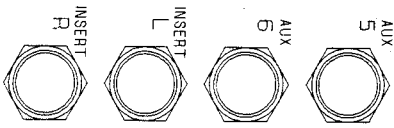
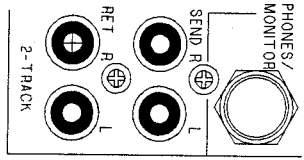
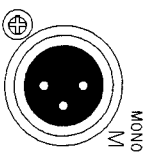
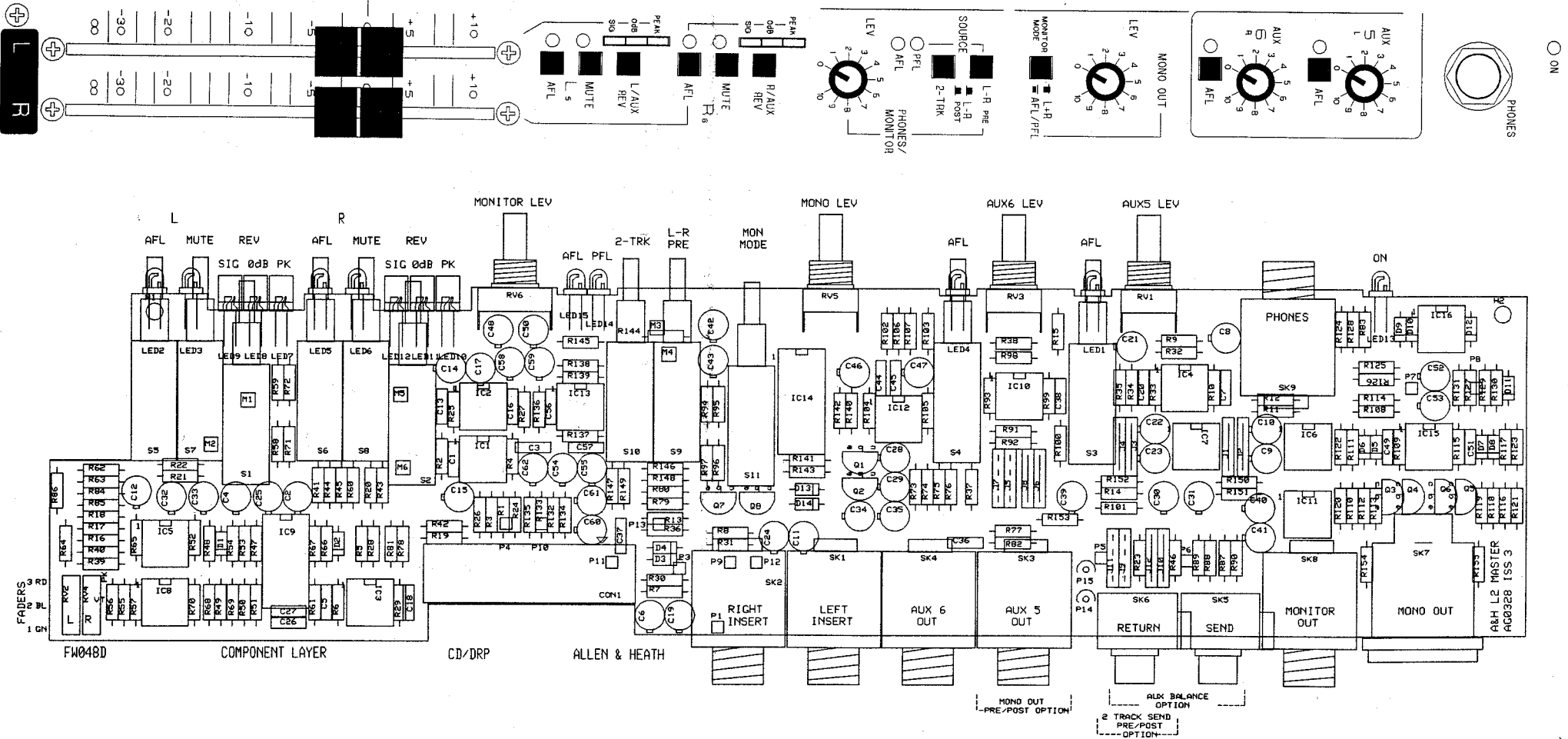
**MODE SWITCHING**

These simplified block diagrams illustrate the Group, L/R and Mono signal path switching which configures the GL2 for F.O.H or stage MONITOR use.





# MASTER SECTION



○ ON

PHONES

A8 & L2 MASTER  
AG3028 1SS 3

MONO OUT  
PRE-POST OPTION

2 TRACK SEND  
PRE-POST  
OPTION

ALX BALANCE  
OPTION

FW048D

COMPONENT LAYER

CD/DRP

ALLEN & HEATH

FADERS  
L  
R

L  
AFL MUTE REV SIG 0dB PK

R  
AFL MUTE REV SIG 0dB PK

MONITOR LEV

MONO LEV

AUX6 LEV

AUX5 LEV

AFL PFL 2-TRK L-R PRE MON MODE

AFL

AFL

ON

PHONES

MONITOR OUT

MONO OUT

RETURN

SEND

AUX 6 OUT

AUX 5 OUT

LEFT INSERT

RIGHT INSERT

CON1

IC8

IC9

IC10

IC11

IC12

IC13

IC14

IC15

IC16

LED2

LED3

LED4

LED5

LED6

LED7

LED8

LED9

LED10

RV2

RV3

RV4

RV5

RV6

RV7

RV8

RV9

RV10

RV11

RV12

RV13

RV14

RV15

RV16

RV17

RV18

RV19

RV20

RV21

RV22

SK1

SK2

SK3

SK4

SK5

SK6

SK7

SK8

SK9

SK10

SK11

SK12

SK13

SK14

SK15

SK16

SK17

SK18

SK19

SK20

SK21

P1

P2

P3

P4

P5

P6

P7

P8

P9

P10

P11

P12

P13

P14

P15

P16

P17

P18

P19

P20

P21

S1

S2

S3

S4

S5

S6

S7

S8

S9

S10

S11

S12

S13

S14

S15

S16

S17

S18

S19

S20

S21

C1

C2

C3

C4

C5

C6

C7

C8

C9

C10

C11

C12

C13

C14

C15

C16

C17

C18

C19

C20

C21

R1

R2

R3

R4

R5

R6

R7

R8

R9

R10

R11

R12

R13

R14

R15

R16

R17

R18

R19

R20

R21

Q1

Q2

Q3

Q4

Q5

Q6

Q7

Q8

Q9

Q10

Q11

Q12

Q13

Q14

Q15

Q16

Q17

Q18

Q19

Q20

Q21

D1

D2

D3

D4

D5

D6

D7

D8

D9

D10

D11

D12

D13

D14

D15

D16

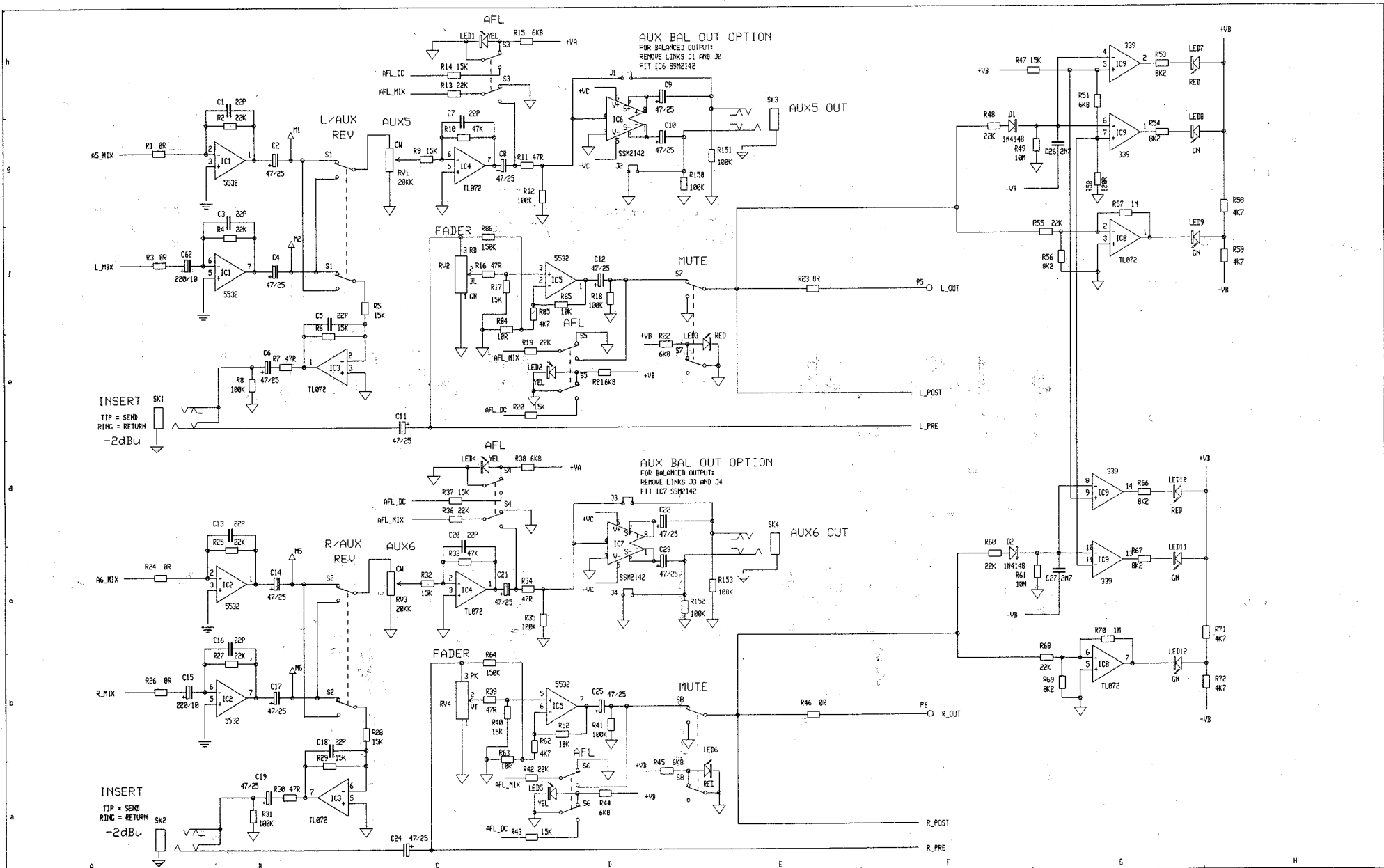
D17

D18

D19

D20

D21



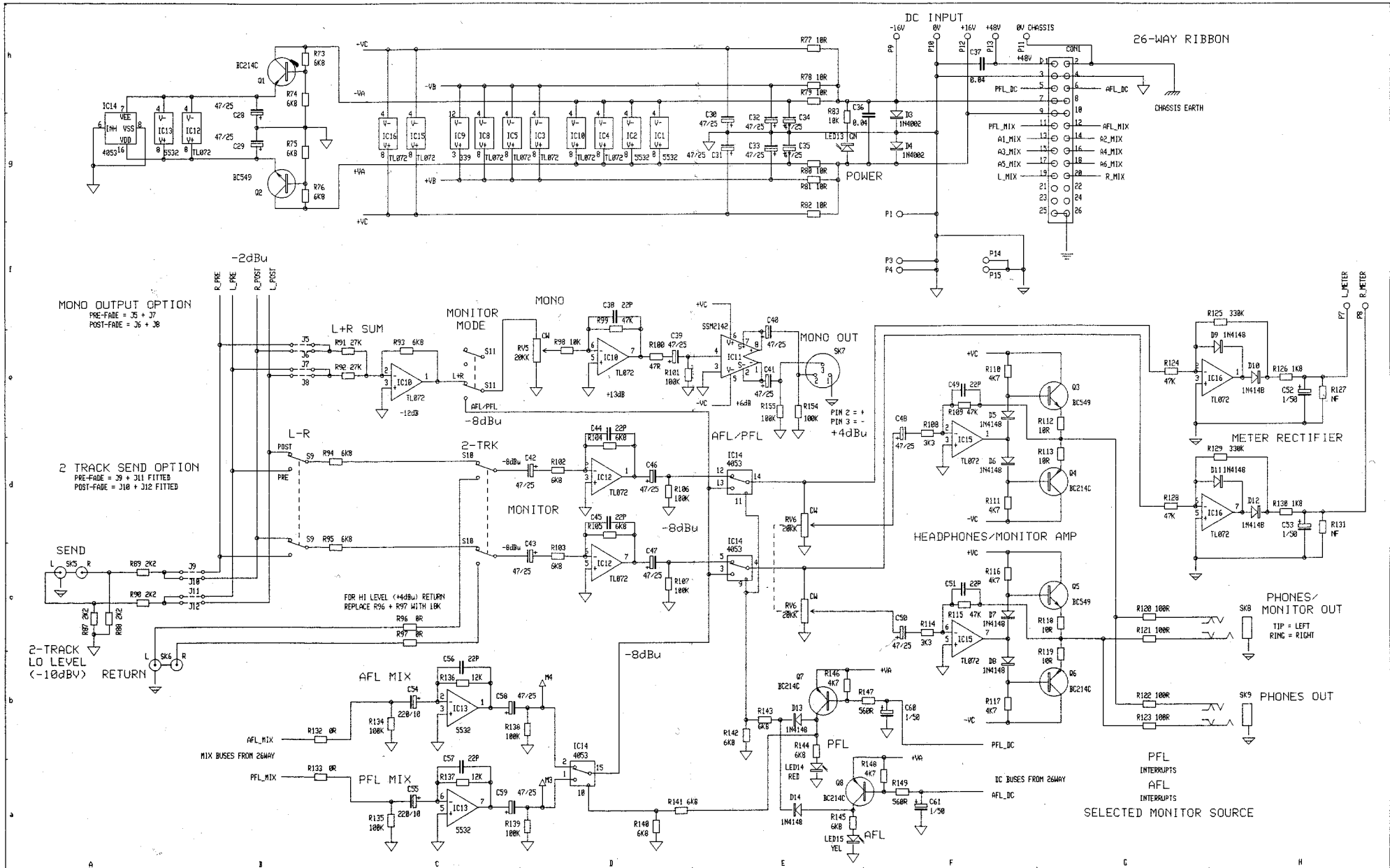
INSERT  
TIP = SEND  
RING = RETURN  
-2dBu

INSERT  
TIP = SEND  
RING = RETURN  
-2dBu

AUX BAL OUT OPTION  
FOR BALANCED OUTPUT:  
REMOVE LINKS J1 AND J2  
FIT IC6 55M2142

AUX BAL OUT OPTION  
FOR BALANCED OUTPUT:  
REMOVE LINKS J3 AND J4  
FIT IC7 55M2142

ISS.	REVISION	BY	DATE	NOTES	UNIT TITLE	MANUFACTURED IN ENGLAND BY
P1 1	ORIGIN	CD DRP	8-6-93 30-8-93	1. RESISTORS MARKED # ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE µF-VOLTS	GL2 SHEET 1 OF 2	ALLEN & HEATH
					DRAWING TITLE	DRAWING No.
					MASTER CIRCUIT DIAGRAM PCB TYPE AG0328	D225
						ISSUE 1
						A2



ISS.	REVISION	BY DATE	NOTES	UNIT TITLE	GL2 SHEET 2 OF 2	MANUFACTURED IN ENGLAND BY
P1	ORIGIN	CD 8-6-93 DRP 30-8-93	1. RESISTORS MARKED 4 ARE 1% ALL OTHERS ARE 5% 1/4W UNLESS OTHERWISE MARKED 2. ELECTROLYTIC CAPACITORS ARE µF/VOLTS	DRAWING TITLE	MASTER CIRCUIT DIAGRAM PCB TYPE AG0328	ALLEN & HEATH
						DRAWING No. D225 ISSUE 1 A2