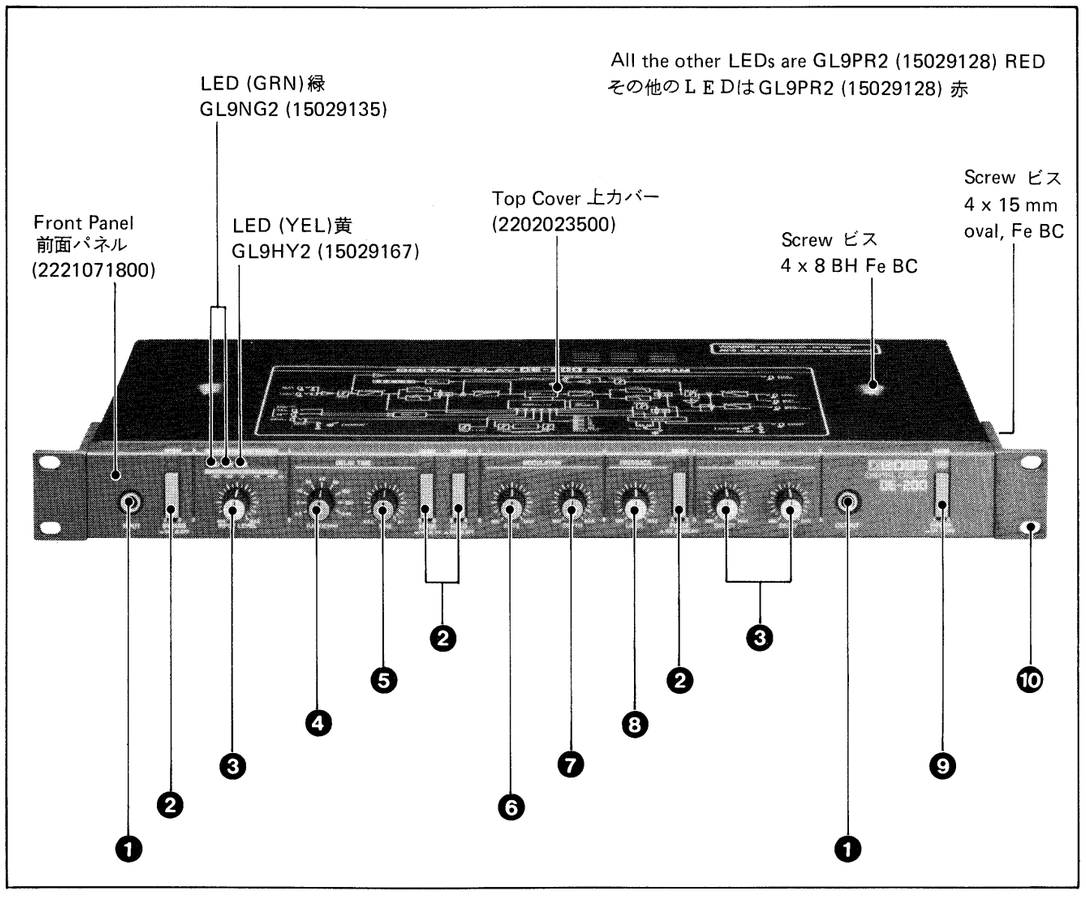
BOSS DE-200

SERVICE NOTES *First Edition*

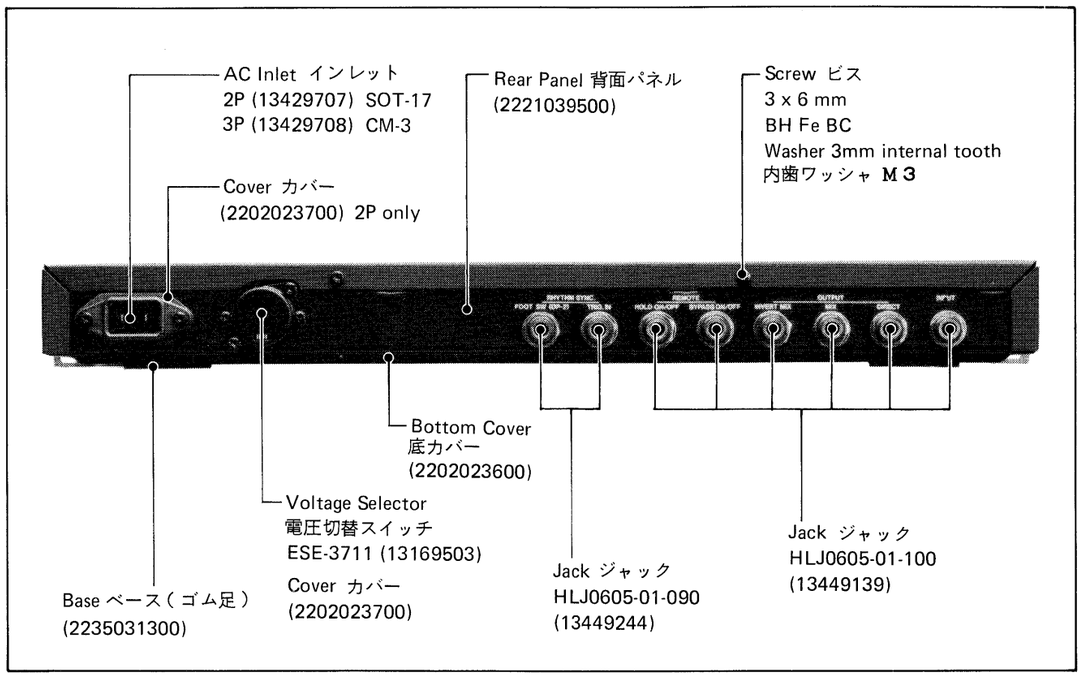
SPECIFICATIONS

Input	Rated: –20dBm, Maximum: +12dBm
	Impedance: 1M Ohms
Output	Rated: –20dBm into 10k Ohms
Dynamic Range	Direct: 110dB
	Delay: 80dB
Total Harmonic	Direct: 0.08%
Distortion	Delay: 0.25%
Delay Time	1.25ms–640ms @ MODE X1
	2.5ms–1280ms @ MODE X2
Frequency Response	Direct: 10Hz–100kHz +0.5, –3dB
	Delay: 10Hz–10kHz +0.5, –3dB @ MODE X1
	10Hz–4.5kHz +0.5, –3dB @ MODE X2
Power Consumption	9 Watts
Dimensions	482(W) x 44(H) x 240(D) mm
	19(W) x 1-3/4(H) x 9-7/16(D) in
Weight	3.5 kg / 7 lb 11oz

FRONT VIEW



REAR VIEW



DISASSEMBLY

Removal of Bottom Cover exposes the component side of Main Board.

メイン基板の部品側は底カバーをはずすだけで点検することができます。

1 .... Jackジャック HLJ2317-01-100 (13449138)

2 .... Button ボタン (2247057900)
Switch スイッチ SUF-12 (13129342)

3 .... Knob (ORN) ツマミ 橙 (2247025900)
Pot. ボリューム EVH-6PA332A14 10KA (13219363)

4 ... Knob (GRN) ツマミ 緑 (2247026000)
Switch スイッチ SRJ4049 (13119808)

5 .... Knob (GRN) ツマミ 緑 (2247026000)
Pot. ボリューム EVH-6PA332B54 50KB (13219342)

6 .... Knob (BLU) ツマミ 青 (2247026200)
Pot. ボリューム EVH-6PA332CF5 250KC (13219365)

7 .... Knob (BLU) ツマミ 青 (2247026200)
Pot. ボリューム EVH-6PA332B54 50KB (13219342)

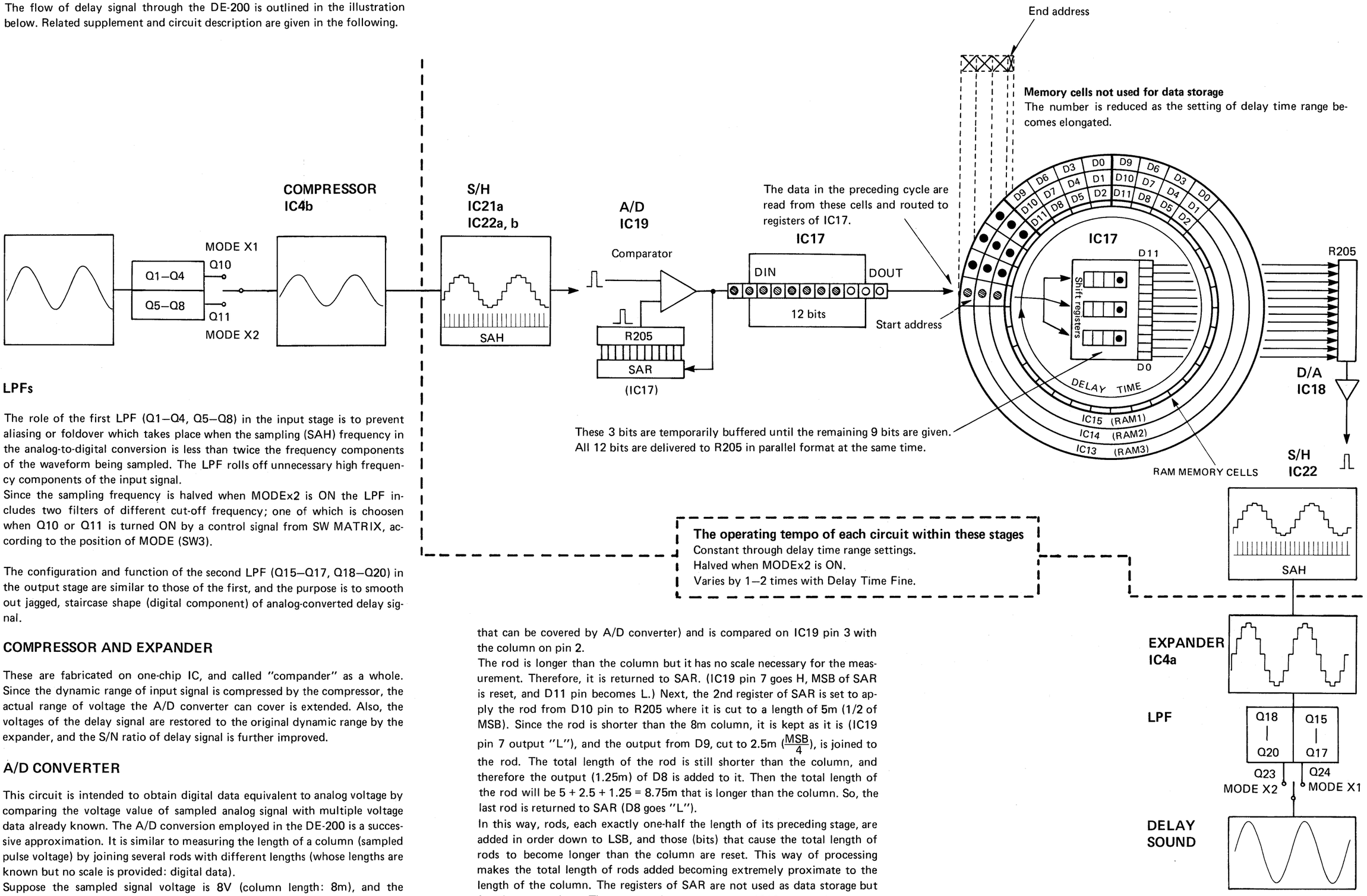
8 .... Knob (YEL) ツマミ 黄 (2247026100)
Pot. ボリューム EVH-6PA332C14 10KC (13219364)

9 .... Button ボタン (2247057900)
Power Switch 電源スイッチ SDGA-3P (13129124)

10 .... Rack Angle ラック・アングル (2212051700)

CIRCUIT DESCRIPTIONS

The flow of delay signal through the DE-200 is outlined in the illustration below. Related supplement and circuit description are given in the following.



LPFs

The role of the first LPF (Q1–Q4, Q5–Q8) in the input stage is to prevent aliasing or foldover which takes place when the sampling (SAH) frequency in the analog-to-digital conversion is less than twice the frequency components of the waveform being sampled. The LPF rolls off unnecessary high frequency components of the input signal.
Since the sampling frequency is halved when MODEx2 is ON the LPF includes two filters of different cut-off frequency; one of which is choosen when Q10 or Q11 is turned ON by a control signal from SW MATRIX, according to the position of MODE (SW3).

The configuration and function of the second LPF (Q15–Q17, Q18–Q20) in the output stage are similar to those of the first, and the purpose is to smooth out jagged, staircase shape (digital component) of analog-converted delay signal.

COMPRESSOR AND EXPANDER

These are fabricated on one-chip IC, and called "compander" as a whole. Since the dynamic range of input signal is compressed by the compressor, the actual range of voltage the A/D converter can cover is extended. Also, the voltages of the delay signal are restored to the original dynamic range by the expander, and the S/N ratio of delay signal is further improved.

A/D CONVERTER

This circuit is intended to obtain digital data equivalent to analog voltage by comparing the voltage value of sampled analog signal with multiple voltage data already known. The A/D conversion employed in the DE-200 is a successive approximation. It is similar to measuring the length of a column (sampled pulse voltage) by joining several rods with different lengths (whose lengths are known but no scale is provided: digital data).
Suppose the sampled signal voltage is 8V (column length: 8m), and the maximum voltage handled by A/D converter is 20V (20m). Then, one rod (MSB) from SAR in IC17 is applied through D11 pin to R205 (ladder resistor), where it is cut to a length of 20÷2 = 10m (1/2 of the maximum voltage that can be covered by A/D converter) and is compared on IC19 pin 3 with the column on pin 2.
The rod is longer than the column but it has no scale necessary for the measurement. Therefore, it is returned to SAR. (IC19 pin 7 goes H, MSB of SAR is reset, and D11 pin becomes L.) Next, the 2nd register of SAR is set to apply the rod from D10 pin to R205 where it is cut to a length of 5m (1/2 of MSB). Since the rod is shorter than the 8m column, it is kept as it is (IC19 pin 7 output "L"), and the output from D9, cut to 2.5m ($\frac{MSB}{4}$), is joined to the rod. The total length of the rod is still shorter than the column, and therefore the output (1.25m) of D8 is added to it. Then the total length of the rod will be 5 + 2.5 + 1.25 = 8.75m that is longer than the column. So, the last rod is returned to SAR (D8 goes "L").
In this way, rods, each exactly one-half the length of its preceding stage, are added in order down to LSB, and those (bits) that cause the total length of rods to become longer than the column are reset. This way of processing makes the total length of rods added becoming extremely proximate to the length of the column. The registers of SAR are not used as data storage but for the comparison. The outputs from comparator IC19 are used to set or reset each register of SAR and are also delivered as serial data from D OUT pin to RAMs IC13–IC15 and stored in memory cells.

RAM

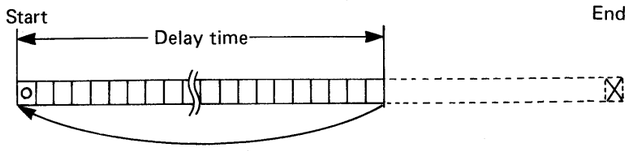
Refer to the Main Controller Block Diagram and Timing Diagram. When the delay time has been set, 3 bits (1 bit each) from the start address of the 3 RAMs are simultaneously read on the negative going edge of CAS1–CAS3. (Naturally, no "Music data" are in memory cells when the power is first applied to the DE-200 or when no musical signal is being applied to the DE-200.) Successively, the data from IC19 are written into these 3 memory cells in order. The operation is repeated for other memory locations keeping pace with the step of address. When the set delay time has passed, the memory cells at start address are read again. Memory cells not read/written yet at that point will be left unused. Conversely, the more the number of memory cells are, the longer the delay time. This is very similar to a phenomenon on a tape echo machine such that changing the (endless) tape length with the tape speed kept constant causes the repeat rate of echo to change. In the DE-200, in the MODEx1, the output frequency (MSCK) of VOC (IC16) remains unchanged regardless of the delay time range set. Since the main controller IC17 determines the tempos of the control signals for A/D, D/A and RAM to MSCK, these tempos are kept constant as well. In the case of tape echo, reducing the tape speed by 1/2 causes the repeat rate to be halved. While in the DE-200, when MODEx2 is turned ON, RING1 of IC17 goes H and MSCK is divided by 2, causing the output frequencies of timing generator to be halved.

RHYTHM SYNCHRONIZATION

The DE-200 is provided with rhythm sync function with which the start and stop of delay can be done by external trigger signal. An example of the effects will be delay sounds synchronizing with the tempo from the rhythm machine.

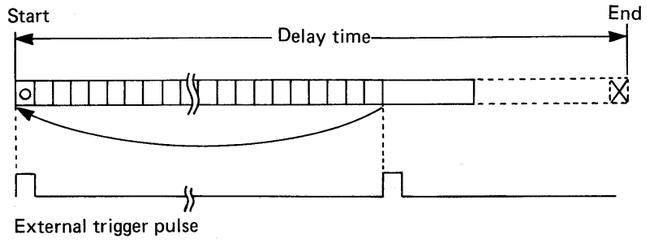
Normal mode

Memory cells are read/written in the order from the start address up to the one corresponding to the length of delay time, and are again accessed with the start address.



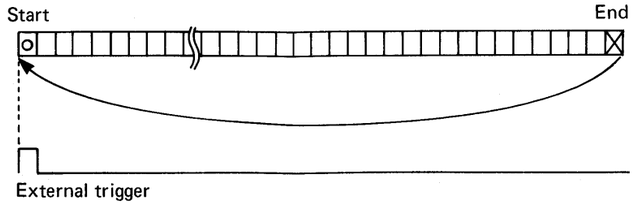
Sync mode 1

When, in this mode, the trigger interval is shorter than the maximum delay time, the delay time is set to the maximum irrespective of the delay time setting on the panel. The first trigger causes the delay to start.
When the second trigger is applied within the maximum delay time, the RAM address returns to the start point and stops there. The address will advance when the next trigger is applied.

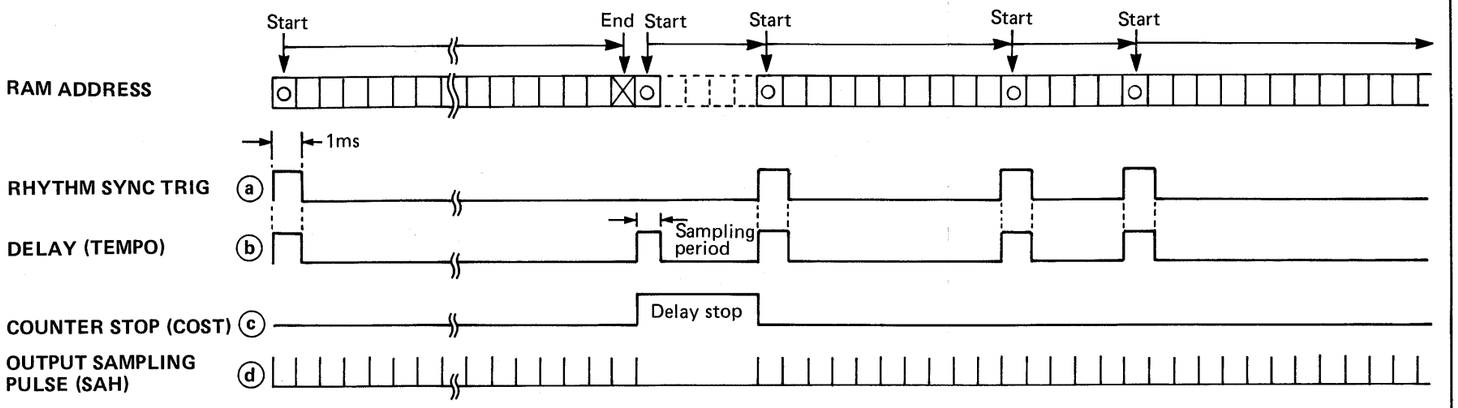


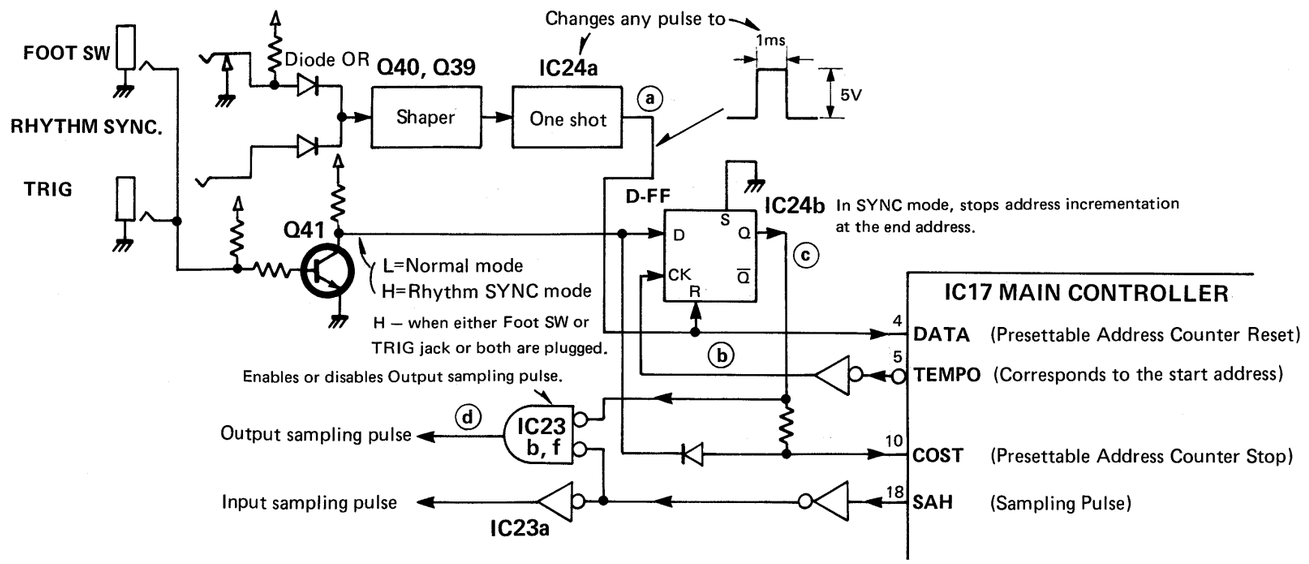
Sync mode 2

When the trigger interval is longer than the maximum delay time, the address automatically returns to the start point even the second trigger is absent on completion of read/write at the end address. The address will not restart until the next trigger is applied.



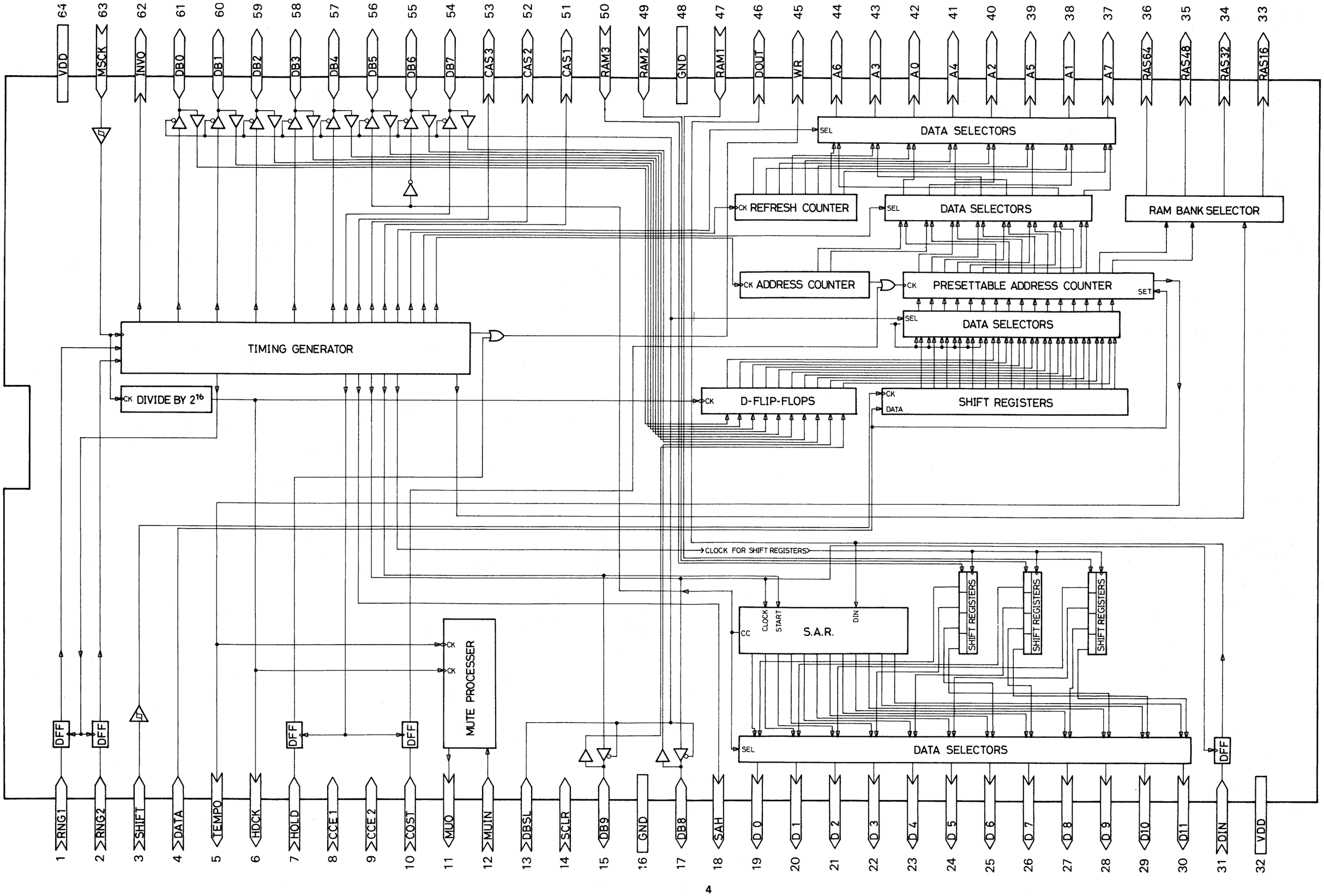
RHYTHM SYNC TIMING DIAGRAM



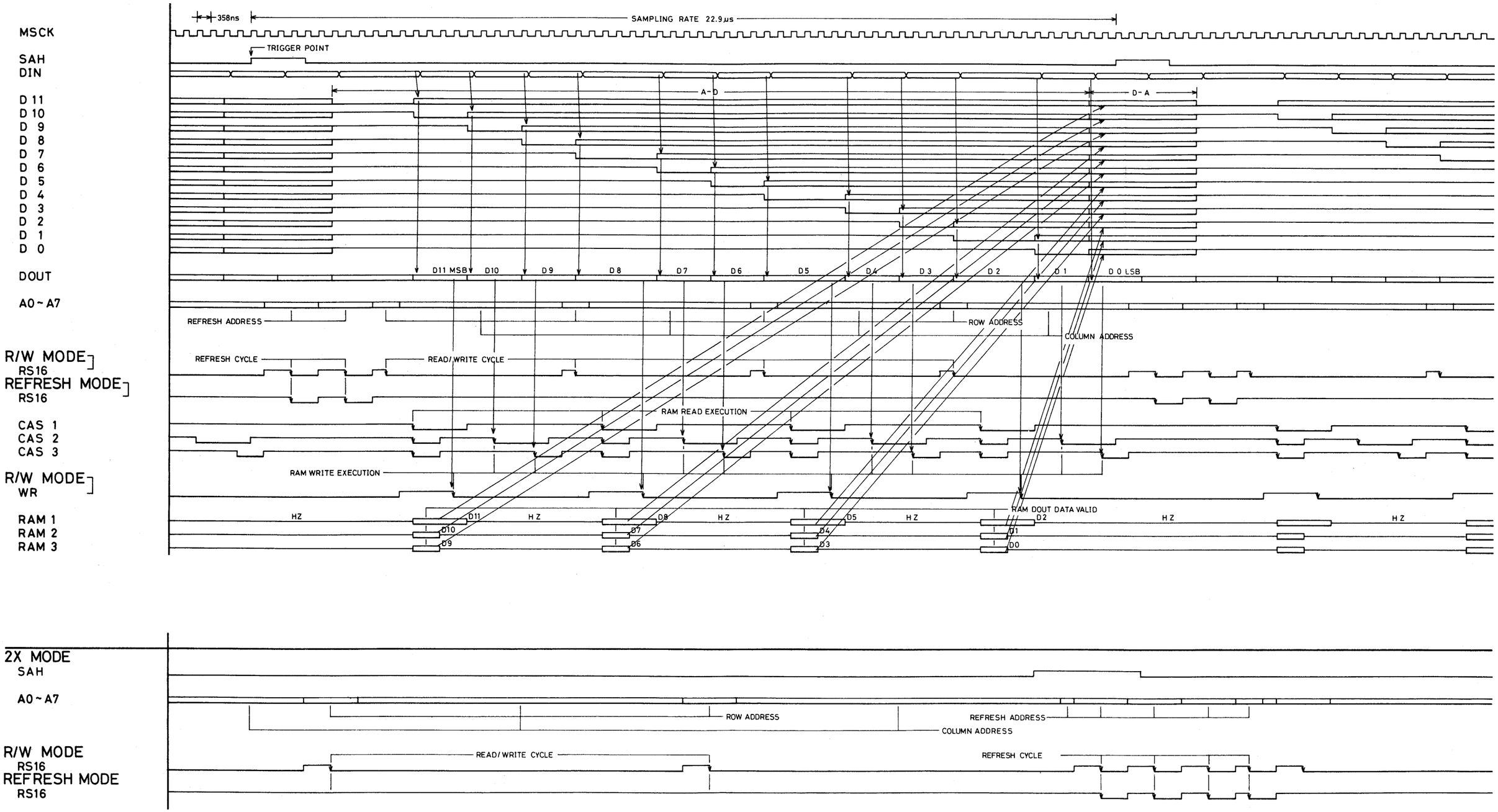


An external trigger, after converted into (a), resets IC24b and Presettable Address Counter which initializes RAM address (at the start location). When the address counter has incremented up to the end address without being disturbed by an external trigger, it returns to the start address and at the same time places TEMPO (b) which causes IC24b to latch Q41 output(D).Being in SYNC mode, D is H and IC24b turns its Q to H (c). This high (c) also inhibits SAH from being gated through IC23 b and f, disabling output sampling pulses (d) until the next rise edge of a and b.

MAIN CONTROLLER BLOCK DIAGRAM
IC17



MAIN CONTROLLER TIMING DIAGRAM
IC17



DELAY SOUND FAILURE CHECKING
– A/D, D/A and RAMs –

If delay sound is abnormal, check on 3 separate groups of A/D cycle, D/A cycle and RAMs.
Apply rated sine waves to the INPUT jack and observe the waveform on TP-6.

A/D cycle

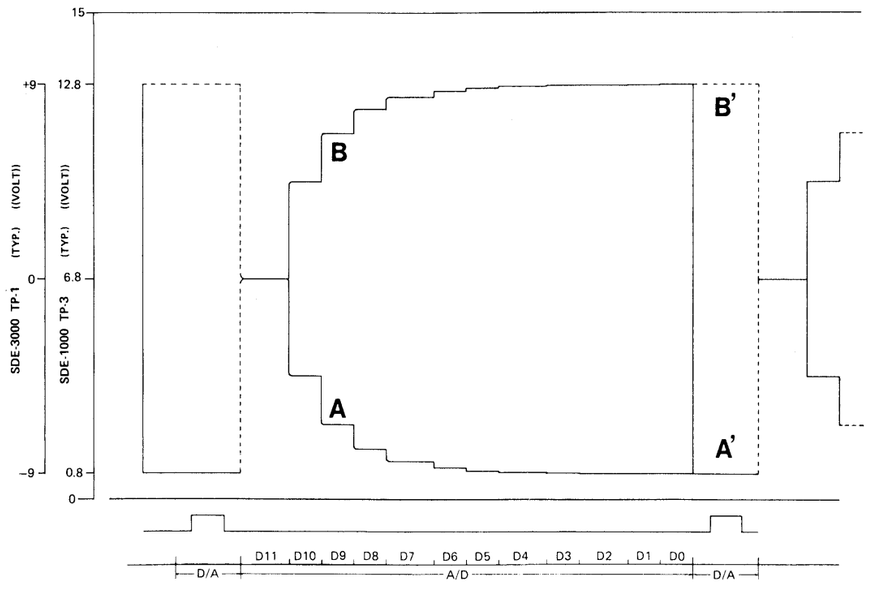
Check to see that the level of each stepped wave increases and decreases in 1/2 steps. This will prove difficult to achieve in LSB portions because the amplitude difference between adjacent steps becomes smaller and smaller. All "1" & All "0" Tests described below will be a great help.

D/A cycle

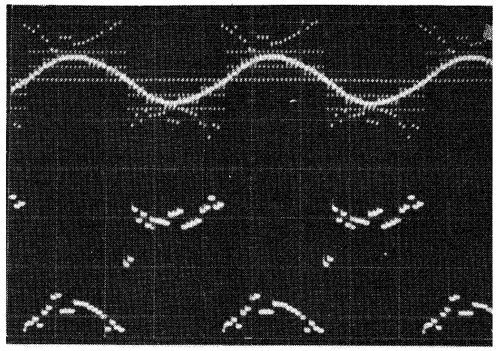
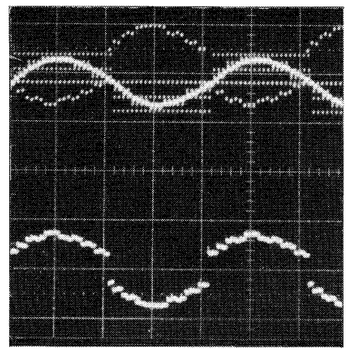
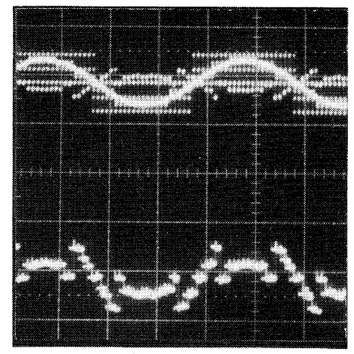
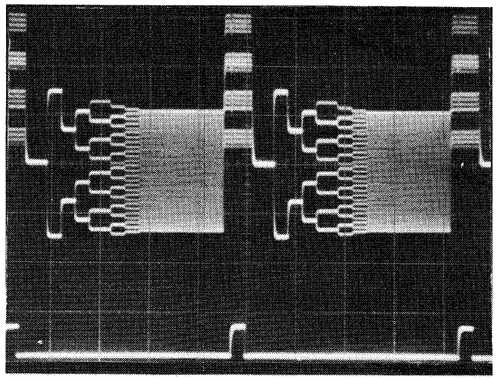
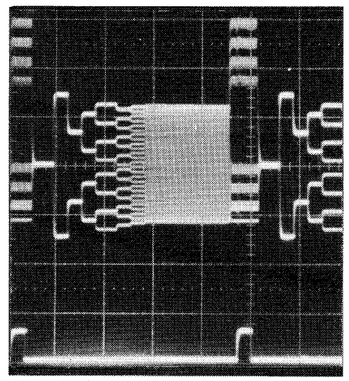
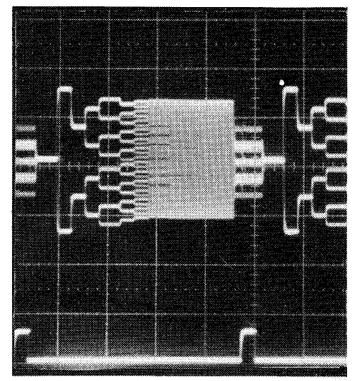
Set the delay time range to 640ms. If the waveform of D/A cycle jitters for a moment, a part of RAM's memory cells must be defective. When the output of a certain RAM is not delivered at all, the waveform will be as in the photos. When the defective RAM cannot be located, go to the All "1" & All "0" checks.

ALL "1" & ALL "0" TESTS

When the input signal is sinewave, the data in A/D, D/A, RAM, etc. vary with the lapse of time, causing each data bit to change to "1" or "0", and this makes it difficult to decide whether a bit is normal or not. The following method is prefarably empolyed to fix all bits at "1" or "0". Disconnect pin 7 of IC19 from R198 and R199. This means that the output of comparator IC19 is kept at "H" during A/D cycle and that each output from IC17 D11–D0 is greater than the value of input signal. In other words, input signal small than LSB (D0) is applied to the circuit. Then, curve A in the diagram appears on TP-6.
Next, short-circuit the DIN of IC17 to the ground. The waveform of TP-6 changes to B. The waveform of D/A cycle is reversed delaying for the period of delay time.
When the waveform level of A/D cycle is changed in 1/2 steps, then the D/A converter operation is normal. If it is difficult to check because a portion of the waveform near LSB is too small, gradually increase the oscilloscope sensitivity. Also, check D11–D0 pins of IC17 for presense of +5V or 0V.
If the waveform of D/A cycle is abnormal, observe the RAM1–RAM3 pins of IC17 individually.

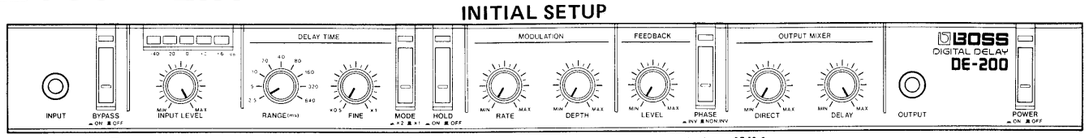


EXAMPLES OF RAM FAILURE
–No data on one RAM pin of Main Controller–

INPUT –20dBm 1kHz	RAM1 (IC15)	RAM2 (IC14)	RAM3 (IC13)
TP-6 TP-2 0.2ms/div			
TP-6 TP-5 5μs/div			

ADJUSTMENT

INITIAL SETUP



OFF x1 OFF NON. INV

1. LEVEL METER CALIBRATION

1-1. Apply –20dBm, 1kHz, sine waveform to INPUT jack.

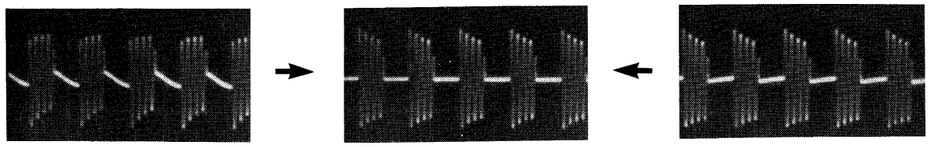
1-2. Adjust RT8 (LED LEVEL) so that 0dB (yellow) LED lights up.

2. COMPRESSOR

2-1. Apply 50mVp-p, 1kHz, 4-0-4 cycle burst tone signal to INPUT jack.

2-2. Connect the scope to TP-1.

2-3. Adjust RT9 (THD) for a straight DC level.



3. CV OFFSET

3-1. Turn FINE to X1.

3-2. Adjust RT12 (CV OFFSET) so that 0V is read at TP-3.

4. CLOCK FREQUENCIES

4-1. Connect a frequency counter or the scope to TP-5.

4-2. Turn FINE to X1 and adjust RT14 (CLOCK LOW) for 25.5 ± 0.2kHz or 38.91–39.53μs.

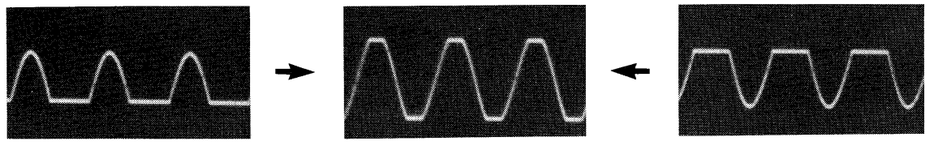
4-3. Turn FINE to X0.5 and adjust RT13 (CLOCK HIGH) for 52.5 ± 0.4kHz or 18.90–19.19μs.

5. A/D & D/A BIAS

5-1. Apply 3.5Vp-p, 200Hz, sine waveform to INPUT jack.

5-2. Connect the scope to pin 6 (7) of IC21.

5-3. Adjust RT15 (AD BIAS) for symmetrical waveforms.

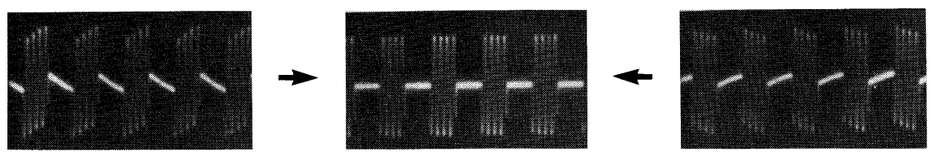


6. EXPANDER

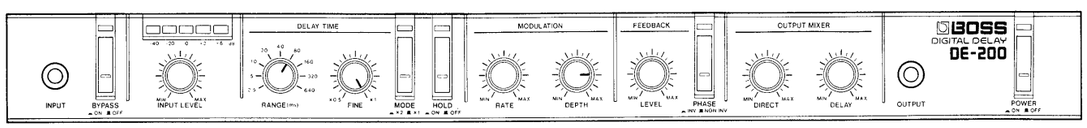
6-1. Apply 50mVp-p, 1kHz, 4-0-4 cycle burst signal to INPUT jack.

6-2. Connect the scope to TP-2.

6-3. Adjust RT10 (THD) for a straight DC level.



7. FEEDBACK

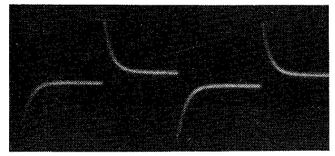
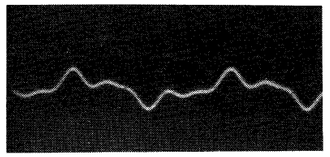
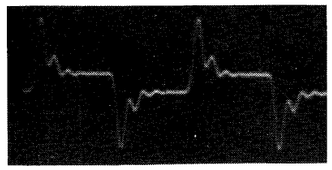
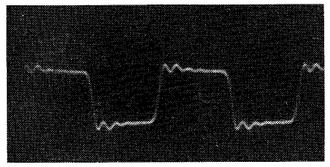
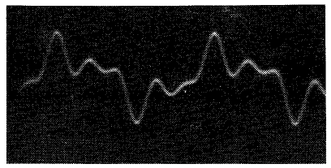
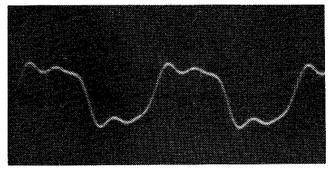
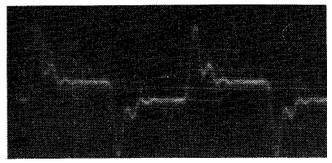
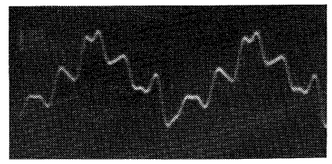
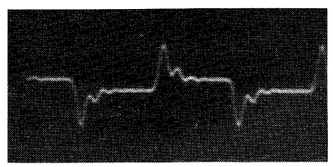
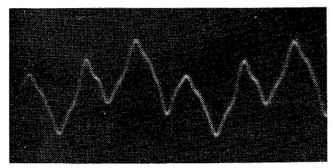
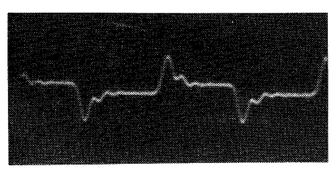
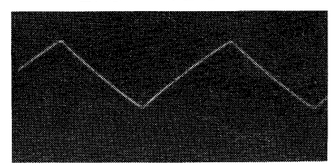


7-1. Connect MIX OUTPUT to amplifier/speaker.

7-2. Apply a signal (e.g. 90mVp-p, ⎍⎍, 1kHz) to INPUT jack for a moment and adjust RT11 (FEEDBACK) for infinite repetition (onset of regeneration).

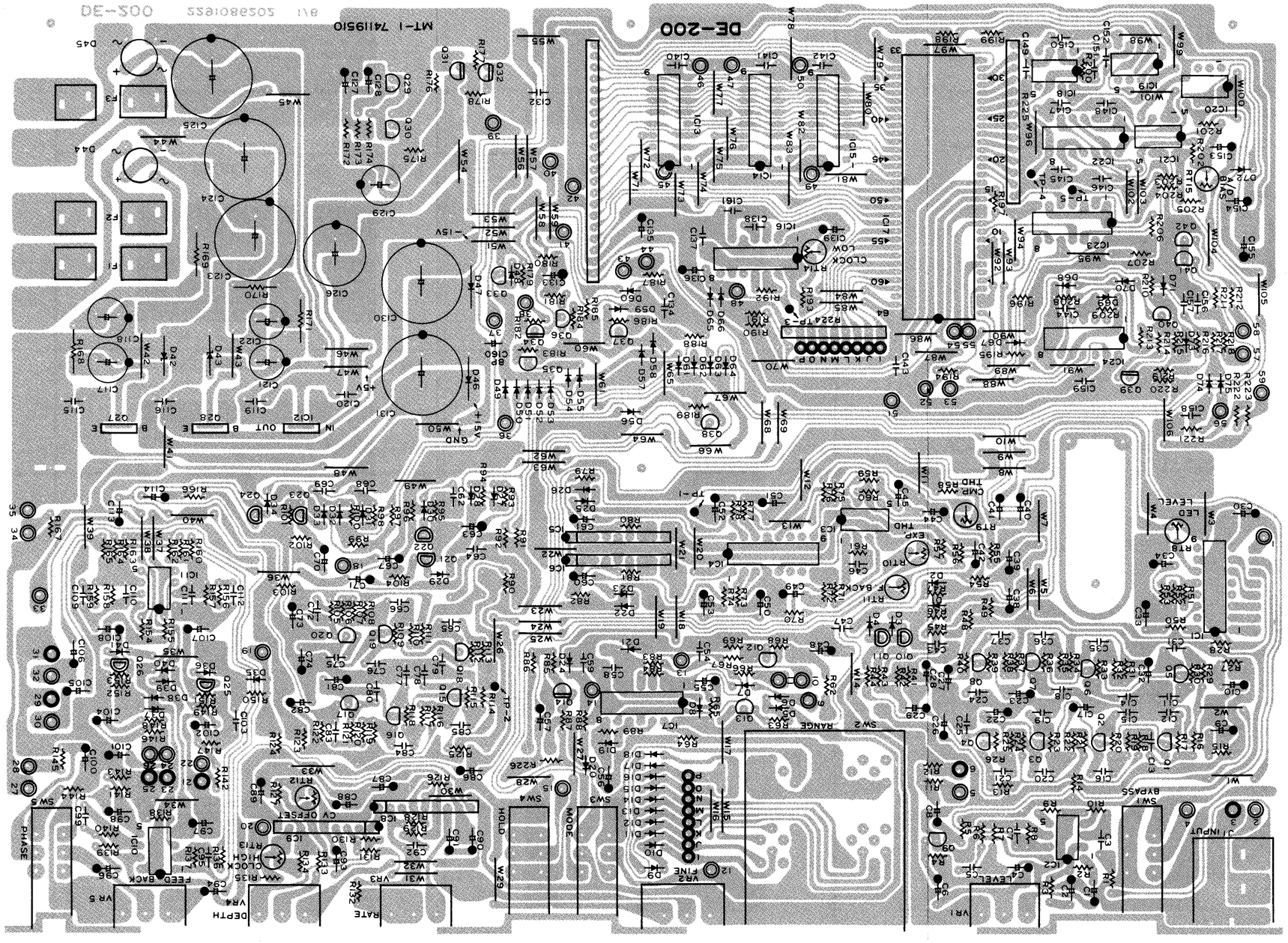
WAVEFORMS

INPUT SIGNAL 1kHz ⎍⎍ 100mVp-p

IC2 pin 7 1.8Vp-p 	Q23D 0.7Vp-p MODEx2 
TP-1 4.2Vp-p MODEx1 	MIX OUT 0.1V/div. MODEx1 
TP-1 2.9Vp-p MODEx2 	MIX OUT 0.1V/div. MODEx2 
TP-6 4Vp-p MODEx1 	MIX OUT 0.1V/div. MODEx1 FEEDBACK @5 
TP-2 1.5Vp-p MODEx1 	MIX OUT 0.1V/div. MODEx2 FEEDBACK @5 PHASE INV 
Q24D 1.2Vp-p MODEx1 	IC86 pin 7 20Vp-p 20ms/div. LFO RATE @ Max. 

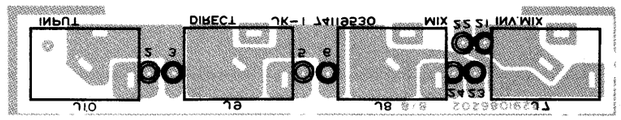
MAIN BOARD MT-1

(7411951000) (pcb 2291086202-1/8)



JACK BOARD JK-1

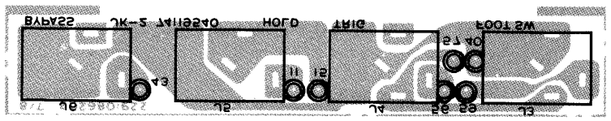
(7411953000) (pcb 2291086202-8/8)



View from foil side

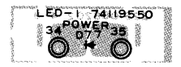
JACK BOARD JK-2

(7411954000) (pcb 2291086202-7/8)



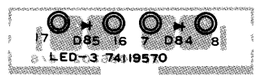
View from foil side

LED BOARDS



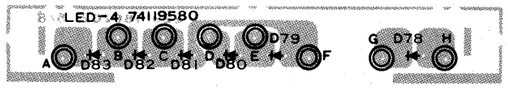
LED-1 (7411955000)
(pcb 2291086202-4/8)

LED-2 (7411956000)
(pcb 2291086202-2/8)



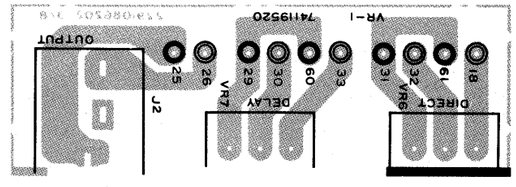
LED-3 (7411957000)
(pcb 2291086202-6/8)

LED-4 (7411958000) (pcb 2291086202-5/8)

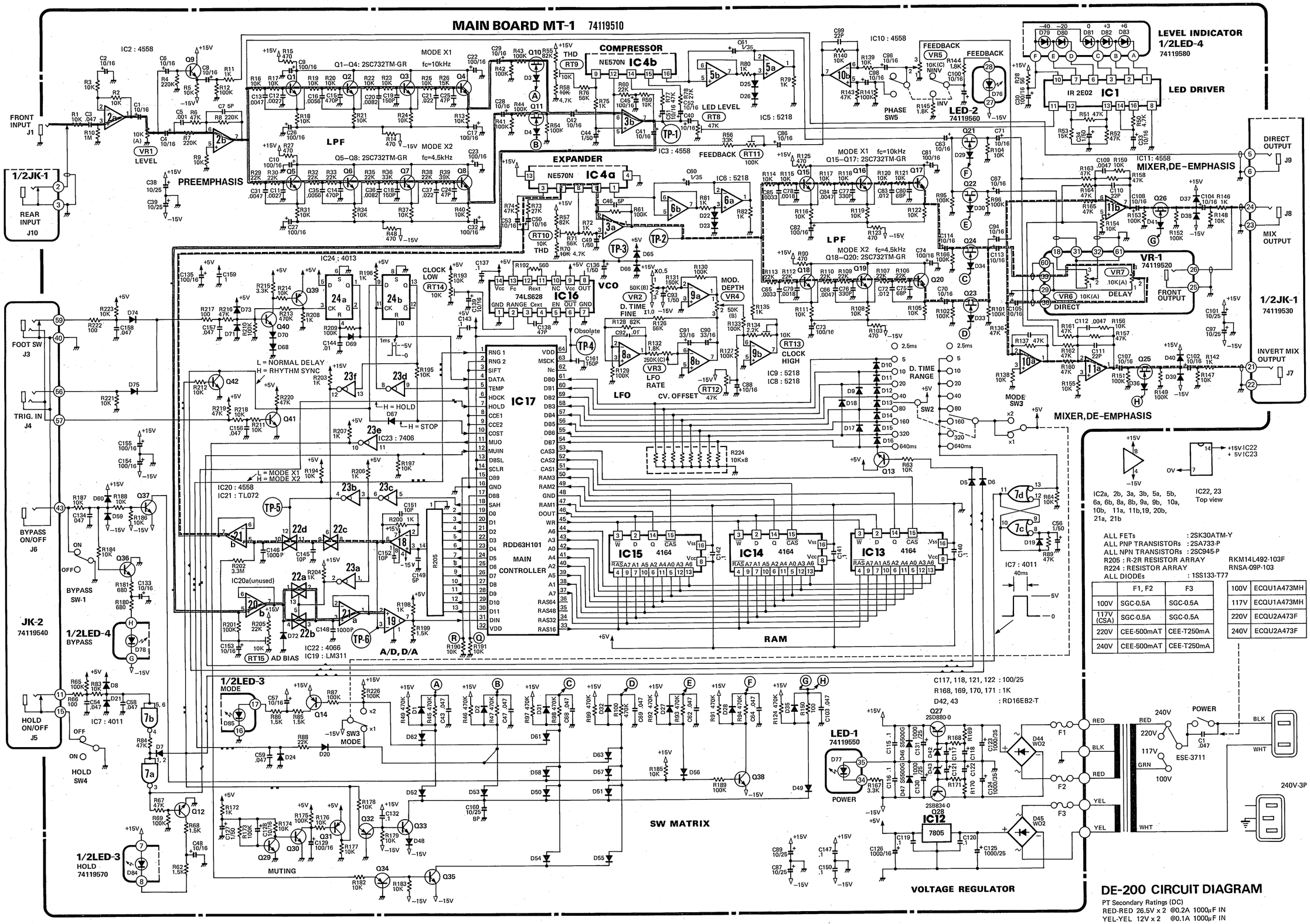


VR BOARD VR-1

(7411952000) (pcb 2291086202-3/8)



CIRCUIT DIAGRAM



	F1, F2	F3
100V	SGC-0.5A	SGC-0.5A
117V (CSA)	SGC-0.5A	SGC-0.5A
220V	CEE-500mAT	CEE-T250mA
240V	CEE-500mAT	CEE-T250mA

100V	ECQU1A473MH
117V	ECQU1A473MH
220V	ECQU2A473F
240V	ECQU2A473F

DE-200 CIRCUIT DIAGRAM

PT Secondary Ratings (DC)
RED-RED 26.5V x 2 @0.2A 1000μF IN
YEL-YEL 12V x 2 @0.1A 1000μF IN

PARTS LIST

CASE ケース

2281040900	Chassis	シャーシ
2212051600	Bracket (Center frame)	アングル（電源SW取付用）
2221039500	Rear panel	背面パネル
2202023500	Top cover	上カバー
2202023600	Bottom cover	底カバー
2235031300	Base (foot)	ベース（ゴム足）
2221071800	Front Panel	前面パネル
2212051700	Rack angle	ラック・アングル

POWER TRANSFORMER 電源トランス

22450366U0	

SWITCH スイッチ

13129124	SDGA-3P	Push プッシュ	power
13169503	ESE-3711	Voltage selector	電圧切替
2202023700	Switch cover スイッチカバー		
13119808	SRJ4049	Rotary ロータリ	range
13129342	SUF12	Push プッシュ	

IC

15229811	RDD63H101	Main controller
15179314	HM4864P-3 (4164)	64K D-RAM
15169356	SN74LS628N	VCO
15169102H0	HD7406P	Hex inverters
15159115H0	HD14066BP	Analog SW
15159105H0	HD14013BP	D-FF
15159104H0	HD14011BP	NAND gates
15189129	TL072	OP amp
15189152	NJM5534D	OP amp
15189102	NJM4558DD	OP amp
15189136	M5218L	OP amp
15219108	NE570	Compander
or		
15219143	μPC1571C	
15219116	IR-2E02	Level meter
15189167	μPC271C	Comparator
15199106F0	μA7805UC	Voltage regulator

TRANSISTOR トランジスタ

15119805	2SB834-O
15129815	2SD880-O
15129104	2SC732TM-GR
15129108	2SC945-P
15119105	2SA733-P

FET

15139101	2SK30ATM-Y
15139103	2SK30ATM-GR

DIODE ダイオード

15019126	1SS-133T-77	
15019652	RD5.6EB2-T	Zener
15019654	RD16EB2-T	Zener
15019209T0	S550OG	
15019236	W02	Rectifier bridge

LED

15029128	GL9PR2	RED 赤
15029135	GL9NG2	GRN 緑
15029167	GL9HY2	YEL 黄

POTENTIOMETER ボリューム

13219363	EVH-6PA332A14	10KA
13219364	EVH-6PA332C14	10KC
13219342	EVH-6PA332B54	50KB
13219365	EVH-6PA332CF5	250KC

TRIMMER POT. 半固定ボリューム

13299140	H0651A013-10KB
13299158	H0651A019-47KB
13299160	H0651A001-100KB

RESISTOR ARRAY 抵抗アレイ

13910103	RNSA-09P103
13919134	RKM14L492-103F

JACK ジャック

13449244	HLJ0605-01-090	RHYTHM SYNC
13449139	HLJ0605-01-100	REMOTE, OUT, IN (rear)
13449138	HLJ2317-01-100	IN, OUT (front)

KNOB, BUTTON ツマミ、ボタン

2247025900	Knob ツマミ	ORN 橙
2247026000	Knob ツマミ	GRN 緑
2247026100	Knob ツマミ	YEL 黄
2247026200	Knob ツマミ	BLU 青
2247057900	Button ボタン	Push switch プッシュ・スイッチ

FUSE, FUSE HOLDER ヒューズ、ヒューズホルダ

12559353	SGC 0.25A	
12559355	SGC 0.5A	
12559508	CEE T250mA	
12559511	CEE T500mA	
12199542	SN5057	Fuse holder ヒューズホルダ

PCB 基板完

7411951000	MT-1	Main (pcb 2291086202-1/8)
7411952000	VR-1	VR (pcb 2291086202-3/8)
7411953000	JK-1	Jack (pcb 2291086202-8/8)
7411954000	JK-2	Jack (pcb 2291086202-7/8)
7411955000	LED-1	LED (pcb 2291086202-4/8)
7411956000	LED-2	LED (pcb 2291086202-2/8)
7411957000	LED-3	LED (pcb 2291086202-6/8)
7411958000	LED-4	LED (pcb 2291086202-5/8)

AC INLET インレット

13429707	SOT-17	2P
13429708	CM-3	3P
2202082000	Inlet cover spacer (Inlet-Panel)	2P only
	インレット・カバー・スペーサ	

OTHERS その他

2246011800	Heat sink ヒートシンク	
2347014700	Flat cable フラットケーブル	8P
2225022000	Shield cover (copper)	Jack Board
	シールド・カバー