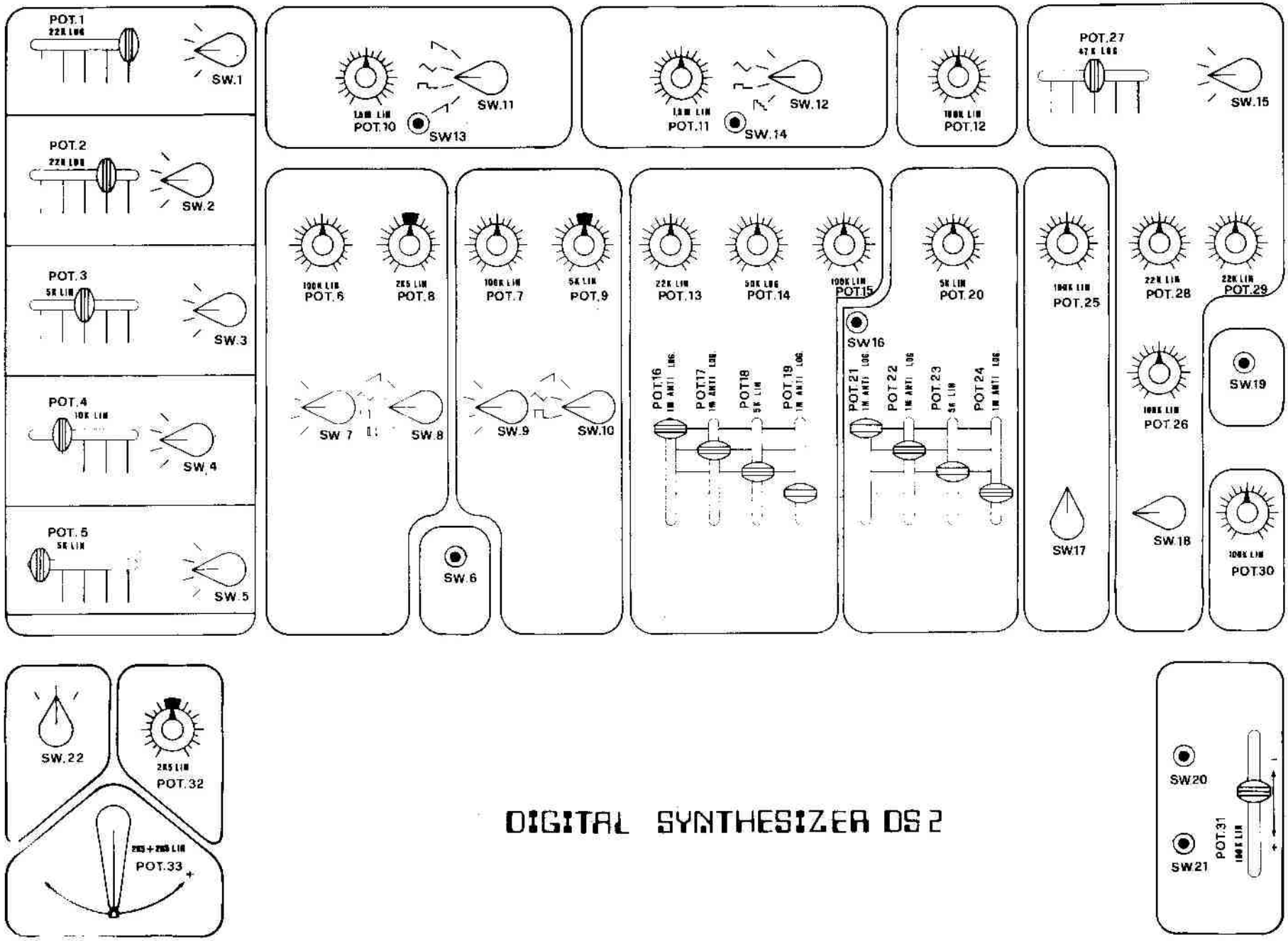
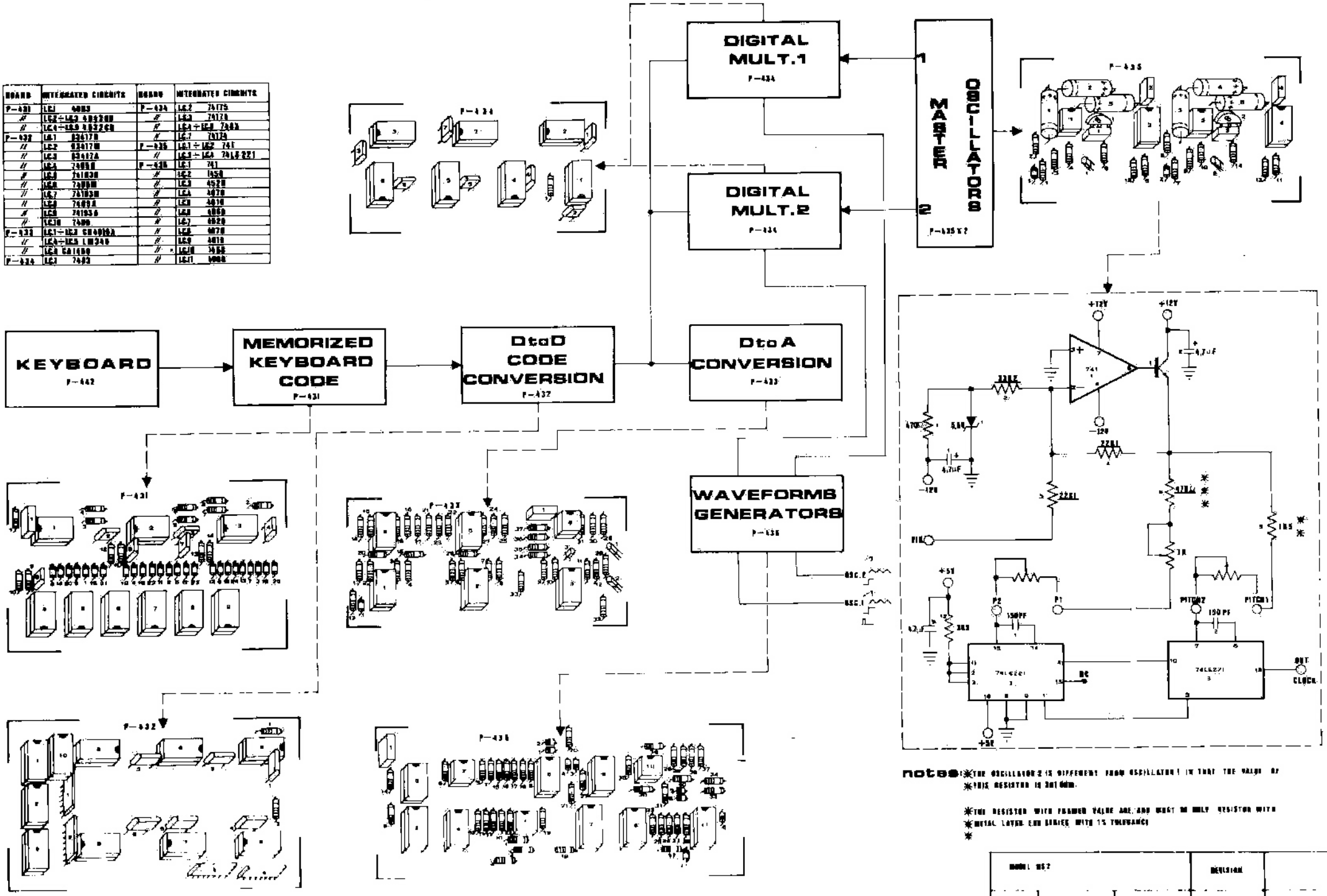


MODEL DS2			REVISION
DATE	DRAWN BY	DESIGNED BY	DATE

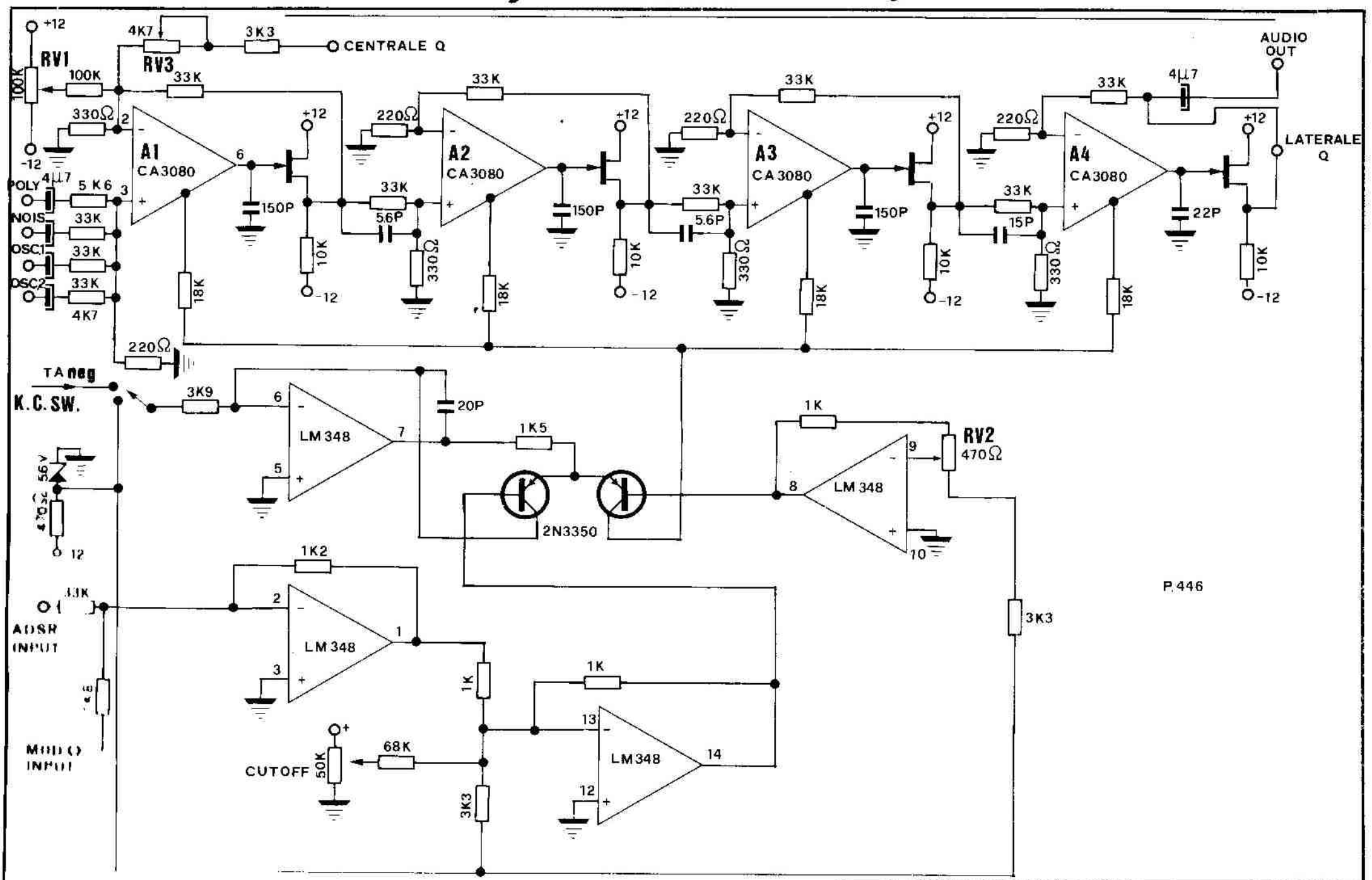
BOARD	INTEGRATED CIRCUITS	BOARD	INTEGRATED CIRCUITS
P-431	LC1 4083	P-434	LC2 74175
//	LC2÷LC3 4042CB	//	LC3 74174
//	LC4÷LC5 4532CB	//	LC4÷LC6 7483
P-432	LC1 93417B	//	LC7 74174
//	LC2 93417B	P-435	LC1÷LC2 741
//	LC3 93417A	//	LC3÷LC4 74LS221
//	LC4 74050	P-436	LC1 741
//	LC5 74103B	//	LC2 1458
//	LC6 74050	//	LC3 4520
//	LC7 74103B	//	LC4 4070
//	LC8 74093A	//	LC5 4010
//	LC9 74193A	//	LC6 4060
//	LC10 7400	//	LC7 4020
P-433	LC1÷LC3 CD4016A	//	LC8 4070
//	LC4÷LC5 LM348	//	LC9 4010
//	LC6 CA1450	//	LC10 1458
P-434	LC1 7483	//	LC11 4000

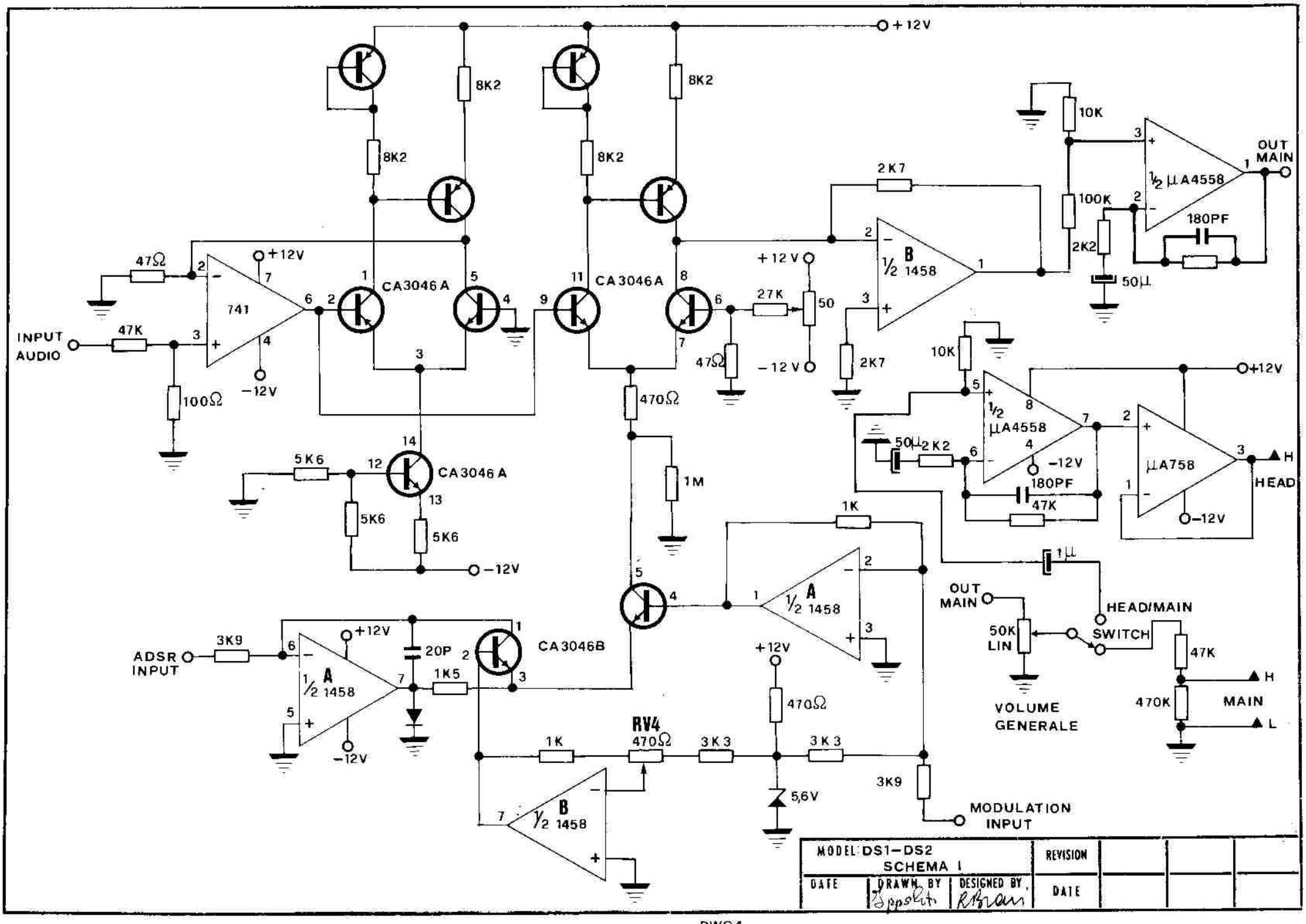


notes: ✱THE OSCILLATOR 2 IS DIFFERENT FROM OSCILLATOR 1 IN THAT THE VALUE OF
✱THIS RESISTOR IS 3K1 OHM.

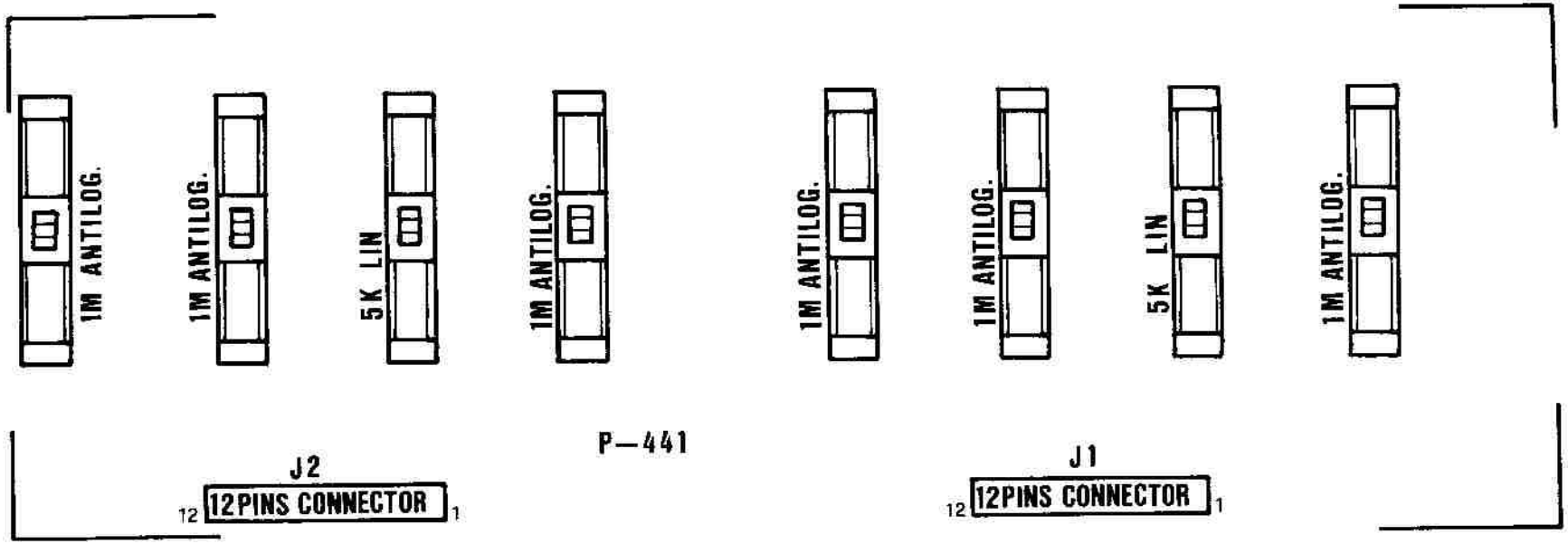
✱THE RESISTOR WITH FRAMED VALUE ARE AND MUST BE ONLY RESISTOR WITH
✱METAL LAYER FOR SERIES WITH 1% TOLERANCE
✱

MODEL MS2			REVISION
DATE 7/1/78	DRAWN BY	DESIGNED BY	DATE


+12
RV1
100K
-12
4K7
RV3
3K3
CENTRALE Q
AUDIO OUT
33K
330Ω
A1
CA3080
150P
10K
5.6P
330Ω
18K
220Ω
A2
CA3080
A3
CA3080
A4
CA3080
4µ7
LATERALE Q
22P
15P
POLY
NOIS
OSC1
OSC2
5K6
TA neg
K.C.SW.
3K9
LM348
20P
1K5
2N3350
1K
RV2
470Ω
56V
1K2
ADSR INPUT
MIDI INPUT
CUTOFF
50K
68K
3K3
P.446
DWG3
MODEL DS1-DS2
SCHEMA H
REVISION
DATE
DRAWN BY
DESIGNED BY


+12V
8K2
8K2
8K2
8K2
10K
OUT MAIN
½ µA4558
100K
2K7
180PF
2K2
50µ
B
½ 1458
+12V
27K
50
47Ω
-12V
2K7
47Ω
741
+12V
-12V
INPUT AUDIO
47K
100Ω
CA3046A
CA3046A
470Ω
1M
5K6
CA3046A
5K6
5K6
-12V
10K
+12V
½ µA4558
50µ
2K2
-12V
180PF
47K
µA758
H
HEAD
-12V
1K
A
½ 1458
1µ
OUT MAIN
HEAD/MAIN
50K LIN
SWITCH
47K
H
470K
MAIN
L
VOLUME GENERALE
ADSR INPUT
3K9
+12V
20P
CA3046B
A
½ 1458
1K5
-12V
+12V
470Ω
RV4
470Ω
1K
3K3
3K3
5,6V
3K9
B
½ 1458
MODULATION INPUT
MODEL DS1–DS2
SCHEMA I
REVISION
DATE
DRAWN BY
DESIGNED BY
DATE

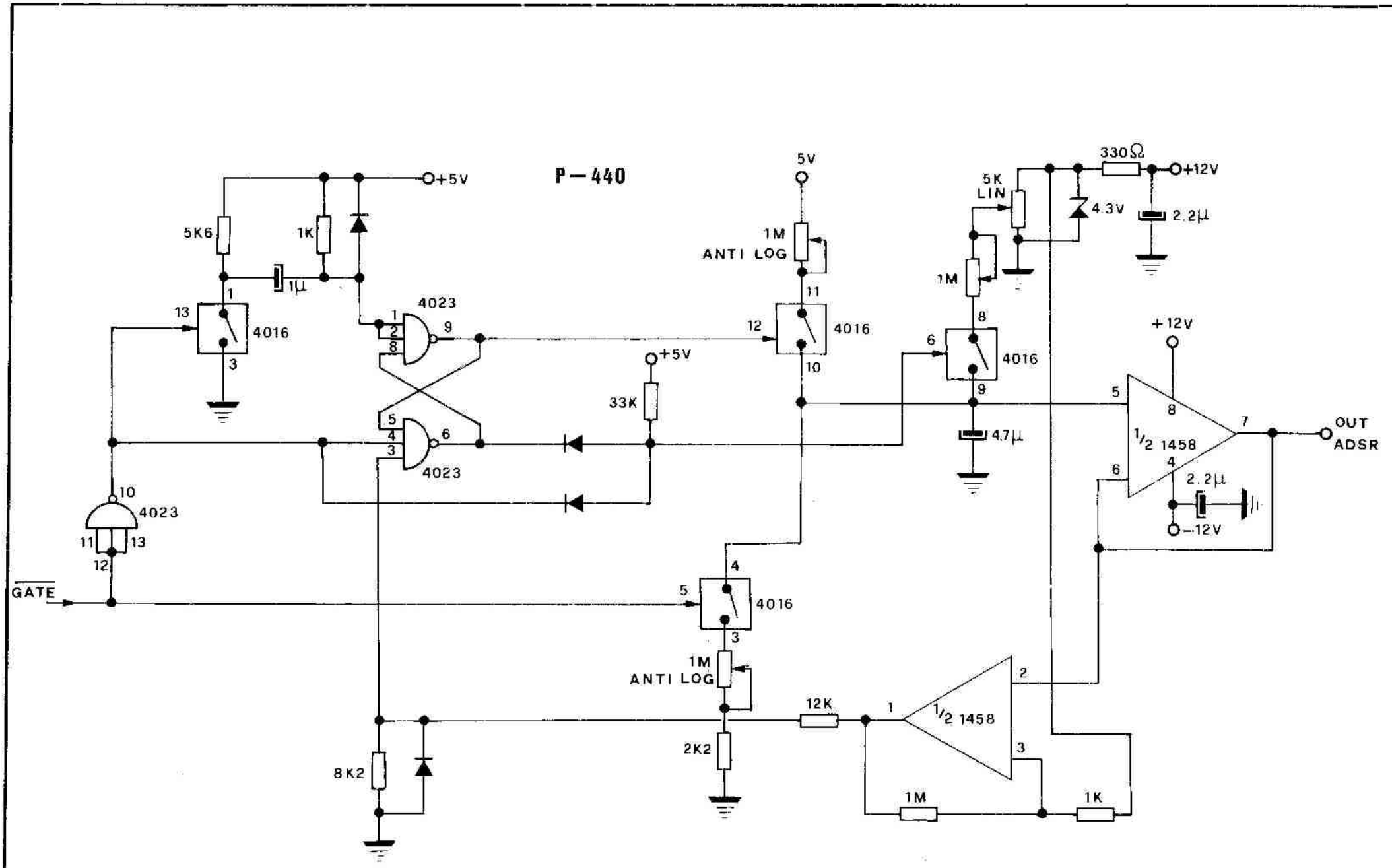
DWG4



PIN	REFERENCE J2	PIN	REFERENCE J1
1	OUT ADSR VCF	1	+12V
2	" " "	2	−12V
3	" " "	3	R POT.
4	+5V	4	S POT.
5	R POT.	5	GND
6	S POT.	6	"
7	GND	7	"
8	"	8	"
9	"	9	D POT.
10	"	10	A POT.
11	D POT.	11	GATE
12	A POT.	12	OUT ADSR VCA

DWG8

MODEL	DS2 SCHEMA 1		REVISION		
DATE	DRAWN BY	DESIGNED BY	DATE		



MODEL DS1–DS2 SCHEMA L			REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

DWG6

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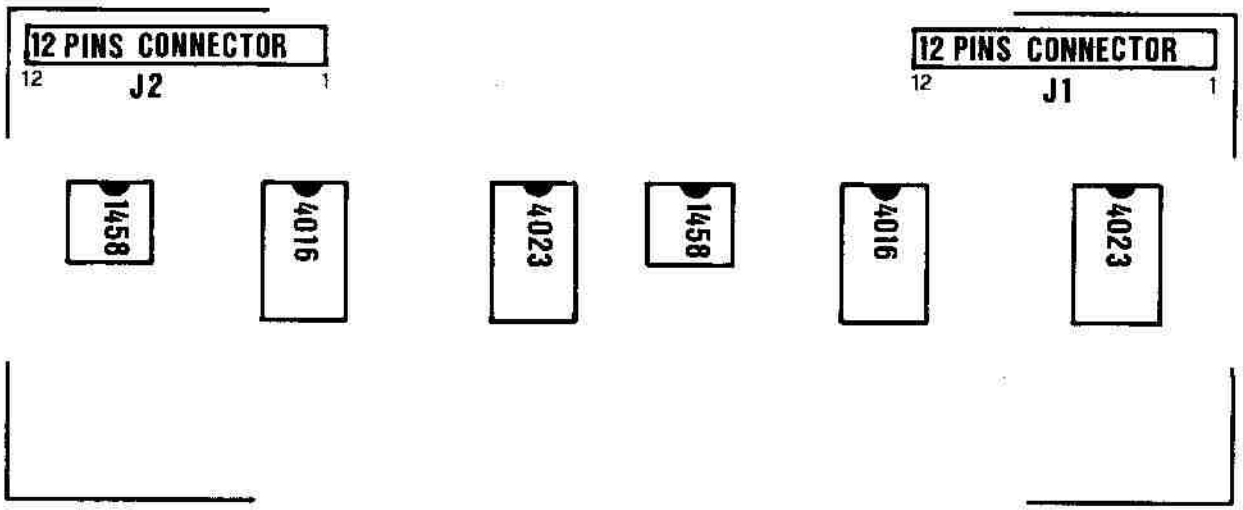
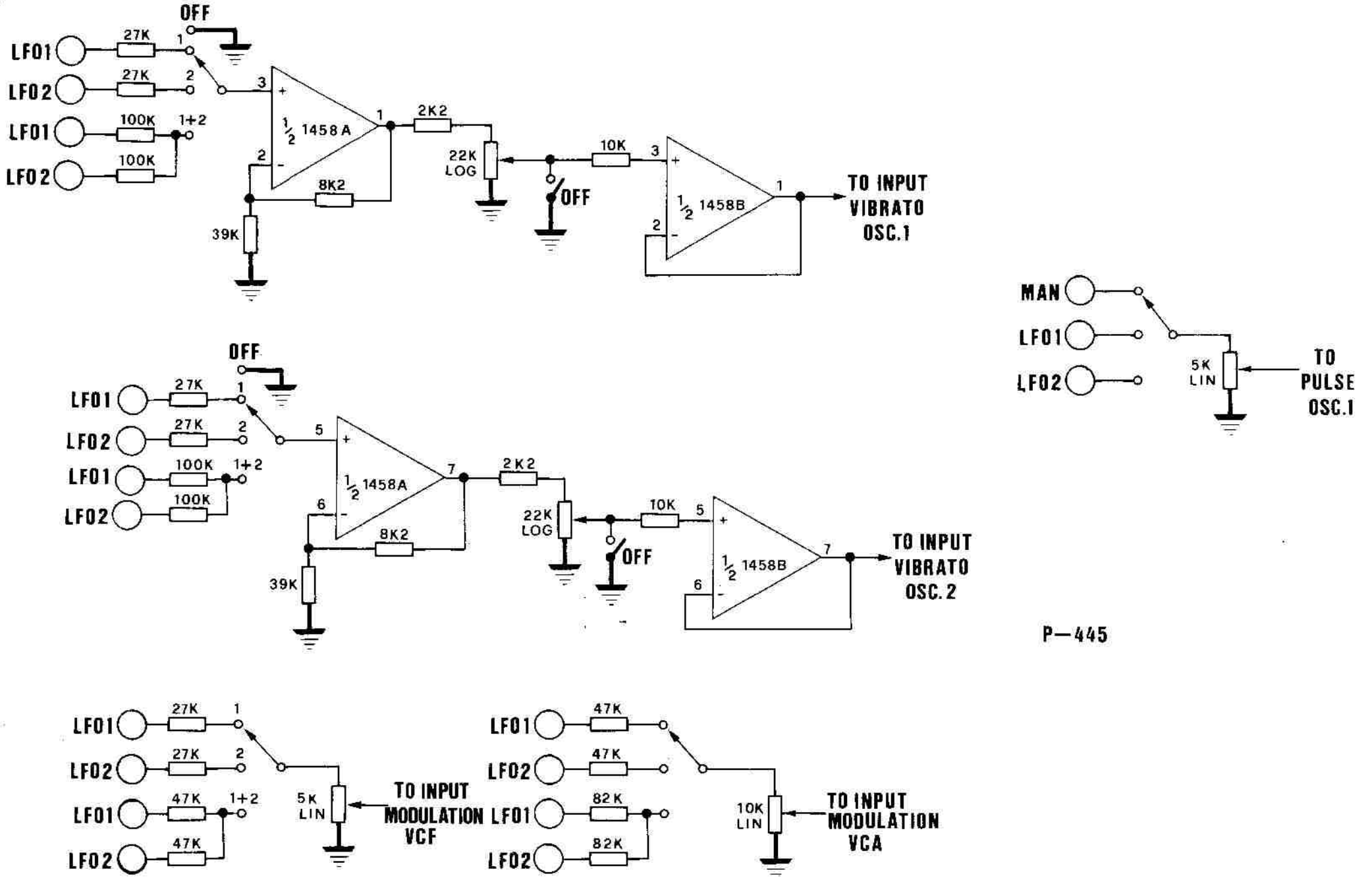


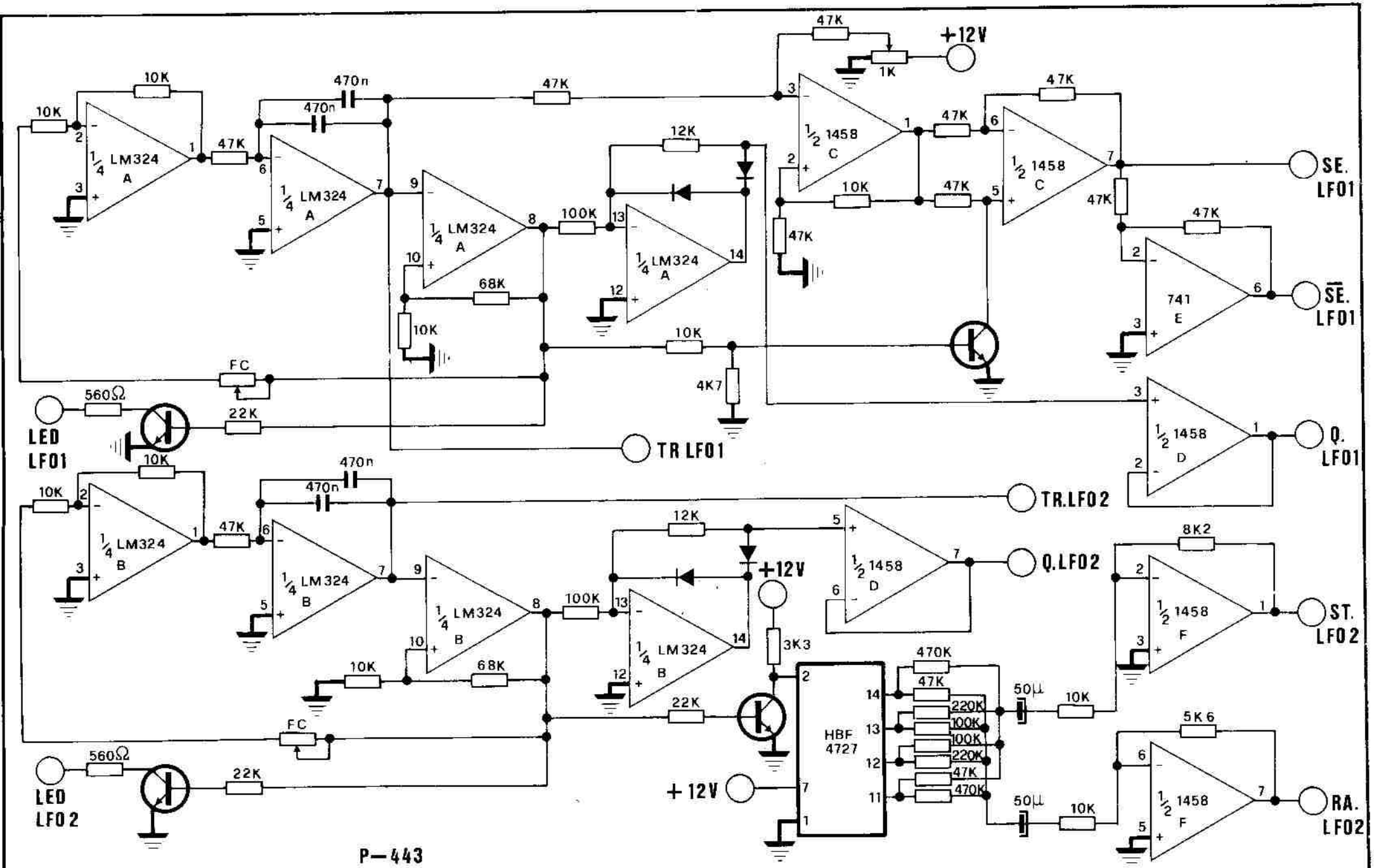
PIN	REFERENCE J1	PIN	REFERENCE J2
1	+12V	1	OUT ADSR VCF
2	−12V	2	
3	R POT	3	
4	S POT	4	+5V
5	GND	5	R POT
6	GND	6	S POT
7	GND	7	GND
8	GND	8	GND
9	D POT	9	GND
10	A POT	10	GND
11	GATE	11	D POT
12	OUT ADSR VCA	12	A POT

MODEL DS DS SCHEMA L			REVISION	-		
DATE	DRAWN BY Ippolito	DESIGNED BY R Bran	DATE			

DWG 7



MODEL	DS2 SCHEMA M		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			



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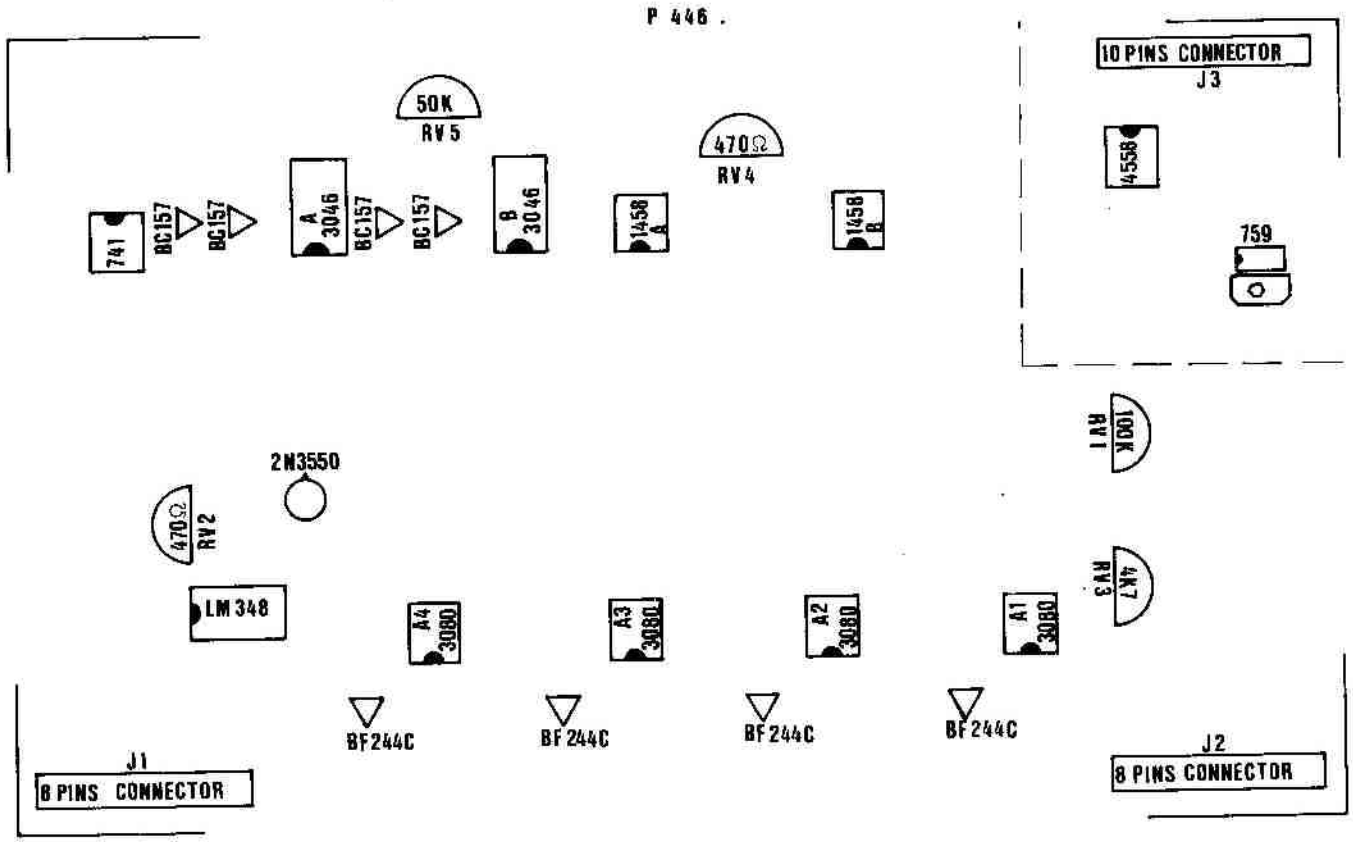
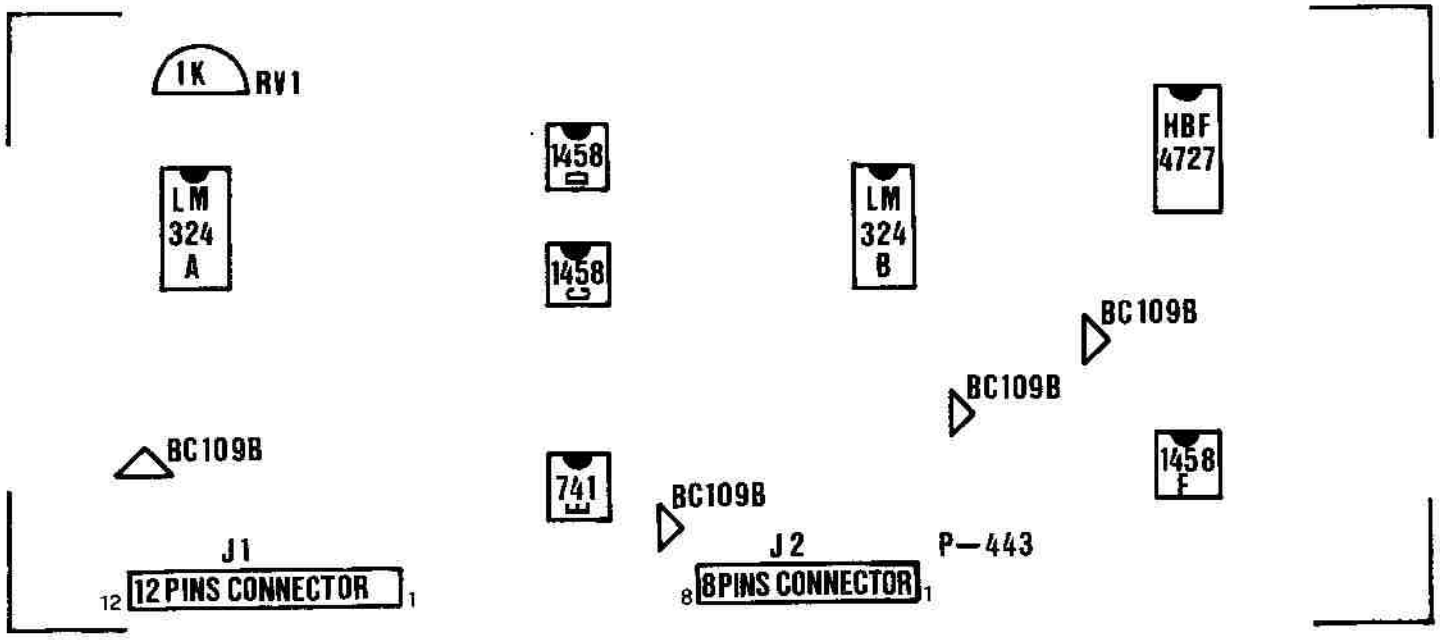
MODEL	DS2 SCHEMA N		REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE			

DWG 9



PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	−5.6V	1 2	GND	1	ADSR VCA
2	CUTOFF POT	3	RESON CENTR.	2	MODULAT INPUT
3	GND	4	POLY	3	−12V
4	MODULAT INPUT	5	NOISE	4	+12V
5	ADSR VCF	6	OSC 1	5	GND
6	KT SW TA	7	OSC 2	6	GND
7	RESONANCE LATER.	8		7	OUT VOL GEN
8	GND			8	INPUT HEAD PH
				9	GND
				10	OUT HEAD PH

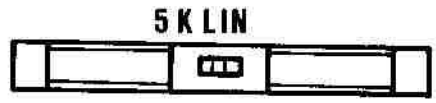
SCHEMA
REVISION
DATE
DRAWN BY
DESIGNED BY
DATE



PIN	REFERENCE J1
1	SE. LFO1
2	SE. LFO1
3	QUADRA LFO1
4	FC LFO1
5	−12V
6	TRI. LFO1
7	GND
8	"
9	"
10	LED LFO1
11	FC LFO1
12	+12V

PIN	REFERENCE J2
1	STAIRCASE
2	"
3	SeH
4	LED LFO2
5	FC LFO2
6	QUADRA LFO2
7	TRI. LFO2
8	FC LFO2

MODEL	DS2 SCHEMA N		REVISION			
DATE	DRAWN BY Bondai G.	DESIGNED BY R Bran	DATE			



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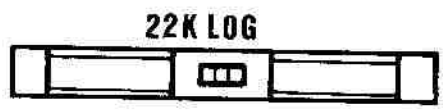
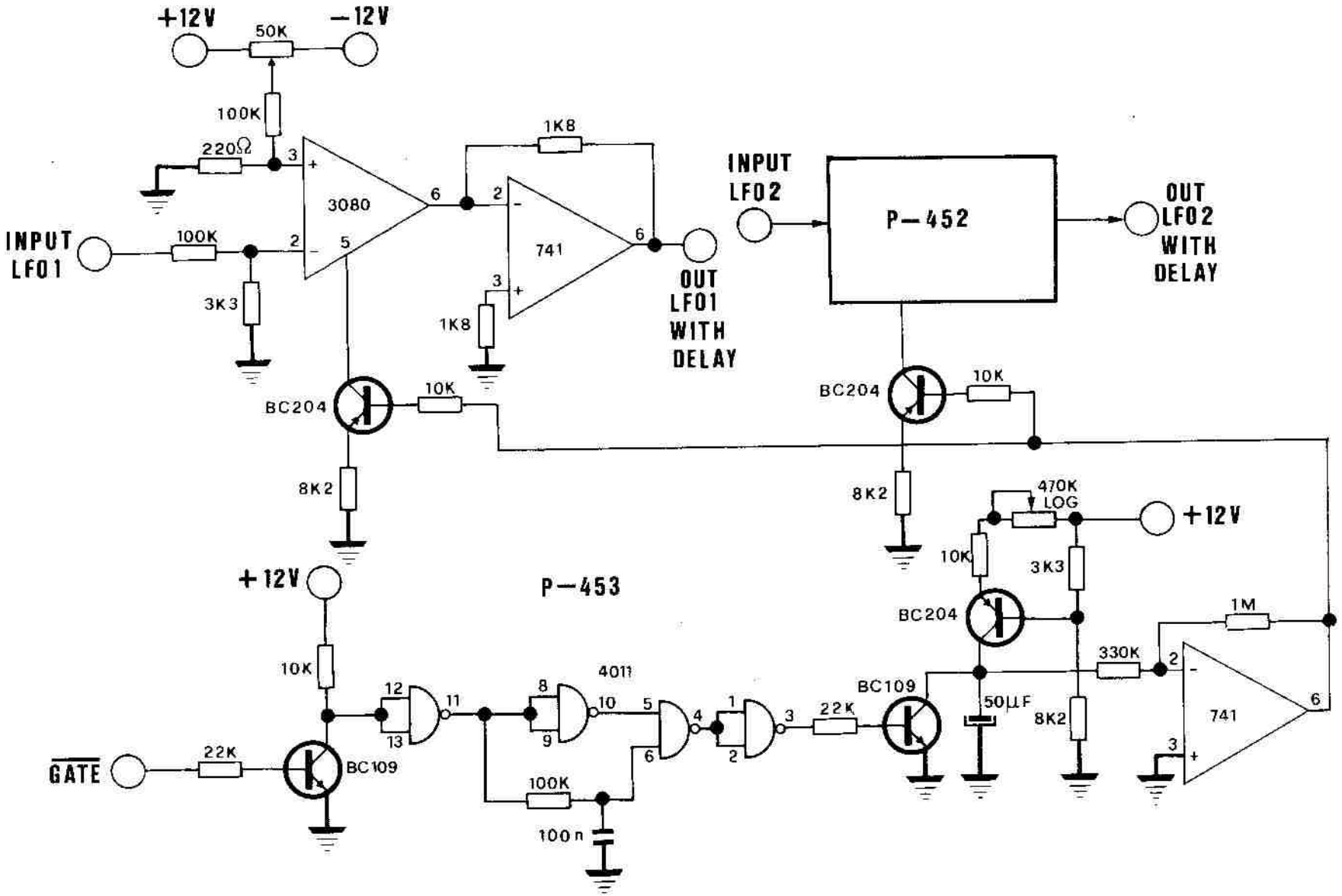
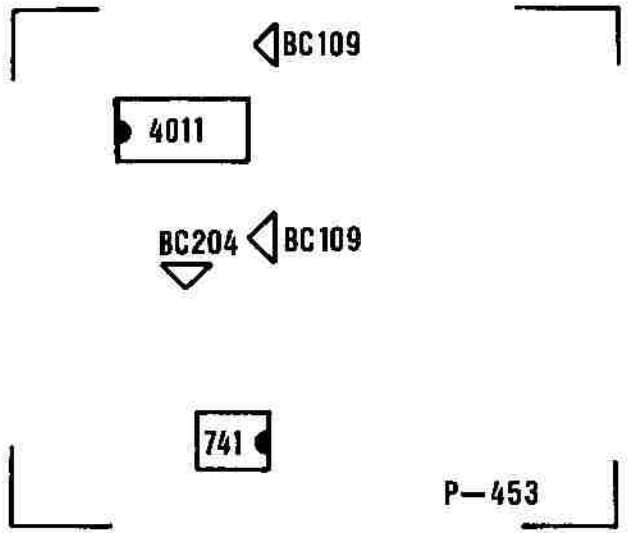


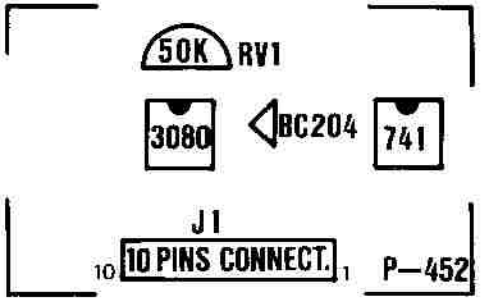
MODEL	DS2 SCHEMA M		REVISION			
DATE	DRAWN BY Bordoni G.	DESIGNED BY R Bordoni	DATE			

DWG 12



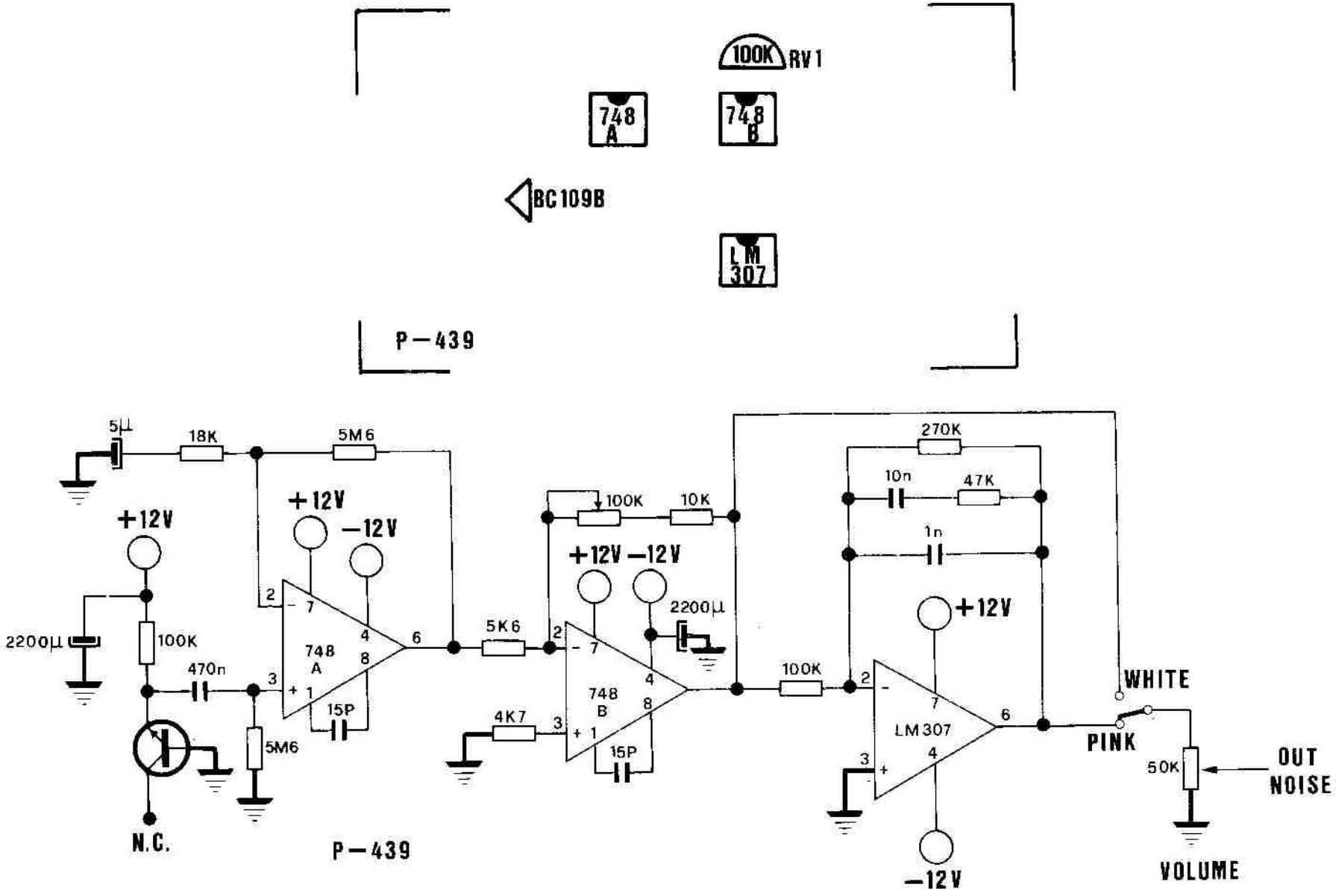
MODEL	DS2 SCHEMA O	REVISION			
DATE	DRAWN BY	DESIGNED BY	DATE		



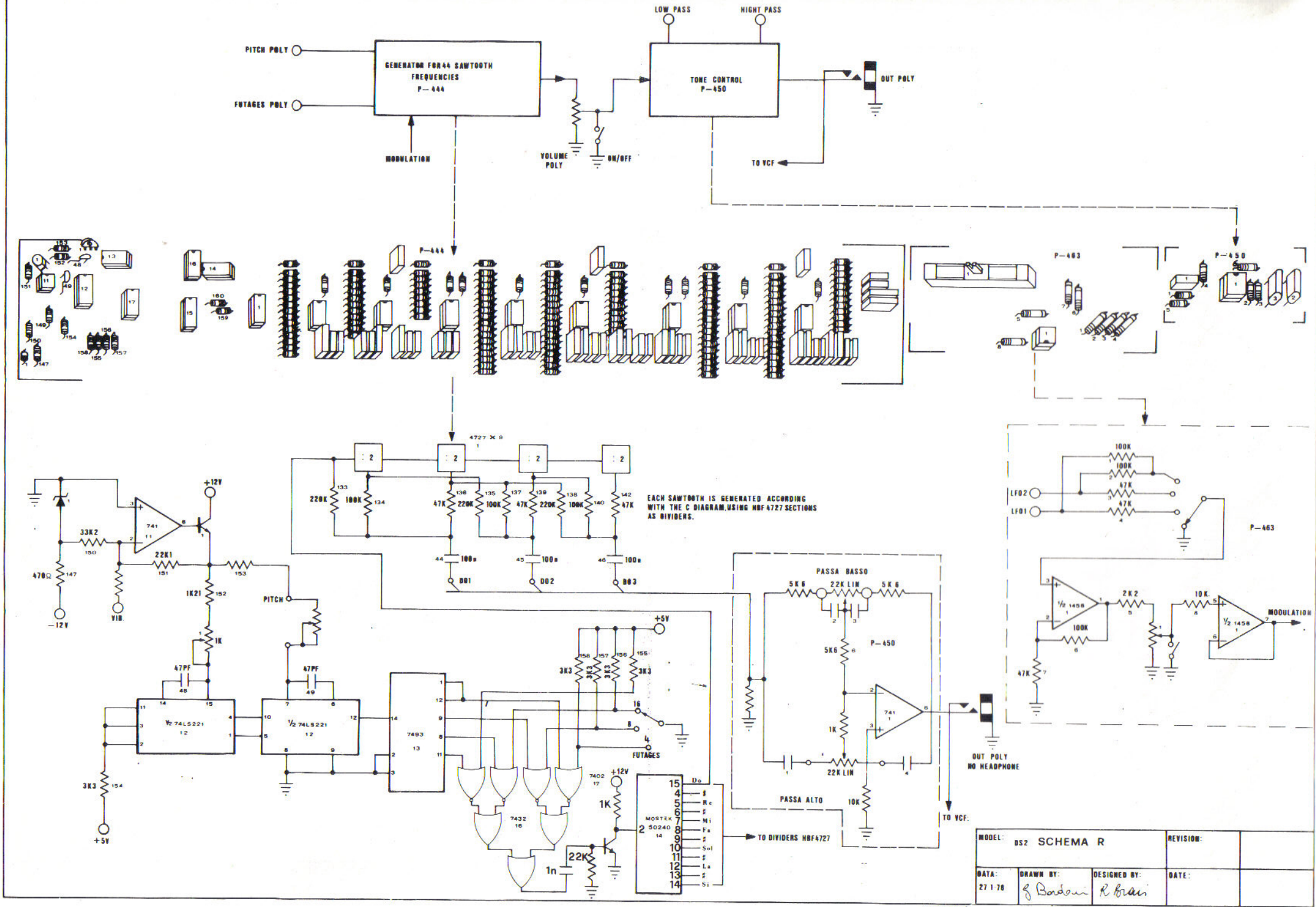


PIN	REFERENCE J1
1	+12V
2	OUT LFO1 or LFO2 WITH DELAY
3	PIN 6 741
4	−12V
5	GND
6	"
7	"
8	INP. LFO1 or LFO2
9	" " " "
10	" " " "

MODEL	DS2 SCHEMA Q		REVISION			
DATE	DRAWN BY Bordai G.	DESIGNED BY R Bordai	DATE			

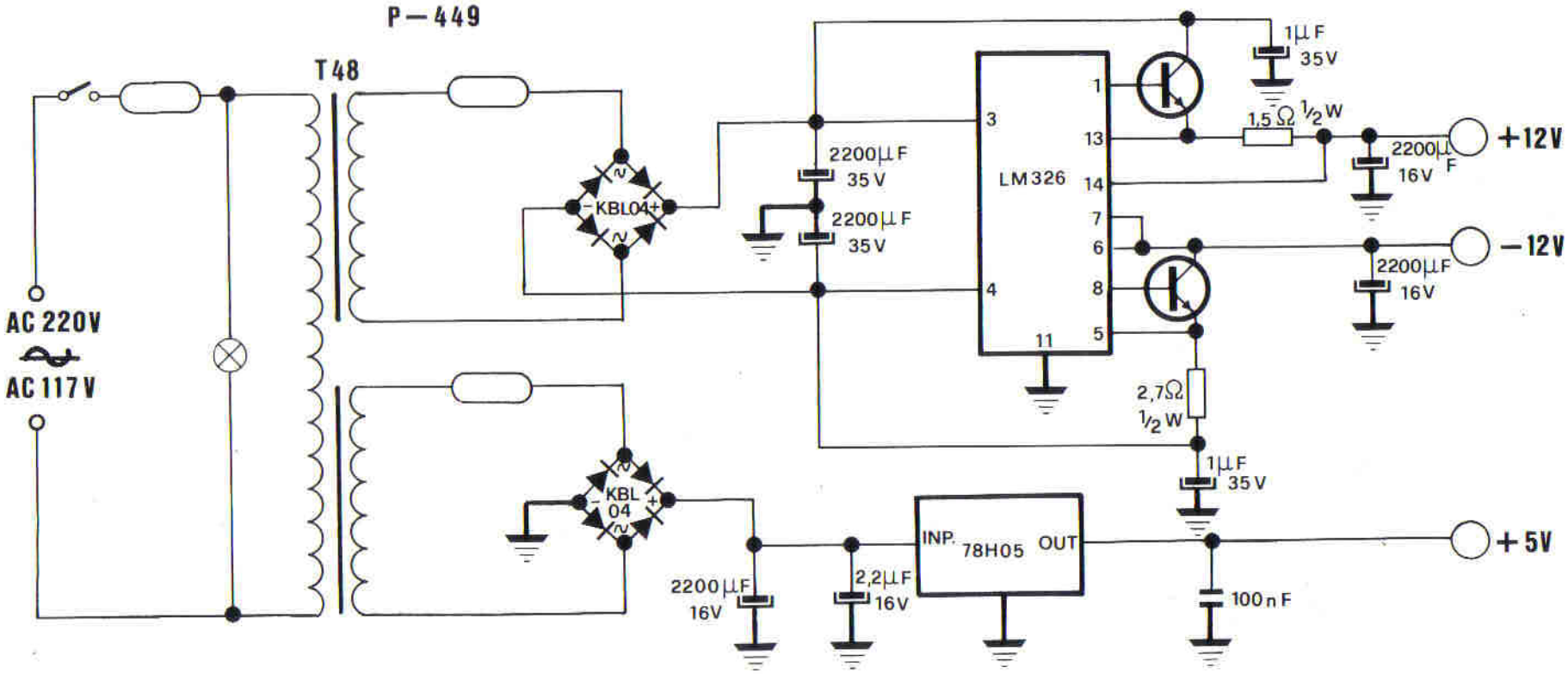


MODEL DS1 DS2 SCHEMA O			REVISION			
DATE	DRAWN BY Bordoni G.	DESIGNED BY R Brain	DATE			



MODEL: DS2 SCHEMA R			REVISION:	
DATA: 27 1 78	DRAWN BY: J Bordeau	DESIGNED BY: R Brau	DATE:	

DWG 16



MODEL DS2 SCHEMA P			REVISION			
DATE	DRAWN BY Bordain G.	DESIGNED BY R Brain	DATE			

DWG17

LM
326

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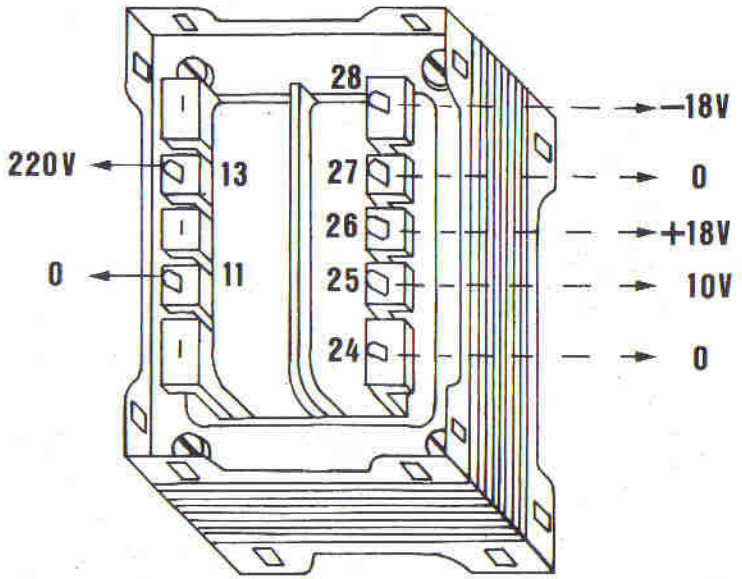

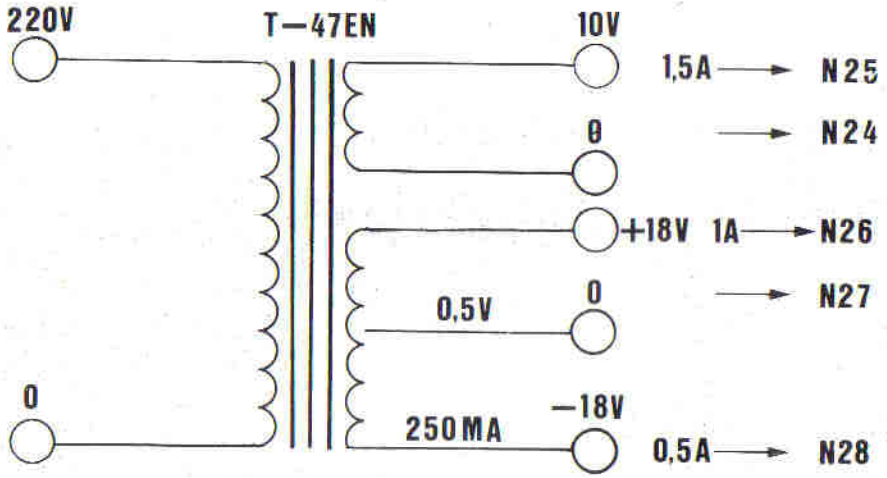

MODEL	DS2 SCHEMA P		REVISION			
DATE	DRAWN BY Bordoni G.	DESIGNED BY R Brai	DATE			