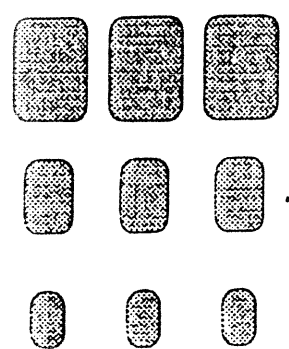


7
6
5
4
3
2
1

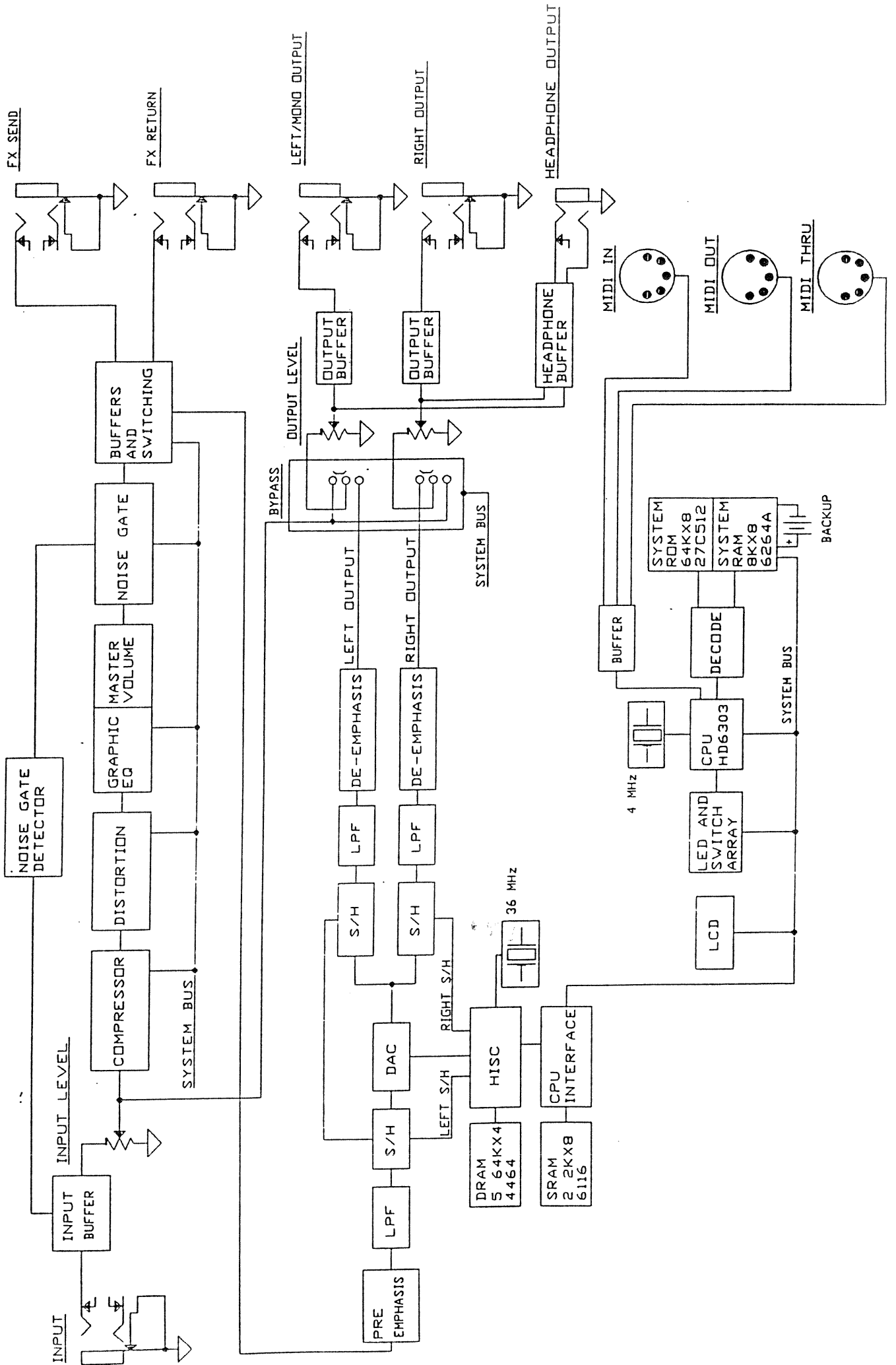


RP-1

Service Manual

- **BLOCK DIAGRAM**
- **SETUP PROCEDURES**
- **SCHEMATIC DIAGRAMS**
- **PARTS LISTS**
- **PC BOARDS**
- **HISC PINOUT**
- **HISC PIN DESCRIPTIONS**

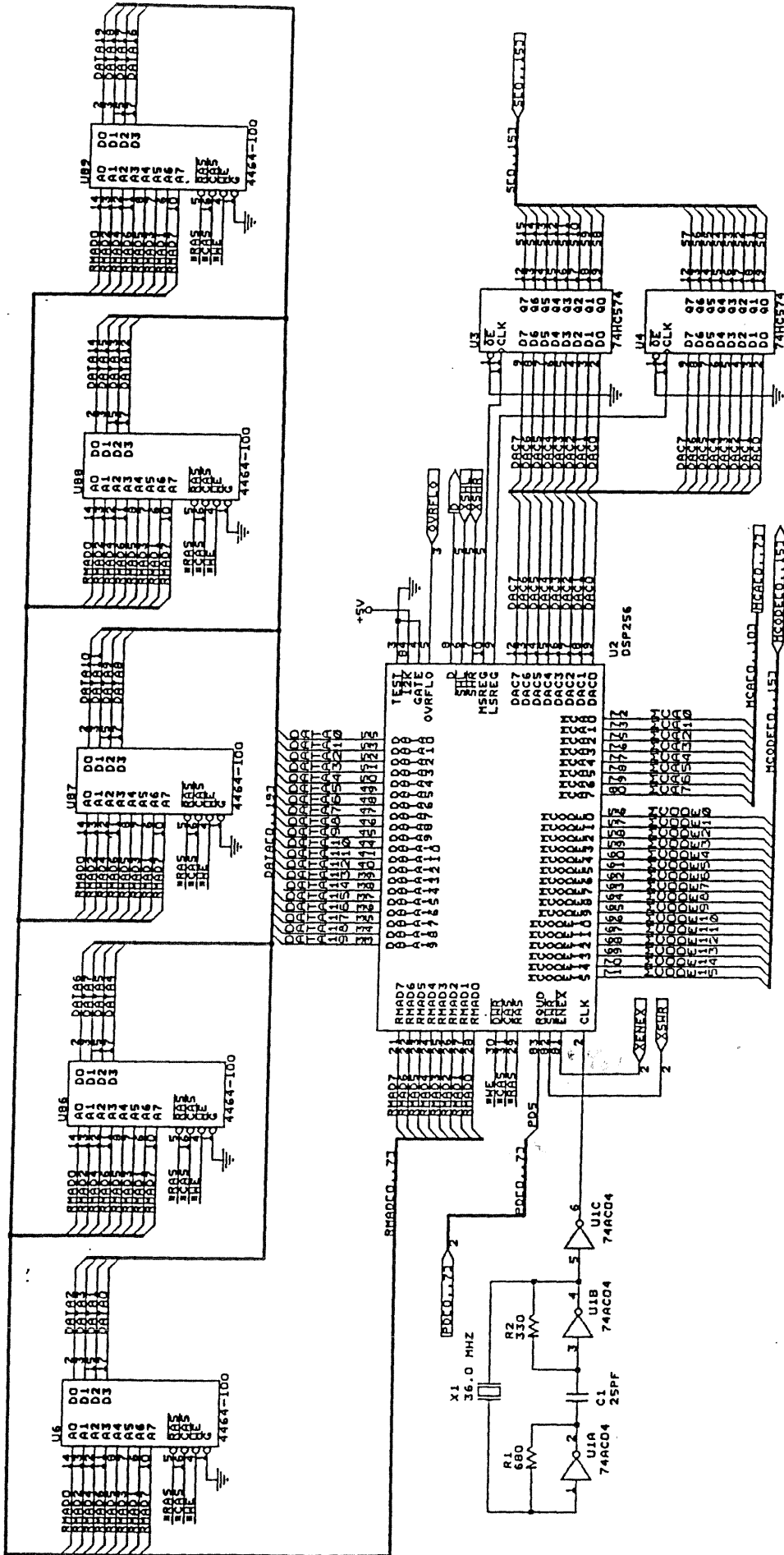
RPf BLOCK DIAGRAM



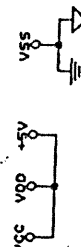
RP-1 Setup and Test Procedures

To access the RP-1 setup and test menus, enter the UTILITY mode and scroll left or right until the software version number is displayed. Press the parameter down button twice to enter the test menu. Scroll right to access the compressor gain trim, distortion gain trim, and A/D calibration programs. The procedures for these setup routines are detailed below. Further scrolling will show the EQ test, speaker simulator test, compression test, distortion test, noise gate test, HISC test, RAM test, and display tests. When done, return to the main utility menu.

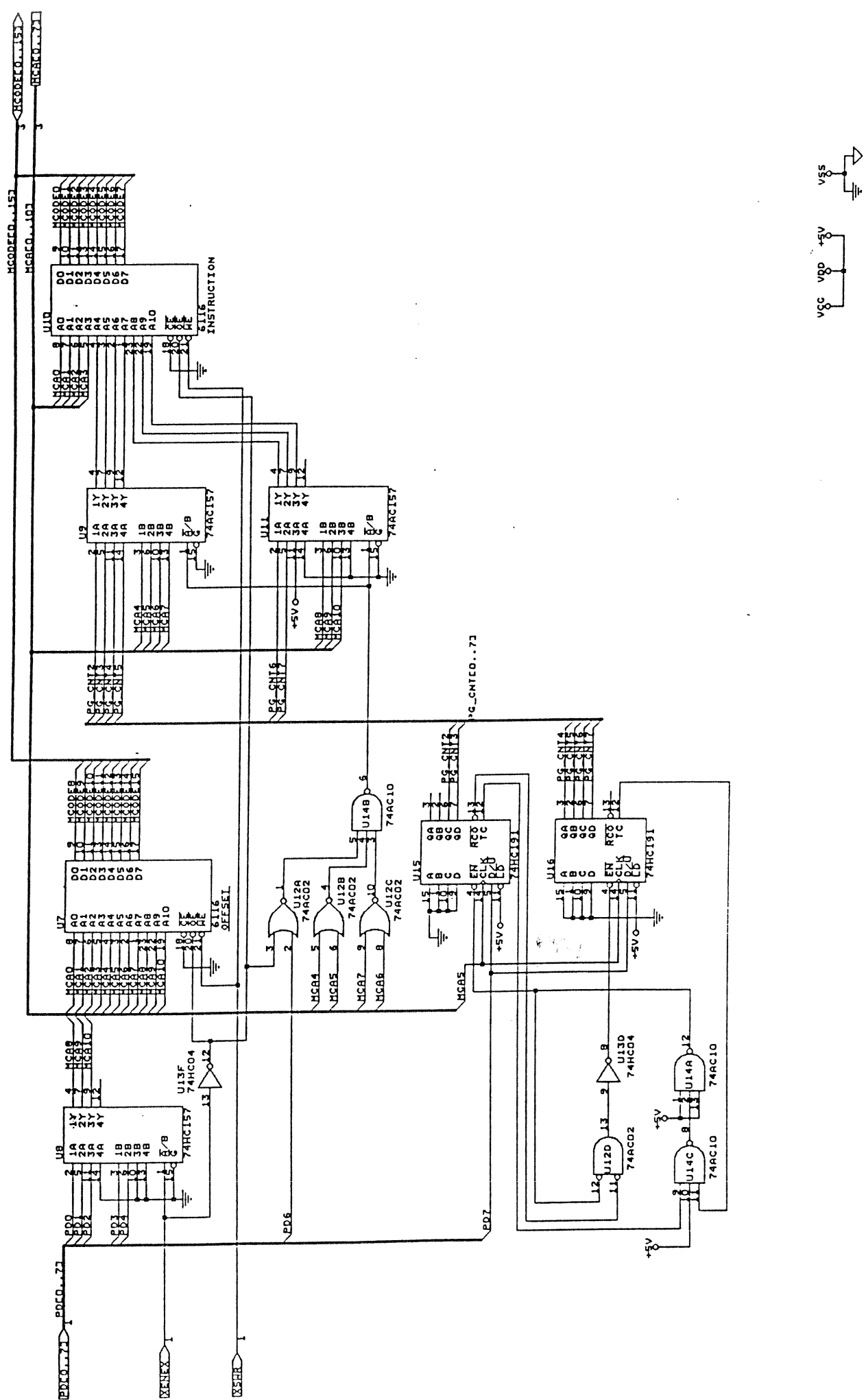
1. Compressor gain trim: With a 1 Vp-p, 1 KHz sine wave measured at test point one (TP1) on the main PCB, adjust P6 (50K trimpot) until the signal measured at TP4 is the same amplitude as the signal at TP1.
2. Distortion gain trim: Adjust P7 (50k trimpot) until the voltage measured at pin 7 of U97 is between -3mV DC and +3mV DC.
3. A/D Calibration
 - a) Gain: With a 14 Vp-p, 1KHz sine wave measured at TP2, adjust P2 (10K trimpot) until the signal measured at TP3 is 14 Vp-p.
 - b) Bias: Reduce the signal level 50 dB to 44.3 mVp-p and adjust P3 (50K trimpot) until the signal seen at TP3 is just barely all positive going or all negative going.



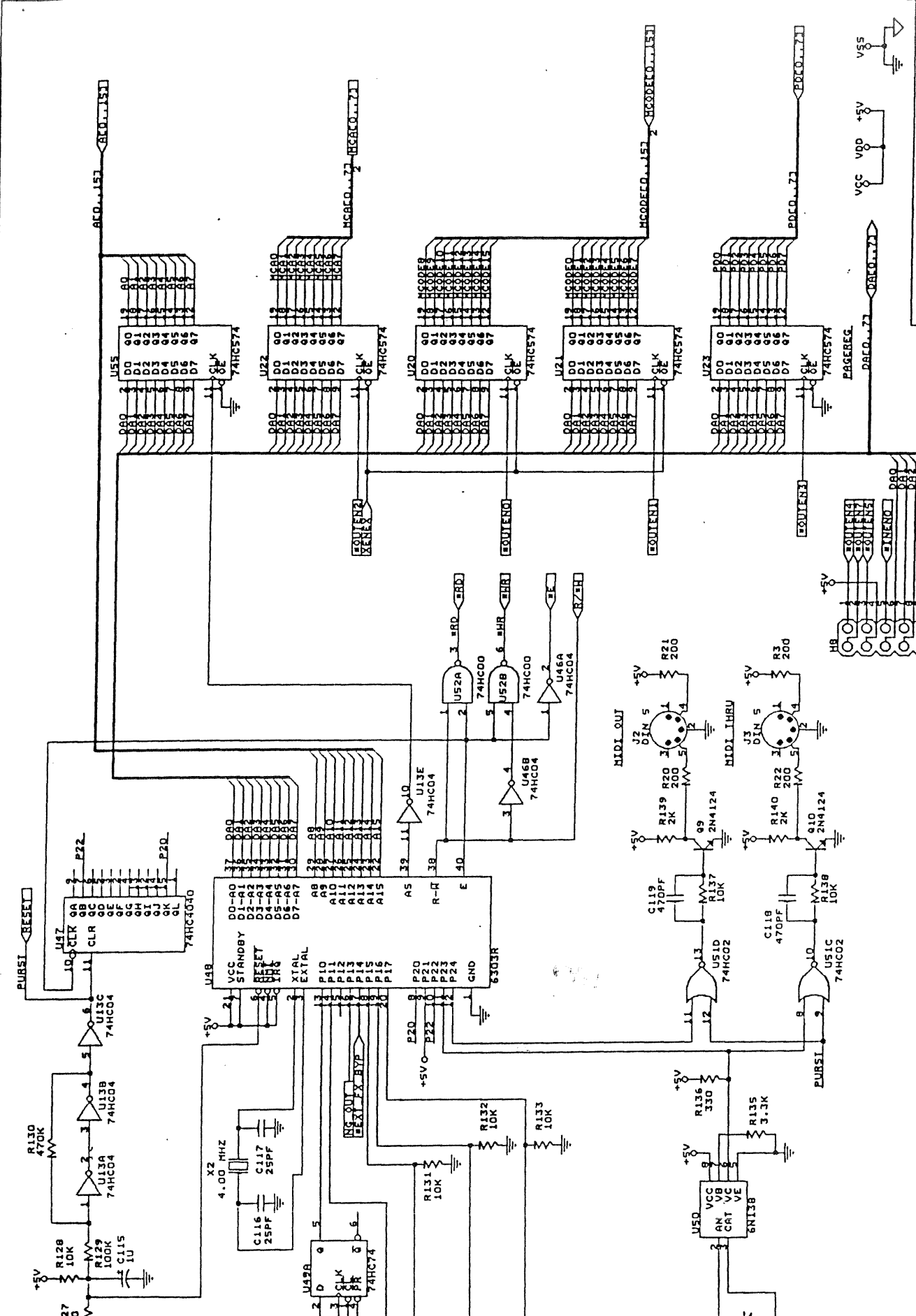
IRP1MA801.SCH
 IRP1MA802.SCH
 IRP1MA803.SCH
 IRP1MA804.SCH
 IRP1MA805.SCH
 IRP1MA806.SCH
 IRP1MA807.SCH
 IRP1MA808.SCH
 IRP1MA809.SCH
 IRP1MA780.SCH



000 Electronics Inc.
 5639 So. Riley Lane
 Salt Lake City, Utah 84107
 Title RP-L MAIN BOARD (HISC SECTION)
 Size Document Number REV

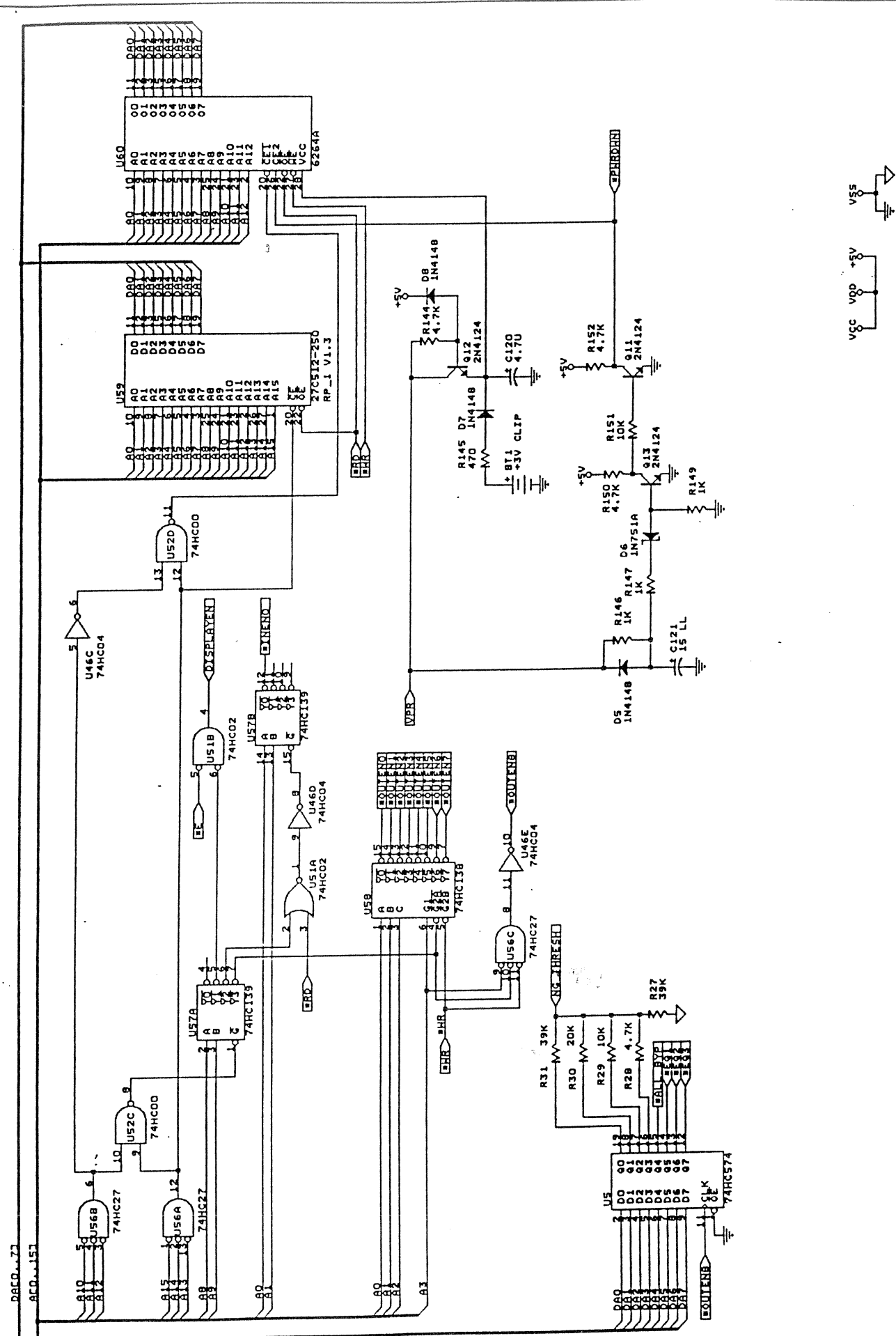


Digitech
 5639 So. Allev Lane
 Salt Lake City, Utah 84107
 Title
 AP-1 MAIN BOARD (UPDATE AND INST. REG)
 Size
 B
 Document Number
 RPAH802.SCH
 Rev
 AB
 Date
 May 19, 1992 15:01 2 of 10

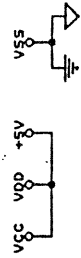


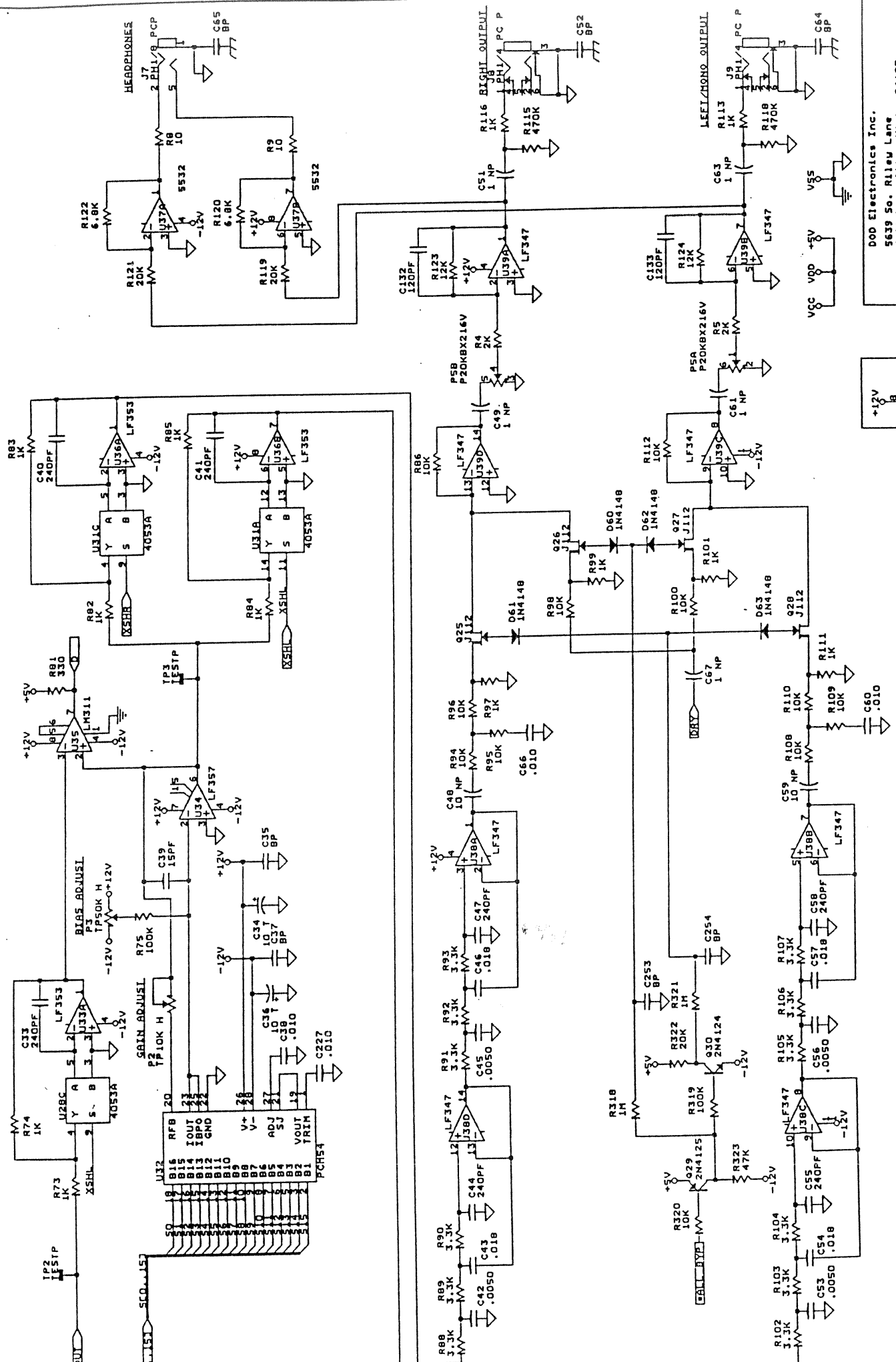
Digitech
 5639 So. Riley Lane
 2811 Lake City, Utah 84107
 Title RP-1 MAIN BOARD (PROCESSOR, MIDI)
 Size Document Number RP1MAB03.SCH
 8
 Rev 1.1 12/27/82 HCN

HCN_15
 3 of 3



D1eitech
 8639 So. Riley Lane
 Salt Lake City, Utah 84107
 Title RP-1 MAIN BOARD (EPROM, SRAM, DECODE)
 Size Document Number RP1M804.SCH
 Rev B
 Date May 81 1992 Sheet 4 of 10



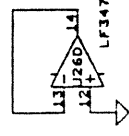
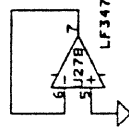
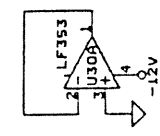
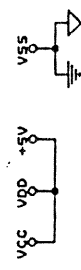
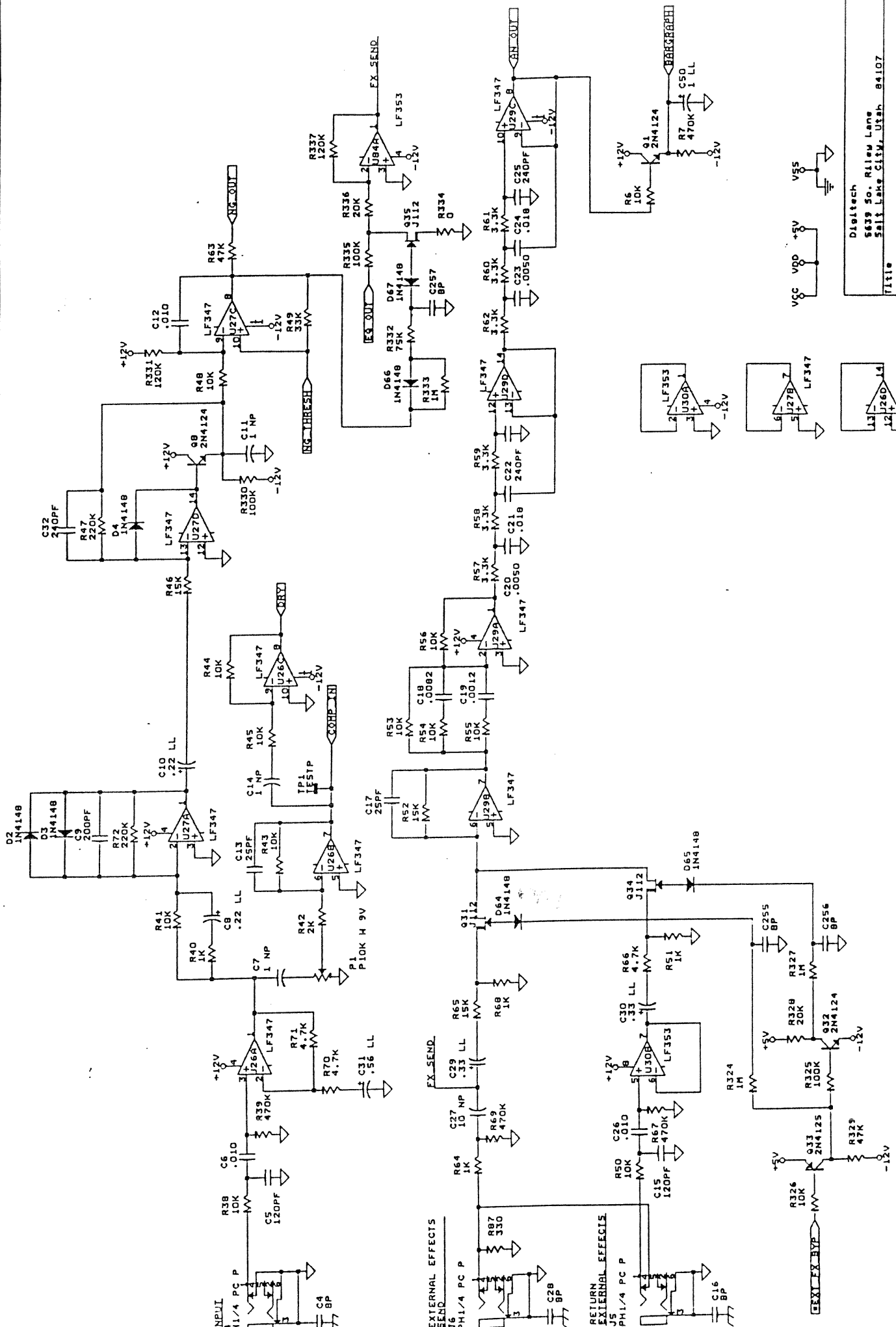


DOD Electronics Inc.
5639 So. Riley Lane
Salt Lake City, Utah 84107

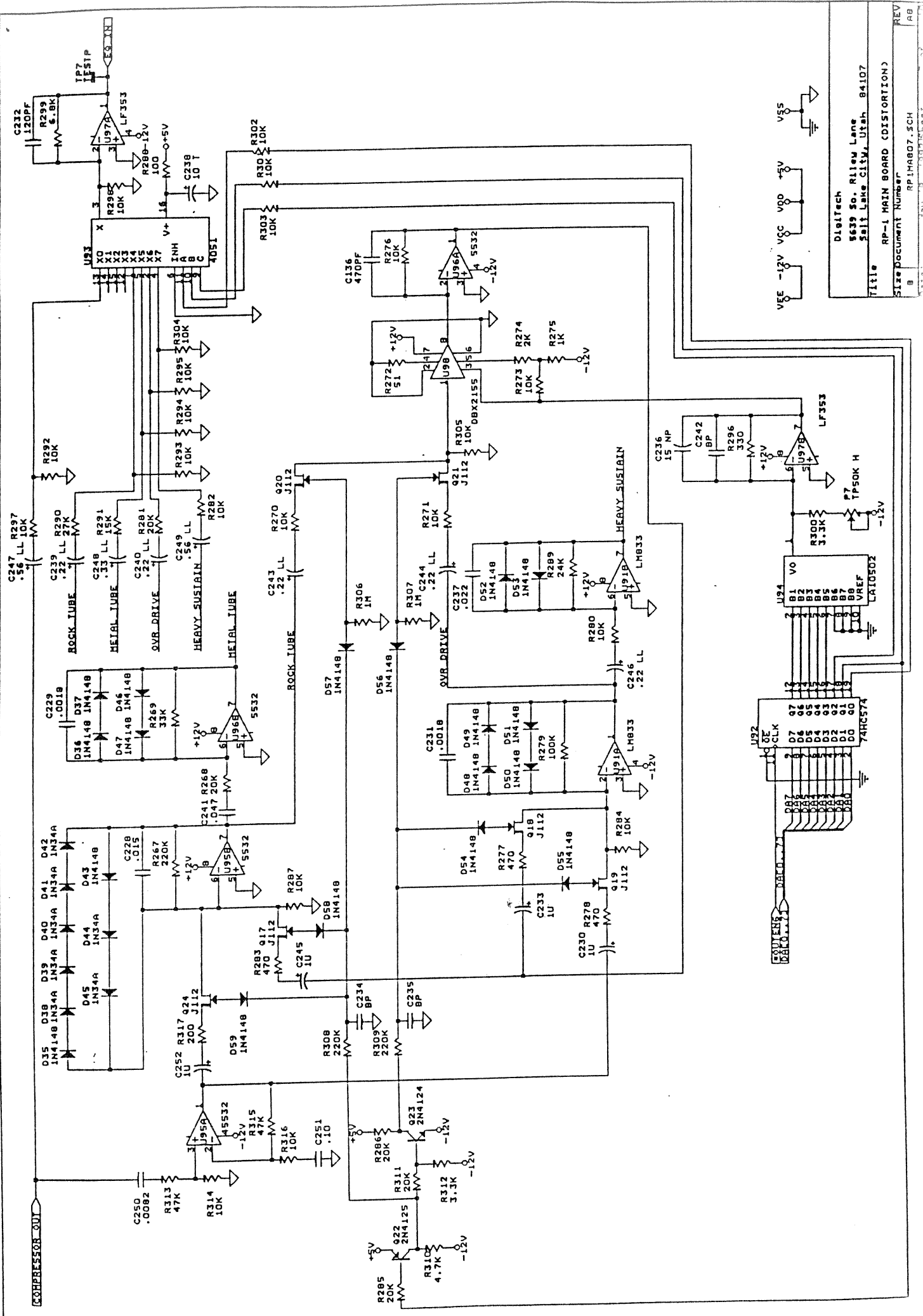
Title RP-1 MAIN BOARD (A/D/A, OUTPUT)

Size Document Number RP 1MAG05.5CH

REV B

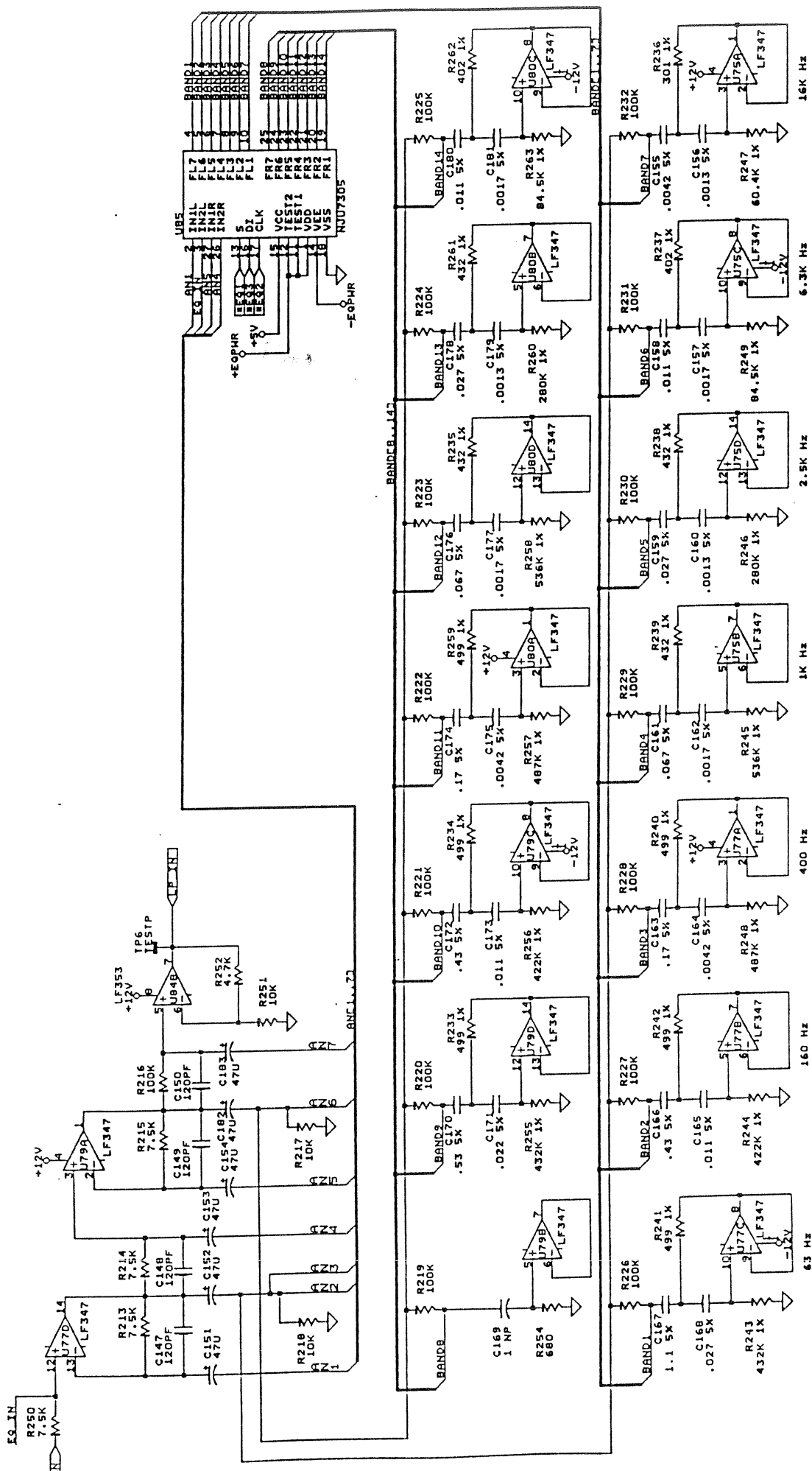


Disltech
 5839 So. Rilew Lane
 Salt Lake City, Utah 84107
 Title
 AP-1 MAIN BOARD INPUT, GATE, FX LOOP
 Size Document Number
 8
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 REV
 A8

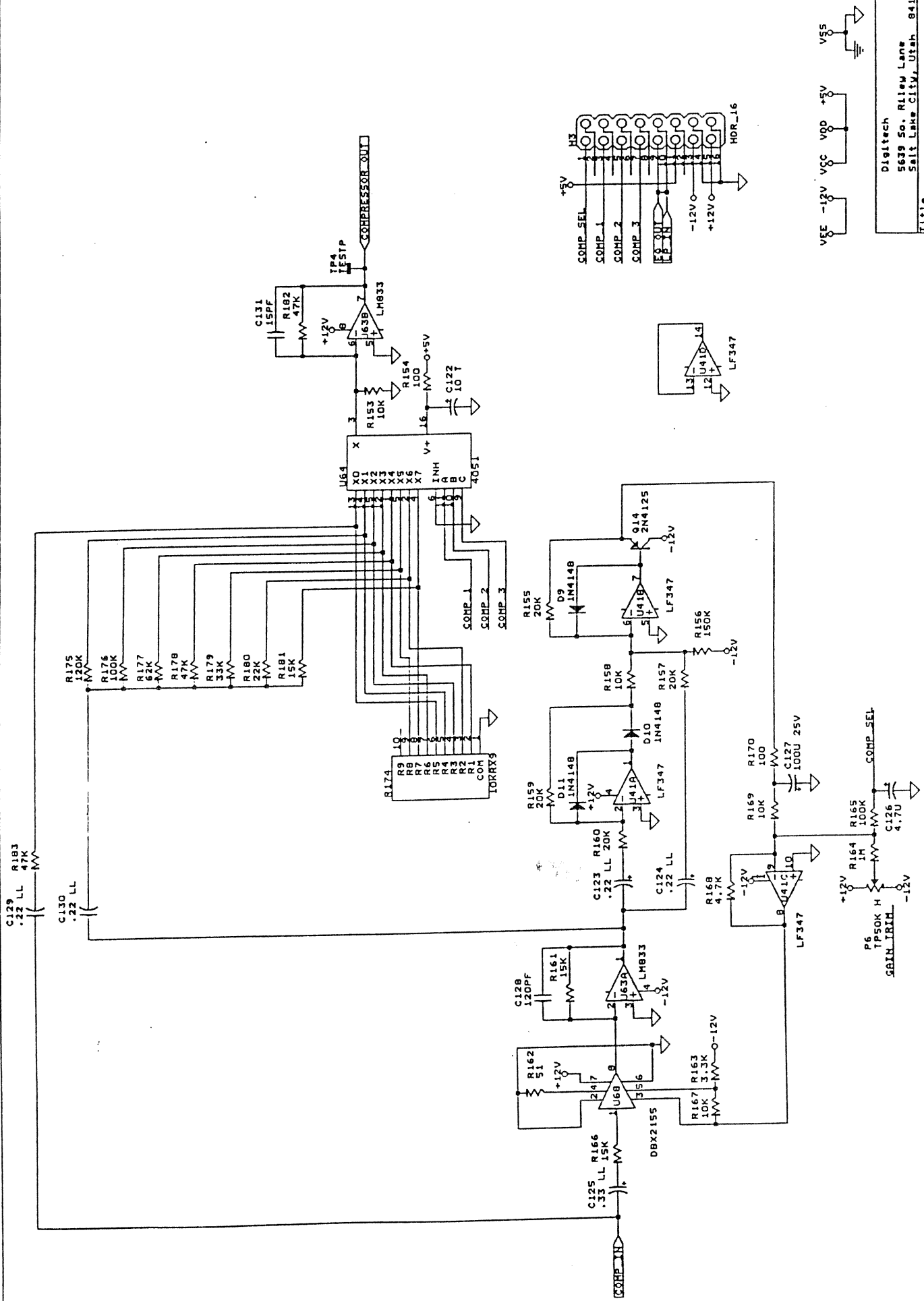


Title
 RP-1 MAIN BOARD (DISTORTION)
 Size Document Number
 RPIHAB07.SCH
 REV
 AB

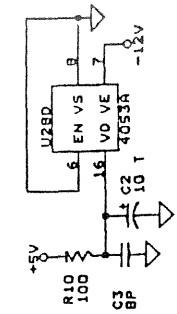
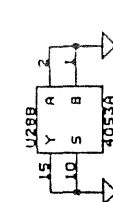
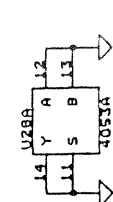
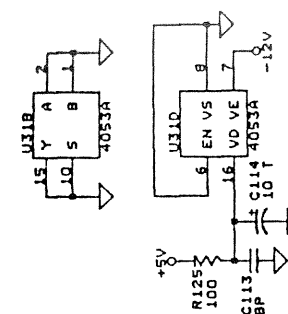
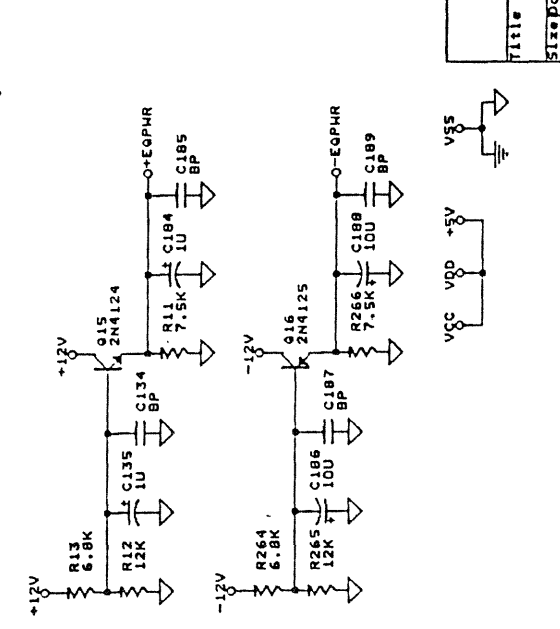
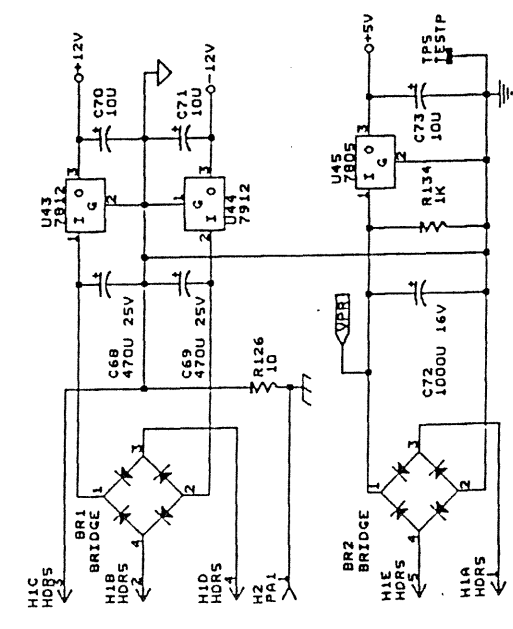
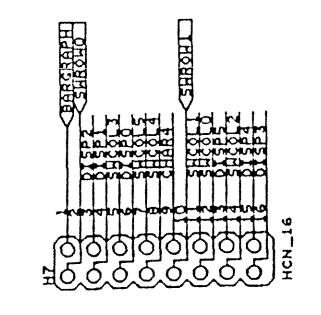
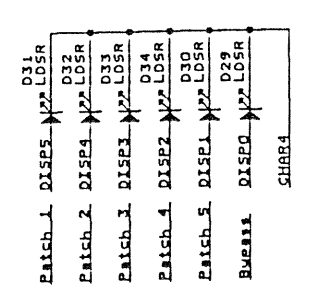
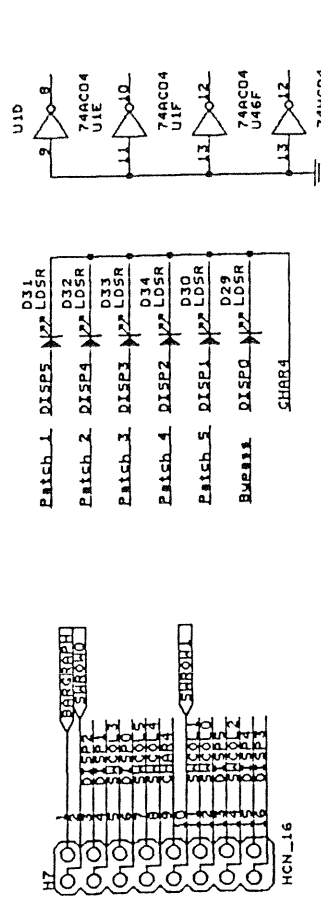
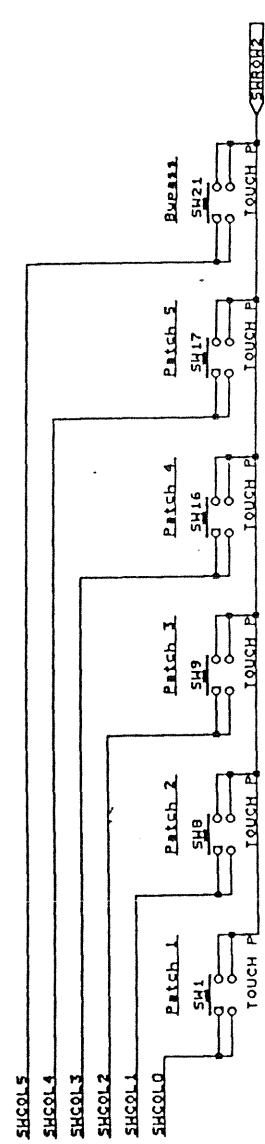
DigiTech
 5639 So. Rillee Lane
 Salt Lake City, Utah 84107



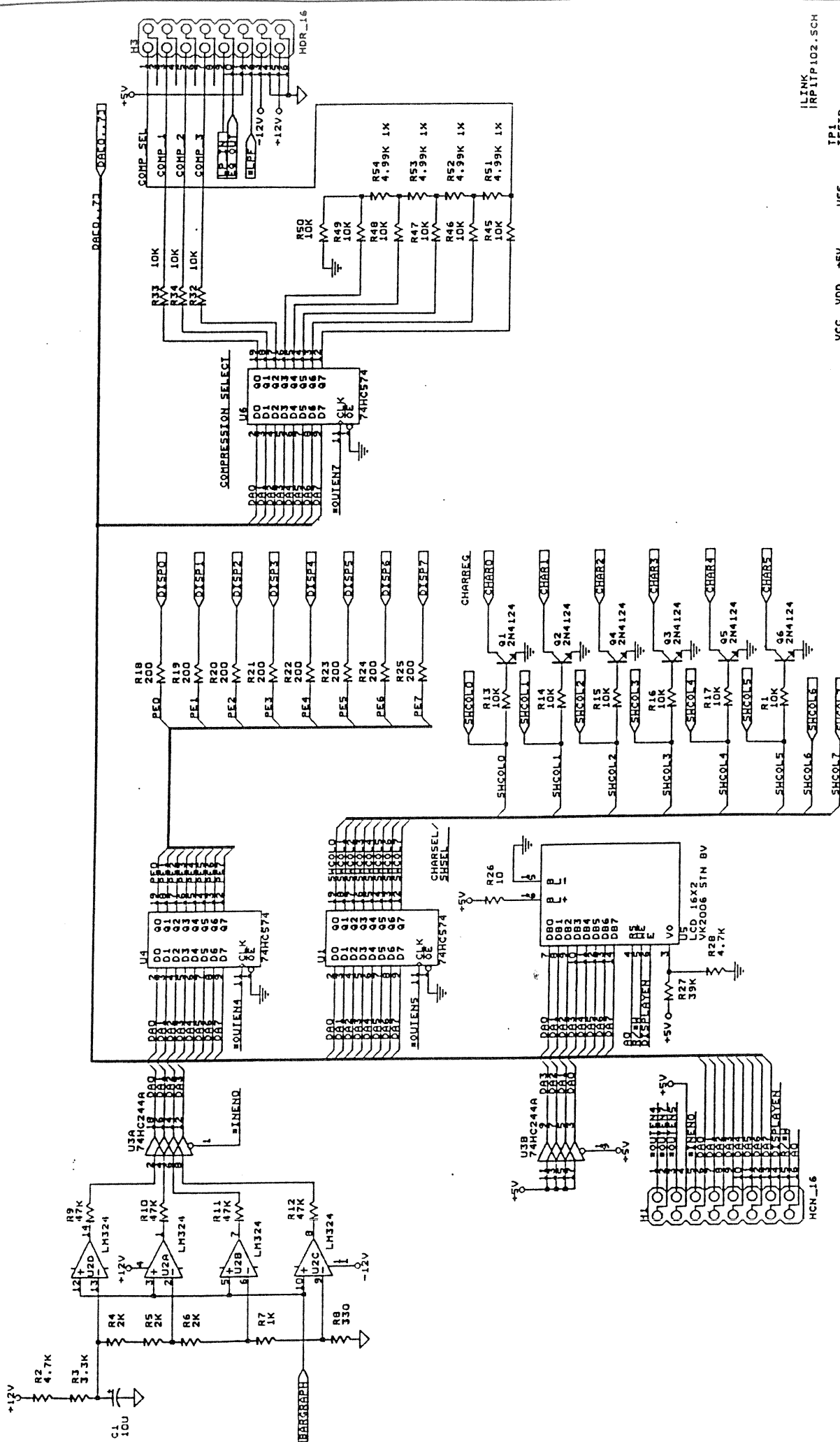
DOD Electronics, Inc.
 5639 So. Rliev Lane
 Salt Lake City, Utah 84107
 Title: RP-1 MAIN BOARD (GRAPHIC EQ)
 Size: Document Number: AP-1M808.SCH
 Rev: A8
 Date: May 18, 1992 Sheet 8 of 10



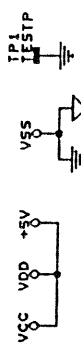
Digitech
 5639 So. Riley Lane
 Salt Lake City, Utah 84107
 Title RP-1 MAIN BOARD (COMPRESSOR)
 Size Document Number RP1M8091.SCH
 B REV AB



- NOT USED
- C137-156
 - C192-201
 - C203-210
 - D12-28
 - H4-5
 - J1-7
 - K1-7
 - R14-17, 23-26
 - R76-80
 - R114, 117
 - R141-143, 171-173
 - T77
 - U34, 212, 253
 - Y6
 - Z1
- LAST REF.
- BR2
 - BR1
 - C257
 - D67
 - H8
 - J10
 - K10
 - Q35
 - R337
 - SM21
 - TP1
 - Y9
 - X1

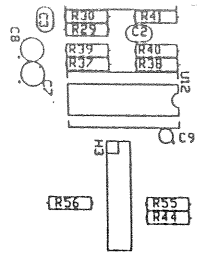


ILINK
IRPLTP102.SCH

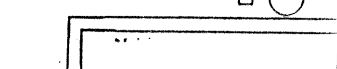
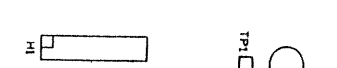
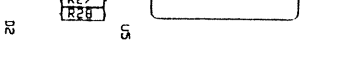
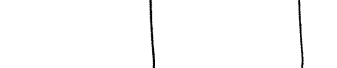
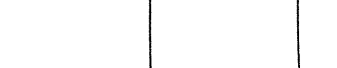
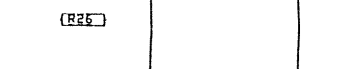
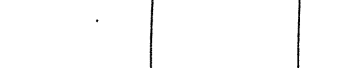
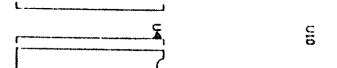
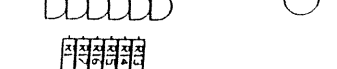
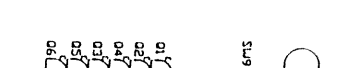
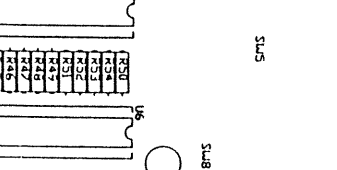
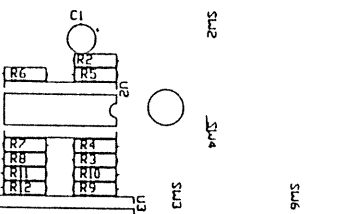


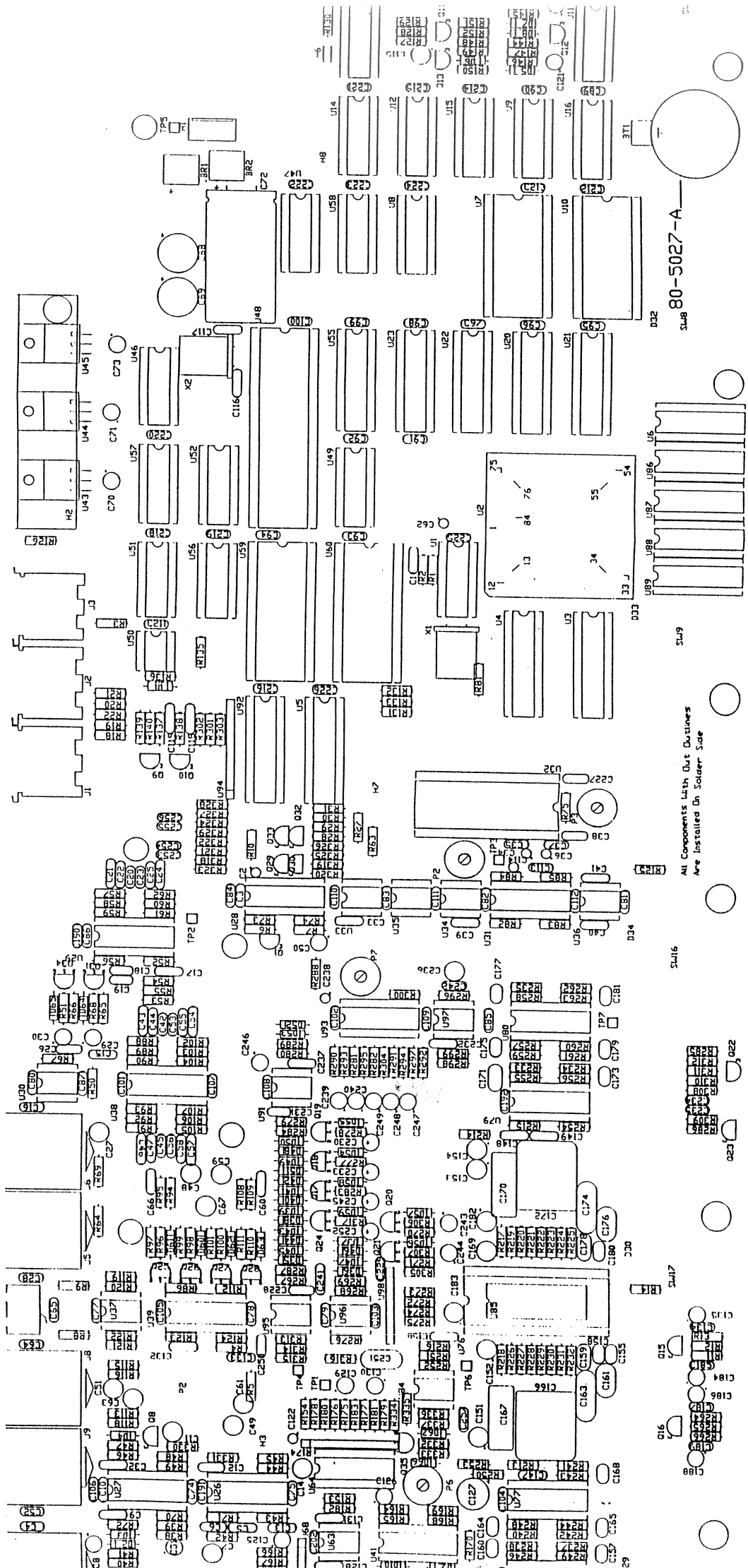
Dialtech
3639 So. Riley Lane
Salt Lake City, Utah 84107
Title RP-1 TOP BOARD (LCD, HEADROOM)
Size Document Number B
RPLTAC001.SCH
REV 10

All Components with Out Outlines
Get Installed On Solder Side



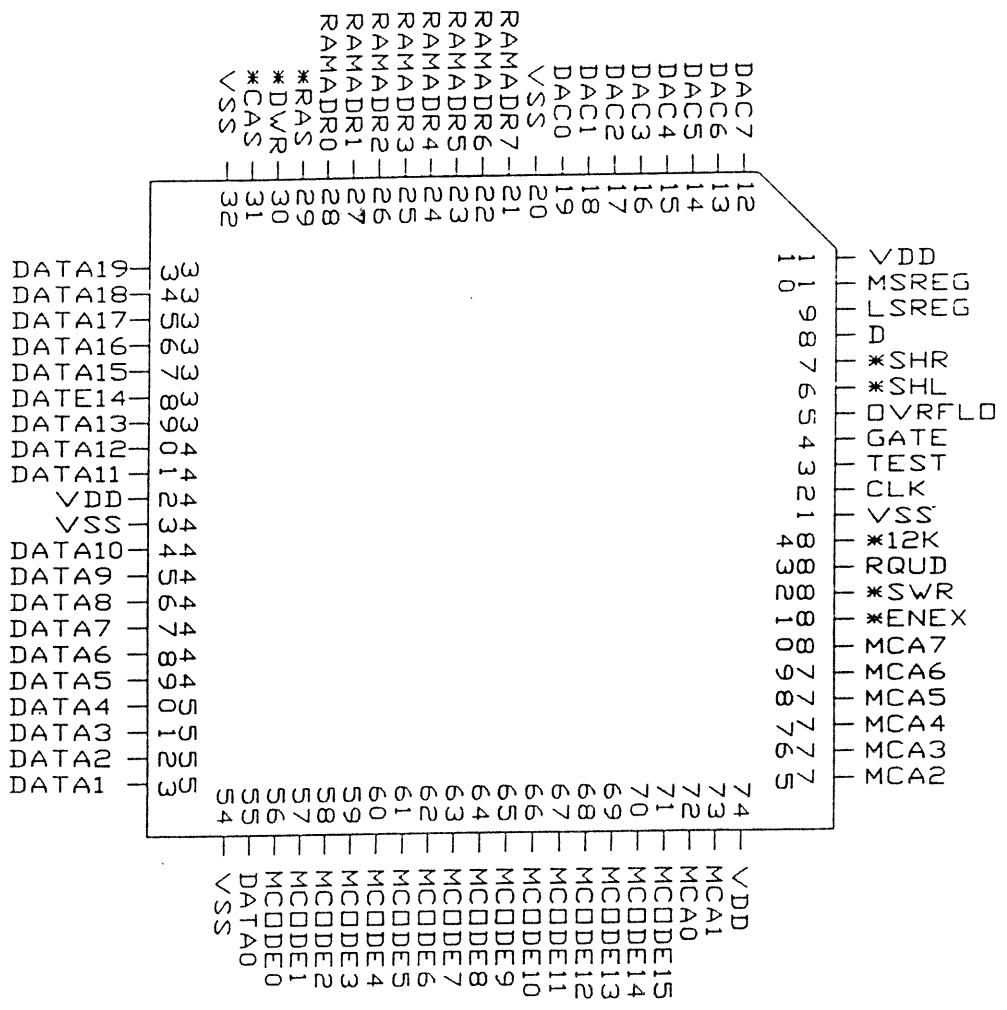
S413





80-5027-A
Sub

All Components With Out Outlines
Are Installed On Solder Side



FUNCTIONAL PIN DESCRIPTION FOR HISC

<u>Description</u>	<u>Pin</u>
VSS: ground (GND)	1,20,32,43,54
CLK: oscillator input	2
TEST: in-house test only (GND)	3
GATE: in-house test only (GND)	4
OVRFLO: indicates internal math overflow	5
SHL: sample/hold left	6
SHR: sample/hold right	7
D: DAC compare input	8
LSREG: clocks lower byte DAC output	9
MSREG: clocks upper byte DAC output	10
VDD: +5V power	11,42,74
DAC7..DAC0: DAC output data	12,13,14,15,16,17 18,19
RAMADR7..RAMADR0: DRAM address output	21,22,23,24,25,26 27,28
RAS: DRAM row address strobe	29
DWR: DRAM write	30
CAS: DRAM column address strobe	31
DATA19..DATA0: DRAM data	33,34,35,36,37,38, 39,40,41,44,45,46, 47,48,49,50,51,52, 53,55
MCODE0..MCODE15: microcode data	56,57,58,59,60,61, 62,63,64,65,66,67, 68,69,70,71
MCA0..MCA7: microcode address	72,73,75,76,77,78, 79,80
ENEX: enable external microcode write	81
SWR: external microcode write line	82
RQUD: request for microcode update	83
I2K: in-house test only (+5V)	84