SYNTHI-AKS

Circuit Diagrams

and Layouts

from

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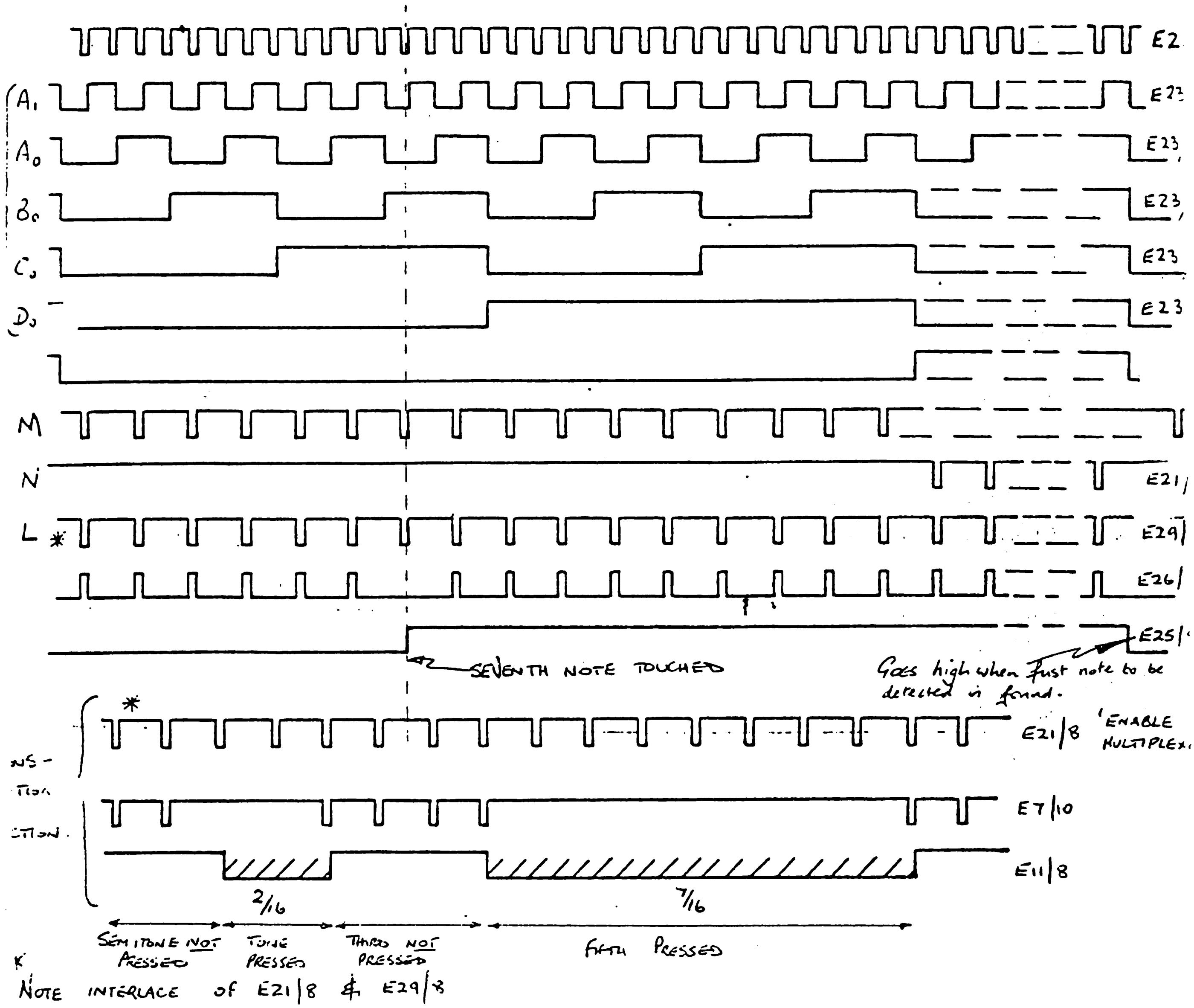
I N D E X

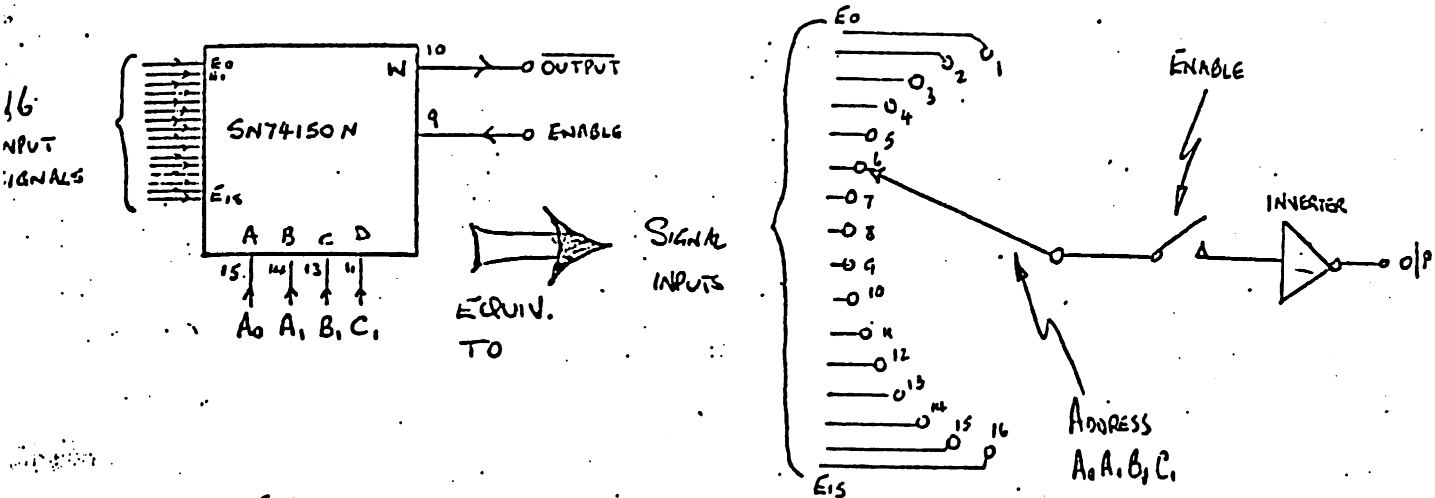
The pulses generated are used to compile various gating signals.

The signal is divided by 2 by E22 (8,9,11,12) and again by 2 by E22 (2,3,5,6), and then by 16 by E23. By gating these signals together, a set of waveforms shown below is produced.



SIGNALS A1, AO, BO, CO provide a four bit address code to the three data multiplexers. The top two multiplexers, E15, E27 are connected to the keyboard, and as only 30 notes are provided, then two inputs (E27 pins 7,8) are left permanently unconnected. The lower multiplexer is the "transposition pad" unit.

MULTIPLEXERS - an electronic 16 way switch; single pole.



The 16 inputs; E0 to E15, can be considered as the 16 inputs to a rotary switch. The switch position (only one pole) is determined by the address code, ie A0, A1, B1, C1, labelled ABCD on the actual device.

	Switch Position	(A A0	B A1	C B1	D) C1
E0	1	0	0	0	0
E1	2	1	0	0	0
E2	3	0	1	0	0
E3	4	1	1	0	0
E4	5	0	0	1	0
E5	6	1	0	1	0
E6	7	0	1	1	0
E7	8	1	1	1	0
E8	9	0	0	0	1
E9	10	1	0	0	1
E10	11	0	1	0	1
E11	12	1	1	0	1
E12	13	0	0	1	1
E13	14	1	0	1	1
E14	15	0	1	1	1
E15	16	1	1	1	1

Where 0 = low voltage) logic levels
1 = high voltage)

This is known as a <u>truth table.</u>

Thus, for an address

D C B A
1 0 1 1   sorry about the reversed code

The switch is at position 12

A B C D
1 1 0 1 ⇒ 12

'A' is known as the least significant bit - LSB

'D' is known as the most significant bit - MSB

<u>The ENABLE SIGNAL</u> acts as a switch; that is when this signal is high (1) the switch is <u>open</u> circuit, and the output (w) is permanently high. When this signal is low (o) the switch is closed and so anyone of the 16 data inputs may be selected. The ENABLE IS SOMETIMES called the <u>STROBE.</u>

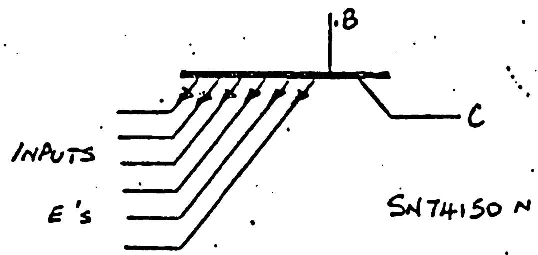
Note that the output shows the inverted data. Thus to summarise. With a high (1) at data input 12, and address code of

A	B	C	D
1	1	0	1

and an enable signal of logic 0, the output is (1) inverted, namely 0.

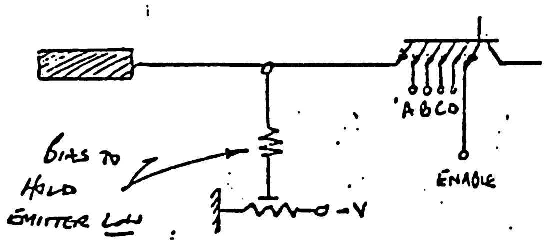
TOUCH SENSITIVITY.

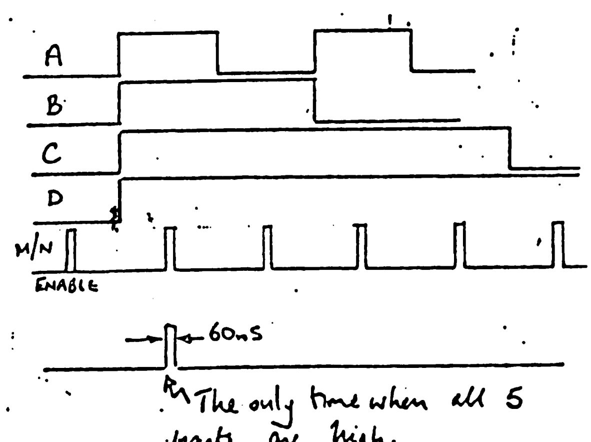
The input to a TTL gate looks like:-



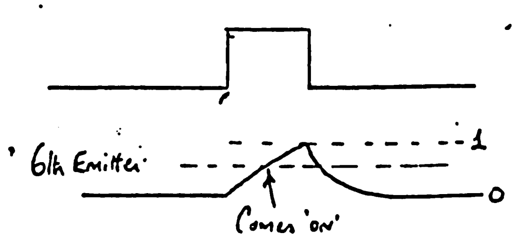
This is a multiple emitter, transistor, i.e. a transistor with, in this case, 6 emitters.

In the multiplexer, 4 of them are connected to the address code, one to the enable signal and the last to the touch plate.

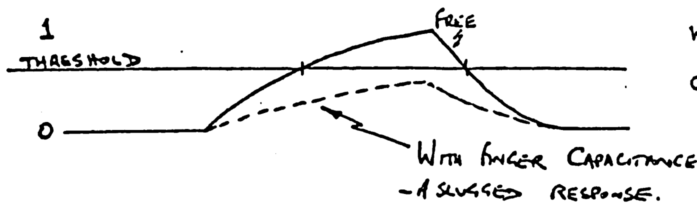




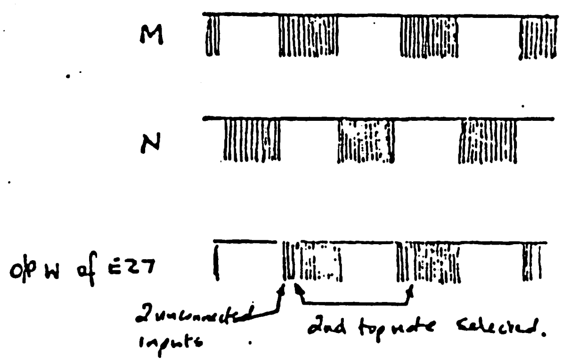
For each specific input there will only be one point in the Address cycle (32 bits) when all 5 emitters are high at the same time. When the bias is correctly aligned, the circuit will behave as follows:-



looking at the last trace we see that sixth emitter, which is connected to the touch plate, is dragged up, due to the associated capacitance of itself WRT its sister emitters. Infact, it is dragged up so far that it changes state from a '0' to a '1'. BUT when a finger is placed on the associated touch plate, the capacitance of the finger increases the total capacitance as seen by the emitter, increasing it by as much as 10 to 100 pF, and this is sufficient to prevent it from changing state. Thus, pressing the pad with a finger will prevent the data multiplexer output from changing state.



The enable signals 'M' and 'N' are

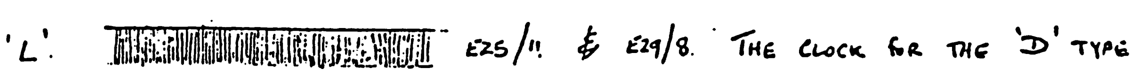


Thus one multiplexer is addressed, and then the other (i.e. E15 and 27) is then the other etc.

If more than one note is pressed, then several gaps in the outputs will be generated; however; the electronics that follow select the first note to appear, and as the keyboard is swept (addressed) from top to bottom, then the highest note of all the notes pressed is selected.

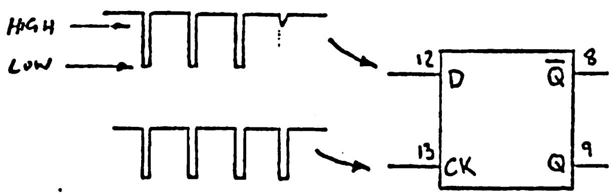
This piece of electronics is E26 (11,12,13) (4,5,6)
E25 (8,9,10,11,12,13), E16, E17, E18.

The two data outputs of MULTIPLEXERS E15, E17 are OR'ED together by E26 (11,12,13) (that is they are effectively just added together).

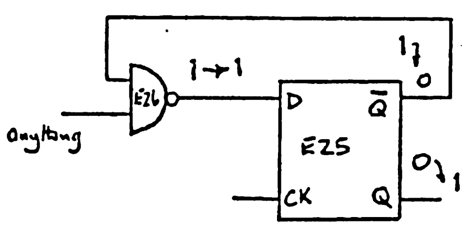


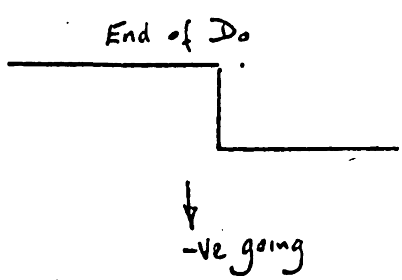
*WHEN looking for these waveforms, you much SYNC OFF of DO E23/11.

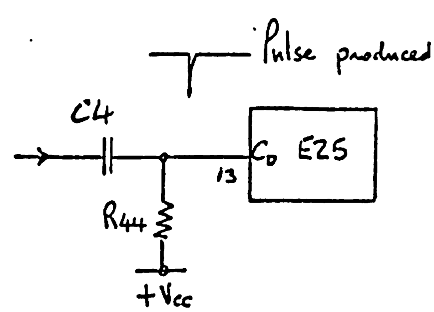
Now consider the 'D' type E 25 (8,9,10,11,12,13).
Assume that pin 8 is at logic 1. Therefore, Pin 5 E26 is at logic 1, and it is thus "enabled" in that is allows signals at its other pin (pin 4) to pass through it. The signal at pin 4 is the summed data output, which when it passes through the gate, is inverted. Notice that the clock pulses are coherent with the data signal.



The D type operates as follows. It is an edge triggered device; that is data at its' D input is transferred to the Q output on the +ve transition of the clock. That is, put a 1 on pin 12, clock the device and a 1 appears at pin 9, the Q output. SO, in the present example, when there are no notes pressed, the data is low when it is clocked, and so Q remains Low. But, when that data is high, then Q goes high, therefore Q (pin 8) goes low and in doing so inhibits E26 (4,5,6) the output of which thus remains high. The circuit has latched up, and it will remain latched up until it is released by a clearing pulse. Thuse, E25, Q9 goes high and remains there when it detects the f first note. (See page 2, waveforms). Now, E25, Q9 clocks the D types E16,17,18, which are fed with the address code (A , A_0, B_0, D_0,). So, as soon as the first note is detected, its address is clocked into E16,17,18 which act as a one bit memory. At the end of one address sweep (about 100µ sec.) the D type E25 is unlatched by a negative going pulse produced by differentiating the address bit D_0 (23 pin 11) with the CR network C4, R44.

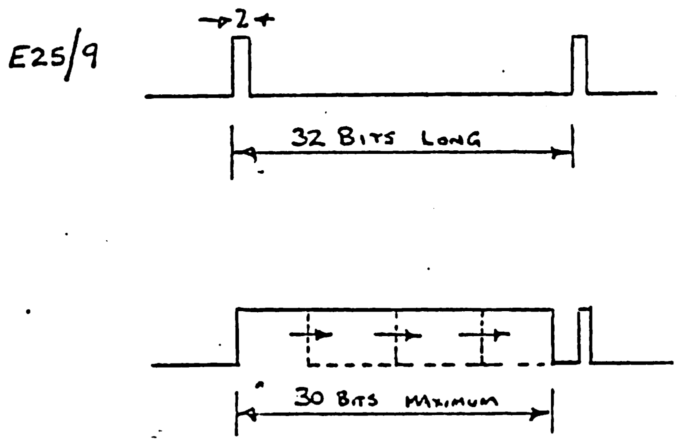






A LOW ON THE CLEAR INPUT OF A D TYPE CLEARS THE Q OUTPUT TO LOGIC 0

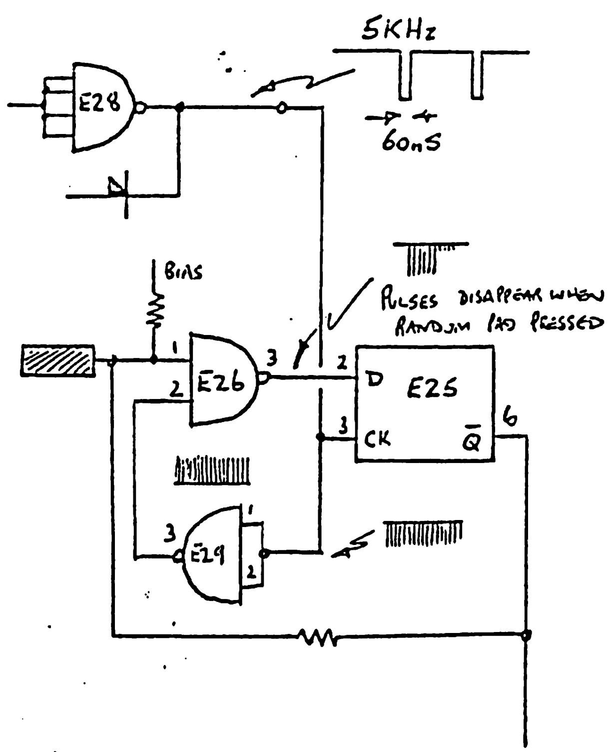
Thus, the D types E16, 17, 18 form a short term memory that is continually being updated (every 100 μsec) as to highest key that is being selected. The output Pin 9 E25 is an <u>excellent</u> place to test the keyboard to see if the multipexer for the KB and/or the address code is functioning.



2ND BOTTOM NOTE PRESSED.

AS YOU SWEEP YOUR FINGER UP THE KEYBOARD THE WAVEFORM CHANGES AS SHOWN. (THE PULSE WIDTH ELONGATES)

<u>RANDOM FUNCTION</u> This is the same touch sensitive detector as for the KEYBOARD. However, as there is only one input, then no addressing is required. A slow clock pulse generator is used, (5KHz, 60n sec. pulses).



A separate oscillator, rather than the address oscillator is used, because:-

1. A long enough gap must be provided to allow the floating gate time to discharge.

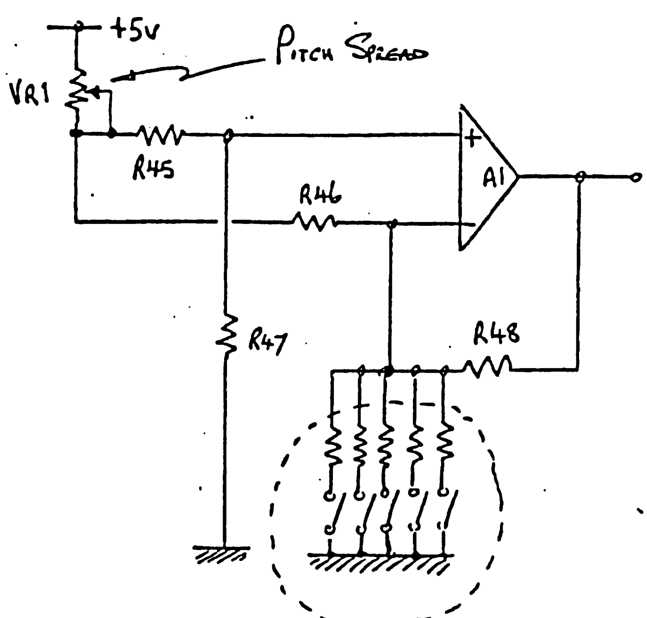
2. If the address clock were to be used, the Random would not be random; this is because the network has a tendancy to select the largest clock pulse and this means that particular notes occur more readily than others.

The operation is as follows. When a missing pulse is detected by E25 pin 2, the $\overline{Q}$ output goes low and so the cct folds over. The $\overline{Q}$ is connected to the set input of E25. This will cause the Q output to go high and in doing so it ' records ' an address. (Any address in fact; it depends upon when the Random is pressed) . When the random is released, the set input of E25 pin 10 returns to 1, and the circuit operates as before. As the Q output E25 pin 6 can go low at anypoint in time, then any note is selected, and hence the term ' random '.
N.B. The random function can generate errors; this is a design error.

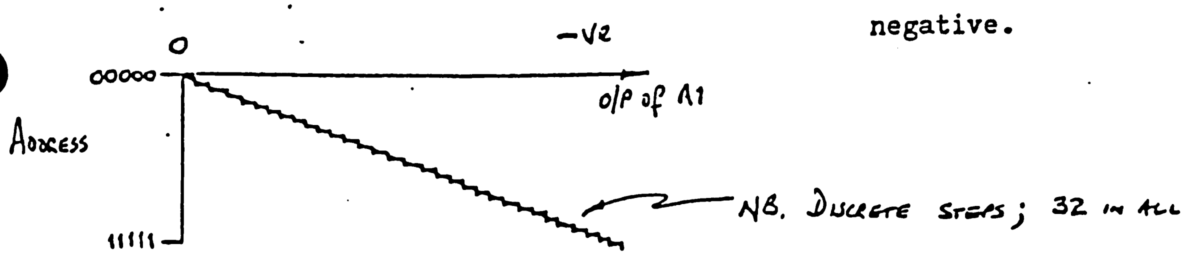
The errors can be generated by the random accidentally selecting address code Binary 11111 (i.e. 32). This is the ' Skip ' code, and it will cause the meter to prematurely reset, and the memory to corrupt. To demonstrate this phenonemum, try this test; Set the Sequencer clock speed to about 3 to 4 on the knob, press record and then tap the random pad. There is a 32:1 chance of generating the skip code, and this will be detected by a premature reset of the meter.

DAC

The short term memory E16,17,18 feeds Q1 to 5 which form a DAC. (Digital to Analogue Converter) Slightly re-drawing the circuit, we the following;



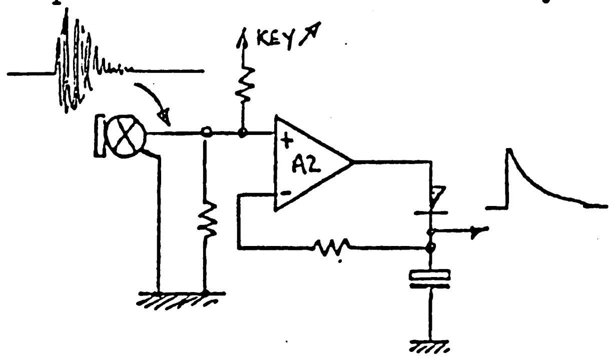
Inside the dotted box are 5 resistors and 5 switches. The resistors are R49 to R54, 1% m.o. resistors. The switches are Q1 to 5 and these are controlled by th stored address in E16, 17, 18.
When the address is 00000, all the switches are off, and so the circuit is just a simple differential amplifier, and the voltage at the output of A1 is OV. When the switches turn ' ON ', the output goes negative.



* NOTE WRT the short term memory E16,17,18. The lower half of E18 is different to the other 5 sections. This is the "key-pressed" section. It uses the clock line as its data input. This is because, when Q9, E25 is high, then a key is being pressed, and this is the data that it requires. It is clocked by $\overline{Do}$ (known as $\overline{F}$@8, E26) at the end of an address sweep, and so its Q output (i.e. 9, E18) is high when a key is pressed and low when no key is pressed.

Note that the negative (1-0) transition of the $\overline{Q}$ output (8, E18) is used to control the <u>envelope trigger</u> by turning transistor Q6 on when a key is pressed. The envelope trigger control pot is used to determine whether the trigger is generated from the real time or recorded output.

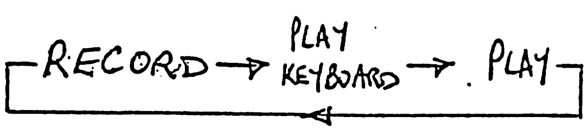
<u>DYNAMIC RESPONSE</u> The crystal gives the K.B. a dynamic function, but this is only employable in real time. That is, <u>no</u> information about the key pressure is recorded. The crystal produces a click when the K.B. is hit.

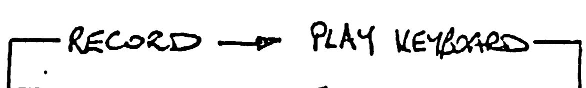


The network is a voltage follower with a diode in the feedback loop. The junction between the diode and the capacitor tries to follow the +ve voltage transient of the input and decays slowly (due to the storage of the capacitor) after the signal has ceased. This voltage is used to control one of the output channels on a Synthi A.

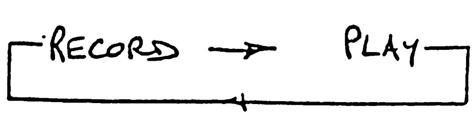
<u>RECORD, PLAY, CONTROL LOGIC</u> * note RECORD AND PLAY are clocked from the random clock gen.

The RECORD and PLAY pads operate in the same way as the Random touch pad. However, the interconnection of E10 (1,2,3,4,5) with E10 (8,9,11,12,13) and E10 with E18, provide a sequential mode of operation. That is:-





these two sequences are permissible.



NOTHING HAPPENS

RECORD → KEYBOARD → PLAY ◯ REMOVE FINGER - ALLOWS SEQUENCE TO PLAY. PRESSING 'PLAY' MERELY STOPS SEQUENCE.

		RECORD	TOUCH K.B.	PLAY
E10	Q6	0	1	0 - 1
	Q8	1	1	0 - 1
		1	2	3 3a

REVERTS BACK TO A 1 WHEN FINGER IS RELEASED

ASSUME E18/8 IS HIGH
E10/6 IS HIGH
E10/8 IS HIGH

1. The record pad is pressed. The data presented at the D input (2, E10) is high during the clock. Therefore Q goes high, $\overline{Q}$ goes low. This sets E10 (* a low on its set input) and so the D type is latched up, and it will remain there until it is cleared. The $\overline{Q}$ pin 6 is also connected to the clear of the lower E10 D type, but this has no effect as the D type is already in its cleared mode.

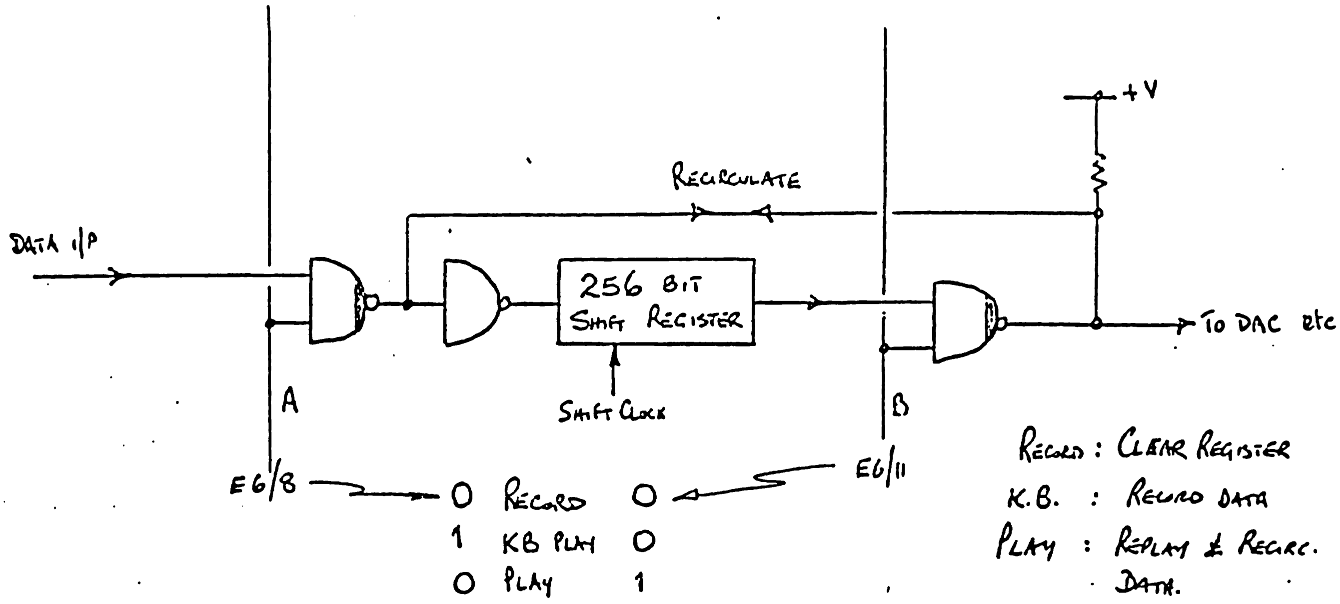
2. When the keyboard is pressed the KEY voltage (i.e. E18, 8) goes low, and this clears E10 (2,3,4,5,6). (The clear overides the set control). The $\overline{Q}$ output (E10, 6) then goes high, whereas the lower D type still remains unchanged.

3. Play is pressed. A logic high is presented to the D input (12, E10) and so the $\overline{Q}$ goes low. However as there is no...

3a. latch up it returns to its high level as soon as the finger is released. Note, that when at the record mode, the clear input (13, E10) is low and so the lower half of E10 is prevented from changing state; that is, Record Play does nothing.

Control Logic This is E6. The logic sequence (Above) is presented to E6. The output sequence generated by E6 is as follows:-

	PIN	RECORD	KEYBOARD	PLAY	
E6	8	0	1	0	no jump as above.
	11	0	0	1	



Lines A and B open and close the sets of input/output gates. Only one set of gates (A or B) is ever open. When the logic level on A is high, gates connected to it are open. When the logic level on A is low, gates connected to it are closed.

RECORD MODE: BOTH SETS OF GATES ARE CLOSED. CLOCK TO SHIFT REGISTERS IS VERY FAST, LATTER FILLS WITH 0'S

KEYB'D Mode. This is "record" mode (confused?); data is accepted, because A is high. The data is clocked into the shift register at a slower rate, this rate being variable. If you are unlucky, you can overfill the shift register, and the front of the data is merely lost out of the end of the device.

Play. Data is replayed and recirculated, because line B is high. The replay clock rate is also variable. When an unfilled part of the shift register is detected a skip mode is implemented and the shift register skips all the blank locations until it finds the start of the data, which it then plays at its slow rate. Pressing the play pad stops the shift clock from operating in its "play" mode and so pressing play whilst the machine is replaying does two things:-

1. Effectively pauses the device
2. Upon releasing finger, the sequence restarts (proceeded by a skip block).

If the shift register has been overfilled, then there are no blank locations and so when the play is pressed, the machine rapidly searches for an empty location and cannot find one. The result is a buzz sound as all the data rapidly recirculates. Also, as there are no blank locations, the machine does not know where the sequence start is. Therefore overfilled sequences, when replayed will start anywhere.

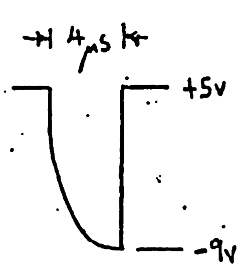
The memory is a 6 bit word, 256 bits long. 5 bits are used to record the note selected. The sixth is used to trigger the envelope trigger; that is if.the envelope trigger pot is in the right position.

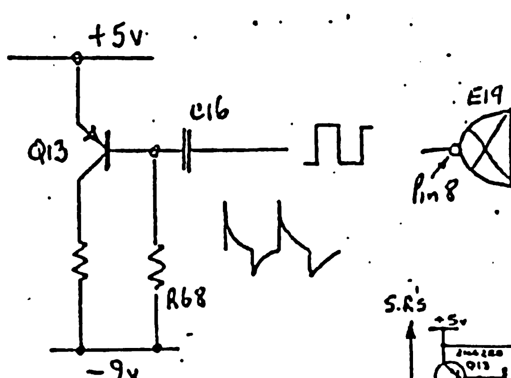
SHIFT CLOCK/SKIP GENERATOR

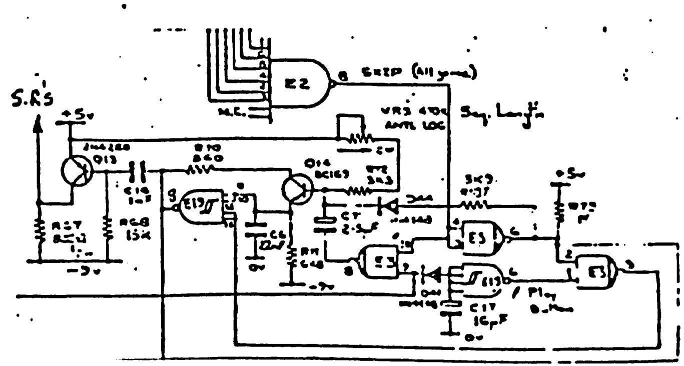
E19, Q14, C6, R71, R70, R72, VR3 is the high speed skip generator. It is a schmitt trigger oscillator. When C7 is operational the oscillator reverts to a low speed clock generator. In normal operation pin 8, E3 is low, C7 is thus effective and so a slow clock is generated. (Normal operation is during the recording and playing back, and not the pressing of those pads).

In normal operation, the output of E2 is high (i.e. the input is not all 1's) and so is the input pin 9, E3. When RECORD is pressed, all the inputs to E2 are high, the output of E2 goes low, and sets the skip oscillator into its skip mode, by making C7 ineffective. The shiftregister is thus filled with 0's. Also, the two meterdivider circuits E20, E24 are reset to zero.

When the KEYBOARD is pressed, the input gates to the shift registers are opened, and so the inputs to E2 change from all 1's to a mixture of 0's and 1's. (Note an all 1's condition cannot occur in normal operation). The output of E2 goes to 1. Thus, the output pin 8 of E3 goes to 0, C7 is functional so the oscillator begins to clock in its slow mode. Also, the reset on E24, 20 is in its count mode, the clock being taken from E19 pin 8. The output from E19, 8 is differentiated by C16, R68 to give a very shart pulse, which appears at Q13's collector, and is used to drive all the shift registers.







When the PLAY pad is pressed. Input pin 9, E3 goes low (but only for the duration of the pressing of the pad); this causes the data to rapidly recirculate (skip), usually for one bit only (because E3, 8 is high).

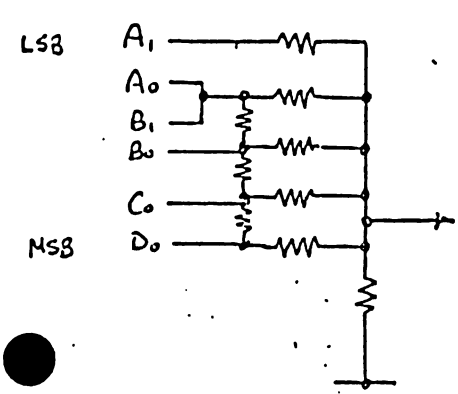
E3, 9 is low. Hence E19,6 is high.
E2, 8 is high.

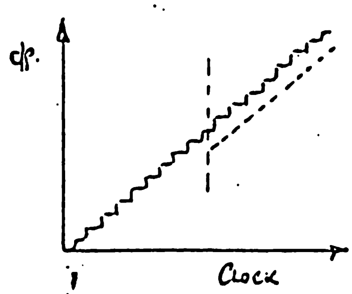
Nothing happens until an "all low-state" of the shift registers is detected by E2 (*all 1's as seen by E2). When this state is located, E2 ,8 falls to 0, therefore E3, 6 goes high, and in doing so resets E20, E24. Also, there are now two high's at the input to E3, (1,2,3) and so E3, 3 goes low and in doing so disables E19 (8,9,10,12,13) the oscillator. If there are no empty storage locations, the network just rapidly recirculates, and a "buzz" is heard.

When the play pad is released, pin 9,E3 goes high, however E3, 8 still remains high; E19, 6 takes a short time to go low because of the effect of E17: (This eliminates spurious effects when operating the play pad.) When E19,6 goes low, E3, 3 goes high, thus enabling the clock oscillator. The clock is in its high speed mode (skip) and so it races past all the unused storage area and when it comes to the first piece of data, E2, 8 goes high, the clock thus reverts to its slow speed mode, and E24, E20 is set to its count mode. Thus, the stored data is replayed, and when the end is reached there is a rapid skip and the process repeats itself.

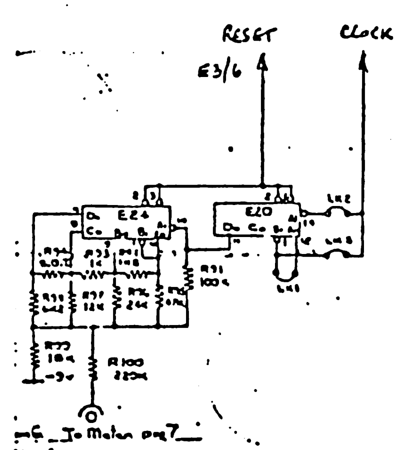
METER COUNTER

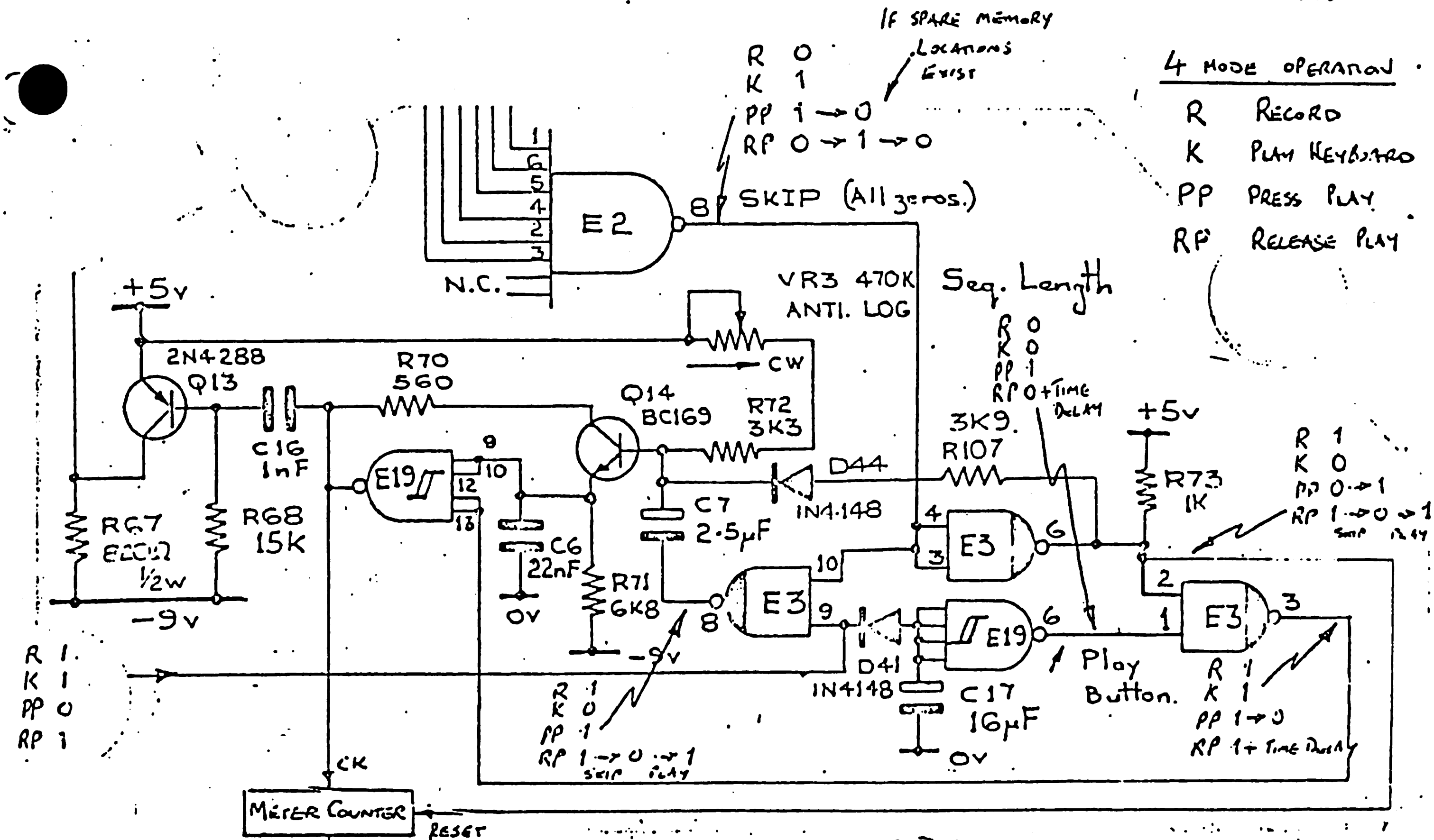
The clock is divded by ÷ 16 twice, which is 256, the length of the memory. The 5 most significant bits are decoded in the meter DAC. This is E24 and the resistor network. The network is a "weighted/ladder" - (a Cockeral special).

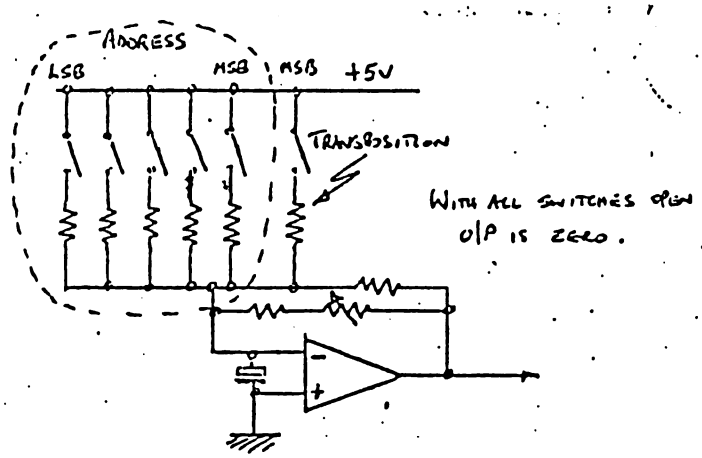




THE BIGGEST ERROR IN LINEARITY COMES ½ WAY WHERE A PRONOUNCED STEP CAN SOMETIMES OCCURE.







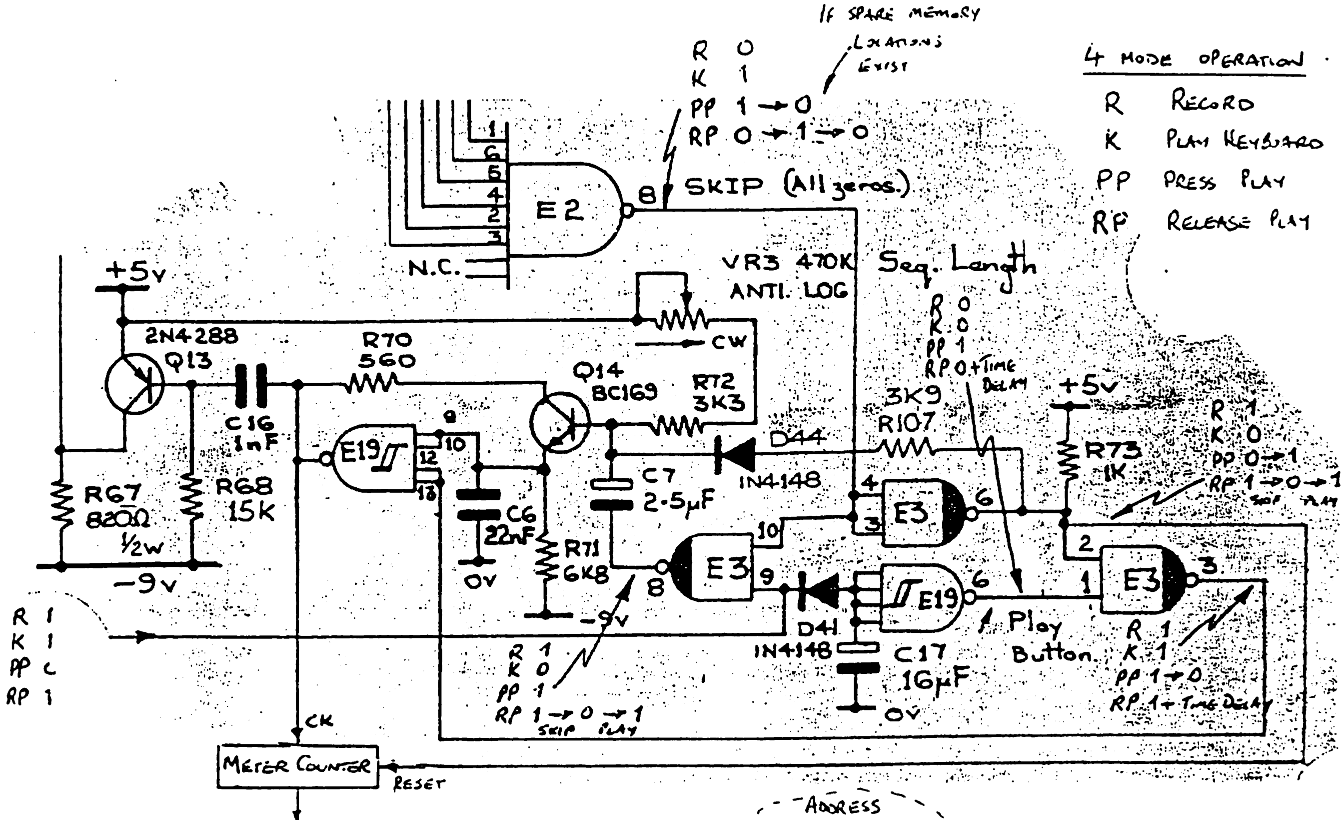
MEMORY DAC

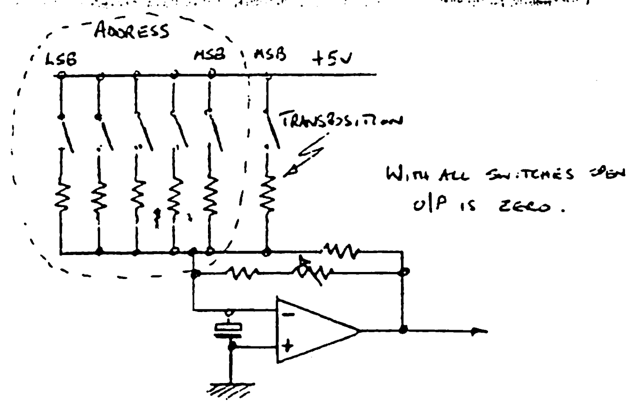
The second DAC is a 5 bit device with a 6th bit controlled by the transposition pad. The "transposition pad" bit is the same order of magnitude as the MSB of the address bits.

The switches are transistors Q7 and Q8—Q12 and the operation is similar to the real time DAC. Note, that the transposition acts only on the recorded output DAC, but no record of transposition playing is stored in the memory. Transposition is real time only.

TRANSPOSITION.

The transposition multiplexer operates in a similar manner to the two other multiplexers. One difference is a feed-back circuit E11 (8,12,11) that causes single events to be multiplied. Looking at E7, we have:-





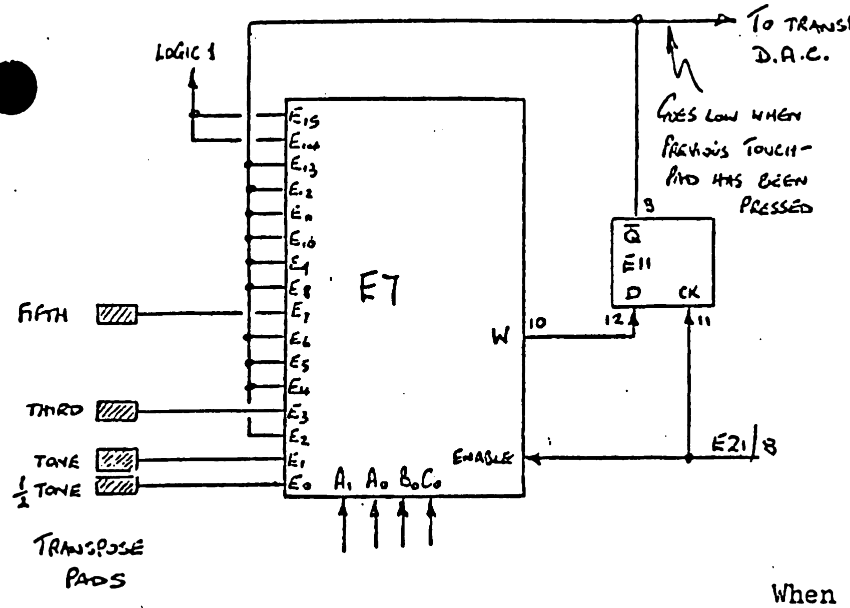
MEMORY DAC

The second DAC is a 5 bit device with a 6th bit controlled by the transposition pad. The "transposition pad" bit is the same order of magnitude as the MSB of the address bits.

The switches are transistors Q7 and Q8—Q12 and the operation is similar to the real time DAC. Note, that the transposition acts only on the recorded output DAC, but no record of transposition playing is stored in the memory. Transposition is real time only.

TRANSPOSITION.

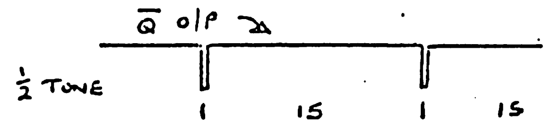
The transposition multiplexer operates in a similar manner to the two other multiplexers. One difference is a feed-back circuit E11 (8,12,11) that causes single events to be multiplied. Looking at E7, we have:-



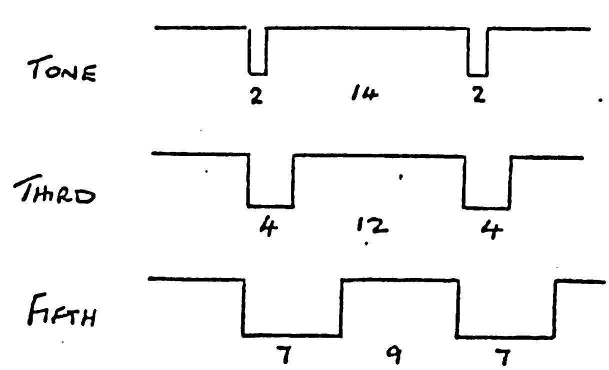
The multiplexer is addressed in the usual way, and is enabled and has the same touch sensitivity as before.

When Eo is pressed, it is prevented from going high, and so the output at W is high for Eo.

therefore pressing Eo produces a 1 bit pulse at E11 pin 8.



Pressing the tone causes W to be high for E1. But the output $\overline{Q}$ of E11 is fed back to E2. And so when E2 is addressed the output is again high but stops when it gets to E3.



*Notice E14, E15 are never low.

Now, the output from E11 pin 8 is used to control the DAC on the recorded output. As the transposition signal is a mark/space ratio signal, then the resultant product from the DAC must be smoothed out, this being accomplished by C5. The transposition signal is used to control a logic switch of equal status to the MSB of the 5 bit DAC.

The thirty notes available from the keyboard form $2\frac{1}{2}$ octaves, (i.e. 12 notes per octave). Therefore 12 logic bit = 1 Octave
or 1 semitone = 1 logic bit.
where 1 octave = 12 semitones.

The MSB of the address is equivalant to 16 logic bits. Therefore as the transpose controls a switch of equal status to the MSB, then one bit of the transpose signal = 1 semitone.

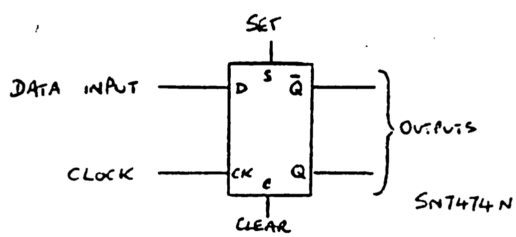
Therefore, pressing the $\frac{1}{2}$ tone pad = 1 bit = 1 semitone.
pressing the tone pad = 2 bits = 2 semitones.
pressing the third pad = 4 bits = 4 semitones.
pressing the fifth pad = 7 bits = 7 semitones.

that is, pressing the <u>keyboard</u> and the transposition pad, tranposes the note generated upwards by the respective amount.

* Example:- pressing the $\frac{1}{2}$ tone, third and fifth will shift a note up by one octave. (That is, if the keyboard has been adjusted to $2\frac{1}{2}$ octaves)
1 + 4 + 7 = 12 semitones = 1 octave.

(* An octave - the ratio of two frequencies which are at frequencies of F and 2F. F being arbitary).

<u>APPENDIX</u>



D type, used usually as a one bit delay or an edge detector.

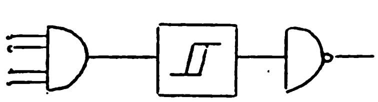
Logic data is presented to the D input. The data (0 or a 1) appears at the Q output after the +ve edge of the clock pulse, that is:-

data is transferred to the Q output on the +ve edge of the clock:-

<u>Set</u> - a 0 on the set puts Q to 1
<u>Clear</u>- a 0 on the clear puts Q to 0

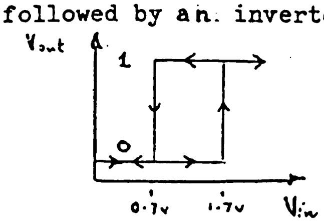
set and clear are independant of the clock and overide the D input.

<u>SCHMITT</u>

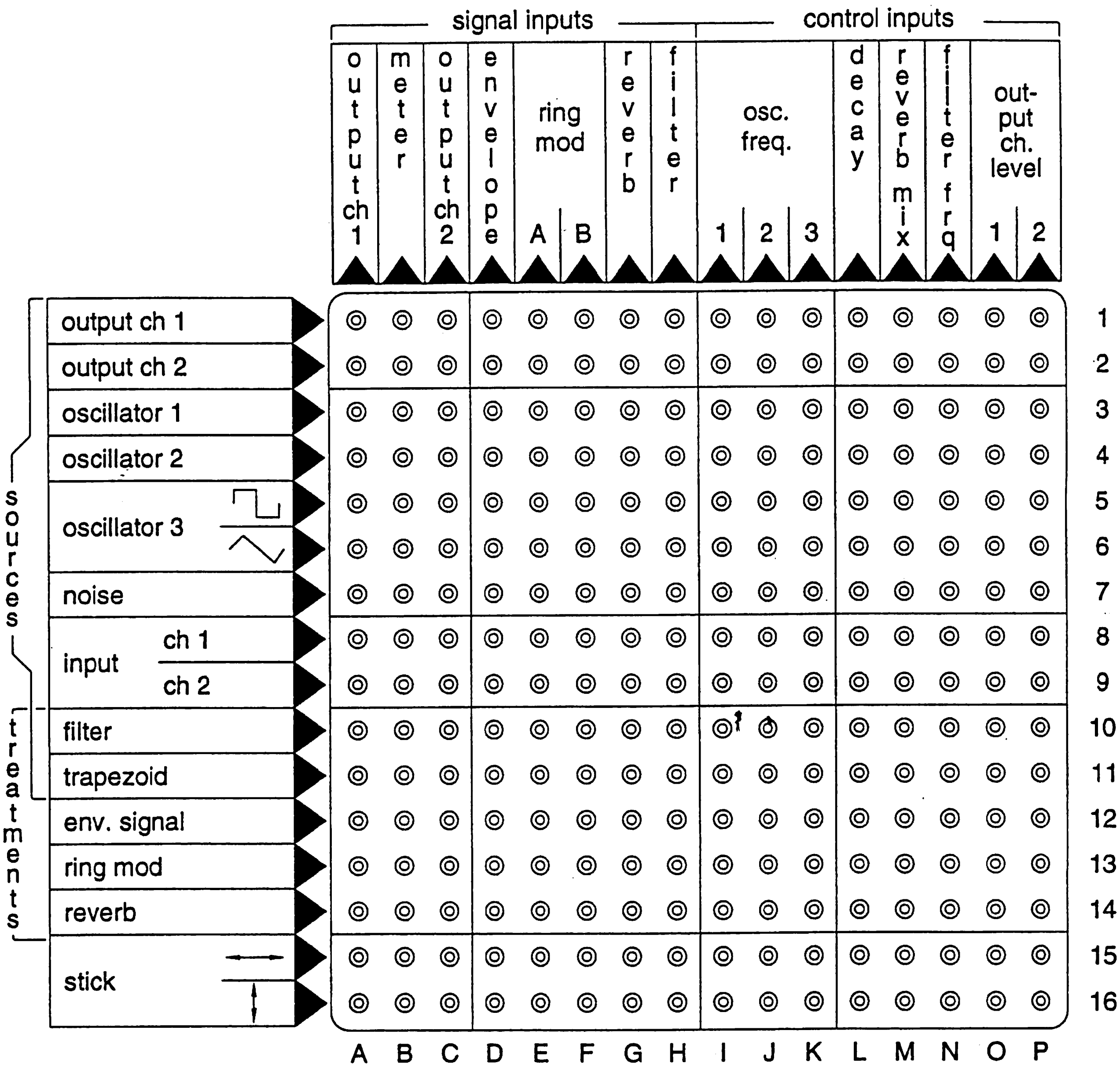


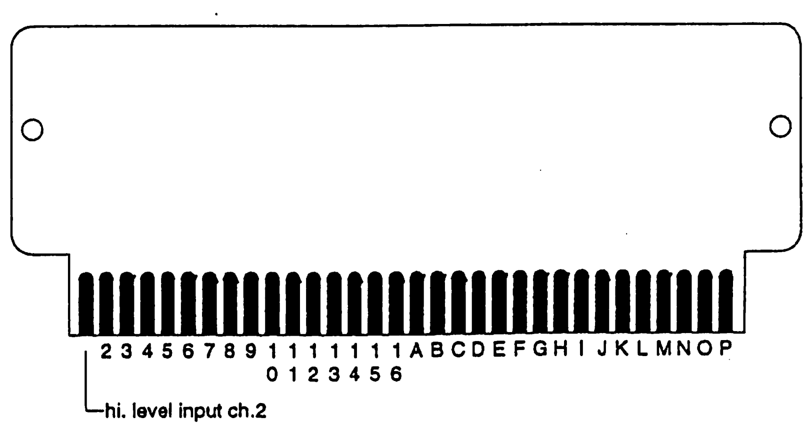
SN7413N

The SN7413N looks like a 4 input AND, followed by a schmitt trigger, followed by an inverter. The schmitt trigger exhibits a phenomena known as Hysterysis.

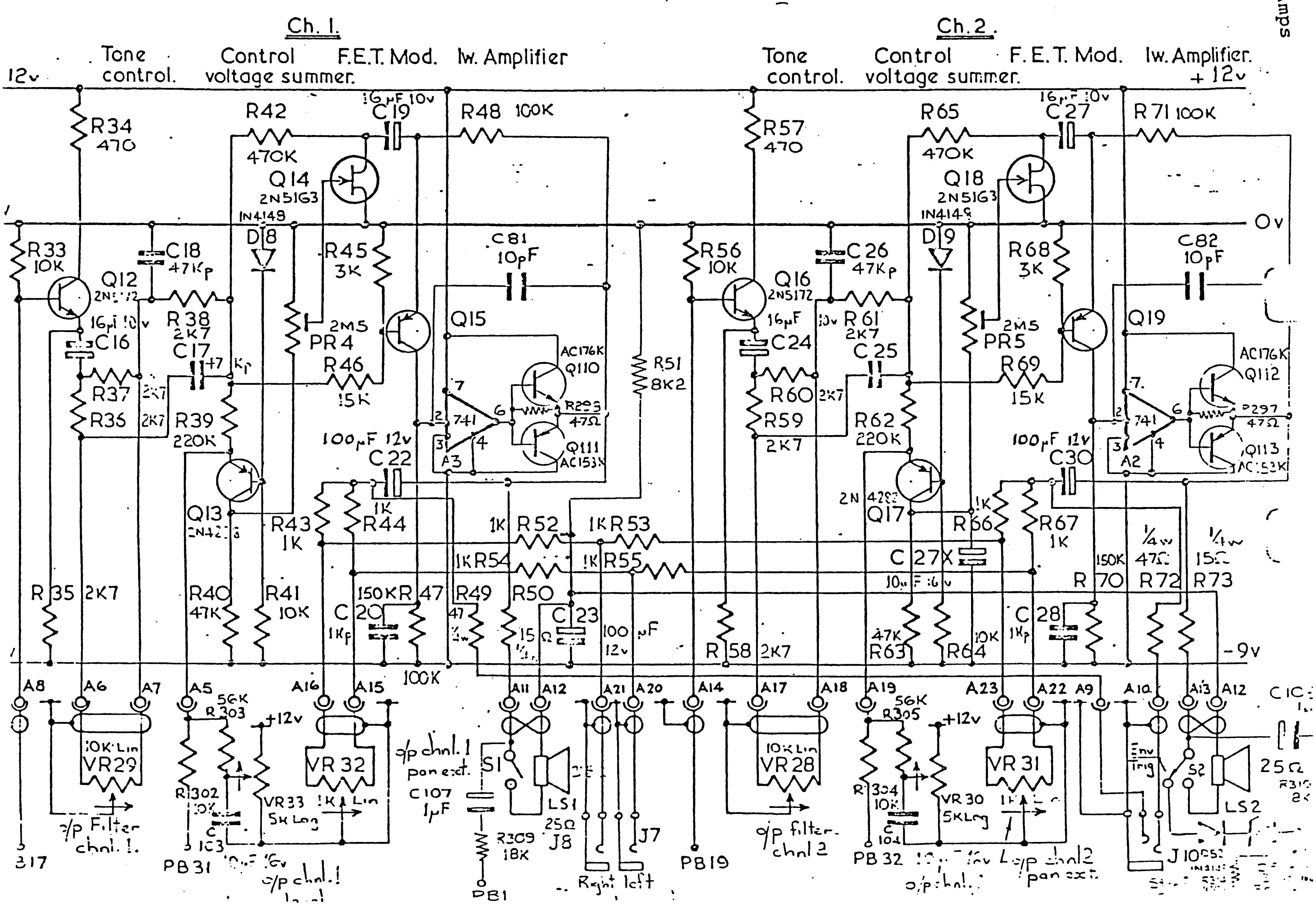


AKS Patch Sheet





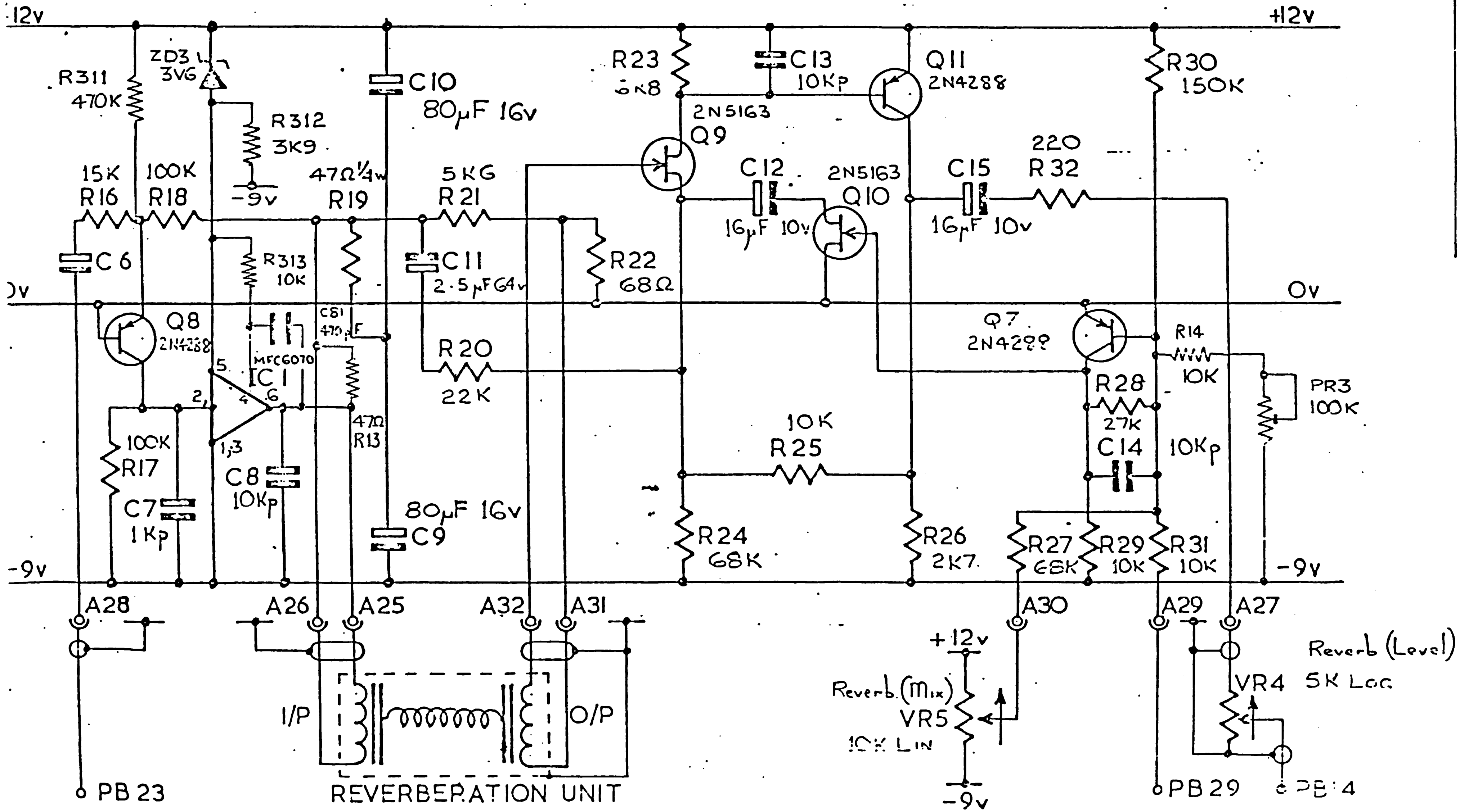
Output Amps
Board A



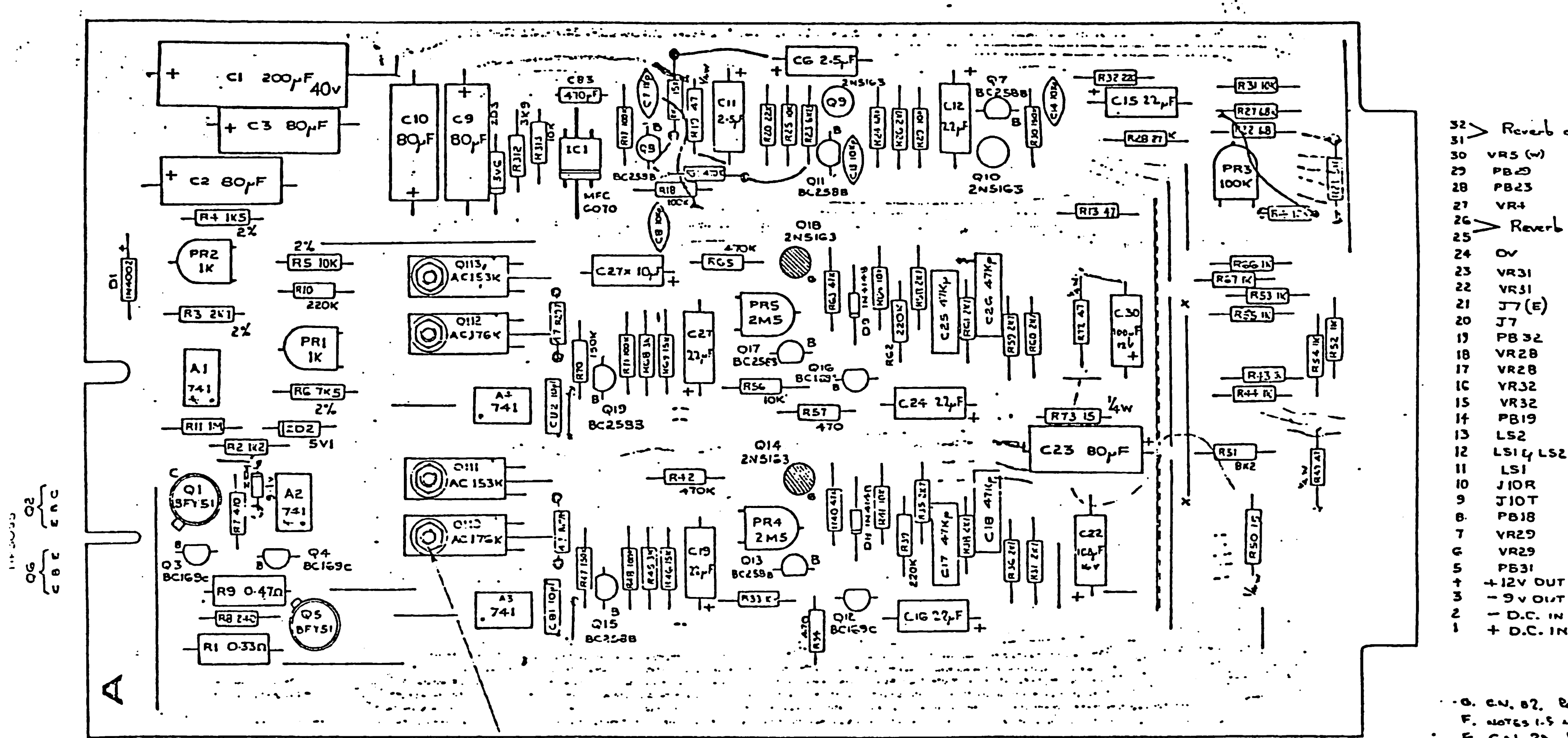
REVERBERATION P.C. BOARD A.

Hi-Zo drive amplifier.

Pick-up amplifier & voltage controlled mixer.



NOTE! Q14 & Q18 MATCHED FOR V_P & I_{DSS}.



Mounting Pads to be used on Q1 & Q5 TO5 types

4 x 6BA - 1/2 CH. (0-SIN) + FULL NUT & S PROOF

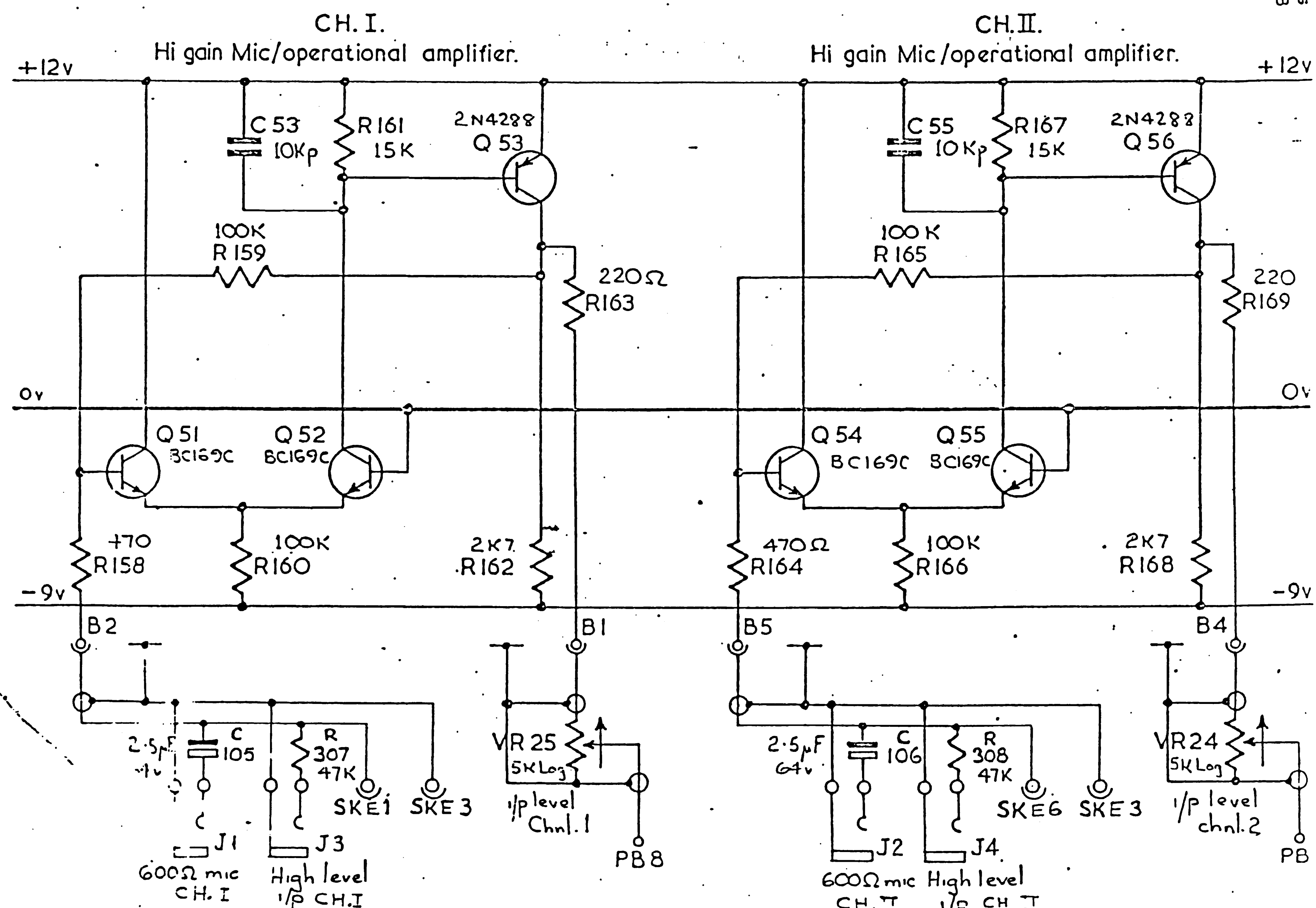
* ALSO ALL TEXAS TYPE PREFERRED

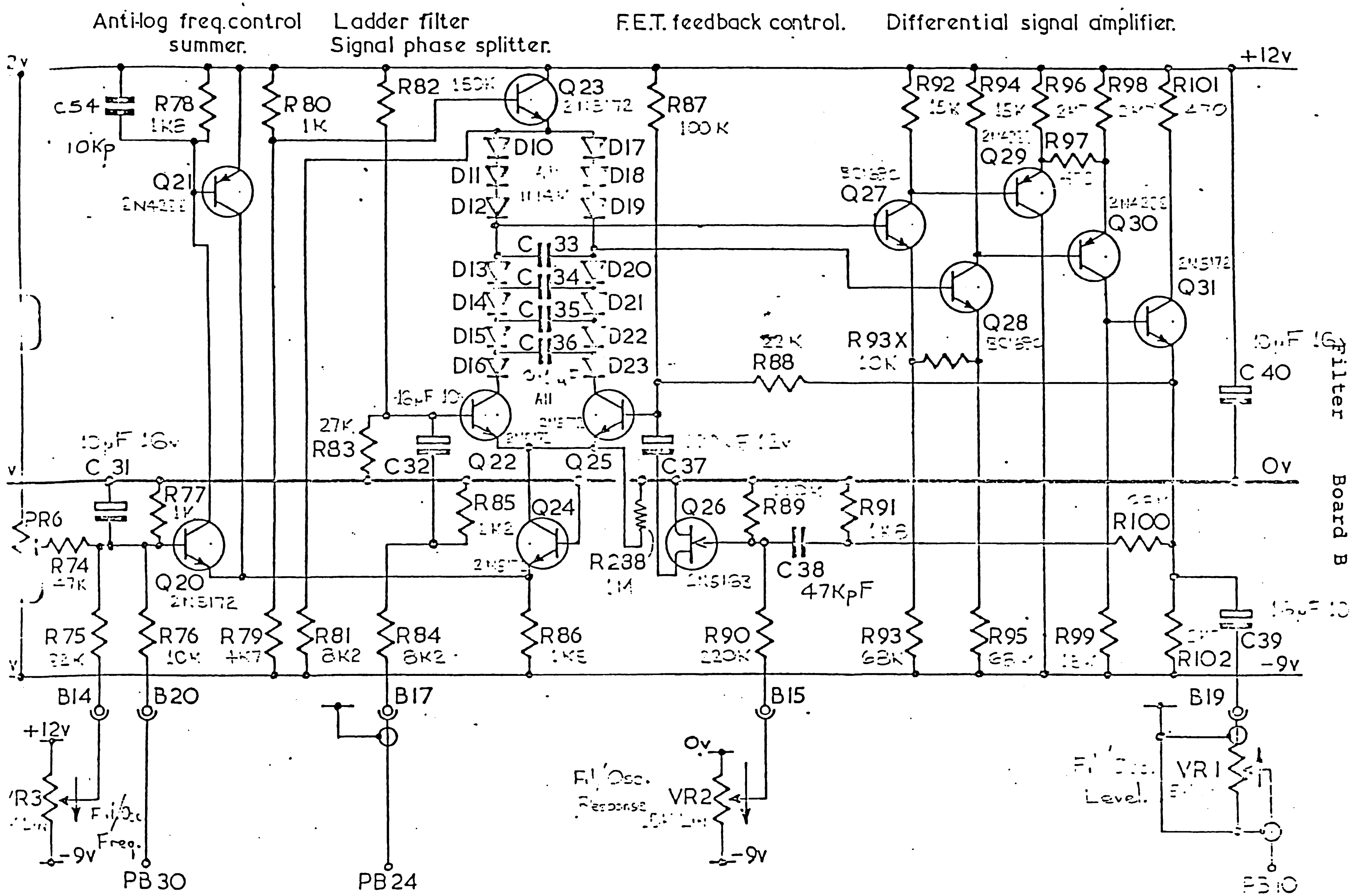
G. C.N. 82. Rc. 15.8.73.
F. NOTES 1-5 ADDED Rc. 11.6.73
E. C.N. 29 Rc. 21.5.73.
D. C.N. 44 / C.N. 33 5/3/73
C. Power Amp. Redesign

HILTON ELECTRONICS (WAREHAM) LTD

TITLE 'A' BOARD SYNTHI AKS & 1.51

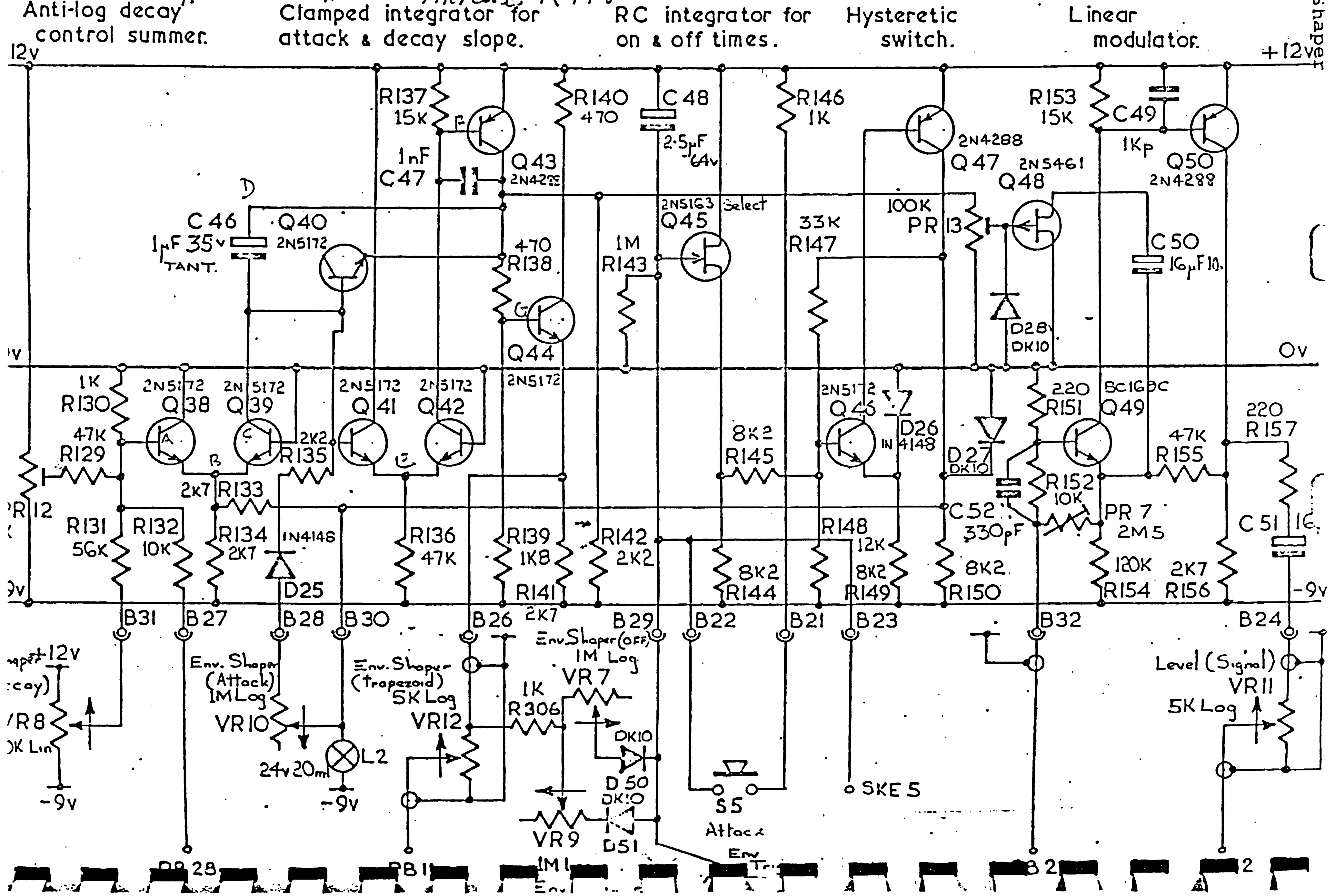
NOTE: 1. C1 SHOWN AS 25V ON BOARD
2. R34 VALUE i.e. 470 NOT SHOWN ON BOARD.
3. LINK BETWEEN POINTS X-X NOT SHOWN ON BOARD.
4. POS. NOT SHOWN ON C16.
5. C12, 15, 16, 19, 22, 24, 27, 30 SHOWN AS 100μF ON BOARD.


CH. I.
Hi gain Mic/operational amplifier.
CH. II.
Hi gain Mic/operational amplifier.
+12v
0v
-9v
C53 10Kp
R161 15K
2N4288 Q53
100K R159
220Ω R163
Q51 BC169C
Q52 BC169C
470 R158
100K R160
2K7 R162
B2
B1
2.5μF
C 105
R 307 47K
SKE1
SKE3
VR25 5K Log
I/P level Chnl. 1
PB8
J1 600Ω mic CH. I
J3 High level I/P CH. I
C55 10Kp
R167 15K
2N4288 Q56
100K R165
220 R169
Q54 BC169C
Q55 BC169C
470Ω R164
100K R166
2K7 R168
B5
B4
2.5μF 64v
C 106
R 308 47K
SKE6
SKE3
VR24 5K Log
I/P level chnl. 2
PB
J2 600Ω mic CH. II
J4 High level I/P CH II

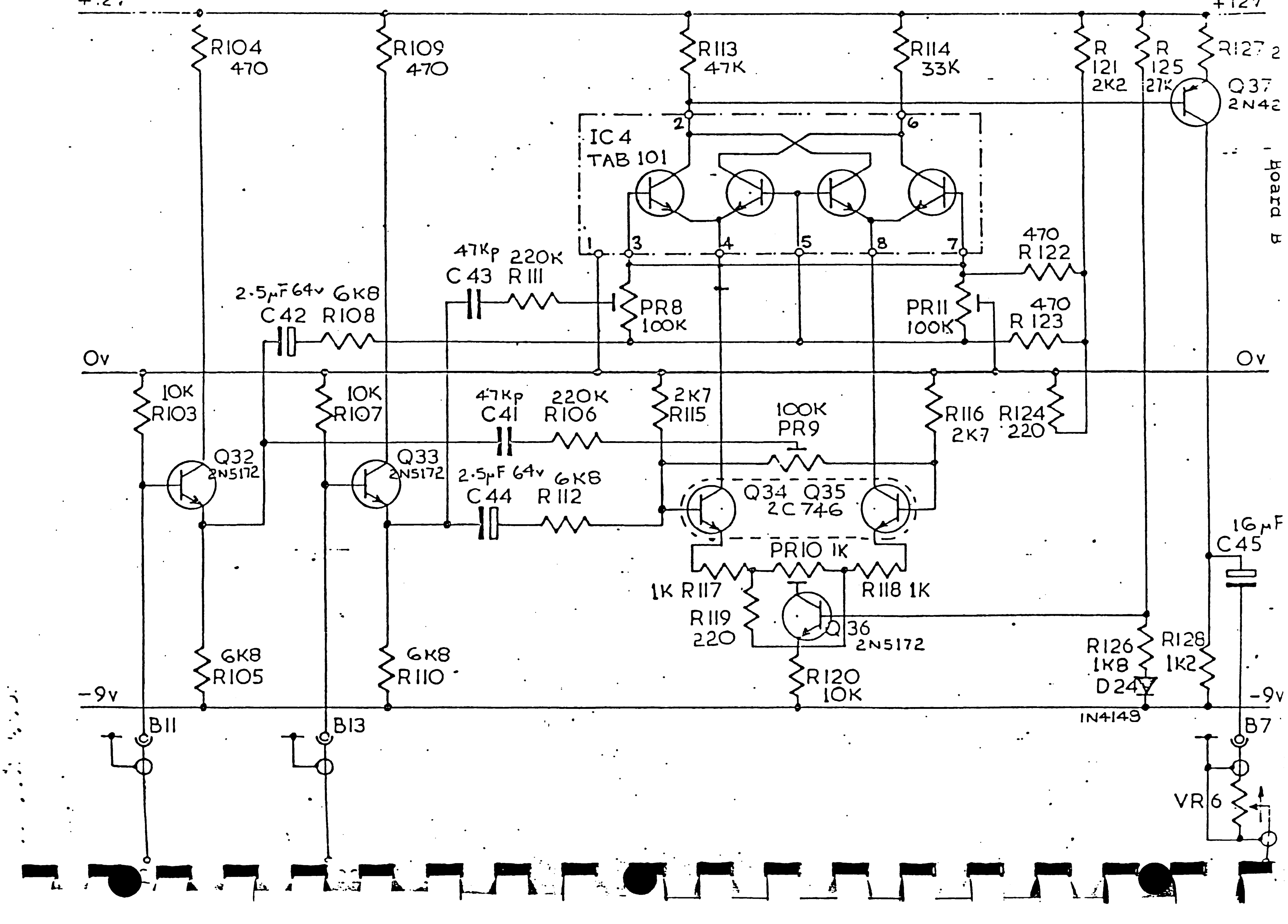

Anti-log freq.control summer.
Ladder filter Signal phase splitter.
F.E.T. feedback control.
Differential signal amplifier.
+12v
0v
-9v
Filter
Board B
C54
10Kp
R78
1K8
R80
1K
R82
Q23
R87
100K
R92
15K
R94
15K
R96
R98
R101
R97
Q21
2N4289
Q29
Q27
Q30
Q31
Q28
D10
D11
D12
D17
D18
D19
C33
C34
C35
C36
D13
D14
D15
D16
D20
D21
D22
D23
All
R93X
10K
R88
22K
C40
R83
27K
C32
C31
C37
Q22
Q25
R85
Q24
Q26
R89
R91
R100
PR6
R77
1K
R74
47K
Q20
R238
C38
47KpF
C39
R75
R76
10K
R79
4K7
R81
8K2
R84
8K2
R86
R90
220K
R93
68K
R95
R99
R102
B14
B20
B17
B15
B19
+12v
VR3
-9v
Freq.
PB30
PB24
0v
VR2
-9v
Level.
VR1

of proper ON-OFF times.

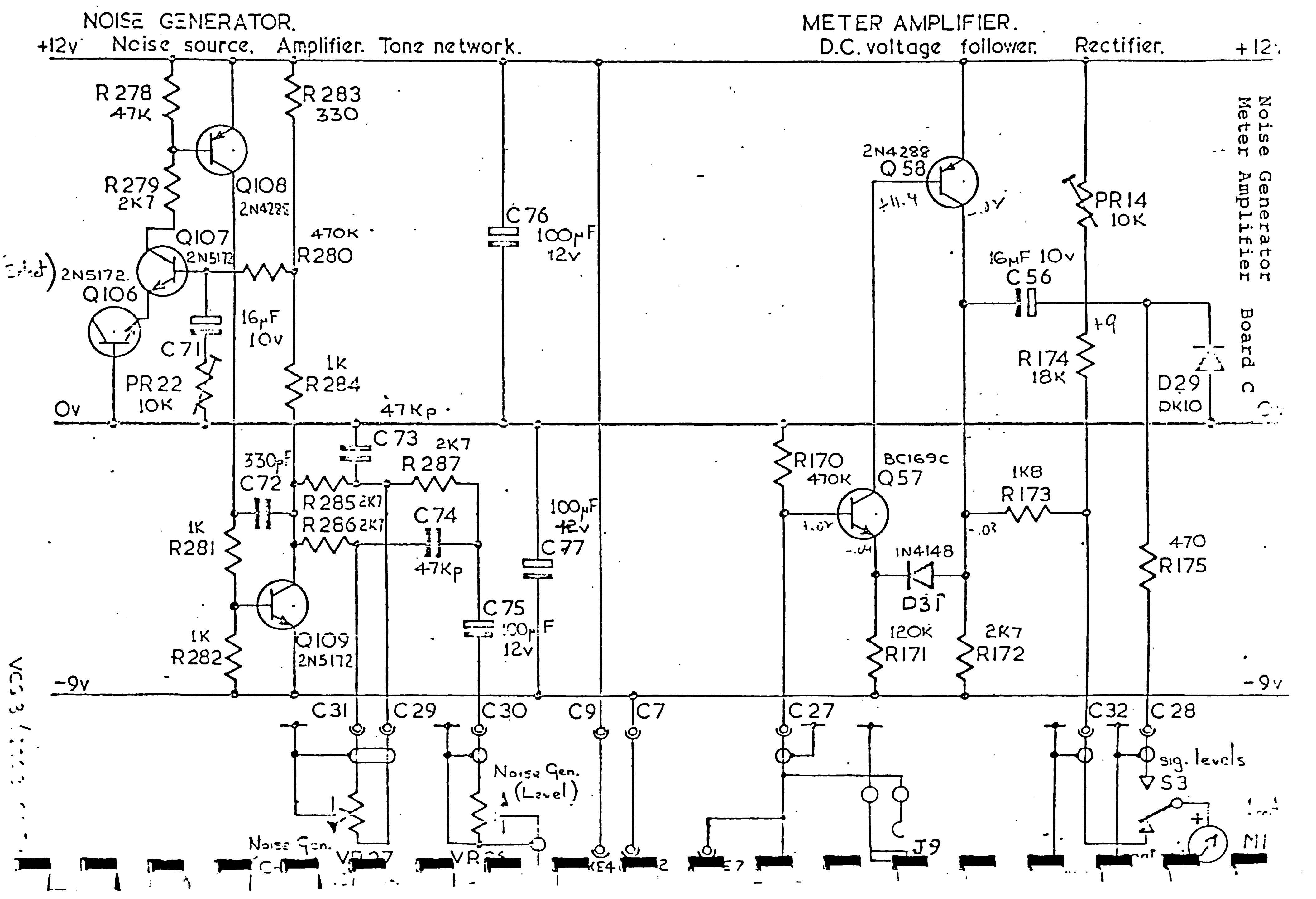
Trapezoid Should be even I around Zero - Select R139
ON Time infinite Reduce R148
off " " increase R148

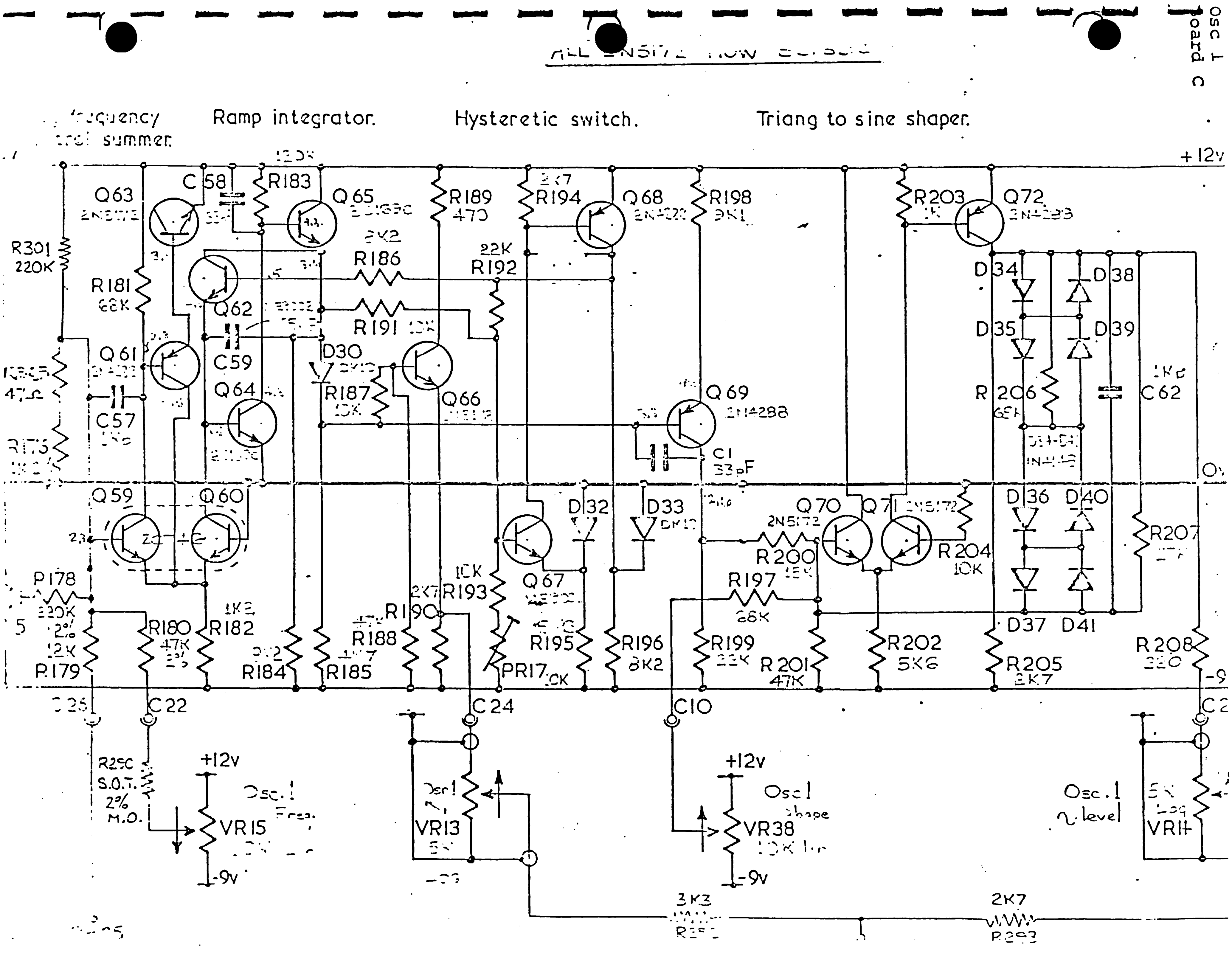


Double balanced modulator

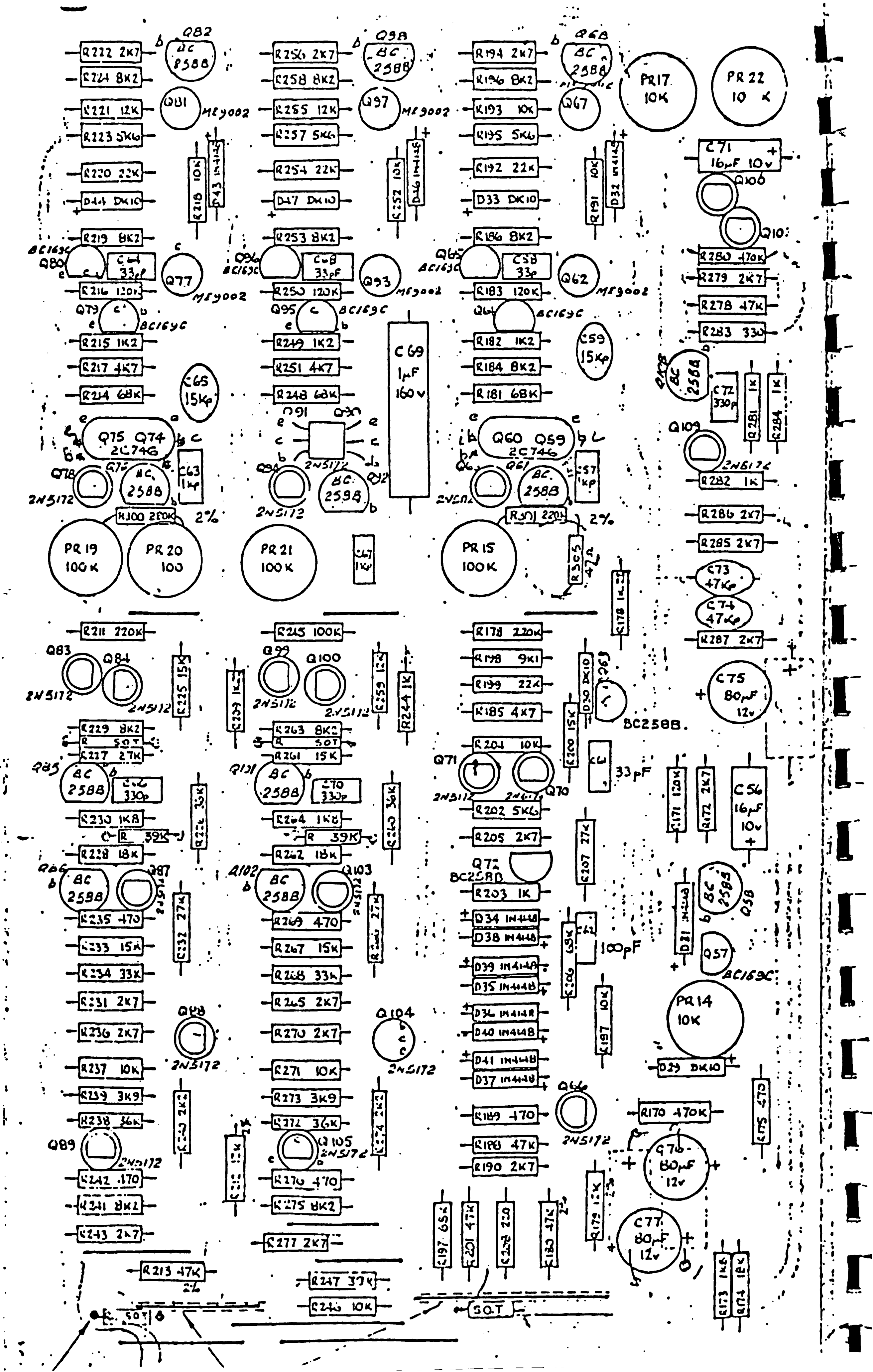


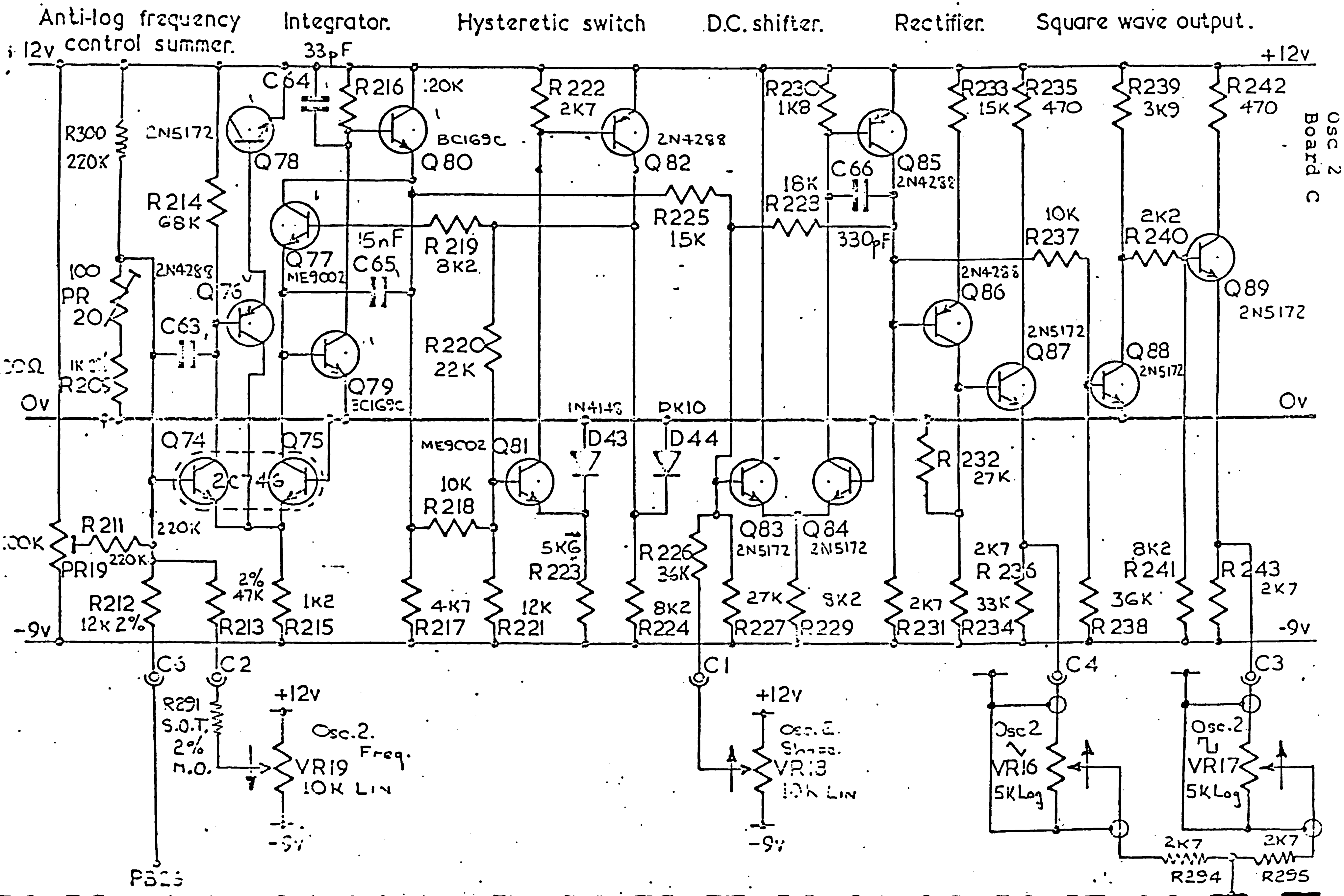
ALL


NOISE GENERATOR.
+12v
Noise source.
Amplifier.
Tone network.
METER AMPLIFIER.
D.C. voltage follower.
Rectifier.
Noise Generator Meter Amplifier Board C
R278 47K
R279 2K7
Q108 2N4288
Q107 2N5172
2N5172. Q106
C71
16µF 10v
PR22 10K
R283 330
470K R280
1K R284
C76 100µF 12v
47Kp
0v
330pF C72
1K R281
1K R282
Q109 2N5172
C73
2K7 R287
R285 2K7
R286 2K7
C74
47Kp
C75 100µF 12v
100µF 12v C77
-9v
C31
C29
C30
C9
C7
Noise Gen. (Level)
Noise Gen.
VR27
2N4288 Q58
PR14 10K
16µF 10v C56
+9
R174 18K
D29 DK10
R170 470K
BC169C Q57
1K8 R173
1N4148
D31
470 R175
120K R171
2K7 R172
C27
C32
C28
sig. levels
S3
J9
M1

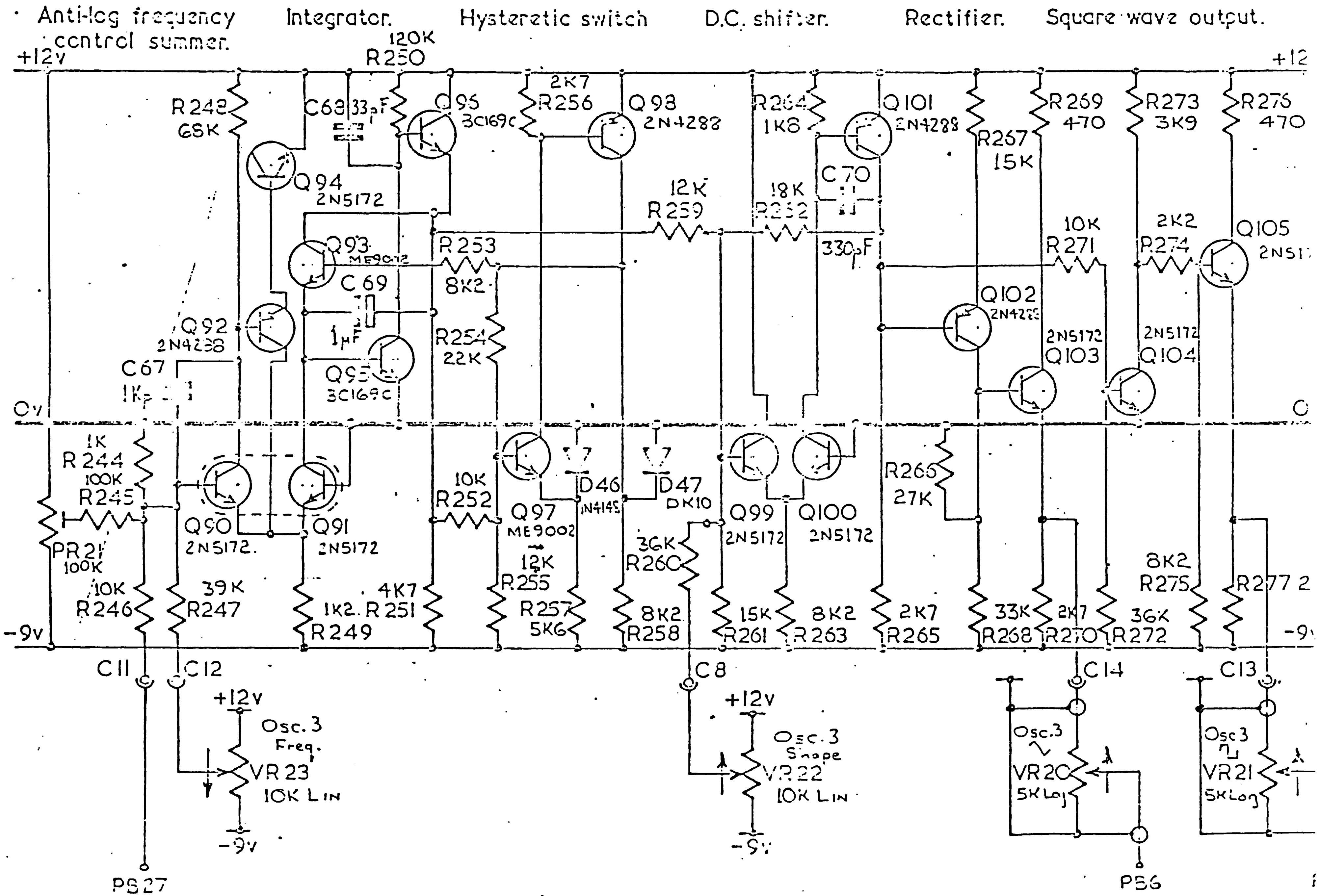


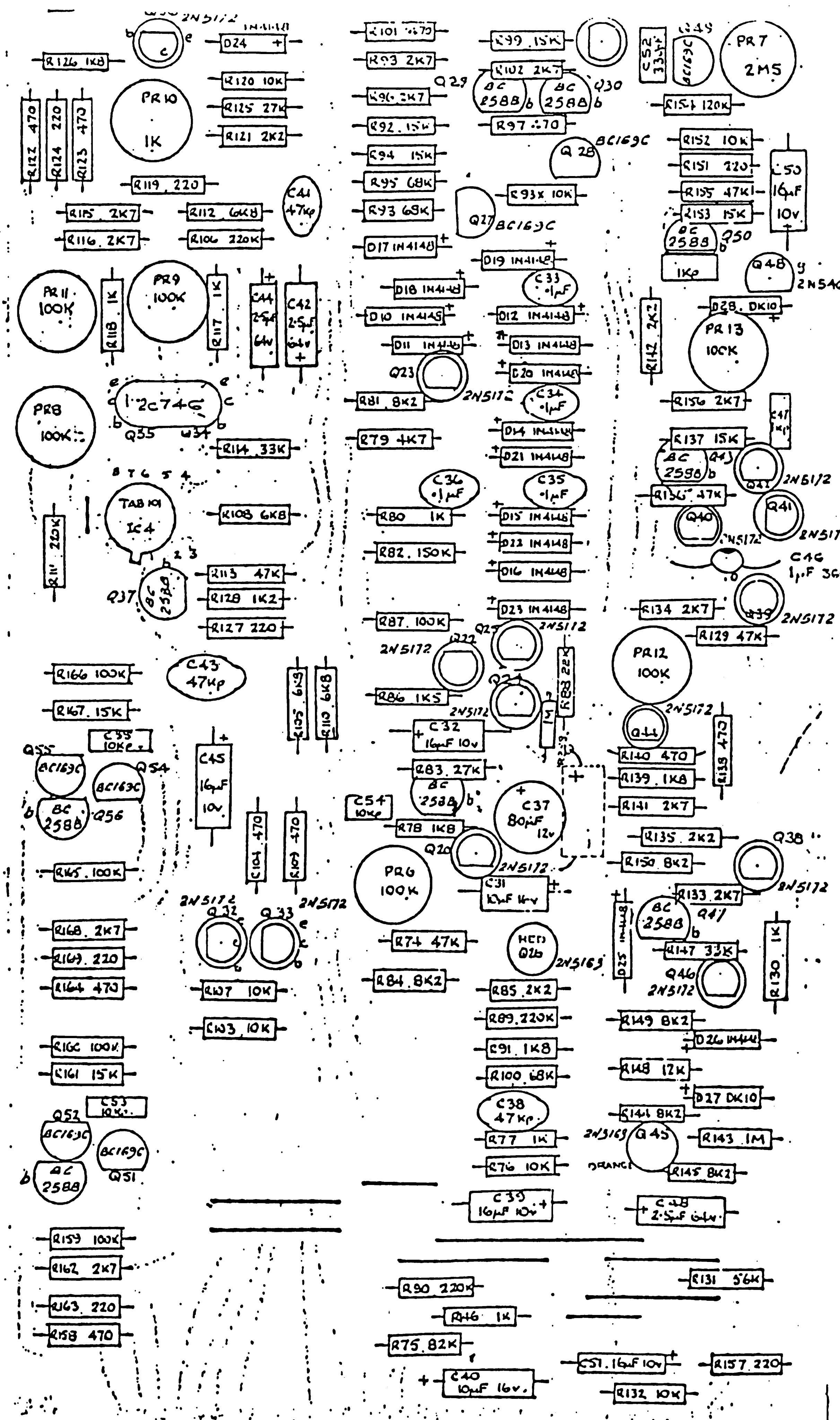
Osc 1
Board C
Frequency control summer
Ramp integrator.
Hysteretic switch.
Triang to sine shaper.
+12v
0v
-9
R301 220K
R181 68K
R179 12K
R180 47K 2%
R182 1K2
P178 220K 2%
C57 1n
C58
C59
R183
R184
R185
R186 2K2
R187 10K
R188
R189 470
R190
R191 10K
R192 22K
R193 10K
R194 2K7
R195
R196 8K2
R197 68K
R198
R199 22K
R200
R201 47K
R202 5K6
R203 1K
R204 10K
R205 2K7
R206
R207
R208
C62
C1 33pF
Q59
Q60
Q61
Q62
Q63
Q64
Q65
Q66
Q67
Q68
Q69 2N4288
Q70
Q71 2N5172
Q72
D30
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
PR17 10K
C22
C24
C10
R290 S.O.T. 2% M.O.
VR15
Osc.1 Freq.
VR13
VR38 10K lin
Osc 1 shape
Osc.1 ∿ level
VR14
+12v
-9v
3K3
2K7
R293


Q82 BC 258B
R222 2K7
R224 8K2
R221 12K
R223 5K6
Q81 ME9002
R220 22K
D44 DK10
R218 10K
D43 IN4148
R219 8K2
Q80 BC169C
C64 33pF
Q77 ME9002
R216 120K
Q79 BC169C
R215 1K2
R217 4K7
R214 68K
C65 15Kp
Q75 Q74 2C746
Q78 2N5172
Q76 BC 258B
C63 1Kp
R300 220K 2%
PR19 100K
PR20 100
Q98 BC 258B
R256 2K7
R258 8K2
R255 12K
R257 5K6
Q97 ME9002
R254 22K
D47 DK10
R252 10K
D46 IN4148
R253 8K2
Q96 BC169C
C68 33pF
Q93 ME9002
R250 120K
Q95 BC169C
R249 1K2
R251 4K7
R248 68K
Q91 Q90 2N5172
Q94 2N5172
Q92 BC 258B
C69 1μF 160v
PR21 100K
C67 1Kp
Q68 BC 258B
R194 2K7
R196 8K2
R193 10K
R195 5K6
Q67
R192 22K
D33 DK10
R191 10K
D32 IN4148
R186 8K2
Q65 BC169C
C58 33p
Q62 ME9002
R183 120K
Q64 BC169C
R182 1K2
R184 8K2
R181 68K
C59 15Kp
Q60 Q59 2C746
Q61 BC 258B
C57 1Kp
R301 220K 2%
PR15 100K
R305 47Ω
PR17 10K
PR22 10K
C71 16μF 10v
Q106
Q107
R280 470K
R279 2K7
R278 47K
R283 330
Q108 BC 258B
C72 330p
R281 1K
R284 1K
Q109 2N5172
R282 1K
R286 2K7
R285 2K7
C73 47Kp
C74 47Kp
R287 2K7
C75 80μF 12v
R211 220K
Q83 Q84 2N5172
R225 15K
R229 8K2
R SOT
R227 27K
Q85 BC 258B
C66 330p
R230 1K8
R 39K
R226 33K
R228 18K
Q86 BC 258B
Q87 2N5172
R232 27K
R235 470
R233 15K
R234 33K
R231 2K7
R236 2K7
Q88 2N5172
R237 10K
R239 3K9
R238 36K
R240 2K2
Q89 2N5172
R242 470
R241 8K2
R243 2K7
R213 47K 2%
SOT
R245 100K
Q99 Q100 2N5172
R259 1K2
R244 1K
R263 8K2
R SOT
R261 15K
Q101 BC 258B
C70 330p
R264 1K8
R 39K
R260 36K
R262 18K
Q102 BC 258B
Q103 2N5172
R269 470
R267 15K
R268 33K
R265 2K7
R270 2K7
Q104 2N5172
R271 10K
R273 3K9
R272 36K
R274 2K2
Q105 2N5172
R276 470
R275 8K2
R277 2K7
R247 33K
R246 10K
R178 220K
R178 1K2
R198 9K1
R199 22K
R185 4K7
D30 DK10
Q63 BC258B
R204 10K
R200 15K
C61 33pF
Q71 2N5172
Q70 2N5172
R202 5K6
R205 2K7
R207 27K
Q72 BC258B
R203 1K
D34 IN4148
D38 IN4148
D39 IN4148
D35 IN4148
D36 IN4148
D40 IN4148
D41 IN4148
D37 IN4148
C62 100pF
R197 10K
R189 470
R188 47K
R190 2K7
Q66 2N5172
R197 65K
R201 47K
R208 220
R180 47K
R179 1K
SOT
R171 120K
R172 2K7
C56 16μF 10v
Q58 BC 258B
D31 IN4148
Q57 BC169C
PR14 10K
D29 DK10
R170 470K
R175 470
C76 80μF 12v
C77 80μF 12v
R173 1K6
R174 18K

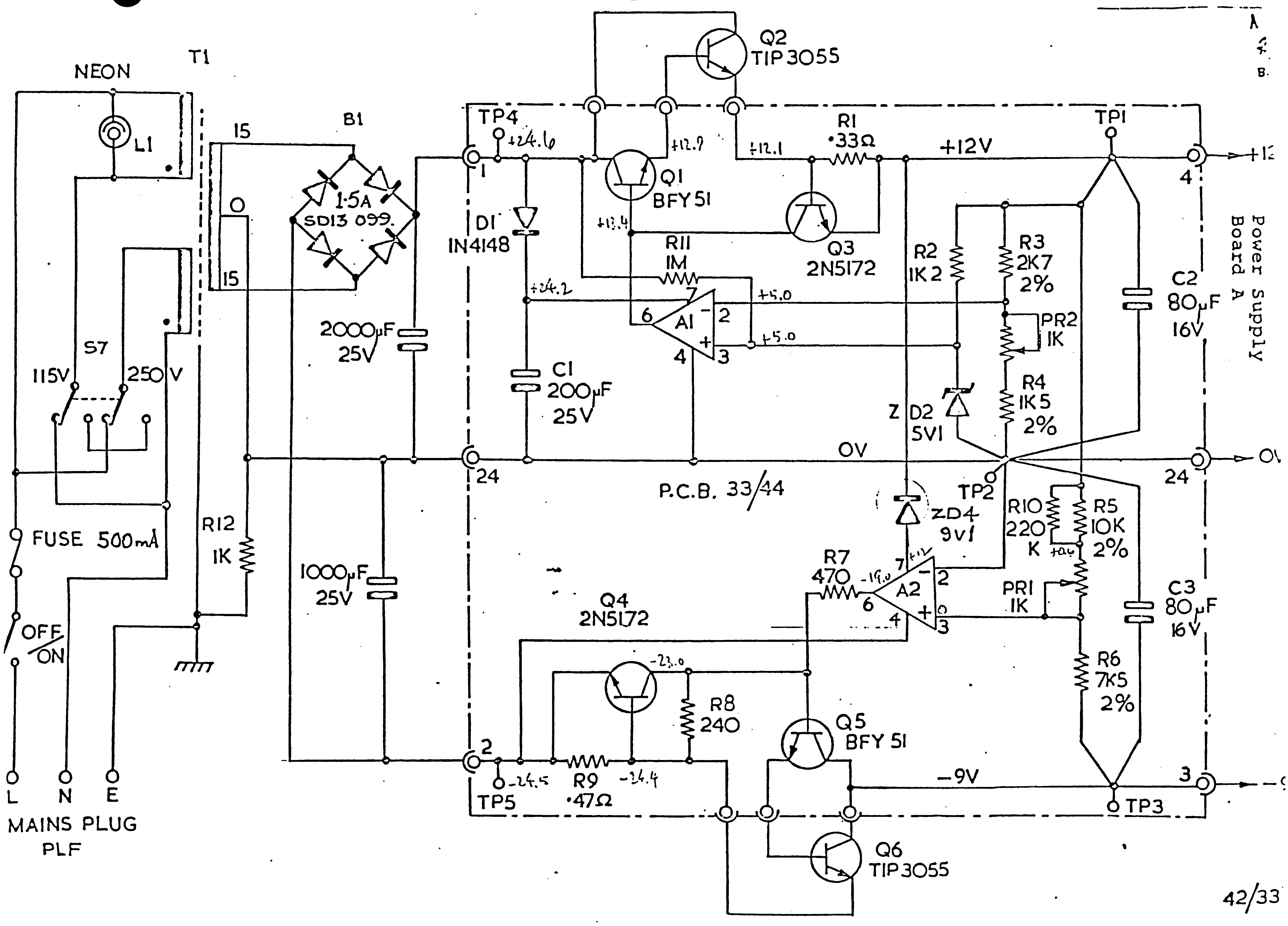

Anti-log frequency control summer.
Integrator.
Hysteretic switch
D.C. shifter.
Rectifier.
Square wave output.
+12v
0v
-9v
Osc 2 Board C
R300 220K
2N5172
Q78
C64
33pF
R216 120K
BC169C
Q80
R222 2K7
2N4288
Q82
R230 1K8
Q85 2N4288
C66 330pF
R233 15K
R235 470
R239 3K9
R242 470
R214 68K
Q77 ME9002
15nF C65
R219 8K2
R225 15K
18K R223
10K R237
2K2 R240
Q89 2N5172
100 PR 20
2N4288 Q76
C63
Q79 BC169C
R220 22K
2N4288 Q86
2N5172 Q87
Q88 2N5172
1K R209
1N4148 D43
DK10 D44
Q74 Q75 2C746
ME9002 Q81
10K R218
R232 27K
R211 220K
100K PR19 220K
5K6 R223
R226 33K
Q83 2N5172
Q84 2N5172
R212 12K 2%
2% 47K R213
1K2 R215
4K7 R217
12K R221
8K2 R224
27K R227
8K2 R229
2K7 R231
33K R234
2K7 R236
36K R238
8K2 R241
R243 2K7
C5 C2 C1 C4 C3
R291 S.O.T. 2% M.O.
+12v
Osc.2. Freq.
VR19 10K LIN
-9v
Osc.2 Shape
VR13 10K LIN
Osc 2 VR16 5K Log
Osc.2 VR17 5K Log
2K7 R294
2K7 R295
PB23

Osc 3 Board C


Anti-log frequency control summer.
Integrator.
Hysteretic switch
D.C. shifter.
Rectifier.
Square wave output.
+12v
0v
-9v
R248 68K
C68 33pF
R250 120K
Q95 3C169C
R256 2K7
Q98 2N4288
R264 1K8
Q101 2N4288
R267 15K
R269 470
R273 3K9
R276 470
Q94 2N5172
C70
R259 12K
R262 18K
330pF
R271 10K
R274 2K2
Q105
Q93 ME9002
R253 8K2
C69 1μF
R254 22K
Q102 2N4288
Q92 2N4288
Q96 3C169C
2N5172 Q103
2N5172 Q104
C67
R244 1K
R245 100K
PR21 100K
Q90 2N5172
Q91 2N5172
R252 10K
Q97 ME9002
D46 1N4148
D47 DK10
R260 36K
Q99 2N5172
Q100 2N5172
R266 27K
R246 10K
R247 39K
R249 1K2
R251 4K7
R255 12K
R257 5K6
R258 8K2
R261 15K
R263 8K2
R265 2K7
R268 33K
R270 2K7
R272 36K
R275 8K2
R277
C11
C12
C8
C14
C13
Osc. 3 Freq.
VR23 10K Lin
Osc. 3 Shape
VR22 10K Lin
Osc. 3
VR20 5K Log
Osc 3
VR21 5K Log
PS27
PS6



2N5172
IN4148
D24
R126 1K8
R120 10K
R125 27K
R121 2K2
PR10
1K
R122 470
R124 220
R123 470
R119 220
R115 2K7
R116 2K7
R112 6K8
R106 220K
C41 47Kp
R101 470
R93 2K7
R96 2K7
R92 15K
R94 15K
R95 68K
R93 68K
D17 IN4148
R99 15K
R102 2K7
Q29
Q30
BC 2588
R97 470
Q28
BC169C
R93X 10K
Q27
BC169C
D19 IN4148
C52 33Kp
Q49
BC169C
PR7
2M5
R154 120K
R152 10K
R151 220
R155 47K
R153 15K
C50 16μF 10v
Q50
1Kp
Q48
2N5461
PR11 100K
R118 1K
PR9 100K
R117 1K
C44 2.5μF 64v
C42 2.5μF 64v
D18 IN4148
D10 IN4148
D11 IN4148
C33 ·1μF
D12 IN4148
D13 IN4148
D20 IN4148
Q23
2N5172
R142 2K2
D28 DK10
PR13 100K
PR8 100K
2c746
Q35
Q34
R114 33K
R81 8K2
R79 4K7
C34 ·1μF
D14 IN4148
D21 IN4148
R156 2K7
C47 1Kp
R137 15K
BC 2588
Q43
Q42
2N5172
TAB101
IC4
R108 6K8
R80 1K
C36 ·1μF
C35 ·1μF
D15 IN4148
D22 IN4148
D16 IN4148
R82 150K
R136 47K
Q40
Q41
2N5172
C46 1μF 36v
R111 220K
Q37
BC 2588
R113 47K
R128 1K2
R127 220
R87 100K
D23 IN4148
2N5172
R134 2K7
Q39
2N5172
R129 47K
PR12 100K
Q22
Q25
R88 22K
R166 100K
C43 47Kp
R105 6K8
R110 6K8
R86 1K5
R167 15K
C55 10Kp
Q55
BC169C
Q54
BC169C
BC 2588
Q56
C45 16μF 10v
C32 16μF 10v
R83 27K
C54 10Kp
BC 2588
C37 80μF 12v
R78 1K8
Q20
2N5172
Q44
R140 470
R139 1K8
R138 470
R141 2K7
R135 2K2
R150 8K2
Q38
2N5172
R165 100K
C104 470
R109 470
PR6 100K
C31 10μF 16v
R133 2K7
BC 2588
Q47
2N5172
Q32
Q33
R168 2K7
R169 220
R164 470
R74 47K
RED Q26
2N5163
D25 IN4148
R147 33K
Q46
2N5172
R130 1K
R107 10K
R103 10K
R84 8K2
R85 2K2
R89 220K
R91 1K8
R100 68K
R149 8K2
D26 IN4148
R160 100K
R161 15K
R148 12K
D27 DK10
C53 10Kp
Q52
BC169C
BC169C
Q51
BC 2588
C38 47Kp
R77 1K
R76 10K
R144 8K2
Q45
2N3163
ORANGE
R143 1M
R145 8K2
C39 16μF 10v
C48 2.5μF 64v
R159 100K
R162 2K7
R163 220
R158 470
R90 220K
R46 1K
R75 82K
C40 10μF 16v
C51 16μF 10v
R131 56K
R157 220
R132 10K


NEON
T1
L1
15
O
15
B1
1·5A
SD13 099.
2000μF
25V
S7
115V
250V
FUSE 500mA
OFF/ON
R12
1K
1000μF
25V
L N E
MAINS PLUG
PLF
Q2
TIP3055
TP4
+24.6
1
D1
IN4148
+24.2
C1
200μF
25V
Q1
BFY51
+12.9
+13.4
R11
1M
A1
7 6 2 3 4
+5.0
+12.1
R1
·33Ω
Q3
2N5172
+12V
TP1
R2
1K2
R3
2K7
2%
PR2
1K
R4
1K5
2%
Z D2
5V1
C2
80μF
16V
4
Power Supply
Board A
OV
24
P.C.B. 33/44
TP2
ZD4
9V1
R10
220K
R5
10K
2%
A2
R7
470
-19.0
PR1
1K
C3
80μF
16V
Q4
2N5172
-23.0
R8
240
R6
7K5
2%
2
-24.5
TP5
R9
·47Ω
-24.4
Q5
BFY51
-9V
3
TP3
Q6
TIP3055
42/33

S E R V I C E   M A N U A L

Synthi A/VCS3

DK1/2 keyboard

KS sequencer

Compiled by Electronic Music Studios, Trendeal Vean Barn, Ladock, Truro TR2 4NW.

Telephone 0726-883265

CONTENTS:

NOTE:

Transistor types used in cur machines have varied from time to time.

The following types are the most widely used:

NPN sil BC 169C	2N 5172
PNP sil BC 258B	2N 4288
Fast NPN sil ME9002	2N 706
Fet 2N 5163	
Fet 2N 5461	

Diodes:

DK10 - small signal germanium

1N4148 - 1N 914

SYNTHI A ALIGNMENT

Synthi A	Testing Manual Board
1. Power Supply	A
2. Output Channels	A
3. Reverberation	A
4. Envelope Shaper	B
5. Filter Oscillator	B
6. Ring Modulator	B
7. Input Channel Preamplifiers	B
8. Oscillator 1	C
9. Oscillator 2	C
10. Oscillator 3	C
11. Noise Generator	C
12. Meter Amplifier	C

Board A is on the left side as you look at the opened back of the machine. Board B is in the middle, with Board C on the right.

SPECIFICATIONS

Power: 100-130V or 200-250V ac.

Stereophones level: 10V p.p max into 50 ohms

Scope output: 5V p.p max

Signal output: 2V p.p max into 600 ohms

Control output; 15V dc max into 10K ohm

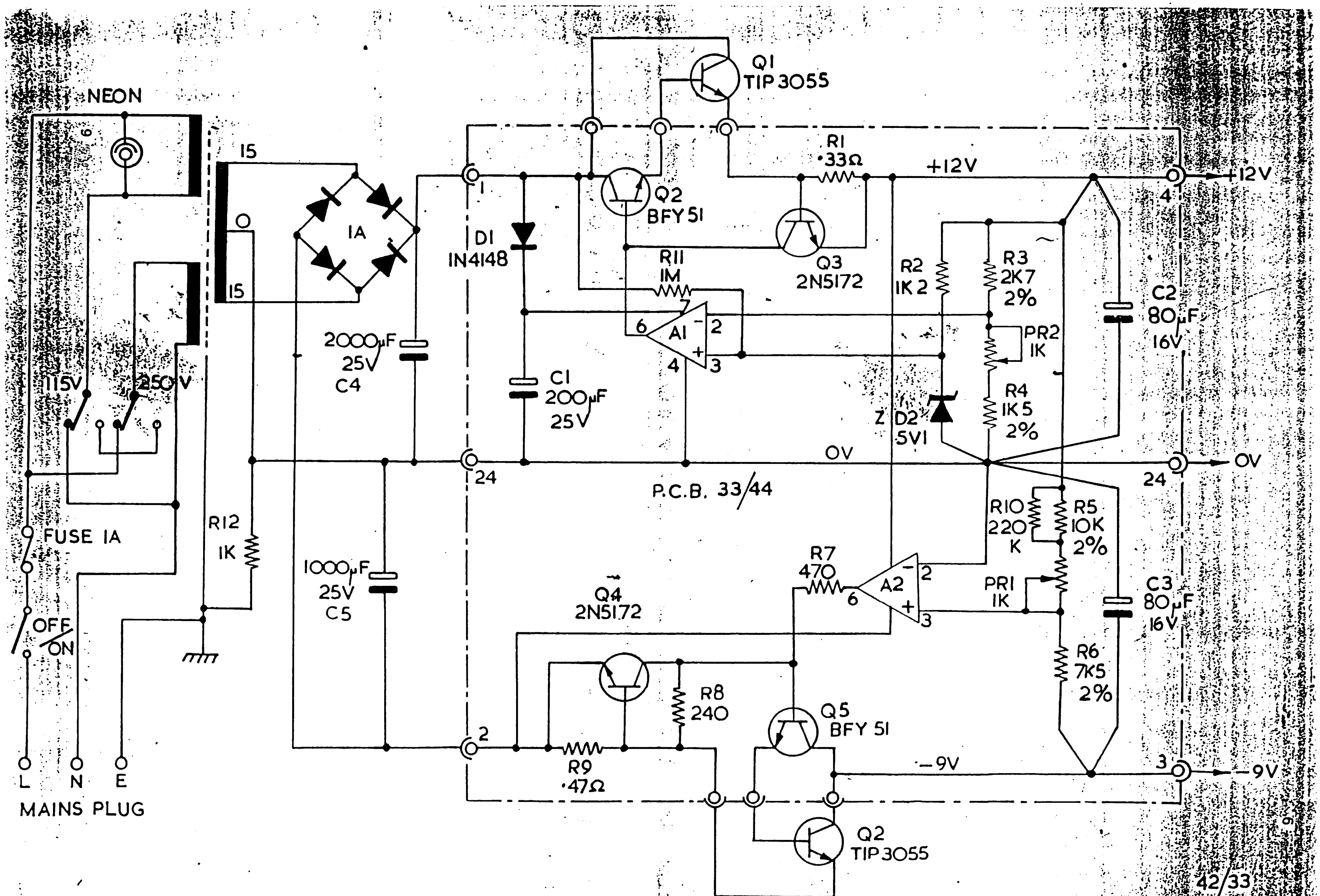
Signal Input; ac - 1.8V p.p into 50K ohm. dc- 2.5V max into 50K ohm.

Microphone Input; 5mV into 600 ohms

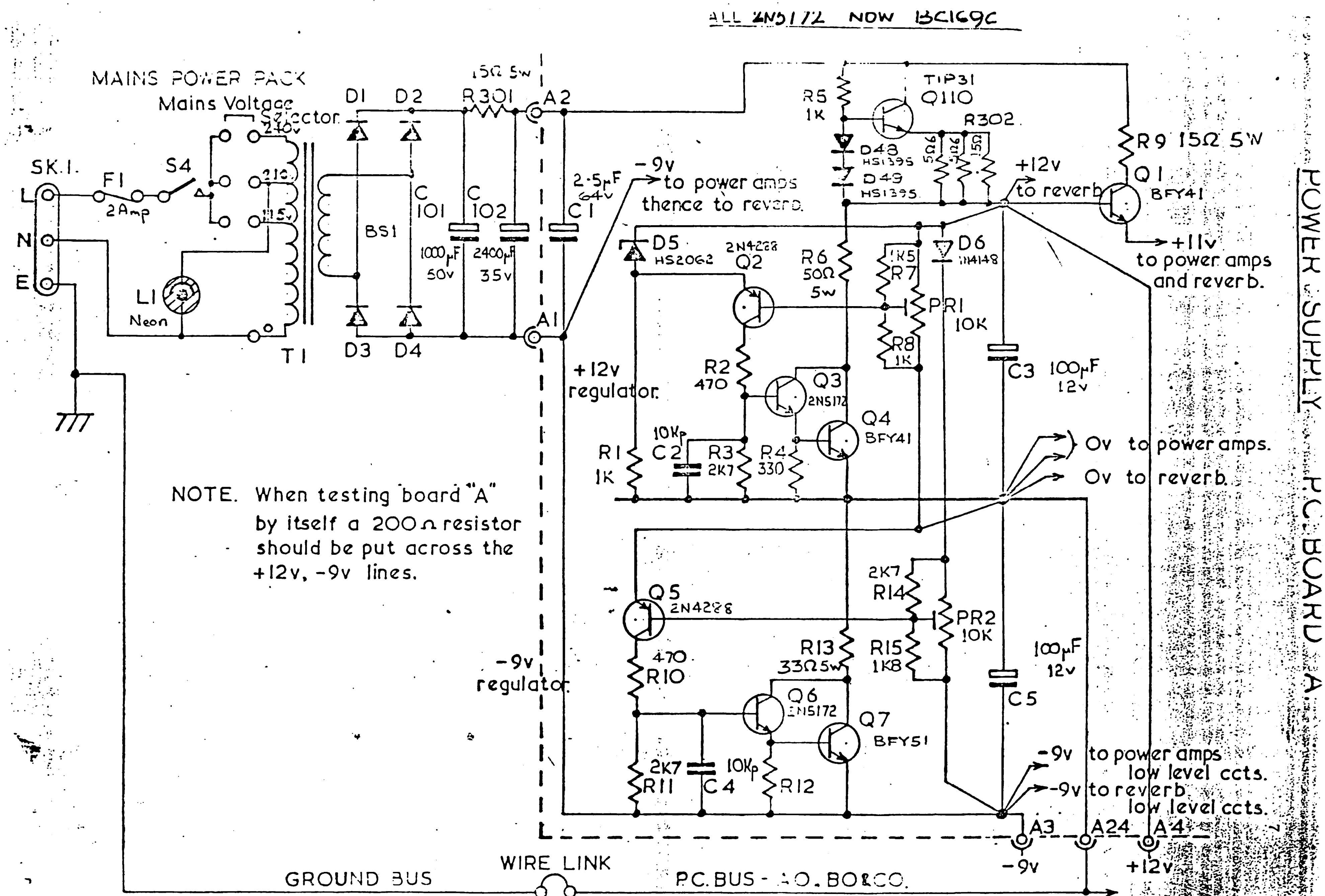
Devices

Oscillator 1	Range: 1Hz-10kHz (on dial) Outputs: Sine 2V p.p (with shape control) Sawtooth 2V p.p Control Sensitivity; 0.32 Volts/Octave
Oscillator 2	Range; 1Hz-10kHz (on dial) Outputs: Triangle/Sawtooth 3V p.p Square/Pulse 2V p.p Control sensitivity; 0.32 Volts/octave
Oscillator 3	Range: 0.02(40"period) - 500Hz(on dial) Outputs: Triangle/Sawtooth 3V p.p Square/Pulse 2V p.p Control Sensitivity: 0.26 Volts/octave
Noise Generator	Level: 3V p.p white and coloured
Filter/Oscillator	Range: 5Hz-10kHz (on dial) Cut-off rate: 18 dB/Octave Q: Variable up to 20 Frequency Control : 0.2Volts/Octave
Ring Modulator	Input level: 1.5V p.p max. Output level: 6V p.p max. Input rejection: -50 dB (with 1.5V p.p input)

Envelope Shaper	Duration: Attack 2ms-1s On 0-2.5s Decay 3ms-15s Off 10ms-5s (+Off position)
	Trapezoid Output: ± 3V dc max.
	Decay Control; 0.4 Volts/octave
Reverberation	Max time: 2s
	Output Level: 5V p.p
	Mix VC : -2V for 0%, +2V for 100% mix
Joystick	Voltage Output: 2 x ±1.5V dc
Meter Input	Control Voltage mode: ±1V dc
	Signal mode: 4V p.p
Input Amplifiers	Sensitivity: 1.8V for High Level Inputs 5mV for Microphone Inputs
Output Amplifiers	Output level: 2V p.p into 600 ohm (panned) 10V p.p into 50 ohm (unpanned) 5V dc into 10K ohm (unpanned) VC level: 15 dB/Volt



POWER SUPPLY CIRCUIT SYNTHI A


ALL 2N5172 NOW BC169C
MAINS POWER PACK
Mains Voltage Selector
240v
210v
115v
SK.1.
L
N
E
F1
2Amp
S4
L1
Neon
T1
D1
D2
D3
D4
BS1
15Ω 5w
R301
C 101
1000μF 50v
C 102
2400μF 35v
A2
A1
C1
2·5μF 64v
-9v
to power amps thence to reverb.
D5
HS2062
2N4288
Q2
R6
50Ω
5w
R5
1K
TIP31
Q110
R302
D48
HS1395
D49
HS1395
5Ω6
5Ω6
15Ω
+12v
to reverb
R9 15Ω 5W
Q1
BFY41
+11v
to power amps and reverb.
D6
1N4148
1K5
R7
PR1
10K
R8
1K
C3
100μF 12v
+12v regulator
R2
470
Q3
2N5172
Q4
BFY41
R1
1K
10Kp
C2
R3
2K7
R4
330
Ov to power amps.
Ov to reverb.
NOTE. When testing board "A" by itself a 200Ω resistor should be put across the +12v, -9v lines.
Q5
2N4288
2K7
R14
PR2
10K
R13
33Ω5w
R15
1K8
100μF 12v
C5
-9v regulator
470
R10
Q6
2N5172
Q7
BFY51
2K7
R11
C4
10Kp
R12
-9v to power amps low level ccts.
-9v to reverb low level ccts.
A3
A24
A4
-9v
+12v
GROUND BUS
WIRE LINK
P.C. BUS - A.O. BO&CO.
POWER SUPPLY P.C. BOARD A.

Power Supply

Before turning on, set PR1 cw and PR2 ccw with only A board plugged-in.
Set PR2 for +12V ± 0.1V
Set PR1 for -9V ± 0.1V
Check PR2 again and reset if necessary
N.B. -9V rail is parasitic on the +12V supply.
Plug in B and C cards and recheck +12V and -9V rails.

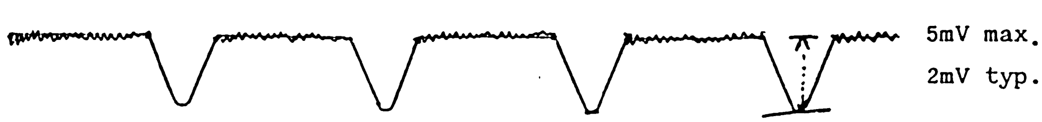
These should not have altered. If they have, suspect either B or C board or poor regulation on A board. Plug-ni keyboard as extra load. +12 and -9 Volt rails should not have moved more than ± 0.1V measured always on the A board. (C board voltage may be 20 mV lower)

Monitor the rails on the scope (5mV/cm). Look for hum and noise. These should be much less than 5mV. Noise, if present, will probably be due to the zener diode.

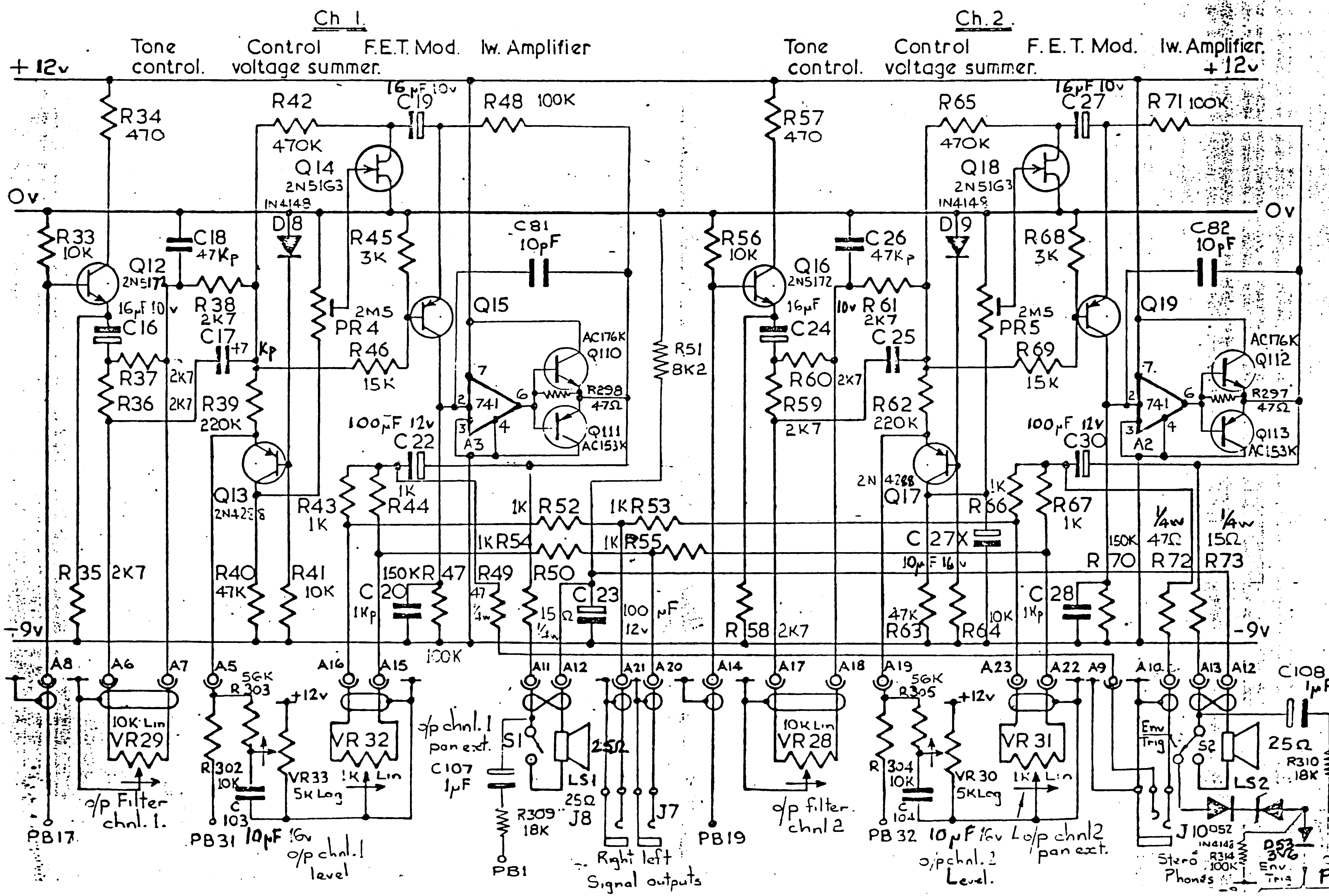
Power supplies should stabilise on full load for specified fluctuations.
110/240 nominal : +10% or -23%
110 nominal : 100V-135V for 125 sufficient
240 V nominal: 200V-260V

Hum can also be checked by the following:
Check Output Filters on 10
Output Controls on 10.0.10.10
Patchboard vacant
Monitor (5mV/cm) on signal output
Load unit with keyboard
100 Hz ripple as shown.
Noise can be seen which should never exceed 10mV p.p. Even with noise level up. With noise level down, the noise on this waveform should be quite low. Zener diode noise will be very obvious.

N.B. A2 normally gets hot, dodgy D1 gives large 100Hz ripple on Output.
Always clean edge-connectors and check clean presets on A board.



ALL 2N5172 NOW BC169C



OUTPUT CHANNEL AMPLIFIERS & P.C. BOARD A

Output Channels

Set Output Channel Filters to 5.
Set Output Level row to 0.0.10.0 and connect traces of scope (5mV/cm) to both signal outputs.

Connect full level ramp signal at 261 Hz from Oscillator 1 to both Outputs. Trim PR4 and PR5 for minimum signal breakthrough. (Maximum 5mv p.p) Replace presets if adjustment is erratic.

Reset Output Channel row controls to 5.0.10.5. Output levels should be around 1V p.p and should be within 20% of each other. Check signal tracking in the same manner for Output settings 4 and 6 as well. If one level is consistently high, pad out resistor across its control pot (R305 = 56K)

Successful tracking will depend on the characteristics of the pots and the correct matching of the FETs Q14 & Q18.

Connect the joystick row via two shorting pins to both VC level inputs. Swing stick up and down to check for 20% level tracking tolerance.(Level pots should be at zero). Inaccuracies in stick tracking may be adjusted by altering the value of R302 or R304 (10K) which are mounted under the patchboard rear.

Check correct operation of Pan controls, which only affect the Signal Outputs. Check also the Output Filters. Use noise as a good source.

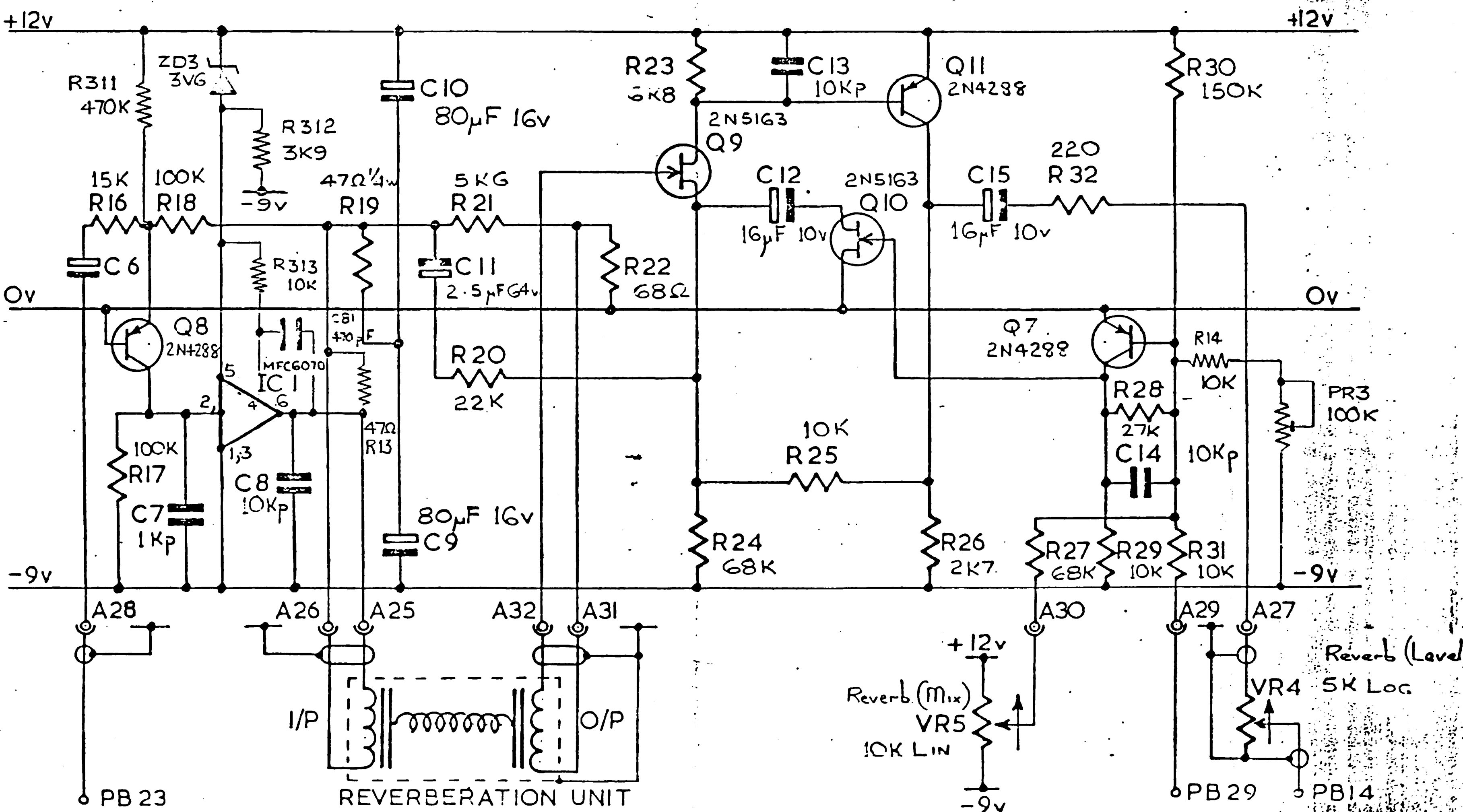
Check for max. outputs on the Signal Output socket of at least 2.5V p.p before the onset of clipping. Level controls should be at about 6. Check headphone signal is good. Check for instability of Output Amps by driving hard with low frequency. (Oscillator 3 square wave). The level control of the channel NOT beirg driven should be on zero. Monitor the two signal outputs. The undriven channel will show breakthrough. Plug in headphones and check for oscillation. Reduce drive to Output Channel 2. Keep checking for oscillation. Then repeat for other Output Channel.

N.B. DC offset across loudspeaker is 1.8V ± 10%.

ALL 2N5172 NOW BC16?

Hi-Zo drive amplifier.

Pick-up amplifier & voltage controlled mixer.



Reverberation

Set PR3 fully clockwise before operating. Feed large amplitude tone bursts into reverb. Adjust PR3 so that the output is dry at Mix setting of zero and reverberation progressively increases from setting of 2.

Maximum dryness on the Mix control should be no worse than that obtained with the VC Mix input row on the patchboard grounded.

Check voltage control of Mix with the joystick.

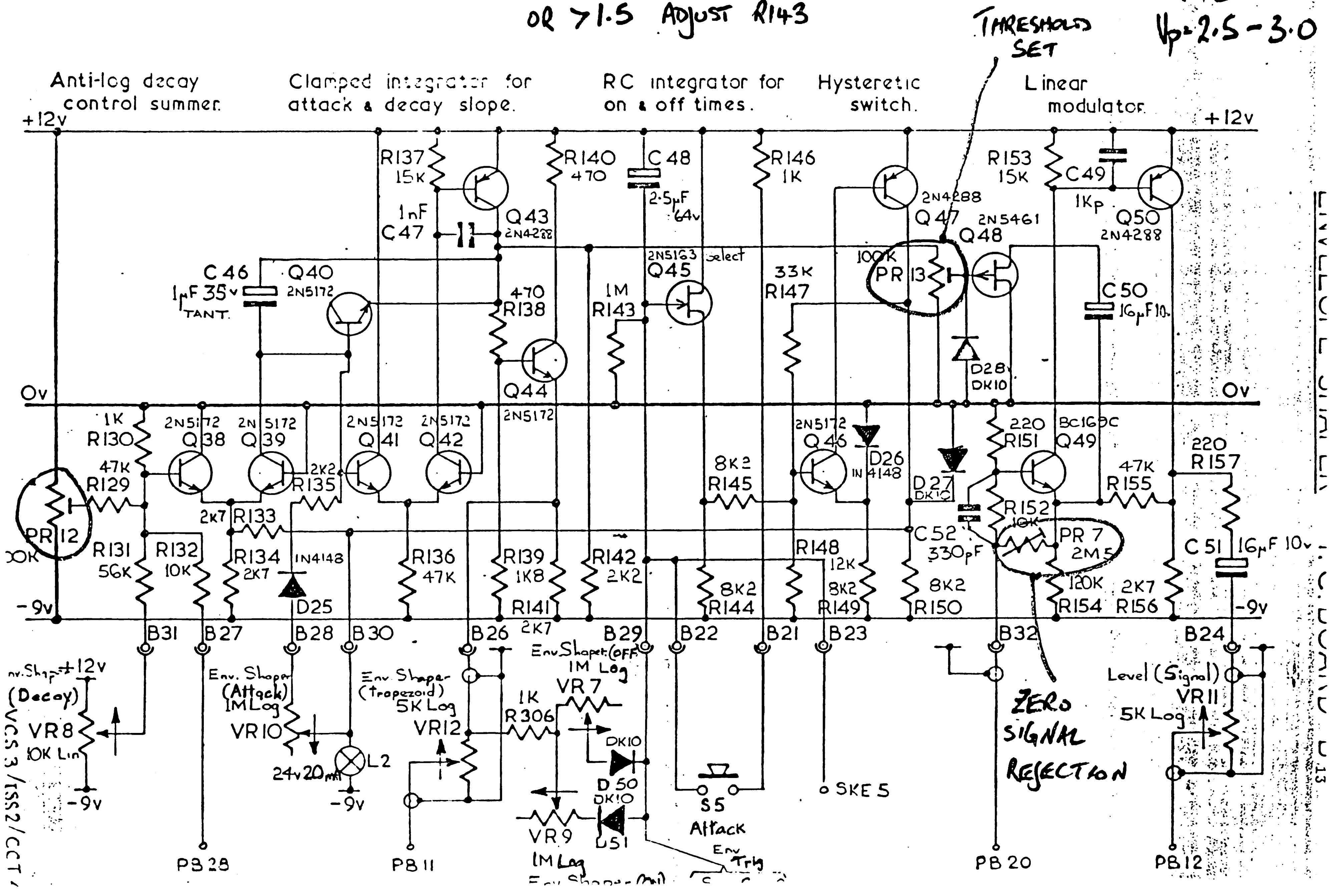
Hold input amplitude constant and sweep frequency of tone. Check for rattles, buzzes or abnormal resonances in the spring. Check spring is correct way round. If Mix control is wrong change Q10.

N.B. Reverb amplifier should clip symmetrically.

Q45 3.5-4.0 OR >1.5 ADJUST R143

ALL 2N5172 NOW BC169C

Q48 Vp=2.5-3.0



Envelope Shaper

Put scope on 2V/cm and connect to Trapezoid output. With envelope controls at 0.0.0.0. Adjust PR12 so that frequency of trapezoid oscillation is about 90% of the maximum possible frequency. Connect Filter output on 261 Hz (Frequency setting 5) with maximum output to Envelope Input. Monitor Envelope output. Set PR13 clockwise.

Set envelope controls 0.0.0.10. Adjust PR7 for minimum signal. Adjust PR13 until signal reappears, then back off slightly. The final envelope shaper signal breakthrough should be 5 mV or less p.p. With the Attack button pressed the output signal should be greater or the same as the input signal.

Set controls 0.10.0.10. this gives maximum On time. Press Attack button which should recycle the envelope shaper and lamp should come On, staying on for about 5 seconds. (absolute minimum 4 seconds). This corresponds to an automatic recycle On time of 2.5 seconds which is the minimum spec. (On time is always shorter if recycled automatically). On time is controlled by R148 in conjunction with Q45.

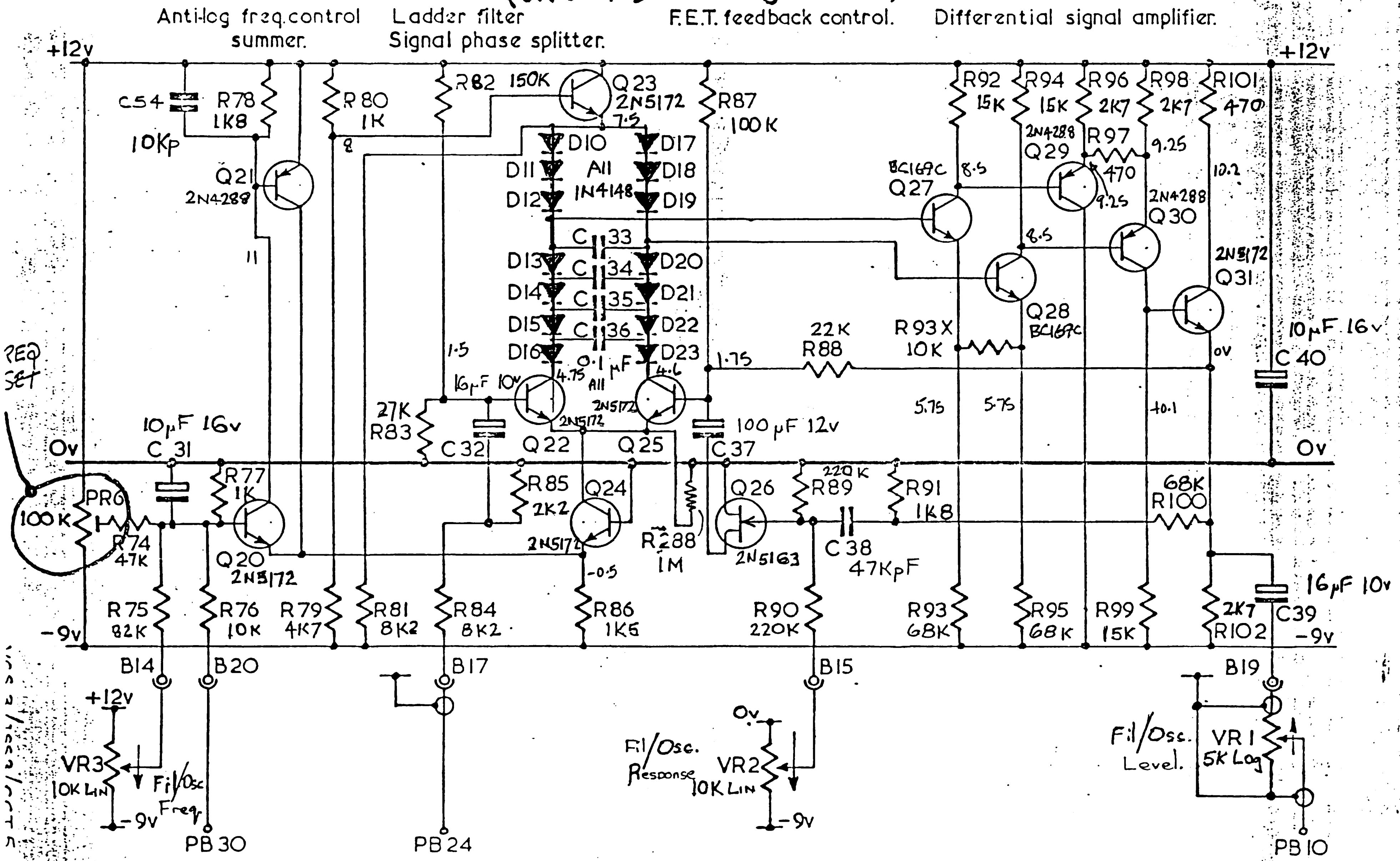
Set controls 0.0.10.5. Press Attack button and time the Decay time. This should exceed 15 seconds, and the envelope shaper must automatically recycle at the end of the decay.

Set controls 0.0.0.7 to 10. Envelope shaper must not recycle with the Off time on 10, so check it doesn't on 7 or so, which will indicate the behaviour on 10. Check input breakthrough at the same time, and adjust PR7 again if necessary.

On and Off times are controlled by R148 (range 10-18K). If On time is infinite at 10, reduce R148, if Off time infinite, increase R148. The value of Vp for Q45 (3.5 - 4.0 nominal) is critical. Failure here upsets recycling. Also leaky C48 or dodgy envelope trigger components .

Q26 2.5 - 3.5
(or > 1.5 and adjust R89)

2.5 - 3.0 RED
3.5 - 4.0 ORANGE



Voltages measured @ osc 250c/s Avo 25v D.C.

Filter/Oscillator

With Response on 10, level full and Frequency on 5, check for oscillation. About 1.5V p.p should be obtained. The shape should be reasonably sinusoidal especially when only just oscillating (on Response control).

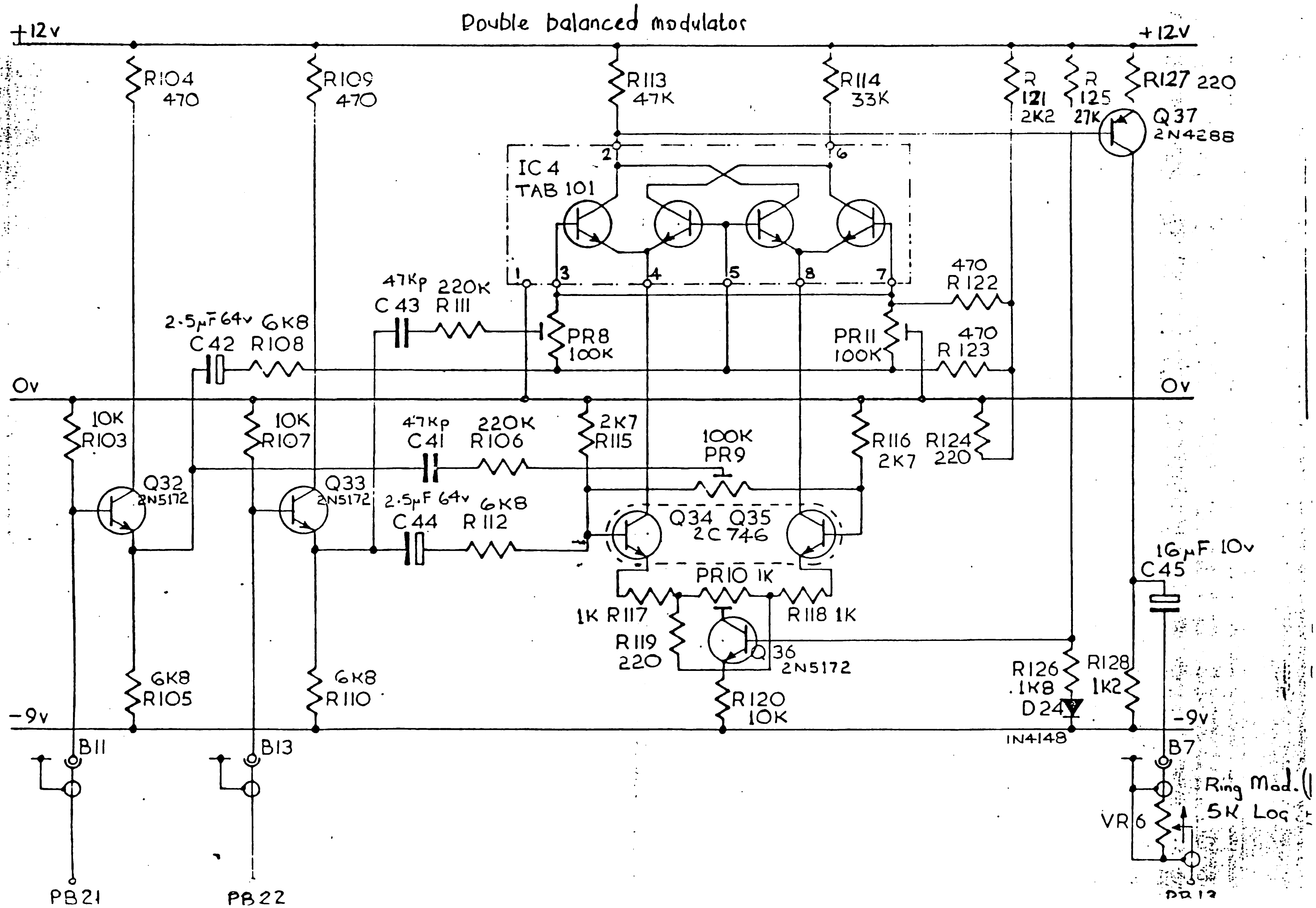
Distortion should be eliminated either by diode bridging or by replacement of offending diode. Bad diodes can be detected by applying the tip of a soldering iron quickly to the diode body. Allow enough time for the diode to cool down before moving on to the next one.

Response control should make the filter oscillate only above 5 for all frequency settings. If this does not occur correctly, adjust R90 or suspect wrong Vp FET. Frequency range on the Frequency knob should be roughly 10Hz to 12kHz. If oscillations stop at one extremity of Frequency pot increase R75. Adjust PR6 for oscillation frequency of 261Hz with F on 5. Noise level of Filter output signal with Response set below point of Osc should be below 5mV p.p.

Check correct filtering using square wave input with swept F.

Intermittent noise: Try soldering iron tip on diodes.
R288 = 1 megohm stops Filter latching-up.

A : 2N5172 NOW BC169C



Ring Modulator

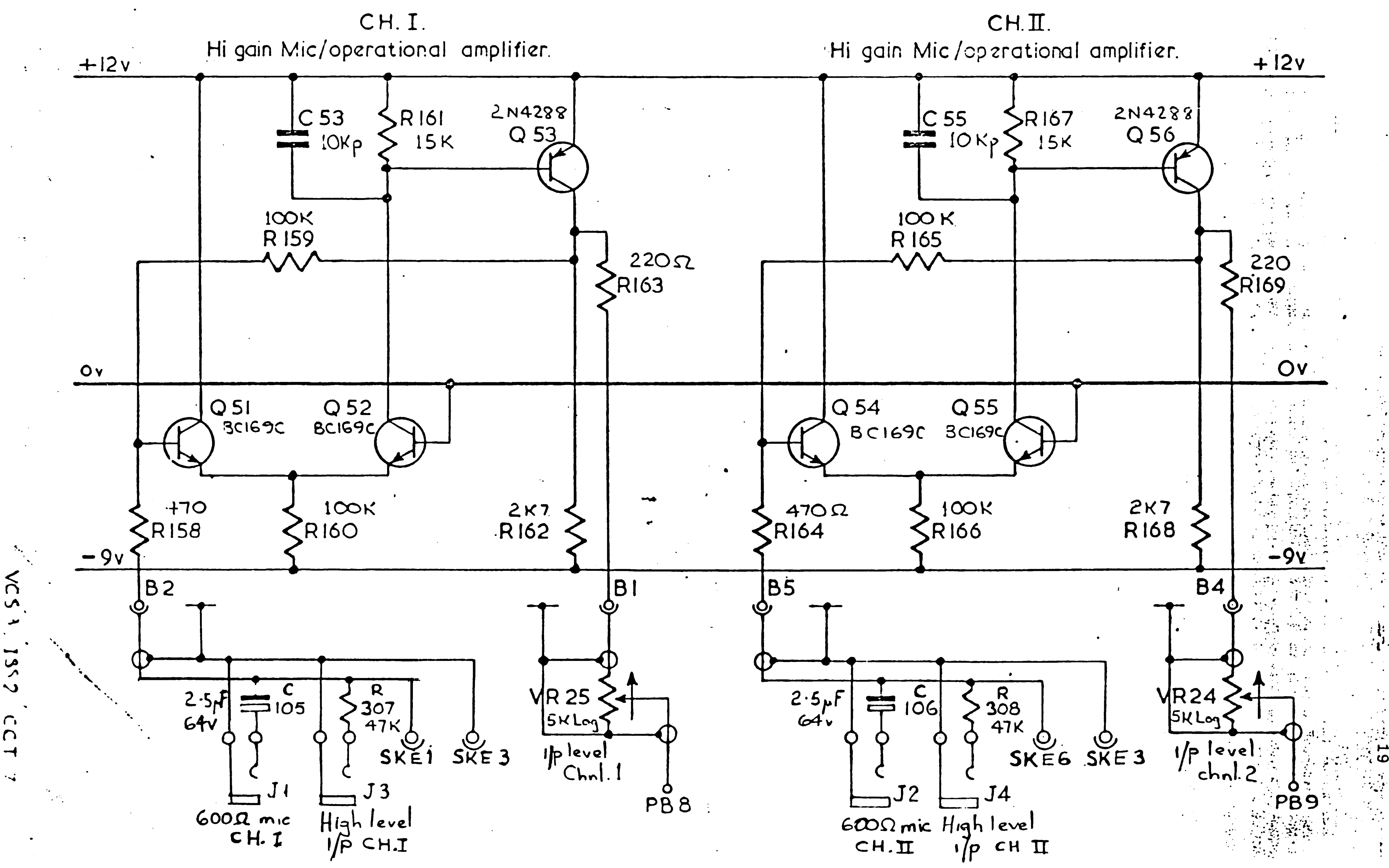
Use filter sinewave output, F on 5. Maximum response, maximum level into both inputs of ring modulator. Ring Modulator level maximum. Check output is double frequency of input, and at least as big. Remove pin to Input B. Drive input A and adjust presets for minimum breakthrough. (PR9 - second harmonic rejection, PR10 - fundamental rejection).

Drive Input B by removing pin to Input A and reinserting pin for input B. Trim presets for rejection. (PR8 - second harmonic, PR11 for fundamental). This one should NOT drift. Input A drifts quite a bit and should ideally be adjusted with the back on the machine after it has fully warmed-up. If this is not possible ensure that Input B is used for the continuous signal to minimise breakthrough.

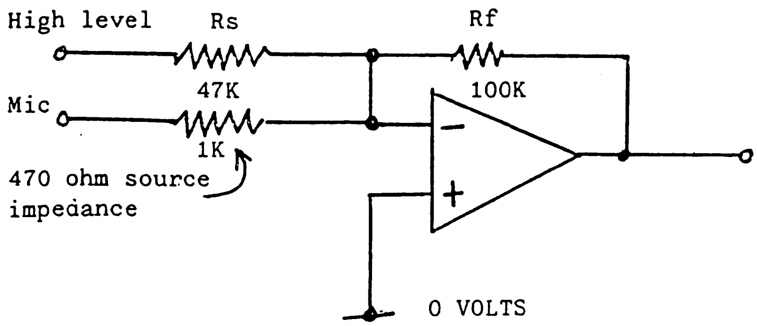
With an input level of 1.5V p.p up to 10mV p.p maximum is allowed for breakthrough. This gives about 60 dB rejection.

If higher harmonics are a problem, then filter signal must be too impure. Try backing off response, or use an external signal generator. 1.5V p.p at 261 Hz.

If reasonable rejection is unobtainable, change matched pair BC169C or TAB101 where appropriate. 2C746 used on later models. Do not bridge with resistors. Replace presets if adjustment is erratic.


CH. I.
Hi gain Mic/operational amplifier.
CH. II.
Hi gain Mic/operational amplifier.
+12v
0v
-9v
C 53 10Kp
R161 15K
2N4288 Q 53
100K R 159
220Ω R163
Q 51 BC169C
Q 52 BC169C
470 R158
100K R160
2K7 R162
B2
B1
2.5μF 64v
C 105
R 307 47K
SKE1
SKE 3
VR 25 5K Log
I/P level Chnl. 1
PB8
J1 600Ω mic CH. I
J3 High level I/P CH.I
C 55 10Kp
R167 15K
2N4288 Q 56
100 K R 165
220 R169
Q 54 BC169C
Q 55 BC169C
470Ω R164
100K R166
2K7 R168
B5
B4
2.5μF 64v
C 106
R 308 47K
SKE6
SKE 3
VR24 5K Log
I/P level chnl. 2
PB9
J2 600Ω mic CH. II
J4 High level I/P CH II

Input Channel Amplifiers



Inverting Operational amplifier

DC gain = $\frac{Rf}{Rs}$

High level gain = 2

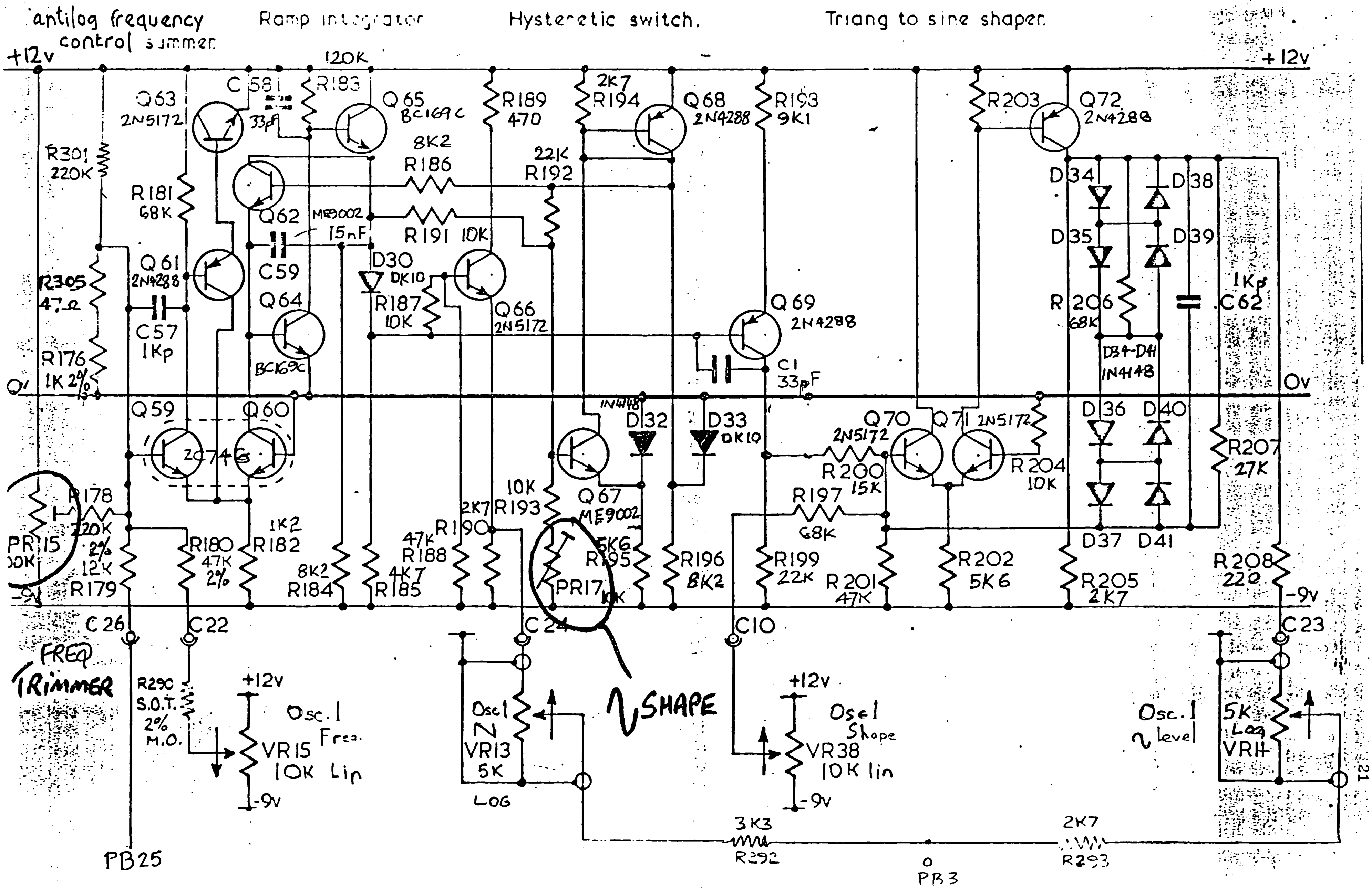
Microphone gain = 100

Using a signal generator check the two inputs for the expected gains. This is best done by monitoring the control output with shorting pin. High level gain can be checked by applying about 2V p.p and looking for 4V at the output.

Low level (microphone) gain : 50mV should give 5V p.p.

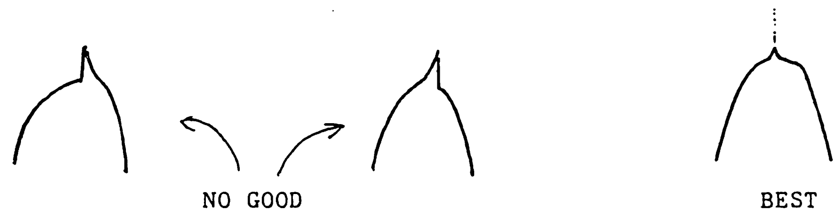
Check for minimal DC offset by plugging input channel inot the meter switched to Control Voltages, and then rotating the input level pot. No more than ± ½ a division movement should occur. (approx 200mV).

Pay special attention to condition of pot tracks.


antilog frequency control summer
Ramp integrator
Hysteretic switch.
Triang to sine shaper.
+12v
0v
-9v
Q63 2N5172
C58 33pF
R183 120K
Q65 BC169C
R189 470
R194 2K7
Q68 2N4288
R198 9K1
R203
Q72 2N4288
R301 220K
R181 68K
R186 8K2
R192 22K
Q62 ME9002
C59 15nF
R191 10K
D30 DK10
R187 10K
Q66 2N5172
Q61 2N4288
R305 47Ω
C57 1Kp
Q64 BC169C
R176 1K 2%
Q69 2N4288
C1 33pF
D34
D35
D38
D39
R206 68K
D34-D41 1N4148
C62 1Kp
Q59
Q60
2C746
D32 1N4148
D33 DK10
Q70 2N5172
Q71 2N5172
R204 10K
R200 15K
R197 68K
D36
D40
D37
D41
R207 27K
PR115
R178 220K 2%
R179 12K
R180 47K 2%
R182 1K2
R184 8K2
R185 4K7
R188 47K
R190 2K7
R193 10K
Q67 ME9002
PR17 10K
R195 5K6
R196 8K2
R199 22K
R201 47K
R202 5K6
R205 2K7
R208 220
C26
C22
C24
C10
C23
FREQ TRIMMER
R290 S.O.T. 2% M.O.
Osc.1 Freq.
VR15 10K Lin
Osc1 VR13 5K LOG
SHAPE
Osc1 Shape
VR38 10K lin
Osc.1 level
5K Log VR11
3K3 R292
2K7 R293
PB25
PB3

Oscillator 1

The first operation is to adjust the shape of the sinewave, since the adjustment affects frequency. Using the vernier control and PR15 if necessary, obtain an output of 400Hz. Turn the ramp down and adjust the sine shape control for the best sine shape. Trim PR17 to balance out the spike on the peak of the sinewave. This may best be seen by expanding the X and Y inputs on the scope.



The best position is shown, where the small spike is triangular and balanced. A small thin spike may also appear but is not important.

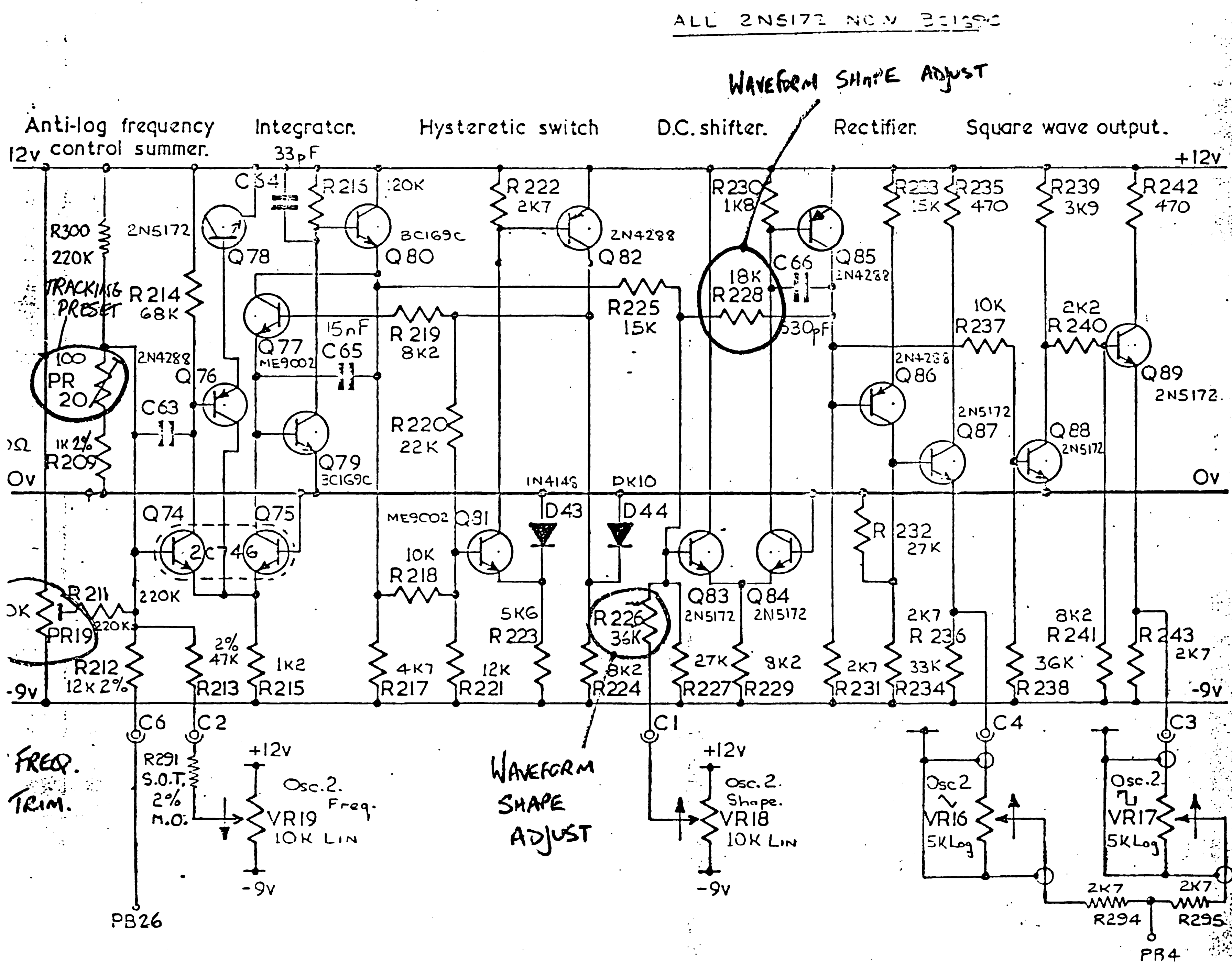
Test the main shape control. A good sinewave should be acheived on 5. (±½ division). If further out, R197 or R201 may need to be adjusted.

Set PR16 halfway and leave it alone. Set frequency vernier dial to 6 and adjust PR15 for 261Hz. Rotate vernier to 8 and check for 2088Hz. Absolute mazimum error ± 1 division. For fudge procedure, see Osc 2 writeup.

Sine Output should be around 1.5V p.p
Ramp Output should be around 1.5V p.p

N.B. Ramp shape is not controllable.

Pitch characteristic is 0.32 Volts/Octave.



R227 was 15K NOV. 2.8.72

OSCILLATOR 2 P.C. BOARD C.

Oscillator 2

Set square level to zero, ramp at maximum. Set PR20 halfway. Vernier on 6. Trim PR19 for 261Hz. Increase vernier to 8. Check frequency is about 2088Hz. If beyond spec then R291 SOT will have to be added in the range 8-22K. Check that 10 on vernier dial gives at least 10kHz.
If vernier dial at 8 gives less than 2088Hz then short circuit R291 and R213 will have to be reduced. These should be 2% resistors.
Shape controls should operate identically to those on Osc 3 (see next page) except that levels are reduced, and the two outputs are summed into the patchboard on Mark 11 machines. Remember to turn down unwanted signal.
Resistors R226 and R228 are the relevant ones to set the shape.
Pulse level should be 2V p.p. Ramp level should be 3.5V.
N.B. Osc2 and 3 waveforms are not symmetrical with respect to zero volts.

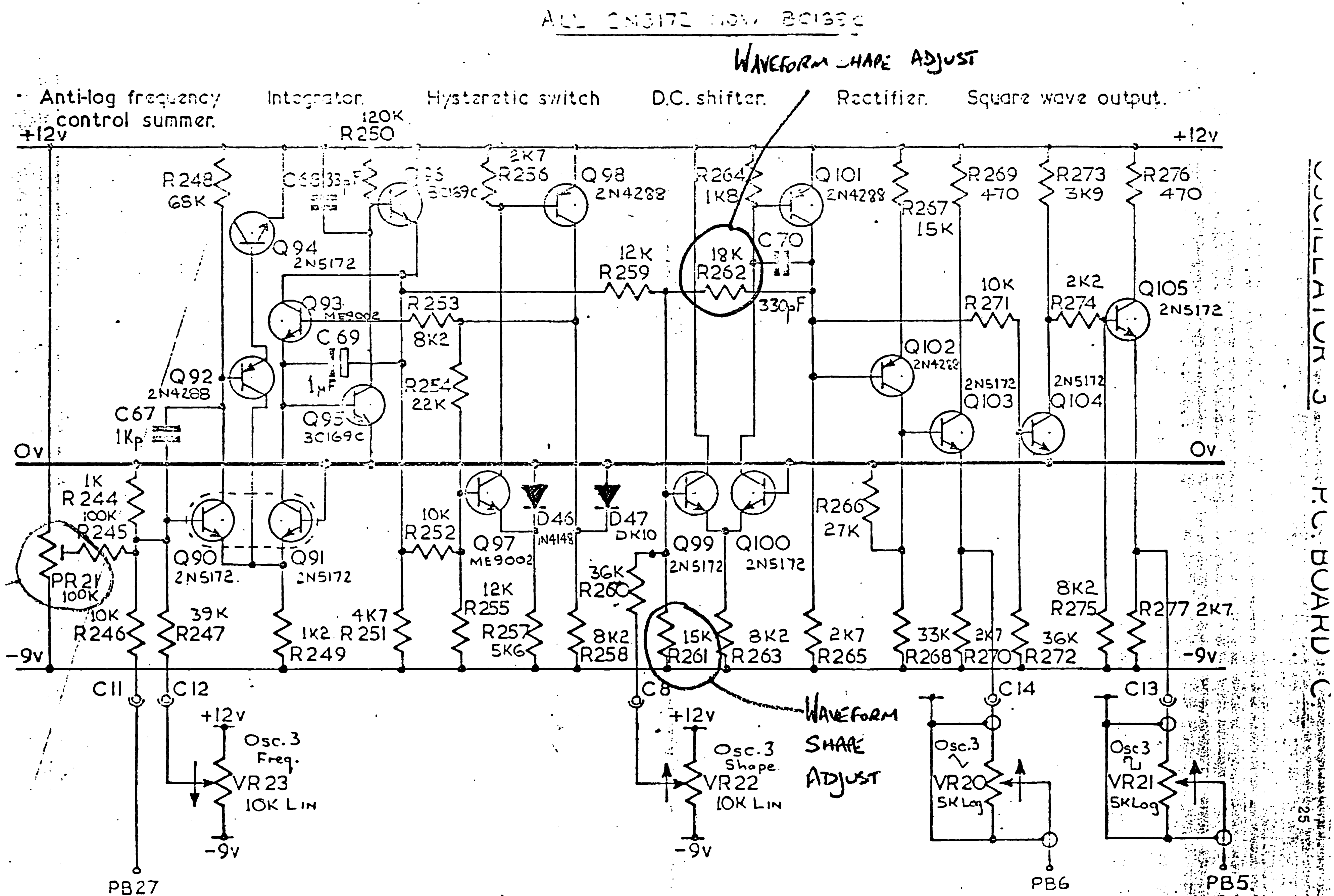
Tracking

Mix Osc 1 and Osc 2 ramp outputs into Output Channel 1. Use PR20 only to trim the tracking of Osc 1 and Osc 2. Using the joystick on max with range control to limit frequency range. Set both verniers to 6 and tune for zero beats. Advance the joystick range control which will increase both frequencies until the beats begin. Trim PR20 to zero beats, and remember which way you turned it. (N.B. The preset is a very fine adjustment, and when the tracking is nearly right it will be necessary to make very very small movements). Having trimmed PR20, turn the range control back to zero, readjust one of the verniers near 6 to give zero beats and then advance range control of joystick to where it was before. If beats are faster you know you turned the preset the wrong way. Repeat procedure until tracking goes to about 2kHz. Ideally a test 'back' should now be fitted and a final adjustment made after another 10 minutes have elapsed.

Faults

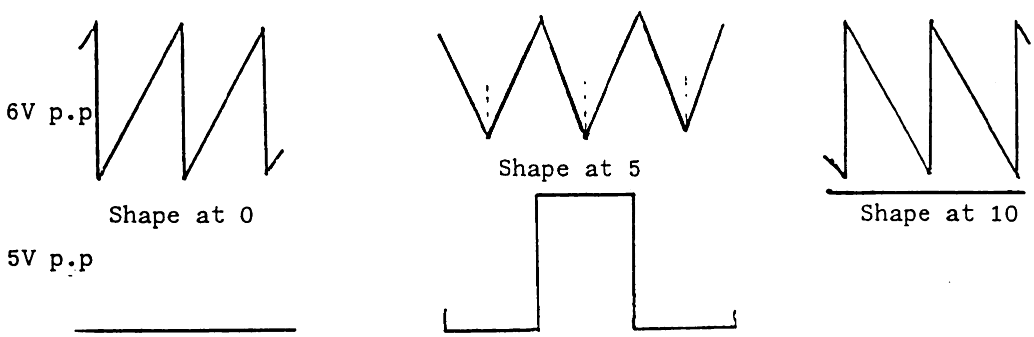
Tracking from 261Hz to about 2kHz should be achieved with a maximum of 3 beats per second on the way. A curved Voltage/Frequency response may occur where zero beats are produced in more than one place. This is due to a mismatch in the matched pair transistors (Q74 & Q75 for Osc 2). Fit a new transistor here or in Osc 1.

N.B. Always use specially matched 2K7 pins for tracking tests.


WAVEFORM SHAPE ADJUST
Anti-log frequency control summer.
Integrator.
Hysteretic switch
D.C. shifter.
Rectifier.
Square wave output.
+12v
0v
-9v
R248 68K
C68 33pF
R250 120K
Q96 BC169C
R256 2K7
Q98 2N4288
R264 1K8
Q101 2N4288
R267 15K
R269 470
R273 3K9
R276 470
Q94 2N5172
Q93 ME9002
C69 1μF
Q92 2N4288
Q95 BC169C
C67 1Kp
R253 8K2
R254 22K
R259 12K
R262 18K
C70 330pF
R271 10K
R274 2K2
Q105 2N5172
Q102 2N4288
Q103 2N5172
Q104 2N5172
R244 1K
R245 100K
PR21 100K
Q90 2N5172
Q91 2N5172
R252 10K
Q97 ME9002
D46 1N4148
D47 DK10
Q99 2N5172
Q100 2N5172
R266 27K
R260 36K
R246 10K
R247 39K
R249 1K2
R251 4K7
R255 12K
R257 5K6
R258 8K2
R261 15K
R263 8K2
R265 2K7
R268 33K
R270 2K7
R272 36K
R275 8K2
R277 2K7
C11
C12
C8
C14
C13
Osc. 3 Freq.
VR23 10K LIN
Osc. 3 Shape
VR22 10K LIN
Osc. 3
VR20 5K Log
VR21 5K Log
PB27
PB6
PB5
OSCILLATOR 3 P.C. BOARD C

Oscillator 3

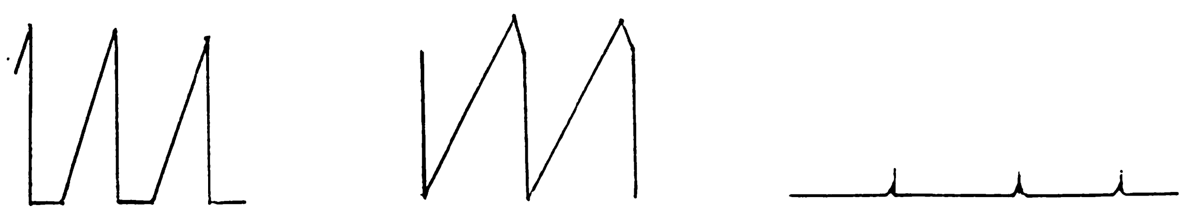
Check frequency control pot for even change in frequency.
Adjust PR21 so that when the vernier is at 8 the frequency is 63Hz.
Note: Vernier 10 should give 500Hz. Period at 0 should be greater than 20 sec.
Adjust values of R261 & R262 with pad resistors to achieve correct shapes of waveforms as shown below:



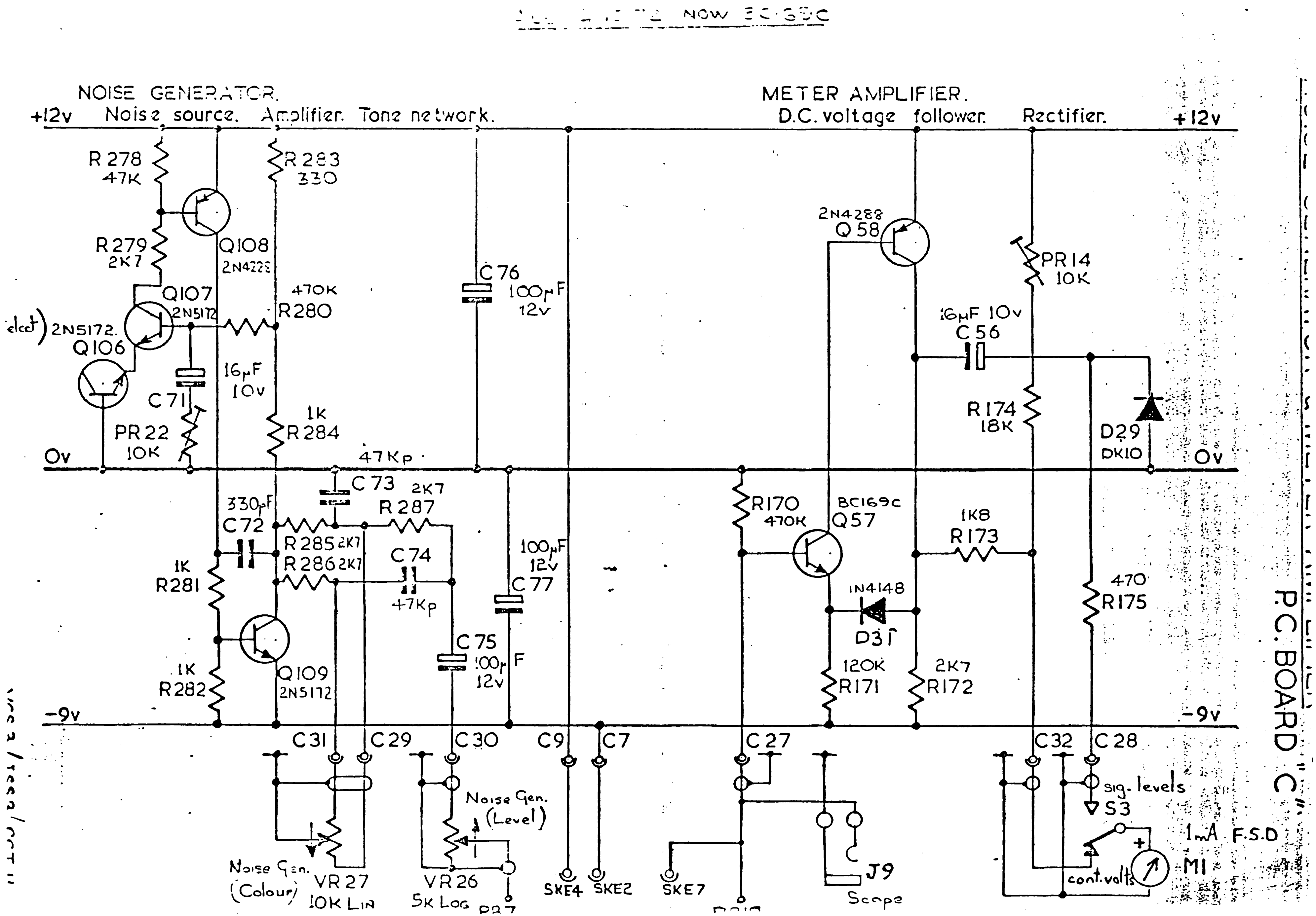
Triangle and square wave should occur on 5. Maximum of ½ division error allowed.
Check Voltage control input.

Faults

Osc 3 breaks through to Osc 2 and to a lesser extent Osc 1. Effect dependent on Osc 3 shape control setting. Triangle was 'furry', with 10mHz oscillations visible all over C board. Strongest near Q101. Cause: instability in Q99. Q100, Q101. Cure, C70 330pF change to 1nF.



Ramp defects   Ramp defects   Pulse defects at 0 and 1



NOISE GENERATOR.
+12v Noise source. Amplifier. Tone network.
METER AMPLIFIER.
D.C. voltage follower. Rectifier. +12v
R 278 47K
R 283 330
R 279 2K7
Q108 2N4228
Q107 2N5172
2N5172.
Q106
470K R280
C71
16μF 10v
PR22 10K
1K R284
C76 100μF 12v
47Kp
Ov
C73
2K7 R287
330pF C72
R285 2K7
R286 2K7
C74 47Kp
1K R281
1K R282
Q109 2N5172
C75 100μF 12v
100μF 12v C77
-9v
C31 C29 C30 C9 C7 C27 C32 C28
Noise Gen. (Level)
Noise Gen. (Colour)
VR27 10K Lin
VR26 5K Log
SKE4 SKE2 SKE7
J9 Scope
2N4288 Q58
PR14 10K
16μF 10v C56
R174 18K
D29 DK10
R170 470K
BC169C Q57
1K8 R173
470 R175
1N4148 D31
120K R171
2K7 R172
sig. levels S3
cont. volts
1mA F.S.D M1
P.C. BOARD "C"

Noise Generator & Meter Amplifier

Colour control on 5, max output. Select a noise diode which gives wideband noise and can be adjusted to give 3V p.p with PR22 roughly midway (to give some later adjustment margin).
Lumpy or crackly sounding noise diodes should be rejected.

Meter

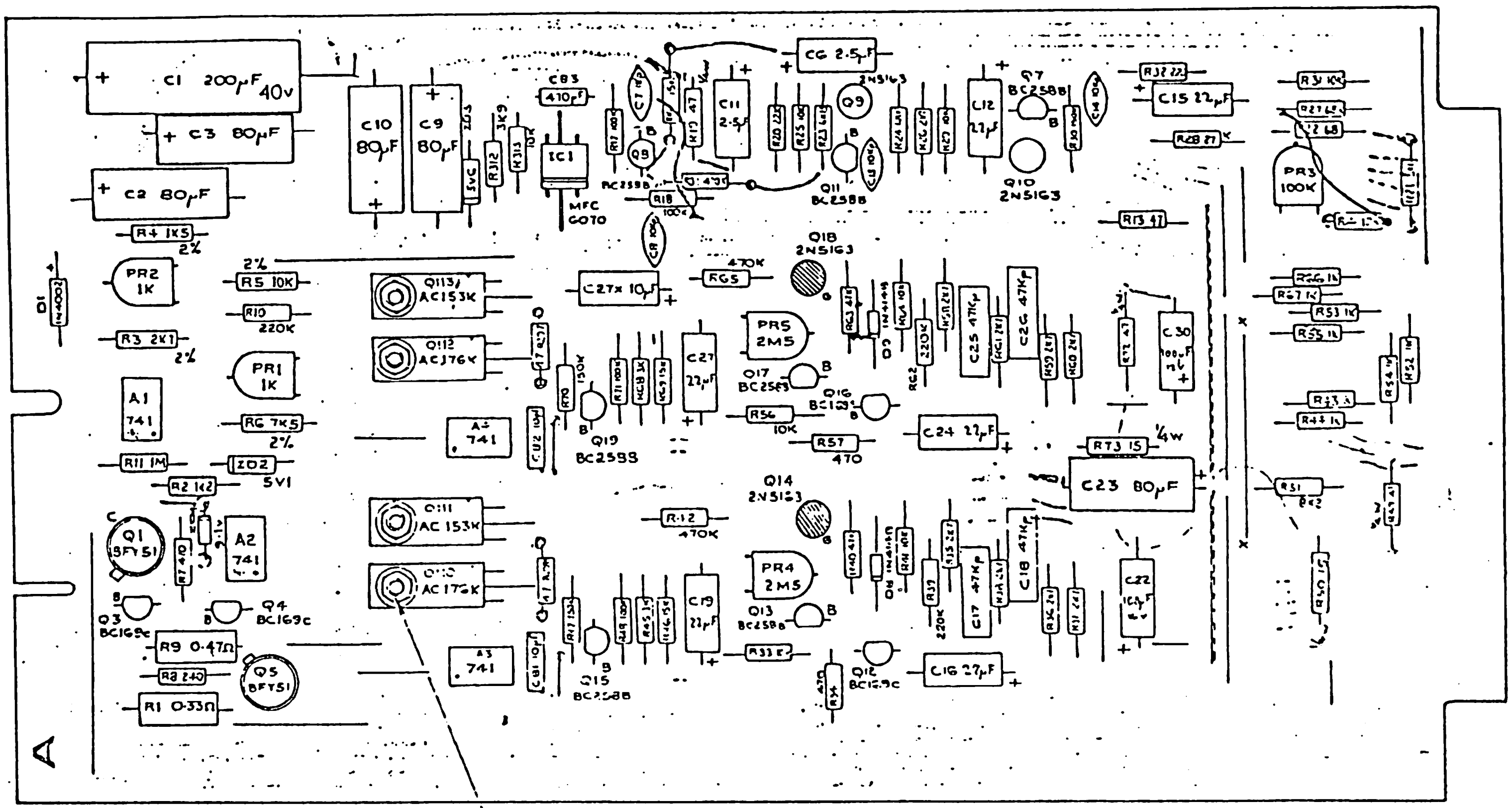
Check left hand zero of meter with machine off or switched to Signals.
Switch to Control Voltages and adjust PR14 for accurate centre zero.
Switch the meter switch a few times and recheck zero again.
Patch the joystick to Meter for swings in both + and - directions.

Check for needle sticking at either end of travel. Switch to Signals and test with Osc 2 sawtooth at max level. Vary level to check proportionality.

Faults

Watch out for the resistor R170 on the C board, which often touches the -ve end of C76, and has been known to produce curious failures on soak test.

NOTE! Q14 & Q18 MATCHED FOR V_p & I_{DSS}



TIP3055 Q2 E B C

Q6 C B E

Mounting Pads to be used on Q1 & Q5 TO5 type.

* + GBA - ½ C.H (or SIM) + FULL NUT & S PROOF

32, 31 > Reverb o/p
30 VR3 (W)
29 PB29
28 PB23
27 VR1
26, 25 > Reverb i/p
24 0V
23 VR31
22 VR31
21 J7 (F)
20 J7
19 PB32
18 VR28
17 VR28
16 VR32
15 VR32
14 PB19
13 LS2
12 LS1 & LS2
11 LS1
10 J10R
9 J10T
8 PB18
7 VR29
6 VR29
5 PB31
4 +12V OUT
3 -9V OUT
2 - D.C. IN
1 + D.C. IN

G. C.N. 82 & ...
F. NOTES 1-5 ADDED ...
E. C.N. 23 ...
C.N. 44
D. C.N. 33 ...
C. ...

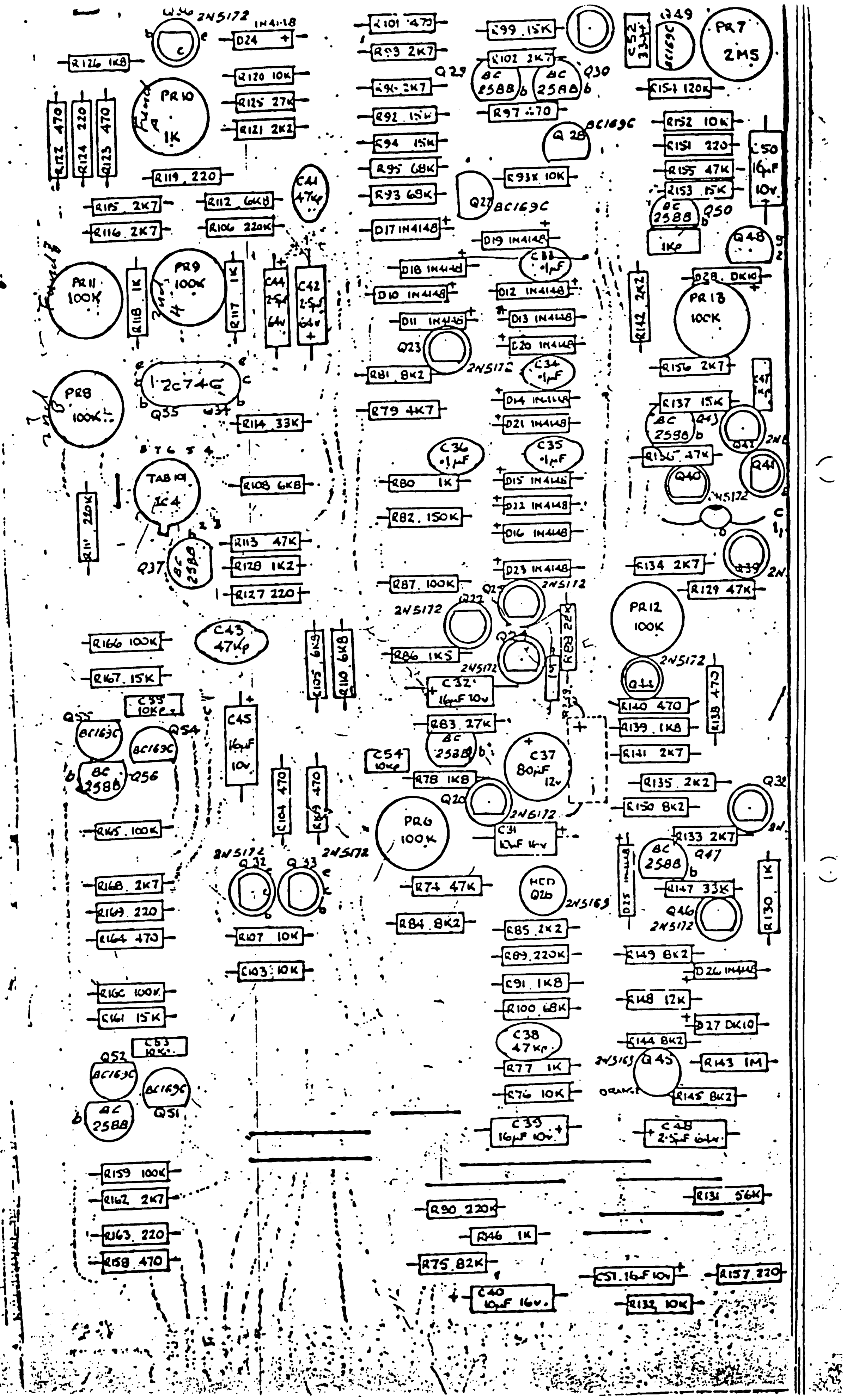
HILTON ELECT...

TITLE 'A' BOARD SYNTHI AKS

* A... ... TYPE PREFERRED

NOTES: 1. C1 SHOWN AS 25V ON BOARD
2. R34 VALUE I.E. 470 NOT SHOWN ON BOARD
3. LINK BETWEEN POINTS X-X NOT SHOWN ON BOARD.
4. POS. NOT SHOWN ON C16.
5. C17, 19, 16, 19, 22, 24, 27, 30 SHOWN AS 16μF ON BOARD.

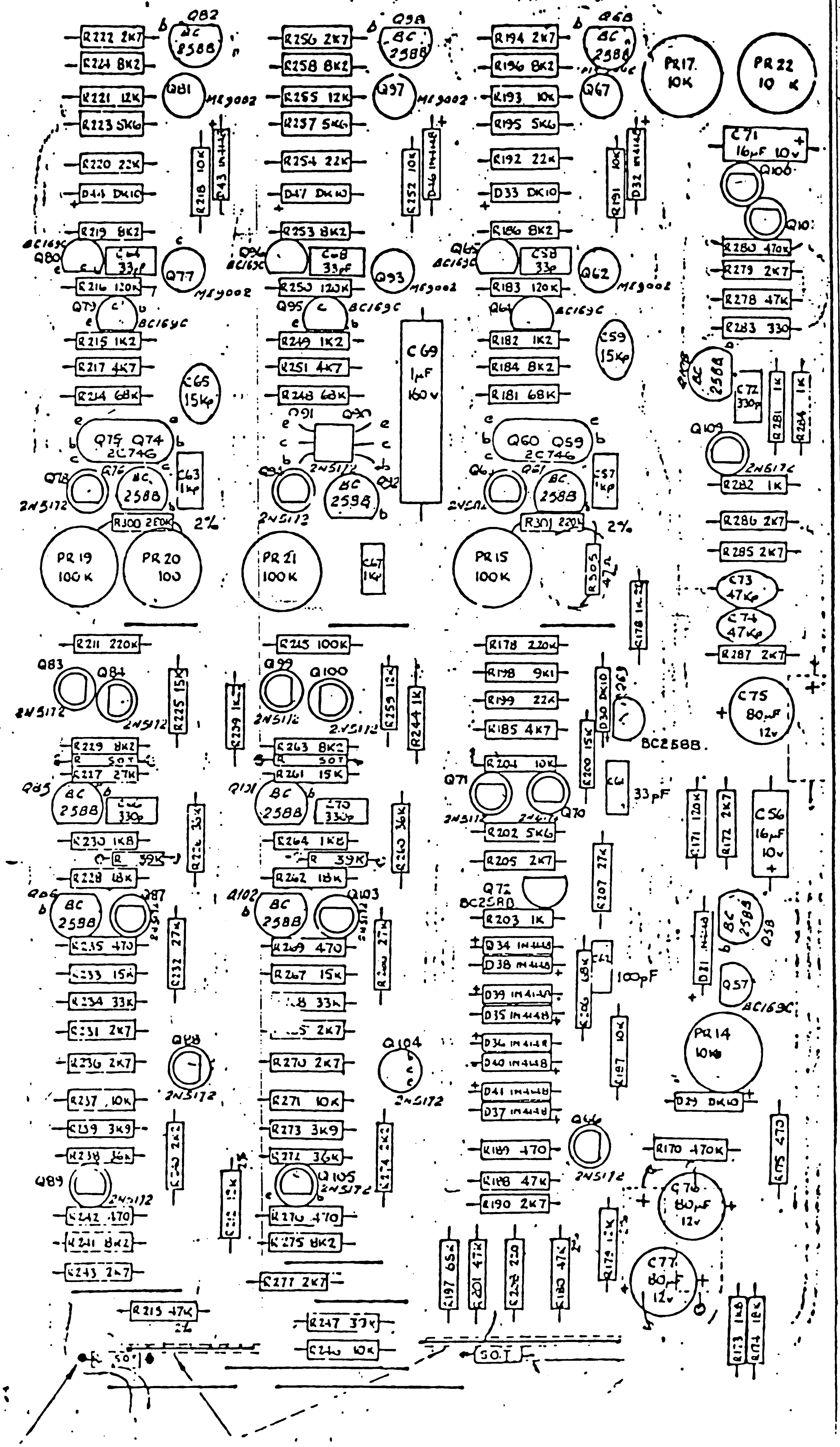
DRG NO 4.3 ...



2N5172
IN4148
D24
R126 1K8
R120 10K
R125 27K
R121 2K2
PR10 1K
R122 470
R124 220
R123 470
R119 220
R115 2K7
R116 2K7
R112 6K8
R106 220K
C41 47kp
PR11 100K
R118 1K
PR9 100K
R117 1K
C44 25uF 64v
C42 2.5uF 64v
PR8 100K
2c746
Q35
R114 33K
TAB101 1C4
R111 220K
R108 6K8
R113 47K
R128 1K2
R127 220
Q37
BC 258B
R166 100K
C43 47kp
R167 15K
R105 6K8
R110 6K8
C55 10Kp
Q55
BC169C
Q54
Q56
C45 16uF 10v
C104 470
R165 100K
Q32
Q33
R168 2K7
R169 220
R164 470
R107 10K
C103 10K
R160 100K
R161 15K
C53 10K
Q52
Q51
R159 100K
R162 2K7
R163 220
R158 470
R101 470
R98 2K7
R96 2K7
R92 15K
R94 15K
R95 68K
R93 68K
D17 IN4148
D18 IN4148
D10 IN4148
D11 IN4148
Q23
R81 8K2
R79 4K7
C36 .1uF
R80 1K
R82 150K
R87 100K
Q22
R86 1K5
C32 16uF 10v
R83 27K
C54 10kp
R78 1K8
Q20
PR6 100K
R74 47K
R84 8K2
R99 15K
R102 2K7
Q29
Q30
BC 258B
R97 470
Q28
BC169C
Q27
R93X 10K
D19 IN4148
C33 .1uF
D12 IN4148
D13 IN4148
D20 IN4148
C34 .1uF
D14 IN4148
D21 IN4148
C35 .1uF
D15 IN4148
D22 IN4148
D16 IN4148
D23 IN4148
Q25
Q24
R88 22K
C37 80uF 12v
C31 10uF 16v
HCD Q26
2N5163
R85 2K2
R89 220K
C91 1K8
R100 68K
C38 47kp
R77 1K
R76 10K
C39 16uF 10v
R90 220K
R46 1K
R75 82K
C40 10uF 16v
C52 33uF
Q49
BC169C
PR7 2M5
R154 120K
R152 10K
R151 220
C50 16uF 10v
R155 47K
R153 15K
Q50
Q48
R142 2K2
D28 DK10
PR13 100K
R156 2K7
C47
R137 15K
Q43
Q42
R136 47K
Q40
Q41
Q39
R134 2K7
R129 47K
PR12 100K
Q44
R138 47K
R140 470
R139 1K8
R141 2K7
R135 2K2
Q31
R150 8K2
R133 2K7
Q47
D25 IN4148
R147 33K
Q46
R130 1K
R149 8K2
D26 IN4148
R148 12K
D27 DK10
R144 8K2
Q45
R143 1M
R145 8K2
ORANGE
C48 2.5uF 64v
R131 56K
C51 16uF 10v
R157 220
R132 10K

C

on the artwork.



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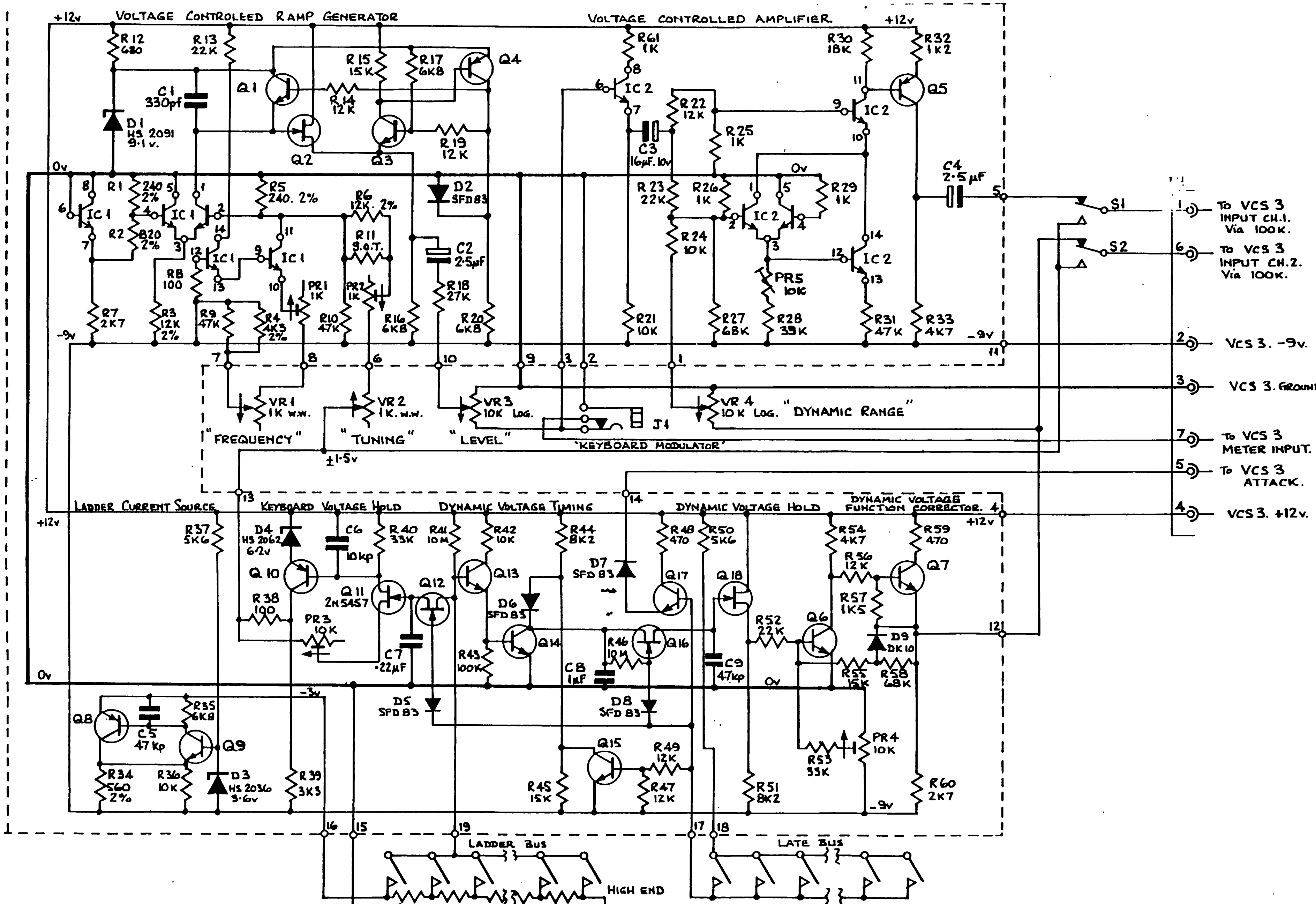
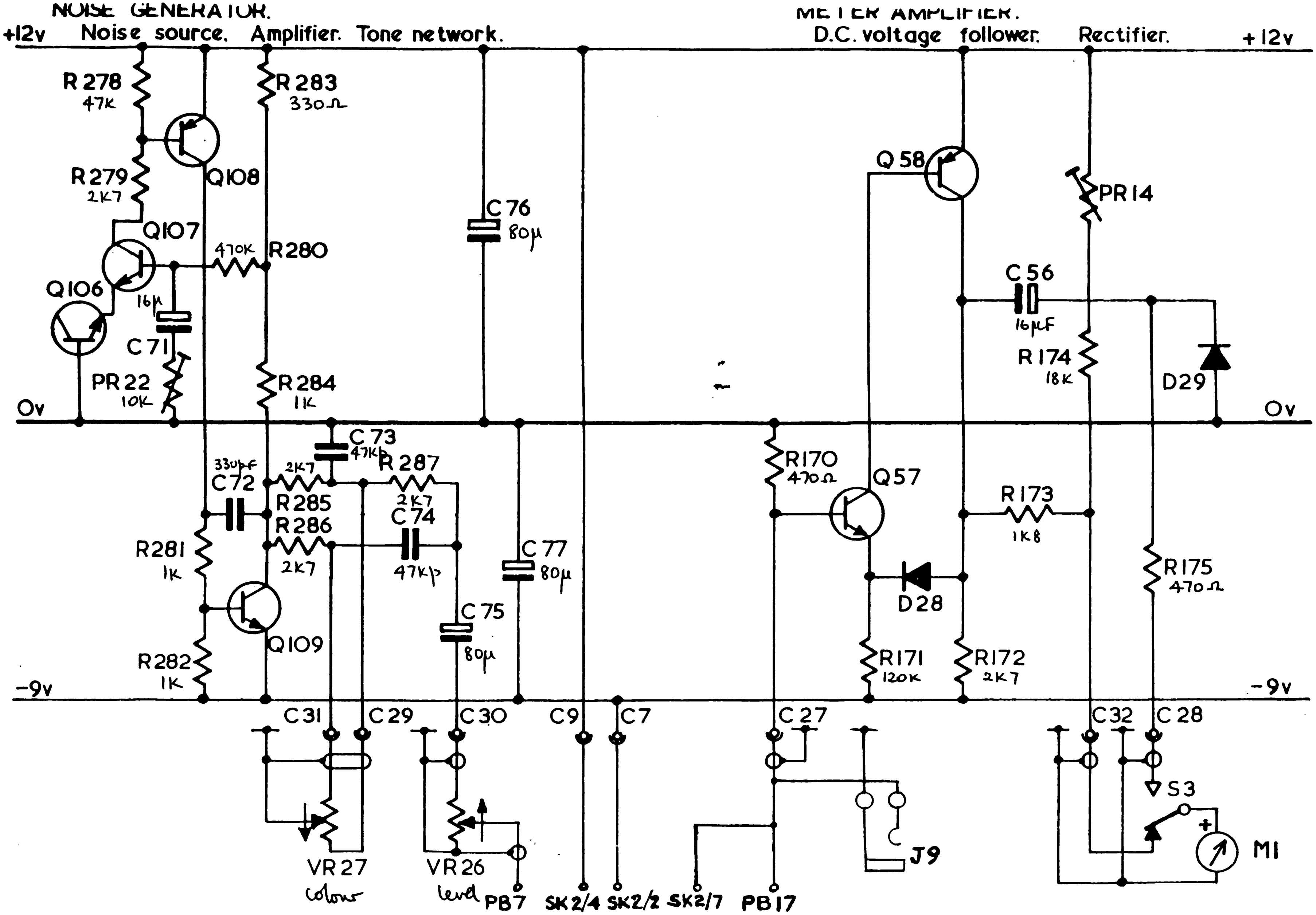
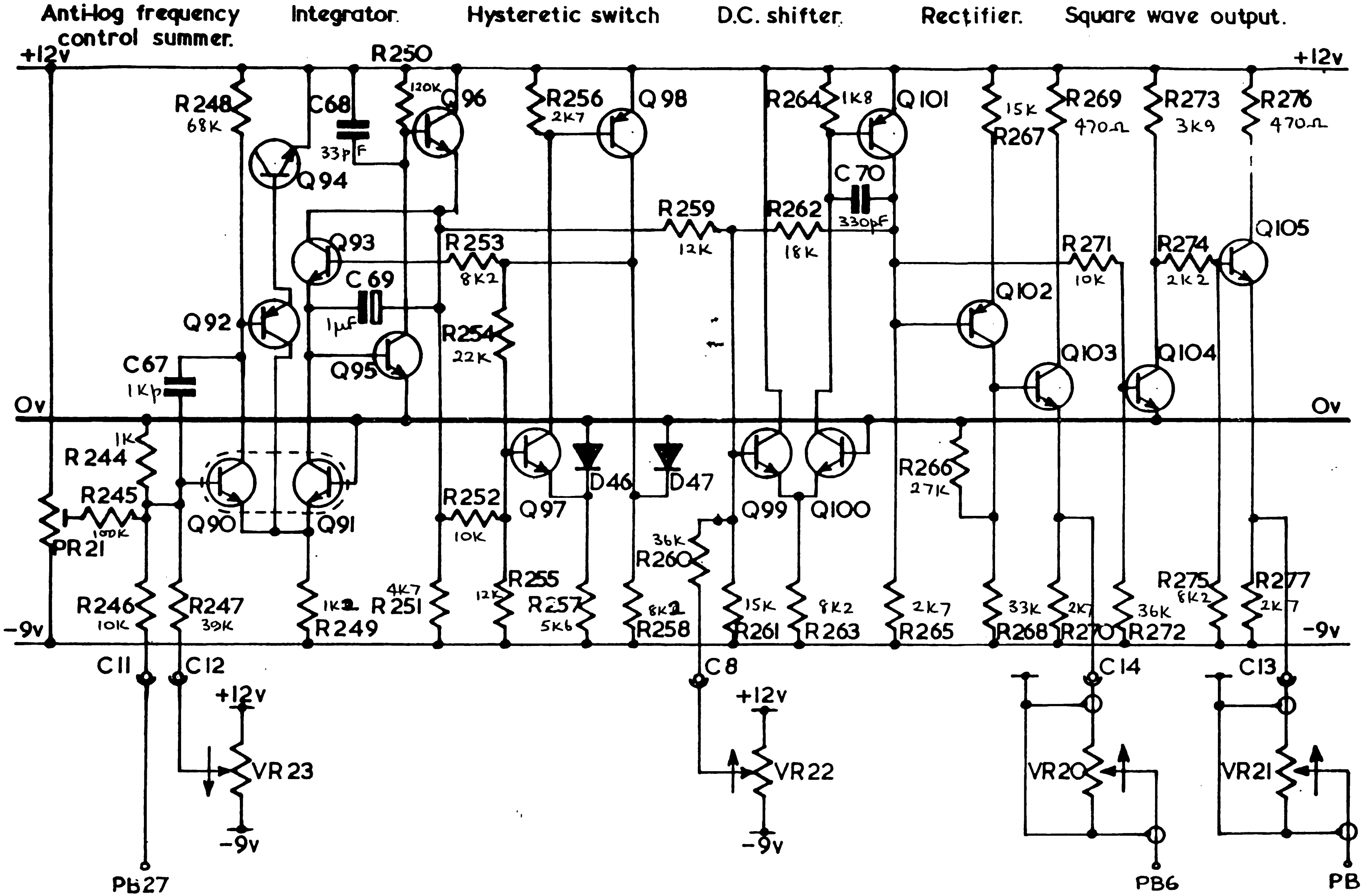


CIRCUIT DIAGRAM.
DYNAMIC KEYBOARD.

IOISE GENERATOR & METER AMPLIFIER P.C. BOARD "C"



VCS 3/ ISS.3/ CCT 11.

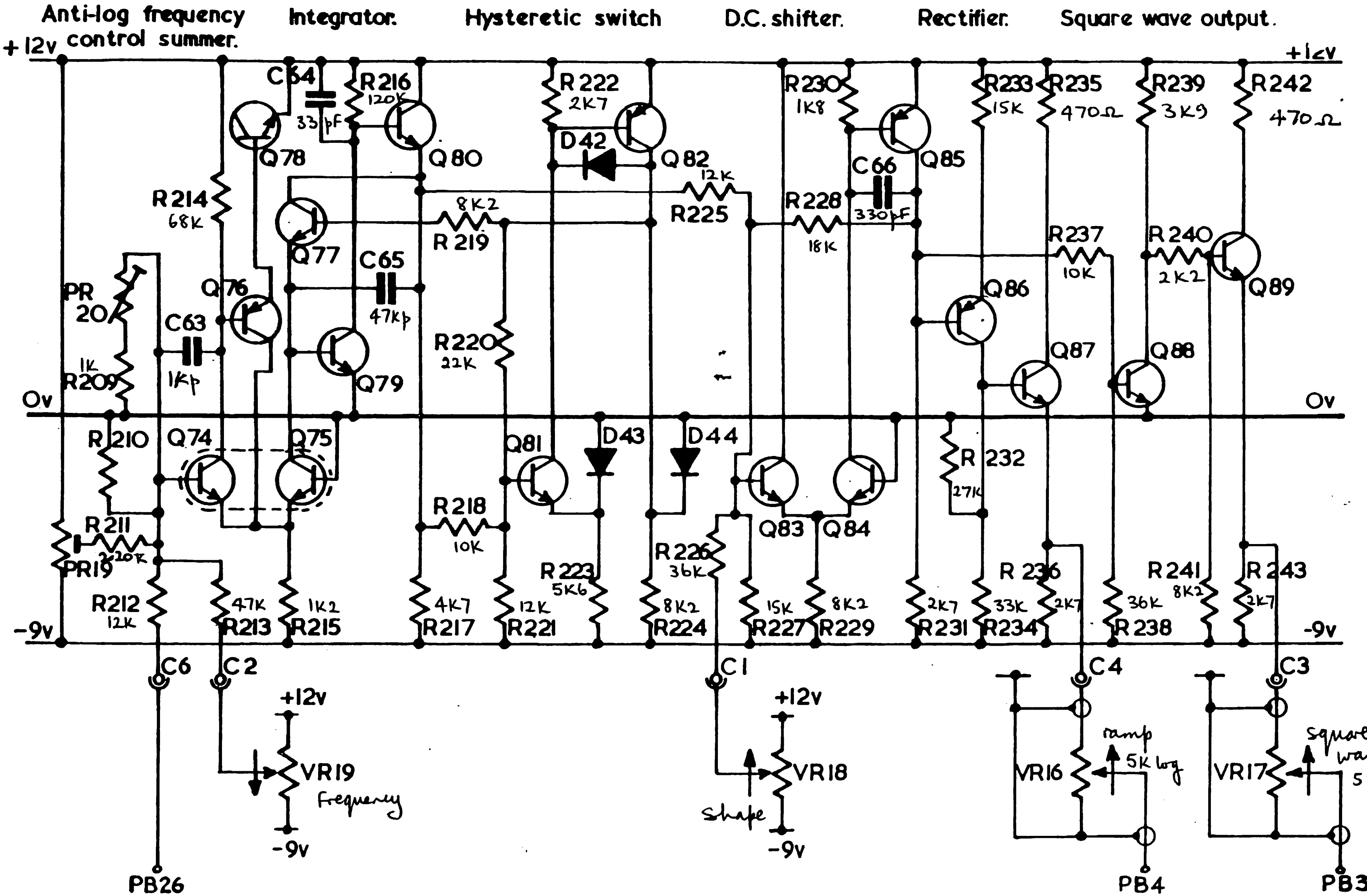


OSCILLATOR 3

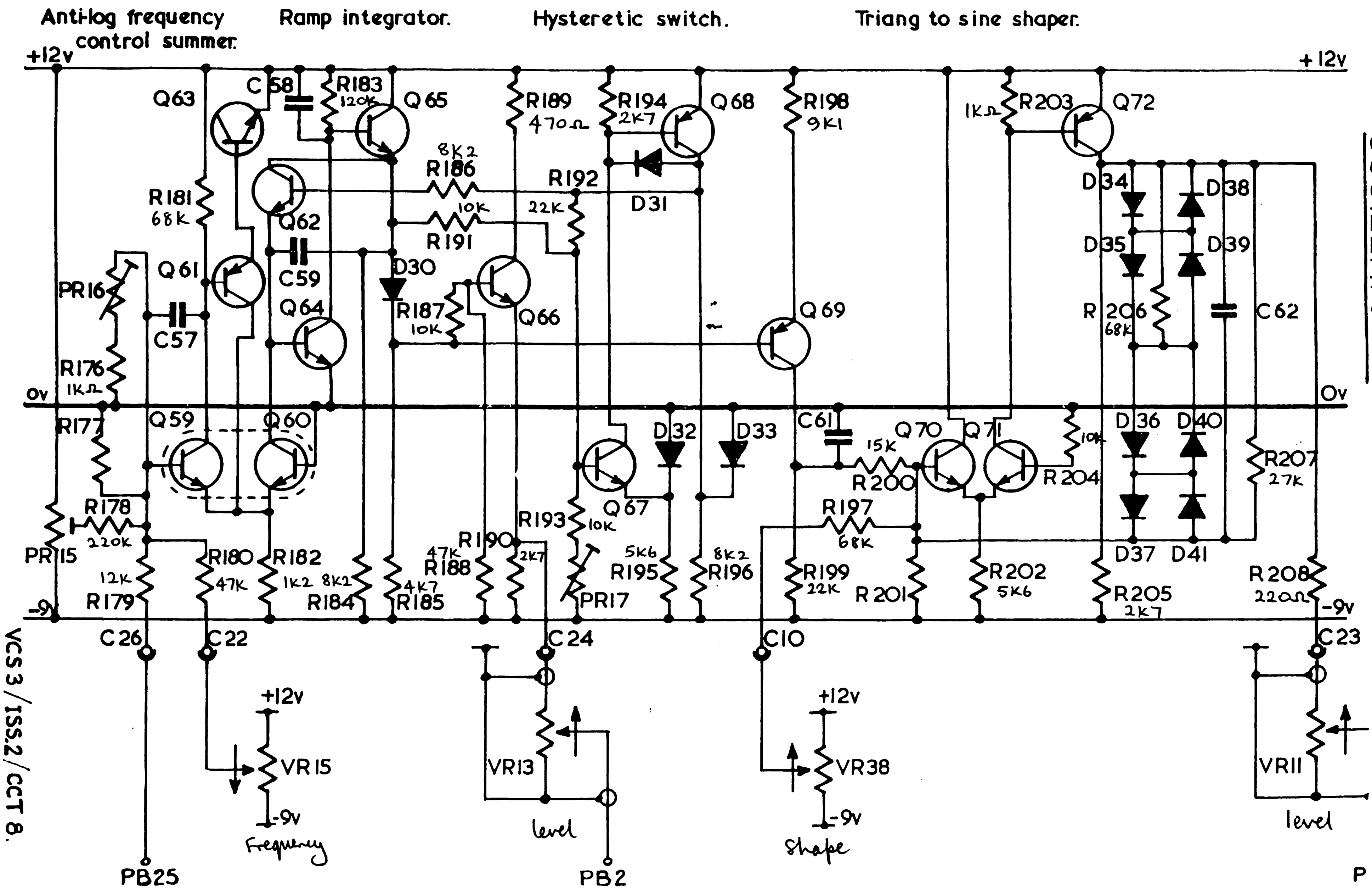
P.C. BOARD C.

VCS 3/1552/CCT 10

OSCILLATOR 2 P.C. BOARD C.

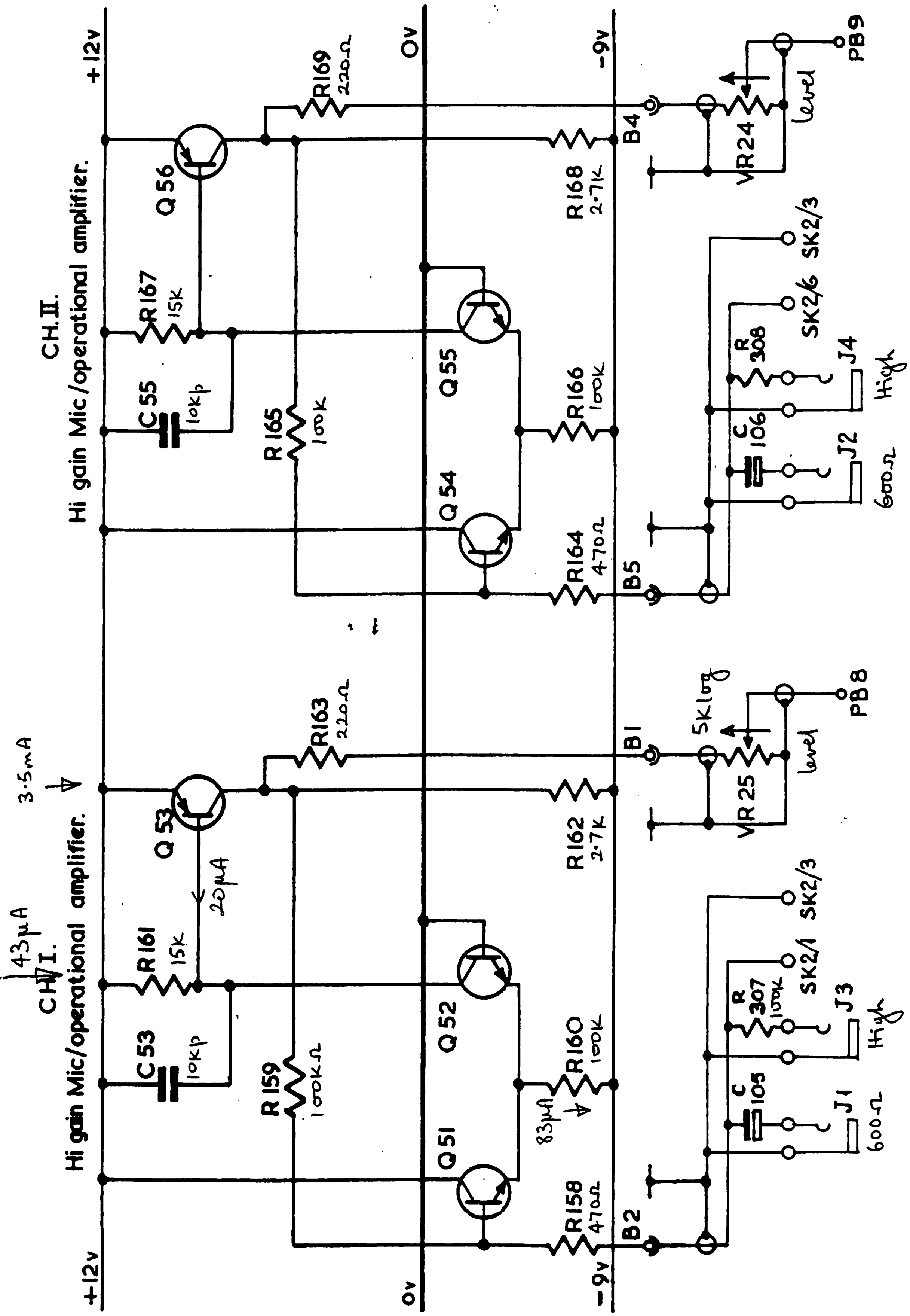


VCS3/ISS2/CCT9.



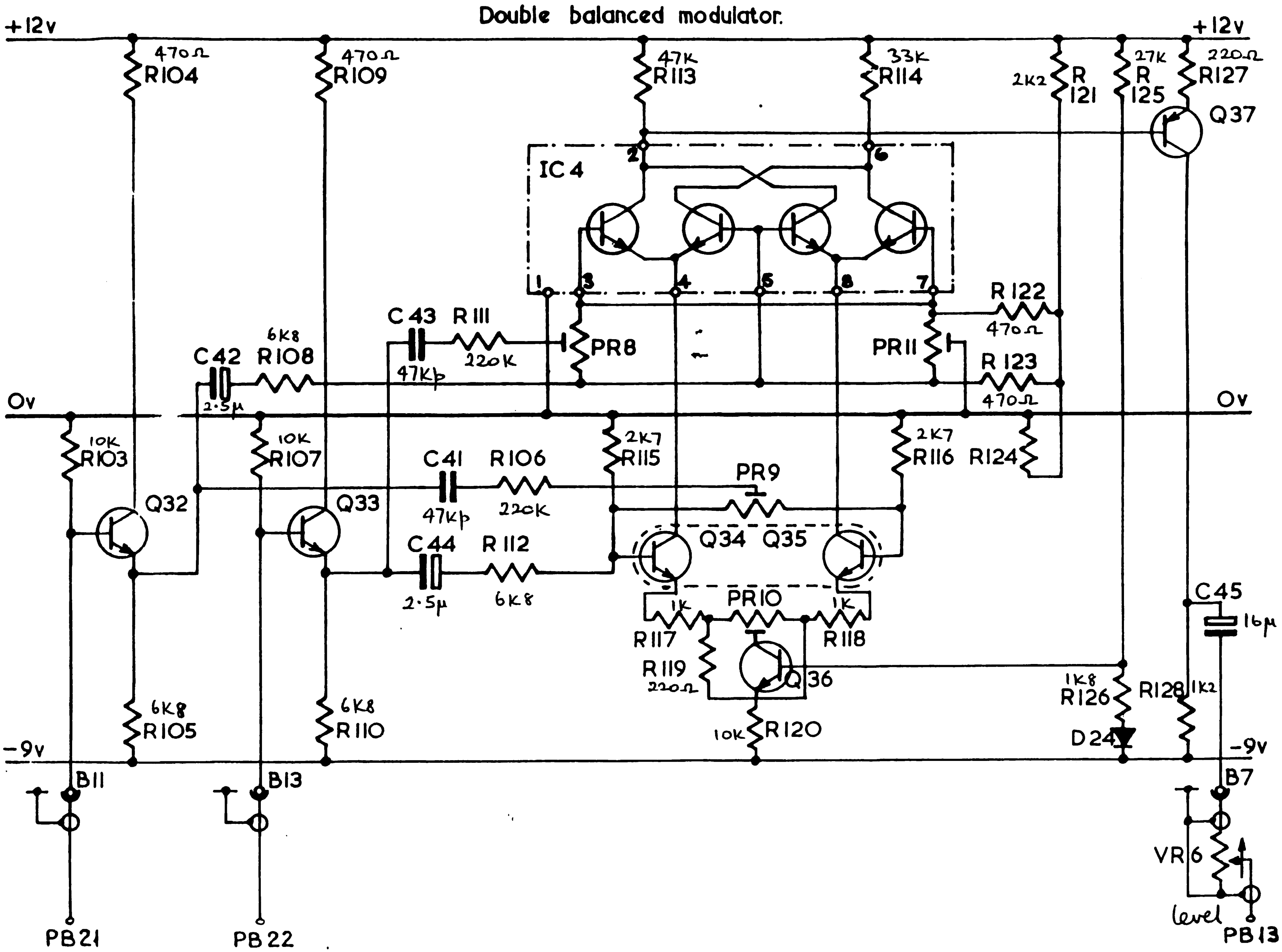
Anti-log frequency control summer.
Ramp integrator.
Hysteretic switch.
Triang to sine shaper.
+12v
0v
-9v
Q59
Q60
Q61
Q62
Q63
Q64
Q65
Q66
Q67
Q68
Q69
Q70
Q71
Q72
C57
C58
C59
C61
C62
R176 1KΩ
R177
R178 220K
R179 12K
R180 47K
R181 68K
R182 1K2
R183 120K
R184 8K2
R185 4K7
R186 8K2
R187 10K
R188 47K
R189 470Ω
R190 2K7
R191 10K
R192 22K
R193 10K
R194 2K7
R195 5K6
R196 8K2
R197 68K
R198 9K1
R199 22K
R200 15K
R201
R202 5K6
R203 1KΩ
R204 10K
R205 2K7
R206 68K
R207 27K
R208 220Ω
PR15
PR16
PR17
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
C26
C22
C24
C10
C23
VR15
VR13
VR38
VR11
Frequency
level
Shape
level
PB25
PB2
P
VCS3/ISS.2/CCT 8.

INPUT CHANNEL AMPLIFIERS P.C.BOARD "B"



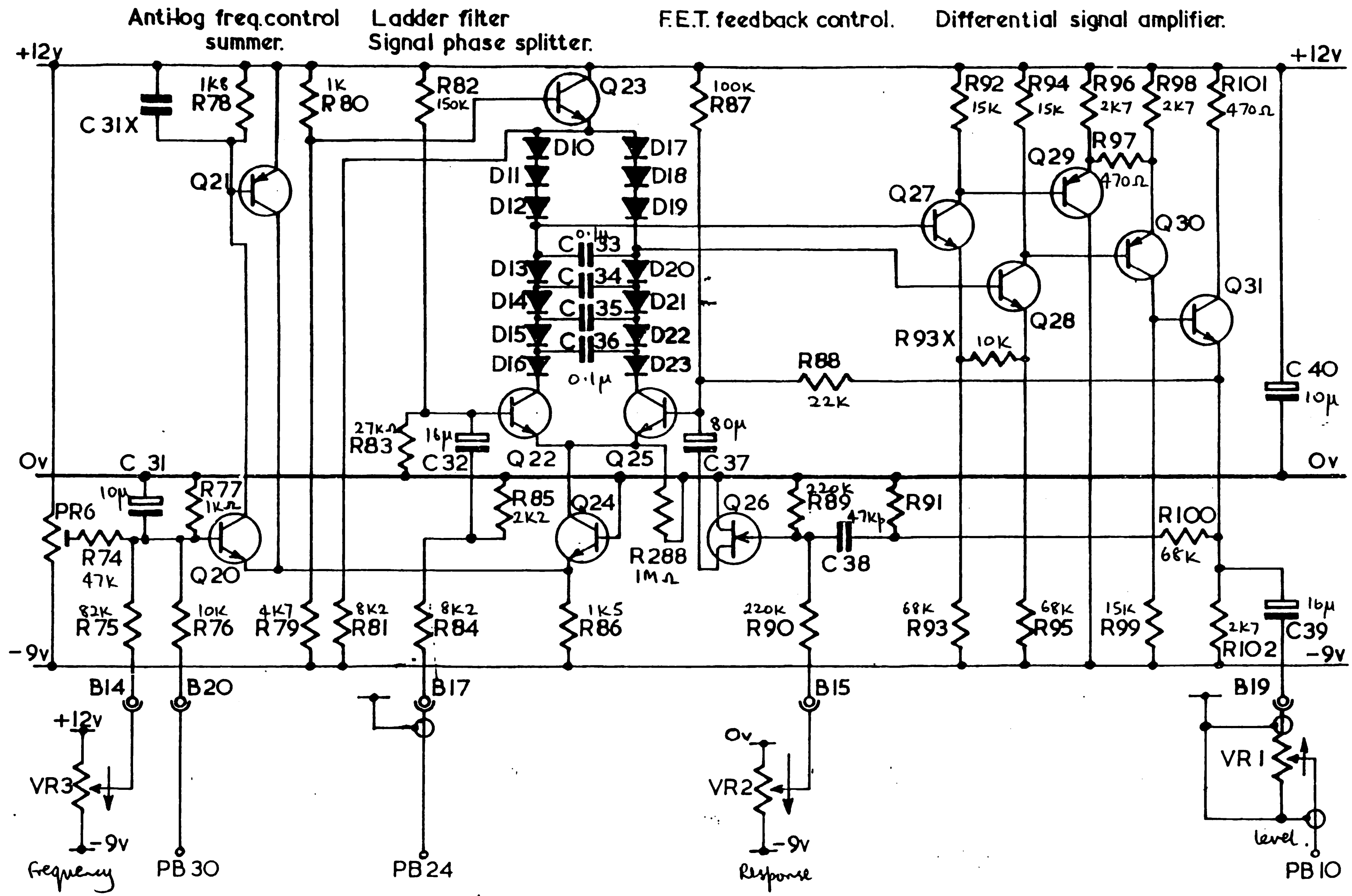
VCS 3 / ISS.2 / CCT 7

RING MODULATOR P.C. BOARD "B"

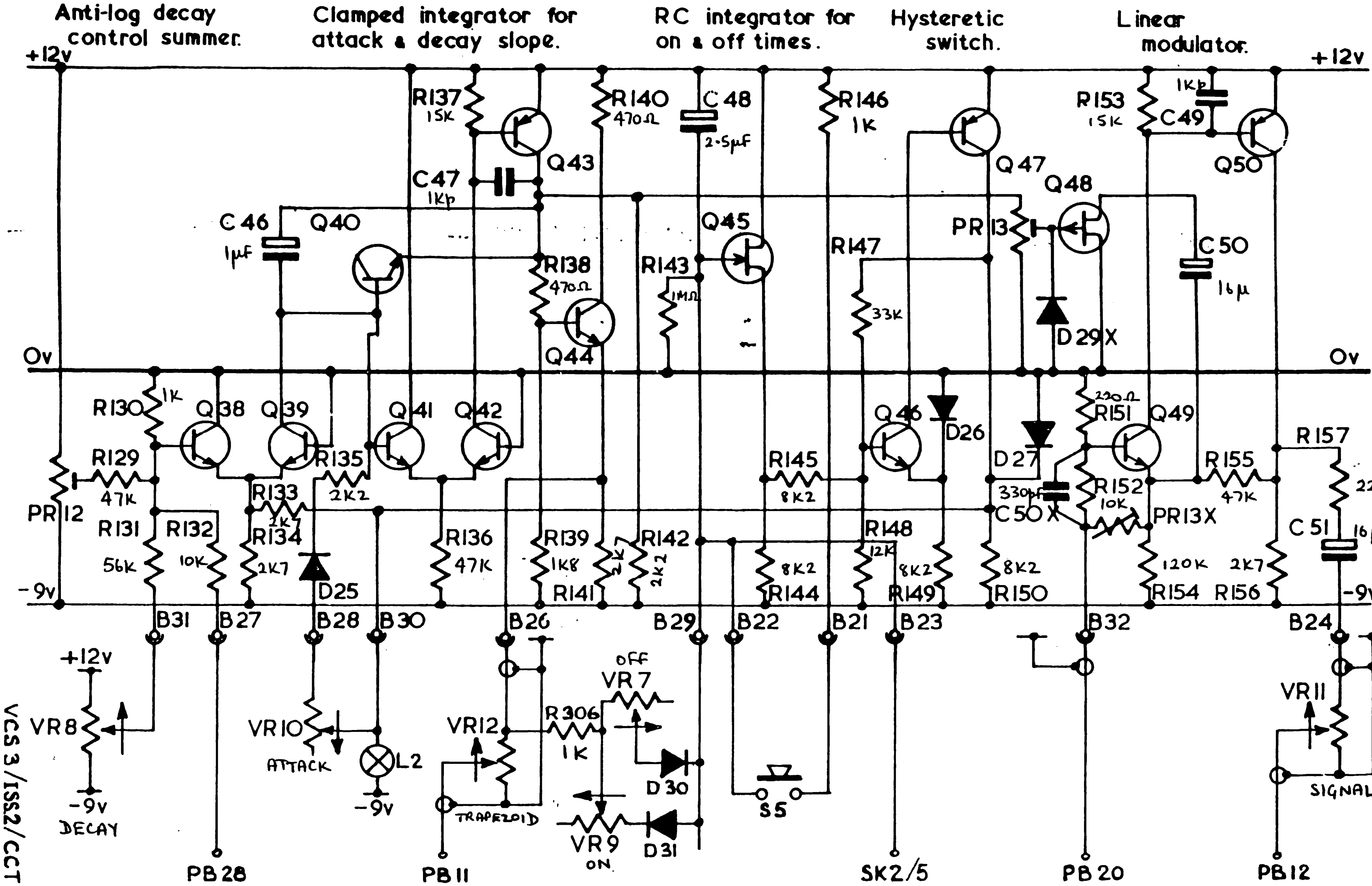


VCS3/ISS2/CCT6.

FILTER P.C. BOARD B



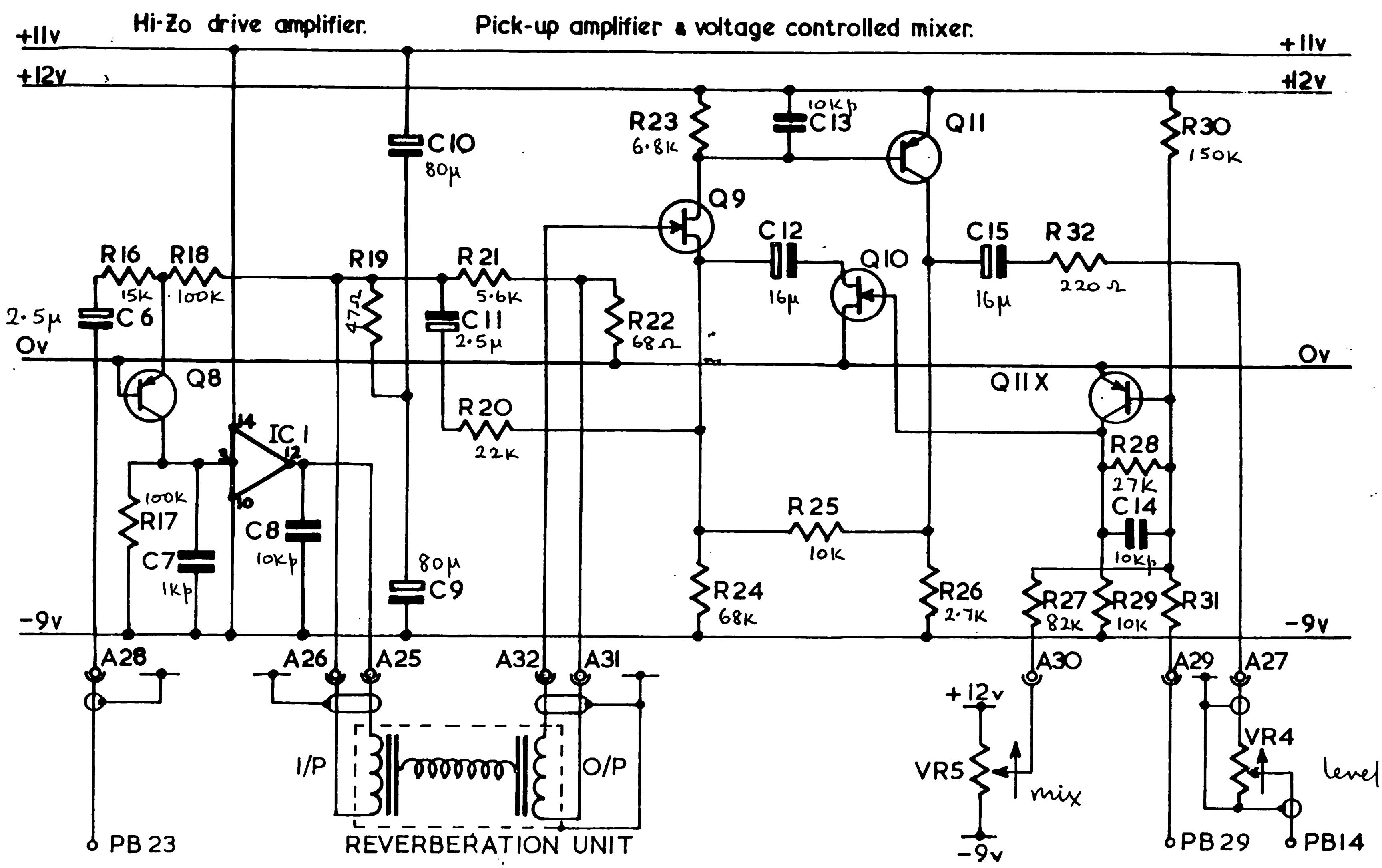
VCS 3/1SS3/CCT 5.



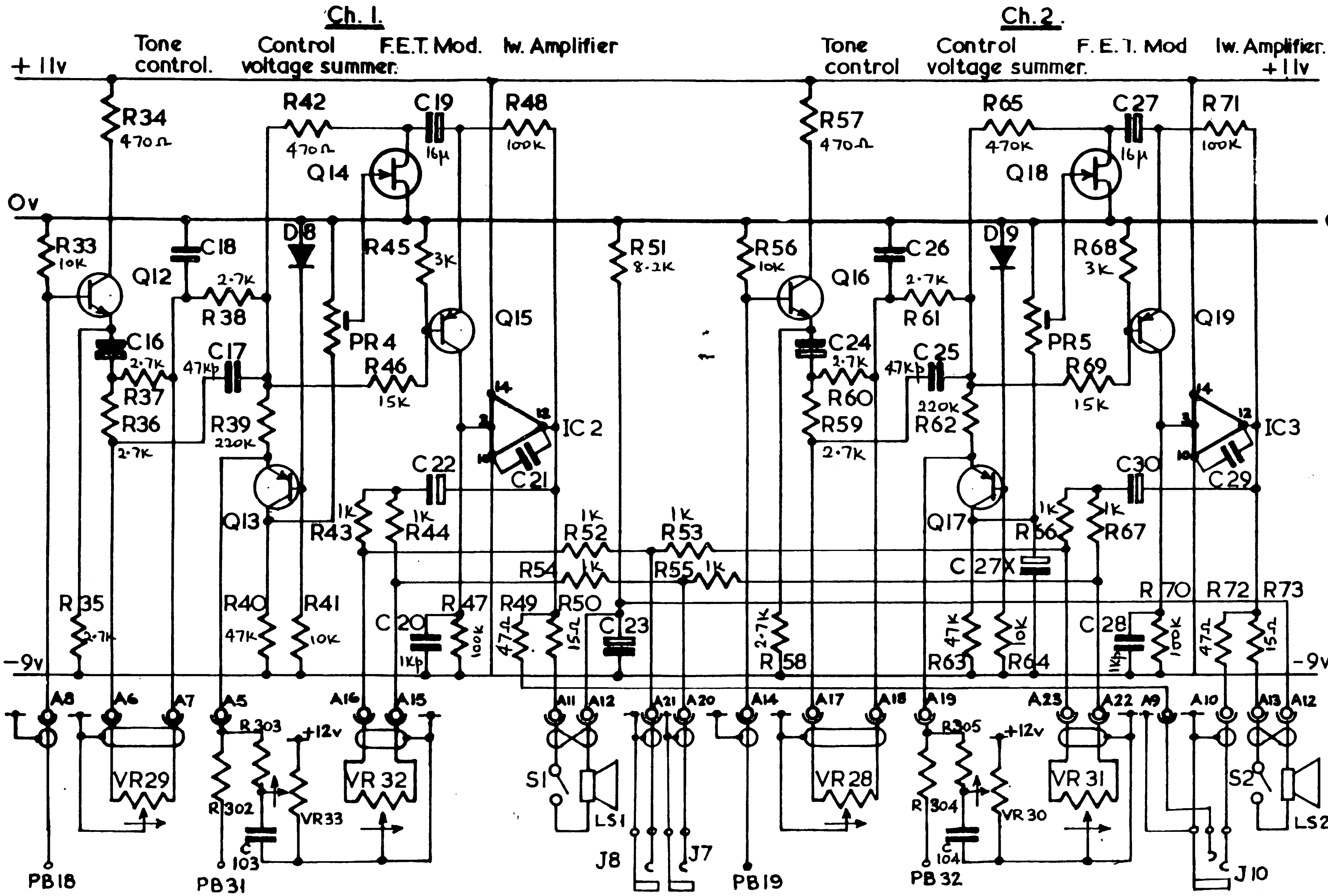
ENVELOPE SHAPER P.C. BOARD B

VCS 3/ISS2/CCT 4.

REVERBERATION P.C. BOARD "A"

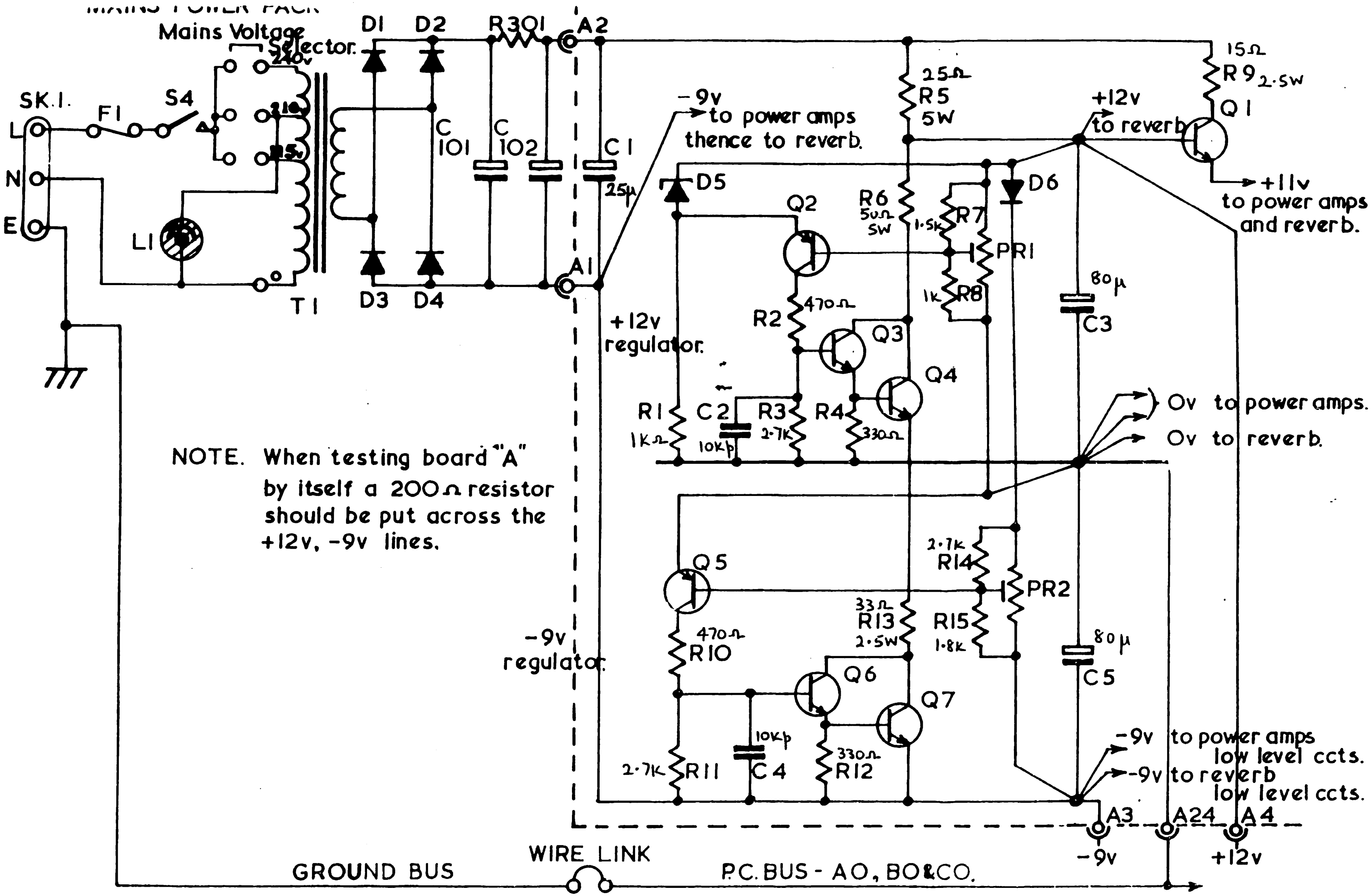


VCS3/ISS.2/CCT 3.



VCS3/ISS.2/CCT 2.

OUTPUT CHANNEL AMPLIFIERS P.C. BOARD 3



POWER SUPPLY P.C. BOARD A.

VCS 3/ISS.2/CCT1

Dynamic Keyboard - Setting-up procedure

Set all knobs and presets halfway.
First set the keyboard zero volts at middle F sharp. Press middle F sharp with scope on Pin 13 of keyboard circuit. Adjust PR3 for 0 Volts ± 50 mV.
Check that top C gives 1.5V ± 200 mV
Check that bottom C gives -1.5V ± 200 mV
Check drift rate when key is released. Should be less than 100 mV per minute.
If greater suspect Q12. This should have a Vp of 2.5 - 3.0.

Keyboard Oscillator

Press middle F sharp. With VR1 (Frequency) at 5 and VR3 clockwise put scope on live connection of jack socket 'Keyboard Modulator'. Adjust PR1 for 248 Hz at F sharp or 261 Hz for middle G.
If PR1 is off range clockwise then snip R9.
If PR1 is off range counterclockwise then reduce R9 value by half.
Hold down bottom C, and set VR2 (Tuning) to 5. Press C one octave higher.
Trim PR2 to get exactly an octave higher than bottom C.
If PR2 is off range clockwise then snip R11
If PR2 is off range counterclockwise suspect circuit fault.
With Frequency at 0 press lowest note. Should be lower than 30 Hz.
With Frequency at 10 press highest note. Should be higher than 8 kHz.

Dynamic Voltage

Short across C9 and trim PR4 for +3V at Pin 12 on keyboard circuit.
DO NOT PRESS A KEY WITH SHORT IN PLACE.
Check for drift, which should be less than 100mV in ten seconds.
Check that Dynamic Range has no effect on keyboard oscillator loudness when turned to zero. If so re-adjust PR4.

Contact Displacement

Each note has two sets of contacts. One pair, that is not connected to the resistors, must be adjusted to make about .03" after the other pair. With practice it is possible to do this by eye using a fine pair of tweezers.
With VR1 and VR2 halfway, VR3 and VR4 fully clockwise and both switches up.
Monitor the signal output on a scope. Strike each note with a even force.
This should give about 10 dB less (⅓ as much) than hitting it hard. Maximum level should give about 2V p.p on the scope. Adjust the crooked member of the late pair where necessary. Closing the gap makes the note louder. If

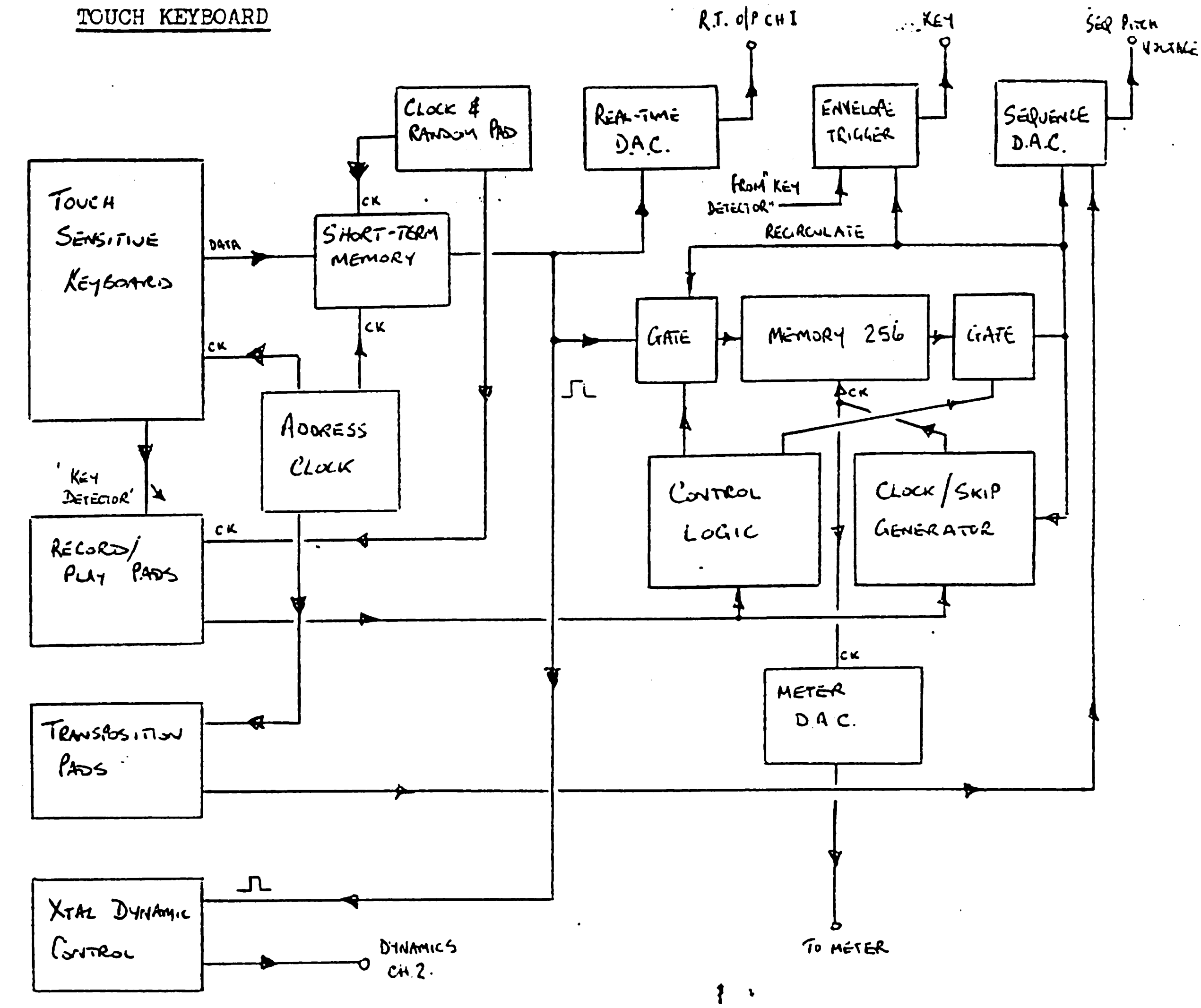
Dynamic Keyboard - Contact displacement(continued)

visual alignment still gives performance inconsistencies this is almost certainly due to contacts being dirty. This is a frequent source of problems on the keyboard generally, giving swoops and dithering pitches at different places on the keyboard. Use cotton buds and Isopropyl alcohol to carefully wipe each surface of each contact. Extreme care must be taken not to disturb the contact displacement, but this will restore precision to the keys. Never use an abrasive substance on contacts since they are gold-plated. Blistered plating means new contacts must be fitted.

Setting up DK2 keyboard

DK2 keyboards are duophonic, so that Channel 1 pitch voltage comes from the lower note being played, with Channel 2 pitch voltage coming from the upper note. This second upper note voltage is derived from the lower note and PR6 needs to be adjusted to get the relationship right. Connect Channel 2 Voltage to control an oscillator with the Input Channel gain at maximum. Hold down the bottom key with sellotape and play the top note. If the oscillator pitch shifts adjust PR6 until there is no more movement.
Some keyboards were modified from DK1 (monophonic) to DK2 bY the addition of a small pc board under the main one. In these cases PR6 is the preset on the small board.

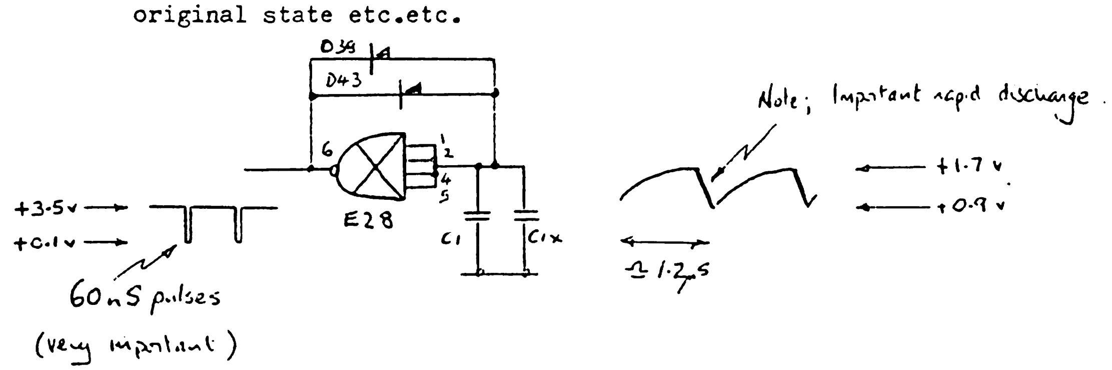
TOUCH KEYBOARD

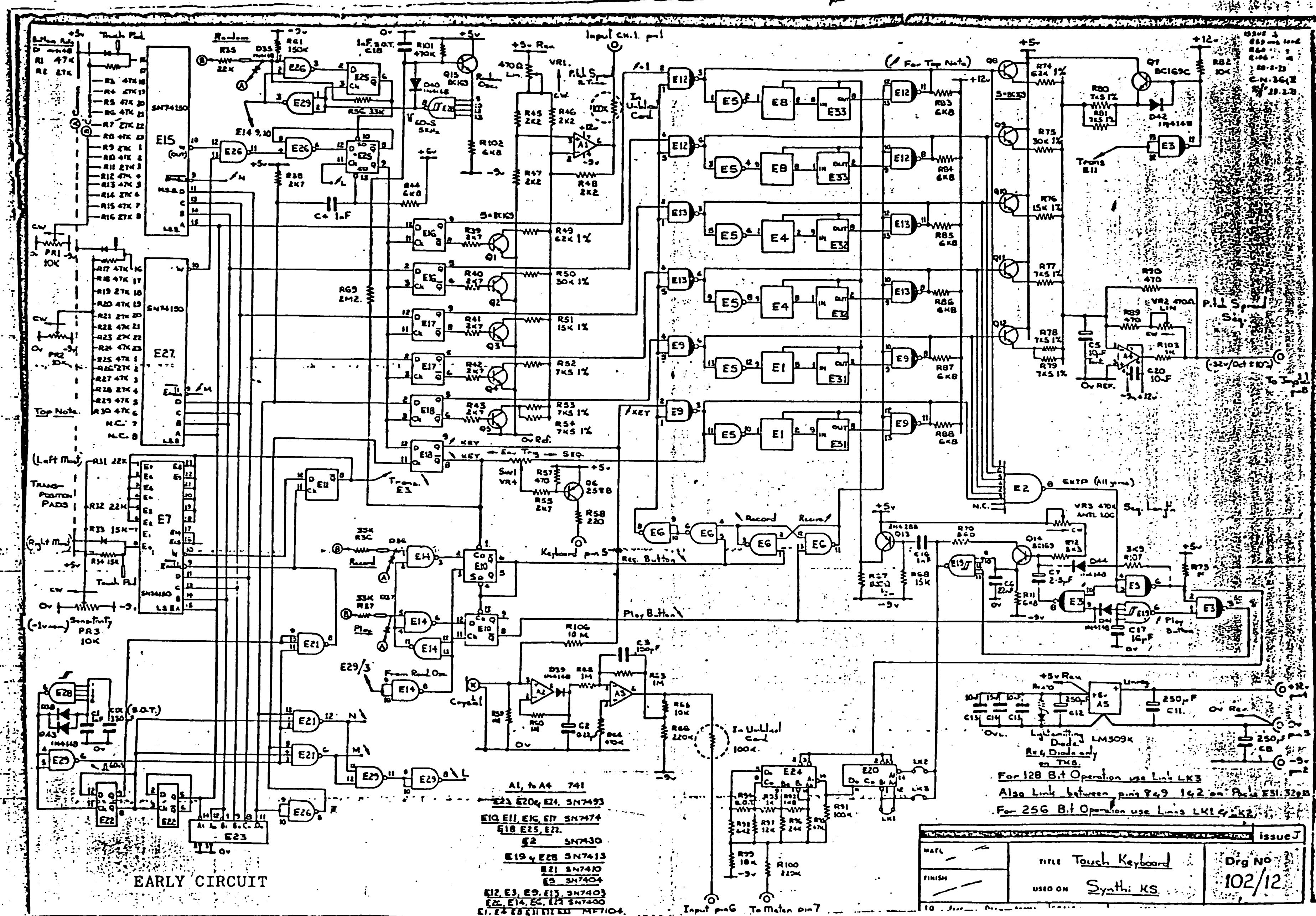


FIRSTLY. The Touch Keyboard and address clock.

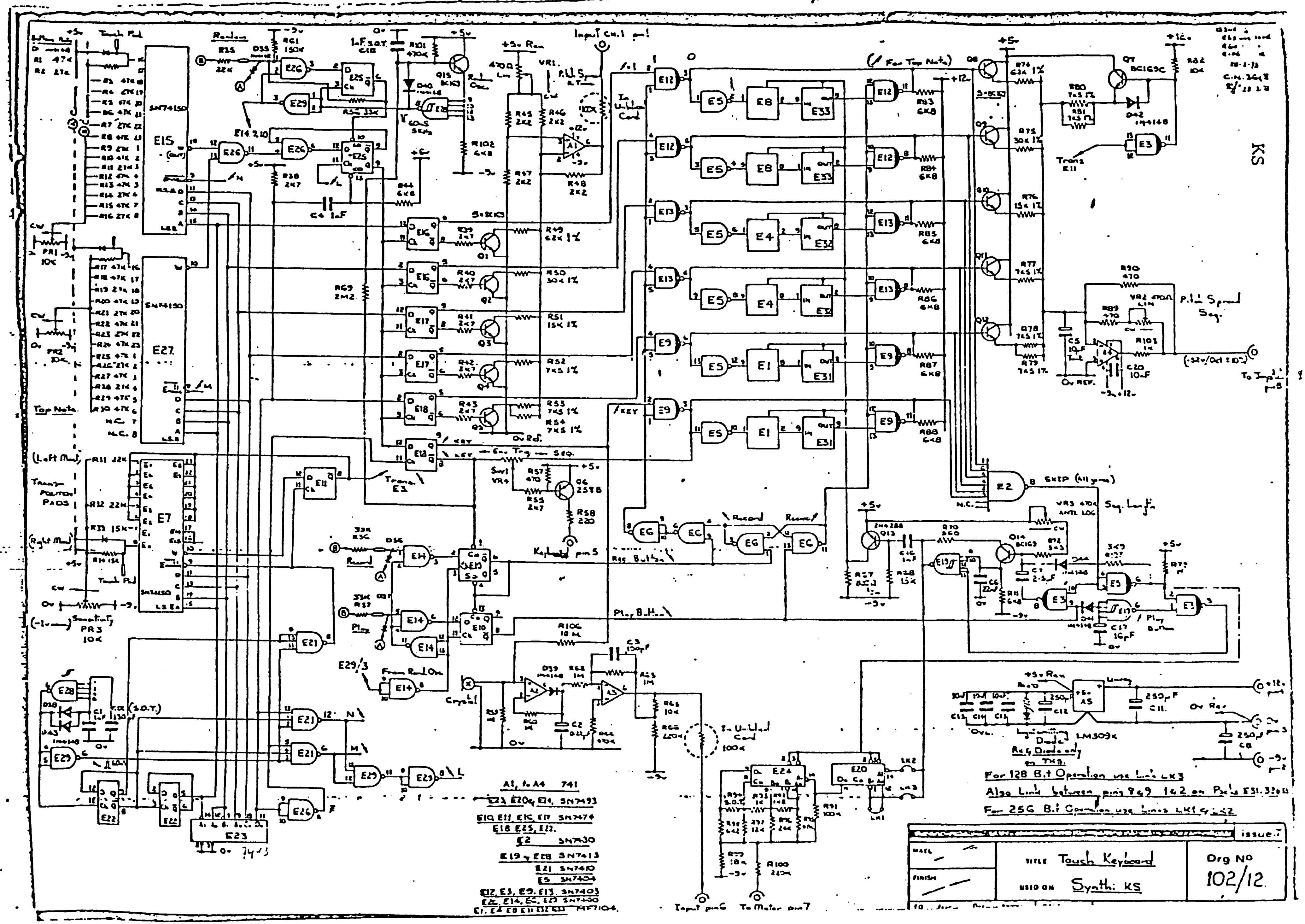
The address clock is an oscillator, E28 (Pins 1,2,4,5,6), being a conventional schmitt trigger oscillator.

OPERATION Pin 6 is high; D38, 43 are off, C1 and C1X charged up by way of Pins 1,2,4,5 until upper threshold voltage (about +1.7v) is reached, the schmitt then fires, Pin 6 goes low, D38, 43 turn on and discharges C1 and C1X until the lower threshold voltage (about 0.9v) is reached. The schmitt then reverts back to its original state etc.etc.

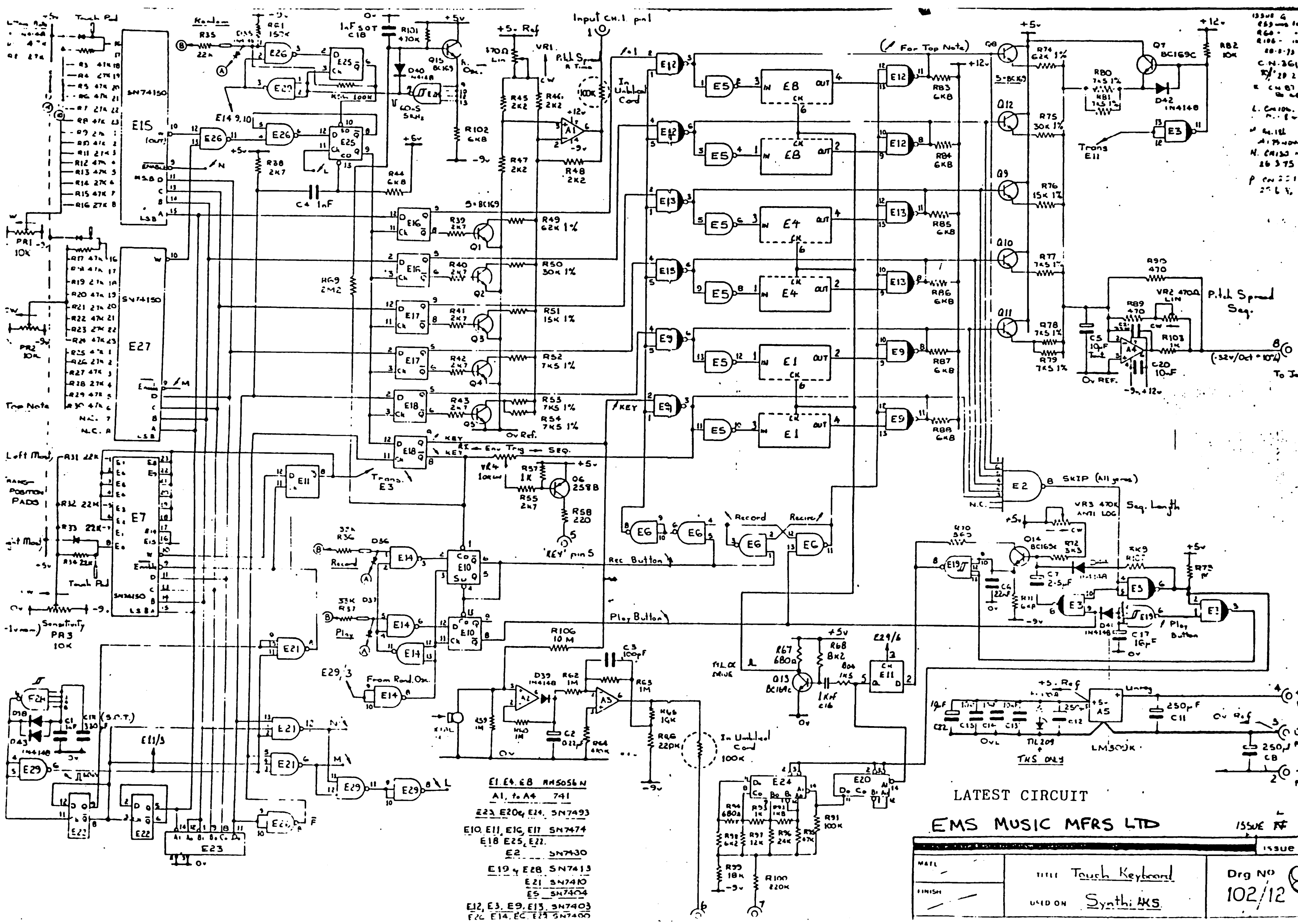




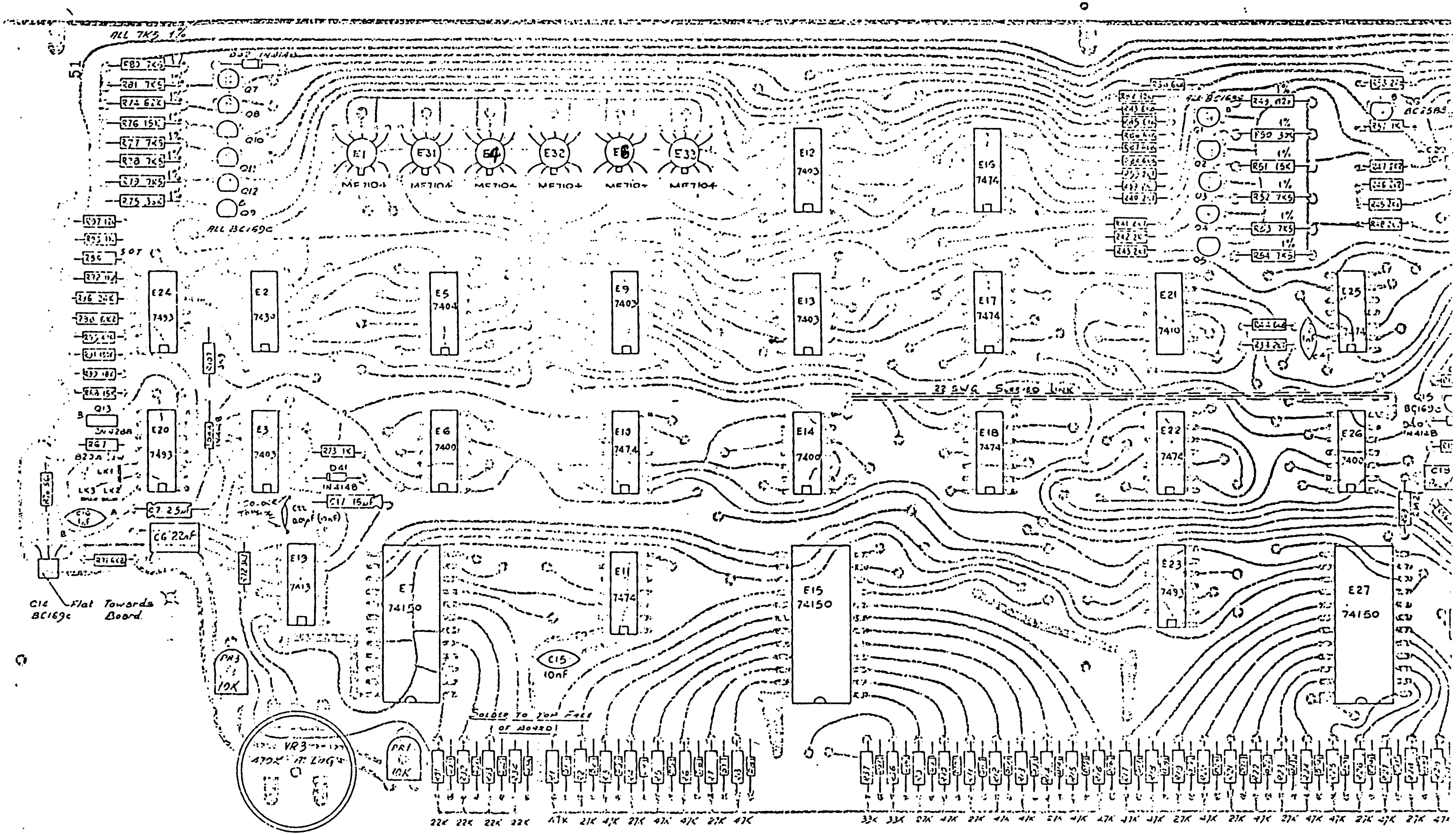
For 128 Bit Operation use Link LK3
Also Link between pins 8 & 9 1 & 2 on Packs E31:32 & 33
For 256 Bit Operation use Links LK1 & LK2
A1, to A4 741
E23 E20 & E24 SN7493
E10, E11, E16, E17 SN7474
E18 E25, E22.
E2 SN7430
E19 & E28 SN7413
E21 SN7410
E5 SN7404
E12, E3, E9, E13, SN7403
E26, E14, EG, E29 SN7400
SN74150
LM309K
issue J
TITLE Touch Keyboard
USED ON Synthi KS
Drg NO 102/12
EARLY CIRCUIT



For 128 Bit Operation use Link LK3
For 256 Bit Operation use Links LK1 & LK2
A1, to A4 741
E12, E3, E9, E13 SN7403
E2 SN7430
E21 SN7410
E5 SN7404
E27 SN74150
E15 SN74150
LM309K
Touch Keyboard
Synthi KS
Drg No
102/12
issue 7
Pitch Spread Seq.
SKIP (All zero)
Seq. Length
Keyboard pin 5
Input pin 6
To Meter pin 7
Top Note
Random
Record
Play
Crystal



LATEST CIRCUIT
EMS MUSIC MFRS LTD
TITLE Touch Keyboard
USED ON Synthi AKS
Drg No 102/12
E1. E4. E8 RM5056N
A1. to A4 741
E23 E20, E24. SN7493
E10. E11, E16, E17 SN7474
E18 E25, E22.
E2 SN7430
E19 & E28 SN7413
E21 SN7410
E5 SN7404
E12, E3. E9. E13. SN7403
E26 E14. E6. E29 SN7400
E15
SN74150
E27
E7
Touch Pad
Random
Input CH.1 pin1
P.L.L. Spread
SKIP (All zeros)
Seq. Length
Pitch Spread Seq.
To Joys
Record
Play
Rec Button
Play Button
'KEY' pin 5
LM309K
TTL 209
TKS ONLY

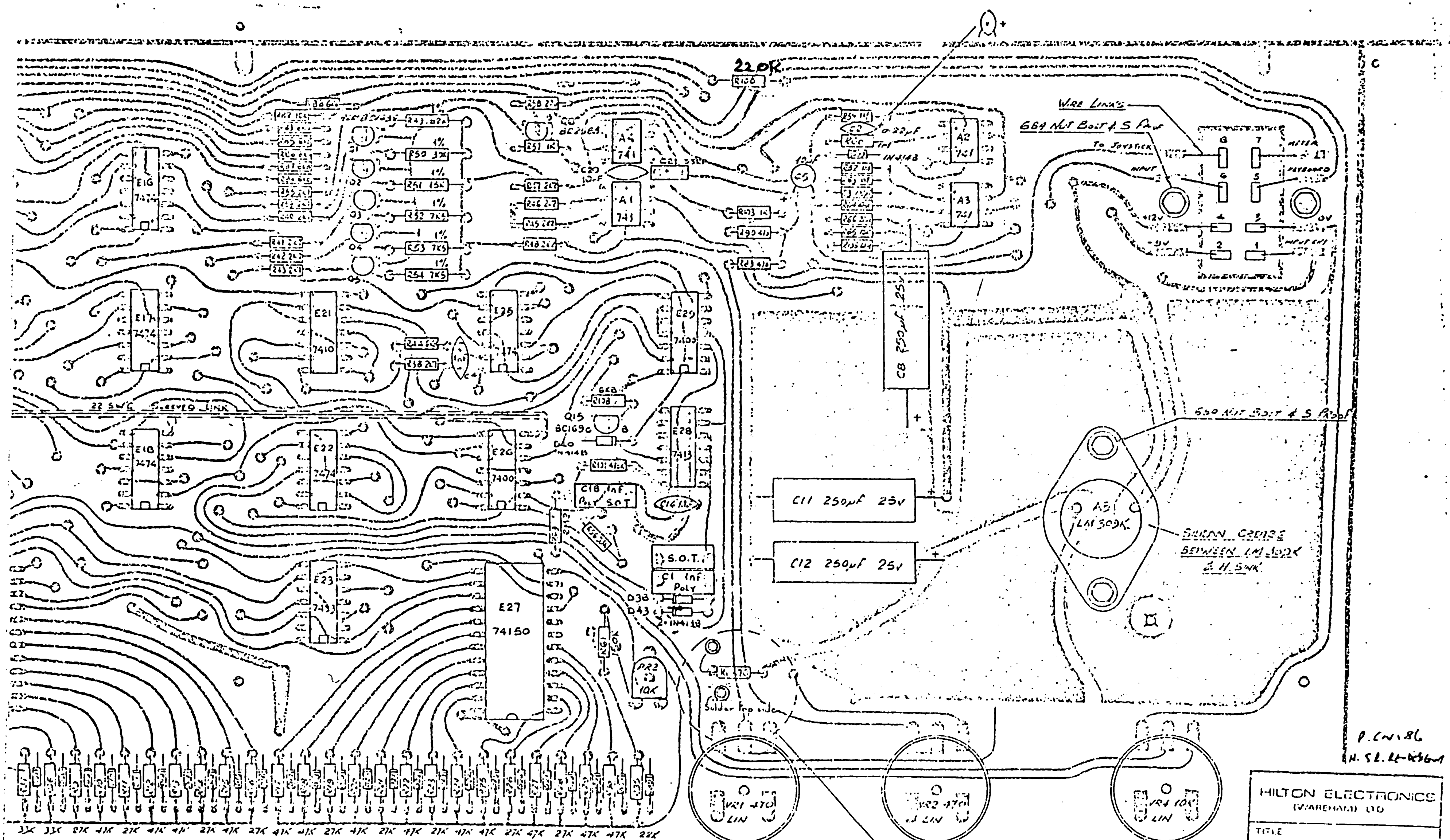


* INSERT LINK LK3 FOR 64 BIT STORAGE

INSERT LINK LK1, LK2 & PACKS E31, E32 & E33 FOR 128 BIT STORAGE

UNLESS OTHERWISE STATED ALL DIODES 1N4148

NOTE WIRE LEADS SHOULD ...



UNLESS OTHERWISE STATED ALL DIODES 1N4148

128 BIT STORAGE

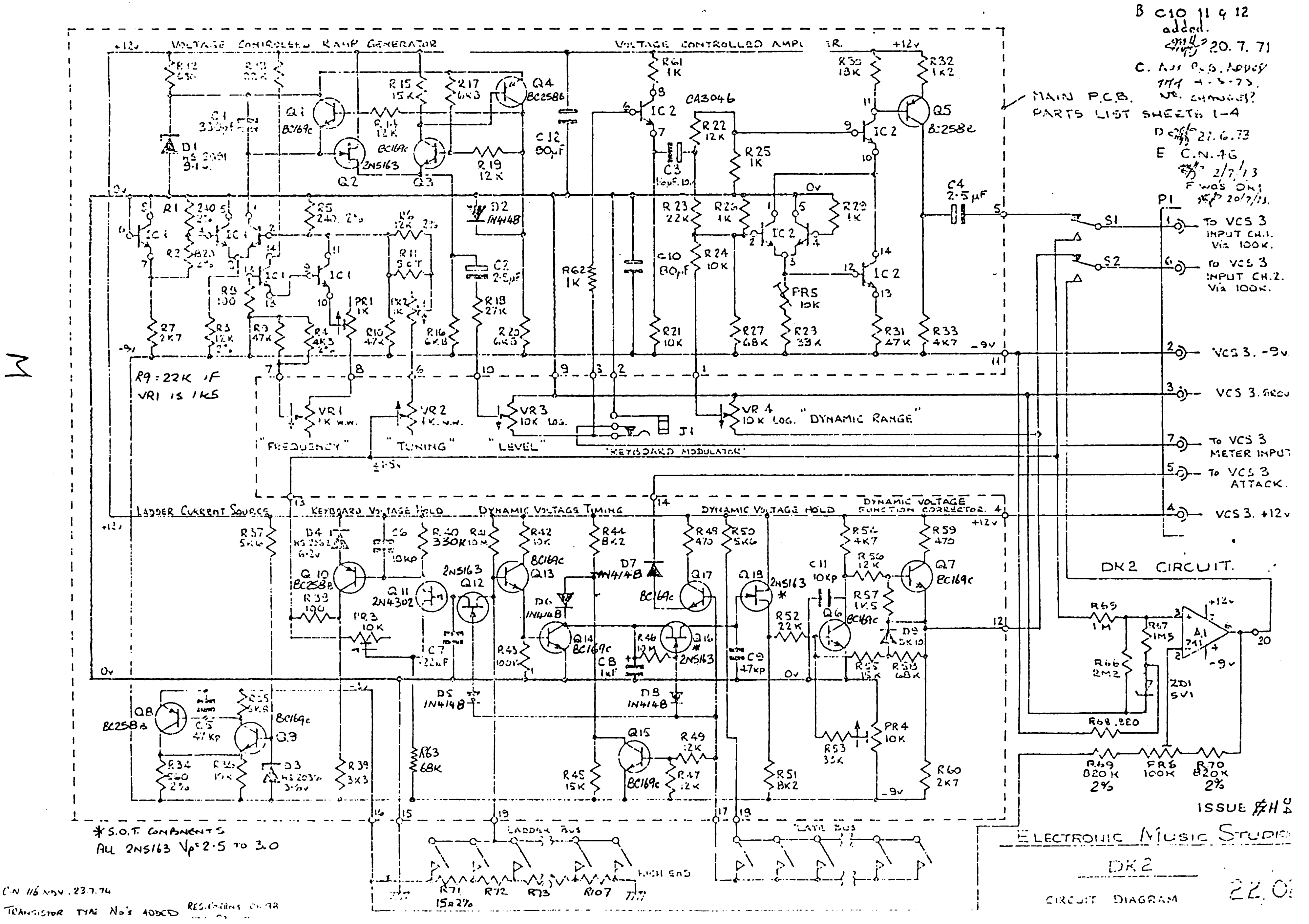
NOTE WIRE LEADS SHOULD BE SOLDERED TO THE CRYSTAL LEADS AND THE WIRE LEADS ARE TO BE SOLDERED INTO THE PCB THE CRYSTAL SHOULD THEN BE ARALDITED TO THE BOARD

NOTES
PIN 14 : +5V, PIN 7 : 0V } TYPES 7400, 7403, 7410, 7413, 7430, 7474.
PIN 5 : +5V, PIN 10 : 0V } TYPE 7493
PIN 24 : +5V, PIN 12 : 0V } TYPE 74150

HILTON ELECTRONICS (WAREHAM) LTD

TITLE TOUCH KEYBOARD ASSY. AKS.

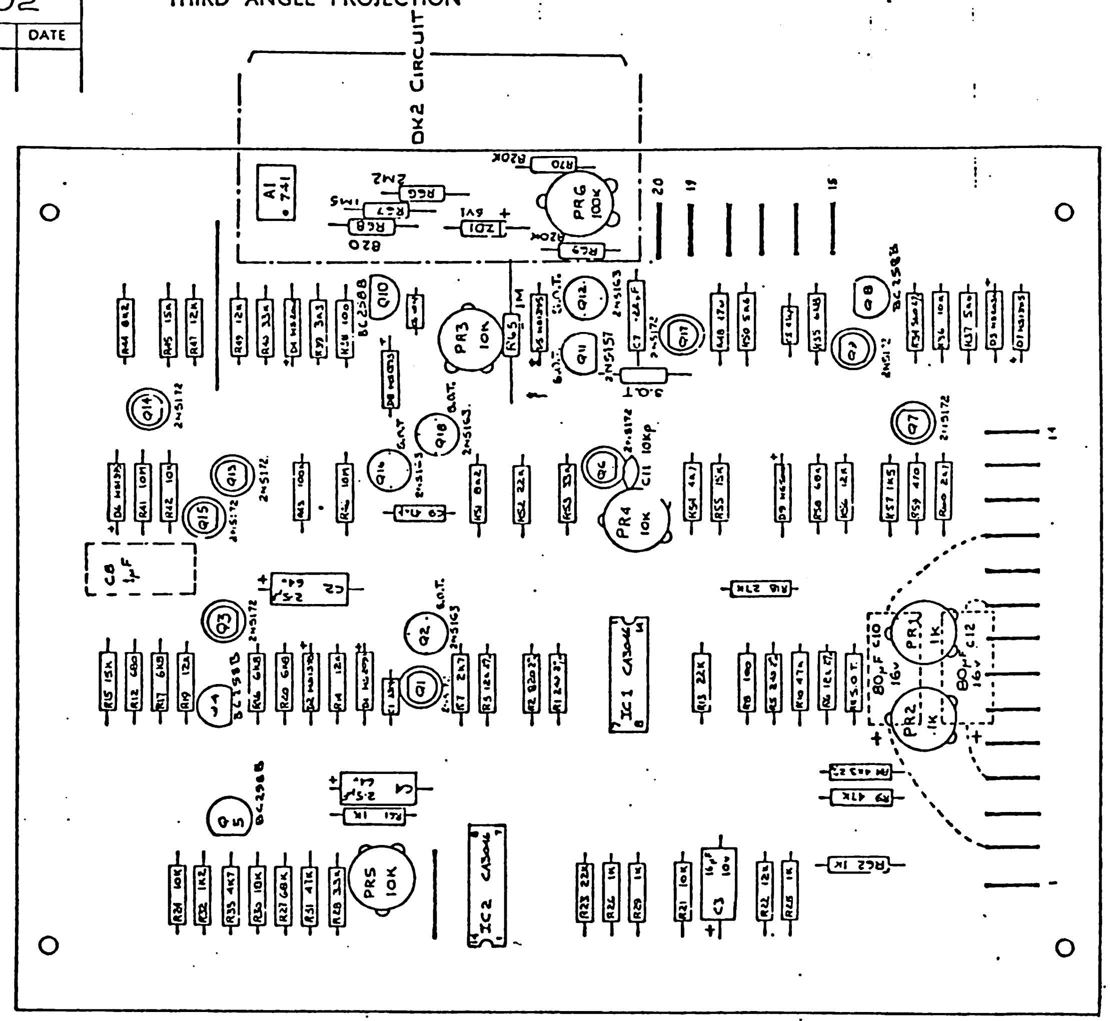
DRG No 103/4



B C10 11 & 12 added. 20. 7. 71
C. ALT P.C.B. LAYOUT 4-5-73. NO CHANGES?
D 21.6.73
E C.N. 46 2/7/73
F was OK! 20/7/73.
MAIN P.C.B. PARTS LIST SHEETS 1-4
VOLTAGE CONTROLLED RAMP GENERATOR
VOLTAGE CONTROLLED AMPLIFIER.
CA3046
R9 = 22K IF VR1 IS 1K5
"FREQUENCY"
"TUNING"
"LEVEL"
"DYNAMIC RANGE"
"KEYBOARD MODULATOR"
LADDER CURRENT SOURCE
KEYBOARD VOLTAGE HOLD
DYNAMIC VOLTAGE TIMING
DYNAMIC VOLTAGE HOLD
DYNAMIC VOLTAGE FUNCTION CORRECTOR.
To VCS 3 INPUT CH.1. Via 100K.
To VCS 3 INPUT CH.2. Via 100K.
VCS 3. -9v.
VCS 3. GROUND
To VCS 3 METER INPUT
To VCS 3 ATTACK.
VCS 3. +12v
DK2 CIRCUIT.
LADDER BUS
GATE BUS
HIGH END
* S.O.T. COMPONENTS
ALL 2N5163 Vp = 2.5 TO 3.0
C.N 116 NOV. 23.7.74
TRANSISTOR TYPE No's ADDED
ISSUE H
ELECTRONIC MUSIC STUDIOS
DK2
CIRCUIT DIAGRAM
22.0

DRG. No. 23/02		
ISSUE	ALTERATIONS	DATE

THIRD ANGLE PROJECTION



B Q14 & Q15 Re..
C10, 11, 12 add.
20 7. 7

C Q1 - Q19, ...
28. 9. 7

D ... changed.
8-4-73

E. ... (Q8, Q10, Q4 ...)
now BC258B
was 2N4288
30-4-73

F Auxiliary ...
added

G C.N. 6+
2. 6. '3

H was DK1
20.7.'

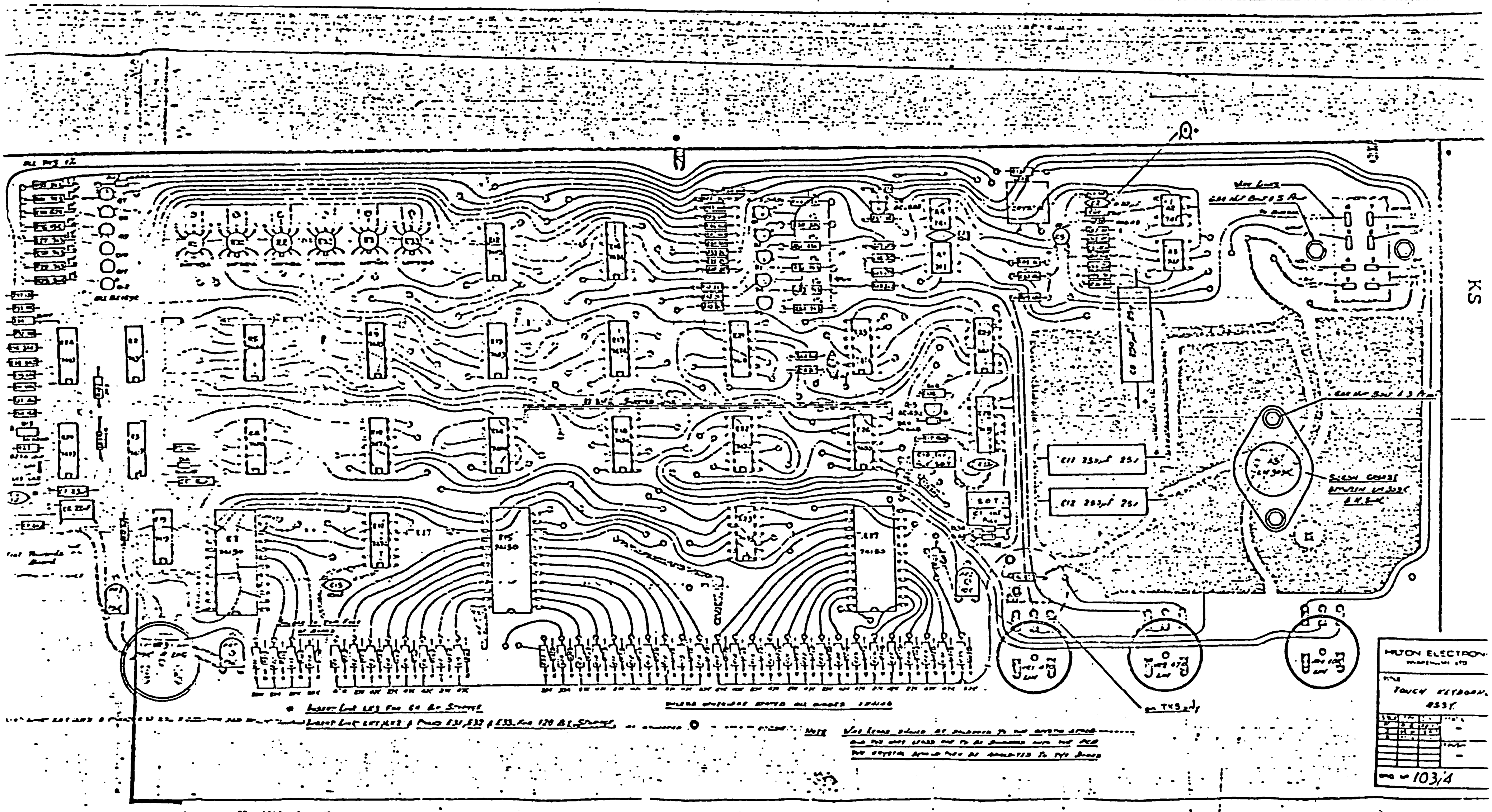
J. S.O.T. ...

ALL 2N5163 & 2N5457 SELECTED

Q1	2N5172
Q2	2N5163
Q3	2N5172
Q4	BC158B
Q5	BC158B
Q6	2N5172
Q7	2N5172
Q8	BC258B
Q9	2N5172
Q10	BC258B
Q11	2N5457
Q12	2N5163
Q13	2N5172
Q14	2N5172
Q15	2N5172
Q16	2N5163
Q17	2N5172
Q18	2N5163

NOTES.
1. C10 C12 & C8 TO BE MOUNTED ON TRACK SIDE
2. Q3, 4, 5, 13, 14 & 15 TO BE MOUNTED FLAT ON P.C.B.

TOLERANCE.			MATERIAL.	TITLE	USED ON				
	INCH	METRIC		COMPONENT LAYOUT DK 2		DRAWN	M.C.M	CHECKED	
3 FIGURE	±·005	—				DATE	12·9·70	APPROVED	
2 "	±·010	±·1				SCALE	2:1	TRACED	


KS
ELECTRON
TOUCH KEYBOARD
ASSY.
103/4