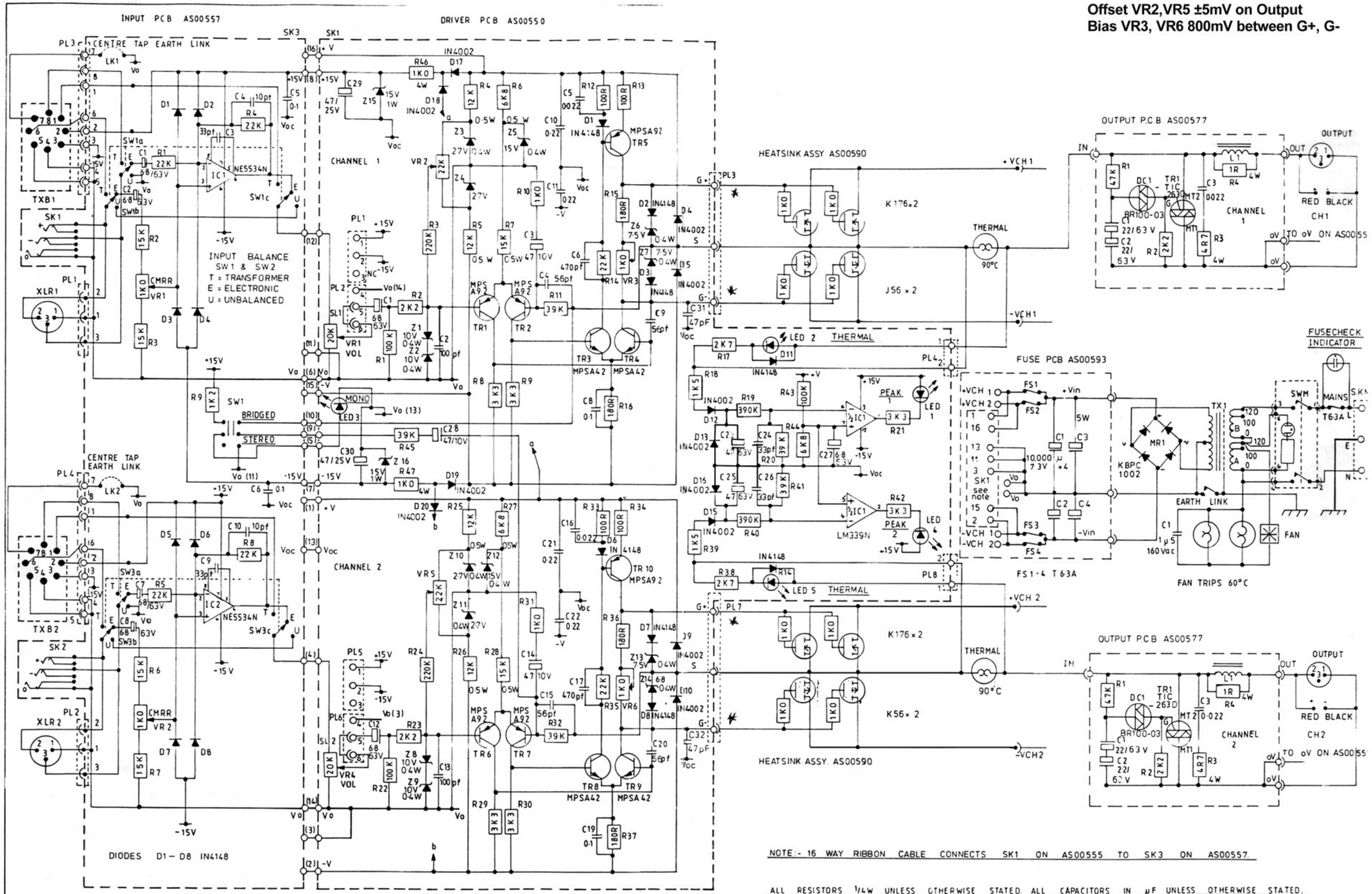
Offset VR2,VR5 ±5mV on Output
Bias VR3, VR6 800mV between G+, G-



ISSUE 4	ISSUE 3	ISSUE 2	ISSUE 1		DRAWN S. HOLMES.	DATE 6-8-85	MATERIAL –	TITLE CIRCUIT DIAGRAM	DRAWING NO
	AMENDED TO ACCOMODATE REVISE[illegible] TIONS OF C31 & C32	R21 & R42 ON DRIVER PCB AS00550 WERE 1K5 SEE CHANGE NOTE	C1 was 2µ2 changed to reduce fan idling speed	HH electronic	CHKD	SCALE –	FINISH –	VX-450	1630
	[illegible] SH	3/12/86 SH	31/10/86 SH		FILE –	TOL –			