3 THEORY OF OPERATION

3.1 System Overview

As shown in Fig. 3.1, the 224X is divided into 11 major functional modules:

1 Control Head
2 Transition
3 Single-Board Computer (SBC)
4 Nonvolatile Storage (NVS)
5 Timing and Control (T&C)
6 Data Memory (DMEM)
7 Arithmetic Unit (ARU)
8 Floating Point Converter (FPC)
9 Audio Input (AIN)
10 Audio Output (AOUT)
11 Power Supplies (PS1, PS2, and PS3)

Except for the control head, Transition module, and power supplies, all modules plug into an 8-slot card cage and are interconnected via a motherboard. The card cage and the power supply are contained in a mainframe. The control head is connected to the mainframe by a 25-conductor cable. The Timing and Control (T&C), Data Memory (DMEM), and Arithmetic Unit (ARU) modules comprise a dedicated, 293-ns-cycle, microprogrammed digital signal processor (DSP).

During normal operation, signal flow begins with the two audio input channels. The Audio Input (AIN) module filters, samples, and digitizes analog audio signals into 14-bit floating point representations (12-bit mantissa, 2-bit exponent). These floating point representations are then converted into 16-bit fixed-point two's complement numbers by the Floating Point Converter (FPC) module. The DSP processes this information and generates up to four independent channels of output data. This processed data is passed back to the FPC module, which reconverts it into floating point form. To generate the audio output, the Audio Output (AOUT) module reconstitutes four analog signals from the digital data stream.

The Single Board Computer (SBC) module is a controller that interfaces the control head to the DSP. The microprocessor (an 8080) on the SBC module scans the switches and pots on the control head and drives the control head displays. It processes the information received from the control head and changes the program running in the DSP. In addition, the SBC module performs various housekeeping tasks, such as power-up diagnostics and storing and retrieving nonvolatile user setups from the Nonvolatile Storage (NVS) module.

3.2 Control Head and Transition Module

The control head contains the switches and slide pots that allow a user to modify the control parameters of the reverberation and effects programs and control program access. In addition, the control head displays program and input signal level information.

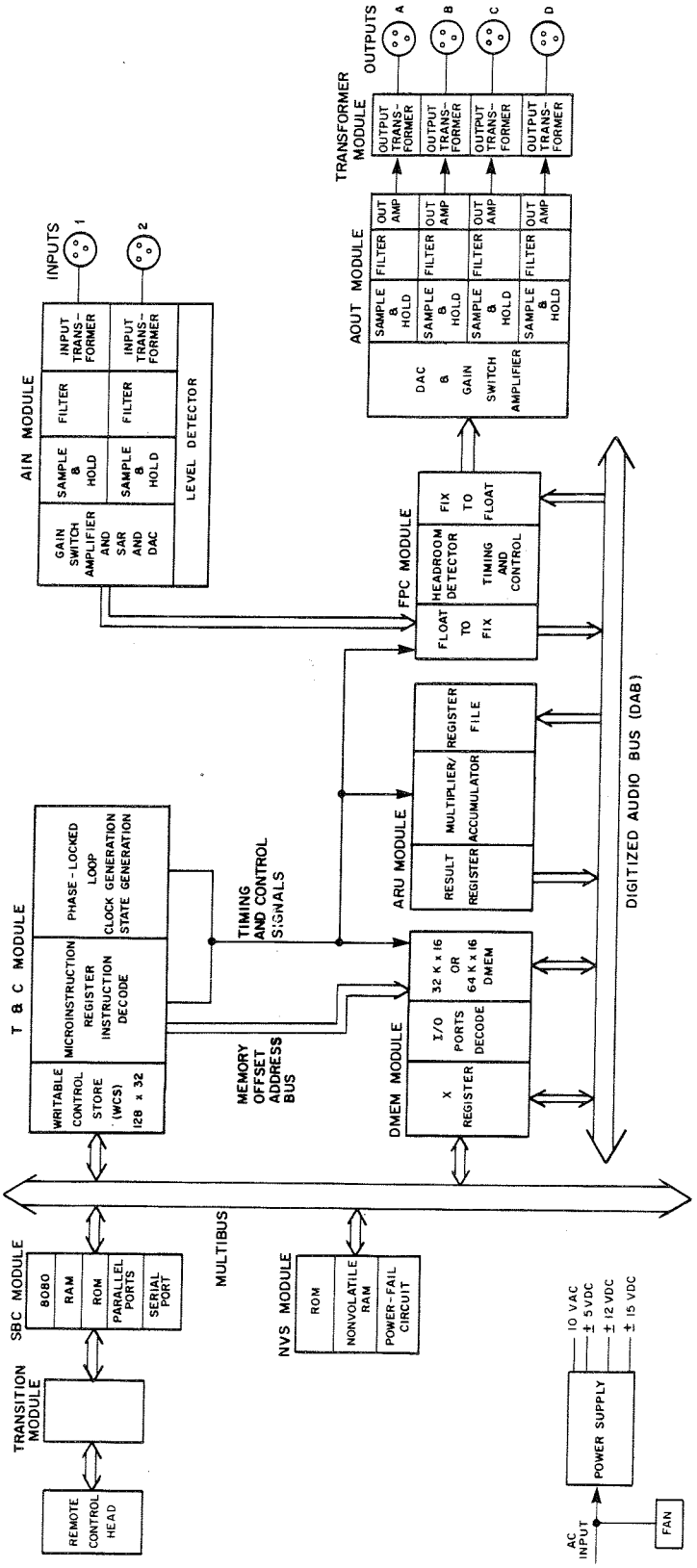


Fig. 3.1. Detailed Block Diagram -- 224X.

The control head consists of two board assemblies connected by a 27-pin flexible cable. The display and pushbutton board has three diodes, eight current-limiting resistors, switches, and LED displays. The second board contains all the remaining electronics, including the slidepots, and a 25-pin I/O connector. The I/O connector has 14 signal wires and two power wires. The rest of the 25 lines are used for digital and chassis ground returns. Ground returns are inserted between signal lines to prevent signal interference. The 14 signal wires connecting the control head to the mainframe consist of three groups of signals from three I/O ports on the SBC module: eight lines from port A form a bidirectional data bus; four lines from port B form a 4-bit address; two lines from port C serve as control signals. Table 3.1 lists the cable and connector wiring runs and tie points between the control head and the SBC module.

Table 3.1. Control Head to Mainframe Wiring.

25-pin Connector (Control Head to Mainframe)	50-pin Connector (Transition to SBC Module)	Function Name
1	2	GND
2	1	PB3
3	3	PB2
4	5	PB1
5	7	PB0
6	4, 6, 8	GND
7	*	GND (Chassis)
8	20	GND
9	21, 29	PC1
10	30	GND
11	25	PC0
12	26	GND
13	33	PA7
14	35	PA6
15	37	PA5
16	39	PA4
17	47	PA3
18	45	PA2
19	41	PA1
20	43	PA0
21	34, 36, 38, 40, 42, 44, 46, 48	GND
22	**	AC1
23	**	AC1
24	**	AC2
25	**	AC2

* Connected to chassis, not to SBC module.
** Connected to 10-Vac secondary, not to SBC module.

The control head interfaces with the SBC module through a 25-pin cable, with a transition at the mainframe to a 50-pin cable: this cable, in turn, connects to the J1 edge connector on the SBC module. The transition from 25 to 50 conductors is made through the Transition module, which is also used as an input point for the AC power to the control head, or 10-Vac power supply generated from a separate secondary of the power transformer. The 10-Vac power supply is fused to protect against cable shorts or similar faulty conditions.

Power Supply. The power supply for the control head consists of a full-wave bridge with filter and a 5-V 7805 regulator. The unregulated dc supply directly powers the LED displays.

Rectification at the control head allows power transmission to the control head without IR voltage drop in the ground returns, because a voltage drop in the ground returns would degrade noise margins and increase noise spikes in the logic signals.

Display Section. The display section is based on a scanned display concept in which all digits share a common segment drive. All digits use a common anode, and current flows through digit segments only if the cathode for that digit is grounded. The display and data transfer sections of the control head use as few interconnection wires as possible. The segment data comes out on port A; the 4-bit address selecting the digit comes out on port B; the control signals come out on port C.

The display cycle is controlled by software. At the end of a cycle, the eight lines of port A are used to send pot or switch data back to the SBC module. Addresses for the switches and pots are the same as for the respective digit just used during a display cycle. Table 3.2 lists the various display and read-back device addresses. The command sequences used are as follows:

```
ACTION

Load Digit, Port B
Load Segments, Port A
Set PC2/ (ACK/)
Set PC0 (STCONV)
Clear PC0
.
Delay Approximately 500 us
.
Clear PC2/
Set PC1/ (Read Enable)
.
Delay 12 us
Read Data
Clear PC1/
.
.
Select Next Digit
Repeat Sequence
```

Table 3.2. Control Head Displays, Pots, and Pushbuttons.

	Port B 4-Bit Addresses																	
	0		1		2		3		4		5		6		7		8	
	0000		0001		0010		0011		0100		0101		0110		0111		1000	
Port A 8-bit data bus	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write	Read
	Digit 0	Bass-Pot	Digit 1	Mid	Digit 2	Cross-over	LEDs	Treble Decay	LEDs	Depth	LEDs	Pre-Delay	LEDs	Push-button	LEDs	Push-button		Push-button
PA0	SEG a	LSB	SEG a	LSB	SEG a	LSB	PROG 1	LSB	IMED	LSB	SEC	LSB	L 0dB	PROG 1	R 0dB	IMED	---	BASS
PA1	SEG b		SEG b		SEG b		PROG 2		SET		MS		L 6dB	PROG 2	R 6dB	SET	---	MID
PA2	SEG c		SEG c		SEG c		PROG 3		CALL		Hz		L 12dB	PROG 3	R 12dB	CALL	---	CROSS-OVER
PA3	SEG d		SEG d		SEG d		PROG 4		SHIFT		kHz		L 18dB	PROG 4	R 18dB	SHIFT	---	TREBLE
PA4	SEG e		SEG e		SEG e		PROG 5		REG A		OVFL		L 24dB	PROG 5	R 24dB	REG A	---	DEPTH
PA5	SEG f		SEG f		SEG f		PROG 6		REG B		---		BASS-POT	PROG 6	TREBLE DECAY	REG B	---	PRE-DELAY
PA6	SEG g		SEG g		SEG g		PROG 7		REG C		---		MID POT	PROG 7	DEPTH	REG C	---	---
PA7	DP	MSB	DP	MSB	DP	MSB	PROG 8	MSB	REG D	MSB	---	MSB	CROSS-OVER	PROG 8	PRE-DELAY	REG D	---	---

A 74LS42 4-to-10 line decoder, controlling 75376 high-current drivers, selects digits. The LEDs are arranged into eight digits: 0, 1, and 2 correspond to the three 7-segment displays, and 3 to 9 are groupings of the various discrete LEDs on the panel. Refer to the schematics for details. 75327 driver arrays, current-limited with 150-ohm resistors, provide segment drive. The RDENB/ signal disables segment drive when pot or switch data is to be transmitted over the eight data lines.

Each time a display cycle is begun, a one-shot U2 fires to start the 75326 drivers for a period of several microseconds. If the SBC module becomes hung up in an unresolved operation, the one-shot times out, turning off all displays to prevent sustained high current (50 mA) from being drawn to any LED. The LEDs can run at high currents for only brief periods.

Slidepot Digitization. The control head uses an ADC-0817, which is a complete A/D subsystem capable of scanning up to 16 inputs and converting each input amplitude to an 8-bit binary code representation. A clock source, a start conversion pulse, and addresses are the only inputs. The ADC-0817 is used in a ratiometric configuration -- that is, the pot terminals and chip +REF (pin 19) are tied to 5 V, and the low terminals and ground (0 V) are tied to -REF (pin 23). The pots represent the complete range from -REF to +REF as a linear function of the position of the slidepots. The ADC translates this to 0000 0000 - 1111 1111 codes.

The start conversion pulse (STCONV) is filtered for noise rejection and routed to the start-convert and address-latch inputs of the ADC. The ADC synchronizes this command to its free-running input clock and begins a conversion cycle. Within 64 clock cycles, or 128 us, assuming a 500-kHz clock, the ADC-0817 completes the conversion and outputs the result at tristate outputs. An internal analog multiplexer selects the desired pot.

The clock to the ADC-0817 A/D converter is generated by a CMOS/RC free-running square-wave oscillator running at a nominal 500 kHz $\pm$150 kHz ($\pm$30%). The actual conversion time ranges from 70 to 130 us. When RDENB/ is LOW and the digit address is 0 through 5, data from the ADC-0817 outputs is gated onto the PA0-7 data bus. A tristate LS244 is used for this function.

Switch Data. The switches are all normally open pushbuttons arranged in three banks corresponding to digits 6 to 8. Germanium diodes 1N283 are used to isolate each bank or column of switches if more than one pushbutton is pressed at the same time.

The banks are wired into rows assigned to data lines PA0-7. Pull-up resistors ensure proper threshold for the tristate buffers. A complete bank or column of switches can be read when RDENB/ is LOW and the bank's digit line is selected. Any pushbutton pressed corresponds to data out onto the bus as a TTL logic "0". Refer to the schematics or Table 3.2 for details of pushbutton and pot assignments.

3.3 Single-Board Computer (SBC) Module

The SBC module is a National Semiconductor BLC-11 (or equivalent) using an 8080 microprocessor. It also includes 1K bytes of RAM at hexadecimal addresses 3C00 to 3FFF and supports four 5-V 2716 ROMs to provide a total of 8K bytes of ROM at hexadecimal addresses 0 to 1FFF.

The SBC module controls all functions of the control head, such as reading switches and slide pots, as well as data display. Its ROMs also contain the reverberation and effects software, which controls the DSP. The multibus provides the pathway for interaction between the SBC and the DSP. The software can be updated and expanded simply by replacing ROMs. The SBC module has three parallel ports and one serial port. The serial port is normally not used, but it has been configured as an RS-232 data set at 4800 baud (settable from 110 to 9600 baud).

Parallel port A is a bidirectional port and is used in mode 2. Parallel port B is used in mode 0 and provides four output bits used as an address to the control head. Parallel port C provides both control bits for port A and the control head.

3.4 Nonvolatile Storage (NVS) Module

The NVS module (sometimes referred to as the memory expansion module) provides nonvolatile memory consisting of (1) battery-backed-up RAM for the 36 user storage registers that hold customized reverberation and effects program variations, and (2) ROM storage expansion for the reverberation and effects software. The NVS module is contained on a single multibus-compatible board that plugs into the OPTION slot on the 224X card cage.

A NiCad battery backup powers the RAM of the NVS module to preserve the memory contents after power has been shut off. The RAM consists of four 1K x 4-bit RAMs (U5, U6, U12, U13) for a total of 2K bytes. It resides in memory address from hexadecimal 2000 to 27FF. The battery backup can protect the memory contents for as long as three months without recharging. All control head settings and register stores can be saved. The batteries are maintained at full charge by a trickle charger that operates when the 224X is turned on. The charger consists of a 78L05 that regulates the +12-V supply down to +5 V plus a diode drop. This voltage powers the battery supply Vbb via CR1 when power is on. The battery is charged via R16, a 270-ohm resistor. The batteries are fully charged after power has been on for 20 hours. An on-board detection circuit monitors the ac mains power and places the memory in protected store mode when a power outage is detected.

The 10-Vac power supply is conditioned to a TTL-compatible level to trigger the one-shot U21. Under normal power-up, the one-shots are continuously triggered, thus disabling the power-fail signal PFAIL. When a power failure occurs, the one-shot is not triggered and PFAIL will be activated. When PFAIL is activated, the write signals to the nonvolatile RAMs are disabled, preventing any accidental erasure to the contents. Part of the power fail circuitry is powered from the battery voltage Vbb to prevent any unpredictable behavior at power fail.

The ROM section of the NVS module has sockets for eight 2732-type 4K x 8 ROMs for storage of reverberation and effects software. The ROM resides in memory address from hexadecimal 8000 to FFFE. Memory location FFFF is mapped to a 4-position dip switch. (Thus the last byte in the last ROM cannot be read by the microprocessor.)

The dip switch may be preset to one of 16 code combinations, corresponding to 15 registers. The software reads the switch setting upon power-up to determine which register, if any, has been selected. By changing the switch settings, the 224X can power up with a predetermined program setup.

3.5 Timing and Control (T&C) Module

The T&C module contains the clock and state generation circuitry, 512 bytes of microprogram memory, an interface between the SBC module and the microprogram memory, and microinstruction decode and control signal generation logic.

The clock generation circuitry on the T&C module is synchronized to the SBC module by a phase lock loop. 02/ is the clock signal generated by the SBC module, running at 2.048 MHz. An MC4044, U27, forms the phase comparator and the low pass filter. The voltage controlled oscillator is formed by an LC tank oscillator, with a varactor, CR1, for voltage control. A divide-by-15 counter, U41, is embedded in the phase lock loop, making it a frequency multiplier of 15. Thus the master clock, MC, runs at 30.72 MHz. Since the LC tank oscillator output is divided by 2 by a J-K flip-flop, U26, to become MC, the oscillator actually runs at 61.44 MHz. This clock can be observed at TP2 (OSC). MC is driven from a Schottky nand gate, U40, with an active pull-up, Q3.

The state generation circuitry consists of a divide-by-9 counter, U56, and an 8-bit shift register U39. Thus the system clock period is at 3.41 MHz, i.e., 293 ns, which is divided into nine time slots, MS0-MS8. These nine time slots are grouped into three, AS0, AS1, and AS2 by U38, U25, and U23. Refer to Fig. 3.2 for the basic timing of the T&C module.

The control signal generation is achieved through a writable control store (WCS), formed by four 128 x 8 static RAMs (U2, U15, U29, U43). The WCS is cycled by an eight bit program counter (U1, U14). A 100-step control program is allowed, giving a sampling rate of 34.13 kHz. Thus the counter is normally reset at count 99 by a RESET signal that is generated by the WCS itself. The WCS program is loaded from the SBC module. Thus the address from the counter is multiplexed with the address from the SBC module. The bidirectional data bus to the WCS is buffered by bidirectional drivers, U3, U16, U30, U44, to the SBC module.

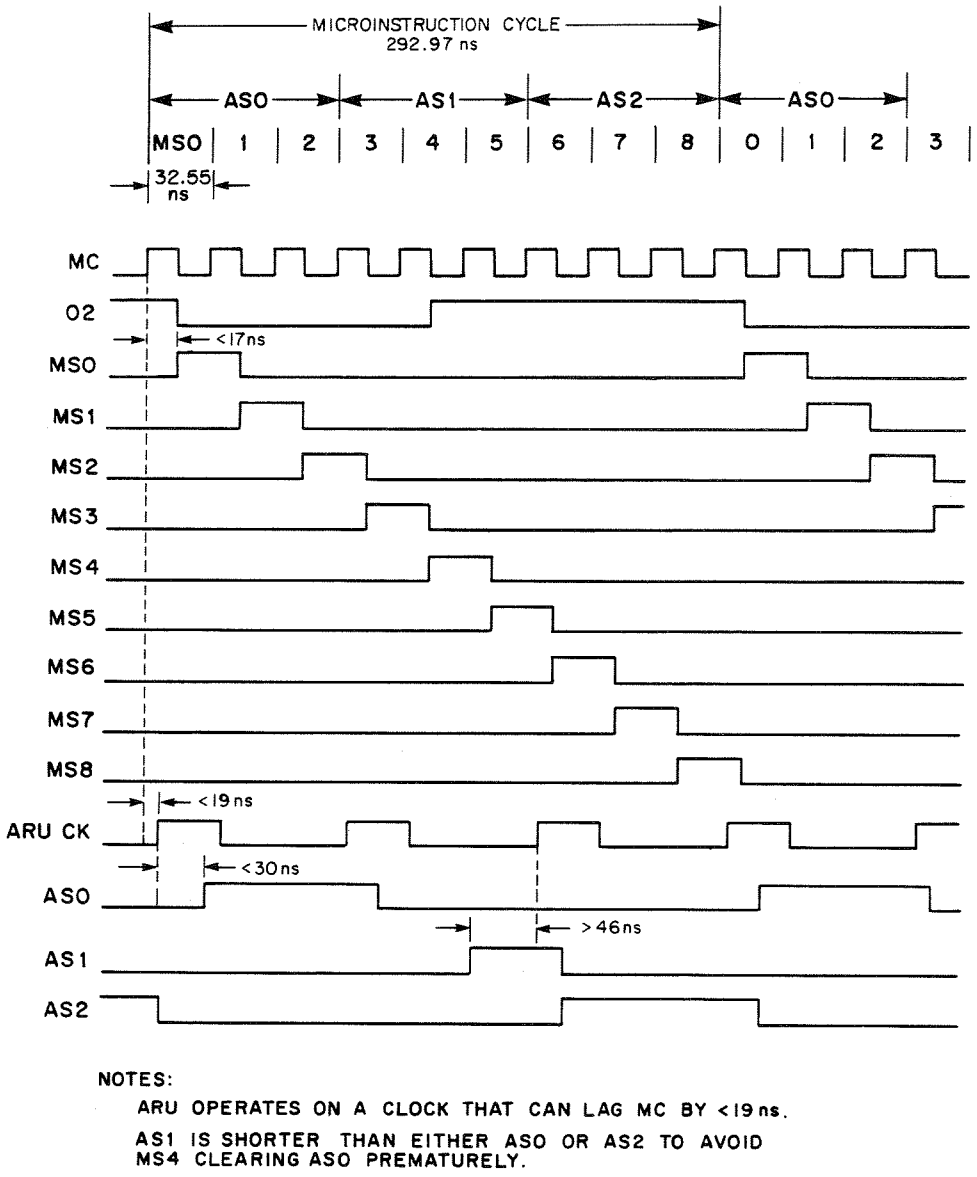


Fig. 3.2. T&C Module Timing.

The least significant 16 bits of the WCS word are normally used as an address for the data memory. The remaining 16 bits contain the multiplier coefficient, the register file addresses, and miscellaneous control signals. They are clocked by a 32-bit microinstruction register, U4, U5, U17, U18, U31, U45. The upper 16 bits of the microinstruction register are formed by 74S163 counters for the synchronous clear functions that they provide. The upper 16 bits of the microinstruction register are cleared whenever the cycle is used by the SBC module in accessing the WCS, since the data on the microinstruction bus, MI0-MI31, may not be valid. The microinstruction word is set up such that all zeros correspond to a no-operation. The lower 16 bits of the microinstruction word can be "don't cares," since they represent only an address.

The remaining control signal generation circuitry consists of decoders (U47, U48, U49, U32, U34), which generate the control signals that are encoded in the instruction word; register U19, U20, which further pipelines and synchronizes the required control signals; and flip-flops U24, U22, U21, U20, which generate more complicated control signals from the basic timings MS0-MS8. The multiplier coefficient from the microinstruction word, C0/ to C5/, is serialized into an even and an odd stream, M0/ and M1/, by shift registers U10 and U11 for the serial multiplier in the ARU module.

The access to the WCS from the SBC module is decoded by U50 and synchronized by U52 and U53. Since the multibus is an asynchronous bus, an acknowledge signal to the SBC module, XACK/, is generated by U54. The WCS can be accessed from the SBC module in two modes. First, the DSP can be halted by stopping the program counter (U1, U14) by asserting HALT/. In this mode, the SBC module can read from and write to the WCS anytime. The WCS is mapped into hexadecimal address locations 4000 - 41FF of the SBC module address space. The decoder U46 decodes the least significant two bits of the address from the SBC module to select one out of the four 128 x 8 bit static RAMs and the corresponding bidirectional drivers. Alternatively, the SBC module can also access the WCS while the DSP is running, allowing it to change program characteristics on the fly. In this mode, a protect bit in the microinstruction determines when the SBC module can access the WCS. The program must be organized such that the microinstruction, which is displaced during an SBC access, is a no-operation. Normally, the SBC module only writes into the WCS in this mode, which only takes up one microinstruction time. Reading from the WCS in this mode can take up to three microinstruction times. In this mode, a flip-flop, half of U53, is used to attempt to synchronize pairs of SBC module accesses in the same sample time: an allowed access slot not utilized will disable the next access slot.

Finally, there is some diagnostic hardware included in the T&C module. Three groups of eight timing control signals can be read by the SBC module via tristate bus drivers, U6, or registers U7 and U8. The DSP is halted when these diagnostic ports are being read. In the registers U7 and U8, the signals being read are dynamic and thus need to be sampled by appropriate clocks. Note that the digital overload signal SAT is also read through one of these diagnostic ports, U8. This allows the SBC module to detect when digital overflow has occurred in the ARU module. The SAT signal is first clocked through a flip-flop. Then it triggers a one-shot since the SAT signal can be transient. When the overflow is continuous, the one-shot is not triggered. Thus the SAT signal is OR-ed with the output of the one-shot, which is then read by the SBC module. U9 forms a shift register to perform a serial-to-parallel conversion of the four serial bit streams S0, S1, M0/, M1/ to be observed. Exclusive or gates U12 minimize the hardware needed to observe the bit streams. ARUCK fires one-shot U13, the output of which drives an LED on the edge of the board. This gives a preliminary indication of whether the clock is running. Another test point TP1 is available for test synchronization purposes.

3.6 Data Memory (DMEM) Module

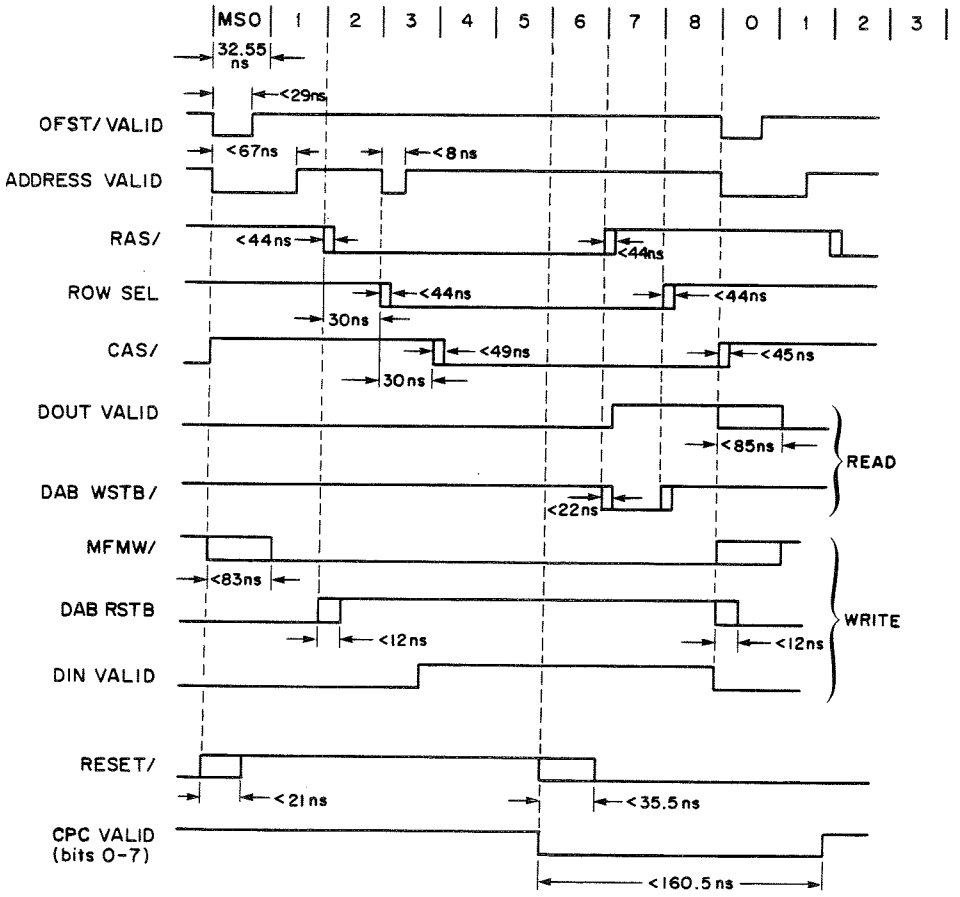
The DMEM module contains the data memory, control signal and address generation circuitry, the XREG (DMEM transfer register), diagnostic ports, and the 8080 port-decoding circuitry. The DMEM communicates with the rest of the system over the digitized audio bus (DAB).

The address to the data memory coming from the microinstruction is in the form of an offset relative to a current position in memory. This current position is held by a 16-bit current position counter (U51 and U65) and is normally incremented once every sampling interval. The absolute address of a memory reference is computed by subtracting the offset from the current position. A 2's complement subtraction is performed by adding the complemented 16-bit word, OFST/, to the output of the current position counter and tying the carry input of the adder (U49, U50, U63, and U64) high. A multiplexer (U18 and U36) is used to multiplex the resulting address onto the seven address lines of the 16K dynamic RAMs. The circuitry is set up such that either 2 banks of 16K dynamic RAMs or 1 bank of 64K dynamic RAMs can be used. The address and control lines of all the RAMs are tied together. Because the RAM outputs are capable of fanning out to 10 low-power Schottky TTL loads, they are tied directly to the DAB without buffering.

The timing and control signals for the DMEM modules are generated by a delay-line circuit (U59) based on signals supplied by the T&C module MEMAC, DABSTB, and MEMWR. Refer to Figure 3.3 for the data memory timing.

In addition to the data memory circuitry, the DMEM module also contains some decoders (U55, U56, U57) which are used to generate the strobes used in the I/O access of the ports used in various modules in the DSP from the SBC module. The open collector-gate U52 is used to return an acknowledge, XACK/ to the SBC module after an I/O access. The nand gates U53 and U54 are used to implement the single cycle/halt/run control modes of the DSP. The module can single cycle, halt, or let continue run the DSP through accessing these latches via the I/O ports.

Some diagnostic circuitry is also included on the DMEM module. The tristate bus drivers U48 and U62 are used to enable the SBC module to read the OFST/ lines when they are static. U42 forms the bus test register, which enables the SBC module to sample and read its own data bus DATA/ on the DMEM module. U38, U39, U40, and U41 form the X register, which enables the SBC module to read from and write to the DAB. U38 and U40 are used to send data from the DAB to the SBC module and U39 and U41 are used to send data from the SBC module to the DAB.



NOTES:
CAS/ FALLS ONLY WHEN MEMAC IS HIGH, INDICATING MEMORY OPERATION.
CRITICAL TIMING PATH FOR DIN IS XFER CK TO RESULT REGISTER OF ARU.

Fig. 3.3. DMEM Timing.

3.7 Arithmetic Unit (ARU) Module

The ARU consists of a 4 x 16-bit register file, a 16 x 6-bit 2's complement multiplier with saturation logic, a 20-bit accumulator, and a 16-bit result register. The 4 x 16-bit register file acts as a temporary store for the multiplicands taken from the DAB. The source of the multiplicand can thus be from the FPC module, DMEM module, the SBC module via the X registers on the DMEM module or even from the result register. The multiplier performs a 16 x 6-bit multiply and accumulate every system clock time (i.e., 293 ns). The 6-bit multiplier coefficient and the control signals to the multiplier are generated from the T&C module. The result register acts as a buffer between the outputs of the multiplier and the DAB, allowing the multiplier to perform the next multiplication without having to wait for its previous result to be read by the other parties on the DAB. In a similar manner, other parts on the ARU are pipelined to maximize the operating speed of the essentially serial multiplier through the register file, the partial product register, and the accumulator.

The 4 x 16-bit register file (U29, U30, U31, U32) has independent write addresses (WA0, WA1) and read addresses (RA0, RA1), which are controlled by the microinstruction. In this way, data on the DAB can be written into the register file at one address while data at another address can be read by the multiplier. Note that the write signal to the register, DAB WSTB/, is active every system clock time (293 ns) although the data on the DAB is not always relevant. Address 3 in the register file is used as a pass-through location in these instances.

The multiplier is implemented by a modified shift and add serial multiply technique. Instead of the normal shift and add, two shifts and adds are performed at the same time such that the multiply is twice as fast. A system cycle time (293 ns) is divided into three ARU states: AS0, AS1, and AS2. During each of these states, a double shift and add is performed. This gives a 6-bit multiply in a system cycle time. The double shift is performed by a "dual rank" shift register (one which shifts by two bits at a time) (U3, U4, U15, U16, U17, and U18). The double shift is performed by interleaving the bits to two sets of the shift register: U4, U18, and U15 form one shift register that receives the even-numbered bits, and U3, U17, and U16 form another register that receives the odd-numbered bits. In the first ARU state, AS0, the contents of the register file are simply loaded into the shift register. The output of the shift register is split into two groups: one is the direct output and the other the output shifted right by one bit. Depending on the 6-bit multiplier coefficient from the microinstruction, which is serialized into bit streams M0/ and M1/ in the T&C module, these two are blanked or added to the other (by the nand gates U14, U26, U27, U28, U40, U41, U50, U51, U52, and U53). The result is loaded into the partial product register (U10, U11, U12). Note that the adder forming the partial products is used as a negative logic adder because the nand gates provide an inversion, and the carry input of the adder is tied high. This inversion is taken into account by the following stage of exclusive or gates.

The partial product register acts as a pipeline register for the second stage of addition. As the double shift and add circuit previously described proceeds to perform another double shift and add in the second ARU state, AS1, the partial product is added to the accumulator. The outputs of the partial product register are passed through a set of exclusive or gates (U5, U6, U7, U8, and U9) controlled by the sign bit of the multiply CSIGN/. Depending on the logic state of CSIGN/, the data can be negated by inverting the data and tying high the carry input of the adder that follows. U19, U20, U21, U22, and U23 form the adder that adds the partial product to the accumulator.

Overflow in the ARU has to be handled properly. In this system, saturation arithmetic is performed. In the event of a positive or negative overflow, the most positive number or the most negative number is forced in place of the overflow number. This is implemented by the most significant two bits in the 20-bit data path within the multiplier. It should be noted that, in forming the 20-bit word to the multiplier from the 16-bit data from the register file, the most significant bit of the 16-bit word is the two most significant bits in the 20-bit word and the

least significant three bits of the 20-bit word are tied to zero. Thus, the most significant two bits of the 20-bit word should always be the same unless an overflow has occurred. This condition is detected by exclusive or gate U42. This would force the multiplexors (U33, U34, U35, U36, and U37) to select either the most positive or the most negative numbers, depending on the MSB of the overflow number. The accumulator is formed by 4-bit counters 74LS163s (U45, U46, U47, U48, and U49). The counting function is not used, however; only the synchronous load and clear functions are used.

Because of pipelining, the final result of the multiply and accumulate does not become available until the very end of AS0 of the next system cycle. If a transfer to the result register command is present in the microinstruction, the result register is loaded at this time by XFER CK. If the zero accumulator command is given, the accumulator is also cleared at this instant. Refer to Fig. 3.4 for the ARU module timing.

3.8 Floating Point Converter (FPC) Module

The FPC module serves as an interface between the DSP and the two analog modules: AIN and AOUT. For the DSP, the analog I/O looks simply like another device that can be read from and written into via the DAB. For the analog modules, the FPC module is the source of the timing strobes and clocks that direct the A/D and D/A conversion processes. In addition, the FPC module is responsible for making the floating point/fixed-point translation required for communication between the two analog modules and the DAB.

The FPC module has four major functions:

1. Timing and control generation
2. Input floating-to-fixed-point conversion
3. Output fixed-to-floating-point conversion
4. Headroom level indication.

Timing and Control Generation Circuitry. Besides supplying its own timing and control signals, the FPC module generates the timing and control signals for the analog modules. It generates these signals based on several signals from the T&C module: FPC CK, which occurs every system clock time (293 ns), provides the basic clock; RESET/, which occurs every sample time (29.3 ns), synchronizes the timing cycles; RD AD/ and WR DA/, which control the reading from and writing to the floating-to-fixed-point circuitry. The timing and control signals are generated by an 8-bit input cycle counter (U7 and U8), which drives a 256- x 4-bit ROM (U6). Some of the outputs of the ROM are deglitched by a register (U18), and some are directly used as timing and control signals. Because 100 system clock times occur in each sample time, only the first 100 locations of the ROM are used.

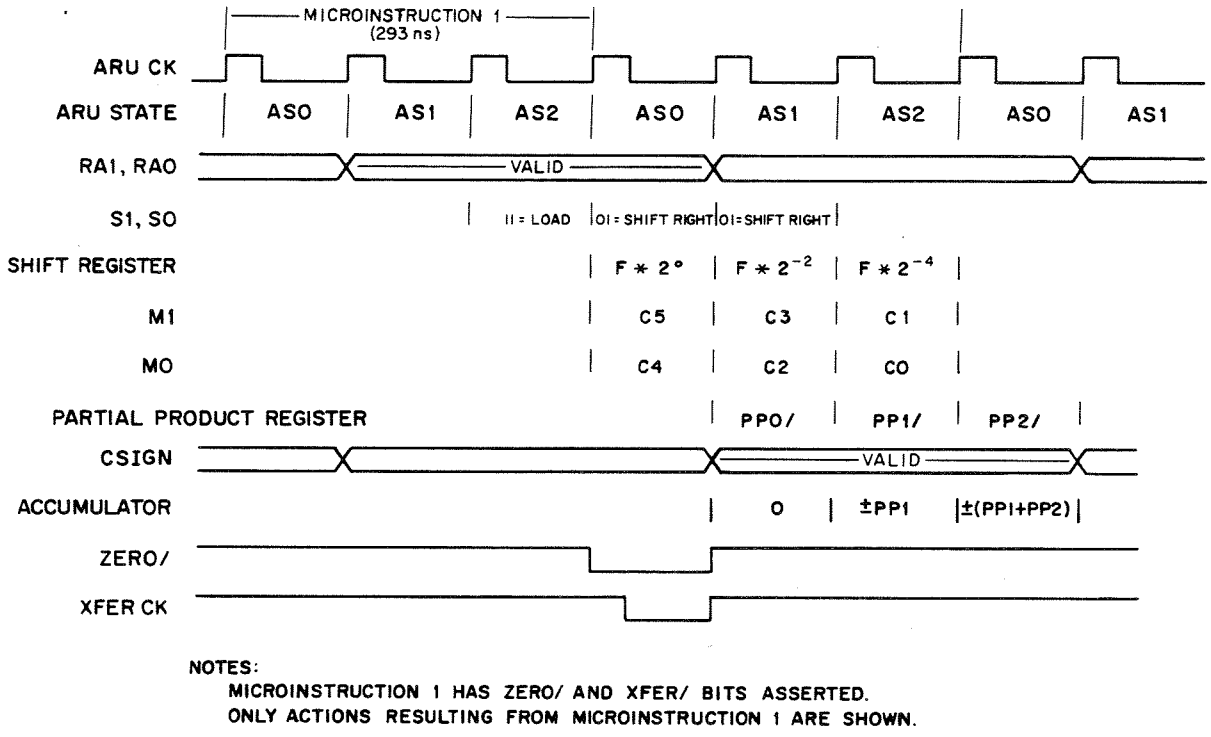


Fig. 3.4. ARU Module Timing.

Two multiplexors (U4 and U42) implement a self-test mode in which the FPC CK signal is replaced by 02/, the SBC system clock (488 ns) and the RESET/, RD AD/, WR DA/, and the output channel select signals SDAA, SDAB< SDAC< SDAD, are substituted by signals decoded from the counter by nand gates (U5).

The select signal to the multiplexors, FPC DBUG, is tied low in the T&C, ARU, and DMEM modules. Thus, when these modules are removed, the FPC DBUG signal floats high and the self-test mode is automatically activated. In the self-test mode, the only external signal needed is the 02/ clock. The input from the left channel is immediately transmitted to the output channels A and B via the FPC module. Similarly, the right channel is transmitted to channels C and D. In this way, the FPC, the AIN, and the AOUT modules can be checked independently of the DSP. However, in using the 02/ signal from the SBC module, the sampling frequency changes from 34.13 kHz to 20.48 kHz. To obtain the correct sampling rate, the SBC module must be removed also and a 3.413-MHz TTL-compatible input clock must be supplied to pin A28 of the backplane connector using a signal generator.

Input Floating-to-Fixed Point Conversion Circuitry. At the beginning of a sample cycle (starting with state 0 of the input cycle counter), the successive approximation register (SAR) on the AIN module is instructed to start an input conversion by bringing STCONV/ signal high and sending thirteen clock pulses on the CNVCK signal. Just after the twelfth clock pulse, the SAR contains valid input data. The LOAD signal to the shift registers (U27, U28, U38, and U39) is then brought high, loading the input data into the shift registers. STCONV/ is brought low again and the thirteenth clock pulse on the CNVCK resets the SAR, readying it for the next conversion.

Shift register U27, U28, U38, and U39 and counter U16 perform the floating-point-to-fixed-point conversion. Note that the LOAD signal is asserted for two clock pulses. The first clock pulse loads the input gain counter, U16, with the input gain bits IGA1 and IGA0. Because a one is also loaded into bit 2 of the input gain counter (U16 pin 12), which is connected to the S1 input of the shift register, both S1 and S0 of the shift register are high for the second clock pulse, causing it to load the 12 bits from the SAR. When LOAD returns low, the input gain counter counts up, and the shift register shifts left until QC QB QA = 000. Gain bits of 00 result in four shifts; 01 results in three shifts; 10 in two shifts; and 11 in one shift. By the fourth clock pulse following the falling edge of LOAD, the Channel 2 conversion is complete. Tristate drivers U25 and U26 enable this data onto the DAB when the DSP asserts the RD AD/ line. Meanwhile, CH1L (a signal derived from CH1 on the AIN module) goes high, causing an input channel switch. A similar conversion for Channel 1 takes place during the second half of the input conversion cycle. Refer to Fig. 3.5 for the floating-to-fixed-point conversion and A/D conversion cycle timing.

Output Fixed-to-Floating-Point Conversion Circuitry. The 4-bit register, U40, and the 16-bit register, U36, U37, comprise a double buffer that stores the output channel select code, SDAA-SDAD, and the 16-bit fixed point output value from the DSP, respectively. When the DSP signals an output to the D/A by asserting WR DA/, the double buffer is loaded and NEW DAT/ (U3 pin 6) is asserted, indicating that the double buffer is full. At the next clock pulse, BUSY from the strobe counter, U1, U2, is inspected. If BUSY is high, indicating that a D/A conversion is currently taking place, nothing happens. If BUSY is low, the 16-bit data stored in the double buffer is loaded into shift register U23, U24, U34, U35; the 4-bit select code stored in the double buffer is loaded into register U41; and the flag NEW DAT/, is deasserted, indicating that the double buffer is ready for the next output value. NOR gate U14 pin 1 ensures that this flag is not deasserted if the DSP reloads the double buffer, just as the old information in the double buffer is loaded into the shift registers.

When the shift register is loaded, strobe counter, U1, U2, and output gain counter U43 are loaded, initiating an output cycle. Refer to Fig. 3.6. The output gain counter counts up from zero and the shift register shifts left until NOR gate U14 pin 4 detects one of two conditions: (1) The sign bit is about to be shifted out of the shift register (that is, the two MSBs disagree). When STOP/ goes low, the fixed-to-floating-point conversion is complete. (2) The counter has incremented three times.

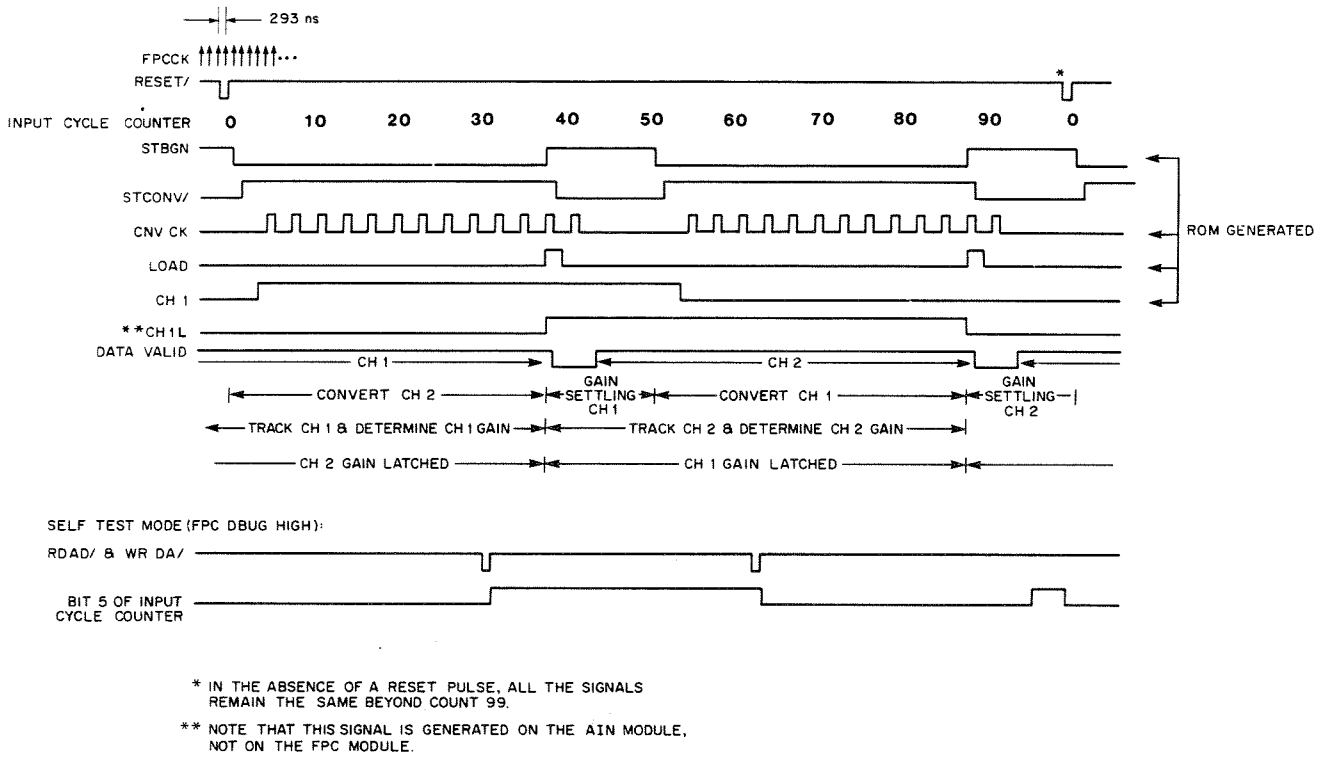


Fig. 3.5. Floating-to-Fixed-Point Conversion and A/D Cycle Timing.

The two LSBs of the output gain counter are transmitted to the gain switch amplifier (GSA) on the AOUT module as output gain bits OGA1, OGA0. Meanwhile, the strobe counter has been counting up from its initially loaded value of hexadecimal 2A. After allowing enough time for the fixed-to-floating-point conversion to complete and then enough time for the GSA and D/A converter on the AOUT module to settle, flip-flop U3 pulses the multiplexor enable U42 pin 15, thereby strobing the appropriate output line OUTA-OUTD.

Headroom Level Circuitry. The headroom level information is sent to the FPC module from the AIN module, where rectifiers and comparators generate a 5-bit code representing the instantaneous levels of the analog inputs. Because this information is multiplexed between the two input channels, the FPC module demultiplexes it by clocking two headroom registers, U31, U32 and U21, U20, on opposite edges of the channel select signal, CH1. Peak detection occurs by clearing a register bit any time the corresponding headroom bit is asserted. What remains in the register, then, is the complement of the largest headroom word that has occurred since the register was initialized. The SBC module reads a headroom register by strobing either HR1/ or HR2 low, enabling the tristate drivers U19 or U30 onto the SBC module data bus. The rising edge of the strobes trigger a one-shot, which initializes the corresponding headroom register.

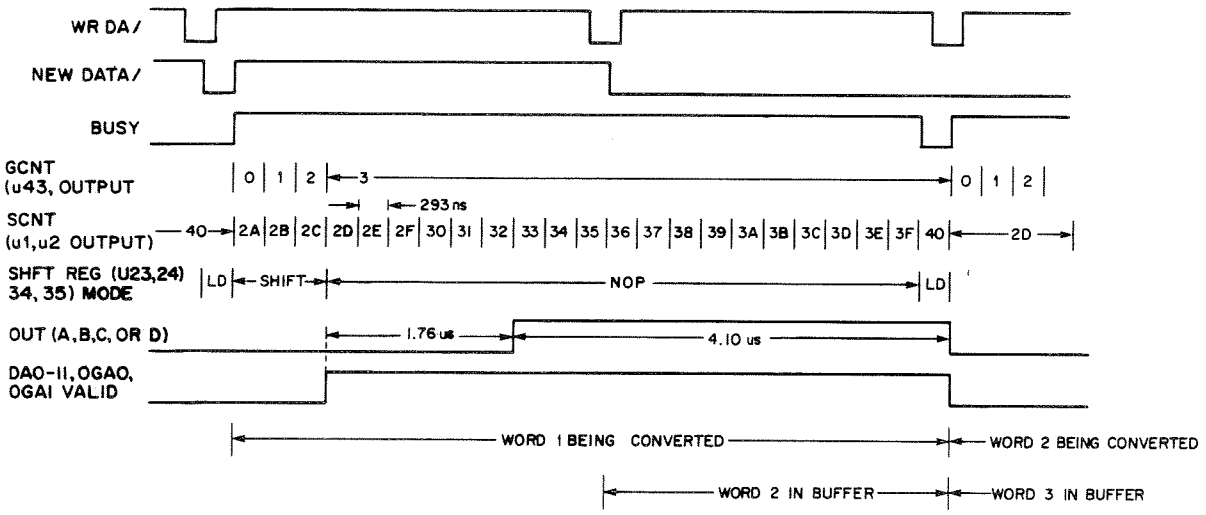


Fig. 3.6. Fixed-to-Floating-Point Conversion and D/A Cycle Timing.

3.9 Audio Input (AIN) Module

The AIN module gain conditions, filters, and digitizes two input channels of audio signals in a floating point format. The major subsections of the module are:

1. Input gain conditioning and filtering
2. Sample-and-hold and multiplexer circuits
3. Gain ranger
4. Analog-to-digital converter (ADC)

Input Gain Conditioning and Filtering. Inputs are transformer-coupled and then gain-conditioned by a buffer stage with an adjustment range of 15 dB. The nominal level at the output of buffer stage U1 is +13 dBm (5-V peak) at 1 kHz. This amplitude corresponds to the onset of clipping in the ADC. Diode clamps prevent overloading the input stage of U1.

The input filters are 7-pole active elliptical (or Cauer) networks synthesized from "FDNR" networks. The nominal cut-off frequency for the input filters is 15 kHz to prevent aliasing distortion at a sampling rate of 34.13 kHz. The next stage is a shelving preemphasis network with 50-us

and 12.5-us time constants. The last filter stage provides aperture correction to compensate for the slight amount of high-frequency loss introduced by the sampling process.

Sample-and-Hold and Multiplexer Circuits. The input sample-and-hold (S&H) circuits are designed so that when one channel is tracking, the other channel is in hold mode. Control signal CH1L places U20 in hold mode when HIGH, simultaneously placing U21 in tracking mode. Analog switch U22 is controlled by HLCH1L, an inverted and level-shifted version of CH1L. This switch is configured so that the "held" channel is commutated to the gain switch amplifier (GSA) stage.

Gain Ranger. Both filtered channels are sent to precision full-wave rectifier circuits that give a positive output equal to the peak amplitude of their inputs. The rectified output of the tracked channel is routed by analog switch U14 to an amplitude quantizer made up of five comparators biased at 5.0 V, 2.24 V, 1.12 V, 0.56 V, and 0.280 V, respectively. These thresholds are arranged so that 5 V corresponds to the onset of clipping in the ADC, and each of the lower thresholds is 6 dB apart and allows determination of the optimum gain to be used for the GSA. Table 3.3 shows how the proper gain is selected for signals of various amplitudes.

Table 3.3. Comparator Outputs Showing Selected Gains for Various Signals.

Signal	U15-13 (5.0 V)	U15-1 (2.2 V)	U15-2 (1.12 V)	U16-1 (560 mV)	U16-2 (280 mV)	GAIN A (dB)	IGA1	IGA0
>5.0 V	0	0	0	0	0	0	0*	0*
2.24-5.0 V	1	0	0	0	0	0	0	0
1.12-2.24 V	1	1	0	0	0	6	0	1
560 mV-1.12 V	1	1	1	0	0	12	1	0
280 mV-560 mV	1	1	1	1	0	18	1	1
<280 mV	1	1	1	1	1	18	1	1

*Comparator outputs are decoded and latched to provide gain-control signals IGA0 and IGA1.

The 5-V and the 280-mV comparator outputs are needed for headroom display only, while all of the additional comparators provide gain-change information as well as headroom display. A gain of 6 dB is added whenever a signal falls below 45% of the clipping level. A signal level falling to 45% of the clipping level would then be increased by a factor of two to

about 90% of clipping level to take full advantage of the ADC's usable dynamic range. The technique of gain ranging used here is commonly referred to as "instantaneous floating point conversion" -- that is, an appropriate gain is selected just before converting each sample. The gain thus follows the envelope of the converted signal.

Excellent signal reconstruction can be achieved if the ADC is properly offset to deliver a zero code for 0-V input. Good gain matching is provided by using a precision resistor network to set the gain of U23. The resistor feedback ratio is selected by analog switch U24. Because U24 conducts negligible current, errors resulting from switch resistance are also negligible. U24 also provides a decode function for gain bits HLG0 and HLG1. Voltage offset in this stage is not important, provided that it is proportional to gain. Maximum offset due to accumulated errors should never exceed 80 mV at this output stage.

Analog-To-Digital Converter. The analog-to-digital converter (ADC) is a 12-bit successive-approximation type. A 12-bit current output digital-to-analog converter (DAC) is sequenced by a successive approximation register (SAR) chip, U26. This device receives its start command (STCONV) and conversion clock (CNVCLK) from the FPC module. An LM211 comparator is used to compare the DAC's output with the input signal. The output of this comparator is used as the input to the SAR.

3.10 Audio Output (AOUT) Module

The AOUT module provides four output channels serviced from a single timeshared DAC and gain switch amplifier. The AOUT module has four major subsections:

1. Digital-to-analog converter (DAC)
2. Gain ranger
3. Demultiplexor and sample-and-hold circuits
4. Filtering and output gain conditioning

Digital-to-Analog Converter. The DAC, U2, is updated by 12-bit word DA0 to DA11. The DAC responds with an analog output in the range of -5 to +5 V.

Gain Ranger. Gain control is set by two bits, OGA1 and OGA0, which control analog switch U3. U3 selects one of four taps from precision divider network RD2. Gain selection is either 1, 1/2, 1/4, or 1/8 $\pm$0.05%. U4 operates as a high input impedance follower to prevent loading of the attenuator network.

Demultiplier and Sample-and-Hold Circuits. The corresponding channel-selection signal OUT A, B, C or D goes high approximately 1.76 us after DAC and gain data become valid. This delay allows time for the DAC and GSA to stabilize before placing the selected output sample-and-hold in the sample mode. The OUT (sample) command is valid for approximately 4.08 us. During this time, U6 switches the output gain-conditioned DAC voltage to capacitor C13, 16, 17, or 20. U7 and U8 provide high impedance buffering to prevent discharge of the sample capacitors during the hold period.

The +7- and -7-V CMOS switch bias is provided by zener diode regulators, CR5 and CR6. Power-on muting is provided by transistor Q9, which is held off for several seconds after power is applied. R159 charges a 22-uF capacitor from -7 to +7 V. Saturation of Q9 places a ground signal on pin 6 of U3, enabling U3 to pass signal.

Filtering and Output Gain Conditioning. Output deemphasis is provided by stages U13 and U21. Filtering is provided by 7-pole elliptical (Cauer) filters. Adjustments to compensate component sensitivity are provided for each section. These settings should never need adjustment if related components are not changed.

The output stage consists of a level adjustment potentiometer and an opamp stage with a complementary output transistor buffer for each channel. Overall, negative feedback is provided around the stage to maintain fixed gain and provide low distortion. A loading network is also provided to maintain high-frequency stability. Each output stage drives an output transformer on the audio transformer board at the rear of the chassis with the audio I/O connectors. The output transformer provides a voltage gain of about 2.5.

3.11 Power Supplies

The three 224X power supplies produce six regulated dc voltages and one unregulated ac voltage.

+5-V and -5-V Power Supplies. The +5-V and -5-V power supplies are derived from a single secondary winding fused in both legs by a pair of 15-amp slow-blow fuses. The +5-V power supply consists of a uA723 regulator, a current boost transistor, and a pair of high-current pass transistors. The regulator is a current foldback design that limits short-circuit currents to less than 3 A.

Over-voltage protection is provided by a crowbar circuit. The +5-V power supply is designed to provide a continuous 10 A. Both voltage and current limits are adjustable.

The -5-V power supply is a 7905 monolithic regulator fused at 2.5 A. This power supply is both current-limited and thermally protected. It is designed to provide 250 mA.

+12-V and -12-V Power Supplies. The +12-V and -12-V power supplies are derived from a single secondary fused in both legs by a pair of 3-A slow-blow fuses. The +12-V power supply consists of a LM317K monolithic voltage regulator controlled by a pair of 1% resistors. This power supply is both thermal- and current-protected, and provides 1.25 A. The -12-V power supply is derived from a 7912 monolithic voltage regulator that is both thermal- and current-protected, and provides 150 mA.

The +12-V power supply is interlocked with the -5-V power supply so that +12 V is not available until after -5 V is available. Should any problems occur with the +12-V power supply, check to be sure that the -5-V power supply is available.

+15-V and -15-V Power Supplies. The +15-V and -15-V power supplies use a tracking design that allows the -15-V power supply to track the +15-V power supply. Both are derived from a single secondary fused in both legs by a pair of 2-A slow-blow fuses. The +15-V power supply is an LM317 monolithic voltage regulator incorporating an adjustable resistor network.

The -15-V power supply is a 7912 controlled by an LM301 opamp that senses the difference between the +15-V and -15-V outputs and forces the -15-V output to track the +15-V output. A balance control is provided to trim the -15-V output. The ±15-V power supplies are not ground-referenced to the ±5-V or ±12-V power supplies unless the analog boards are installed in the 224X chassis. All voltage measurements must be referenced to the correct ground. The ±15-V power supplies provide 750 mA and are current and thermal protected.

Mains Circuit. The mains circuit for the 224X uses a dual primary transformer with 120-V and 100-V taps (a pair of DPDT switches select the operating voltage: 100, 120, 220, 240 V). This supply is switched on both sides of the line. A primary fuse is provided on the chassis ahead of the RFI filter unit. Fan power is maintained at 120 V by placing the fan across one of the 120-V primaries.