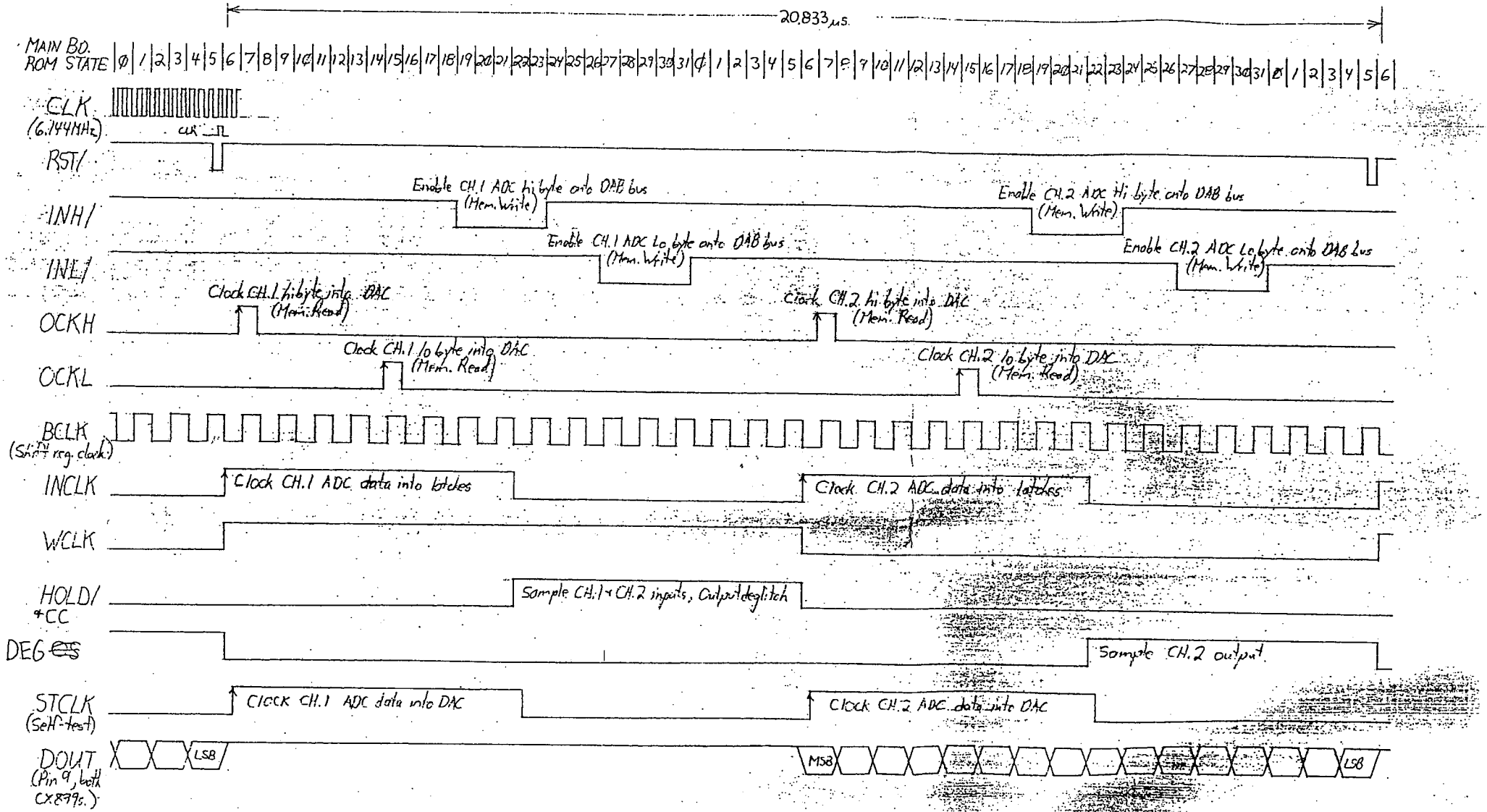

20.833 µs.
MAIN BD. ROM STATE
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 0 1 2 3 4 5 6
CLK (6.144MHz)
RST/
INH/
Enable CH.1 ADC hi byte onto DAB bus (Mem. Write)
Enable CH.2 ADC Hi byte onto DAB bus (Mem. Write)
INL/
Enable CH.1 ADC Lo byte onto DAB bus (Mem. Write)
Enable CH.2 ADC Lo byte onto DAB bus (Mem. Write)
OCKH
Clock CH.1 hi byte into DAC (Mem. Read)
Clock CH.2 hi byte into DAC (Mem. Read)
OCKL
Clock CH.1 lo byte into DAC (Mem. Read)
Clock CH.2 lo byte into DAC (Mem. Read)
BCLK (Shift reg. clock)
INCLK
Clock CH.1 ADC data into latches
Clock CH.2 ADC data into latches
WCLK
HOLD/ *CC
Sample CH.1 + CH.2 inputs, Output deglitch
DEG
Sample CH.2 output
STCLK (Self-test)
Clock CH.1 ADC data into DAC
Clock CH.2 ADC data into DAC
DOUT (Pin 9, both CX8979s.)
LSB
MSB
LSB

Check pin 26 of U16 and U17 (ADCs) with properly grounded 10X probe on a scope of at least 100 MHz bandwidth. Set scope input for AC couple, 100 mV/div. Clock signal should be a 48 MHz sine wave (about 21 ns period) of at least 300 mV peak-to-peak amplitude.

Check pin 2, serial data input of shift registers U6 and U13. Signals should be clean and CMOS level.

INPUT/OUTPUT LEVELS (0 dBV = 1 V)

1.07Vrms

Converter input level for full scale is ±10.0 V peak, ±0.50 V or +17.0 dBV, ±0.4 dBV. Input impedance is 10.0 kilohms. Output level is ±3.24 V peak or +7.2 dBV, ±0.5 dBV. Output impedance is 50 ohms.

Converter response extends to dc, and for this reason, dc blocking is inserted just before the input (on the main board) to ensure that offset voltages from previous stages do not cause asymmetrical clipping. Maximum dc offset at the converter output should be less than 100 mV.

Full-scale input level injected into the Model 1300 input filters on the main board is approximately +9 dBV.

ADJUSTMENT PROCEDURE

Channel 1

Center trimpots R15, R18, R24 and R27. Connect channel A scope probe to south side of R60, the converter's channel 1 output. Connect channel B of scope to distortion analyzer output (distortion residue). Synchronize the scope to audio oscillator's sync output. Adjust oscillator for 200 Hz at full-scale converter level. Trim R15 for lowest distortion while watching distortion residue on scope. If large spikes are evident in residue and distortion readings are greater than 0.5% (-46 dB), reduce oscillator level slightly, as long as the input level to the converter remains within the limits outlined in the previous section. Now trim R18 for lowest distortion. THD at this point should be below 0.01% (-80 dB). Switch analyzer to level mode and set the full-scale reference level. Remove input signal and check that converter output is at 0 V, ±100 mV. If not, adjust R18 to correct level. Check dynamic range. If analyzer does not show the level to be at least 90 dB below the previously set reference, very slightly adjust R18 for lowest noise. Make certain that output offset, after making this adjustment, does not exceed 100 mV. Reapply input signal and recheck THD. Repeat trimming procedure until the three conditions of distortion, noise, and offset are minimized.

Channel 2

Connect channel A scope probe to south side of R61, the converter's channel 2 output. Trim R24 for lowest distortion while watching distortion residue on scope. If large spikes are evident in residue and distortion readings are greater than 0.5% (-46 dB), reduce oscillator level slightly, as long as the input level to the converter remains within the limits outlined in the previous

section. Now trim R27 for lowest distortion. THD at this point should be below 0.01% (-80 dB). Switch analyzer to level mode and set the full-scale reference level. Remove input signal and check that converter output is at 0 V, ±100 mV. If not, adjust R27 to correct level. Check dynamic range. If analyzer does not show the level to be at least 90 dB below the previously set reference, very slightly adjust R27 for lowest noise. Make certain that output offset, after making this adjustment, does not exceed 100 mV. Reapply input signal and recheck THD. Repeat trimming procedure until the three conditions of distortion, noise, and offset are minimized.

PERFORMANCE TESTS

1. **Signal-to-Noise:** Input full scale (just below clipping). Measure output level. Remove input signal and substitute short circuit. Measure new output level referenced to full scale level. It should be essentially white noise as observed on scope or spectrum analyzer. (Use 22.4 Hz - 22.4 kHz audio bandpass filter for measurement.) Noise should be at least 90 dB below reference level.

2. **Channel Separation:** Input full scale at 200 Hz to channel 1. Measure output level and set reference. Short channel 2 input and measure output level with channel 1 still at max. level. Sweep oscillator up to 20 kHz, while observing channel 2 output level. Verify >80 dB below reference level at 1 kHz, >60 dB below reference from 20 Hz to 20 kHz. Reverse channels and repeat.

3. **Frequency Response:** With W3 again in place, measure frequency response of converter at -10 dB relative to clipping level. This will be essentially the summed response of the input anti-alias and output anti-image filters. Spec is ±0.5 dB, 20 Hz to 18 kHz and +0.5/-1.0 dB, 20 Hz to 20 kHz.

4. **THD:** Measure total harmonic distortion plus noise using the audio bandpass filter with the analyzer. Measure converter at a level just below clipping as well as 20 dB below clipping at 20 Hz, 200 Hz, 2 kHz and 20 kHz. Spec is:

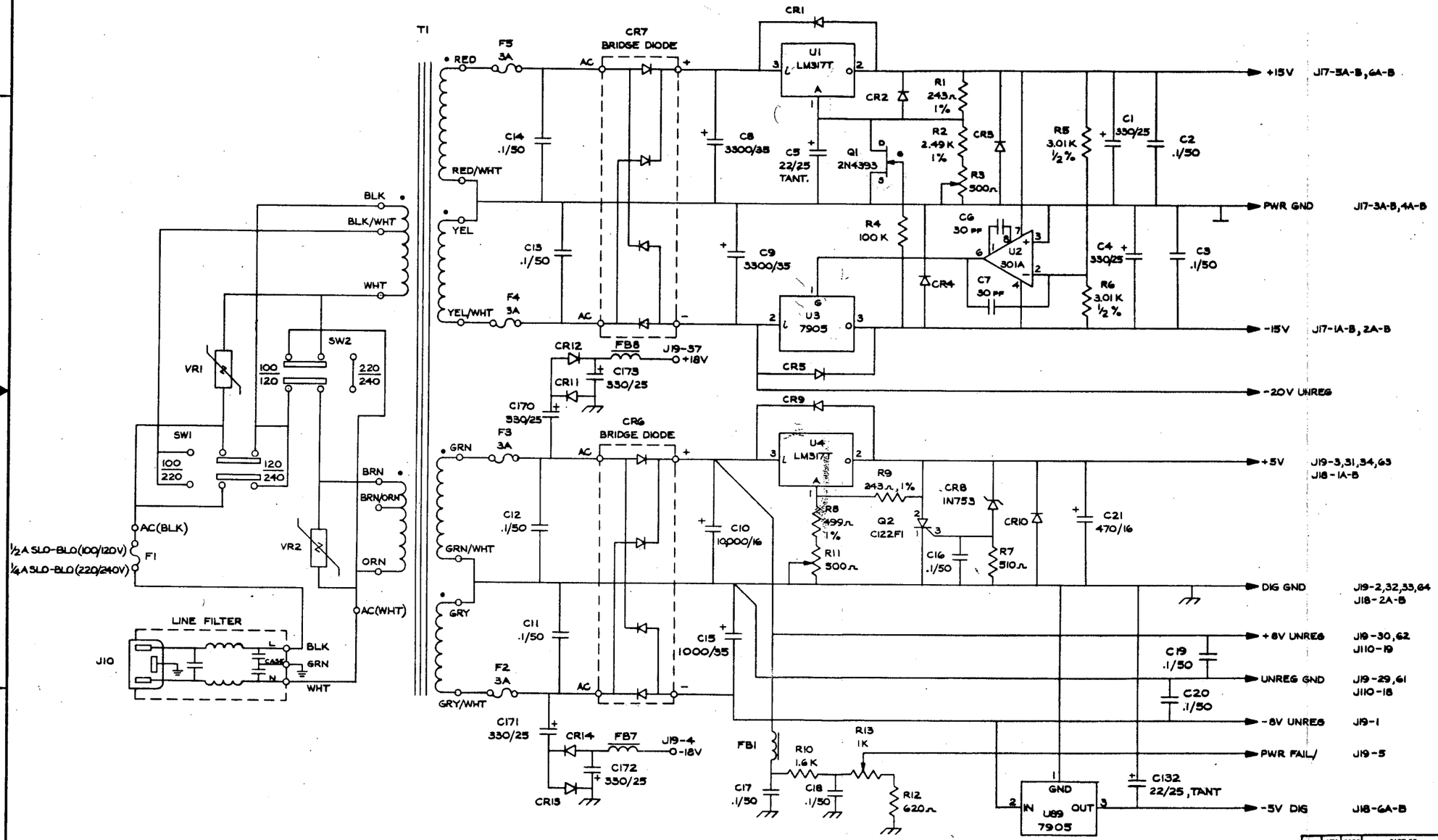
at 20 Hz	0.007% / 0.05%	at -20 dB
at 200 Hz	0.007% / 0.05%	at -20 dB
at 2 kHz	0.007% / 0.05%	at -20 dB
at 20 kHz	0.03% / 0.05%	at -20 dB

5. **IMD:** Measure SMPTE intermodulation distortion using 60 Hz and 7 kHz mixed 4:1. Measure at a level just below clipping and 20 dB lower. Spec is: 0.02% full level; 0.05% at -20 dB.

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
0	RELEASE FOR PRODUCTION	5-23-83 JCR	CS 7/1/83
1	REVISED PER ECO NO. 831103-00.	6/6/83 JCR	JCR 7/7/83
2	REVISE FOR STEREO RELEASE	2/21/84 JCR	CS 2/27/84

NOTES

1. RESISTORS ARE 5%, ¼ WATT UNLESS OTHERWISE INDICATED.
2. CAPACITOR VALUES ARE IN μF/VOLTS UNLESS OTHERWISE INDICATED.
3. POWER SUPPLY DIODES ARE IN4004 UNLESS OTHERWISE INDICATED.



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN JCR	5/23/83
CHECKED	6/6/83
ISSUED	7-7-83

lexicon

PC DOC, SCHEMATIC
MAIN BOARD, POWER SUPPLY, M1800

SIZE D | FSCM NO. | DWG. NO. 060-03644 | REV. 2
SCALE NA | SHEET 5 OF 5