4 PULSE INPUT CONTROL MODULE

4.1 Introduction

The Pulse Input Control Module is available in 50- or 60-Hz field versions for frame interpolation. This module allows the 1300 to be connected to a synchronizer that provides a pulse whose period represents the delay between a reference and video feed signal. One TTL input pulse signal is required for measurement to determine the amount of compensation needed to correct audio delay. The measured pulse width is added to the base delay (selected with the BASE DELAY switch), and the total delay is applied to the audio signal. Pulse jitter can be overcome by selecting appropriate compensating pulse hysteresis on an internal 10-position switch. The switch is factory preset for a 312-us window. Hysteresis is described in greater detail in Sec. 4.4.

Figure 4.1 is a connection diagram for a typical system configuration using the Model 1300 with a Pulse Input Control Module.

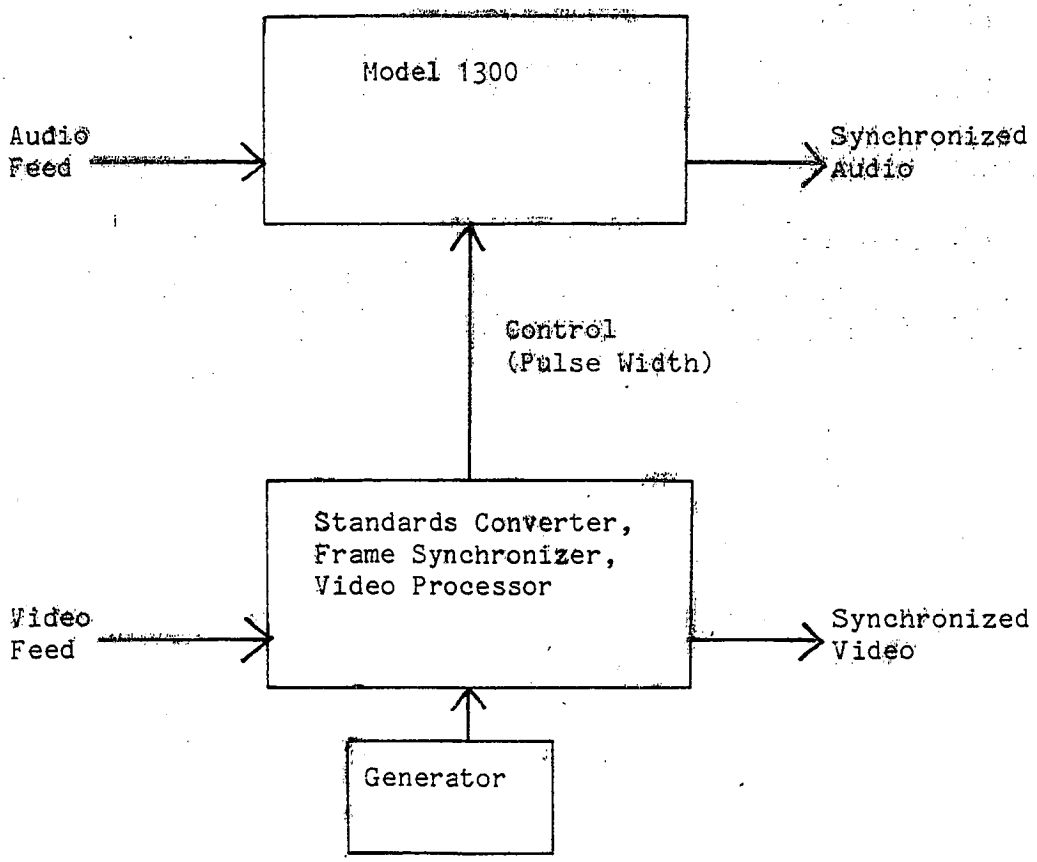

Fig. 4.1. Connection Diagram for Typical System Configuration for the Pulse Input Control Module.

4.2 Basic Operation

Turn on the 1300 by plugging it in.

Set the front-panel toggle switch labeled DISPLAY to show delay time in either frames or milliseconds. Next, set the four-position BASE DELAY switch (comprising four rotary thumb-wheel switches) to the appropriate fixed delay time (in milliseconds) required (for example, a known delay introduced by a satellite link or land lines).

Compensated delay time is automatically determined by the microprocessor in the Pulse Input Control Module. When the front-panel COMP toggle switch is set to IN, the control module determines the amount of delay that compensates for the difference between the reference video and video feed signals; it then adds the compensated delay to the fixed delay determined by the BASE DELAY switch and applies the total delay to the audio input signal. When the COMP switch is set to OUT, the 1300 applies only the delay time determined by the BASE DELAY switch to the audio input signal.

Delay processing is completely bypassed by setting the front-panel toggle switch labeled AUDIO to BYPASS.

4.3 Theory of Operation

Figure 4.2 shows a generalized block diagram of the Pulse Input Control Module, and the remainder of this section describes how the module functions. For convenience, the theory is divided into input/output control, microprocessor, and firmware.

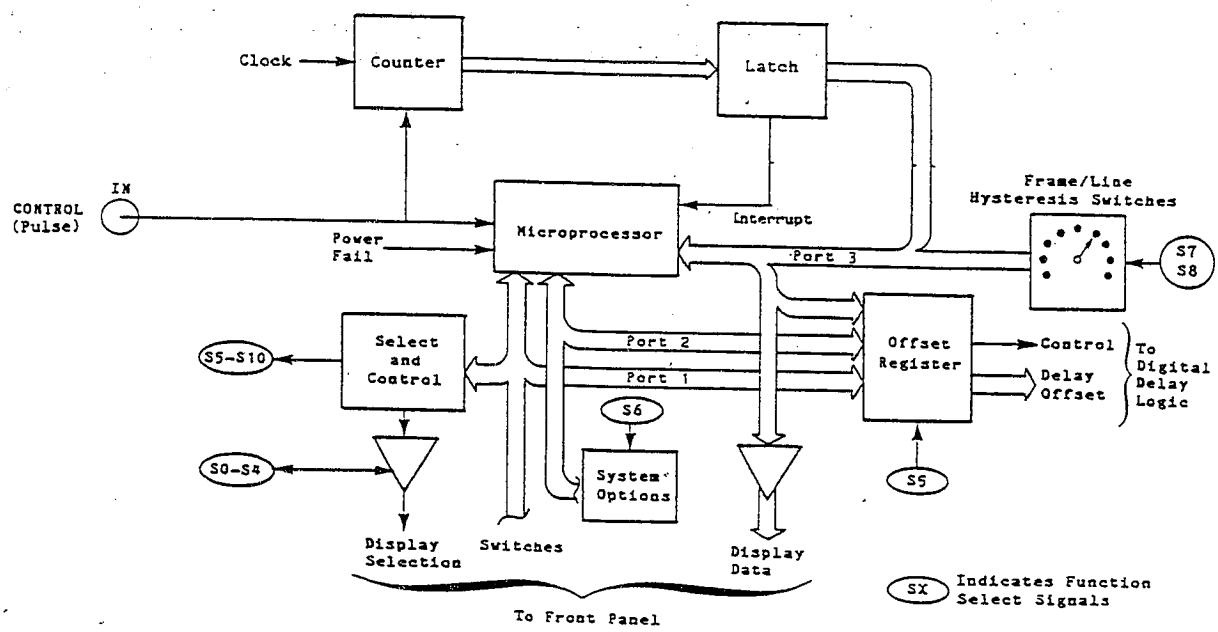

Fig. 4.2. Pulse Input Control Module Block Diagram.

Input/Output Control

Pulse Measurement

The pulse signal to be measured is applied to the control input BNC connector (J1) on the rear panel of the unit. Input requirements are a TTL signal level with a <0.8-V, 1-mA sink capability and a +5-V or open collector source having rise and fall times <10 us. An active high or active low pulse can be used for compensation delay measurement by jumper selection. To measure an active low pulse (negative going), use jumper position W1; to measure an active high pulse (positive going), use jumper position W2 (see Fig. 4.4 later).

Pulse width is measured by comparing the width to a finer repetitive crystal-controlled clock period. During the pulse active period, the counter (U21 and U19B) counts until the trailing edge of the active pulse occurs. Flop U20A is clocked high to indicate and hold the end-of-pulse condition, which is then clocked synchronously into U11B. This causes the counter value to be loaded into the U16 and U17 storage latches and interrupts the microprocessor. When the microprocessor absorbs the latched counter value, the flops U20A and U11B are reset and the counter is reset to zero. The reference clock is 51.2 Hz, or 19.53 us, and therefore each count represents a 19.53-us subinterval of the incoming pulse being measured.

The microprocessor translates the count value into compensation delay to be forwarded to the audio delay logic and the front panel display. Although pulse resolution is 19.5 us, the realized minimum pulse width is limited to 58.6 us because of the ± 1 count of pulse hysteresis performed by the microprocessor and because of the asynchronization of the first count with the sampling clock. The maximum pulse width measurable is limited by the size of the counter (4096 counts). 19.53 us per count yields a maximum measurement of 79.99 ms. Pulses greater than 80 ms cause the counter to overflow and give improper width measurements to the microprocessor. The microprocessor tests the pulse width for more than 1 second and assumes maximum compensation if the pulse remains at the active level. Therefore, the limits to pulse width and repetition rate are determined by the microprocessor. Figure 4.3 shows the sequence of events that occurs for any pulse input.

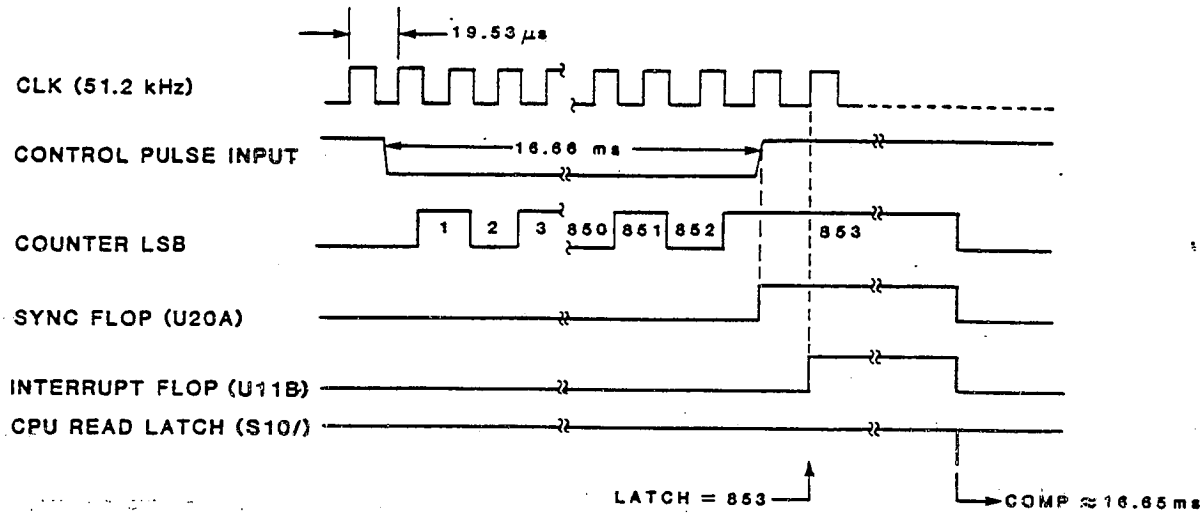

Fig. 4.3. Timing Diagram -- Pulse Input Control Module.

Microprocessor

The 1300 uses an 8-bit microprocessor with three 8-bit I/O data ports. Port 1 controls a function-select decoder, provides 2 bits of the delay offset word and control data (bypass, fade, and mute signals), and reads all front-panel switches. Port 2 reads jumper assignments for options and configurations and outputs 8 bits of the delay offset word. Port 3, the address port, reads the difference latch and the internal pulse hysteresis switches and outputs information to the front-panel LED driver and 8 bits of the delay offset word.

The microprocessor communicates with all hardware functions through a function-select decoder (U6) that generates signals S0 to S10 to perform various functions. To operate the front-panel display, the microprocessor (through the function-select decoder) uses S0 through S3 to activate the digits in the front-panel window and read the settings of the Base Delay switch. Signal S4 is used to activate front-panel LEDs and to monitor all front-panel toggle switches. Signal S5 is used to output the offset delay word (if it's ready) to an offset latch; S6 is used to read jumper assignments. S7 is used to read the internal frame hysteresis switches, and S8 the pulse present signal and internal pulse hysteresis switch. Signals S9 and S10 are used to permit reading the pulse counter latch via the microprocessor address port.

All of the microprocessor's ports must simultaneously transfer the 18-bit delay offset word to a 24-bit register (U4, U7, U8). This transfer is accomplished by loading S5 into U6; setting offset bits 0 to 7 on port 2, bits 8 to 15 on the address port, bits 16 and 17 on port 1; and then enabling S5 by setting port 1 bit 0 to 0. This process permits the time-for-write (TFW) pulses to clock the port parallel data into the offset register in sync with the delay logic. By disabling U6 and waiting a while, the offset sync flop (U11) clocks off and prevents further loading

of the microprocessor's output ports into the offset latches. When loading an offset word into the offset register, the remaining bits of U7 must contain the appropriate control signals: bypass, fade, and mute.

Firmware

The microprocessor performs the previously described control and computational tasks by executing a series of factory preset instructions in a specific repetitive sequence. Table 4.1 lists function-select decoder signals, their functions, and the order in which the microprocessor performs them.

Table 4.1. Sequence of Microprocessor-controlled Tasks.*

Sequence No.	Function-Select Decoder Signal	Function
1	S0	Activate front-panel digit 0 and read Base Delay switch SW0
2	S2	Activate front-panel digit 1 and read Base Delay switch SW1
3	S2	Activate front-panel digit 2 and read Base Delay switch SW2
4	S3	Activate front-panel digit 3 and read Base Delay switch SW3
5	S4	Activate front-panel LEDs and read all front-panel toggle switches
6	S5	Output offset delay word (if ready) to the offset latch
7	S6	Read jumper assignments for options and configurations
8	S8	Read internal pulse hysteresis switch and pulse present signal

*Any change in pulse input signals or base delay settings causes a momentary break from this sequence to perform display and delay updates.

The system scan sequence program cycles repetitively supporting the front-panel display and monitoring switches for any change. If a change occurs, it is ignored for about 1 second while scan cycles continue, then computation takes place. S9 and S10 are activated when a pulse measurement interrupts the processor.

The Pulse Input Control Module is designed to accommodate many different pulse timing conditions. The minimum pulse width is the minimum hysteresis attainable (±19.5 us) plus one pulse, or 58.6 us. The maximum pulse width is set by firmware to 79.94 ms, allowing a 60-us margin before the hardware counter overflows. Pulse rate is also flexible: a maximum of 100 pulses per second (10 ms apart) with no limit to the minimum rate (0) is possible. The Pulse Input Control Module compensates for delay on the basis of continuous pulse data. Therefore, continuous pulses are recommended because delay compensation is retained (if the compensation switch is on) indefinitely after the last accepted pulse has been received.

4.4 Pulse Hysteresis

To prevent the 1300 from inappropriately tracking pulse jitter and constantly correcting for inconsequential pulse width drift, the Pulse Input Control Module has a switch to adjust the jitter hysteresis window, allowing an operator to determine the amount of drift significant to require delay correction.

The pulse hysteresis digit switch (SW3) is next to U14 (see Figs. 4.4 and 4.5). This switch adjusts the pulse hysteresis window from ±20 to ±2496 us. Table 4.2 shows the equivalent value of each switch setting (the switch is factory preset to 5, corresponding to a 312-us window).

Table 4.2. Pulse Hysteresis Switch Settings.

Switch Setting	± Number of Microseconds
0	20
1	39
2	78
3	117
4	156
5	195
6	312
7	624
8	1248
9	2496

Internal Adjustments. The line hysteresis digit switch (SW3) is next to the frame hysteresis switches (see Figs. 4.4 and 4.5). This switch adjusts the line hysteresis window of from ±1 to ±128 lines. Table 4.2 shows the equivalent value of each switch setting (the switch is factory preset to 5, corresponding to a 20-line window).

Table 4.2. Line Hysteresis Switch Settings.

Switch Setting	± Number of Lines
0	1
1	2
2	4
3	6
4	8
5	10
6	16
7	32
8	64
9	128

4.5 Delay Change

The 1300/S performs changes in delay either instantaneously or gradually; when the Compensation switch is off, the 1300/S changes delay instantly, and with the Compensation switch on, delay changes are performed gradually at a rate of 0.6 to 0.7 frames per second, depending on the transmission standard.

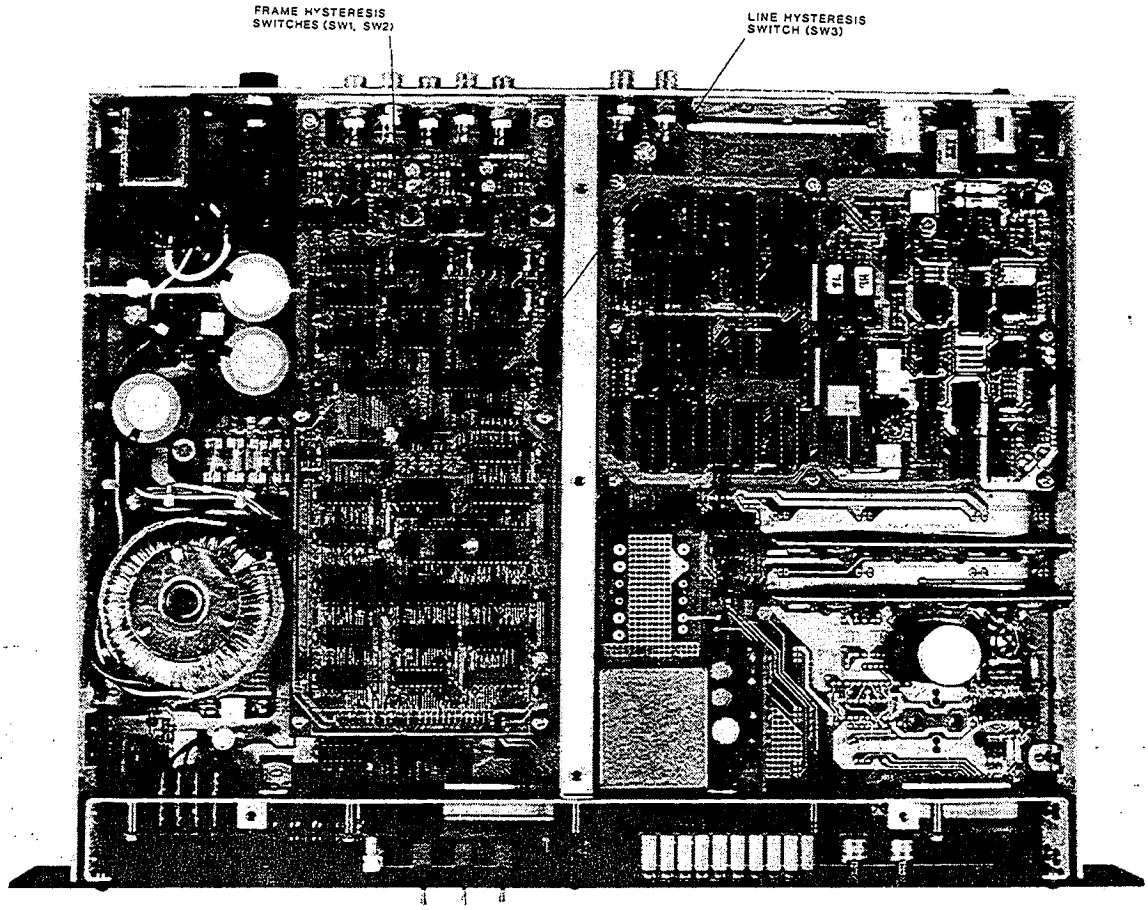

Fig. 4.4. Location of Hysteresis Switches.

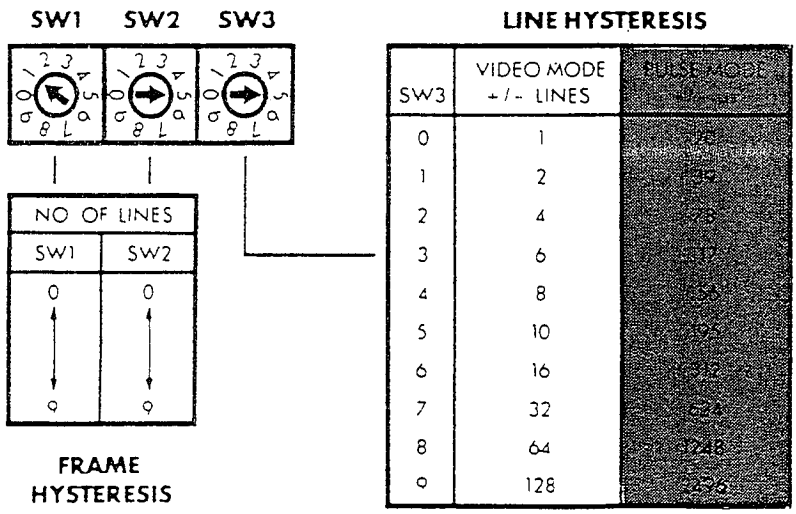

Fig. 4.5. Frame and Line Hysteresis Switch Settings.