Service Manual

Lexicon

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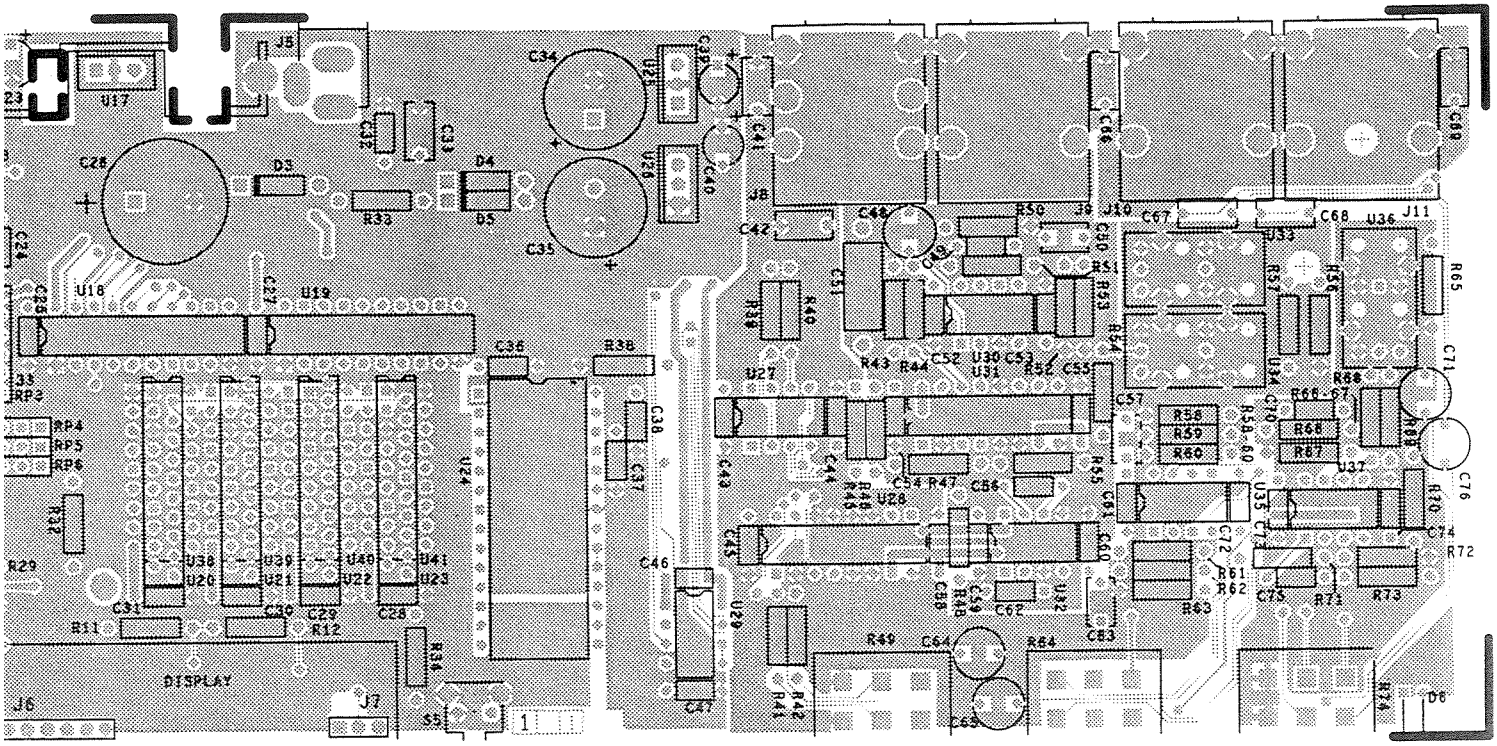
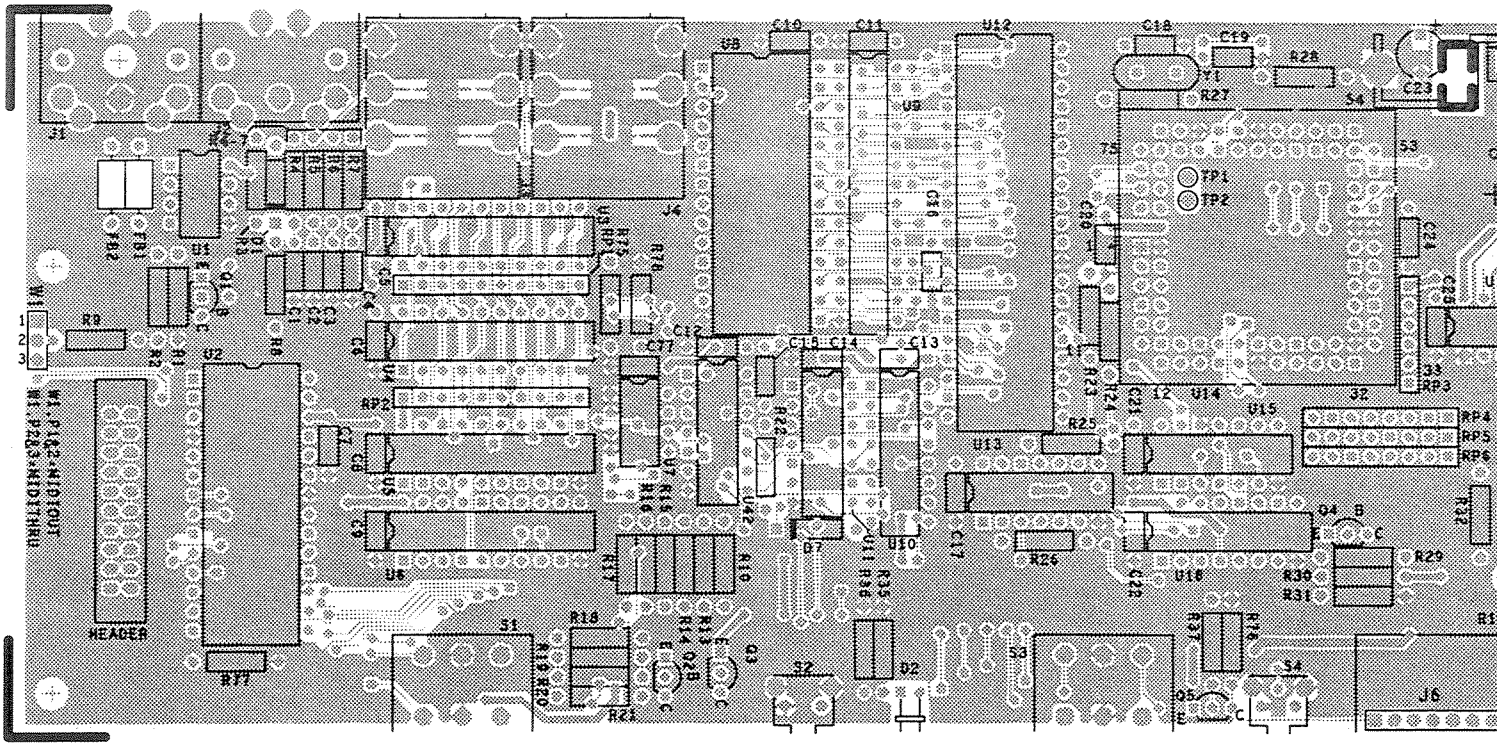


Reflex Main Board COMPONENT PLACEMENT	
SHEET 1 OF 1	11/22/94 REV 1
Lexicon	100 BEAVER STREET WALTHAM, MA 02154


W1.P1&2:MIDIOUT
W1.P2&3:MIDITHRU
HEADER
TP1
TP2
Y1

1 Controls and Connectors

The Front Panel

MIX
Controls the proportion of processed (wet) to unprocessed (dry) signals sent to the outputs.

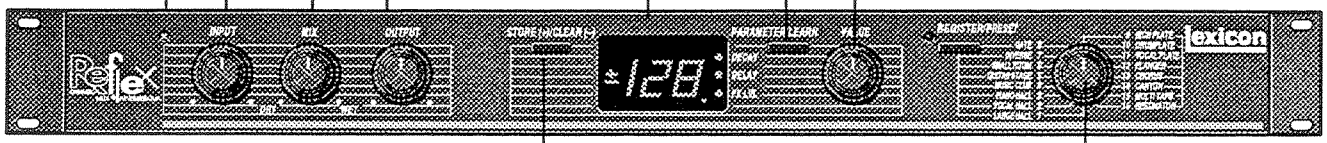
INPUT
Sets the level of the incoming signal. — Status LED is off when the incoming signal is too low (<-30dB). Acceptable levels are indicated by green (-30 to -12dB) and orange (-12 to -6dB). The LED lights red to indicate overload (-6 to 0dB).

OUTPUT
Controls Reflex output level.

DISPLAY
+ = store function enabled
– = clear function enabled
1-128 = ID number of currently running effect or parameter setting
• = Edit indicator or patch indicator depending on mode of operation
LEDs = currently selected parameter

PARAMETER/LEARN
Selects DECAY, DELAY or FX LVL for adjustment with VALUE knob. Holding sets Reflex to the same MIDI channel as a connected device, and activates patch assignment.

VALUE
Adjusts value of selected parameter. Display of parameter values is indicated by flashing of the selected parameter LED.



STORE (+)/CLEAR (-)
The STORE/CLEAR button selects Reflex's readiness to store an effect or to clear a register. These states are indicated by a + (store) or - (clear) symbol in the display.

REGISTER/PRESET
Button selects preset or register mode.

LED lights when register mode is selected, turns off in preset mode.

Knob will select presets 1-16 or registers 1-128, depending on button setting.

Storing and Clearing Reigsters

To store or clear the currently running effect...

1. Briefly press STORE/CLEAR to display "+" or "-", depending on whether you want to store or clear a register.
2. Press and hold STORE/CLEAR. If you were in preset mode, the register LED will go on, indicating that Alex has automatically switched to register mode — selecting whatever register is being pointed to by the PRESET REGISTER knob. The + or - symbol in the display will flash, indicating that the store or clear function is armed.
3. Releasing STORE/CLEAR with a flashing + displayed, will store the currently running effect into the register indicated on the display, overwriting the effect previously stored there. The display will flash briefly to indicate the store operation was successful.

   Releasing STORE/CLEAR with a flashing - displayed, will clear the contents of the displayed register. The display will flash briefly to indicate the clear was successful. (The ID number of cleared registers flash when selected with the PRESET/REGISTER knob.)

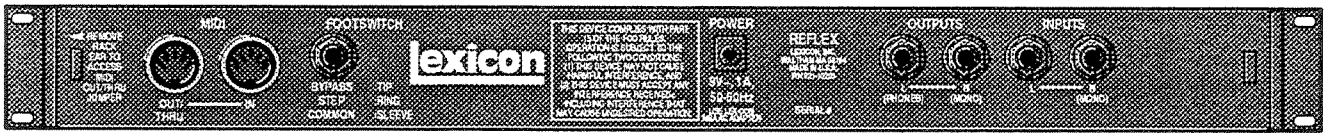
   To restore a cleared register, simply repeat the clear operation.

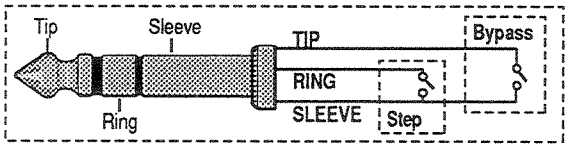
Store and clear operations are executed on release of the STORE/CLEAR button. If you want to store to or clear a different register than the one displayed, turn the PRESET/REGISTER knob to the register number you want *before* releasing STORE/CLEAR.

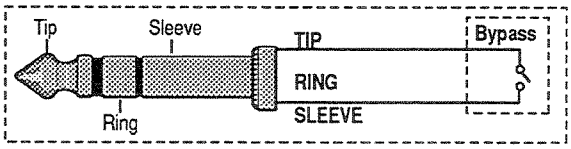
The Rear Panel

Audio connections to Reflex are unbalanced and should be made with high quality shielded cables with 1/4" tip-sleeve phone jacks at the Reflex end.

Reflex produces stereo effects from either mono or stereo sources. With mono sources the dry signal appears in mono at both output connectors along with the stereo effects. For instruments and sources with stereo outputs, use both inputs. We recommend using the outputs in stereo whenever possible, but if mono output is required, you can use either output connector. The left and right signals are summed internally when only one output is used.







Footswitches

A footswitch connected via the rear-panel footswitch jack allows you to perform register step and/or bypass functions. Two momentary footswitches can be wired to a tip-ring-sleeve connector. A stereo Y-connector allows two identical single switches to be used.

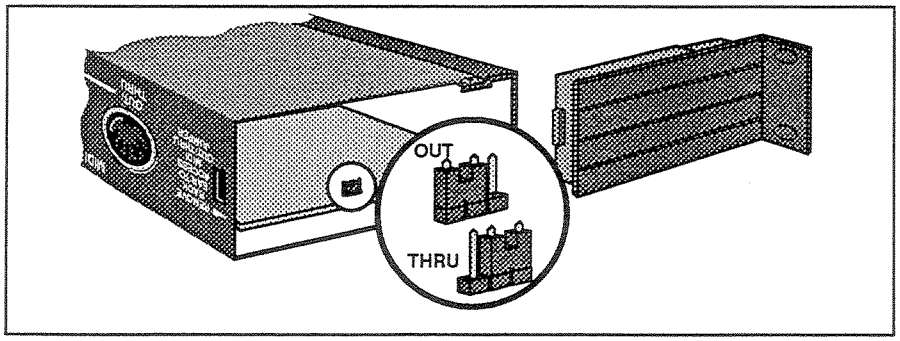
When shipped, Reflex is configured to use momentary switches. You can change this configuration to allow the use of latching switches by performing the following procedure:

1. Simultaneously press the PARAMETER/LEARN and the REGISTER/PRESET buttons. This will put the unit into Advanced Programming Mode (lighting all 3 front panel parameter LEDs).
2. Turn the REGISTER/PRESET knob to 15. The letter "F" should appear on the display.
3. Turn the VALUE knob to select 0 (latching) or 1 (momentary).
4. Press the REGISTER/PRESET button to restore normal front panel operation.

MIDI OUT/THRU Jumper

When shipped, Reflex is configured for MIDI OUT operation. You can reconfigure the unit for MIDI THRU operation with the following procedure.

1. Disconnect power.
2. Remove the two top and bottom cover screws which are closest to the rear panel MIDI connectors.
3. Lay the unit upside down and remove the rack ear.
4. Lift the jumper off of its pins and reposition it according to the functionality you want.
5. Replace the rack ear and the cover screws.
6. Reconnect power.



MIDI OUT/THRU Jumper

Setting Audio Levels

1. Turn Reflex's INPUT and OUTPUT controls all the way down (fully counter-clockwise).
2. Connect Reflex inputs to an audio source, and Reflex outputs to an amplifier or mixer.
3. Apply an input signal at a level that you typically use.
4. While sending audio to Reflex, gradually turn up the INPUT control until the Input Status Indicator lights green. Continue to advance INPUT until the LED shows red on only the loudest peaks. If the LED shows red continuously, turn the INPUT control down.
5. If Reflex is using a console's sends and returns, set the MIX control fully clockwise (100% wet). If you are using an instrument amplifier, start with MIX set halfway up.
6. Gradually increase the setting of the OUTPUT control until the audio level from the amplifier or mixer is approximately the same as when Reflex is bypassed.

Periodic Maintenance

Under normal conditions Reflex requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon, Inc.
100 Beaver Street
Waltham MA 02154
Telephone: 617-736-0300
Fax (Customer Service): 617-788-0499

ATT: Customer Service

Returning units for service

Before returning a unit, for warranty or non-warranty service, consult with Lexicon to determine the extent of the problem, and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return a Reflex to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, both inside and outside of package

Please enclose a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Service personnel.

2 Specifications

Audio Inputs (2)

Level	-30dBu minimum
Impedance	stereo/50 kΩ unbalanced mono/25 kΩ unbalanced

Audio Outputs (2)

Level	-2dBu nominal +8dBu maximum
Impedance	75Ω unbalanced
Muting	reduces transients during power on/off

Footswitch Connectors

T/R/S phone jack for bypass and register step

MIDI Connectors

5-pin DIN connectors for MIDI IN and MIDI OUT or THRU (selectable via internal jumper)

Frequency response

Wet	20Hz-15kHz, +1dB to -3dB
Dry	20Hz-20kHz, ±0.5dB

THD+N

Wet	<0.05% @ 1kHz
Dry	<0.025% @ 1kHz

Dynamic Range

85dB, typical,
20Hz-20kHz bandwidth

Conversion

16 bit linear PCM encoding; 31.25kHz sampling rate

Power Requirements

9VAC, 1A wall transformer provided

Dimensions

19"W x 1.75"H x 4"D
(483 x 45 x 102mm)

Weight

2 lbs 11 oz (1.22 kg)

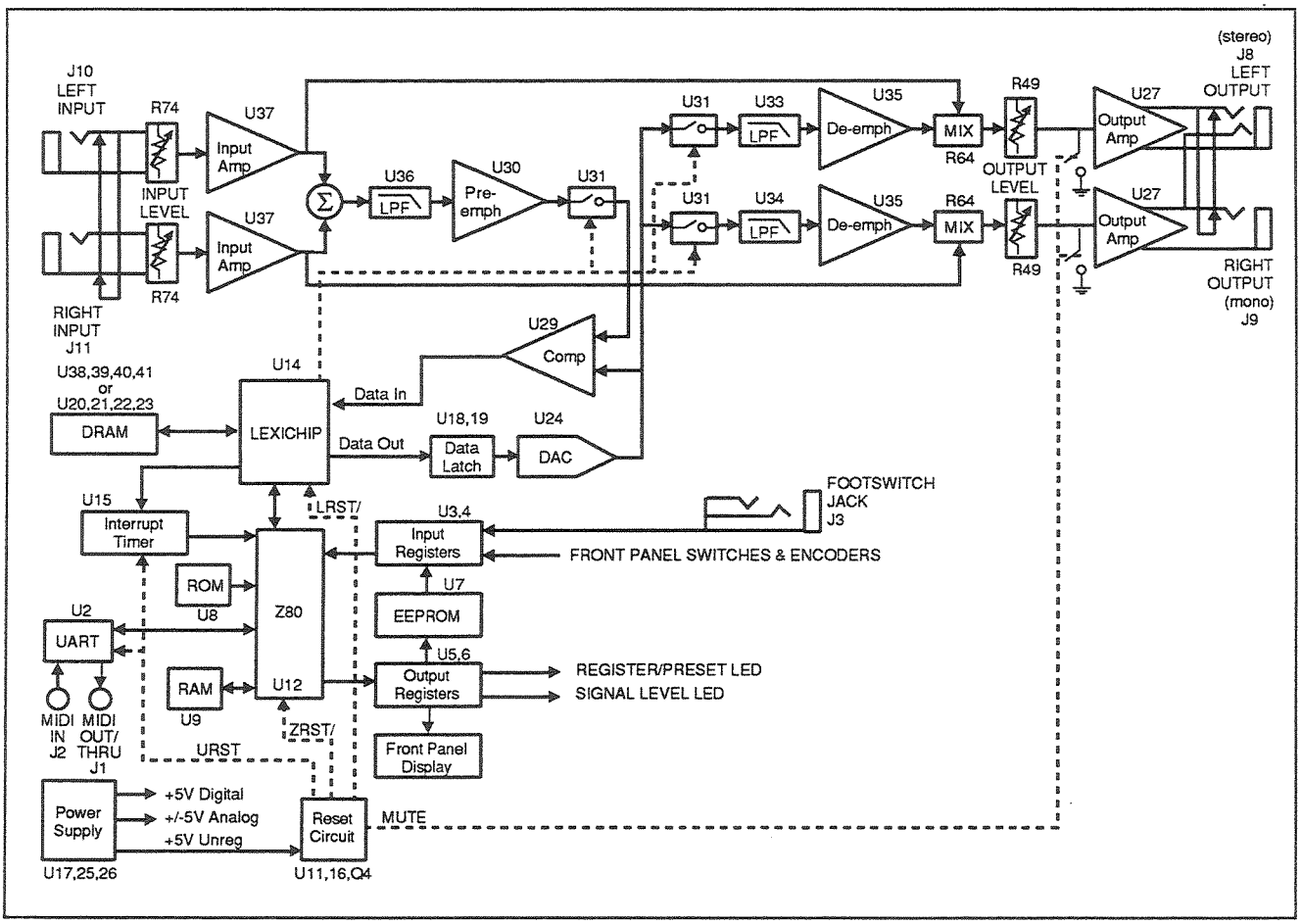
Environment

Operating Temperature	32° to 104°F (0° to 40° C)
Storage	-20° to 170°F (-30° to 75° C)
Relative Humidity	95% non-condensing

Specifications subject to change without notice.

3 Performance Verification

Reflex Block Diagram



Required Equipment

- Clean, antistatic, well lit work area
- Variac, 1 amp minimum
- Double footswitch (Lex #750-09365 or equivalent)
- MIDI cable (1 ft. minimum)
- Low Distortion Sine Wave Audio Oscillator
- THD+N Distortion Analyzer
- Stereo headphones
- Two (2) audio cables unbalanced and shielded with 1/4" phone plug on one end and the appropriate connection on the other end to connect to the Audio Oscillator output and Distortion Analyzer input
- Y connector for connecting the audio cables to the oscillator
- 9VAC power supply (Lexicon #470-09650)

Initial Inspection

1. Inspect the unit for any obvious signs of physical damage.
2. Verify that all front panel knobs operate smoothly and freely.
3. Verify that all screws and rear panel jacks are secure and inspect the AC power supply for any sign of physical damage.
4. Turn the REGISTER/PRESET knob, to select 16 RESONATOR.
5. Turn VALUE to the 6:00 position.

Power Up

AC Current

1. Set the Variac to 0VAC minimum.
2. Connect the 9VAC power supply to the isolated variable output of the Variac.
3. Connect the 9VAC power supply to the power input on Reflex.
4. Slowly increase Variac to 120VAC.
5. Verify the AC current draw is <0.12 Amps.

On normal power up, Reflex will run the following tests:

Display Test
ROM Test
SRAM Test
WCS Test (Writable Control Store)
Interrupt Test

On normal power up, all display segments except for the decimal point, and all LEDs except for the headroom LED, light for about 2 seconds. This is followed by the display of **L** for approximately 7 seconds, after which the display will indicate the current position of the REGISTER/PRESET knob. In this case, **+16** should be displayed with the DECAY LED lit.

NVS Inititialization

1. Power cycle Reflex while pressing and holding STORE/CLEAR and PARAMETER/LEARN.
2. After 3 or 4 seconds, verify that the letter **d** appears on the display, then release the buttons.
3. Press and hold the REGISTER/PRESET button until the display goes blank, then release the button.
4. Press the REGISTER/PRESET button and verify the display reads: **15**.
5. Press the REGISTER/PRESET button and verify that the **+** symbol flashes momentarily, and is followed by a display of: **15**.
6. Turn the REGISTER/PRESET knob counterclockwise to point to 10 Drum Plate. The display should read: **9**.
7. Press the REGISTER/PRESET button, and verify that the display reads: **1**. This display will flicker for approximately 18 seconds, following which an **L** will be displayed for approximately 7 seconds. After this, the display will read: **+10** (the current position of the REGISTER/PRESET knob) .
8. Turn the REGISTER/PRESET knob clockwise to select 13 CHORUS. The display should read **13**.

Display

1. Power cycle Reflex and verify that all display segments except the decimal point, and all LEDs except for the headroom LED, light for approximately 2 seconds. This is followed by the display of **L** for approximately 7 seconds, after which the display will indicate the current position of the REGISTER/PRESET knob. In this case, **+13** should be displayed.
2. Power off Reflex.

Functional Tests

Connections

1. Using the 15 foot 1/4" phone plug cable supplied with the footswitch, connect one end to the footswitch and the other end to the Reflex rear panel FOOTSWITCH (Bypass/Step) jack.
2. Connect the MIDI cable between the Reflex rear panel MIDI IN and MIDI OUT/THRU jacks.

Encoders

1. Power on Reflex while pressing and holding STORE/CLEAR and PARAMETER/LEARN.
2. After 3 or 4 seconds, verify that the letter **d** appears on the display, then release the buttons.
3. Press and hold the REGISTER/PRESET button until the display goes blank. The display should read: **12.**
4. Press STORE/CLEAR to enter the test. Verify that the display becomes dim and that the display reads: **– C.**
5. Turn the REGISTER/PRESET knob to its 6:00 position and verify that the display reads **+ 0.**
6. Turn the REGISTER/PRESET knob clockwise one position, and turn VALUE clockwise one position. The display should read: **+1.**
7. Reset each knob to the remaining 14 positions and verify that the + symbol is displayed when both knobs are in the same position. The display should also indicate the current encoder positions in hexadecimal.

NOTE: When the knobs are in different positions, the – symbol will be displayed along with the current position of the REGISTER/PRESET knob (0-15). When the knobs are in matching positions, the – symbol will change to the + symbol. To check the current position of VALUE, press STORE/CLEAR

REGISTER/PRESET Knob Position	Display Reading	REGISTER/PRESET Knob Position	Display Reading
Large Hall	0	Rich Plate	8
Vocal Hall	1	Drum Plate	9
Piano Hall	2	Vocal Plate	A
Music Club	3	Flanger	b
Guitar Stage	4	Chorus	C
Small Room	5	Canyon	d
Inverse	6	Multi Taps	E
Gate	7	Resonator	F

Press the REGISTER/PRESET button to exit the Encoder Test.

Front Panel Buttons and Footswitches

1. Turn the REGISTER/PRESET knob to select 14 CANYON. The display should read: **13**.
2. Press the REGISTER/PRESET button to enter the Button Test.
3. Verify that the display reads: **0**.
4. Individually press each button and footswitch, and verify that the display indicates the correct value according to the following table when each button is pressed. When no buttons are being tested, **0** should be displayed.

Front Panel Button	Footswitch
STORE/CLEAR = 1 PARAMETER/LEARN = 2 REGISTER/PRESET = 3	Left Footswitch = 4 Right Footswitch= 5

5. To exit the test, simultaneously press PARAMETER/LEARN and STORE/CLEAR. Verify that **13** is displayed when the buttons are released.

Dynamic RAM

1. Turn the REGISTER/PRESET knob clockwise to select 7 INVERSE. The display should read: **6**.
2. Press the REGISTER/PRESET button to enter the test. Verify that **r** appears on the display. After 13 seconds, the + symbol should appear on the display.
3. Press the REGISTER/PRESET button to exit the test. The display should read: **6**.

MIDI

1. Turn the REGISTER/PRESET knob clockwise until the display reads: **11**.
2. Press the REGISTER/PRESET button to enter the test. Verify that r appears on the display. After 4 seconds, the + symbol should appear on the display, followed by **11**.
3. Remove the MIDI cable and the Footswitch cable.
4. Power off Reflex.

Listening Tests

Setup

1. Connect stereo headphones to the Reflex rear panel Left Output (Phones).
2. Using the 2 audio cables for the sine wave audio oscillator, connect the left and right inputs of Reflex to the Y connector and connect the Y connector to the output of the sine wave audio oscillator.
3. Set the Reflex front panel OUTPUT control fully counterclockwise.
4. Set the Reflex front panel INPUT and MIX controls fully clockwise.
5. Power on Reflex, and power on the low distortion sine wave audio oscillator.
6. Input a 220Hz sine wave at -50dBV to Reflex.
7. Turn the REGISTER/PRESET knob to select 1 LARGE HALL. The display should read: **1**.
8. Put on the headphones.
9. Set OUTPUT to a comfortable listening level.

Smooth Pots

1. Individually sweep the INPUT, MIX and OUTPUT controls over their entire range.
2. Verify that no pops, clicks or scratchiness are heard when turning the controls.

Quick Listen

1. Set the INPUT and MIX controls fully clockwise.
2. Set OUTPUT to a comfortable listening level.
3. Vary the frequency on the oscillator.
4. Verify that no pops, clicks, buzz, or other audio artifacts are heard.

Shock Test

1. Lift each end of Reflex 4" off the bench and drop it.
2. Verify that no audio, display, or LED intermittents are caused by this action.

NOTE: TO AVOID DAMAGE TO THE UNIT, KEEP ONE CORNER OF THE UNIT TOUCHING THE BENCH AT ALL TIMES.

Headroom LED

1. Disconnect the headphones.
2. Set both the INPUT and OUTPUT controls fully counterclockwise.
3. Increase the oscillator level to -35dBV.
4. Slowly increase INPUT over its entire range.
5. Verify that the headroom LED, lights green, then red during the clockwise rotation of the knob.
6. Remove audio cables and power cable from Reflex.

Factory Settings

1. Set all front panel knobs fully counterclockwise.
2. Set the REGISTER/PRESET and VALUE knobs to their 6:00 positions.

Diagnostics

Reflex software contain two categories of Diagnostics: Power Up Diagnostics, which are run automatically each time the unit is powered on, and User Diagnostics, which are invoked by simultaneously pressing the front panel STORE/CLEAR and PARAMETER/LEARN buttons during power up.

Power Up Diagnostics

When power is first applied to the system, a series of diagnostic tests are run to help avoid having the normal operating software attempting to run on faulty hardware.

When the system first powers up, the maskable interrupt (from the UART/ MIDI IN) is disabled, the UART is initialized and the nonmaskable interrupt (NMI) is disabled by toggling DISABLEINT/ from Output Register 2 (U5 pin 9) low. Nonmaskable interrupts, which occur frequently (every 512us), must be tightly controlled. A low on the DISABLEINT/ line prevents the NMI/ line from being pulled low and triggering an interrupt. Once the DISABLEINT/ line is low the software loads software into the Lexichip which allows it to output a WC/ signal at the proper frequency (32kHz). At this point, the software jumps to the diagnostic section, which turns on all of the front panel LEDs except the headroom LED for approximately two seconds. It turns off the LEDs, checks to see if a key was pressed and then begins running its tests.

At power up the following diagnostic tests are run:

A	ROM Test
B	RAM Test
C	WCS Test
E	Interrupt Test

Upon completion of these tests, the SRAM (U9) is cleared to all 0s, and the normal operating software is run.

Pass/Fail of Power Up Diagnostics

When the Power Up Diagnostics pass, the display stays blank until the normal operating software displays the letter L (while the registers are read from the EEPROM), then the selected preset or register ID number. If a test fails, the letter ID of the test is displayed and the test is continuously re-run. To skip a failing test, press and hold the STORE/CLEAR and PARAMETER/LEARN buttons for approximately 1/2 second.

ROM Test

This is a checksum test of the system ROM. A checksum test is performed by reading each memory location in ROM and adding the stored value stored. This number is compared with the total calculated when the software was first assembled. A mismatch indicates a problem with the ROM or with the Z80's ability to read the ROM (shorted address line, etc...). The last two memory locations are reserved to store the comparison value. In practice, the ROM test is primarily useful for verifying that the contents of the ROM were transferred correctly from the master and are uncorrupted.

RAM Test

Several tests that get performed on the SRAM (U9) in the system. First, the RAM is filled with the value 55 hex (0101 0101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (1010 1010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is repeated, checking for AA's and storing 0's. Then, the memory is checked for 0's and the test exits.

WCS Test

The WCS test is identical to the SRAM test except that it is run on the program memory space in the Lexichip 2 (U14).

Interrupt Test

This test verifies that the NMI Interrupt is working, and that it occurs at the proper intervals. The interrupt is allowed to run for a period of time that should allow 20 interrupts. A count of the interrupts is kept and compared for overshoot and undershoot. More than 21 interrupts means the interrupt is too short. Fewer than 19 interrupts means it's too long. Note that the User Diagnostics allow you to distinguish overshoot and undershoot.

User Diagnostics

The User Diagnostics provide more interactive access to the tests run by the Power Up Diagnostics, and also provide access to tests, troubleshooting tools and system configuration tools not available from the normal operating system.

NOTE: As User Diagnostics must operate within the limits of the front panel controls, it is not always readily apparent to a casual observer what the current mode of the system is. Care should be taken to keep track of where you are and how you got there.

Accessing User Diagnostics

To access User Diagnostics, press and hold the STORE/CLEAR and PARAMETER/LEARN buttons during power up. The letter **d** appears on the display to indicate you have entered User Diagnostics. Release the buttons and wait approximately one second. To begin using the diagnostics, press STORE/CLEAR, PARAMETER/LEARN or REGISTER/PRESET.

The Diagnostics Menu

The User Diagnostics contain 21 tests and tools. Turn the REGISTER/PRESET knob to select sixteen of these menu items, each of which has a displayed ID number. Execute any displayed item by pressing STORE/CLEAR, PARAMETER/LEARN or the REGISTER/PRESET button. An additional five menu items are selected in an "Alternate Mode". Access this mode by continuously holding down PARAMETER/LEARN. In this mode, the decimal point will light. While holding down PARAMETER/LEARN, turn the REGISTER/PRESET knob to select an item and press the STORE/CLEAR or REGISTER/PRESET button to execute any displayed item.

Following is a list of all of the available tests and tools, their ID numbers and REGISTER/PRESET knob positions.

ID	REGISTER/PRESET Knob Position	Test/Tool Name
0	1 LARGE HALL	Footswitch Latch Mode
1	2 VOCAL HALL	Footswitch Momentary Mode
2	3 PIANO HALL	SRAM Test
3	4 MUSIC CLUB	WCS Test
4	5 GUITAR STAGE	Interrupt Test
5	6 SMALL ROOM	ROM Test
6	7 INVERSE	DRAM Test
7	8 GATE	Burn-In Test
8	9 RICH PLATE	Audio I/O Test
9	10 DRUM PLATE	Return to normal operating mode
10	11 VOCAL PLATE	EEPROM Checksum
11	12 FLANGER	MIDI Test
12	13 CHORUS	Encoder Test
13	14 CANYON	Switch Test
14	15 MULTI TAPS	Display Error History
15	16 RESONATOR	Initialize EEPROM

Alternate Mode (Press and hold PARAMETER/LEARN)

ID	REGISTER/PRESET Knob Position	Test/Tool Name
0.	1 LARGE HALL	Read Log
1.	2 VOCAL HALL	MIDI Tool
2.	3 PIANO HALL	Sinewave @ 440Hz or 1kHz.
3.	4 MUSIC CLUB	MIDI Terminal
4.	5 GUITAR STAGE	Select DRAM Size

Error Reporting

In general, the User Diagnostics displays a + or – sign to indicate PASS or FAIL results of the test. Most tests run extremely fast, so the + or – sign flashes almost immediately. Others, such as the DRAM test take longer. Longer tests display a small r to indicate that the test is running. Tests that fail briefly flash an error number on the display which can help trace the problem. Refer to individual test descriptions to see if detailed error codes are supported.

Footswitch Selection (Mechanically Latched Switches) (0)

This function allows the end user to change the footswitch input so that mechanically latched footswitches (2) can be used to control the Register Step Up and Bypass Function.

Footswitch Selection (Momentary Switches) (1)

This function allows the end user to change the footswitch input so that momentary footswitches (2) can be used to control the Register Step Up and Bypass Function. This is the factory default setting.

SRAM Test (2)
This is actually several tests that get performed on the SRAM (U9) in the system. First, the RAM is filled with the value 55 hex (0101 0101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (1010 1010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is repeated, checking for AA's and storing 0's. Then, the memory is checked for 0's and the test exits.

The following error codes are used for this test:

1	55 test
2	AA test
3	00 test

WCS Test (3)
The WCS test is identical to the SRAM test except that it is run on the program memory space in the Lexichip 2 (U14).

The following error codes are used for this test:

1	55 test
2	AA test
3	00 test

Interrupt Test (4)
This test verifies that the NMI Interrupt is working, and that it occurs at the proper intervals. The interrupt is allowed to run for a period of time that should allow 20 interrupts. A count of the interrupts is kept and compared for overshoot and undershoot. More than 21 interrupts means the interrupt is too short. Fewer than 19 interrupts means it's too long. Note that the User Diagnostics allow you to distinguish overshoot and undershoot.

The following error codes are used for this test:

1	Interrupt count was <19 over a period of 10.24ms. Too slow or dead.
2	Interrupt count was ≥22 over a period of 10.24ms. Too fast.

ROM Test (5)
This is a checksum test of the system ROM (U8). A checksum test is performed by reading each memory location in ROM and adding the stored value stored. This number is compared with the total calculated when the software was first assembled. A mismatch indicates a problem with the ROM or with the Z80's (U12) ability to read the ROM (shorted address line, etc...). The last two memory locations are reserved to store the comparison value. In practice, the ROM test is primarily useful for verifying that the contents of the ROM were transferred correctly from the master and are uncorrupted.

The number 1 (failed) is the only error code available for this test.

DRAM Test (6)

The DRAM test is a little different than the other memory tests because the Z80 does not have direct access to the actual DRAM. The only way the Z80 (U12) can read from or write to the DRAM (U38-41 or U20-23) is through the Lexichip. The Lexichip II has 6 internal register locations through which the Z80 can read and write data to the digital audio bus. A special microcode program is loaded into the Lexichip to run the test.

While the test is running, the letter r is displayed to indicate that the test is running. The test takes approximately 13 seconds for 64K DRAM, 50 seconds for 256K DRAM and 4 minutes for 1 MEG DRAM. The first thing that the DRAM test does is determine the size of the DRAM. The current software expects the DRAM to be either 64K, 256K, 1 MEG or 4 Meg RAMs.

If a failure occurs, the diagnostics may indicate which DRAM(s) is at fault. The display will flash an error code in hexadecimal from 1-F four times after the PRESET/REGISTER button is pressed. Below is a table illustrating which DRAM(s) are associated with each error code.

Display:	HEX)	Decimal	4464 DRAM
	1	1	U20
	2	2	U21
	3	3	U20, U21
	4	4	U22
	5	5	U20, U22
	6	6	U21, U22
	7	7	U20, U21, U22
	8	8	U23
	9	9	U20, U23
	A	10	U21, U23
	B	11	U20, U21, U23
	C	12	U22, U23
	d	13	U20, U22, U23
	E	14	U21, U22, U23
	F	15	U20, U21, U22, U23

The following error codes are used when using the View Previous Test and Results Tool (Test 14):

1 5555 test
2 AAAA test
3 Address Test (address is written into the memory)

Burn-In Test (7)

This is a diagnostic sequencing utility that continuously runs the following tests, until a test fails, or power is removed from the unit.

ROM Test (5)
SRAM Test (2)
WCS Test (3)
Interrupt Test (4)
DRAM Test (6)

If a test fails the – sign is displayed. To find out what test failed, press any front panel button to display the test number as shown in parenthesis next to the test above.

Audio I/O Test (8)
This test loads a microcode program into the Lexichip (U14) which passes converted audio directly to the DAC (U24) for output with processing. The code is loaded, the + sign is flashed, and you are returned to the diagnostics menu with the I/O program running. The I/O remains running until another diagnostic changes the Lexichip WCS. Please note that this version of the I/O program has alternate memory access to offset 0 and FFFF, to induce digital noise like that of a typical reverb program.

Return to normal operating mode (9)
This allows you to exit the diagnostics and return to the regular operating system. Changes to the MIDI configuration are kept intact and the size of the DRAM is calculated. Note that the MIDI configuration will be erased if the SRAM test is run. The MIDI channel will end up being channel 1 because the SRAM test clears the RAM to 0 when it is done.

EEPROM checksum (10)
This test reads each byte in the User Register portion of the EEPROM (U7) and adds them to calculate a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum is recalculated each time a register is stored.

MIDI Wrap Around Test (11)
This test checks the operation of the UART (U2) and MIDI IN and OUT hardware by transmitting a series of characters to the MIDI OUT port and reading the MIDI IN port to see if the data matches. Before transmitting data the UART is checked for data waiting to be transmitted. If this part of the test fails the UART itself may be bad, the 500KCLK clock may be missing or the address line (SADR0) to the chip may be open. Data is then read from the UART and the UART is asked if it has data waiting (which it shouldn't because it was just read). Note that the C/D pin on the UART controls whether we are communicating data (0) (transmit or receive) with the UART or control/status (1). If it is stuck low, then data can only be sent and received with no control or status. Stuck high means that we can only read status and send control information to the chip. For this test to pass this bit must toggle.

At this point, data is sent to the UART. After an interval long enough for the UART to transmit the byte, the status register in the UART is read to see if the byte was transmitted. The status register is then read again to see if a byte has been received. If so, the byte is read from the UART and checked against the byte transmitted to see if they match. This repeats until the entire string has been tested. The bytes tested are the ASCII equivalents for the following string: "Does this thing actually work??", followed by the hex values AA (1010 1010 binary) and 55 (0101 0101 binary).

While the test is running the letter r is displayed.

The following error codes are reported for this test:

1	the buffer initially was not empty
2	the receive buffer should be empty but is not
3	the transmit buffer should be empty but is not
4	the receive buffer should have data but doesn't
5	data sent doesn't match the data received

Encoder Test (12)

This is a utility that displays the position of the two front panel knobs and indicates whether or not they are in the same position. When run, the test displays the current position of the REGISTER/PRESET knob and a + or – sign. The + sign is displayed if both the REGISTER/PRESET knob and the VALUE knob are in the same position. The – sign indicates that they are in different positions. To view the position of VALUE as the Z80 (U12) sees it, press and hold STORE/CLEAR. Note that the value displayed does not directly represent the binary value being read by the Z80. The Z80 reads the value then converts the grey scale values output by the encoders to contiguous values. The following table indicates the logic levels for the 16 positions of the encoders. These logic levels are located at U4 (74HC541):

Logic Levels at U4				
Displayed Value	SW-1	SW-2	SW-3	SW-4
0	1	1	1	1
1	1	1	0	1
2	0	1	0	1
3	0	1	1	1
4	0	0	1	1
5	0	0	0	1
6	0	0	0	0
7	0	0	1	0
8	0	1	1	0
9	0	1	0	0
A	1	1	0	0
B	1	1	1	0
C	1	0	1	0
D	1	0	0	0
E	1	0	0	1
F	1	0	1	1

When troubleshooting encoder problems, refer to above table that lists SW-1 to SW-4 logic level values at U4 (Input register 1 74HC541). Signals that are labeled SW1-1 to SW1-4 are associated with the REGISTER/PRESET encoder. Signals that are labeled SW2-1 to SW2-4 are associated with the VALUE encoder.

Press the STORE/CLEAR and PARAMETER/LEARN buttons together to exit the test.

Switch Test (13)

The switch test displays a number when each of the buttons are pressed as shown:

Front Panel	Footswitch
STORE/CLEAR = 1 PARAMETER/LEARN = 2 REGISTER/PRESET = 3	REGISTER STEP UP = 4 BYPASS = 5

Press the STORE/CLEAR and PARAMETER/LEARN buttons together to exit the test.

View Previous Test and Results Tool (14)

This tool allows you to view the error code from the last test that was run. When run, the last error code is displayed. Press PARAMETER/LEARN to display the ID number of the last test. This tool was included in case the error code flash is missed.

EEPROM Initialize Enable (15)

Performing this function sets a flag in the SRAM (U9) that enables the EEPROM (U7) to be initialized when you return to normal operating mode by selecting Test 9. This initialization writes the 16 factory presets 8 times into 120 user registers. It also initializes any corrupt registers variables, sets the DRAM size to 64K, disables the MIDI Bypass, sets the footswitch to "momentary", sets the MIDI channel to 1, clears all of the "Cleared Register Flags" and turns the OMNI Mode off.

MIDI Troubleshooting Tool (ALT 1)

This is a simple troubleshooting tool that continuously outputs a MIDI clock message (F8 hex) to the MIDI OUT port. To run this tool, press STORE/CLEAR. The display will indicate r. On a scope this looks like a 130us. pulse. Press PARAMETER/LEARN to disable Reflex's ability to detect incoming MIDI clock. To exit the tool, press STORE/CLEAR or PARAMETER/LEARN. To return to normal operating mode, select 9 with the REGISTER/PRESET knob, then press STORE/CLEAR again.

Sinewave Generator (ALT 2)

This is another troubleshooting tool that outputs a digitally-generated sinewave to the DAC (both outputs). When selected, the display indicates either **1.** (if the REGISTER/PRESET knob is in the RICH PLATE position) or **4.** (if the knob is in any other position). The **1** represents 1kHz and the **4** represents 440Hz. To output a sinewave at the indicated frequency, press any key. An r is displayed. Press any key to exit the generator. Because the sinewave is digitally generated the distortion at the output should be the lowest the system can produce (typical .01%). Output level is full scale for the converter (5.5dBu typical with the OUTPUT level CW).

Set DRAM Size (ALT 4)

This tool allows you to set the DRAM size to 64K, 256K or 1 Meg in the event that the installed DRAM is changed. Currently, Reflex has 64K DRAM installed. DRAM size is stored in the EEPROM (U7) and read each time the DRAM test is run. When the EEPROM is initialized, the DRAM size is set for 64K and stored in the EEPROM. The rule of thumb here is that either the EEPROM must be initialized before running the DRAM test or the operator must set the size. The size is set manually using diagnostics 4A (alternate mode). When selected, this diagnostic displays a number from 0-3 which can be changed by turning the VALUE knob. The size is set (written to the EEPROM) when STORE/CLEAR, PARAMETER/LEARN or REGISTER/PRESET is pressed. The + will flash on the display followed by 4. The values represent the DRAM sizes as follows:

0 = 64K
1 = 256K
2 = 1 Meg
3 = No DRAM size at this selection

Audio Performance

Oscillator and Analyzer Default Settings

Unless otherwise noted, the following settings are used for the audio performance tests:

Oscillator		Analyzer	
WAVEFORM	SINE	FILTER	OFF
OUTPUT	UNBAL	BANDWIDTH	22Hz-22kHz
	- 25Ω	INPUTS	100kΩ (except WETGAIN=600Ω)
	FLOAT		

Setup

1. Connect the appropriate cable between the oscillator output and the Reflex Left Input.
2. Connect the appropriate cable between the analyzer input and the Reflex Left Output.
3. Turn the Reflex front panel INPUT and OUTPUT knobs fully clockwise.
4. Turn the Reflex front panel MIX knob fully counterclockwise.
5. Power cycle Reflex while pressing and holding down the STORE/CLEAR and PARAMETER/LEARN buttons. Wait for the letter d to appear on the display, then release the buttons.
6. Press and hold the REGISTER/PRESET button until the display goes blank.
7. Turn the REGISTER/PRESET knob to select 9 RICH PLATE. The display should read: 8.
8. Press the REGISTER/PRESET button and verify that the + symbol, followed by an 8 flashes once on the display.

Dry Gain Test

This test checks the input to output gain characteristics of Reflex through the dry signal path.

1. Apply a 1kHz signal at -26dBV to the Reflex Left Input.
2. Set the scale on the distortion analyzer to measure +4dBV signal level.
3. Verify an output of 3.5dBV +/-0.56dBV at the Reflex Left Output.
4. Connect the oscillator output to the Reflex Right Input.
5. Connect the analyzer input to the Reflex Right Output.
6. Verify an output of 3.5dBV +/-0.56dBV at the Reflex Right Output.

Dry Signal-to-Noise

This test checks Reflex signal-to-noise through the dry signal path.

1. Set the scale on the distortion analyzer to measure -80dBV signal.
2. Disconnect the oscillator from the Reflex Input, or turn the oscillator off.
3. Verify that the noise floor is <77dBV.
4. Connect the oscillator output to the Reflex Left Input.
5. Connect the analyzer input to the Reflex Left Output.
6. Repeat the test, verifying the levels at the Reflex Left Output.

Dry THD+N

This test checks Reflex THD+N through the dry signal path.

1. Apply a 1kHZ signal at -26dBV to the Reflex Left Input.
2. Adjust the scale on the distortion analyzer to measure .025% THD+N.
3. Verify a distortion level <0.02% & >0.001% THD+N at the Reflex Left Output.
4. Connect the oscillator output to the Reflex Right Input.
5. Connect the analyzer input to the Reflex Right Output.
6. Verify a distortion level <0.02% & >0.001% THD+N at the Reflex Right Output.

Dry Frequency Response

This test checks the frequency response of Reflex through the dry signal path at the following frequencies:

20kHz 3kKz
5kHz 20Hz

1. Apply a -26dBV signal at 1kHZ with the analyzer BANDWIDTH filters off to the Reflex Right Input.
2. Set the scale on the distortion meter to measure +4dBV.
3. Use the output level at the Reflex Right Output for the 0dB reference to check frequency response.
4. Verify that the signal level output is within +/-0.56dB of the reference at the above frequencies.
5. Connect the oscillator output to the Reflex Left Input.
6. Connect the analyzer input to the Reflex Left Output.
7. Repeat the previous tests verifying levels for the Reflex Left Output.

SET THE MIX KNOB FULLY CLOCKWISE BEFORE PERFORMING THE FOLLOWING TESTS

Wet Gain

This test checks the input-to-output gain characteristics of Reflex through its wet signal path.

1. Apply a 1kHz signal at -26dBV (into a 600Ω load) to the Reflex Left Input
2. Set the scale on the distortion analyzer to measure +5dBV signal level.
3. Verify an output of 5.5dBV +/-1.56dBV at the Reflex Left Output.
4. Connect the oscillator output to the Reflex Right Input.
5. Connect the analyzer input to the Reflex Right Output.
6. Verify an output of 5.5dBV +/-1.56dBV at the Reflex Right Output.

Wet Signal-to-Noise

This test checks Reflex signal-to-noise through the wet signal path.

1. Set the scale on the distortion analyzer to measure -80dBV signal.
2. Disconnect the oscillator from Reflex, or turn the oscillator off.
3. Verify that the noise floor is <71dBV.
4. Connect the oscillator output to the Reflex Left Input.
5. Connect the analyzer input to the Reflex Left Output.
6. Repeat the test, verifying the levels at the Reflex Left Output.

Wet THD+N

This test checks Reflex THD+N through the wet signal path.

1. Apply a 1kHZ signal at -26dBV to the Reflex Left Input.
2. Adjust the scale on the distortion analyzer to measure .05% THD+N.
3. Verify a distortion level <0.05% & >0.005% THD+N at the Reflex Left Output.
4. Connect the oscillator output to the Reflex Right Input.
5. Connect the analyzer input to the Reflex Right Output.
6. Verify a distortion level <0.05% & >0.005% THD+N at the Reflex Right Output.

Wet Frequency Response

This test checks the frequency response of Reflex through its wet signal path at the following frequencies:

15kHz	100Hz
8kHz	20Hz
3kHz	

1. Apply a -30dBV signal at 1kHZ with the analyzer BANDWIDTH filters off to the Reflex Right Input.
2. Set the scale on the distortion meter to measure +4dBV.
3. Use the output level at the Reflex Right Output for the 0dB reference to check frequency response.
4. Verify that the signal level output is within +1.06dB/-3.56dB of the reference at the above frequencies.
5. Connect the oscillator output to the Reflex Left Input.
6. Connect the analyzer input to the Reflex Left Output.
7. Repeat the previous tests verifying levels for the Reflex Left Output.

Disassembly/ Reassembly

Disassembling the Unit

To disassemble the unit, use the following procedure:

1. Remove seven screws from the housing: one (1) from the rear panel, three (3) from the top, and three (3) from the bottom.
2. Carefully remove the unit's end caps, swinging them out by the rack ears.
3. Remove five (5) plastic nuts from the jacks on the rear panel.
4. Hold the front panel, and carefully remove the cover.
5. To disattach the circuit board from the front panel:
   - Pull off the five (5) knobs on the front panel
   - Remove the five (5) nuts and washers from the front panel.
   - Hold the unit face down, and carefully separate the circuit board assembly from the front panel.

     NOTE: The buttons are loose and can fall out.
   - Carefully remove the buttons from the rear of the front panel.

Reassembling the Unit

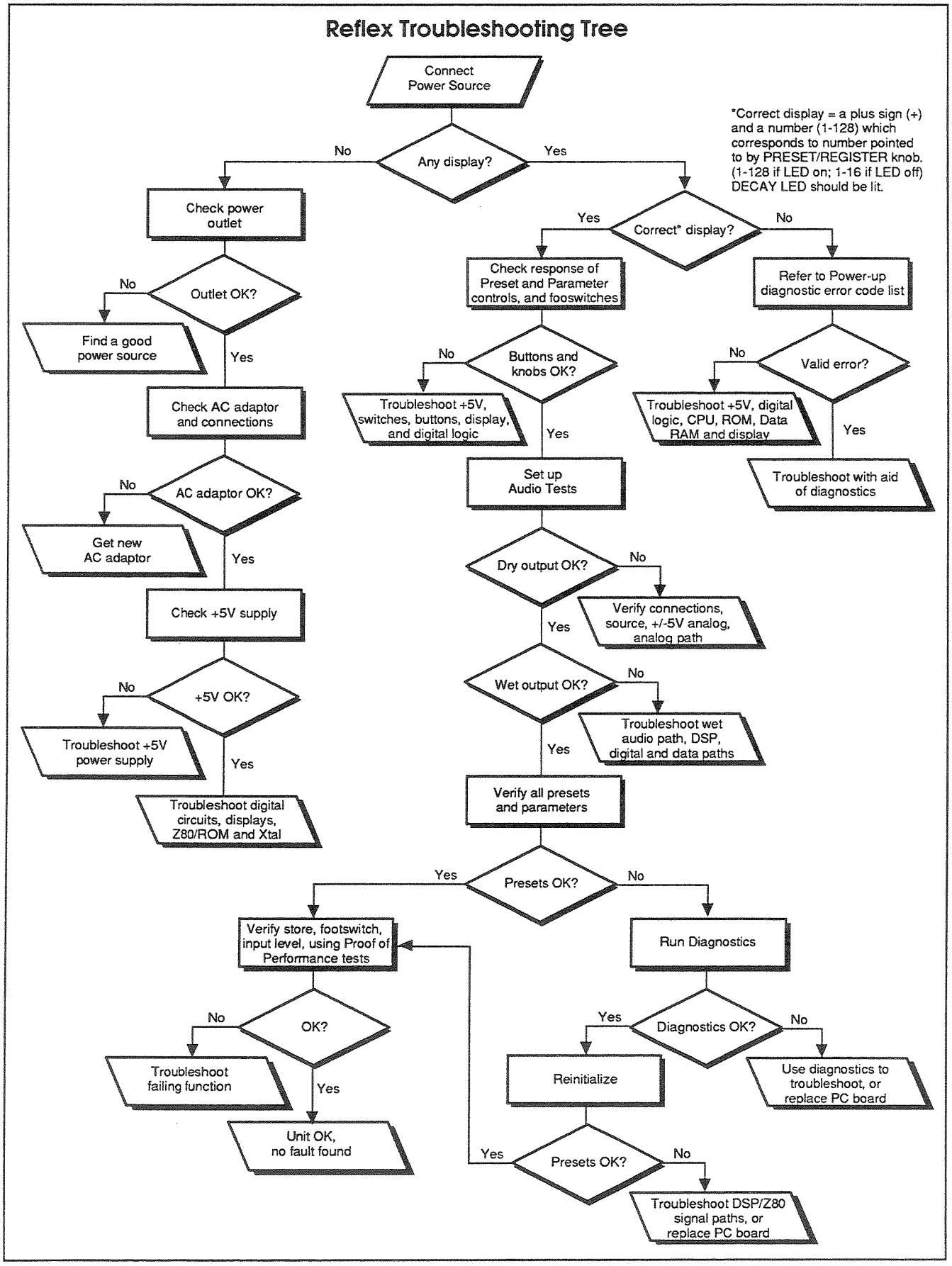
To reinstall the front panel and circuit board assembly:

1. Hold the front panel face down, and reinsert the buttons.
2. Continue to hold the front panel face down so as not to loosen the buttons. From the rear, carefully position the circuit board and insert it into the front panel. Replace the nut and washer on one potentiometer at each end and hand tighten.
3. Replace the remaining potentiometer nuts and washers. Check for alignment, then tighten all nuts. Do not overtighten.
4. Replace the cover, being careful to align the jacks, and the power connector with the holes in the rear of the cover.
5. Replace the five (5) plastic nuts on the jacks. Be careful not to over-tighten these, as the nuts can strip the threads of the jacks.
6. Replace the single screw in the rear of the unit, but do not tighten it.
7. Install the two end caps by hooking the rear tab of each into each end of the cover.
8. Holding the end caps in place, install the six (6) remaining screws. Tighten the rear-panel screws which are next to the power connector.

Removal and Installation of Components

From time to time, it may be necessary to replace pots, jacks, the display, or other components. When desoldering, be careful not to overheat the board, use all caution to prevent damage to the circuit board, traces and pads.

When installing pots, jacks or displays, make sure that they are mechanically flush with the circuit board prior to soldering in place. If not properly aligned, stress can be placed on the new components and the board — resulting in early failure of the board and/or component.


Reflex Troubleshooting Tree
Connect Power Source
Any display?
No
Yes
*Correct display = a plus sign (+) and a number (1-128) which corresponds to number pointed to by PRESET/REGISTER knob. (1-128 if LED on; 1-16 if LED off) DECAY LED should be lit.
Check power outlet
Outlet OK?
No
Yes
Find a good power source
Check AC adaptor and connections
AC adaptor OK?
No
Yes
Get new AC adaptor
Check +5V supply
+5V OK?
No
Yes
Troubleshoot +5V power supply
Troubleshoot digital circuits, displays, Z80/ROM and Xtal
Correct* display?
Yes
No
Check response of Preset and Parameter controls, and fooswitches
Refer to Power-up diagnostic error code list
Buttons and knobs OK?
No
Yes
Troubleshoot +5V, switches, buttons, display, and digital logic
Valid error?
No
Yes
Troubleshoot +5V, digital logic, CPU, ROM, Data RAM and display
Troubleshoot with aid of diagnostics
Set up Audio Tests
Dry output OK?
No
Yes
Verify connections, source, +/-5V analog, analog path
Wet output OK?
No
Yes
Troubleshoot wet audio path, DSP, digital and data paths
Verify all presets and parameters
Presets OK?
Yes
No
Verify store, footswitch, input level, using Proof of Performance tests
OK?
No
Yes
Troubleshoot failing function
Unit OK, no fault found
Run Diagnostics
Diagnostics OK?
Yes
No
Reinitialize
Use diagnostics to troubleshoot, or replace PC board
Presets OK?
Yes
No
Troubleshoot DSP/Z80 signal paths, or replace PC board

4 Theory of Operation

Analog and Converter Circuitry

Input stage

Separate unbalanced 1/4" phone jacks (J10 and J11) are provided for left and right input signals. A single input source will be routed to both left and right input stages by applying the signal to either input jack, thereby maintaining the proper operating level.

Capacitors (C66-69) at the inputs prevent unwanted high frequency interference from entering or leaving the Reflex through the input cables. DC isolation is accomplished by bipolar capacitors (C71 and C76) in line with the signal path. The left and right signals feed a dual potentiometer (R74) which controls the input signal level to the preamplifier stage. A dual op amp (U37) acts as a preamp by providing 30dB of gain.

The left and right outputs of the preamp are applied to the stereo Mix control (R64) and are also terminated by resistors (R68 and R69) which sum the left and right signals. This summed signal is applied to a passive 5-pole 16 kHz low pass filter (U36). The output of the filter goes to a pre-emphasis op amp stage whose output drives the sample and hold circuit.

SAH

The sample and hold circuitry consists of an op amp (U30), an SPDT analog switch (U31) and a capacitor (C51). The SAH is controlled by the SAMP signal command from the Lexichip II, which terminates at pin 11 of U31. When SAMP is high, pins 13 and 14 of switch U38 are shorted, which performs the sample function. At this time, the output level from pin 1 of U30 is used to charge C51.

The hold function takes place when SAMP goes low, shorting pins 12 and 14 of switch U31. The charge across C51 keeps audio level constant during the A/D conversion. SAH output is passed through an AC coupling capacitor (C48) and a pulldown resistor (R50) to prevent DC offsets from affecting system performance.

DAC

The analog to digital conversion is accomplished by a comparator (U29), the Lexichip II (U14), and a 16-bit digital-to-analog converter (DAC, U24). The SAH output is applied to pin 3 of the comparator; the output DAC output feeds pin 2. During the analog-to-digital conversion cycle, the internal successive approximation register (SAR) of the Lexichip II is used in conjunction with a DAC to output different voltages which are compared with the audio signal level. The conversion is complete when the two voltages are equal. After conversion, the L+R signal is processed digitally.

Separate left and right signals reappear after the analog-to-digital conversion and digital signal processing. At this time, the Lexichip II sends 16-bit data to the DAC, which converts it into analog voltage levels which are applied to the output hold circuitry.

Deglitch (Output Hold)

Separate output hold circuits are provided for reconstruction of the left and right audio signals. This circuitry includes a dual op amp (U32) and two analog switches (U31). DEG0 and DEG1 commands from the Lexichip terminate respectively at pins 10 and 9 of U31, providing separate control of the right and left output hold switches. During the digital-to-analog conversion cycle, either the DEG0 or DEG1 signal goes high when the DAC is ready to output the right or left analog voltage. This permits capacitors C56 or C62 to charge to the corresponding voltage level for the audio waveform. When the DEG0 or DEG1 signal goes low, the related capacitor will remain at the current signal level until the next conversion cycle.

Output Circuitry

The left and right signals from the output hold circuitry are applied to separate 5-pole passive low pass filters (U33 and U34). De-emphasis circuitry is incorporated into the signal path to compensate for the pre-emphasis function performed before the conversion process. A dual op amp (U35) with its associated circuitry provides the de-emphasis function.

The outputs of U35 are applied to one end of the stereo Mix control, R64. The other end of this potentiometer is connected to the outputs of the input preamplifier. By adjusting the wiper of the Mix control, the ratio of wet (processed) to dry (unprocessed) signal can be controlled.

The wipers of R64 are connected to one end of the Output level control, R49 through bipolar AC coupling capacitors (C64 and C65) to prevent DC offset voltages from appearing at the next stage. R49 adjusts the signal level being applied to the output amplfier, U27. This dual op amp provides unity gain and buffers the left and right signals separately.

Two analog switches (U28) provide output muting during power up or power down conditions. The RSTMUTE/ signal that controls these switches is generated from the reset circuitry and is terminated at pins 9 and 10 of U28. When the RSTMUTE/ is low, pins 4 and 5 of U28 are connected for the left output and pins 15 and 2 are connected for the right output, creating a low impedance signal path to ground. These switches are placed in parallel with the output level pot, before the output stage. The 2KΩ series resistors provide a minimum 25dB of attenuation when the switch is on (RSTMUTE/ is low).

An impedance of 75Ω is developed by R39 and R40 for the left and right outputs. These resistors also provide current limiting protection. The output 1/4" unbalanced phone jacks (J8 and J9) are configured in such a way that the left and right output signals are summed together if only the right jack (J9) is connected. The left jack (J8) can support stereo headphones if the right jack (J9) is not connected. The left channel appears on the tip, the right channel on the ring of a stereo phone plug through this 3-conductor 1/4" phone jack.

The output amps can drive high-impedance (>100 Ω) headphones, but are not designed for low impedance headphones. For best results, use a headphone amp. Finally, capacitors C41 and C42 prevent unwanted high freqency interference from entering or leaving the Reflex through the output cables.

Reset, System Processor, Memory Mapping, Interrupt Timer

Power Fail/Reset

Reset signaling is controlled by the +5VUNREG voltage. If the +5VUNREG voltage at the input of the +5V regulator (U17) is high enough to create a 2 volt or greater drop across the regulator (regulator dropout voltage = 2.0V = Vin - Vout) then the differential between the voltage divider (R29 and R30) at the emitter of Q4, and the regulated +5VD at the base of Q4 will be enough to turn on Q4.

As Q4 turns on, the voltage across R31 goes from 0V to about +6V. This voltage is the signal that allows the quad latch (U16) which generates the reset states to be cleared (power-down/brown-out) or have the reset states clocked through (power-up) by the monostable multlivibrator circuit (R22, C15, and U11).

During power down or brown-out all reset signals occur simultaneously as Q4 turns off and clears the reset latch (U16). On power-up the action of the various reset signals is sequential. This is due to the quad latch (U16) clocking its output states back through as inputs as desribed below.

Once the +5V digital rail is stabilized and the multivibrator is running, the Lexichip II (U14) and the UART (U2) will come out of reset (LRST/ and URST). This occurs well after (more than 230ms) the Lexichip crystal starts running . URST also clears the interrupt timer so, once the word clock is generated, there will be one complete interrupt period clocked through before the Z80 NMI has to be enabled.

70ms after this occurs, the Z80 will come out of reset (ZRST/). The Z80 needs to come out of reset after the Lexichip II is running because the Z80 derives its clock from the Lexichip. As the Z80 comes out of reset, the output registers are enabled (DISPLAYEN/), so the Z80 can write to the display, control the EEPROM clock for the reset circuit and disable the NMI.

The reset circuit proceeds normally, as on power-up. EEPCLK is pulled low by a 10kΩ resistor (R78), allowing U16 to be clocked by the oscillator until the Z80 writes EEPLCK as high. EEPLCK is written high when the Z80 comes out of reset, disabling the oscillator from clocking through RSTMUTE/ signal. This is accomplished by gating the oscillator output with the EEPCLK signal using an AND gate (U42). The RSTMUTE/ signal will now get set the first time the EEPROM gets written to or EEPCLK goes low for two oscillator periods. This will be sometime after the power-up diagnostics have run and the WCS is initialized.

Z80, ROM, RAM, Memory Map

A Z80 microprocessor (U12) is utilized as the Host Processor for the Reflex. Its primary responsibilities are:

- Processing of data and instructions to and from the UART (U2)
- Processing of data and instructions to and from the Lexichip II (U14)
- Handling of user control and front panel display

48Kbytes of ROM space are used in a single 27C512 PROM (U8).Audio effects, diagnostics, I/O and housekeeping subroutines are contained in this memory space.

The Z80 scratch pad memory is 8Kbytes SRAM. This RAM (U9) space is volatile and any system parameter changes made must be copied into EEPROM (U7) to be saved on power down.

The Lexichip II contains its own on-board program RAM and I/O registers which are addressable by the Z80. The Lexichip II occupies 1K of the Z80's 64K addressable memory space.

The address decoding scheme is very simple. Memory mapping is used exclusively. The memory map consists of: one 48k block for ROM, one 8k block for SRAM, and eight 1k blocks for I/O and peripherals, of which only four 1K blocks are used. The decoding circuitry consists of three sections: (U11) HC14 inverter, one section of (U42) OR gate and (U10) HC138, a 3 to 8 demultiplexer.

ADDRESS (HEX)	SIZE	SIGNAL	DESCRIPTION
E000 - FFFF	8k	RAM/	RAM select
DC00 - DFFF	1k	N/C	Not used
D800 - DBFF	1k	N/C	Not used
D400 - D7FF	1k	N/C	Not used
D000 - D3FF	1k	N/C	Not used
CC00 - CFFF	1k	IO2/	Output Register 2 select, ORed with WR/ Input Register 2 select, decoded at chip by RD/
C800 - CB00	1k	IO1/	Output Register1 select, ORed with WR/ Input Register 1 select, decoded at chip by RD/
C400 - C7FF	1k	UART/	UART select
C000 - C3FF	1k	LEX/	Lexichip select
0000 - BFFF	48k	EPROM/	ROM select

64k Total Z80 memory space

NMI/ Circuit (Interrupt Timer)

The interrupt timer consists of half of a dual 4-bit binary counter (U15), one section of a Schmidt inverter (U11), and one half of a flip flop (U13). After power-up, once the Z80 is running and U15 is released from reset, it will count 16 high to low WC/ transitions. Transitions occur every Lexichip-generated word clock period of 32µs. Interrupts to the Z80 occur every 512uS with a low pulse of approximately 32uS. The negative transition of this pulse triggers the interrupt. This interrupt period offers ample time for the Z80 to perform its housekeeping and critical timing related task without worrying about MIDI IN while in the NMI routine.

The Z80 uses the NMI/ to service the timer interrupt. The NMI/ can be masked (DISABLEINT/) by writing a 0 to pin 8 of Output Register 2. DISABLEINT/ is the data input for the flip-flop (U13) which gets clocked by the WC counter to generate the NMI/.

If DISABLEINT/ = 0, the NMI/ signal will always be clocked through as HIGH and the NMI/ will never be asserted at the Z80.

If DISABLEINT/ = 1, the NMI/ signal will get clocked as a LOW pulse of approximately 32µs as previously desribed . The actual negative-going edge of this pulse triggers the interrupt.

NMI behavior on Power Up

In the Interrupt Timer circuit, NMI/ is generated from a flip-flop whose output is not predictable on power up. DISABLEINT/ (the D input) is set by the Z80 as soon as it comes out of reset on power up. After this occurs, the Z80 writes to the Lexichip to program its word clock as an output so that the interrupt timer will begin being clocked.

NMI/ is at a HIGH or LOW steady state. The Z80 NMI/ input is negative edge triggered. When the Lexichip is reset on power-up, the chip defaults to being a slave and attempts to syncronize its internal word clock to any external signal on the WORD CLOCK pin. The Z80 has to program the Lexichip to become the WC master. When the Lexichip is the word clock master, it drives its internal word clock out on WC/, pin 59 of U14.

The Interrupt Timer cannot increment until the Z80 tells the Lexichip to be the WC master. Because the Interrupt Timer is not incrementing on power-up, NMI/ cannot occur. This is the normal mode of operation.

Because the interrupt timer counter (U11) gets reset on power-up, the first time NMI/ can change state is when the Qd O/P of the counter goes HIGH. This will occur after 8 WC/ are generated after power up (256µs) if DISABLEINT/ is set high.

INT/ CKT (MIDI IN)

The Z80 INT/ input is dedicated to servicing MIDI IN. The RxRDY (UARTINT) output becomes 1 when the UART receives one character of data and transfers that data to the receive data buffer; that is, when the data can be read. RxRDY output is the same as bit 1 in the status register which is read in the polling application.

UARTINT gets inverted by U11 to generate INT/ which is tied to the INT/ input on the Z80. When the Z80 gets reset on power-up the INT/ is disabled by default. This interrupt must be software enabled before it can used.

Front Panel, Foot Switches, MIDI I/O, EEPROM

I/O Registers

There are two output registers, U6 (74LS374) and U5 (74HC374) and two input registers, U4 (74HC541) and U3 (74HC541). Output Register 1 and Input Register 1 (U6 and U4) share the same memory space. The outputs and inputs are separately decoded using the read and write signals. The same is true for Output Register 2 and Input Register 2 (U5 and U3).

O/P Registers

OUT1 (U6) drives the 24 display LED segments. The three digits of the display are time-multiplexed. Approximately every 6 ms, two digits are turned off and the other digit is turned on. To drive the middle digit (LSD), the Z80 writes to OUT2 (U5), a 0 to pin 3, and a 1 to pin 18 and 17. This turns on Q3 and turns off Q2 and Q5. Q3's collector sources current into the common anode of the middle digit on the display board. At the same time, the Z80 writes 0's to the appropriate segment outputs of U6. U6 must be an LS part because an HC part can't sink enough current to drive a multiplexed display. Each output of U6 has a 270 Ω series resistor to current limit the LEDs on the display board.

As an HC374 can directly drive a non-multiplexed LED, U5 directly drives the input level indicator LED (D6). D6 is a bicolor LED, which can switch between red and green. R11, R12, and R34 are used to current limit the input level LED and provide equal intensity for both colors. The RED/ and GRN/ signals work together to select color. If GRN/ is high and RED/ is low, the level LED lights red. If GRN/ is low and RED/ is high, the level LED lights green.

Note the output registers are disabled (DIPLAYEN/) on reset so the display will be blank when the Z80 is not running.

The following table shows the LED matrix at Output Register 1 when the MSD at Output Register 2 is active 0. The MSD drives the overflow digit display and the front panel LEDs. Only MSD, LSD or XSEG can be active 0 at any given time.

Overflow Digit

(MSD active 0; LSD active 1; XSEG active 1)

Data Bit <0:7>	Signal Name	Active State	Description
0	DECAY/	0	Turns on front panel DECAY LED
1	b/	0	Turns on **b** segment of overflow digit display
2	c/	0	Turns on **c** segment of overflow digit display
3	d/	0	Turns on + segment of overflow digit display
4	REG/	0	Turns on front panel REGISTER/PRESET LED
5	DELAY/	0	Turns on front panel DELAY LED
6	g/	0	Turns on – sement of overflow digit display
7	FXLVL/	0	Turns on front panel FX LVL LED

The followingtable shows the LED matrix at Output Register 1 when the LSD at Output Register 2 is active 0. The LSD drives the middle 7-segment display. Only MSD, LSD or XSEG can be active 0 at any given time.

Middle Digit
(LSD active 0; MSD active 1; XSEG active 1)

Data Bit <0:7>	Signal Name	Active State	Description
0	a/	0	Turns on a segment of middle digit display
1	b/	0	Turns on b segment of middle digit display
2	c/	0	Turns on c segment of middle digit display
3	d/	0	Turns on d segment of middle digit display
4	e/	0	Turns on e segment of middle digit display
5	f/	0	Turns on f segment of middle digit display
6	g/	0	Turns on g sement of middle digit display
7	dp/	0	Turns on decimal point of middle digit display

The followingtable shows the LED matrix at Output Register 1 when XSEG at Output Register 2 is active 0. XSEG drives the least significant digit display. Only MSD, LSD or XSEG can be active 0 at any given time.

Least Significant Digit
(XSEG active 0; MSD active 1; LSD active 1)

Data Bit <0:7>	Signal Name	Active State	Description
0	a/	0	Turns on a segment of least significant digit display
1	b/	0	Turns on b segment of least significant digit display
2	c/	0	Turns on c segment of least significant digit display
3	d/	0	Turns on d segment of least significant digit display
4	e/	0	Turns on e segment of least significant digit display
5	f/	0	Turns on f segment of least significant digit display
6	g/	0	Turns on g sement of least significant digit display
7	dp/	0	Turns on decimal point of least significant digit display

The followingtable defines Output Register 2.

Data Bit <0:7>	Signal Name	Active State	Description
0	RED/	0	If GRN/ is 1, and RED/ is 0, Level LED lights red
1	GRN/	0	If GRN/ is 0, and RED/ is 1, Level LED lights green
2	LSD/	0	Activates middle digit display. Only LSD/, MSD/ or XSEG/ can be active.
3	MSD/	0	Activates overflow digit display. Only LSD/, MSD/ or XSEG/ can be active.
4	XSEG/	0	Activates least significant digit display. Only LSD/, MSD/ or XSEG/ can be active.
5	EEPDAI	0/1	EEPROM serial data and address
6	EEPCLK	0/1	EEPROM serial clock
7	DISABLEINT/	1	Control signal to disable NMI/

EEPROM 64kbits (8k x 8), 24C65 interface

Non-volatile data storage is incorporated with 2 wire serial/I^2C EEPROM. This serial EEPROM (U7) uses a two wire bus protocol. Pin 5 of U7 is the serial address/data input/output. This is a bidirectional pin used to transfer addresses and data into and out of the device. Pin 6 of U7 is the serial clock input used to synchronize the data transfer to and from the device.

Output reg 2 (U5) bits 5 and 6 are used to generate the serial clock and data for the EEPROM. Input reg 2 bit 7 is used to read the serial data from the EEPROM.

Software requirements

After addressing the EEPROM, EEPDAI must remain in a high logic state, so that the EEPROM SDA signal can pull this signal to a low logic level to generate an acknowledge pulse after the reception of each byte.

A note on the electrical interface for the EEPROM data I/O

A series resistor (R75) is added between the output data port of Output register 2 and the bidirectional data port on the EEPROM. When trying to read from the EEPROM, the two outputs drive each other. As both devices are CMOS, no current will be flowing when their outputs are at the same logic level, and the devices will not be driving each other. If the outputs are at different logic states, the EEPROM will be pulling its output up or down during a read operation. When the EEPROM is not being addressed it goes into a standby mode where the data pin sits at a high logic level.

The EEPROM interface is essentially a programmable Z80 serial port which uses two bits of Output Register 2 for writing addresses/data and clocking and one bit of Input Register 2 to read data back.

I/P Registers

The two input registers (U4 and U3, 74HC541) are used for reading front panel switches (S2, S4, S5) and encoders (S1 and S3), as well as the footswitches (J3 and J4) and EEPROM serial data. It is necessary to have pullup resistors at the rotary encoders greater than 31kΩ because the on resistance for the encoders is specified to be less than 5kΩ. RP2 serves this function. RP1 pulls up the inputs to input register 2, preventing U3 inputs from floating and providing a default non-active switch state of logic high. Footswitch jacks J3 and J4 use resistors (R4, R5) and capacitors (C1, C2) to filter out RFI.

The followingtable defines Input Register 1. Encoders output gray scale code.

Data Bit <0:7>	Signal Name	Active State	Description
0	SW1-1	0	Value Adjust encoder bit 0 (LSB)
1	SW1-2	0	Value Adjust encoder bit 1
2	SW1-3	0	Value Adjust encoder bit 2
3	SW1-4	0	Value Adjust encoder bit 3 (MSB)
4	SW2-1	0	Register/Preset Select encoder bit 0 (LSB)
5	SW2-2	0	Register/Preset Select encoder bit 1
6	SW2-3	0	Register/Preset Select encoder bit 2
7	SW2-4	0	Register/Preset Select encoder bit 3 (MSB)

The followingtable defines Input Register 2.

Data Bit <0:7>	Signal Name	Active State	Description
0	PARAM/	0	Parameter Select switch
1	REG-PRE/	0	Register/Preset Select switch
2	STR-CLR/	0	Store or Clear Register function switch
3	FOOT-BYP/	0	Footswitch Select for Bypass function
4	FOOT-REG/	0	Footswitch Select for Register Step function
5	FS2TIP/	0	not used
6	FS2RING/	0	not used
7	EEP_DAO	0/1	Serial data from EEPROM

MIDI I/O

The MIDI interface utilized by Reflex complies with the MIDI specification. It incorporates 5-pin, female DIN connectors for input and output (J2 and J1). MIDI IN is opto-coupled for ground isolation through U1 to the UART, U2. The MIDI OUT signal is provided by the UART and is fed to current loop driver Q1 and out J1. FB1 and FB2 are used to reduce RFI radiation. Jumper W2 is provided for alternately configuring J1 as a MIDI THRU jack instead of MIDI OUT

The Z80 uses the UART as a peripheral I/O device and programs it to communicate in an asynchronous serial data protocol. The UART data available output (RxRDY, pin 14) which signals that the UART has received a complete character, is inverted by section of the U11 Schmidt inverter before being used to interrupt the Z80.

The UART runs at 4mHz (ZCLKDLYD/). This is a dedicated clock which is the complement of ZCLKDLYD. The spec states the clock frequency must be more than 4.5 times the TxCLK or RxCLK in async mode using x16 clock mode.

The MIDI spec Transmit and Receive Baud rate = 31.25k. TxCLK/RxCLK = 31.25k x16 = 500kHz. Therefore, the UART CLK must be greater than 4.5 x 500kHz (2.25mHz), and less than 8mHz (max clock freq for UART).

The TxCLK and RxCLK is divided down from ZCLKDLYD with half of a dual 4-bit binary counter (U11) to derive the 500kHz clock signal.

Lexichip II, DRAM, Clocks

The Lexichip II (U14) performs all of digital effects processing for the Reflex. It receives instructions from its internal program RAM, referred to as the Writeable Control Store (WCS). Address, data, and control lines for the WCS, as well as various Lexichip II control and status registers are shared with the Z80 bus.

This allows the Z80 to load audio effects programs into the Lexichip II, monitor status of audio data, and synchronously change program parameter values in the audio programs. The Z80 treats this memory as RAM mapped memory in its memory space between addresses C000 and C307 HEX.

An internal crystal oscillator driver circuit drives a 16MHz crystal mounted across pins 75 and 76 on the Lexichip II. Internal Lexichip II circuitry divides this clock frequency down to provide the 4MHz ZCLK. ZCLK clock is reclocked by a 16MHz master clock generated by the Lexichip II using one half of U13 (74HC74). This is to ensure setup and hold times for writing Lexichip II WCS. The reclocked ZCLK (ZCKDLY) is also divided by four with one half U15 and used for the Baud clock on the UART. The inverted reclocked ZCLK(ZCLKDLY/) from U13, pin 8 is used as the 4MHz UART clock. All clock signals are conditioned with 100Ω dampening resistors. The same is true for Lexichip II DRAM addresses and control signals.

Word Clock (pin 59) from the Lexichip is used as the clock reference for Reflex. It operates at 31.25kHz rate and is the heartbeat of interrupt timing circuitry as explained in the Z80 interrupt timer section.

Audio memory is configured with 4) 64K X 4bit DRAMS (U38, 39, 40, 41) with layout supporting 4) 256K X 4bit or 4) 1M X 4bit chips (U20, 21, 22, 23). This provides the LEXICHIP with 64K by 16-bit memory for audio data storage. Memory speeds of 100ns or faster are more than adequate when the Lexichip is running at 16MHz. DRAM read, write, and refresh functions are performed by a dedicated set of address and control lines, and a 16-bit wide data bus provided by the LEXICHIP.

DAC/ADC Control Logic and Data Port

Internal control logic circuitry enables the Lexichip to command complete control over external DAC functionality with minimal external circuitry.

Two 8-bit latches (U18 and U19) are used to latch 16-bit data out to the DAC via the DAB (digital audio bus). Lexichip output CCLK1 clocks data into these DAC conversion latches.

An internal Successive Approximation Register (SAR) allows the DAC, in conjunction with an external comparator, to perform analog to digital conversions. A data value is latched into the conversion latch, DAC output is compared to the analog input by the comparator. The resulting output data (DATA) is applied to Lexichip input SI1, and the SAR logic circuitry determines either the the next DAC output or an end of conversion. Converted data is then processed by the Lexichip with instructions from its WCS.

DAC logic signals are provided by the Lexichip to control the Sample and Hold (SAH) and deglitch functions and conversion data latching. A Word Clock signal (WC/) is used as a clock reference and indicates the beginning of a conversion cycle.

On the falling edge of WC/, SAMP goes low in order to hold an input sample for A/D conversion. The internal SAR then applies a DAC output t DAB0-15. This data is latched into the conversion latches on the positive edge of the CCLK1 signal. The DATA signal from comparator is then compared by the Lexichip to determine the next SAR value. Sixteen SAR output samples are required to perform an analog conversion. Since the later samples produce smaller voltage changes on the DAC output, less time is required for the DAC to settle. The time duration between CCLK1 pulses toward the end of the A/D conversion is, therefore, reduced.

The 17th CCLK1 pulse after WC/ latches left channel data out to the DAC. After sufficient DAC settling time, the left channel deglitch switch is disabled by the high state of DEG0, applying a DAC sample to the left channel output circuitry. The last CCLK1 pulse in the WC/ cycle latches right channel data to the DAC. DEG1 goes high which applies the DAC sample to right channel output circuitry.

Power Supply

The Reflex power supply provides three regulated DC output voltages: +5VDC for digital circuits, +5VDC for analog circuits, and -5VDC for analog circuits.

AC power is provided by an external transformer rated at 9VAC @1.0A. The transformer output is terminated with a 5 mm/2.5 mm barrel type connector (J5), with its mating input jack located on the Reflex rear panel. A .01 µF capacitor (C32) is connected across the AC input to help prevent noise spikes from entering the unit. In addition, C32 and C33 stop circuit generated RFI from radiating through the power line.

The single 10 Ω series resistor (R33) that is shared by the inputs to the analog voltage regulators (U25 and U26) prevents one rail from rising much faster than the other. This quiets down the output op-amp's transients and makes for better audio muting.

All three regulated supplies (+/- 5 VDC analog and +5 VDC digital) consist of a single diode (D4, D5, and D3) used as a half-wave rectifier to produce the unregulated 5 volt supply (approximately 10 VDC) across each supply's filter capacitor (C34, C35, and C26). The analog supplies use 1000 µF electrolytics and the digital supply uses a 3300 µF electrolytic capacitor due to the added load of more circuitry and front panel display. Each supply is post-regulator filtered with a 22 µF capacitor (C39, C40, and C23). The +5VUNREG supply is monitored by the reset circuit for power up and power fail conditions.

Voltage regulation is handled by three TO220 packaged ICs:

+5VDC digital circuits - U17 (7805)
+5VDC analog circuits - U25 (7805)
-5VDC analog circuits - U26 (7905)

Current limiting and short circuit protection are incorporated into the internal circuitry of these ICs.

MAIN BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
POTENTIOMETERS			
200-09545	POT,RTY,PC,50KAX2,6MMFL,16,17L	2	R49,74
200-09546	POT,RTY,PC,10KBX2,6MMFL,16,17L	1	R64
RESISTORS			
202-00505	RES,CF,5%,1/4W,10 OHM	2	R33,38
202-00512	RES,CF,5%,1/4W,75 OHM	2	R39,40
202-00514	RES,CF,5%,1/4W,100 OHM	6	R8,23-26,32
202-00518	RES,CF,5%,1/4W,220 OHM	3	R1-3
202-00520	RES,CF,5%,1/4W,270 OHM	11	R10-17,19,20,34
202-00521	RES,CF,5%,1/4W,330 OHM	2	R70,73
202-00529	RES,CF,5%,1/4W,1K OHM	3	R18,21,37
202-00533	RES,CF,5%,1/4W,2K OHM	8	R28,35,36,41-44,76
202-00534	RES,CF,5%,1/4W,2.2K OHM	2	R9,75
202-00541	RES,CF,5%,1/4W,4.3K OHM	2	R68,69
202-00542	RES,CF,5%,1/4W,4.7K OHM	2	R4,5
202-00549	RES,CF,5%,1/4W,10K OHM	2	R50,78
202-00580	RES,CF,5%,1/4W,1M OHM	2	R22,27
203-00455	RES,MF,1%,1/4W,681 OHM	1	R30
203-00456	RES,MF,1%,1/4W,1.00K OHM	1	R29
203-00459	RES,MF,1%,1/4W,2.00K OHM	6	R45-47,55,59,62
203-00471	RES,MF,1%,1/4W,10.0K OHM	3	R31,66,71
203-02010	RES,MF,1%,1/4W,4.87K OHM	2	R58,63
203-02611	RES,MF,1%,1/4W,5.62K OHM	4	R51,52,60,61
203-02658	RES,MF,1%,1/4W,340 OHM	2	R67,72
203-08191	RES,MF,1%,1/4W,2.21K OHM	6	R48,53,54,56,57,65
205-02212	RES,NET,SIP,2%,BUS EL,47KX9	2	RP1,2
205-03531	RES,NET,SIP,2%,BUS EL,10KX5	1	RP3
205-09499	RES,NET,SIP,2%,ISOL EL,100X4	3	RP4-6
CAPACITORS			
240-00611	CAP,ELEC,22UF,16V,RAD	2	C39,40
240-06096	CAP,ELEC,10UF,25V,RAD,NON-POL	5	C48,64,65,71,76
240-06611	CAP,ELEC,1000UF,25V,RAD	2	C34,35
240-09541	CAP,ELEC,3300UF,16V,RAD	1	C26
241-00654	CAP,TANT,22UF,16V,RAD	1	C23
244-01151	CAP,PP,1000PF,2.5%	1	C51
244-06883	CAP,MYL,.01UF,5%,RAD	3	C50,57,63
245-00590	CAP,CER,150PF,500V,10%,Y5P	4	C41,42,67,68
245-01258	CAP,CER,470PF,50V,10%,Z5P	3	C33,66,69
245-03609	CAP,CER,.1UF,50V,Z5U,AX	42	C5-17,20-22,24,25
245-03610	CAP,CER,.01UF,100V,Z5U,AX	2	C32,36
245-03867	CAP,CER,10PF,100V,COG,10%,AX	2	C18,19
245-03869	CAP,CER,100PF,100V,COG,10%,AX	2	C1,2
245-07344	CAP,CER,470PF,100V,COG,10%,AX	2	C56,62
245-07544	CAP,CER,18PF,100V,COG,10%,AX	3	C49,70,75
FERRITE BEAD			
270-00779	FERRITE,BEAD	2	FB1,2
DIODES			
300-01029	DIODE,1N914 AND 4148	1	D1
300-01030	DIODE,1N4004 AND 4005	3	D3-5

PART NO.	DESCRIPTION	QTY	REFERENCE
TRANSISTORS			
310-01646	TRANSISTOR,2N4403	5	Q1-5
INTEGRATED CIRCUITS			
330-01293	IC,DIGITAL,74LS374	1	U6
330-03581	IC,DIGITAL,74HC138	1	U10
330-03583	IC,DIGITAL,74HC374	1	U5
330-03585	IC,DIGITAL,74HC14	1	U11
330-03638	IC,DIGITAL,74HC393	1	U15
330-04509	IC,DIGITAL,74HC74	1	U13
330-07260	IC,DIGITAL,74HC32	1	U42
330-07536	IC,DIGITAL,74HC574	2	U18,19
330-07715	IC,DIGITAL,74HC541	2	U3,4
330-08169	IC,DIGITAL,74HC175	1	U16
330-09350	IC,DIGITAL,LEXICHIP 2A	1	U14
340-00725	IC,LINEAR,LM311	1	U29
340-00742	IC,LINEAR,7805 (LM 340 T-5)	2	U17,25
340-01525	IC,LINEAR,7905,-5V REG	1	U26
340-01566	IC,LINEAR,LF353,DUAL OP AMP	2	U30,32
340-06036	IC,LINEAR,UPC4570,DUAL OP AMP	2	U35,37
340-08950	IC,LINEAR,RC4556	1	U27
345-06037	IC,INTER,82C51A	1	U2
346-06896	IC,SS SWITCH,74HC4053	2	U28,31
350-04434	IC,DRAM,64KX4,120NS	4	U38,39,40,41
350-09611	IC,SRAM,8KX8,150NS,.3"	1	U9
350-10225	IC,EEPROM,24C65,64K,SER	1	U7
350-10230	IC,ROM,27512,REFLEX,V1.00	1	U8
355-06038	DAC,PCM54HP	1	U24
365-04834	IC,UPROC,Z80B,CMOS,6MHZ	1	U12
375-02247	IC,OPTO-ISOLATOR,6N138	1	U1
380-09525	MOD,LPF,LC,5P,16KHZ	3	U33,34,36
CRYSTALS			
390-06647	CRYSTAL,16.000 MHZ,.01%	1	Y1
DISPLAYS/INDICATORS			
430-07325	LED,RED,T1,LITON	1	D2
430-07337	LED,T1,RED/GRN	1	D6
SWITCHES			
452-09555	SW,RTY,BCD,16POS,17.5MM	2	S1,3
453-09550	SW,PBM,1PIT,6MM SQ,PCRA,130GF	3	S2,4,5
CONNECTORS			
490-02356	CONN,JUMPER,.1X025,2FCG	1	W1 JUMP PIN 1 & 2
510-02671	CONN,POST,100X025,HDR,3MC,GOLD	1	W1
510-06042	CONN,DC POWER,PC,DJ005,2.5MM	1	J5
510-09553	1/4"PHONE JACK,PCRA,3C,SW,OF	2	J3,8
510-09554	1/4"PHONE JACK,PCRA,2C,SW,OF	3	J9,10,11
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	2	J1,2
SOCKETS			
520-01458	IC SCKT,28 PIN,PC,LO-PRO	1	U8
520-06184	IC SCKT,PLCC,84 PIN	1	U14
HARDWARE			
620-09648	LUG,SOLDER,.5IDX.72OD/FL.25TAB	5	J3,8,9,10,11
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	2	HEATSINK GND BRKT MTG

PART NO.	DESCRIPTION	QTY	REFERENCE
BRACKET			
701-09640	BRACKET,KEYSTONE,#621,4-40	1	GND BRKT
HEAT SINK			
704-09508	HEAT SINK,TO-220,THERM,7019B	1	U17

DISPLAY BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
DISPLAYS/INDICATORS			
430-07325	LED,RED,T1,LITON	3	D1-3
430-09549	LED,DSPLY,7-SEG,RED,1.5DIG,.56	1	DISP1
CONNECTORS			
510-09551	CONN,POST,100X025,HDR,3MC,RA	1	J2
510-09552	CONN,POST,100X025,HDR,7MC,RA	1	J1

MECHANICAL PARTS

PART NO.	DESCRIPTION	QTY	REFERENCE
TRANSFORMERS			
470-09650	XFORMER,PLUG-IN,120V,9VAC,10MM	1	
470-10162	XFORMER,PLUG-IN,9VAC,1A,MSA-E	1	
470-10164	XFORMER,PLUG-IN,9VAC,1A,MSA-UK	1	
470-10166	XFORMER,PLUG-IN,9VAC,1A,MSA-J	1	
HARDWARE			
550-09570	KNOB,17.5MM,6MM/FL,BLK/WHT LN	5	
550-09610	BUTTON,.16X.61,BLK	3	
641-10243	SCRW,4-40X3/8,TH,T9,BZ,LOK	7	END CAPS (4),
644-09567	WSHR,INT,STAR,7MM,ZN	2	MAIN BD
MECHANICALS			
700-10220	COVER	1	
702-09564	PANEL,SIDE CASTING,BLK	2	
702-10218	PANEL,FRONT	1	
703-09537	LENS,DISPLAY	1	
720-09539	TAPE,FOAM,.032X.25X7		

6 Schematics

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