Service Packet

PCM 70

Digital Effects Processor

lexicon

Safety Precautions

Service operations must only be performed by a qualified service technician. If you have any doubts about your ability to perform a procedure, please contact Lexicon for assistance.

> **WARNING!** Hazardous voltages exist inside this unit when the power cord is connected; use extreme caution when servicing and adjusting. Always place the unit on an isolation transformer before servicing.

Static Electricity Precautions

Many of the PCM 70's internal components are extremely sensitive to static electricity. The following practices minimize possible damage to components resulting from electrostatic discharge:

1. Minimize handling of boards and integrated circuits (ICs).
2. Keep parts in original containers until ready for use.
3. Discharge personal static before handling devices.
4. Use antistatic containers for handling and transport.
5. Do not slide devices over a surface.
6. Avoid plastic, vinyl, or styrofoam in the work area.
7. Handle ICs only at a static-free work station.
8. Use only grounded-tip soldering irons.

Notice

Lexicon, Inc. reserves the right to make changes in this service packet and the product it describes at any time and without notice or obligation.

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100 Beaver Street
Waltham, MA 02154
(617) 891-6790
Telex 923 468

Printed in the United States of America

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Obtaining Factory Service and Parts

Returning Units For Service

Before returning a unit, always consult with Lexicon to determine the extent of the problem.

If you choose to return a PCM 70 to Lexicon or a designated facility for service, Lexicon assumes no responsibility for the unit in shipment from customer to factory, whether in or out of warranty. All shipments must be well-packed (using the original packing materials, if possible), properly insured, and consigned to a reliable agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Address
- City, State, Zip Code
- Telephone Number (include Area Code)
- Serial number of unit
- Description of problem
- Desired return date
- Preferred method of return shipment

Please include a brief note describing conversations with Lexicon personnel, and give the name and telephone number of the person directly responsible for maintaining the unit. Do *not* include accessories such as manuals, remote switches, etc.

Ordering Parts

When ordering parts, identify each part by its type, value, and Lexicon Part Number. Example:

10 kilohm rotary potentiometer, Lexicon # 200-02616

Replacement parts can be ordered from:

Lexicon, Inc.
100 Beaver Street
Waltham, MA 02154 USA
(617) 891-6790
Telex 923 468
Attn: Customer Service

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Description and Specifications

2.1 Description and Controls

The PCM 70 is a sophisticated Digital Effects Processor with more than 40 digital effects and reverb programs, including Chorus and Echo, Resonant Chords, Multiband Delays, Rich Chamber, Rich Plate, and Concert Hall. More than 70 parameter types can be edited to produce just the sound you need. The PCM 70 is equipped with Lexicon's Dynamic Midi™, offering real-time remote control of up to 10 parameters at the same time from a MIDI keyboard or sequencer. Below is a brief description of the front and rear panel controls and connectors. For detailed operating instructions and a comprehensive description, refer to the *PCM 70 Owner's Manual*, part # 070-04337.

2.1.1 Front Panel Controls and Indicators

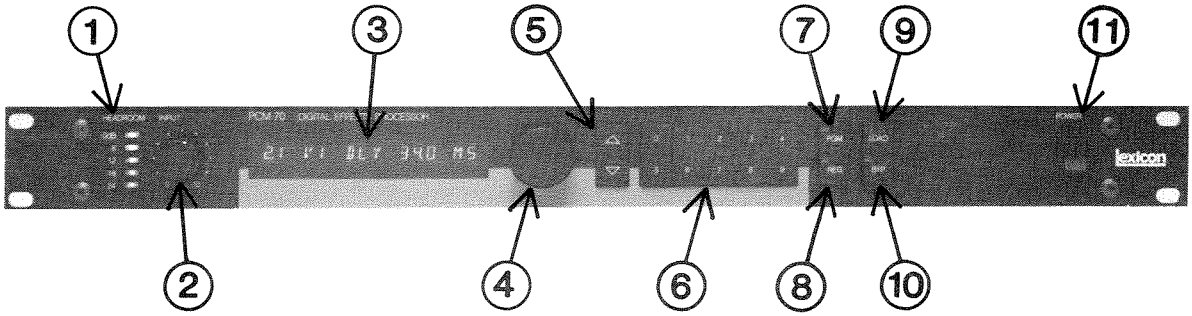

Figure 2.1. PCM 70 front panel.

1 Headroom Indicator

This five-segment LED display shows signal level and headroom available for the input signal. For optimum performance, adjust the input level so that all the LEDs *except* the red 0 dB indicator flash on peaks. When the red LED flashes there is no more headroom available before clipping or overload occurs. The input signal level is too high, and should be reduced.

2 Input Level Control

This rotary knob controls the level of the input signal. If the red LED in the headroom indicator flashes, lower the input level with this control.

3 Display Window

The Display Window indicates the location number and name of a selected program or register, or it displays a selected parameter.

4 Soft Knob

The Soft Knob is used together with the Display Window to edit the PCM 70's variable parameters.

5 Up and Down Keys

The Up and Down keys are used to select a row of programs, registers, or parameters.

6 0-9 Keys

The 0-9 keys are used to move from column to column within a row. Used in combination with the Up and Down keys, they allow you to move rapidly to any preset program, register, or parameter.

7 PGM Key

The PGM (Program) key toggles the PCM 70 in and out of the program mode. When the LED in the upper left-hand corner of the key is lit, the unit is in the program mode, and the Up, Down, and 0-9 keys may be used to select a preset program. The number and name of the selected program will appear in the display window. **Note:** The selected program isn't actually loaded until you press the Load key.

If the PGM key is pressed and held, the family of preset programs that the current program or register is derived from appears in the display window.

8 REG Key

The REG (Register) key toggles the PCM 70 in and out of the register mode. When the LED in the upper left-hand corner of the key is lit, the unit is in the register mode, and the Up, Down, and 0-9 keys may be used to select a register. The number and name of the selected register will appear in the display window. Note: A register isn't actually loaded until you press the Load key.

A register may be identical to a preset program, or it may contain a modified (edited) version of a program. If the REG key is pressed and held, the display window indicates the program or register number that was most recently loaded, and whether or not it is in an original or modified form.

9 LOAD Key

Press the LOAD key briefly to load a selected program or register into the PCM 70. When the LOAD key LED is lit (and the PCM 70 is in the parameter mode) its function varies, depending upon which parameter is active.

10 BYP Key

When the BYP (Bypass) key is pressed briefly, a small LED in the upper left-hand corner of the key lights, and all processing functions are bypassed, i.e., the main input is directly connected to both outputs. Press the BYP key again and the PCM 70 will return to normal operation. The bypass function may also be controlled with an optional remote footswitch.

11 Power Switch

The Power switch turns the PCM 70 on and off; the unit powers up in the same condition it was in when it was last turned off. The PCM 70 has a lithium backup battery which maintains the data memory even when power is off or disconnected.

2.1.1 Rear Panel Connections

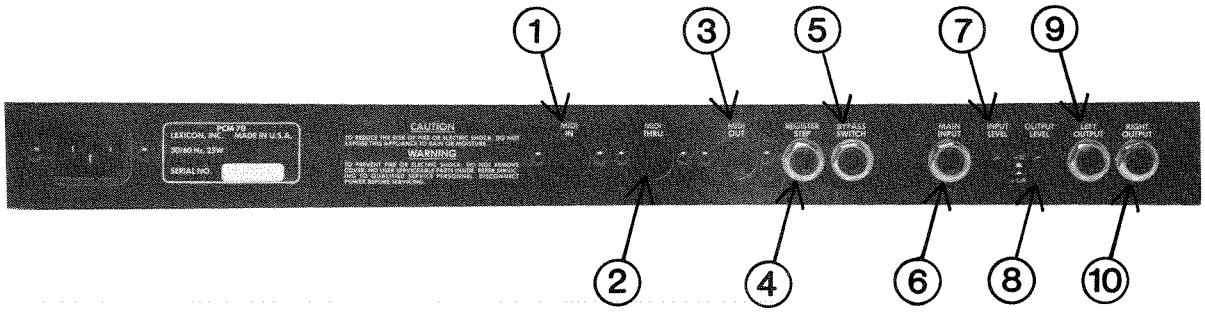

Figure 2.2. PCM 70 rear panel.

1 MIDI In

The MIDI In jack receives MIDI information from another MIDI-equipped device, such as a synthesizer or a sequence recorder.

2 MIDI Thru

The MIDI Thru jack retransmits MIDI information received at the MIDI In jack, without any change.

3 MIDI Out

The MIDI Out jack sends MIDI program change information from the PCM 70 to another MIDI-equipped device.

4 Register Step

This jack steps through the programs or registers in the current row. It accepts a 1/4-in. phone plug (tip/sleeve) wired to a momentary contact footswitch (we suggest Lexicon footswitch 750-02834 or A-FS-41).

5 Bypass

This jack allows remote control of the bypass function. It accepts a 1/4-in. tip/sleeve phone plug for connection to an optional locking footswitch (we recommend Lexicon footswitch A-FS-41.)

The PCM 70 can be placed in bypass mode from either the rear panel bypass switch jack or the front panel switch. The Bypass key indicator lights when the unit is in bypass mode. In the bypass mode, the signal continues to pass through some of the PCM 70's circuitry. The input signal is electronically routed to both left and right outputs, and the input level control remains effective.

6 Main Input

This jack is the audio input to the PCM 70. It accepts a 1/4-in. tip/ring/sleeve or tip/sleeve plug. Levels and impedance are determined by the Input Level pushbutton. In the +4 dB sensitivity mode the input matches balanced or unbalanced studio-level signals; in the -20 dB sensitivity mode the input matches unbalanced high impedance signals from instruments, microphones, and other low-level equipment.

7 Input Level

This pushbutton selects levels and impedance for the Main Input:

+4 dB: -8 to +18 dBV balanced or unbalanced, 40 kilohms parallel with 150 pF.

-20 dB: -23 to +3 dBV unbalanced, >500 kilohms parallel with 150 pF.

8 Output Level

This pushbutton selects levels for the Left and Right Outputs:

+4 dB: + 10 dBV maximum output into 600 ohms; +16 dBV maximum output into 10 kilohms or greater.

-20 dB: -8 dBV maximum output into 10 kilohms or greater.

9 Left and Right Outputs

The Left and Right audio output jacks accept 1/4" tip-ring-sleeve phone plugs. Output Level is determined by the program currently in use, and the Output Level pushbutton discussed above. Output impedance is 600 ohms, regardless of level setting.

When connecting the PCM 70 to a mono system, use either of the two output jacks. The left and right signals are summed internally when only one jack is used.

2.2 Specifications

The following specifications are subject to change without notice.

Frequency Response

Processed Signal:	20 Hz to 15 kHz, ±1 dB
Direct Signal:	20 Hz to 20 kHz, ±0.25 dB

Dynamic Range

Processed Signal:	80 dB, 20 Hz to 20 kHz noise bandwidth

Total Harmonic Distortion and Noise

Processed Signal:	<0.05% @ 1 kHz and full level
Direct Signal:	<0.025% @ 1 kHz @ 3V out

Audio Input

Levels	*+4 dB*;	-8 to +18 dBV balanced
	-20 dB;	-23 to +3 dBV unbalanced
Impedance	*+4 dB*;	40 kilohms, paralleled with 150 pF (balanced)
	-20 dB;	>500 kilohms, paralleled with 150 pF (unbalanced)
Connector		1/4" tip/ring/sleeve phone jack

Audio Outputs (Two)

Levels	*+4 dB*;	+10 dBV into 600 ohms +16 dBV into >10 kilohms
	-20 dB;	-8 dBV into >10 kilohms
Impedance	600 ohm unbalanced	
Connectors	1/4" tip/ring/sleeve phone jack	

Remote Bypass

1/4" tip/sleeve phone jack for latching footswitch (Lexicon A-FS-41)

Remote Register Select

1/4" tip/sleeve phone jack for momentary contact footswitch (Lexicon 750-02834)

Displays

FIP	16 digit, 14 segment alphanumeric fluorescent display
LEDs	5 segment headroom indicator with 24 dB range Bypass, Program, Register, and Load button indicators

Power

Nominal	100, 120, 220, 240 Vac (-10%, +5%) Switch-Selectable; 50-60 Hz, 25 W maximum

RFI Shielding

Meets FCC Class A computer equipment requirements

Protection

Mains fused; internal voltage and current limiting

Environment

Operating	0 to 35°C (32 to 95°F)
Storage	-30 to 75°C (-22 to 167°F)
Humidity	95% maximum without condensation

Dimensions

Standard 19" rack mount; 19"w x 1.75"h x 13.5"d (483 x 45 x 344 mm)

Weight

10.7 lb (4.9 kg)
Shipping weight 12.5 lb (5.7 kg)

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Performance Verification and Calibration Procedures

3.1 Periodic Maintenance

Under normal conditions a PCM 70 requires minimal maintenance. Use a soft lint-free cloth lightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit. Do not use alcohol-, benzene-, or acetone-based cleaners or strong commercial cleaners. Never use abrasive materials such as steel wool or metal polish. If the PCM 70 has been subjected to dusty environments, use a vacuum or *low-pressure* blower to clean dust out of its interior.

3.2 Performance Verification

This section will help you determine if a unit is operating correctly. Always complete the performance verification before proceeding to calibration procedures.

The following equipment is required:

1. Variac
2. Digital Multimeter (DMM)
3. Low distortion audio oscillator (with single ended 600 ohm output)
4. Dual trace 60 MHz oscilloscope (with 1X, 10X probes)
5. THD+N distortion analyzer/level meter (with switchable 30 kHz LP or audio bandpass input filtering)
6. Sweep frequency XY recorder (optional)
7. Lexicon Dual Footswitch (part #750-02433)
8. 1/4" shorting plug (short the Tip, Ring and Sleeve together)
9. 40 kilohm 1/4" Plug (tie 40 kilohms between Tip and Ring, short Ring and Sleeve)
10. 1/4" CMR cable (1 conductor shielded, one end Tip hot, gnd. Ring and Sleeve, other end Tip and Ring shorted to hot, Sleeve gnd.)
11. MIDI cable (2 conductor shielded w/5 pin DIN connectors--pin 2 gnd, pins 4 & 5 signal)
12. A high quality music source/playback system
13. Pulse generator or drum machine (optional)
14. A MIDI-equipped musical instrument (optional)

3.2.1 Initial Tests

1. Inspect the unit for obvious signs of physical damage. Verify that all pots, switches and keys operate smoothly.

2. Verify that the front panel hex screws and rear panel jacks are secure.

3. Connect a high quality music source and monitor system to the PCM 70. NOTE: A recording of a solo voice or instrument is a good signal source for evaluation of the effects programs in rows 0 and 1. A pulse generator or a drum box are good signal sources to evaluate the resonant chords programs in ROW 2 and the reverb programs in ROW 3, 4 and 5. For best results with the reverb programs, use a long pulse repetition rate with the pulse generator, or use a snare with a long repetition rate on the drum machine so that the entire reverb tail following the pulse or snare can be heard.

   A MIDI-equipped musical instrument is also useful for verifying the functionality of the Corresponding Register Table (PGM 7.1) and the MIDI patch parameters within each program.

4. Set up the proper signal levels through the machine.

5. Exercise the INPUT pot. No intermittents or scratchiness should be heard.

6. Run through all the programs and perform critical listening tests for excess or unusual noise or other audio irregularities. Enter the parameter mode within programs and vary some parameters to verify proper functionality. NOTE: Setting some parameters to the top end of their range (such as CHORUSING, FDBK and RSNC) can cause processor overload and resultant audio noise and feedback. Exercise restraint.

7. Verify that the PCM 70 can be powered up and down with the MIX parameter set to "100% WET" without beeps, honks or other evidence of processor problems.

3.2.2 Front Panel Diagnostics

Power up the PCM 70. "PCM 70 VERX.XX" should be displayed for approximately 2 seconds. If any of the key sequences described below are initiated within this two second window, the corresponding diagnostic routines will be entered. NOTE: The PCM 70 must be powered down to escape from some of these test modes.

1. **Key and Soft Knob Test** (Press "2" then press LOAD)

   When this test is entered, pressing any key will cause the FIP to display the legend of the key pressed, and a running total of the number of times all keys are pressed. Turning the Soft Knob will cause the direction of the turn and an increment number to be displayed. Verify that one "click" of the Soft Knob will cause only one display increment.

2. **Display Test** (Press "3" then press LOAD)

   When this test is entered, each segment and each digit of the display and the key LEDs should flash on and off until another key is pressed.

3. **Midi Wraparound Test**

   Connect a MIDI cable from MIDI OUT to MIDI IN on the back panel of the PCM 70. Press key "4" then press LOAD. The PCM 70 will send itself MIDI data and the display will indicate "OKAY", "NO DATA", or "BAD DATA".

3.2.3 Rear Panel Test

1. Connect a latching footswitch to the BYPASS jack on the rear panel of the PCM 70. "BYPASS ON" and "BYPASS OFF" should be alternately displayed and the BYP key LED should turn on and off when the footswitch is pressed.

2. Connect a momentary contact footswitch to the REGISTER STEP jack on the rear panel of the PCM 70. Press PGM. Verify that the PCM 70 steps through and loads programs when the footswitch is pressed. Press REG. The PCM 70 should step through and load registers when the footswitch is pressed, provided some registers have been stored by the user.

3.2.4 Memory Backup Test

All user registers and the parameters of the currently running program in the PCM 70 are stored in non-volatile RAM; in other words, this data will be preserved when the PCM 70 is powered down. The following procedure will verify that memory backup is occurring.

1. Power on the PCM 70.

2. Load a preset program.

3. Enter the parameter mode and alter a parameter from its preset default setting. Remember the altered setting.

4. Power down the PCM 70, wait a few moments, and turn on power.

5. Verify that the PCM 70 is running the same program it was running when powered down, and that the parameter you changed has maintained its altered setting.

3.2.5 Signal Test

Use an oscilloscope and THD+N distortion analyzer/level meter to monitor the signals described in this section. Bandwidth limit the input to the analyzer with either a 30 kHz LP or audio bandpass filter, unless otherwise directed. In working through the procedure, leave all controls in their last defined state.

1. Preset the PCM 70 as follows:

   a) Power on the unit. After two seconds an effects program will be automatically loaded.

   b) Either the PGM or REG key will be lit. Press the lit key and you will access the effects parameter matrix. Access parameter 0.0 (MIX) by pressing the "Up Arrow" or "Down Arrow" keys to reach matrix row 0, and pressing key "0" to move to column 0. Turn the Soft Knob until the display reads: "MIX 0 % WET".

   c) Press the 1 key to access Effects Level parameter. Turn the Soft Knob until the display reads "FX LEVEL +12 DB".

   d) Turn the INPUT LEVEL control fully ccw, and switch the rear panel INPUT/OUTPUT LEVEL pushbuttons to their 'in' (+4) position.

3.2.6 Headroom Display

2. Apply 0 dBV (1 Vrms) @ 1kHz to J3 (the MAIN INPUT jack). Turn the INPUT LEVEL control up to where the 0 dB HEADROOM LED just turns off.

3. Reduce the output level of the oscillator 20 dB. Verify that only the -24 dB HEADROOM LED is lit. Switch the rear panel INPUT LEVEL pushbutton to its "out" (-20) position. Verify that the HEADROOM LEDs up to -6dB are now lit.

4. Turn the PCM 70 INPUT LEVEL control fully cw. Decrease the oscillator's output level until the 0 dB HEADROOM LED just turns on. Verify that this occurs for an input level of -26 dBV $\pm$1dB.

5. Switch the rear panel INPUT LEVEL pushbutton back to its 'in' (+4) position. Increase the oscillator's output level to where the 0 dB HEADROOM LED just turns on. Verify that this occurs for an input level of -11 dBV $\pm$1 dB.

3.2.7 Main Input to Left and Right Output (Dry Signal Path)

6. Switch the rear panel INPUT LEVEL pushbutton to its 'out' (-20) position. Set MIX to "0% WET". With the front panel INPUT control full up (cw), apply a -28dBV signal to J3. Monitor the level at J1 and J3 with the distortion analyzer/level meter (with no output load). It should measure +3.3dBV ±1.5dB.

7. Add 40 kilohms in series with the input (tip of 1/4" plug) to simulate a high impedance source. There should be no appreciable drop in output level. Remove the series source resistance.

8. Measure THD+N @ 1 kHz and 10 kHz at J1 and J2. Adjust the output level of the oscillator to where the 0dB HEADROOM LED just turns on. Verify that distortion is <.025% @ 1kHz and <.05 @ 10 kHz.

9. Set a 0dB reference on the analyzer. Insert a 1/4" shorting plug into J3. Measure noise. Verify that it is <-65 dB. Remove the plug.

10. Switch the rear panel INPUT LEVEL pushbutton to its 'in' (+4) position. Input -12dBV @ 1 kHz with the INPUT control full up (cw). The signal level at J1 and J2 should measure +3.8dBV ±1.5 dB.

11. Add 40 kilohms in series with the input. Verify that this causes a 6 dB drop in output level from J1 at J2. Remove the series source resistance.

12. Measure THD+N @ 1 kHz and 10 kHz at J1 and J2. Adjust the output level of the oscillator to where the 0dB HEADROOM LED just turns on. Verify that distortion is <.025% @ 1kHz and <.05 @ 10 kHz.

13. Set 0dB reference on analyzer. Insert a 1/4" shorting plug into J3. Measure noise. Verify that it is <-80 dB. Remove the plug.

14. Measure the frequency response at J1 and J2 @ 20Hz, 200Hz, 2kHz and 20kHz. Verify a consistency of ±0.25dB. Switch out the 30 kHz LP of audio bandpass input filtering on the analyzer/level meter before taking any readings.

15. Input +16 dBV at 100Hz, 1kHz and 10kHz via the special CMR cable described on page 3-1. Verify that the level at J1 and J2 is < -14dBV for each frequency. Remove the CMR cable.

3.2.8 Main Input to Left and Right Out (Wet Signal Path)

16. Set parameter 0.0 (MIX) to "100% WET" and parameter 0.1 ("FX LEVEL") to "+12 DB". Apply a -12dBV signal @ 1kHz to J3. The signal level at J1 and J2 should measure +14dBV ±1.5dB with no output load. Switch the analyzer's 30 kHz LP or audio bandpass filtering back in.

17. Adjust the oscillator's output level so that the 0dB HEADROOM LED just turns on. Measure the WET THD+N performance of the PCM 70 @ 1kHz and 3kHz through J1 and J2. Verify that the distortion figure for both signal paths and both frequencies is <.025%.

18. Measure the WET THD+N performance of the PCM 70 @ 5kHz, 10kHz and 12kHz through J1 and J2. The distortion figure at these frequencies for both signal paths should be <.05%.

19. Measure the WET THD+N performance of the PCM 70 @14kHz through J1 and J2. Verify that the distortion figure for both signal paths is <.1%.

20. Reduce the output level of the oscillator 20 dB @ 1kHz. Only the -24dB HEADROOM LED should be on. Measure the WET THD+N performance of the PCM 70 through J1 and J2. Verify that the distortion figure for both signal paths is <.15%.

21. Increase the oscillator level to where the 0dB HEADROOM LED just goes on. Monitor the signal level at J1 or J2 and set the 0dB reference level on the analyzer/level meter. Insert a 1/4" shorting plug into J3 and measure the wet noise performance through J1 and J2. Verify that the noise figure for both signal paths is <-80dB. Remove the plug.

22. Apply -12dBV @ 1kHz to J3. Measure the frequency response of the wet signal paths through J1 and J2. Verify a level consistency of ±1.0dB over a bandwidth of 20 Hz to 15kHz. Switch out the 30kHz LP or audio bandpass input filtering on the distortion analyzer/level meter before taking any readings.

3.3 Calibration Procedures

3.3.1 Power Supplies and Clocks

1. Remove the top and bottom covers of the unit and make the following checks:

   a) Verify the presence of a protective cover under the power supply.

   b) Verify that the voltage option switch (SW 3) is set to the proper line voltage.

   c) Verify that the power supply jumper (located below the voltage option switch) is installed as specified in Table 3.1.

Ac Line Voltage	Jumper Position
100V	E24 - E23
120V	E24 - E22
220V	E24 - E23
240V	E24 - E22

Table 3.1. Jumper positions for different ac line voltages.

   d. Verify the the value of fuse (F1) is correct as specified in Table 3.2.

100/120V	220/240V
1/4A	1/8A
3AG	3AG
SLO-BLO	SLO-BLO

Table 3.2. F1 fuse selection for different ac line voltages.

   e. Verify that all socketed ICs are fully and correctly seated.

   f. Verify that jumper tab W8 is across pins 1 and 2 (RUN-position) of the post block.

2. Connect the PCM 70 to an ammeter-equipped variac or an isolation transformer.

3. Turn on the PCM 70 and slowly bring up the variac to the required line voltage while observing the ammeter. Current should peak at approximately 0.28 A and settle to approximately 0.2 A for a 100/120V unit, and peak at 0.13 A and settle to approximately 0.1 A for a 220/240V unit. If the unit draws excessive current, turn it off and check the power supply rails for shorts.

4. Probe TP24, pins 5 and 6 with a DMM. Trim the +5V digital power supply to 5.08 Vdc by adjusting trimpot R131. If the supply cannot be trimmed to this value, faulty components may be the cause.

5. Attach the common (ground) probe from a DMM to a PCM 70 ground and measure the power supplies. Refer to Table 3.3. All power supplies should be providing the correct voltage; if they are not, faulty components or low line voltage may be the cause.

Supply (Vdc)	Limits (Vdc)	Location on Motherboard Rail	Ground
+15V	+14.25V to +15.75V	TP24, p2	TP24, p1
-15V	-14.25V to -15.75V	TP24, p3	TP24, p1
HV	+30 to +37V	U52, p10	U52, p9
+5V, ANA	+4.5V to +5.5V	CR9, cathode	CR9, anode
+5V, DIG	5.08V	TP24,p5	TP24, p6
VfilA, VfilB	7-9Vac p-p w/+6Vdc bias	TP23, p1, p3	TP23, p2

Table 3.3. Power supply limits and test locations.

6. Using a dual trace oscilloscope with either 1X or 10X probes, verify that regulation performance of the supply rails meets the specification listed in Table 3.4. Conduct this test at the nominal ac line voltage of the unit. Be sure to ac couple each of the oscilloscope's vertical input channels and select the ac line as the trigger source.

Supply (Vdc)	Input Ripple/ Probe Location	Output Noise/ Probe Location	Ground Ref. Location
+5V	<1.6Vp-p/U99,p14	<10mV/TP24,p5	TP24,p6
+15V	<1.6Vp-p/U72,p1	<10mV/TP24,p2	TP24,p1
-15V	<1.6Vp-p/U92,p2	<10mV/TP24,p3	TP24,p1

Table 3.4. Power supply input ripple and output noise limits.

7. Alternately set the variac to both extremes of the ac line operating range given in Table 3.5. With a DMM, verify that all regulated voltages remain within their tolerance range, as specified in Table 3.3.

Nominal Vac	Operating Vac
100	90 - 105
120	108 - 126
220	198 - 231
240	216 - 252

Table 3.5. Nominal and operating line voltages.

8. Reset the Variac to nominal line voltage.

9. Slowly turn down the Variac. The PCM 70 should mute the audio and display "POWER LOW" as line voltages reaches 20% below nominal.

   Note: Rev 2 and later boards are equipped with a trimpot (R160) for setting the threshold for POWER LOW. Set R160 for POWER LOW indication at 20% below line voltage.

10. Return the variac to nominal line voltage. The PCM 70 should display "POWER OKAY" and return to the currently running program.

11. Vary the +5V DIG supply between +4.75 - +5.25V by turning trimpot R131. The unit should not reset and should operate normally under both of these conditions. Retrim R131 to 5.08Vdc.

12. Check all clocks for good logic levels, symmetrical square waves and proper periods as specified in Table 3.6.

Clock	Period	Probe Location	Ground Ref. Location
MC	77 ns	U36, TP21, p2	TP21, p1
ZCLK	308 ns	U68, p9	TP21, p1
MIDICLK	2 us	U60, p11	TP21, p1
SAMP	29.5 us	TP25, p1	TP25, p2

Table 3.6. Clock periods.

3.3.2 Output VCA Calibration

Note: For Rev 2 and later boards *only*, trim R158 for +3 mV at U17, pin 7, with no input before continuing.

The PCM 70's output levels are processor controlled via 2 DACs and 3 VCAs. This procedure will calibrate the VCAs for minimum distortion.

1. Power the PCM 70 off and on. While "PCM 70 VER 1.XX" is displayed, press Button "1" ("GENERIC PROGRAM" displayed), then press LOAD. Next press Button "7" to access the Diagnostic Programs. Dial in "DIAGNOSTIC 0" with the Soft Knob, then press LOAD. Access parameter 0.1 and with the Soft Knob set "FX LEVEL" to "+12 DB". Access parameter 0.0. With the Soft Knob set MIX to "0% WET".

2. With the input signal remaining the same as in step 5), connect a distortion analyzer/level meter to J2 (the LEFT OUTPUT jack) and monitor THD+N. Adjust trimpot R86 for minimum distortion.

3. Set MIX to "100% WET". Adjust trimpot R36 for minimum distortion.

4. Connect the distortion analyzer to J1 (the RIGHT OUTPUT jack). Adjust trimpot R10 for minimum distortion.

5. Attach top and bottom covers.

4

Circuit Description

This section is a guide to the organization and function of the various circuit blocks within the PCM 70. It is provided as an aid to qualified service personnel and is not intended to be a primer in analog and digital circuit theory.

Note: The PCM 70 circuit board layout is divided into sections to aid in the location of circuit subgroups:

- I/O - Mix
- Power Supply
- Headroom
- Converter
- Master Processor
- Slave Processor
- High Speed Processor
- Writable Control Store
- MIDI Interface

4.1 Analog Circuitry

4.1.1 Audio Input Stage

Signals enter the PCM 70 through the Main Input (J3) in a balanced mode with the rear panel Input Level switch (SW2) in the +4 position, and in a single ended mode with the switch in the -20 position. The input stage (U19) provides 0 dB gain in +4 mode and 16 dB gain in -20 mode. Its output is fed to the Input Level control (R71) on the front panel and from there to U17 for 15.5 dB of gain. The output of this stage is fed to a 15.25 kHz hybrid low-pass anti-alias filter (LPF3). This filter has a 6 dB loss in its passband. Further gain of 17.5 dB is provided by the other half of U17 to bring the signal up to a maximum level of 7 V RMS (20 V peak-to-peak), which is full scale for the A/D converter. This is the input to the sample-hold circuit, described in the A/D converter section.

4.1.2 Headroom Monitoring

The signal input to the sample-hold circuit is also scaled down to a maximum of 5 V peak to peak by a resistive divider, and full-wave rectified by U6. Q2 and C42 provide a peak hold function with a discharge rate controlled by R22. This peak hold

voltage is then quantized in 6 dB steps from 0dB of headroom (maximum converter level) to 24 dB below maximum level by a comparator/driver IC (U7), which drives the five front panel LEDs. The reference voltage for the internal comparators and LED drive current are set by R67 and R68. An additional signal, OVLD, from the ARU (U25) is Ored (via CR19) with the rectifier output to provide an indication of digital processor overload. When this signal goes high, the peak-hold voltage is raised to a level which will cause the 0 dB headroom LED to be lit.

The peak-hold voltage is also routed to an 8-bit monolithic A/D converter (U23) which interfaces to the master processor. Half-scale conversion level is set by a combination of internal and external (R98 and R99) resistors such that the maximum output code is produced at approximately 0 dB of headroom. This A/D Converter is a successive approximation converter with a microprocessor-compatible interface. Conversion speed is controlled by a clock input (SAB2). As configured, one conversion takes about 130 us, providing the CPU with the capability of level-dependent parameter variation. See the master processor section for the method of initiating and reading a conversion.

4.1.3 Analog to Digital Conversion

The sample-hold circuit is comprised of op amp U11, gain-setting resistors R55 and R56, "hold" capacitor C36, JFET transistor Q4, and Schottky diodes CR12 and CR13. The signal SAMP (see Basic sample cycle timing diagram, Figure 4.3) is level shifted by C55, R81, R82, and R83 to swing between 0 and -5 V, and is used to drive the gate of Q4. The frequency of the sampling signal is 33.85 kHz. When high, Q4 conducts and the circuit looks like a simple unity gain inverting op amp stage with a polypropylene capacitor in its feedback loop. This capacitor will charge up to the input signal level within several time constants.

This is the sampling mode of the circuit, wherein it will acquire the present level of the input voltage. During the middle 50% of the 29.5 us sampling cycle, SAMP goes low, and Q4 will be cut off, appearing as an open switch.

This puts the circuit in the hold mode, where the charge on C36 will maintain the op amp's output voltage at a constant level (that level which it has just acquired) during A/D conversion. During the hold mode, CR12 prevents negative-going input signals from causing Q4 to conduct (due to the input voltage dropping below the gate voltage) by clamping the input at -0.3 V. CR13 reduces feedthrough of positive-going signals. When switched to the hold mode, OUT (which is derived from SAMP) also goes low, allowing the output of U11 to be routed to the input of the 16-bit DAC (U15) through analog switch U10. This feedback resistor input converts the sampled voltage to a current and is summed with the current generated by the DAC itself. This current is fed to comparator U16, whose output (DATA) goes to the Converter Management Unit (U20).

The CMU's major function is to perform a 16-bit successive approximation conversion. It also contains registers to store the A/D conversion result and the digital output word for the D/A portion of the cycle. A/D conversion is controlled by ST/ and CCLK (see Basic sample cycle timing diagram, Figure 4.3). There are 17 CCLK

rising edges; the first, occurring while ST/ is low, is used to reset the successive approximation register to all bits high except the MSB (DAC 15), which is low, corresponding to a zero (no current) output of the DAC. Refer to Table 4.1 for an explanation of the complementary offset binary coding used by the DAC.

The DAB bus is in complementary two's complement form, which is accomplished by internally inverting the MSB (DAB 15) going out of and into the CMU. This coding is shown in Table 4.1.

	MSB |	LSB |	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000	000	+Full Scale	-1 LSB
Mid Scale	0111	111	Zero	-Full Scale
All bits OFF	1111	111	-Full Scale	Zero
	1000	000	-1 LSB	+Full Scale

Table 4.1. Complementary offset binary coding.

As can be seen above, the A/D conversion process attempts to cancel the current summed in from the sampled signal input. The comparator (U16) determines for each successive bit whether the summed current is under or over the "null" point. A perfect 16-bit conversion would result in Iout (= Iin + Idac) being within 1/2 LSB (±15nA) of 0. The Schottky diodes (CR10 and CR11) provide a low clamp voltage (0.3 V) with fast recovery to aid the DAC and comparator in settling rapidly. Successive rising edges of CCLK latch the resulting comparator data into the register and set the next bit low, until 16 iterations have been completed. The final clock edge strobes the full 16-bit word to the input register, where, on the first program step of the next cycle, it is enabled onto the DAB bus by signal IN.

During the A/D conversion process, op amp U5 is disconnected from the DAC by OUT/ going high, and its output clamped to its input through analog switch IC U10 by OUT going low.

4.1.4 Digital to Analog Conversion

At the completion of A/D conversion, SAMP, OUT, and OUT/ change state, which causes the following; the input of op amp U5 is connected to the DAC's current output, the output of this op amp is connected to the feedback resistor input of the DAC, the output of U11 is disconnected from the DAC, and the sample-hold circuit returns to the sampling mode. MUTE inhibits the signals OUT and OUT/ from switching to this D/A conversion state, and is generated by the master processor whenever a program is changed, in order to prevent glitches at the output. In the D/A conversion mode, op amp U5 is thereby configured as a current-to-voltage converter. While the sample-hold is acquiring the next sample, the DAC performs two output conversions, one for each output channel, each occupying slightly more than 7 us. The first (left) output cycle begins immediately, the digital word having been latched into the CMU by the first OCLKD pulse, occurring at the middle of the program cycle. The DAC and current-to-voltage converter are allowed to settle for a

little less than 3 us, and, for the next 4 us, the deglitcher circuit (U4 and U9) acquires the output sample.

The deglitcher circuit is an exponentiate and hold stage whose purpose is to remove errors due to DAC transition glitches and current-to-voltage amplifier slewing, which would manifest themselves as distortion and aliasing. The deglitchers have a gain of -11.5 dB. DMOS switch U4 adds very little switching energy to the signal due to its low parasitic capacitance. SDEG1 going high enables the circuit to acquire the output sample. When this signal goes low, the circuit is put in the hold mode, and SDEG1/ will go high, causing the audio signal at the input to the switch to be shunted to ground. This prevents the next (right channel) output sample from feeding through, which would result in crosstalk and distortion problems.

After the left output has been deglitched, the signal OCLKD pulses again, latching the right channel digital word into the CMU on the last (127th) program step. Another 3 us is allowed for settling during the beginning of the next program cycle and this output sample is deglitched by the other halves of U4 and U9 with the signals SDEG2 and SDEG2/, in the same manner as the left channel circuit. Once this is completed, the sample-hold circuit has acquired the next input sample, and another A/D conversion begins.

Since it can be difficult to trace a signal on the digital audio bus (DAB), a test mode is provided in the CMU. By moving jumper W8 to self-test mode (STS), the CMU internally routes the just-converted digital word to the output latch where it is directly applied to the next D/A cycle (both left and right). In this way, the conversion process can be tested independently from the memory or processor cycle.

4.1.5 Output Filtering

The deglitchers are followed by two-pole inverting low-pass filters (U8) with moderate Q's (a slightly peaked response) whose function is to smooth the sample-to-sample discontinuity and provide correction for the slight high frequency rolloff caused by the sample reconstruction. These are called aperture correction circuits, and have a gain of 0 dB (unity). The signals are then passed to 9-pole hybrid low-pass filters (LPF1 and LPF2) identical to the input filter, to remove sampling clock and image residues. These filters have a 6 dB loss in the passband. The filtered outputs are routed to the mix circuit.

4.1.6 Output Mix

The digitally-controlled mix circuit consists of two basic blocks. The first, which interfaces to the master processor, is a dual 8-bit current-output DAC (U22). One output controls the unprocessed, or "dry" signal level, while the other output controls the processed, or "wet" signal level. The second block is the Voltage Controlled Amplifiers (VCAs), which perform the actual gain control on the wet and dry audio signals.

When the unit is in the mix control mode, turning the Soft Knob causes two 8-bit words per mix setting to be sequentially loaded into the dual DAC from the master processor. These 8-bit words, or mix coefficients, are derived from the characteristic equation of standard mix circuits:

$$(Av1)^2 + (Av2)^2 = k$$

where k is a constant, Av1 is the dry signal voltage gain, and Av2 is the wet signal voltage gain.

At a mix setting of 50, both mix coefficients are identical, resulting in an equal mix of wet and dry signal. At a setting of 0, the dry coefficient is at a maximum and the wet at a minimum; the 100 setting produces the opposite coefficients. See Figure 4.1.

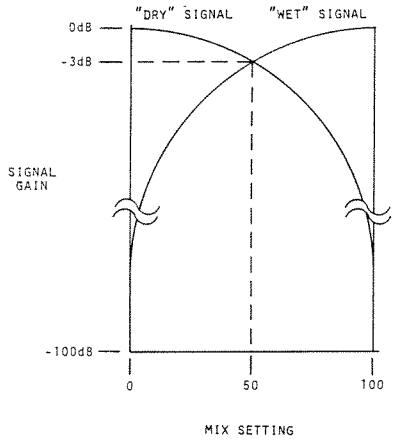

Figure 4.1. Wet and dry mix coefficients.

Both coefficients are internally latched by the dual DAC, and a current is produced at both outputs which is proportional to their respective coefficients. These currents are converted to voltages ranging from 0 to -5 V by op amp U24. The op amp outputs are then divided down to limit the range to between 0 and -600 mV by R91 and R92 (dry), and R93 and R94 (wet), and then low pass filtered. These signals are the wet and dry control voltages fed to the VCAs.

Returning to the audio signal path, the output of the input level buffer (U17) is also fed to a voltage divider (R95 and R96) and on to the input of the dry VCA (U14), the output of which goes directly to the inverting input of op amp U19.

The VCA can be looked at as a voltage controlled resistor; when the control voltage is at 0, the VCA behaves as a "0 ohm" resistor and the gain of the circuit is determined by the op amp's feedback resistor (R105) and the input resistor (R90), in this case unity gain. As the control voltage becomes negative, the "resistance" of the VCA increases, thereby reducing the gain of the circuit. The VCA's gain constant is 1 dB of attenuation for each 6 mV drop in control voltage. The left and right processed audio from the output low-pass filters (LPF1 and LPF2) are fed through series resis-

tors (R14 and R44) and into their VCAs (U2 and U13 respectively) which are both controlled by the wet control voltage. The outputs of these VCAs feed the inverting inputs of U1 and U12 respectively, just as in the previously described dry circuit. Note however, that in this case the gain controlled dry mix signal is summed into both of these op amps, through R34 and R77. The resulting output is then the sum (or mix) of the unprocessed audio with the left (or right) processed audio signal. The maximum gain of this circuit to either input is 3.5 dB. Output level control is performed by the master processor simultaneously modifying both gain coefficients.

Each 1 LSB increment of the coefficients will result in an attenuation of about 0.4 dB. Trimpots R10, R36, and R86 provide symmetry adjustment for each of the three VCAs, allowing distortion to be minimized.

4.1.7 Audio Output Stage

The mix circuit is followed by the other halves of U12 and U1 for the left and right channels, respectively, which serve as the output buffers. These have a gain of about 15.5 dB.

The output levels can be switched together to provide high level or 24 dB attenuated lower level signals by means of the rear panel output level switch (SW1). Output impedance is maintained at approximately 600 ohms for either position. A further feature of the output stage is a ground referenced output to minimize common mode noise. This functions whenever tip-ring-sleeve phone plugs are used on the left (J2) or right (J1) outputs. Tip-ring plugs will simply disable this feature.

If only one output is plugged in, both left and right outputs are summed together by way of the tip switch of each output jack connecting to the tip of the other jack. The tip switch of the jacks is closed when there is no plug inserted, thereby completing the connection.

Provision has been made for muting both outputs during power-up, power-down, power failure, and brownout conditions. A signal, PFAIL/, generated by a comparator in the digital section, drives the base of Q5. If any of the above conditions occurs, PFAIL/ will go low, turning on Q5, which will rapidly discharge C18. This raises the gate voltage of n-channel JFETs Q1 and Q3, causing them to conduct. The JFETs are connected between each output and ground and have very low on resistance (< 10 ohms), enabling them to effectively mute the outputs before any undesirable transients can be emitted as the power rails collapse. During power-up, the outputs will remain muted until C18 (charging through R3) reaches a voltage negative enough to turn off the JFETs. This time constant has been designed to allow the unit to "set-up" before it will pass audio.

4.1.8 Power Supply

The analog + and - 15 V power supplies use fixed linear regulators, (U72 and U92 respectively) from a bridge-rectified (CR42) center-tapped secondary of the power transformer, T1. One additional analog supply is a zener regulated (CR9) + 5 V for the 16 bit DAC (U15), analog switch IC U10, and the mix circuit DAC (U22).

The digital + 5 V power supply uses a switching regulator (U99) from a + 18 V secondary, rectified by bridge CR52. The switching regulator is synchronized by signal SAB5 to operate at twice the audio sampling frequency (67.7 kHz) in order to minimize noise caused by interference frequencies.

Inductor L1 and capacitor C143 serve to low-pass filter the pulse-width modulated output of the switching regulator, resulting in a dc output voltage with minimal ripple. A high-current Schottky switching diode (CR47) on the output of the regulator prevents any appreciable negative voltage swing.

Refer to the power supply schematic and switching supply simplified block diagram in Chapter 7 for the following explanation. The error amp amplifies the difference between Vsense (set by trimpot R131, which is used to adjust this supply voltage to the proper value), and an internal reference voltage, and then outputs this voltage to a comparator. The comparator compares this error signal to a sawtooth waveform of the clock signal, created by a ramp generator. At any time the error signal is greater than the ramp voltage, the comparator output will be high. Conversely, if the error signal is below the ramp voltage at any particular point in time, the comparator output will be low. Refer to the waveform chart (Figure 4.2). If Vsense is below Vref (indicating the 5 V supply is slightly low due to increased loading), the error signal will become more positive, so the ramp voltage will be lower than the error signal for a longer period of time, meaning that the comparator output will remain high for a greater percentage of the clock (SAB5) period.

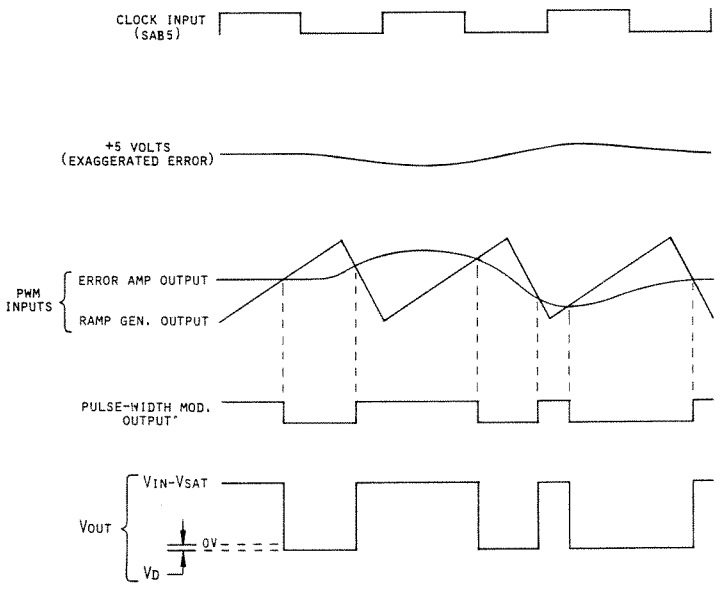

Figure 4.2. Waveform chart.

This pulse-width modulated signal drives the base of a 2A Darlington switching transistor, which will then remain "on" for a longer period of time, dumping more current into inductor L1, and increasing the charge on C143, thereby raising the 5 V supply back up to the proper level. Thus, a feedback loop is created which maintains the supply voltage at a constant level, even under changing load conditions.

Should there be a catastrophic failure of this circuit, or a short from a higher potential supply to the +5 V supply occurs, overvoltage protection is provided by a crowbar SCR (Q10) triggered by zener diode CR39, which will shunt the rail to ground, protecting the digital circuitry.

The fluorescent indicator panel (FIP) requires two separate supplies; a high voltage (+ 35 Vdc) for the grid (digits) and anodes (segments), and a 5.5 V RMS ac supply for the filament. The + 35 V supply is generated by a voltage doubler circuit comprised of CR48, CR49, C147, and C149 off of the digital supply's secondary winding. This voltage is delivered to the display driver ICs (U28, U40, U41, and U52). FIP scanning is described in Section 4.3.1.

The filament voltage is generated by its own center-tapped secondary winding of the transformer. The center tap is biased up to + 6.2 V by zener diode CR56, so that when a digit or segment is turned off (display driver output at ground), there is no "ghosting".

The unregulated +18 V used for the +5 V digital supply is also used to supply U103, a quad comparator in the digital section. One section of U103 compares the unregulated + 18 V (divided down to a nominal 5.75 V) to the + 5 V digital supply. When the unit is turned off, or if a power failure/brownout should occur, this voltage will drop below the 5 V threshold, and the comparator's output will go low. It should be noted that because of the switching regulator's feedback loop, regulation of the 5 V supply will be maintained down to an input voltage (the unregulated +18 V) of approximately 10 V, well past the point where this comparator will fire. R147 provides hysteresis to prevent multiple toggling if the input voltage hovers around the trigger point. The PFAIL/ signal will mute the audio outputs (as described in the Audio Output Stage section) and provide a non-maskable interrupt to the master CPU, which will immediately stop processing and prepare for power-down (see Section 4.3.1, which describes the master processor).

All supplies contain extensive RFI protection (C144, 148, 150, 155, 156, 154, 160, and L2) and surge protection (VR1, VR2) to protect from line transients.

4.2 Timing Diagrams

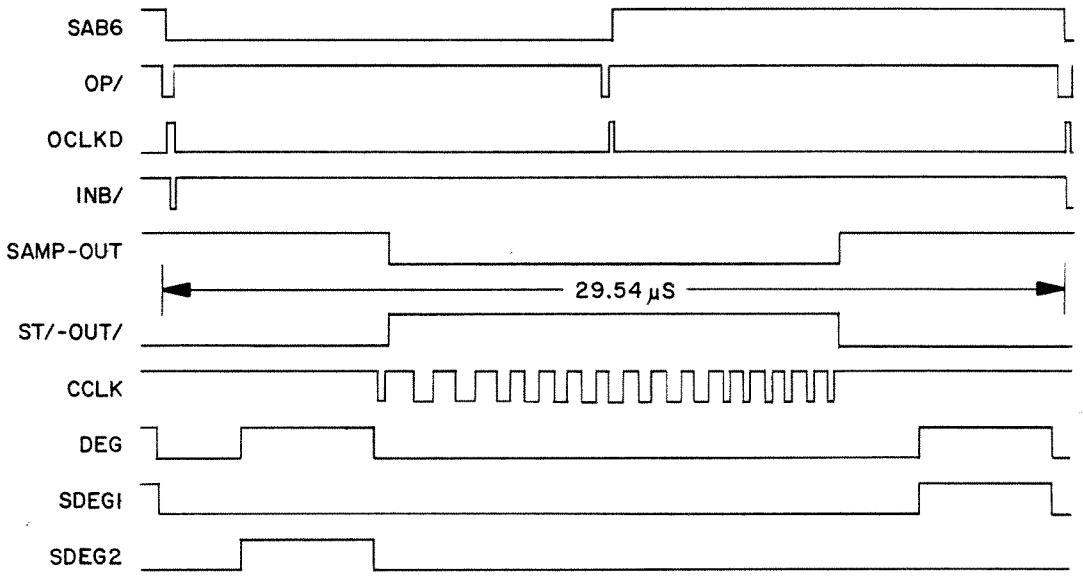

Figure 4.3. Basic sample cycle timing.

Figure 4.3 shows the basic sample cycle timing. During this cycle, input audio is sampled for conversion and processed data is converted for audio output. Signal SAB6 is the MSB of the 7-bit sample cycle counter in the MMU (U54), buffered and synchronized by latch U76 at the beginning of the AS1 period.

OP/ is generated by the HSP microcode as MIB29 and synchronized at AS0/ in U57. It creates OCLK and IN/ timing windows to initiate I/O samples. OCLK becomes OCLKD and is used to clock data from the DAB (Memory Data Bus) to the DAC holding register in the CMU (U20). INB/ enables the previous cycle's input SAR conversion to be gated onto the DAB for placement in the data memory.

To provide input conversion settling time, SA6 is phase shifted by U64, generating SAMP which in turn creates output sample timing of left and right conversion for the DAC (U15). The input sample is converted with the SAR clock (CCLK) coming from the WCS ROM (U67). Deglitch samples are taken when DEG timing is gated (U26) with SAB6 to provide left and right sample/hold output periods SDEG1 and SDEG2.

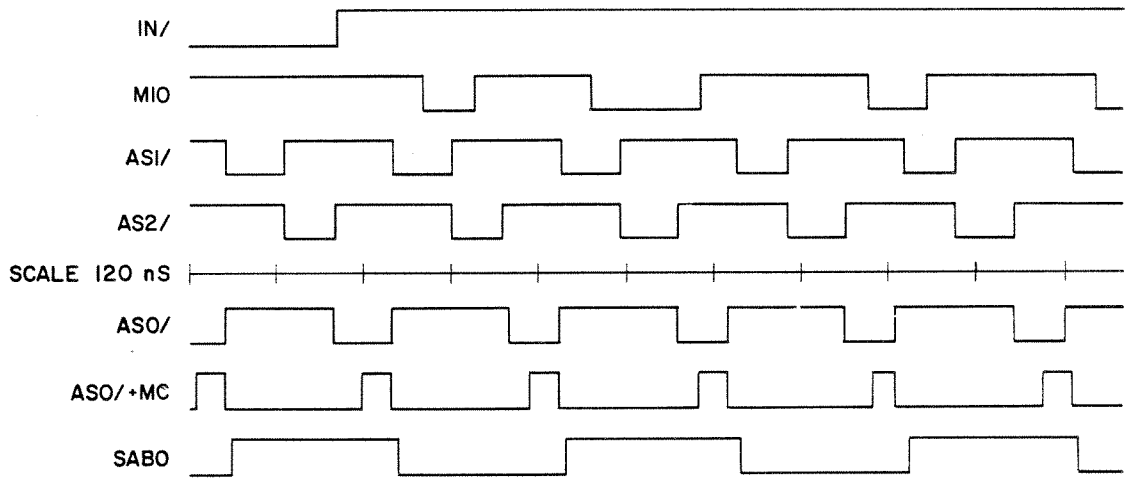

Figure 4.4. Basic WCS logic timing.

The basic timing for the WCS logic is shown in Figure 4.4. There are three sequential periods provided by the HSP control ROM (U49), which represent the finite 3-phase timing of the data processing cycle. The three periods are AS1, AS2, and AS0.

IN/ is shown as a reference only to the beginning of any sample cycle with MI0 indicating when the LSB of program control memory data will occur. SAB0 is the LSB of the memory address counter, which encompasses the three phases as major memory pages. AS1 saves the first byte in the U66 latch. AS2 clocks the second byte plus the latched byte into the MMU 16 bit offset register. The third memory byte is latched at the end of the AS0 period, as are the ROM bytes (U67) using AS0 and MC. The WCS therefore has a 32 bit output within the three phase cycles.

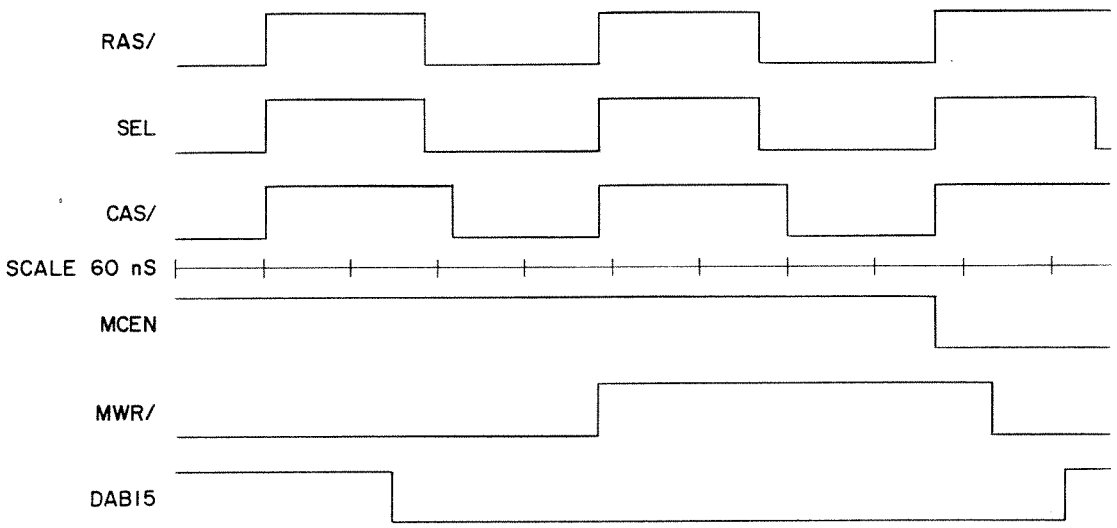

Figure 4.5. Data memory timing.

Figure 4.5 shows the relationship between RAS, SELECT, and CAS--generated when AS0/ is high. The delay line (U53) has 30 ns taps which enables RAS to occur 30 ns after AS0/, and CAS to occur 60 ns after AS0/.

SEL is delayed by U65 to enable setup time for RAS before the YA0-7 address lines change for CAS. In the MMU, RAS, SEL, and CAS are gated with AS0/ in U42 to terminate their periods simultaneously at the beginning of the AS0 cycle. Memory cycles are controlled by MI30 out of the WCS (after synchronization by U57) and delayed by U37 to produce MCEN/. Memory write cycles are created by MI31 out of the WCS after being synchronized and delayed in the same manner. DAB15 is shown to indicate when memory data changes for a write cycle.

4.3 Digital Circuitry

As shown in the block diagram, the PCM 70 digital section is divided into 9 major functional modules:

- Master Processor
- Slave Processor
- Writable Control Store (WCS)
- Timing and Control (T&C)
- Converter Management Unit (CMU)
- Arithmetic Unit (ARU)
- Memory Management Unit (MMU)
- Digitized Audio Memory (DAM)
- Digitally Controlled Mix

The master processor (a Z80 microprocessor) provides interface to all external stimulus to the PCM 70. It scans the switch matrix for switch closure, drives the fluorescent indicator panel (FIP), and monitors the Soft Knob, headroom indicators, and activity on the MIDI interface. The master processor initiates all effects program changes by directing the slave processor as to the change to be made. Battery backed up memory resides within the master's memory address space. Both the master processor and the slave processor run in the maskable interrupt mode 1. The interrupt occurs on carry-out from counter U64. The interrupts occur every 240 us (8 x SA6) providing synchronization for the entire system.

The slave processor (also a Z80 microprocessor) is used exclusively for updating the Digital Signal Processor's micro control store. All activities of the slave processor are initiated by the master processor through the bidirectional communications port.

The WCS, CMU, ARU, MMU, T&C,and DAM modules comprise a dedicated 230 ns-cycle microprogrammed digital signal processor (DSP). For the purpose of this discussion all modules except the WCS module are called the HSP. It is referred to as the high speed processor (HSP) in this document. During normal operation signal flow begins with the single input channel. The AIS module filters, tracks, holds and digitizes audio signals into 16-bit fixed point two's complement numbers. The DSP processes this information and generates two channels of output data. This processed data is passed through the output DAC where it is reconstructed into two analog signals. The analog signals are then filtered and passed on to the AOS.

4.3.1 Master Processor

The master processor is responsible for initiating all activity in the PCM 70. The following devices are monitored by the master processor, and provide a window to the control of the master processor by the user.

Fluorescent Display (FIP)

The fluorescent indicator panel (FIP) is a sixteen segment, sixteen character display. The FIP is based on the scanned display concept in which all digits share a common segment drive. Segment information is supplied to latches U27 and U39. Digit (grid) information is supplied to latches U38 and U51. The output of these devices is fed to high voltage drivers U28, U41, U40, and U51. Each digit must be refreshed at a minimum rate of 200 HZ, the rate at which no flickering will occur. I/O mapping of the FIP can be found in Section 4.4.1. At powerup all devices are cleared to prevent damage to the display.

Soft Knob and Direction Detect

The Soft Knob is a panel mounted rotary incremental encoder. The output of the encoder is shown in Figure 4.6.

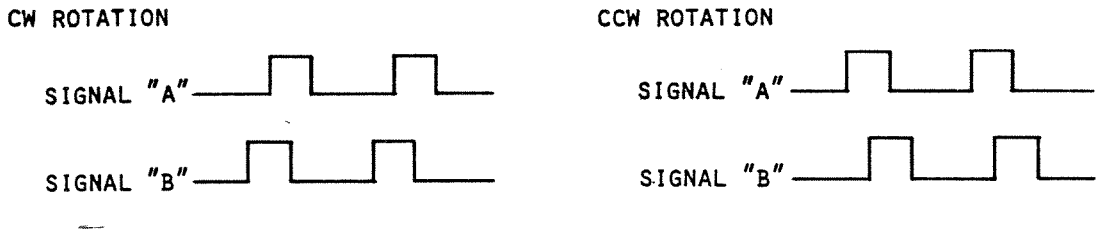

Figure 4.6. Soft Knob Encoder Output.

The encoder has two phases--A and B. These square waves are used to determine both motion and direction by the processor. There are fifty pulses per revolution. U101A is used to automatically determine direction. Both phases of the encoder and the direction bit are monitored through the STATIN port. Signal names are SKNA, SKNB, and SKNDIR. Bit assignments can be found in the Master I/O map, Table 4.6.

Switch Matrix and LEDs

The switch matrix is composed of sixteen momentary contact switches organized into eight columns and two rows. Column selection during scanning is multiplexed with the low eight digit select lines of the FIP. Rows are normally pulled down by resistors R140 and R141. When switch closure occurs and the appropriate column is activated a high level signal appears at the STATIN port for the row activated (see the Master I/O map, Table 4.6.

MIDI Communications Port

The MIDI communications port is provided with standard MIDI hardware interface, composed of three five-pin DIN connectors, MIDI In, MIDI Out and MIDI Thru, 5 mA current loop hardware and a high-speed opto-isolator. The transceiver rate is the standard MIDI 31.25 kB. The serialization and reconstruction of the transmitted and received data is performed by the UART (U97). I/O mapping is provided in Table 4.6.

Register Step and Bypass

Two external control jacks (J5 and J6) are provided on the rear panel of the PCM 70. The Register Step jack (J5) allows the user to connect a footpedal to step through registers. The Bypass jack (J6) allows the user to bypass the digital section of the PCM 70. Register Step and Bypass are two bits in the STATIN port, as described in Section 4.4.1.

Digitally Controlled Mix

The degree to which the unprocessed audio is mixed with processed audio is controlled by a two channel DAC (U22). This mix circuit is described in Section 4.1.6. For I/O mapping see Table 4.6.

Headroom Monitor

The amplitude of the incoming audio signal can be monitored by the master through U23. The procedure for reading this ADC is to first write to the port thus initiating a conversion the reading from the port to obtain the 8-bit digital word. The conversion process is more fully described in the analog section of this document. Refer to Table 4.6 for master processor I/O mapping.

Auto Reset

The PCM 70 is provided with an automatic reset circuit. On power up signal Zrst/ is low until RC network RP3 and C159 charges up to the threshold of U102C and the 5 V rails stabilize thus setting PLOW low to U102B. Once these conditions are met the reset is removed from the master processor and the initialization routine begins. This condition also allows RC combination R136 and C152 to charge, removing the clear signal on U101B. During normal processing, digits are strobed out to the display registers U38 and U51. After initialization is complete the first digits are strobed. Signal SEGSEL0 is strobed low discharging RC combination R137 and C157. On the rising edge of SEGSEL0 a 1 is clocked out to U101B, leaving RC combination R137 and C157 as the controlling input to U102A. As long as the master processor is strobing the segments to the FIP the RC network will remain discharged leaving RC combination RP3 and C159 at the output of U102A charged--ultimately keeping Zrst/ high. If the strobing of the FIP should stop the state of the RC combinations reverses and Zrst/ is driven low, clearing U101B and resetting the CPU. The initialization routines are now run and the process begins again. If the processor is terminally crashed the reset will be attempted once and then stopped. The reset also works for power brown outs or failures.

Powerfail And Battery Backup Circuits

There are two discrete circuits which monitor power levels in the PCM 70. The first is a comparator which monitors the power supplies secondary voltages at pin 5 of U103A. This level detector is used to sense a dropout in the line voltage and generate the signal PFAIL/. PFAIL/ is fed directly to the microprocessor as a non-maskable interrupt, forcing the software to acknowledge an early warning of eminent power loss.

The second power sensing circuit monitors the +5V supply using Q8 and Q9 to detect a half volt drop. When power is lost to the unit the power rails will begin to decay. Q8 will detect a drop in the +5V before it gets below a level which could cause a loss of memory or other circuits to affect memory. Q8 also provides the signal PLOW which is detected by U102B to provide a system reset. The reset will clear the front panel to protect against burnout should the power loss be momentary and force the system to restart. Early power losses detected should provide ample time for the microprocessor to file any necessary information into memory before the +5V failure occurs. PLOW also drives the base of Q9, which will disconnect the failing +5V rail from the memory circuits RP2 and U91. Diode CR46 prevents any leakage current by isolating the battery from the +5V rail and diode CR45 isolates the battery from receiving any charging currents when the power is normal. When PLOW causes a reset it also causes the signal MEMBKU via U102C which in turn disables U102D and drives Q11. Q11 is used to control power to the memory signal buffer U100, thereby disconnecting its outputs from the +5V rail, preventing additional current leakage paths for the battery, and preventing accidental memory access as the power fades. To maintain memory information it is necessary to provide nonchanging, battery level memory control signals. This is accomplished by connecting these memory control signals through RP2 to the controlled +5 or battery power point. The battery is also connected to pin 8 of U103 so that the system program can monitor or be alerted when the battery voltage drops below 2.5 volts and thereby warn the user.

Memory

The master processor has one RAM slot and one ROM slot. The RAM is backed up by a battery for non-volatile storage of system parameters during power down. The socket used for RAM is configurable for an 8k x 8 static RAM. An EPROM or masked ROM may be used in the socket provided for ROM. The system may be configured with either 16k x 8 or 32k x 8 EPROMs. Jumpers W13 and W15 are provided for selection. Memory map addressing is shown in Table 4.5.

Bidirectional Communications Port

Communications between the master and slave processors is provided by the bidirectional communications port composed of data latches U81 and U89, control port U69 and the associated R-S flip flop U79. The scenario in which the port is used is as follows. The master strobes a byte into data latch U81 by activating MPRTOUT/. Strobing this line sets MDAV to a 1. The slave processor in monitoring the status of the port finds MDAV high thus knowing that a byte is available in the port from the master processor. The slave then strobes SPRTIN/ reading in the byte. SPRTIN/ resets MDAV to 0 thus indicating to the master processor that the byte has been read. Passage of data from slave to master is the same except that the strobes used are SPRTOUT/ and MPRTIN/ and the data latch is U89. If the slave processor does not respond to the master processor when data is available, the master may reset the slave by bringing SLVRST/ low. This feature allows the slave processor to be restarted in the unlikely case of a crash. For correct addressing refer to Table 4.5.

4.3.2 Slave Processor

The slave processor is reset from a strobe from the master processor (SLVRST/). After reset initialization the slave processor must only update the WCS with program changes and monitor the bidirectional communications port for commands from the master processor.

Memory

The memory address space is divided into three slots. One slot is for either an 8k x 8 or a 16k x 8 EPROM, one slot is for a 2k x 8 or 8k x 8 static ram and the third slot is for the writable control store. Memory mapping information is found in Table 4.6.

Bidirectional Communications Port

The bidirectional communications port has been fully described above in Section 4.3.1.

WCS Access Control

During the first program load, the Slave has direct control over access to the WCS. The WCS is the micro-control store for the PCM 70. Once the first program is loaded only pseudo control is exercised by the Slave. The process for writing to the Z80 writable control store is explained below.

At power-up of the PCM 70 the writable control must be loaded with a micro program for the use of the HSP. To accomplish this loading, during the Slave's initialization routine COPY/ is strobed. Bit 0 of the data bus is a zero. This sets COPYST/ to 0 in latch U83A. The Slave then strobes COPY/ again with bit 0 set to a 1. This sets COPYST/ to a 1 and provides a clock edge to the clock input of latch U78. The upper seven bits of the data bus should be set to address a used portion of EPROM U67. This action then guarantees that OP/ will occur. COPY/ is strobed a final time with bit 0 reset to 0. A short period should be allowed to elapse (approximately 20 us before the WCS is written to by the Slave. This will insure that OP/ has occurred clocking COPYST/ to U83B. This will set ACCESS to zero thus allowing the Z80 to load the program to the WCS. Once the program has been loaded the Slave again strobes COPY/ but this time bit 0 is a one. Again OP/ strobes U83B to allow the WCS to be in the copy mode (this mode will be explained in the section on the WCS). After at least 30 micro seconds have elapsed the Slave strobes COPY/ with bit 0 again a zero. When both OP/ (MIB 29) and AS1/ are low at the inputs to U65D, the output is 0 and this output is fed to the clock input of U83B. When AS1/ goes high U83B is clocked. This rising edge clocks the output of U83A to the output of U83B. It can be seen that the Slave initiates the change of mode sequence but that the final events do not take place until the HSP starts execution of an operation type instruction. One other point mentioned here in passing but explained fully in the section on the WCS is the addressing of the EPROM containing the high byte of the 32 bit micro instruction. When the WCS is starting the copy mode, COPY/ is once strobed setting COPYST/ to a one. This clock edge clocks data bits 1-7 into U78. These address bits provide provide addressing to U67. The timing diagram for the WCS is shown in Figure 4.4.

Writable Control Store (WCS)

The WCS is composed of four high speed 1k x 4 static RAMs which are divided into two banks of 1k x 8. U75 and U84 form the portion of the WCS which is writable by the Slave processor. U77 and U86 are the portion of the WCS which are either being read by the HSP or are being written into during the copy mode. The high byte of the micro instruction is stored in a 200ns EPROM (U67).

The following description explains in detail the two modes of the WCS. Power-up initialization has been completed by the Master, the Slave is reset and initializes its environment. The Slave is now ready to load the WCS (U75 and U84) with the desired micro-program to be run by the HSP. ACCESS is set to zero thus enabling the Slave data port (U85) and the Slave address port (U94 and one half of U93). This allows the Slave to write to the WCS from its address space. Address buffer U87, one half of U93, and data buffer U74 are at this point disabled. The mapping of the WCS into the Slave address space as follows:

The low three bytes of the micro-word are stored in the high speed RAMs (MIB<0:23>) while the high byte is stored in EPROM U67 (MIB<24:31>). With a micro-program length of 128 steps, 3 x 128 = 384 bytes must be written by the Slave. Loading of each of the three bytes must correspond to the locations that they will be read from when the WCS is in the copy mode. Table 4.2 shows how this has been determined and how this scheme determines the addressing of the slave processor.

bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
AS2/ SADR9	AS1/ SADR8	AS0/ SADR7	SAB6 SADR6	SAB5 SADR5	SAB4 SADR4	SAB3 SADR3	SAB2 SADR2	SAB1 SADR1	SAB0 SAD0

Table 4.2. Slave to WCS address encoding.

The low byte of the micro-instruction is accessed when AS1/ is low. The next byte is accessed when AS2/ is low and the third byte is addressed by AS0/ low. Since only one of AS<0:2> is low at any given time, the following address scheme is derived.

MIB<0:7>

addr bits			AS1/
1010000000	(binary)	=	280h
1011111111	"		2FFh

MIB<8:15>

addr bits			AS2/
0110000000	(binary)	=	180h
0111111111	"		1FFh

MIB<16:23>

addr bits			AS0/
1100000000	(binary)	=	300h
1101111111	"		37Fh

Table 4.3. WCS parallel output sequencing.

Referring to the memory map in Table 4.6, we see that the WCS is mapped into 8000h of the Slave address space. Combining this fact with the addressing scheme shown above we have:

MIB<0:7> 8200h - 82FFh

MIB<8:15> 8180h - 81FFh

MIB<16:23> 8300h - 837Fh

The high byte of the WCS is contained in U67. The method of addressing is explained here. The low order seven bits of the address are provided by the HSP program counter (SAB<0:7>). The remaining seven bits are latched into U78. Since for any given program only one page of 128 bytes is needed, this scheme provides 128 different pages for effects. Address latching occurs at the beginning of the copy mode.

WCS Copy Mode

This section explains the operation of the WCS during copying of the microcode written by the Slave. Once the Slave has written either an entirely new program or just several bytes the WCS is placed in the copy mode. The chain of events that causes this copying is now explained. The Slave strobes COPY/ with bit 0 of the data word set to 1. The upper seven bits of the data byte are used to address the correct page in U67 as explained previously, so care must be taken to either preserve the page number or to change the page address to the appropriate page address. When bit0 is latched into U83 as a 1, the clock edge created by COPYST/ clocks these upper seven bits into U78. If the change to the microcode is such that the page address must change the the audio output must be muted by the Master by asserting MUTE/ before the new program is copied. This will prevent glitching or popping at the audio output. Once the program has been copied the MUTE/ must be removed. Once COPYST/ has been set to a one copying begins when OP/ (which occurs three times every sample cycle, two outputs one input) is active and AS1/goes from low to high. Copying now proceeds with the buffered HSP program counter now addressing the both banks of the WCS. Devices U85, U94 and 1/2 of U93 have all been disabled and devices U74, U87, and 1/2 of U93 are now enabled to allow copying of the updated microcode from U75 and U84 to U77 and U86. During normal operation (COPYST/ set to 0) the microcode used for the current program running is being supplied from U77 and U86. Addressing is provided by the program counter bits SAB<0:6> and AS<0:2>. As each of the three bytes are accessed the rising edge of the respective phase clocks (AS<0:2>) clocks the data from the MI bus into the appropriate pipeline register (U56 or U66).

The MMU contains registers for holding the 16 bit offset information. During AS1/ the low byte of the offset is latched into U66. The high byte is available at the end of AS2/. On the rising edge of AS2/ the 16 bit offset is latched into the the MMU. The third byte of microcode is latched into U56 by the rising edge of AS0/ The fourth byte MIB<24:31> is clocked into U58 when both AS0/ and MC are low (see timing diagram). One of the elegant aspects of the 'copy' scenario is that the mode of the WCS is transparent to the pipeline registers. When copying is occurring, U75 and U84 are being read and U77 and U86 written but the micro control register pipeline is still clocking data off the MI bus, so data being copied is also being used by the HSP.

Data is written to U77 and U86 by creating a clocking signal by ORing MC with ACCESS/. After the copy is completed the Slave sets COPYST/ to zero and allows a brief period of time to elapse for an OP/ instruction to execute thus setting the WCS back to the normal mode.

4.3.3 High Speed Processor

There are five major blocks in the HSP:

- Converter Management Unit (CMU)
- Arithmetic Unit (ARU)
- Memory Management Unit (MMU)
- Timing and Control (T&C)
- Digitized Audio Memory (DAM)

Each of these blocks are explained in detail below. The timing diagram in Figure 4.4 shows the timing relationship of the micro-control bits provided to the HSP by the WCS.

CMU

The CMU is thoroughly described in the analog section of the theory of operation. Let it suffice to say here that all digitized audio is gated from the analog world to the digitized audio bus (DAB) and gated from DAB to the analog world by the CMU.

T&C

The T&C module contains the clock and state generation circuitry and microinstruction decode and control signal generation circuitry. The clock generation circuitry is composed of a crystal clock oscillator (U50) running at 13 Mhz, and driver U36A. This output is used to drive the HSP as the Master Clock (MC) and also is divided to provide clocks for the rest of the system. A divide by four counter (U68) is used to provide both the master and slave processor clocks of 3.25 Mhz. The MC is also divided and used as the clock for the MIDI UART (U97). MC is first divided by two by U68B and then divided by 13 by U60 to produce a 500 khz clock signal.

State generation is performed by U49 and U37. ROM U49 decodes the signals ST0, ST1, DP/, DPD/ and ACC to generate state information for the ARU. This state data is clocked every MC into U37. AS<0:2> are also generated by ROM U49. These phase clocks are used to drive the microprocessor control register pipeline, the ARU, the MMU and all addressing in the WCS.

Microinstruction decode and control signal generation is performed by ROMs U48 and U49. U48 decodes coefficient bits MIB<16:19> to generate the correct mode bits (M4-M0 for the old ARU or F2-F0 the new ARU) as well as CIO/. SC, BCON3, BCON0 and AREG/ are generated by U49 and are latched every MC by U35. All of these signals combined provide state control over the ARU double and single precision multiplies.

Control of the DAM timing is started by clocking and then reclocking MIB30 and MIB31 by U37. The reclocked signals (MCEN/ and MWR) are used to enable memory control (RAS, CAS) hardware when either reading from or writing to DAM. Delay line U53 is used to provide the correct timing relationship between RAS and CAS.

Memory Management Unit (MMU)

The MMU (U54) is clocked by AS2/. The rising edge of AS2/ clocks the micro-program counter which generates SA<0:6>. Address pipe register U76 is used to allow for long propagation delays for transitions on the SA lines. The SAB lines are used for addressing of the WCS as described previously. SAB5 is used to clock U64 for generating SAMP and also to generate ZINT/ for both the master and the slave processor. An interrupt is generated every eight samples cycles or approximately every 236 us. There is a sixteen bit current position counter, a 16 bit offset register and a sixteen bit subtracter within the MMU. The current position counter is clocked by the falling edge of SA6 (the end of the sample cycle). The address offset information is clocked into the offset registers by the rising edge of AS2/. The offset is provided by MIB<0:15> of the micro-instruction during any memory operation. The output of the address offset register is subtracted from the output of the current position counter. The output of the subtracter is multiplexed into the 8-bit address output YA<0:7>. The multiplexer input is selected by the SEL line which is generated using delays of AS0/. SEL high selects the low eight bits of the subtracter.

Digitized Audio Memory (DAM)

The DAM is composed of a bank of dynamic RAM, each 64k x 4, providing 64k words of digitized audio storage. RAS/ and CAS/ are generated using delay line U53 and gates U42, U29 and U43. When MCEN is active, addressing of DAM is allowed. The delay line provides the correct timing relationships between RAS/ and CAS/.

Arithmetic Unit (ARU)

The ARU (U25) consists of four 18-bit register files, an 18 by n-bit multiplier with saturation logic, an 18-bit accumulator and an 18-bit transfer register. The path to and from the ARU is an 18-bit bidirectional data path with bits 0 and 1 tied high. Data can be loaded to the register files in the ARU from either data put onto the DAB from the CMU or data on the DAB can be supplied by reading from the DAM.

The 4 x 18 bit register files act as a temporary store for multiplicands from the DAB. The multiplier performs an 18-bit x 3-bit multiply and accumulate every machine cycle (230 ns). The control signals to the multiplier are generated by the T&C module described previously. The transfer register acts as a buffer between the outputs of the multiplier and the DAB, allowing the multiplier to perform the next multiplication without waiting for its previous result to be read by the other devices on the DAB. Similarly, other parts of the ARU are pipelined to maximize operating speed.

4.4 Memory and I/O Maps

This section provides memory and I/O mapping of the PCM 70. The maps of the master processor are provided first and then the maps of the slave. A bit assignment map is then provided for all I/O ports where necessary. A small dictionary describing signal names may be found at the end of this section.

0000H 3FFFH	16K X 8 EPROM 27128 OR
4000H 7FFFH	32K X 8 EPROM 27256
8000H 9FFFH	8K X 8 SRAM BATT BACKUP
A000H FFFFH	NOT USED

Table 4.4. Master processor memory map.

Signal Name	Read Cycle	Write Cycle	Address
DAC/	----------	DATA	00H
DIGSEL0/	----------	DATA	10H
DIGSEL1/	----------	DATA	20H
SEGSEL0/	----------	DATA	30H
SEGSEL1/	----------	DATA	40H
STATIN/	DATA	----------	50H
STATOUT/	----------	DATA	60H
HEADRM/	DATA	STROBE	70H
SLVRST/	----------	STROBE	80H
MCPRT/	DATA	----------	90H
RDDATA/	DATA	----------	A0H
RDSTAT/	DATA	----------	B0H
WRDATA/	----------	DATA	C0H
WRCONT/	----------	DATA	D0H
MPRTIN/	DATA	----------	E0H
MPRTOUT/	----------	DATA	F0H

Table 4.5. Master processor I/O map.

4.4.1 Master Processor I/O bit assignment

DAC/: This signal is used to strobe data out to the mix D/A converters. The channel which receives the data has been selected by a bit in the STATOUT register.

DIGSEL0/: This port is used to select the digit activated in the low order eight digits on the front panel display. Digits are numbered from 0 to 7 starting from the right most end of the FIP. The digit desired selected by writing a 1 into the corresponding bit. DIGSEL0/ is also used to scan the 8 columns of the switch matrix.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
col 7 digit 7	col 6 digit 6	col 5 digit 5	col 4 digit 4	col 3 digit 3	col 2 digit 2	col 1 digit 1	col 0 digit 0

col 0 : switches 0,8
col 1 : switches 1,9
col 2 : switches 2,10
col 3 : switches 3,11
col 4 : switches 4,12
col 5 : switches 5,13
col 6 : switches 6,14
col 7 : switches 7,15

Note: Columns are numbered from left to right.

DIGSEL1/: This port is used in the same way as DIGSEL1/ except that it is used to select the upper eight digits on the FIP.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
digit 15	digit 14	digit 13	digit 12	digit 11	digit 10	digit 9	digit 8

SEGSEL0/: This port is used to select eight of the sixteen segments used to form characters displayed on the FIP. The table below shows which segments must be activated to display each character.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
seg f	seg g	seg e	seg n	n/a	seg j	seg m	seg d

SEGSEL1/: Same as SEGSEL1/ except that it is used to select the remaining eight segments of the FIP.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
seg dp	seg c	seg h	seg l	seg i	seg k	seg b	seg a

STATIN/: This port is used to determine the status of devices used to interface the PCM 70 to the outside world.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Ext. bypass	Reg. step	Row 2	Softk PhaseB	Row 0	Softk dir	Row 1.	softk. phase A

Row 0: switches 0-7

Row 1: switches 8-15

Soft Knob direction :0=counter-clockwise rotation

:1=clockwise rotation

STATOUT/: This port is used to activate several devices in the PCM 70. These devices are the six switch LEDS, mute control and mix channel select.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LED5/	LED5/	LED4/	LED3/	LED2/	LED1/	DACSEL	MUTE/

LED1-6/ : 0 lights LED. LEDs are numbered from top to bottom and from left to right.

DACSEL : 0 selects channel 0 which controls the attenuation of the unprocessed audio.

DACSEL : 1 selects channel 1 which controls the attenuation of the digitized audio.

MUTE/ : 0 mutes the audio output.

HEADRM/ : This port is used to read the audio signal level. The level is represented by an 8-bit word. The port must first be written to initiate the conversion and then the converted signal is read.

SLVRST/ : This strobe is used by the master to reset the slave on power-up or in the event that the slave crashes.

MCPRT/ : This port is used to determine the status of the communications port between the master and the slave processors.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
N/A	N/A	N/A	N/A	PFAIL/	BLOW	SDAV	MDAV

MDAV : 0 data read by the slave 1 data available for the slave.

SDAV : 0 data not available from the slave 1 data available from the slave.

BLOW : 0 battery is within range
:1 battery is low

MPRTIN/ : This port is used to read data sent by the slave. Reading the port resets SDAV.

MPRTOUT/ : This port is used to write data to the slave from the master. Writing to the port sets MDAV.

4.4.2 MIDI Ports I/O Bit Assignment

RDDATA/ : This port allows the master to read incoming MIDI data from the UART.

WRDATA/ : This port is used by the master to place data on the MIDI lines.

RDSTAT/ : This port is used by the master to determine the status of the MIDI interface.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
N/A	N/A	TBRE	N/A	PE	OE	FE	DA

DA : Data available
FE : Framing error
OE : Overrun error
PE : Parity error
TBRE : Transmitter buffer register empty

WRCONT/ : This port is used to write control information to the UART.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
N/A	N/A	N/A	PI	SBS	EPE	WLS1	WLS2

WLS2 : Character length select
WLS1 : Character length select
EPE : Even parity enable
SBS : Stop bit select
PI : Parity inhibit

0000H 1FFFH	8 X 8 EPROM 2764 OR
2000H 3FFFH	16K X 8 EPROM 27128
4000H 7FFFH	8K X 8 SRAM
8000H 83FFH	1K X8 WCS
8400H FFFH	NOT USED

Table 4.6. Slave processor memory map.

Signal Name	Read Cycle	Write Cycle	Address
COPY/	----------	DATA	00H
SPRTIN	DATA	----------	20H
SPRTOUT/	----------	DATA	30H
NOT USED	----------	----------	40H
SCPRT/	DATA	----------	50H
NOT USED	----------	----------	60H
NOT USED	----------	----------	70H

Table 4.7. Slave processor I/O map.

4.4.3 Slave Processor I/O Bit Assignment

COPY/ : This port is used to set the status of the WCS access line and to provide address bits for the EPROM which contains the upper byte of HSP micro-code.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
N/A	A12	A11	A10	A9	A8	A7	access

ACCESS : 0 allows the writable control store to be written by the slave Z80.

ACCESS : 1 puts the WCS into the copy mode.

SPRTIN/ : This port is used by the slave to obtain data sent by the master. Reading the port resets MDAV.

SPRTOUT/ : This port is used by the slave to send data to the master. Writing to the port sets SDAV.

SCPRT/ : This port is used by the slave to determine the status of the communications port between the master and the slave.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
N/A	N/A	N/A	N/A	PFAIL/	PFAIL/	SDAV	MDAV

MDAV : 0 indicates that no data is available in the master data port.

1 indicates that the master has written data into the port.

SDAV : 0 indicates that the master has read data from the slave data port

1 indicates that the master has not read data in the data port.

5

Troubleshooting Guide

5.1 Introduction

This section contains troubleshooting procedures to help locate malfunctions. A good knowledge of digital and analog electronics is assumed.

The electronics of the PCM 70 consist of two modules: the motherboard and the front panel board. The motherboard contains the power supply, the analog input and output circuitry, the A/D and D/A converter, the digital signal processor, the master and slave microprocessors and their associated circuitry, the writable control store, and the fluorescent indicator panel (FIP) display with its drivers.

The front panel board contains pushbuttons, LEDs and the digital rotary encoder (Soft Knob).

5.2 Preliminary Inspection

A thorough visual inspection of a malfunctioning unit is a good troubleshooting practice. Check for obvious component failures such as burnt or overheated parts or damaged PC board traces. There should be no loose ICs, connectors, or cables. Observe whether the malfunction is intermittent, heat related, or shock related.

Always start with possible global problems and work down to the local level. For instance, first determine whether the problem is mechanical (such as improperly seated ICs or connectors) or electrical. If the problem is electrical, check fuses, the power switch, primary wiring, line voltage, and power supply voltages (including regulator input p-p ripple values for signs of abnormal loading.)

5.3 System Troubleshooting

There are several system diagnostic aids that can be used to isolate problems:

1. Power up diagnostics.

2. Various diagnostic programs that can be called up during power up diagnostics.

3. A self-test jumper located at the converter which disassociates the analog circuitry from the data memory and the digital signal processor.

The power up diagnostics are executed every time the PCM 70 is turned on; they take approximately four seconds to complete. The diagnostics make a single pass through testable features of the unit (digital circuitry that can be examined by the master and slave processors) and if an error is found the FIP will display an error message. These error messages are:

1) MASTER ROM ERR : Master microprocessor ROM checksum error.

2) BATTERY LOW: Nonvolatile RAM backup battery voltage too low to guarantee data retention.

3. POWER LOW: Line voltage too low for proper operation of unit.

4. SYSTEM RESET, LOADING PGM 0.0: Indicates that nonvolatile RAM didn't retain data.

5. SLAVE DEAD ERR: On power up, the Master processor resets the Slave processor. The Slave then conducts its own diagnostics and reports its status to the Master. This error message indicates that the Slave will not report to the Master, indicating that the Slave has not started up, or that attempts to reset the Slave were unsuccessful.

6. SLAVE ROM ERR: Slave ROM checksum error.

7. SLAVE RAM ERR: Unsuccessful Slave write/read RAM test.

8. SLAVE CHECKOUT ERR: The Slave has passed an invalid status code to the master, and has probably crashed.

9. SLAVE WRITE ERR: The Slave won't accept data from the Master, and has probably crashed.

5.3.1 Diagnostic Programs

During the power up diagnostics, other diagnostic programs can be accessed from the front panel by pressing the following keys and then pressing the LOAD key.

0. CLEAR MEMORY: Clears nonvolatile ram of all data. Clearing memory destroys the contents of all registers and should not be executed unless RAM data is validated to be bad or after changing backup battery. The FIP will display "ARE YOU SURE ?", and pressing the 1 key after this prompt will clear memory, reset the system, and load PGM 0.0.

1. GENERIC PGM: Loading this program will allow you to access high speed processor diagnostic programs. 0,1 and 2. Press the 7 key, dial in the program you want with the Soft Knob, and press LOAD. These programs perform the following functions:

   Diagnostic 0: Zero delay with output to both left and right channels
   Diagnostic 1: Zero delay with output to left channel only
   Diagnostic 2: Zero delay with output to right channel only

2. KEY AND SOFT KNOB TEST: Described in Section 3.2.3.

3. DISPLAY TEST: Described in Section 3.2.3.

4. MIDI WRAPAROUND : Described in Section 3.2.3.

5. MIDI EVENTS: This routine will display in decimal the MIDI control code of the device which has generated a MIDI event.

5.3.2 Self-Test Jumper

Moving the blue tab on jumper block W8 from RUN to ST will place the PCM 70 in the self-test mode. When self-test is activated, the only digital signals required to run the analog circuitry are the converter timing signals. Thus, the analog circuitry can be tested without consideration for much of the functionality of the digital circuitry. In a properly functioning unit running Diagnostic 0, the output in self-test and run modes should be identical.

5.3.3 Symptom Troubleshooting

No Display, Garbled or Stuck Display

Check the power supplies and all related circuitry, following the procedure outlined in Section 3.2.2.

Since the display is controlled by the Master processor (U82), display problems are often an indication that either the Master is not running or stuck, or that there is some malfunction in the control and data path from the Master processor to the display.

Assuming that all supply voltages are correct, check Master Processor U82, pin 6 for clocking. If there is no clock, U50, U36 or U68 may be the cause. Since the display is interrupt driven, the Master processor interrupt line should be examined. Check U82 pin 16 or TP22 for interrupts every 236 us. If it is stuck in either logic state, U64, U54, U35, U43, U49 or U102 may be the cause.

Check for constant high on NMI/ and RST/ (U82 pins 17and 26). If these lines go low, the power fail/power low circuitry (U101, U102, or U103 and associated components) may be the cause. Check address MADR <0:15> and data MDB <0:7> lines on the Master processor (U62) for proper activity or shorted lines. If there is no activity, U82, U62, U90, or U91 may be the cause.

Insure that the pin contact lever on the ZIF sockets for ROMs U62, U67, and U95 are fully pushed down. Check pin 11 of U27, U39, U38, and U51 for clocking of display data. If there is no clocking, U59 may be the cause.

Follow the flow of data through latches U27, U39, U38, and U51 to display drivers U28, U41, U40, and U52 where data is converted to HV logic levels, to the FIP. The chip where the data flow stops is the culprit.

If the above circuitry is determined to be functional, the Master should be able to run power up diagnostics. If there is nothing on the display, the FIP is suspect. If the display is garbled, run the display test diagnostic outlined in section 3.2.3 to determine if particular segments of the display are malfunctioning.

No Audio (Dry Signal)

Check the PCM 70 block diagram for the flow of analog signals. The analog signal flow is straightforward, so problems in the input and output stages should be easy to locate, assuming the front panel and Master processor are functioning.

Assuming that all supply voltages are correct, press the BYP key. If there is still no dry audio, probe TP18 with a DMM. A -0.6V level will verify operation of the dry mix DAC. If the DAC checks out OK, the problem is in the dry audio circuitry. Apply -12dBV @ 1kHz to J3 with INPUT and OUTPUT LEVEL pushbuttons "in" and INPUT LEVEL pot fully clockwise. No signal present at TP 14 indicates input stage

problems. Presence of signal at TP 14 but not TP20 indicates VCA (U14) problems. Presence of signal at TP20 and not at J1 and J2, indicates the output stage and output mute FETs Q1 and Q3 and their associated biasing circuitry are suspect (assuming PFAIL/ is high).

No Audio (Wet Signal)

If there is dry audio but no wet audio output, the malfunction is in either the wet analog signal path, the converter circuitry, the high speed processor, or the writable control store/Slave processor.

Assuming all supply voltages are correct, set parameter 0.0 (MIX) to 100% WET and probe TP15. A 0V level will verify operation of the wet mix DAC. Apply -12dBV @ 1kHz to J3 with INPUT and OUTPUT LEVEL pushbuttons "in" and INPUT LEVEL pot fully clockwise. The presence of signal at TP7 but not TP2 or TP13 indicates either converter, HSP or WCS/Slave malfunction. The presence of signal at TP1 and TP12, but not at TP5 and TP11 indicates VCA (U2 and U13) problems.

Place the PCM 70 in converter self-test mode by moving the blue jumper on W8 to its upper position. If wet signal now appears at the output, the problem is probably in the high speed processor, or possibly the writable control store.

If there is no signal in self-test mode, check output of I/V converter U5, pin 6 against Figure 5.1. If the signal appears here but not at TP6 and TP3, deglitch circuitry U4, U9 and associated timing signals SDEG1, SDEG1/, SDEG2, SDEG2/ and DEG (U26, pin 13) are suspect. Check these signals against the timing diagram. If these timing signals are missing or defective, the WCS, MMU, gates U36, U26, U21 or latch U76 are suspect. If these signals are correct, check OUT (U10, pin 16), OUT/ (U10, pin 1) and SAMP (U26, pin 8). If these signals are missing or defective, U64, U26, or U21, are suspect. If these signals are correct, check output of sample/hold circuit (U11, pin 6) against Figure 5.2. If these signals are correct, check INB/ and OCLKD as described in Section 5.3.4. If these signals are correct check the output of the DAC (U15, pin 21) and the comparator (U16, pin 7) vs. CCLK (U20, pin 23). If these signals are missing or defective, the WCS, DAC, comparator, CMU (U20) or U10 are suspect.

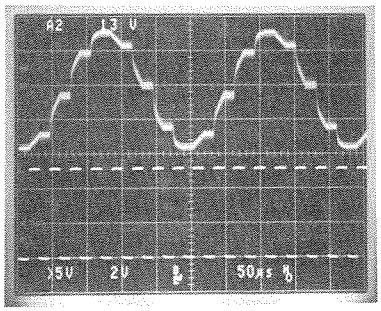

Figure 5.1. Output of sample and hold circuit (upper trace, U11, pin 6) vs. SAMP. (lower trace, U64, pin 14). The input is a sine wave at 4.231 kHz (sampling frequency/8) at maximum converter level--the point at which the red OVLD LED just turns off.

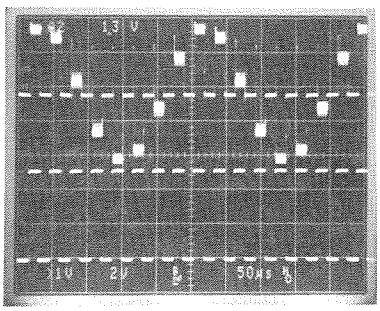

Figure 5.2. Output of I/V converter (upper trace, U5, pin 6) vs. OUT (lower trace, U10, pin 16). The input is a sine wave at 4.231 kHz (sampling frequency/8) at maximum converter level--the point at which the red OVLD LED just turns off.

Noisy or Distorted Audio (Dry Signal)

Assuming all supply voltages are correct, adjust trimpot R86 for minimum dry VCA distortion following the procedure outlined in Section 3.2.8. Monitor the analog signal flow through the test points outlined in Section 5.3.4, *No Audio (Dry Signal)* with a THD+N meter to isolate the problem to input stages, output stages, or VCA.

Noisy or Distorted Audio (Wet Signal)

Assuming all supply voltages are correct, place the unit in self-test mode by moving the blue tab on Jumper Block W8 to the "ST" position. If the noise or distortion goes away, the malfunction is in the HSP or WCS. If the noise or distortion is still present, adjust trimpots R10 and R36 for minimum VCA distortion as outlined in Section 3.2.8. Monitor the analog signal flow through the test points outlined in section 5.3.4, *No Audio (Wet Signal)* with a THD+N meter to isolate the problem to converter or VCAs.

5.3.4 Writable Control Store/Slave Processor

The purpose of the WCS (writable control store) is to provide a 32 bit wide microword for each of the 128 program steps of the high speed processor. Upon a program change or power up, the slave processor downloads a microprogram to the WCS RAM. Until another program change, the slave processor's only function is to dynamically update the microprogram in the WCS RAM.

A good quick test of WCS functionality is to check INB/ (A/D in, U20, pin 18) and OCLKD (D/A out, U20, pin 19) against SAB6 (MSB of HSP program counter) as shown in the converter timing diagrams. This one input, two output per sample cycle system is common to all PCM 70 microprograms, and is a good indication that the slave processor has downloaded a program. If these signals are missing or incorrect, repeated program loads should be attempted to determine a permanent or intermittent malfunction. Check the HSP three phase clock signals AS/<0:2> on U77 against timing diagram. Missing or defective signals indicate a HSP malfunction. Check program counter bits SAB<0:6> on U77. Missing or defective bits indicate the malfunction is in MMU (U54) or U76. Check address bits A7, A8 and A9 on the Opcode ROM (U78 pins 3, 25 and 24, respectively). The binary number on these three pins will correspond to the row number of the downloaded program, i.e., a binary 0 is the diagnostic programs, a binary 1 is Chorus and Echo, binary 2 is Multiband Delay, etc. If there is no correspondence, U78 or the Slave processor is malfunctioning.

If the problem still cannot be found, try replacing WCS RAMs U75, U84, U77, and U86. If this doesn't work, buffers U85, U94, U93, U87, latches U66, U56, U58, and ROMs U67, and U95 are suspect.

Signature analysis is a useful tool in troubleshooting the WCS. Follow the procedures outlined in Section 5.3.6.

5.3.5 High Speed Processor (HSP)

Signature analysis is the major tool for troubleshooting the HSP. The PCM 70 is put into a stable state where signatures can be taken by running Diagnostic 0. Refer to Section 5.3.6, *Signature Analysis* for the proper setups and signatures.

If a signature analyzer is not available, check the three phase clock signals AS0/ (U35, pin 16), AS1/ (U36,pin 8) and AS2/ (U35, pin 2) against timing diagrams. Missing or defective signals point to timing ROM U49, U35, or U36. If the complaint is noise or poor sound a defective HSP data memory may be the cause. RAMs may be swapped from high bits (U45) to low (U30) to help isolate the defective chip. *If swapping alters the quality of the noise, the problem is probably one of the RAMs.* If swapping does not affect the noise, a defective ARU (U25) is possible. A can of freeze spray is helpful in isolating component failure due to heat related timing errors or intermittent mechanical failures. If a RAM, MMU or ARU chip can be quieted by chilling, it should be replaced.

5.3.6 Signature Analysis

Because the digital signals in the PCM 70 can be quite complex, signature analysis tables have been provided as a useful aid in locating the source of a problem.

Signature analysis is a technique used to troubleshoot electronic logic circuits. A signature analyzer (Hewlett Packard 50045A or equivalent) is connected to the PCM 70 being tested and the test pattern is started. Long, complex data stream patterns are compressed into a unique four-segment "signature" that the analyzer will display for each point in the unit being tested as the analyzer probe is moved from point to point. The analyzer requires several signals from the unit under test: the clock signal synchronizes the analyzer and the unit under test; the start and stop signals define the bounds between which the data signal is examined by the analyzer. After the stop signal, the analyzer displays the signature of the data it received. If the signature displayed does not match the corresponding signature given in the table, the circuitry connected to the node is malfunctioning.

The correct signatures for various sections of the PCM 70 are summarized in the signature tables which follow. The conditions for taking the signatures are listed with each module and setup.

Note: The following signature tables apply *only* to REV 2 motherboards.

PCM 70 Signature Tables REV 2 Motherboard Only

WCS
Schematic: Sheet #5, Rev 3
Setup: Clock = AS1/ ⌐L TP21,p3
Start = SAB6 ⌐L TP21,p5
Stop = SAB6 ⌐L
+5V = 6PCP
* = unstable
W8 = ST position
- = Line not associated with circuitry being tested.
F.P. = Program - Diagnostic 0
Lift and jump U54,p15 to 5V

U66:				U76:		
1)	0000	20) 6PCP		1)	0000	20) 6PCP
2)	F170	19) CF94		2)	A70F	19) 3CPF
3)	6PCP	18) 1C8A		3)	4P18	18) 77H9
4)	1C8A	17) 6PCP		4)	2397	17) C469
5)	6575	16) 6575		5)	91FC	16) 5A34
6)	0PCP	15) 3A06		6)	2595	15) 1F8F
7)	84H7	14) UA28		7)	4C2C	14) 3919
8)	079C	13) 079C		8)	6PCP	13) U2U8
9)	PP3F	12) 4270		9)	6PCP	12) U97F
10)	0000	11) 6PCP		10)	0000	11) 0000

U56:				U67:		
1)	0000	20) 6PCP		1)	6PCP	28) 6PCP
2)	6PCP	19) HA2F		2)	0000	27) 6PCP
3)	6PCP	18) 079C		3)	0000	26) 0000
4)	1C8A	17) 079C		4)	A70F	25) 0000
5)	H424	16) HA2F		5)	3CPF	24) 0000
6)	H424	15) 7H14		6)	91FC	23) 0000
7)	1C8A	14) UA28		7)	5A34	22) 0000
8)	6PCP	13) 84H7		8)	U97F	21) 0000
9)	6PCP	12) IC8A		9)	1F8F	20) 0000
10)	0000	11) 6PCP		10)	2595	19) 4F14
				11)	0993	18) CP84
U58:				12)	0993	17) FAPA
1)	0000	20) 6PCP		13)	H1F1	16) 00PF
2)	0993	19) 6PCP		14)	0000	15) 5FC2
3)	0993	18) 6PCP				
4)	0993	17) 6PCP		U65:		
5)	0993	16) 6PCP		1)	0000	14) 6PCP
6)	H1F1	15) FAPA		2)	0000	13) FAPA
7)	H1F1	14) FAPA		3)	0000	12) 6PCP
8)	5FC2	13) 00PF		4)	*	11) 6PCP
9)	5FC2	12) 00PF		5)	6PCP	10) 0000
10)	0000	11) 6PCP		6)	*	9) 6PCP
				7)	0000	8) 0000

HSP
Schematic: Sheet #6, Rev. 3
Setup: Same as WCS

U20:	1)	0000	40)	*	
	2)	*	|	*	
	|	*	23)	*	
	17)	*	24)	0000	
	18)	C75U	23)	9FP0	
	19)	30U4	22)	00PF	
	20)	*	21)	6PCP	
U21:	1)	P732	14)	6PCP	
	2)	898F	13)	A7H5	
	3)	F96C	12)	F96C	
	4)	A7H5	11)	898F	
	5)	9FP0	10)	P732	
	6)	U25P	9)	6PCP	
	7)	0000	8)	0000	
U26:	1)	2P59	14)	6PCP	
	2)	A70F	13)	2P59	
	3)	898F	12)	F9C2	
	4)	6PCP	11)	A7H5	
	5)	6PCP	10)	U25P	
	6)	0000	9)	6PCP	
	7)	0000	8)	9FP0	
U37:	1)	0000	20)	6PCP	
	2)	86A3	19)	6PCP	
	3)	86A3	18)	6PCP	
	4)	86A3	17)	6PCP	
	5)	86A3	16)	6PCP	
	6)	260A	15)	0000	
	7)	260A	14)	6PCP	
	8)	260A	13)	7534	
	9)	260A	12)	6PCP	
	10)	0000	11)	6PCP	
U36:	1)	0000	14)	6PCP	
	2)	6PCP	13)	A110	
	3)	A70F	12)	FUAP	
	4)	F9C2	11)	260A	
	5)	U25P	10)	48C4	
	6)	9FP0	9)	0000	
	7)	0000	8)	6PCP	
U73:	1)	0CFC	14)	6PCP	
	2)	CF94	13)	6575	
	3)	C75U	12)	6575	
	4)	6PCP	11)	0CFC	
	5)	-	10)	0CFC	
	6)	-	9)	F170	
	7)	0000	8)	CF94	

U34:	1)	0000	20)	6PCP	
	2)	6PCP	19)	H424	
	3)	6PCP	18)	FUAP	
	4)	H424	17)	6PCP	
	5)	6PCP	16)	6PCP	
	6)	6PCP	15)	6PCP	
	7)	6PCP	14)	6PCP	
	8)	0000	13)	H424	
	9)	0000	12)	6PCP	
	10)	0000	11)	6PCP	
U48:	1)	6PCP	20)	6PCP	
	2)	0000	19)	6PCP	
	3)	6PCP	18)	6PCP	
	4)	H424	17)	H424	
	5)	H424	16)	6PCP	
	6)	6PCP	15)	0000	
	7)	6PCP	14)	6PCP	
	8)	6PCP	13)	6PCP	
	9)	0000	12)	6PCP	
	10)	0000	11)	H424	
U55:	1)	0000	20)	6PCP	
	2)	6PCP	19)	H424	
	3)	6PCP	18)	H424	
	4)	H424	17)	6PCP	
	5)	H424	16)	6PCP	
	6)	H424	15)	6575	
	7)	H424	14)	FAPA	
	8)	HA2F	13)	HA2F	
	9)	HA2F	12)	HA2F	
	10)	0000	11)	6PCP	

HSP (Cont.)

U57:	1)	0000	20)	6PCP	U49:	1)	7534	16)	6PCP
	2)	5H28	19)	6PCP		2)	6PCP	15)	0000
	3)	0993	18)	6PCP		3)	6PCP	14)	7H14
	4)	0993	17)	H22A		4)	6PCP	13)	H424
	5)	5H28	16)	30U4		5)	A110	12)	1C8A
	6)	86A3	15)	2P59		6)	FUAP	11)	0000
	7)	CP84	14)	5FC2		7)	7H14	10)	6PCP
	8)	1C8A	13)	4F14		8)	0000	9)	0000
	9)	H424	12)	260A					
	10)	0000	11)	0000					

U25 & U35:
Setup: Same as WCS except Clock: AS2/ ⌐└

U25:	1)	0000	40)	*	U35:	1)	0000	20)	6PCP
	2)	*		*		2)	6PCP	19)	14UC
	|	*	33)	*		3)	0000	18)	14UC
	9)	*	32)	0000		4)	658C	17)	6PCP
	10)	6PCP	31)	6PCP		5)	574P	16)	6PCP
	11)	1470	30)	C0A4		6)	0000	15)	38C8
	12)	6PCP	29)	38C8		7)	0000	14)	38C8
	13)	1470	28)	574P		8)	0000	13)	U486
	14)	56C8	27)	0000		9)	2776	12)	A3A4
	15)	56C8	26)	6PCP		10)	0000	11)	6PCP
	16)	6PCP	25)	6PCP					
	17)	6PCP	24)	*					
	18)	6PCP	23)	2776					
	19)	0000	22)	6PCP					
	20)	5F7C	21)	6PCP					

HSP-MMU
Schematic: Sheet#7, Rev.2
Setup: Same as WCS except Clock: AS2/ _┌

U45:	1)	0000	18)	0000
	2)	*	17)	*
	3)	*	16)	9AC0
	4)	A45A	15)	*
	5)	9AC0	14)	09AH
	6)	8H9C	13)	3F8C
	7)	AHF3	12)	AFIP
	8)	3P5C	11)	7C2F
	9)	6PCP	10)	8U70
U44:	1)	0000	18)	0000
	2)	*	17)	*
	3)	*	16)	9AC0
	4)	A45A	15)	*
	5)	9AC0	14)	09AH
	6)	8H9C	13)	3F8C
	7)	AHF3	12)	AFIP
	8)	3P5C	11)	7C2F
	9)	6PCP	10)	8U70
U31:	1)	0000	18)	0000
	2)	*	17)	*
	3)	*	16)	9AC0
	4)	A45A	15)	*
	5)	9AC0	14)	09AH
	6)	8H9C	13)	3F8C
	7)	AHF3	12)	AFIP
	8)	3P5C	11)	7C2F
	9)	6PCP	10)	8U70
U30:	1)	0000	18)	0000
	2)	*	17)	*
	3)	*	16)	9AC0
	4)	A45A	15)	*
	5)	9AC0	14)	09AH
	6)	8H9C	13)	3F8C
	7)	AH53	12)	AFIP
	8)	3P5C	11)	7C2F
	9)	6PCP	10)	8U70
U29:	1)	U40P	14)	6PCP
	2)	U40P	13)	6PCP
	3)	U40P	12)	6PCP
	4)	A45A	11)	6PCP
	5)	A45A	10)	6PCP
	6)	A45A	9)	6PCP
	7)	0000	8)	6PCP

HSP-MMU (cont.)
Setup: Same as WCS except Clock: AS2/ ¬_

U54:	1)	0000	40)	A70F
	2)	0000	39)	3CPF
	3)	09AH	38)	91FC
	4)	8H9C	37)	5A34
	5)	3F8C	36)	U97F
	6)	AHF3	35)	1F8F
	7)	AF1P	34)	2595
	8)	3P5C	33)	3959
	9)	7C2F	32)	5P4A
	10)	8U70	31)	C2CA
	11)	0000	30)	C2CA
	12)	A70F	29)	5PCC
	13)	6PCP	28)	44P2
	14)	0000	27)	APUU
	15)	6PCP	26)	U8H9
	16)	0000	25)	F170
	17)	0000	24)	CF94
	18)	PP3F	23)	6575
	19)	3A06	22)	6575
	20)	0PC4	21)	6PCP

U64:	1)	6PCP	16)	6PCP
	2)	3CPF	15)	*
	3)	A70F	14)	U25P
	4)	0000	13)	FC0U
	5)	0000	12)	*
	6)	0000	11)	*
	7)	6PCP	10)	6PCP
	8)	0000	9)	6PCP

U42:	1)	6PCP	14)	6PCP
	2)	6PCP	13)	U40P
	3)	U40P	12)	9AC0
	4)	6PCP	11)	6PCP
	5)	6PCP	10)	6PCP
	6)	9AC0	9)	6PCP
	7)	0000	8)	0000

U43:	1)	-	14)	6PCP
	2)	-	13)	9AC0
	3)	5P4A	12)	U40P
	4)	30U4	11)	6PCP
	5)	-	10)	0000
	6)	-	9)	6PCP
	7)	0000	8)	0000

6

Parts Lists

The following parts lists are contained in this section in the order listed:

Motherboard

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-04337	1	MANUAL,OWNER'S,M70	
070-04577	1	MANUAL,OWNER'S,ADD,V1.20,M70	
CABLES/CORDS			
680-00841	1	CORD,POWER,PHILLIP #13E37-1	
POTENTIOMETERS			
200-03771	1	POT,RTY,PC,10K-A,6MMX.79",FLAT	R71
TRIM RESISTORS			
201-00159	3	RES,TRM,ST,PC,100K,SA,CER	R10,36,86
201-00430	1	RES,TRM,ST,PC,2K,SA,CER	R160
201-01619	1	RES,TRM,ST,PC,500 OHM,SA,CER	R131
201-04311	1	RES,TRM,ST,PC,100K OHM,SA,1/4"	R158
CARBON FLM RES			
202-00504	3	RES,CF,5%,1/4W,5.1 OHM	R7,29,80
202-00508	2	RES,CF,5%,1/4W,33 OHM	R5,28
202-00510	5	RES,CF,5%,1/4W,51 OHM	R13,43,89,102,107
202-00514	1	RES,CF,5%,1/4W,100 OHM	R83
202-00518	6	RES,CF,5%,1/4W,220 OHM	R110,111,118,119,122,143
202-00523	1	RES,CF,5%,1/4W,390 OHM	R125
202-00529	9	RES,CF,5%,1/4W,1K OHM	R78,106,114,116,121,123,124 R126,136
202-00532	3	RES,CF,5%,1/4W,1.8K OHM	R127,130,132
202-00533	2	RES,CF,5%,1/4W,2K OHM	R54,97
202-00534	6	RES,CF,5%,1/4W,2.2K OHM	R92,93,112,120,128,129
202-00537	2	RES,CF,5%,1/4W,3K OHM	R58,62
202-00538	13	RES,CF,5%,1/4W,3.3K OHM	R11,41,52,87,98,108,109,117 R135,140,141,R154,155
202-00543	5	RES,CF,5%,1/4W,5.1K OHM	R9,23,30,85,144
202-00546	1	RES,CF,5%,1/4W,7.5K OHM	R96
202-00549	6	RES,CF,5%,1/4W,10K OHM	R6,21,33,57,79,145
202-00553	4	RES,CF,5%,1/4W,15K OHM	R61,90,95,105
202-00555	13	RES,CF,5%,1/4W,20K OHM	R3,14,34,44,51,59,72-75,77,81 R147
202-00559	3	RES,CF,5%,1/4W,30K OHM	R32,60,76
202-00562	2	RES,CF,5%,1/4W,39K OHM	R138,139
202-00564	3	RES,CF,5%,1/4W,51K OHM	R20,113,115
202-00570	12	RES,CF,5%,1/4W,100K OHM	R19,24,82,134,148-153,156,157
202-00579	7	RES,CF,5%,1/4W,470K OHM	R1,2,12,25,26,42,88
202-00581	1	RES,CF,5%,1/4W,10M OHM	R22
202-01159	1	RES,CF,5%,1/4W,18K OHM	R133
202-01228	5	RES,CF,5%,1/4W,620 OHM	R4,27,53,99,100
202-01497	1	RES,CF,5%,1/4W,2M OHM	R137
202-02649	2	RES,CF,5%,1/4W,300 OHM	R91,94

Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
METAL FLM RES			
203-00457	2	RES,MF,1%,1/8W,1.50K OHM	R15,17
203-00459	3	RES,MF,1%,1/8W,2.00K OHM	R55,56,68
203-00465	1	RES,MF,1%,1/8W,6.49K OHM	R146
203-00471	4	RES,MF,1%,1/8W,10.0K OHM	R45,46,49,50
203-01145	1	RES,MF,1%,1/8W,1.24M OHM	R159
203-01251	2	RES,MF,1%,1/8W,8.06K OHM	R47,48
203-02352	2	RES,MF,1%,1/8W,24.9K OHM	R8,31
203-02610	1	RES,MF,1%,1/8W,1.65K OHM	R67
203-02611	2	RES,MF,1%,1/8W,5.62K OHM	R16,18
NETWORK RES			
205-03531	3	RES,NET,SIP,2%,10KX5	RP1-3
ELECTROLYT CAP			
240-00608	1	CAP,ELEC,2.2uF,50V,RAD	C159
240-00613	7	CAP,ELEC,22uF,25V,RAD	C18,24,25,33,34,116,117
240-00614	7	CAP,ELEC,47uF,16V,RAD	C8,23,32,44,56,65,68
240-01262	1	CAP,ELEC,330uF,25V,RAD	C136
240-03574	2	CAP,ELEC,3300uF,35V,RAD,LO-PRO	C143,153
240-03901	2	CAP,ELEC,1000uF,35V,RAD,LO-PRO	C118,125
240-04277	2	CAP,ELEC,330uF,50V,RAD	C147,149
TANTALUM CAP			
241-00651	1	CAP,TANT,.22uF,35V,RAD	C42
241-00652	1	CAP,TANT,4.7uF,25V,RAD	C71
241-00655	4	CAP,TANT,22uF,25V,RAD	C7,20,50,51
PCRB/PP CAP			
244-00660	10	CAP,MYL,.01uF,100V,10%,RAD	C4,9,46,52,53,57,81,93,94,102
244-01169	1	CAP,PP,2200pF,2.5%	C139
244-01171	2	CAP,PP,5100pF,2.5%	C27,28
244-01172	1	CAP,PP,6800pF,2.5%	C137
244-02104	2	CAP,PP,100pF,160V,2.5%,AX	C26,29
244-02342	1	CAP,MYL,.68uF,50V,10%,RAD	C138
244-02486	3	CAP,PP,510pF,160V,2.5%,AX	C30,31,36
244-03919	1	CAP,MYL,.015uF,250V,INTL APP	C160
CERAMIC CAP			
245-00596	2	CAP,CER,.005uF,1.6KV,Z5U	C150,156
245-03609	77	CAP,CER,.1uF,50V,Z5U,AX	C2,3,6,11,12,17,37-39,47,49,54 C55,63,66,69,70,72,76,79,80 C82-92,95-101,103-112,114,115 C119-124,126-130,132-135,140 C141,144,146,148,151,152,154 C155,157,158

Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
CERAMIC CAP			
245-03610	2	CAP,CER,.01uF,50V,Z5U,AX	C161,162
245-03867	6	CAP,CER,10pF,100V,COG,10%,AX	C5,10,13,14,48,163
245-03868	9	CAP,CER,33pF,100V,COG,10%,AX	C19,40,41,61,64,67,77,113,165
245-03869	6	CAP,CER,100pF,100V,COG,10%,AX	C35,73,74,142,145,164
245-03870	5	CAP,CER,150pF,100V,COG,10%,AX	C1,15,16,58,59
245-03871	1	CAP,CER,1000pF,100V,X7R,10%,AX	C131
INDUCTORS			
270-00779	5	FERRITE,BEAD	FB1-5
270-03899	1	INDUCTOR,2.2mH,LINE CHOKE	L2
270-04278	1	INDUCTOR,375uH,2A,SWITCHING	L1
DIODES			
300-01024	1	DIODE,1N746	CR37
300-01026	2	DIODE,1N753	CR39,56
300-01029	21	DIODE,1N914 AND 4148	CR1-3,14-19,26-31,35,36,40,41 CR43,55
300-01030	6	DIODE,1N4004 AND 4005	CR32-34,38,48,49
300-01154	1	DIODE,1N751,ZENER,5.1V	CR9
300-02401	14	DIODE,BAR 35,SCHOTTKY,LOW VF	CR10-13,20,21,44-46,50,51,53 CR54,57
300-03498	1	DIODE,SCHOTTKEY,POWER,3A	CR47
300-03546	2	DIODE,BRIDGE,2A,200V	CR42,52
TRANSISTORS			
310-01007	2	TRANSISTOR,2N3904	Q2,8
310-01008	3	TRANSISTOR,2N3906	Q5,9,11
310-01647	2	TRANSISTOR,2N4401	Q6,7
310-03920	1	TRANSISTOR,2N5245	Q4
310-04289	2	TRANSISTOR,J105/J108	Q1,3
SCR			
320-04038	1	TRANSISTOR,C122F1,SCR,BENT	Q10
DIGITAL/CMOS IC			
330-01290	1	IC,DIGITAL,74LS244	U100
330-03586	4	IC,DIGITAL,74HCT244	U69,85,94,98
330-03715	6	IC,DIGITAL,74HCT374	U56,61,66,78,81,89
330-03766	1	IC,DIGITAL,MMU,64K,CMOS	U54
330-03768	1	IC,DIGITAL,CMU,16 BITS,CMOS	U20
330-04040	2	IC,DIGITAL,74F04	U36,43
330-04041	1	IC,DIGITAL,74F10	U42
330-04042	4	IC,DIGITAL,74AHCT374	U55,57,58,76
330-04260	2	IC,DIGITAL,74HCT04	U21,70
330-04261	2	IC,DIGITAL,74HCT00	U26,79
330-04262	1	IC,DIGITAL,74F00	U73
330-04271	4	IC,DIGITAL,74HCT273	U27,38,39,51
330-04272	2	IC,DIGITAL,74HCT163	U60,64

Motherboard (continued)

PART NO.	QTY/DESCRIPTION		REF.
DIGITAL/CMOS IC			
330-04273	2	IC,DIGITAL,74HCT74	U68,101
330-04274	1	IC,DIGITAL,74HCT132	U102
330-04275	1	IC,DIGITAL,74HCT139	U90
330-04292	2	IC,DIGITAL,74F32	U29,65
330-04293	1	IC,DIGITAL,74F74	U83
330-04294	3	IC,DIGITAL,74HCT138	U59,71,80
330-04336	2	IC,DIGITAL,74ALS244	U87,93
330-04362	1	IC,DIGITAL,ARU,18 BIT,CMOS,15M	U25
330-04435	3	IC,DIGITAL,74ALS374	U34,35,37
330-04511	1	IC,DIGITAL,74AHCT244	U74
LINEAR IC			
340-01183	2	IC,LINEAR,LF 356	U5,11
340-01363	1	IC,LINEAR,LM339	U103
340-01566	3	IC,LINEAR,LF353,DUAL OP AMP	U6,9,24
340-02674	1	IC,LINEAR,CMP-05FZ	U16
340-03119	3	IC,LINEAR,DBX 2150A,VCA	U2,13,14
340-03630	1	IC,LINEAR,LM3915	U7
340-03858	2	IC,LINEAR,RC4560NB	U1,12
340-04036	1	IC,LINEAR,7815(LM340T-15),BENT	U72
340-04037	1	IC,LINEAR,7915(LM320T-15),BENT	U92
340-04168	1	IC,SWCHINGREG LAS6320P	U99
340-04433	3	IC,LINEAR,LM833	U8,17,19
INTERFACE IC			
345-02913	4	IC,INTER,NE594,DSP DRVR,8-SEG	U28,40,41,52
SS SW IC			
346-02677	1	IC,SS SWITCH,DG211	U10
346-03329	1	IC,SS SWITCH,SD5000N	U4
MEMORY IC			
350-03493	1	IC,ROM,82S123,M200,DIG	U49
350-04280	4	IC,SRAM,2148,1KX4,45NS	U75,77,84,86
350-04281	1	IC,SRAM,SRM2016,2KX8,250NS,LPS	U96
350-04282	1	IC,SRAM,4364,8KX8,250NS,LPS	U91
350-04428	1	IC,ROM,27256,M70,V1.20-1	U62
350-04429	1	IC,ROM,27128,M70,V1.20-2	U95
350-04430	1	IC,ROM,2764,M70,V1.20-3	U67
350-04354	1	IC,ROM,74S472,M70	U48
350-04434	4	IC,DRAM,64KX4,120NS	U30,31,44,45
CONVERTER IC			
355-03124	1	DAC,PCM53JG-I	U15
355-04170	1	DAC,AD7528	U22
355-04283	1	IC,CONV,ADC0804	U23

Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
SEMICONDUCTORS			
360-01612	2	SEMICOND,VARISTOR	VR1,2
MICROPROC IC			
365-03526	1	IC,uPROC,CDP1854 or IM6402	U97
365-04284	2	IC,uPROC,Z80,CMOS,4MHz	U82,88
OPTO ISLTOR IC			
375-02247	1	IC,OPTO-ISOLATOR,6N 138	U63
MODULES			
380-03956	1	MOD,DLY LINE,5 TAP,30/150NS,LS	U53
380-04187	3	MOD,LPF,9P,15.25KHz	LPF1-3
CRYSTALS			
390-04290	1	CRYSTAL OSC,13.000 MHz	U50
DSPLY/IND/LED			
430-03896	3	LED,GRN,RECT,S197X/079	CR6-8
430-03897	1	LED,YEL,RECT,.197X.079	CR5
430-03898	1	LED,RED,RECT,.197X.079	CR4
430-04169	1	DISPLAY,NEC FIP16A5R	DS1
SLIDE SWITCH			
451-02230	1	SW,SL,2P2T,V-CHNG,PC,4A	SW3
PSH BUT SWITCH			
453-03993	2	SW,PBPP,2P2T,PCRA,2.5MM TRAV	SW1,2
BATTERIES			
460-04285	1	BAT,LITH,3V@160mAh,VERT COIN	BT1
CABLE CONN			
490-02356	2	CONN,JUMPER,.1X025,2FCG	W8,12(2-3)
PC MNT CONN			
510-02106	5	1/4" PHONE JACK,PCRA,3C,SWITCH	J1-3,5,6
510-02671	2	CONN,POST,100X025,HDR,3MC,GOLD	W8,12
510-03922	2	CONN,POST,100X025,HDR,6MCG	TP21,24
510-04286	3	CONN,CIRC DIN,5FC@180DEG,PCRA	J7-9
SOCKETS			
520-00943	3	IC SCKT,16 PIN,PC,LO-PRO	U4,10,49
520-00945	1	IC SCKT,24 PIN,PC,LO-PRO	U15
520-00946	6	IC SCKT,40 PIN,PC,LO-PRO	U20,25,54,82,88,97
520-01361	3	IC SCKT,20 PIN,PC,LO-PRO	U22,23,48
520-01458	5	IC SCKT,28 PIN,PC,LO-PRO	U62,67,91,95,96
520-02177	8	IC SCKT,18 PIN,PC,LO-PRO	U30,31,44,45,75,77,84,86
STRAIN REL			
530-02488	2	TIE,CABLE,NYL,.14"X5 5/8"	L1 MTG

Motherboard (continued)

PART NO.	QTY	DESCRIPTION	REF.
ELECTRONIC HDWR			
600-00871	2	FUSE CLIP,1/4",PC	F1
INSUL/SPACRS			
630-00952	3	INSUL,SEMI,BUSHING,TO-220	Q10,U72,U92 MTG
630-01853	3	INSUL,SEMI,SIL RUB,TO-220	Q10,U72,U92 MTG
630-02740	5	SPCR,#4CLX.21,3/16 RD,NYL	CR4-8
SPCR,NON-INSUL			
635-03633	4	SPCR,SWAGE,#6CLX.17,1/4RD,BR/N	PC BD MTG
THRD-FORM SCRW			
641-04021	3	SCRW,TAP,SW,4-40X1/4,PNH,PH,ZN	Q10,U72,U92 MTG
THREADLS FASTNR			
650-03970	2	POPRVT,1/8X1/8,REG PROT HD,SS	HEATSINK TO MOTHERBOARD MTG
BULK WIRE			
670-01768	1	WIRE,JMP,22AWG,0.5",TEF,WHT	W4
670-01974	4	WIRE,JMP,22AWG,0.1",NON-INSUL	W3,6,13,14
670-03962	1	CABLE,RIB,28AWG,7CX.1",6.2"	P1
BRACKETS			
701-04162	1	BRACKET,HEATSINK,M70	
PLASTICS			
720-03571	0	TAPE,KAPTON,1/2"	L1,1" PIECE

Front Panel Board

PART NO.	QTY	DESCRIPTION	REF.
CARBON FLM RES			
202-00521	4	RES,CF,5%,1/4W,330 OHM	R3-6
ROTARY SWITCH			
452-04233	1	SW,RTY,INC ENCODER,50 POS	SW1
PSH BUT SWITCH			
453-04236	12	SW,PBM,1P1T,TR1-01	SW2-7,10-15
453-04237	3	SW,PBM,1P1T,TR3-01-L5,GRN-LED	SW8,9,16
453-04335	1	SW,PBM,1P1T,TR3,-01-L2,RED-LED	SW17
KNOBS/CAPS			
550-04240	1	BUTTON,BLK,.5SQ,"0",WHT	SW3

Front Panel Board (continued)

PART NO.	QTY	DESCRIPTION	REF.
KNOBS/CAPS			
550-04241	1	BUTTON,BLK,.5SQ,"1",WHT	SW4
550-04242	1	BUTTON,BLK,.5SQ,"2",WHT	SW5
550-04243	1	BUTTON,BLK,.5SQ,"3",WHT	SW6
550-04244	1	BUTTON,BLK,.5SQ,"4",WHT	SW7
550-04245	1	BUTTON,BLK,.5SQ,"5",WHT	SW11
550-04246	1	BUTTON,BLK,.5SQ,"6",WHT	SW12
550-04247	1	BUTTON,BLK,.5SQ,"7",WHT	SW13
550-04248	1	BUTTON,BLK,.5SQ,"8",WHT	SW14
550-04249	1	BUTTON,BLK,.5SQ,"9",WHT	SW15
550-04250	1	BUTTON,BLK,.5SQ,DOWN ARROW,WHT	SW10
550-04251	1	BUTTON,BLK,.5SQ,UP ARROW,WHT	SW2
550-04252	1	BUTTON,BLK,.5SQ,"PGM",WHT	SW8
550-04253	1	BUTTON,BLK,.5SQ,"REG",WHT	SW16
550-04254	1	BUTTON,BLK,.5SQ,"BYP",WHT	SW17
550-04255	1	BUTTON,BLK,.5SQ,"LOAD",WHT	SW9
SPCR,NON-INSUL			
635-04341	3	SPCR,SWAGE,#6CLX.187,1/4RD/BR	
THREADLS FASTNR			
650-03970	2	POPRVT,1/8X1/8,REG PROT HD,SS	
BULK WIRE			
670-01844	3	WIRE,JMP,24AWG,BUSS WIRE	RTY ENCODER - P5 CONN NEED (3) 1/2" LENGTHS
670-03962	3	CABLE,RIB,28AWG,7CX.1",6.2"	P2-4
CHASSIS/MECH			
700-00163	2	BRACKET,KEYSTONE #612	

Front Panel Board (continued)

PART NO.	QTY	DESCRIPTION	REF.
MACHINE SCREWS			
640-02736	4	SCRW,8-32X3/8,BH,SCKT,BLK	FP MTG
640-02812	8	SCRW,4-40X3/8,PNH,PH,BLK	J7-9 MTG (6), J10 MTG (2)
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	MOTHERBD TO CHASSIS MTG
640-03957	7	SCRW,6-32X3/16,TH,PH,BLK	TOP & BOTTOM COVER MTG
640-03977	4	SCRW,6-32X1/2,TH,PH,HDR PT,BLK	TOP & BOTTOM COVER MTG
640-04339	4	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	FP PCB TO MTHBD MTG (2), LED BD MTG (2)
NUTS			
643-01728	4	NUT,6-32,KEP,ZN	TRANSFORMER MTG
643-01732	10	NUT,4-40,KEP,ZN	J7-9 MTG (6), J10 MTG (2),
WASHERS			
644-01253	5	WSHR,INT STAR,3/8CLX.500DX.022	J1-3,5,6 MTG
644-04028	1	WSHR,FL,.160IDX.437ODX.063THK	GROUND LUG MTG
THREADLS FASTNR			
650-03982	5	POPRVT,5/32X1/4,120DEG FLAT HD	XFORMER MTG (2), HEATSINK B
PRE-CUT WIRE			
675-02852	1	WIRE,16G,GRN,4",ST1/4XST&T1/4	AC CONN WIRES J10
675-04348	2	WIRE,18G,BLK,8.5",QDCX.175ST&T	PWR SWITCH WIRES SW4
675-04349	1	WIRE,18G,BLK,1.5",ST&T3/16X3/8	AC CONN WIRES J10
675-04350	1	WIRE,18G,WHT,1.5",ST&T3/16X3/8	AC CONN WIRES J10
675-04351	1	TWST PR,RED/BLK,21.5",ST&T	E1-E7, E2-E8
SLEEVING			
690-02060	3	SLEEVING,SHRINK,3/16"	J10 (1/2" LENGTHS)
690-02061	10	SLEEVING,SHRINK,1/8"	XFORMER(1), CR58(1), CR59-6
CHASSIS/MECH			
700-04137	1	COVER,TOP,M70	
700-04138	1	COVER,BOTTOM,M70	
700-04151	1	CHASSIS,WRAPAROUND,M70	
700-04152	1	CHASSIS,INSERT,FP,M70	
BRACKETS			
701-04316	1	BRACKET,SUPPORT,XFORMER,M70	
PANELS			
702-04206	1	PANEL,OVERLAY,FP,M70	
702-04207	1	PANEL,OVERLAY,CHASSIS,M70	
702-04208	1	COVER,PROTECTIVE,MOTHERBD,M70	
702-04209	1	PANEL,FRONT,M70	
702-04257	1	COVER,PROTECTIVE,AC,M70	
LENS/PLATE/PANL			
703-04205	1	LENS,DISPLAY,M70,.740X3.790	
PLASTICS			
720-03571	0	TAPE,KAPTON,1/2"	
720-04355	10	TAPE,POLYETHYLENE,3/16,3M#5421	FIP MTG

Mechanical

PART NO.	QTY	DESCRIPTION	REF.
DIODES			
300-01024	1	DIODE,1N746	E7 (HV) CR58
300-01029	4	DIODE,1N914 AND 4148	CR59-62
ROCKER SWITCH			
454-03900	1	SW,ROCKER,1P1T,QDC,INTL LINE	SW4
TRANSFORMERS			
470-04315	1	XFORMER,POWER,UI,M70	T1
SOCKETS			
520-00798	1	CONN,AC,SWCT #EAC 309	J10
STRAIN REL			
530-02489	3	TIE,CABLE,NYL,.1"X4"	TRANSFORMER WIRES
GROMMETS			
540-00874	2	GROMMET,9/16 OD,7/16 ID	BRACKET SUPPORT
FEET			
541-00781	4	BUMPER,FEET,3-M #SJ5025	
KNOBS/CAPS			
550-03827	2	BUTTON,.346RD,BLK	SW1,2
550-03926	1	KNOB,.66,6MM/FLAT,BLK/WHT LINE	R71
550-04212	1	KNOB,1.00,6MM/ROUND,BLK	SOFTKNOB
ELECTRONIC HDWR			
600-04352	1	FLAT SPRING CLAMP,2X5/16	FIP CLIP
PC HDWR			
610-02269	3	HARDWARE,PC,RICHCO #MB-3-156	PROT COVER MTG
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,#6,.020THK	TRANSFORMER GROUND
620-04007	1	LUG,SOLDER,LCKING,#8	POWER CORD GND
INSUL/SPACRS			
630-02737	4	WSHR,FL,#8CLX.02TH,BLK,NYL	FP MTG
630-03955	7	WSHR,SHLDR,3/16SHNK,#6CL,FBR	TRANSFORMER MTG
SPCR,NON-INSUL			
635-04340	1	SPCR,4-40X7/8,3/16HEX,BR/N	FRONT PANEL PCB MTG
635-04353	1	SPCR,#4CLX.187,1/4RD,BR/N	FIP CLIP MTG

100/120V Fuse Option

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-00860	1	FUSE,3AG,SLO-BLO,.250 AMP	F1
INSUL/SPACRS			
630-03969	1	INSUL,COVER,AGC,FUSE	F1

220/240V Fuse Option

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-03486	1	FUSE,3AG,SLO-BLO,.125AMP,250V	F1
INSUL/SPACRS			
630-03969	1	INSUL,COVER,AGC,FUSE	F1

8

Backdating This Service Packet

This section contains information necessary to backdate this packet to make it conform with earlier product configurations.

- To identify the configuration of a particular PCM 70, refer to the revision letter printed on a label on the bottom of the main board.
- To backdate this service packet, reverse the changes in descending order (by change number) ending with the change number under the revision letter that matches the unit's.

	Revision Level					
Assembly Name	-	A	B	C	D	E
PCM 70 Main Board	•	1	2	3	4	X

Key:

X = The revision level documented in this Service Packet
• = A revision level that was never used in this unit

Table 8-1. Manual Status and Backdate Information

Unless otherwise noted, these changes should be applied to the parts lists in Chapter 6 and the schematics and assembly drawings in Chapter 7. The specific material affected is easily determined by the type of change.

Newer Units

If and when changes and improvements are made to the PCM 70, they are identified by incrementing the revision letter marked on all units. These changes are documented in the following chapter, and/or on a supplemental change sheet included with the packet.

Change #1

Delete CR58

300-01024 - Diode, 1N746 - CR58
690-02061 - Sleeving, Shrink, 1/2"

The location for CR58 is shown in Schematic 060-04146 (Motherboard, Sheet 10 of 10) and Chassis Assembly Drawing 080-04356 (Sheet 5 of 5).

Change #2

Delete CR59, CR60, CR61, CR62

300-01029 diode, 1N914 & 4148

CR59, CR60, CR61, and CR62 are located as shown in Field Bulletin 070-04664.

Change U62, U67, U95

FROM: 520-01458 - IC, SCKT, 28 Pin, PC, Lo-Pro
TO: 520-04276 - IC, SCKT, 28 Pin, PC, ZIF

Change #3

Change Motherboard

FROM: Rev. 2
TO: Rev. 1

Change U8, U17, U19

FROM: 340-04433 - IC, LINEAR, LM833 - U8, U17, U19
TO: 340-01566 - IC, LINEAR, LF353, - U17
TO: 340-03858 - IC, LINEAR, RC4560NB - U8, U19

Change #4

Delete Kapton Tape

720-03571 - Tape, Kapton, 1/2", on motherboard under L1

9

Updates and Improvements

This chapter provides a brief description of updates and improvements for the PCM 70. It is provided for information only, and is not intended to serve as instructions for updating a unit.

Revision B

Add CR58

Purpose of Change: ECO # 85-1107-00 - Reduce FIP intensity to prevent the possibility of image burn-in.

300-01024 - Diode, 1N746 - CR58
690-02061 - Sleeving, Shrink, 1/2"

Install as shown in Schematic 060-04146 (Motherboard, Sheet 10 of 10) and Chassis Assembly Drawing 080-04356 (Sheet 5 of 5).

Revision C

Add CR59, CR60, CR61, CR62

Purpose of Change: ECO # 851219-00 - Add static protection to muting transistors Q1 and Q3.

300-01029 diode, 1N914 & 4148

Install as described in Field Bulletin 070-04664.

Change U62, U67, U95

Purpose of Change: Replace ZIF sockets with standard low-profile sockets.

FROM:	520-04276 - IC, SCKT, 28 Pin, PC, ZIF
TO:	520-01458 - IC, SCKT, 28 Pin, PC, Lo-Pro

Revision D

Change Motherboard

FROM: Rev. 1
TO: Rev. 2

Change U8, U17, U19

ECO # 850925-00

FROM: 340-01566 - IC, LINEAR, LF353, - U17
FROM: 340-03858 - IC, LINEAR, RC4560NB - U8, U19
TO: 340-04433 - IC, LINEAR, LM833 - U8, U17, U19

Revision E

Add Kapton Tape

Purpose: ECO # 851219-00 - To prevent possibility of switching transformer shorting to PC board.

720-03571 - Tape, Kapton, 1/2", to motherboard under L1

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Field Bulletin

Lexicon Inc. 60 Turner Street Waltham, MA 02154 617-891-6790 Telex 923 468

PCM 70 Version 1.2 Software Update

To improve the operational performance of the PCM 70, software Version 1.2 has been developed. This software is factory installed in all units from serial number 1659 on. Update kits are being shipped to all dealers free of charge for installation in units with earlier serial numbers. **Software Version 1.2 incorporates the following improvements:**

- Faster program to program changes.
- A bug in the Concert Hall programs that causes overload with certain parameter settings has been corrected.
- Parameter settings of the following programs have been improved to make use of more accurate delay times and to set all master controls to zero:

  0.0 CHORUS
  0.3 STEREO FLANGE
  0.7 PSYCHO ECHOES
  0.8 ECHOES BPM
  0.9 CHORUS AND ECHO BPM
  1.1 DOUBLE DELAY
  1.3 CIRCULAR DELAYS
  1.8 BOUNCING BPM
  6.0 MIDI ECHO BPM
  6.1 CASCADE BPM

- The DIFFUSION parameter in the **Chorus and Echo** and **Multiband Delay** families of programs adds between 4 and 20 ms to the selected delay time, resulting in an inaccurate delay time display.

  Effective with version 1.2 of the PCM 70 operating software, when DIFFUSION is set to 0, the delay times shown in the display window are accurate. In applications which require precise delay time settings or relatively short delay times (as in chorusing and flanging effects) DIFFUSION should always be set to 0.

070-04662 1/86

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PCM 70 Zero Insertion Force (ZIF) Sockets

The PCM 70 is equipped with three 28-pin ZIF sockets, designed to facilitate rapid software changes. It has been determined that a few of these sockets have unreliable contacts, causing one or more of the following effects:

- Unusable front panel controls (bad U62 socket)
- "SLAVE DEAD READ ERROR" (bad U95 socket)
- High noise level in some programs (bad U67 socket)

Not all units with ZIF sockets will exhibit these problems.

To Make Repairs

( ) 1. Before you do anything else, read through the following instructions.

( ) 2. Select a clean, static free, well-lighted area in which to work.

( ) 3. Turn off the PCM 70 and disconnect the power cord from the back of the unit.

( ) 4. Remove the top and bottom covers. Note that there are two different sizes of screws present in your unit. These must be returned to their original locations when the unit is closed up.

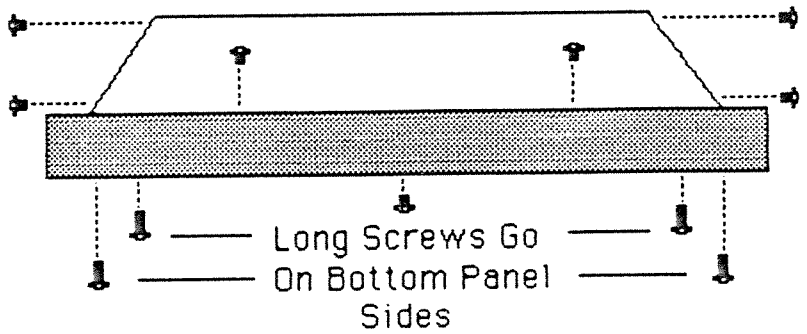

Figure 1. Screw Locations.

( ) 5. Locate the ZIF sockets and release the lever on each one. Reseat the IC in each socket and relock the lever.

( ) 6. Turn on the PCM 70 and recheck it. If it still misbehaves, clear memory as described in the *Solving Problems* chapter of the *PCM 70 Owner's Manual.* (Note that this will erase all user registers.) If clearing memory fails to resolve the problem, call Lexicon Customer Service at (617) 891-6790.

To eliminate the possibility of these problems occuring in current production units we have replaced the ZIF sockets with standard low profile sockets (Lexicon Part # 520-01458). Low profile sockets are factory installed in all units from serial number 70-1807 on. Units with earlier serial numbers have ZIF sockets. If they exhibit any of the above problems, they should be returned to Lexicon for replacement with low-profile sockets.

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PCM 70 Power Up/Down Mute Field Effect Transistors

It has been determined that if static electricity contacts the tip connection of a PCM 70 output jack, it can destroy a FET (which is designed to mute the outputs when power to the unit is turned on or off). This can result in no output from left, right, or both output channels.

To eliminate this possibility we have added four diodes to protect the FETs against large transient voltages such as those caused by static discharge. The diodes are factory installed in all units from serial number 70-1807 on. Units with earlier serial numbers do not have the diodes, and should have them retrofitted.

Installing the Protection Diodes

( ) 1. Before you do anything else, read through the following instructions.

( ) 2. Select a clean, static free, well-lighted area in which to work.

( ) 3. Turn off the PCM 70 and disconnect the power cord from the back of the unit.

( ) 4. Remove the top and bottom covers. Note that there are two different sizes of screws present in your unit. These must be returned to their original locations when the unit is closed up.

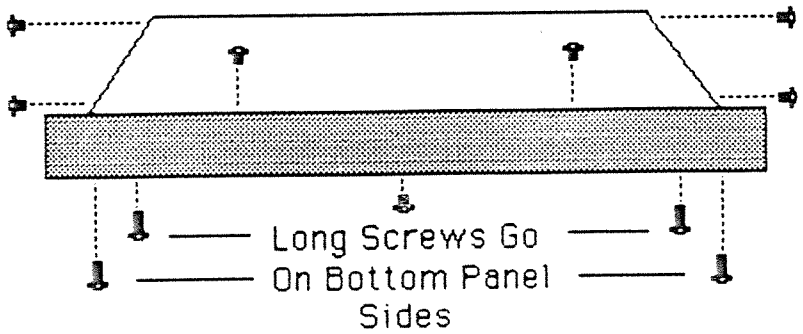
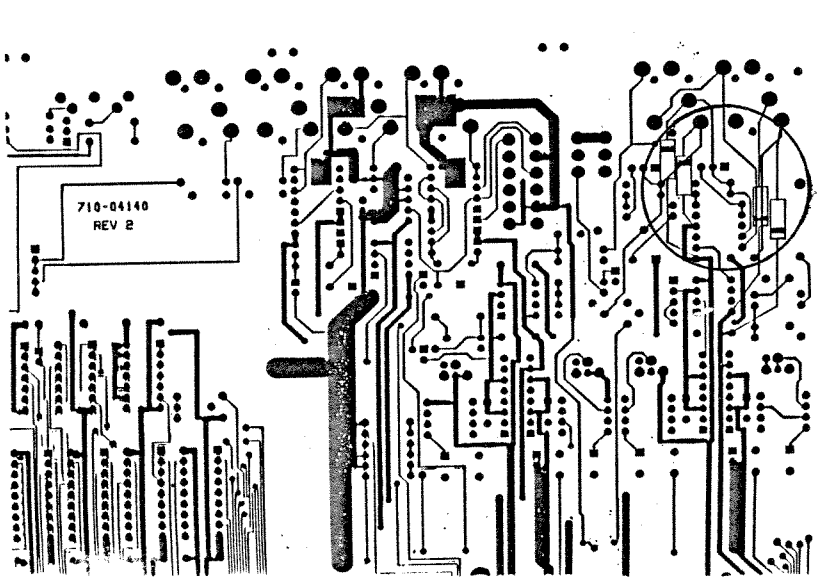


Figure 1. Screw Locations.

( ) 5. Locate the solder side of the main board near the output jacks and refer to Figure 2 for installation locations for the four diodes (IN4148, Lexicon Part # 300-01029). Place teflon sleeving over the diode leads to prevent shorting.

( ) 6. If one or both of the FETs are blown (no output), replace them (Lexicon Part # 310-04289, J105/J108).



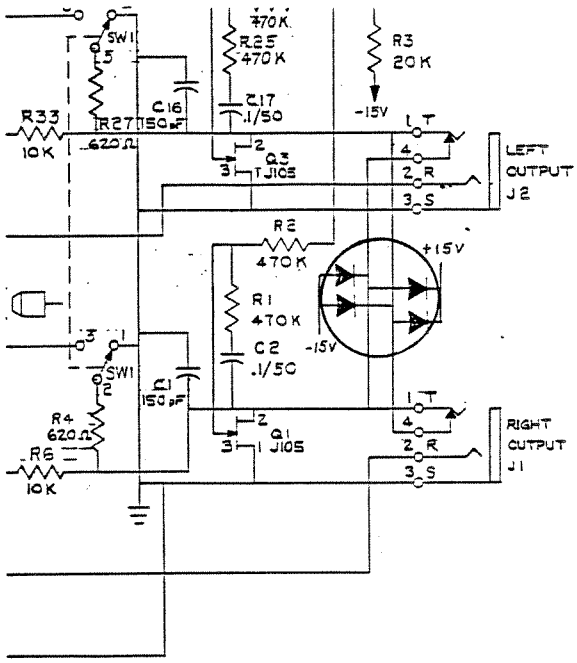


Figure 2. Locations for diodes.

( ) 7. Turn on the PCM 70 and check for output. If the PCM 70 still exhibits problems, check all external connections and level settings. If this fails to identify the problem, call Lexicon Customer Service at (617) 891-6790.

Temporary Emergency Field Repairs

In a field emergency, output can be temporarily restored by removing the blown FET(s)--Q1 for the right channel and Q3 for the left channel. If output returns with Q1 or Q3 removed the unit may be used, but caution should be exercised when turning the unit on or off. The outputs are no longer muted and damage to your monitoring system could result. The defective parts should be replaced as soon as possible.