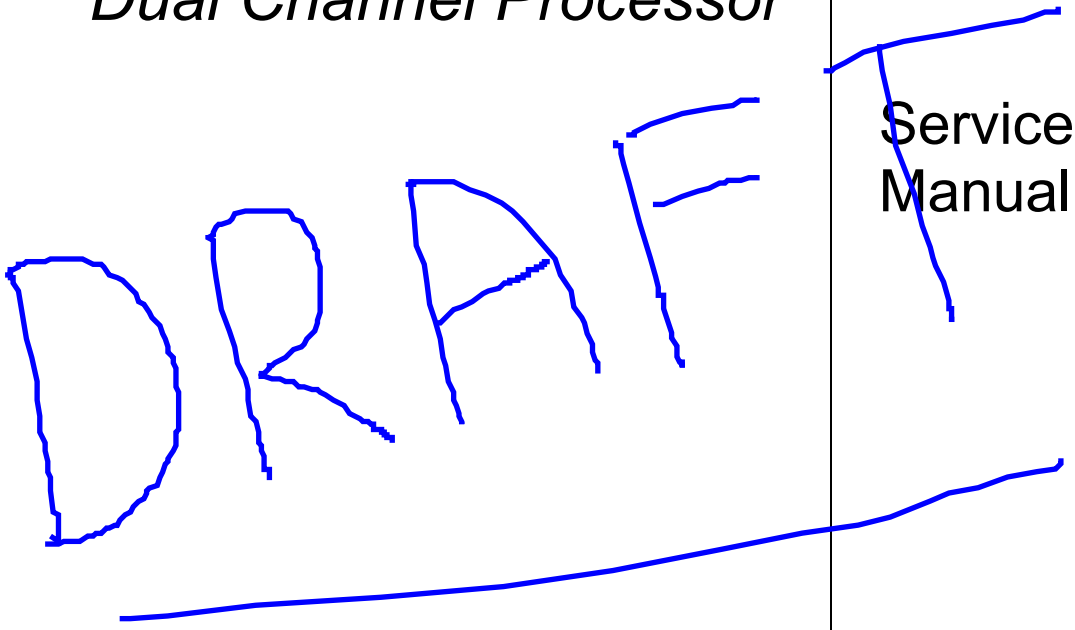
MPX 200

24-Bit

Dual Channel Processor

Service Manual



lexicon

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturers operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

 This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure… voltage that may be sufficient to constitute a risk of shock.

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

 This triangle, which appears on your component, alerts you to important operating and maintenance Instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems.

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

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Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.
*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when: the power supply cord or the plug has been damaged, objects have fallen, or liquid has been spilled into the unit, the unit has been exposed to rain, the unit does not appear to operate normally or exhibits a marked change in performance, the unit has been dropped, or the enclosure damaged.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

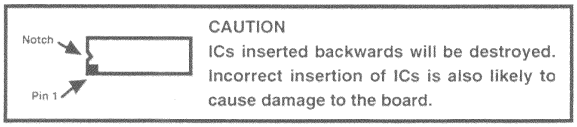
Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.

Table of Contents

Chapter 1 Reference Documents, Required Equipment

Reference Documents

MPX 200 Owner's Manual - Lexicon P/N 070-14738 or latest revision

Required Equipment

Tools

The following is a *minimum* suggested technician's tool kit required for performing disassembly, assembly and repairs:

- Clean, antistatic, well lit work area
- #0 Phillips tip screwdriver
- #1 Phillips tip screwdriver
- Flat Blade screwdriver
- ¼" Hex Nutdriver
- 5/8" Hex Nutdriver
- 7/16" Hex Nutdriver with Full Hollow-Shaft and plastic insert to prevent Front Panel from scratches
- ¼" Combination Wrench
- Solder: 63/37 - Tin/Lead Alloy composition, low residue, no-clean solder.
- Magnification glasses and lamps
- SMT Soldering / Desoldering bench-top repair station

Test Equipment

The following is a *minimum* suggested equipment list required for performing the proof of performance tests.

- Amplifier with speakers or headphones
- Headphones
- Cables: (dependent on your signal source)
  - Audio Input Cable (balanced) with shield and a XLR or ¼ " plug on one end and an appropriate connector on the opposite end for connection to the Low Distortion Oscillator.
  - Audio Output Cable (balanced) with shield and a XLR or ¼ " plug on one end and an appropriate connector on the opposite end for connection to the Distortion Analyzer
  - 5 pin Midi cable
  - ¼ inch phone cable (T/R/S)
- Double Footswitch with 15 foot ¼" phone plug cable configured for tip, ring and sleeve, (Lexicon P/N 750-09277) or equivalent
- Low Distortion Oscillator with single-ended or balanced output, < 100 ohms output impedance, < .005% THD.
- Analog Distortion Analyzer and level meter with single-ended or balanced input and 20kHz or 30kHz Lo Pass Filter
- 100 MHz oscilloscope
- Digital distortion analyzer & digital function generator (e.g. Stanford Research Systems Model DS360 or Audio Precision System 1 with DSP Option /System 2).
- Digital signal source (CD player, DAT, etc.)
- D/A converter (ex.: MPX-500)

Chapter 2 General Information

Periodic Maintenance

Under normal conditions the *MPX 200* system requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and mild detergent to clean the exterior surfaces of the connector box.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. It the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, price and Lexicon Part Number. Replacement parts can be ordered from:

LEXICON, INC.
3 Oak Park
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@lexicon.com
ATTN: Customer Service

Returning Units to Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If Lexicon recommends that a *MPX 200* be returned for repair and you choose to return the unit to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, on both the inside and outside of the package

Please enclose a brief note describing any conversations with Lexicon personnel (indicate the name of the person at Lexicon) and give the name and telephone daytime number of the person directly responsible for maintaining the unit.

Do no include accessories such as manuals, audio cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Customer Service personnel.

Chapter 3 Specifications

Analog Inputs

Connectors: 1/4" unbalanced
Impedance: 500K unbalanced for Direct Instrument input (unit detects a mono input on the right input)
A/D Dynamic Range: >95dB typical, 20Hz-20kHz, unweighted
Levels: -30dBu to +4dBu
Resolution: 24-Bit

Analog Outputs

Connectors: 1/4" unbalanced
Impedance: 75 Ohms for Headphone output (Right only used for mono output; Left only used for stereo headphones)
D/A Dynamic Range: >100dB typical, 20Hz-20kHz, unweighted
Levels : +8dBu typical
Resolution: 24-Bit

Frequency Response: Wet/Dry 20Hz-20kHz, ±1dB
Crosstalk: >55dB
THD: <0.05%, 20Hz-20kHz

Digital Audio Interface

Input Connectors: Coaxial, RCA type; Digital S/PDIF
Output Connectors: Coaxial, RCA type; 24-bit Digital S/PDIF (always active)
Sample Rates: 44.1kHz

Internal Audio Data Path: DSP: 24-bit

Footswitch: Tip/Ring/Sleeve phone jack for Bypass and Tap (optional)

System Specifications

Power Requirements: 100-120/220-240V~; 50-60Hz, 25W
Environment
Operating Temperature: 32° to 104° (0° to 40°C)
Relative Humidity: 95% non-condensing
Dimensions: 19"W x 1.75"H x 5.5" D (483x45x140mm)
Weight: Unit: 3.15lb (1.41kg)

Chapter 4 Performance Verification

This section describes a quick verification of the operation of the MPX 200 and the integrity of its analog and digital audio signal paths.

Initial Inspection:

Inspect the unit for any obvious signs of physical damage. Verify that the front panel controls operate smoothly and correctly. (Refer to the MPX 200 Owner' Manual for detailed explanations of this functionality.) Verify that all screws and rear panel jacks are secure.

Functional Tests:

Initial Power Up Check:

1. The voltage selection switch on the MPX 200 should be checked prior to power-on. It is located on the right side of the unit. Make sure it is switched to the proper AC voltage setting for your area.
2. Connect the power cord to the back of the MPX 200 and the other end into an isolated variable output power supply (Variac).
3. Verify the Variac's AC voltage output is set to 0.
4. Turn the MXP 200 power switch to the On position and slowly increase the AC voltage output of the Variac to the proper voltage.
5. Verify the AC current draw is < .25 amps.

Normal Power Up:

During normal power on, the MPX 200 will perform a series of diagnostic tests. These diagnostic tests should take 10 seconds or less. The diagnostic test sequence is displayed on the front panel LEDs prior to the execution of the test wherever possible for troubleshooting purposes.

If there is a failure, the test number indication LED will remain lit indicating which test has failed and the (Red) LEVEL Clip LEDs will be lit indicating that a failure has occurred. Displaying the Test/Error code on the LEDs before the test is executed makes it possible to determine which test failed if the unit hangs or crashes during the test.

The following is a table of the test numbers, the test names and the diagnostic indicator LEDs.

#1	ROM Checksum	Compressor –20dB
#2	SRAM	Compressor –10dB
#3	LEXICHIP3 WCS	Compressor –3dB
#4	LEXICHIP3 INT	Compressor Threshold
#5	EEPROM	Effects Gate

NOTE: The ROM, SRAM, LEXICHIP3 and CPU must be working properly in order for the Diagnostic LEDs to operate correctly.

If the MPX 200 powers on without a diagnostic failure, the 7-segment display will read “200”, all of the front panel LEDs will light in sequence from left to right, and the unit will enter normal operating mode.

Note: When the tests are loaded a small (r) will appear in the display. This indicates that the test is running. When the tests are actually performed, two other characters will appear, a (P) will indicate the test preformed has passed, and a (f) will indicate the test has failed. After some of the tests, when the load button is pressed and released, the displays will read (d) to indicate that the test has been exited.

Setup

1. Connect one end of the MIDI cable to the jack on the Rear Panel of the unit labeled "MIDI Out/Thru".

2. Connect the other end of the MIDI cable to the jack on the Rear Panel of the unit labeled "MIDI In".
3. Using the ¼" phone cable, connect one end to the ¼" jack marked footswitch on the back of the MPX200.
4. Connect the other end ¼" phone cable to the ¼" phone jack on the footswitch.
5. Using the appropriate power cord, connect the MPX 200 to an appropriate AC voltage source.
6. Set the MPX 200 into Extended Diagnostics mode to perform the following functional tests by turning the power switch to the ON position while holding down the Bypass button.
7. Release the “Bypass” button when the Green LEVEL –30dB LED’s are lit (after approximately 3 seconds).

Switch Test (8)

1. Turn the encoder knob clockwise until the display reads # 8.
2. Press and release the load button to execute the test.
3. The display will read: “r 8”.
4. The MPX 200 is know ready to test both the footswitch functions and the front panel switches.

Footswitches:

1. Press and hold the Left footswitch (labeled Ring) and observe that the Left –30dB headroom LED is lit.
2. Release the Left footswitch and observe that the Left –30dB headroom LED has turned off.
3. Press and hold the Right footswitch (labeled Tip) and observe that the Right –30dB headroom LED is lit.
4. Release the Right footswitch and observe that the Right –30dB headroom LED has turned off.

Front Panel Switches:

1. Press and hold the Edit button and observe that the Edit LED is lit.
2. Release the Edit button and observe that the Edit LED has turned off.
3. Press and hold the Store button and observe that the Store LED is lit.
4. Release the Store button and observe that the Store LED has turned off.
5. Press and hold the Tap/Cancel button and observe that the Tap/Cancel LED is lit.
6. Release the Tap/Cancel button and observe that the Tap/Cancel LED has turned off.
7. Press and hold the Bypass button and observe that the Bypass LED is lit.
8. Release the Bypass button and observe that the Bypass LED has turned off.
9. Press and hold the Compressor button and observe that the Compressor LED is lit.
10. Release the Compressor button and observe that the Compressor LED has turned off.
11. Press and hold the Load button and observe that the Load LED is lit.
12. Release the Load button and observe that the Load LED has turned off.
13. Observe that the 7-segment display reads: “d 8”.

Encoder Test (9)

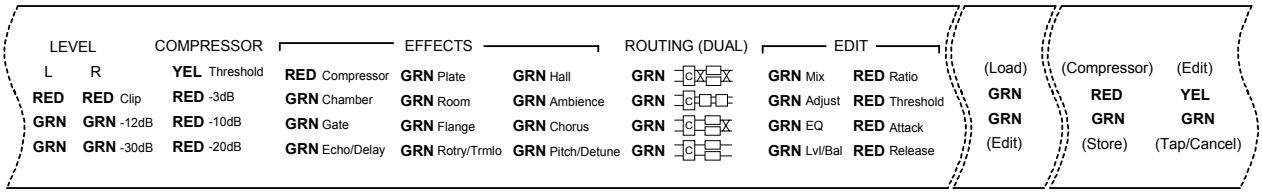
1. Turn the encoder knob clockwise until the 7-segment display reads: “9”.
2. Press and Release the Load button to execute the test.
3. Observe that the 7-segment display reads: “r 9”.
4. Turn the encoder one revolution in a clockwise direction one position at time. The display should indicate the current position of the encoder from 0-15.
5. When the test is complete the display will read: “P 9”.

MIDI Test (10)

1. Turn the encoder knob clockwise until the 7-segment display reads: “ 10”.
2. Press and release the Load button to execute the test.
3. Observe that the display reads: “P10”.

LED Test (11)

1. Turn the encoder knob clockwise until the 7-segment display reads: “ 11”.
2. Press and release the Load button to execute the test.
3. Observe that all of the front panel's LEDs are lit and that the segments on the displays are all off.
4. Observe that the colors of the LEDs are correct as shown below:



5. Turn the encoder knob clockwise one position.
6. Verify that all of the front panel's LEDs turn off and that the display will read all “8.8.8” as shown below:

NOTE: All of the segments on the 7-segment displays should be lit except the rightmost decimal point.

7. Turn the encoder knob clockwise one position.
8. The display should read: “r11” and the Left Green LEVEL –30dB LED should be lit.
9. Turning the encoder knob clockwise one position at a time, observe that that each of the remaining front panel's LEDs, as well as the segments on the 7-segment displays, can be lit individually.
10. Press and release the Load button to exit the test.
11. The display will momentarily read: “d11”, then display: “12”.

EXIT Test (12)

1. Press and release the Load button to execute the test.
2. The displays should read: “ 1” and jump into normal operating mode.
3. Set the power switch to the OFF position to power off the MPX 200.
4. Disconnect all cables from the rear panel of the MPX 200.

I/O Test:

These tests will verify the audio performance of the MPX 200’s audio input and output circuitry.

Setup:

1. Turn on the MPX 200 and wait for the Power On Diagnostics cycle to finish.
2. Turn the Program Select Knob to Program #1.
3. Press the Bypass button on the front panel and verify that the Bypass button LED lights, and the display flashes **bYP**.
4. Connect a (balanced) audio cable between the Low Distortion Oscillator and the MPX 200 Left Input.
5. Connect a (balanced) audio cable between the MPX 200 Left output and the Distortion Analyzer.
6. Set the Distortion Analyzer to measure VRMS.
7. Turn the Input Trim knob fully clockwise.

Analog In To Analog Out Audio Test:

1. Apply a 1kHz-sinewave signal to the MPX 200 Left Input @ 775 mVRMS.
2. Measure the Left Output for a level between 2.273 and 1.781 VRMS.
3. Switch the cables to the Right Input/Output connections and repeat step 3.

Frequency Response:

These tests will verify the frequency response specifications of the Left and Right analog inputs to the Left and Right output signal paths of the MPX 200.

Analog In To Analog Out Frequency Response Test:

1. Disable all Filters on the Distortion Analyzer
2. Apply a 1kHz-sinewave signal to the MPX 200 Left Input @ 218 mVRMS.
3. Connect the Left Output to the Distortion Analyzer.
4. Set the Analyzer for a 0dB reference (@1kHz).
5. Sweep the Oscillator from 20Hz to 20kHz and verify the level stays within +/- 1.0dBr throughout the sweep.
6. Switch the cables to the Right Input/Output connections and repeat steps 4 and 5.

THD+N Measurement:

These tests will verify the THD+N specifications of the MPX 200 Left and Right input to output circuitry.

Analog In To Analog Out THD+N Test:

1. Apply a 1kHz-sinewave signal to the MPX 200 Left Input @ 218 mVRMS.
2. Connect the Left Output to the Distortion Analyzer.
3. Set the Distortion Analyzer to measure THD.
4. Enable the Low pass filters on the Analyzer (30kHz, 20kHz).
5. Verify the Left output THD+Noise level on the Analyzer is <0.05%.
6. Switch the cables to the Right Input/Output connections and repeat step 5.

Crosstalk Test:

Analog In To Analog Out Crosstalk Test:

1. Apply a 1kHz-sinewave signal to the MPX 200 Left Input @ 218 mVRMS.
2. Connect the Right Output to the Distortion Analyzer.
3. Enable the Low pass filters on the Analyzer (30kHz, 20kHz).
4. Sweep the Oscillator from 20Hz to 20kHz and verify the level stays < -55dB through out the sweep.
5. Switch the Input cable to the Right side and the Output cable to the Left and repeat step 4.

Dynamic Range Test:

These tests will verify the Dynamic Range specifications of the MPX 200 Left and Right input to output circuitry.

Analog In To Analog Out Dynamic Range Test:

1. Apply a 1kHz-sinewave signal to the MPX 200 Left Input @ 2.45VRMS
2. Connect the Left Output to the Distortion Analyzer.
3. Set the Distortion Analyzer for a 0dB reference.
4. Remove the Input cable from the Left input.
5. Enable the Low pass filters on the Analyzer (30kHz, 20kHz).
6. Verify the Noise level at the Left Output is < -95dB.
7. Connect the 1kHz-sinewave signal to the Right Input of the MPX 200.
8. Move the Left Output cable to the Right Output.
9. Set the Distortion Analyzer for a 0dB reference
10. Remove the Input cable from the Right input.
11. Enable the Low pass filters on the Analyzer (30kHz, 20kHz).
12. Verify the Noise level at the Right Output is < -95dB.

Digital I/O Functionality

This test will verify that the MPX 200 will pass an S/PDIF signal through its input and output circuitry.

1. Connect a Digital signal (CD player, DAT, etc.) to the S/PDIF input jack on the back of the MPX 200.
2. Connect the S/PDIF output for the MPX 200 to a D/A converter (ex.: MPX 500) for conversion back to an analog signal.
3. Connect the analog output of the D/A converter to your amplifier with speaker output. Be sure to turn the volume down on the amplifier.
4. Set the MPX 200 System Mode for digital Input.
5. Set the MPX 500 System Mode for digital Input.
6. Start playing your digital source.
7. Turn the volume up on your amplifier and verify you have audio and that it is clean and free of any audio defects or artifacts (pops, clicks, static, etc.).

Listening Test:

1. Connect the audio input cable from the output of the Distortion Oscillator to the Left input of the MPX 200.
2. Connect the audio output cable from the Right output of the MPX 200 to the input of the Headphone amplifier.
3. Set the Headphone Amplifier volume control to its lowest setting.
4. Set the Oscillator for 220Hz sinewave at 50m Vrms.
5. Power on the MPX 200 and turn the program knob to the # 111 program: Abyss.
6. Press the Edit button and turn the Mix up to 100%.
7. Put on the headphones and bring the volume up on the Headphone amp to a comfortable listening level.
8. Sweep the input knob over its entire range and verify there are no pops, clicks, distortion, or static noises heard when turning the knob.
9. Swap the cables from the Left Input/Output connectors to the Right Input/Output connectors and repeat the above procedure.

Shock Test:

Note: To prevent damaging the unit, keep the other sides of the unit touching the work surface at all times.

1. While listening to the unit with the headphones lift a corner of the MPX 200 off of the table approximately 4 inches and then drop.
2. Verify that there is no lose of audio or distortion during this action.
3. Repeat this test lifting at each of all four corners of the MPX 200

Lexicon Audio Precision ATE Summary

This chart represents a summary of test Audio Precision test equipment settings and parameters used by Lexicon Manufacturing in production testing of all MPX 200 product. This is provided as a reference and supplement to bench test settings found in the proof of performance in this manual.

A/D Files	Source						Analyzer							
Test	Left Input	Right Input	Freq	Imp.	Bal / Unbal	Gnd / Float	Level	Reading	Upper	Lower	Filter	Imp	Band	Sample Rate
A-DGAIN	-21dBu	-21dBu	997	25 Ohm	Unbal	Float	LEVEL(dBFS)	-1.60	-0.66	-2.54	Off	------	--------	44.1kHz
A-DFREQ	-31dBu	-31dBu	20-20k	25 Ohm	Unbal	Float	LEVEL(dBFS)	0.025	1.06	-1.06	Off	------	--------	44.1Khz
ADSETLVL	-20dBu	-20dBu	997	25 Ohm	Unbal	Float	LEVEL(dBFS)	-20.25	-20.00	-20.50	Off	------	--------	44.1kHz
A-DTHD *	-11dBu	-11dBu	22-20k	25 Ohm	Unbal	Float	FLTLVL(%)	0.005	0.05	0.0007	Band Rej	------	--------	44.1kHz
A-DXTALK *	-11dBu	-11dBu	997	25 Ohm	Unbal	Float	LEVEL(dBFS)	-98.50	-54.94	-120.0	Off	------	--------	44.1kHz
A-DDYNR *	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	FLTLVL(dBFS)	-102.50	-96.94	-120.00	Off	------	--------	44.1kHz

D/A Files	Source						Analyzer							
Test	Left Input	Right Input	Freq	Imp.	Bal / Unbal	Gnd / Float	Level	Reading	Upper	Lower	Filter	Imp	Band	Sample Rate
D-AGAIN	0dBFS	0dBFS	997	----	--------	--------	AMPL(dBu)	8.46	9.52	7.40	Off	100k	10-500k	44.1kHz
D-AFREQ	0dBFS	0dBFS	20-20k	----	--------	--------	AMPL(dBr)	0.001	1.06	-1.06	Off	100k	10-500k	44.1kHz
D-ATHD	0dBFS	0dBFS	22-20k	----	--------	--------	THD+N(%)	0.005	0.05	0.0007	Off	100k	10-22k	44.1kHz
D-AXTALK	0dBFS	0dBFS	997	----	--------	--------	XTALK(dB)	-95.00	-54.94	-120.00	Off	100k	10-22k	44.1kHz
D-ADYNR	-60dBFS	-60dBFS	997	----	--------	--------	AMPL(dBr)	-104.25	-96.94	-120.00	Off	100k	22-22k	44.1kHz

A/A Files	Source						Analyzer							
Test	Left Input	Right Input	Freq	Imp.	Bal / Unbal	Gnd / Float	Level	Reading	Upper	Lower	Filter	Imp	Band	Sample Rate
A-AGAIN *	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	8.29	9.35	7.23	Off	100k	10-500k	44.1kHz
AASETLVL **	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	8.29	8.00	8.50	Off	100k	10-500k	44.1kHz
A-AFREQ *	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	AMPL(dBr)	-0.025	1.06	-1.06	Off	100k	10-500k	44.1kHz
A-ATHD *	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	THD+N(%)	0.006	0.05	0.0007	Off	100k	20-22k	44.1kHz
A-AXTALK *	-11dBu	-11dBu	20-20K	25 Ohm	Unbal	Float	XTALK(dB)	-64.50	-54.94	-120.00	Off	100k	10-22k	44.1kHz
A-ASNRL*	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBr)	-100.50	-94.94	-120.00	Off	100k	20-22k	44.1kHz
A-ADYNRL *	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	THD+N(dBr)	-101.00	-94.94	-120.00	Off	100k	20-22k	44.1kHz
A-ASNRR *	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBr)	-100.50	-94.94	-120.00	Off	100k	20-22k	44.1kHz
A-ADYNRR *	-50dBu	-50dBu	997	25 Ohm	Unbal	Float	THD+N(dBr)	-101.00	-94.94	-120.00	Off	100k	20-22k	44.1kHz
A-AMUTE *	0dBu	0dBu	997	25 Ohm	Unbal	Float	AMPL(dBr)	-38.00	-30.00	-50.00	Off	100k	10-500k	44.1kHz
LISTEN	Off	-24dBu	997	25 Ohm	Unbal	Float	AMPL(dBu)	------	------	------	Off	100k	10-500k	44.1kHz

Chapter 5 Troubleshooting

Check the Lexicon web site for the latest software and information:
http://www.lexicon.com
The Lexicon Studio downloads page:

The Lexicon Support Knowledgebase:
http://www.lexicon.com/kbase/index.asp

Diagnostics

Introduction

This section contains the complete diagnostics descriptions for the Lexicon MPX 200 product.

Diagnostics Test Descriptions

There are two categories of diagnostics that exist in the MPX 200 software: Power On Self Tests (POST), and Extended Diagnostics. The POST are executed automatically when the system is first powered up. The Extended Diagnostics are invoked by pressing and holding the front panel BYPASS button while powering on the unit. The Extended Diagnostics are used to perform functional tests that are not performed during the Power-On Self Tests, and also for troubleshooting purposes.

NOTE: The Extended Diagnostics can also be invoked by pressing and holding the Bypass Footswitch (labeled Ring) while powering on the unit.

Power-On Self Tests (POST)

Upon normal power up, the MPX 200 will perform a series of diagnostic tests. For a description of these tests, refer to Table 2.1. These diagnostic tests have been designed to take less than 10 seconds. The diagnostic test sequence is displayed on the front panel LEDs prior to the execution of the test wherever possible for troubleshooting purposes (provided the LEDs are functioning properly).

NOTE: The first time the MPX 200 is powered on, the EEPROM will be initialized during the EEPROM diagnostic test and the 7-segment display will display "rSt" to indicate that the EEPROM is being initialized. Once the EEPROM has been initialized, the unit will reset and repeat the POST. This initialization process takes approximately 40 seconds, otherwise the POST would normally take approximately 10 seconds.

Throughout this document, these LEDs will be referred to as the Diagnostic LEDs. These LEDs are used to indicate the corresponding test number, and are turned on before each test is executed. Displaying the Test/Error code on the LEDs before the test is executed makes it possible to determine which test failed if the unit hangs or crashes during the test.

Test #	Test Name	Diagnostic LED
1	ROM Checksum	COMPRESSOR "–20dB"
2	SRAM	COMPRESSOR "–10dB"
3	LEXICHIP3 WCS	COMPRESSOR "–3dB"
4	LEXICHIP3 INT	COMPRESSOR "Threshold"
6	EEPROM	EFFECTS "Gate"

Table 2.1

NOTE: The ROM, SRAM, LEXICHIP3 and CPU must be working properly in order for the Diagnostic LEDs to operate correctly.

Upon completion of the POST, the 7-segment displays will display “200”, all of the front panel LEDs will light in sequence from left to right, then the unit will enter normal operating mode.

If a POST fails, the appropriate Diagnostic LED will remain lit indicating which test has failed and the (Red) **LEVEL** Clip LEDs are lit indicating a failure has occurred. If a failure has occurred, the unit should be repaired before proceeding. Refer to the MPX 200 Service Manual, Lexicon P/N 070-14827, for more information.

Pass/Fail Status:

The front panel LEVEL LEDs are used to indicate the pass/fail status of the POST as follows:

The (Green) LEVEL Clip LEDs are lit to indicate when the test has Passed.
The (Red) LEVEL Clip LEDs are lit to indicate when the test has Failed.

Diagnostic Failures:

When a failure is encountered during the test sequence:

The test code is displayed on the Diagnostic LEDs (Refer to Table 1).
The (Red) LEVEL Clip LEDs are turned on to indicate a failure has occurred.
The unit stops executing the POST sequence.
The audio outputs are muted, and the unit will not become operational.

If the Bypass button is pressed after a failure has occurred, the MPX 200 will attempt to continue on with the next test of the POST sequence. The MPX 200 will attempt to do this every time the Bypass button is pressed.

If the STORE button is pressed after a failure has occurred, the MPX 200 will enter the Extended Diagnostics mode.

If the Tap/Cancel button is pressed after a failure has occurred, the MPX 200 will run the test continuously.

The following diagram shows an example of the Diagnostic LEDs Test/Error code 4. This code indicates that the Lexichip3 INT Test (4) has failed:

	LEVEL		**COMPRESSOR**		
	L	**R**	1	Threshold	**<-*indicates Lexichip3 INT test***
Indicates Error ->	1	1	0	-3dB	
	0	0	0	-10dB	0 Gate
	0	0	0	-20dB	0 Echo/Delay

Legend: *0 = LED off, 1 = LED on*

NOTE: During the POST, the LEVEL LEDs display the pass/fail status for tests 3-6 only.

Power On Test Descriptions

ROM Test (1)

The ROM checksum, is a byte size value that is stored in the last location of each bank. The test adds the contents of the entire ROM including the checksum byte. The result should equal zero (8 bit value).

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs:

Test #	Test Name	Diagnostic LED
1	ROM	COMPRESSOR “–20dB”

If a failure occurs, the (Red) LEVEL Clip LEDs will be turned on in addition to the Diagnostic LED, and the CPU will attempt continuously loop the test for troubleshooting purposes.

If the Bypass button is pressed, the failure is ignored and the next test will be executed.

SRAM Test (2)

The SRAM Test performed during the POST is a destructive test, meaning that any data stored in SRAM will be lost. The entire contents of the SRAM is tested by first writing 00 hex (00000000 binary) to all of the memory locations, and then verified by reading back all of the memory locations. This write/read sequence is also performed using the following patterns: 55 hex (01010101 binary), AA hex (10101010 binary) and FF hex (11111111 binary).

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs:

Test #	Test Name	Diagnostic LED
2	SRAM	COMPRESSOR “–10dB”

If a failure occurs, the (Red) LEVEL Clip LEDs will be turned on in addition to the Diagnostic LED, and the CPU will attempt continuously loop the test for troubleshooting purposes.

If the Bypass button is pressed, the failure is ignored and the next test will be executed.

Lexichip3 WCS Test (3)

The Lexichip3 WCS test will check the program memory space (the Writeable Control Store) of the Lexichip3. The RAM (memory space) is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (10101010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is then repeated checking for AA's and storing 0's into memory. Following this test is an Address test to verify all the address lines are active. Finally, the memory is checked for 0's.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs:

Test #	Test Name	Diagnostic LED
3	Lexichip3 WCS	COMPRESSOR “–3dB”

If a failure occurs, the (Red) LEVEL Clip LEDs will be turned on in addition to the Diagnostic LED, and the CPU will attempt continuously loop the test for troubleshooting purposes.

If the Bypass button is pressed, the failure is ignored and the next test will be executed.

If the Tap/Cancel button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

Lexichip3 INT Test (4)

The Lexichip3 INT test will verify that the Lexichip3 interrupt (INT/) is working and occurring at the proper intervals. The Lexichip3 will provide MPX 200 with the interrupt (INT/) to the Z80's maskable interrupt line.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs:

Test #	Test Name	Diagnostic LED
4	Lexichip3 INT	COMPRESSOR “Threshold”

If a failure occurs, the (Red) LEVEL Clip LEDs will be turned on in addition to the Diagnostic LED, and the CPU will attempt continuously loop the test for troubleshooting purposes.

If the Bypass button is pressed, the failure is ignored and the next test will be executed.

If the Tap/Cancel button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

EEPROM Test (6)

This test will read each byte in the User Register portion of the EEPROM and add them together to calculate a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum will be recalculated each time a register is stored.

The test will also verify that the EEPROM has been initialized properly. This is done by storing the software version of the EEPROM in the first five bytes of the EEPROM, and then verifying the stored value is correct when the test is executed. If the stored value read from the first five bytes of the EEPROM is incorrect, the EEPROM will be initialized.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs:

Test #	Test Name	Diagnostic LED
6	EEPROM	EFFECTS “Gate“

If a failure occurs, the (Red) LEVEL Clip LEDs will be turned on in addition to the Diagnostic LED, and the CPU will attempt continuously loop the test for troubleshooting purposes.

If the Bypass button is pressed, the failure is ignored and the next test will be executed.

If the Tap/Cancel button is pressed, the CPU will attempt to go into a mode where it can execute the test continuously.

EXTENDED DIAGNOSTICS

The following tests are available in the Extended Diagnostics:

Test #	Test Name	Diagnostic LED	7 Segment LED Display	Note:
1	ROM Checksum	COMPRESSOR “–20dB”	1	1
2	SRAM	COMPRESSOR “–10dB”	2	1
3	LEXICHIP3 WCS	COMPRESSOR “–3dB”	3	1
4	LEXICHIP3 INT	COMPRESSOR “Threshold”	4	1
5	LEXICHIP3 ADF	EFFECTS “Echo/Delay”	5	1
6	EEPROM	EFFECTS “Gate“	6	1
7	DRAM	EFFECTS “Chamber”	7	3
8	Switch	EFFECTS “Compressor”	8	2
9	Encoder	EFFECTS “Rotry/Trmlo”	9	3
10	MIDI	EFFECTS “Flange”	10	3
11	LED	EFFECTS “Room”	11	2
12	Exit	EFFECTS “Plate”	12	
13	Initialize	EFFECTS “Pitch/Detune”	13	
14	Unused	EFFECTS “Chorus”	14	
15	Unused	EFFECTS “Ambience”	15	
16	Burn In	EFFECTS “Hall”	16	3

LED Off = 0, LED On = 1

Note 1: These tests reside in the POST.
Note 2: These tests require operator interaction and judgment, and do not generate an error message.
Note 3: These tests require operator interaction and judgment, and generate an error message.

The Extended Diagnostics are invoked by pressing and holding the Bypass button while powering on the unit, then releasing the Bypass button once the Green LEVEL -30dB LEDs have lit. After the Bypass button is released, the 7-segment displays as well as the Diagnostic LEDs will indicate the test number selected, and the remaining LEDs will shut off.

For example, when the Lexichip3 ADF Test (5) is selected using the Encoder, the EFFECTS “Echo/Delay” Diagnostic LEDs will be lit. This is useful for debugging the unit should any of the 7-segment displays become inoperative.

When a test has been selected, the Load button must be pressed to execute it.

The leftmost 7-segment display is used to indicate the following:

“r” indicates when the test is running
“P” indicates when the test has passed
“F” indicates when the test has failed.
“d” indicates when the test is done.

NOTE: For tests that require operator interaction and judgment, the 7-segment displays will not indicate when tests are running, or the pass/fail status of the test. For these tests, a “d” is placed in leftmost 7-segment display to indicate when the tests has been exited and the test is done.

The Diagnostic LEDs are also used to indicate the test pass/fail status as follows:

The (Green) LEVEL Clip LEDs are lit to indicate when the test has Passed.
The (Red) LEVEL Clip LEDs are lit to indicate when the test has Failed.

The following tests can be run continuously by pressing the Tap/Cancel button instead of the Load button.

Test #	Test Name	Diagnostic LED	7-segment display
1	ROM Checksum	COMPRESSOR “–20dB”	1
2	SRAM	COMPRESSOR “–10dB”	2
3	LEXICHIP3 WCS	COMPRESSOR “–3dB”	3
4	LEXICHIP3 INT	COMPRESSOR “Threshold”	4
5	LEXICHIP3 ADF	EFFECTS “Echo/Delay”	5
6	EEPROM	EFFECTS “Gate“	6
7	DRAM	EFFECTS “Chamber”	7
8	Switch	EFFECTS “Compressor”	8
9	Encoder	EFFECTS “Rotry/Trmlo”	9
10	MIDI	EFFECTS “Flange”	10
11	LED	EFFECTS “Room”	11

When a test is run continuously a Pass/fail status will be displayed and updated on the front panel LEVEL LEDs and the 7-segment displays each time the test is run.

Extended Diagnostic Test Desriptions

ROM Test (1)

This is the same test that resides in the POST. It was included in the Extended Diagnostics for troubleshooting purposes.

The ROM checksum, is a byte size value that is stored in the last location of each bank. The test adds the contents of the entire ROM including the Checksum byte. The result should equal zero (8 bit value).

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
1	ROM	COMPRESSOR “–20dB”	1

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost digit of the 7-segment display will display an “r” to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment display and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

SRAM Test (2)

The SRAM Test performed during the Extended Diagnostics is a non-destructive test. The non-destructive test will test one memory location at a time, saving the contents from the location being tested into a

register, and then restoring the value when it's done. The entire contents of the SRAM is tested by writing 00 hex (00000000 binary), and verified by reading the same value back from each memory location. This write/read sequence is also performed using the following patterns: 55 hex (01010101 binary), AA hex (10101010 binary) and FF hex (11111111 binary).

This test was included in the Extended Diagnostics for troubleshooting purposes.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment display:

Test #	Test Name	Diagnostic LED	7-segment display
2	SRAM	COMPRESSOR “–10dB”	2

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost digit of the 7-segment display will display an “r” to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment display and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

Lexichip3 WCS Test (3)

This is the same test that resides in the power up diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

This test will check the program memory space (the writeable control store) of the Lexichip3. The RAM (memory space) is first filled with the value 55 hex (01010101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is filled with AA hex (10101010 binary), and the next location is processed. Once the RAM has been checked for 55's and filled with AA's, the process is then repeated checking for AA's and storing 0's into memory. Following this test is an Address test to verify all the address lines are active. Finally, the memory is checked for 0's.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment display:

Test #	Test Name	Diagnostic LED	7-segment display
3	Lexichip3 WCS	COMPRESSOR “–3dB”	3

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost 7-segment display will display an “r” to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

Lexichip3 INT Test (4)

This is the same test that resides in the power up diagnostics. It was included in the Extended Diagnostics for troubleshooting purposes.

The Interrupt test will verify that the Lexichip3 interrupt (ZINT/) is working and occurring at the proper intervals. The Lexichip3 will provide MPX 200 with the interrupt (ZINT/) to the Z80's maskable interrupt line.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
4	Lexichip3 INT	COMPRESSOR "Threshold"	4

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost 7-segment display will display an "r" to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

Lexichip3 ADF Test (5)

This test will verify that the Lexichip3 Audio Data File memory is working.

The Lexichip3 Audio Data File (ADF) is a fast synchronous 128-word SRAM that provides audio data buffering and storage for: external memory references, Serial I/O, and the Host-to-Lexichip data port. ADF locations also function as ARU Registers and as scratchpad memory. This test will verify that the Lexichip3 Audio Data File is working properly.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
5	Lexichip3 ADF	EFFECTS "Echo/Delay"	5

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

NOTE: During the Lexichip3 ADF test, several LEDs may flicker. This is normal operation, and not considered a failure in the unit.

When the test is executed, the left most 7-segment display will display an "r" to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

EEPROM Test (6)

This test will read each byte in the User Register portion of the EEPROM and add them together to calculate a checksum. This value is compared with the checksum value stored in the EEPROM itself. This checksum will be recalculated each time a register is stored.

The test will also verify that the EEPROM has been initialized properly. This is done by storing the software version of the EEPROM in the first five bytes of the EEPROM, and then verifying the stored value is correct when the test is executed. If the stored value read from the first five bytes of the EEPROM is incorrect, the EEPROM will be initialized.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
6	EEPROM	EFFECTS “Gate“	6

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost 7-segment display will display an “r” to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

DRAM Test (7)

The DRAM test puts the Lexichip3 into a mode that allows the Z80 microprocessor to read and write to the 1M X 4 DRAM through the Lexichip3. To actually test the DRAM, the Z80 performs two tests, a data test and an address test. During the data test the Z80 writes AA (hex) (10101010) into all of the memory locations then reads them back to check them. It repeats the process with 55 (01010101). For the address test, the Z80 writes a count into the memory then reads it back (i.e. 00000001, 00000010, 00000011). This test will take approximately 45 seconds to complete.

During the test, there is limited control of the front panel LEDs due to the interrupts being turned off. Because of this, the front panel LEDs cannot be updated to indicate the test number on the Diagnostic LEDs, or the pass/fail status of the test.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment display:

Test #	Test Name	Diagnostic LED	7-segment display
7	DRAM	EFFECTS “Chamber”	7

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost 7-segment display will display an “r” to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

Switch Test (8)

The Switch Test is essentially two tests in one. The combination of the two tests provide a means for verifying the operation of the front panel Switches (6) and Footswitches (2) along with their associated LEDs at the same time.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
8	Switch	EFFECTS “Compressor”	8

Pressing the Load button will execute the test.

Pressing and Releasing the Load button will exit the test.

Footswitches:

When the Left Footswitch (labeled Ring) is pressed, the Left –30dB Headroom LED will be lit. When the Left Footswitch is released, the Left –30dB Headroom LED will go off.

When the Right Footswitch (labeled Tip) is pressed, the Right –30dB Headroom LED will be lit. When the Right Footswitch is released, the Right –30dB Headroom LED will go off.

Front Panel Switches:

When the Edit button is pressed and held the Edit LED will be lit. When the Edit button is released, the Edit LED will be turned off.

When the Store button is pressed and held the Store LED will be lit. When the Store button is released, the Store LED will be turned off.

When the Tap/Cancel button is pressed and held the Tap/Cancel LED will be lit. When the Tap/Cancel button is released, the Tap/Cancel LED will be turned off.

When the Bypass button is pressed and held the Bypass LED will be lit. When the Bypass button is released, the Bypass LED will be turned off.

When the Compressor button is pressed and held the Compressor LED will be lit. When the Compressor button is released, the Compressor LED will be turned off.

When the Load button is pressed and held the Load LED will be lit. When the Load button is released, a “d” will be placed in the leftmost 7-segment display to indicate that the test has been exited.

Encoder Test (9)

During the Encoder test, the Z80 microprocessor reads the value of the encoder, and then expects the next value read from the encoder (when the encoder position is moved) will be at a predetermined incremental

value. Therefore, during the test the encoder must be rotated in a clockwise direction as it's being tested, or the test will fail.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
9	Encoder	EFFECTS "Rotry/Trmlo"	9

Pressing the Load button will execute the test.

When the test is executed, the leftmost 7-segment display will display an "r" to indicate the test is running, and the rightmost digit of the 7-segment displays will indicate the value of the encoder's current position. The values range from (0-15).

MIDI Test (10)

This test will verify that the MIDI Input and MIDI Output/Thru circuits are working. The test will transmit data out of the MIDI OUT jack and will attempt to read the data through the MIDI IN jack. To run this test, a 5 Pin Male DIN to 5 Pin Male DIN Cable (also known as a MIDI cable) must be connected between the MIDI IN jack and the MIDI OUT jack.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
10	MIDI	EFFECTS "Flange"	10

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, the leftmost 7-segment display will display an "r" to indicate the test is running. The pass/fail status of the test is displayed on the 7-segment displays and front panel LEVEL LEDs.

If the test passed, the (Green) LEVEL -30dB LEDs will light.

If the test failed, the (Red) LEVEL Clip LEDs will light.

LED Test (11)

This test will verify that the LEDs and LED driver circuits are working. The test has essentially three sections which perform the following functions:

1. Turn on all of the front panel LEDs, except for the LED segments on the 7-segment display.
2. Turn on all of the LED segments on the 7-segment display only.
3. Turn on each of the front panel LEDs and the LED segments on the 7-segment display individually.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

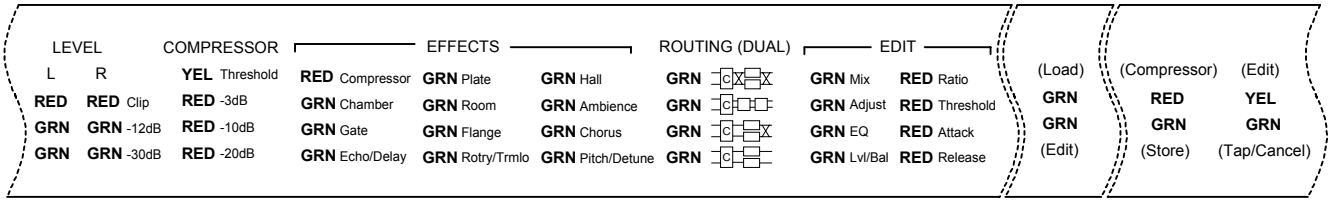
Test #	Test Name	Diagnostic LED	7-segment display
11	LED	EFFECTS “Room”	11

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

When the test is executed, all of the front panel LEDs will be lit, and the remaining LED segments on the 7-segment displays are turned off.

NOTE: The LED colors are indicated in the diagram below:



When the encoder knob is turned clockwise one position, the front panel LEDs will be turned off, and all of the LED segments on the 7-segment displays (except for the rightmost decimal point) will be lit to read: “8.8.8” as shown below:

When the encoder knob is turned clockwise one position, the 7-segment displays will read: “r11” to indicate the test is running, and the Left (Green) LEVEL –30dB LED will be lit.

NOTE: From this point on, each of the front panel LEDs and LED segments on the 7-segment displays can be lit individually by turning the encoder knob clockwise one position at a time.

When the Load button is pressed and released, a “d” will be placed in the leftmost 7-segment display to indicate that the test has been exited.

Exit Test (12)

This selection will allow the user to exit the Extended Diagnostic Mode into normal operating mode. When selected, the Diagnostic LEDs will read the following:

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
12	Exit	EFFECTS “Plate”	12

Pressing the Load button will execute the test.

Initialize Test (13)

This selection will initialize all of the MPX 200 system parameters to their factory default settings.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
13	Initialize	EFFECTS “Pitch/Detune”	13

Pressing the Load button will execute the test.

When the test is executed, the 7-segment displays will display “rSt” to indicate that the EEPROM is being initialized. Once the EEPROM has been initialized, the unit will reset and perform the POST.

Unused (14)

This is not an actual test. When executed, the 7-segment displays will indicate “d14”.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
14	Unused	EFFECTS “Chorus”	14

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

Unused (15)

This is not an actual test. When executed, the 7-segment display will indicate “d15”.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
15	Unused	EFFECTS “Ambience”	15

Pressing the Load button will execute the test.

Pressing the Tap/Cancel button will run the test continuously.

Burn In Tests (16)

During the execution of the Diagnostics in the Burn In loop, the appropriate test code will be displayed on the Diagnostic LEDs (BYPASS, STORE and TAP). This code will be sent to the LEDs before each test is executed. By displaying a test/error code on the LEDs before the test is activated, it will be easier to determine which test failed if the unit hangs or crashes during the Burn In loop. The test numbers and names are also displayed on the 7-segment display, along with the Pass/fail status of each test.

Before the test is executed, the following test code will be displayed on the Diagnostic LEDs, along with the test number on the 7-segment displays:

Test #	Test Name	Diagnostic LED	7-segment display
16	Burn In	EFFECTS “Hall”	16

Pressing the Load button will execute the test.

The Burn In loop will continuously run the following diagnostics:

Test #	Test Name	Diagnostic LED	7-segment display
1	ROM	COMPRESSOR “–20”	1
2	SRAM	COMPRESSOR “–10”	2
3	WCS	COMPRESSOR “–3”	3
4	INT	COMPRESSOR “Threshold”	4
5	ADF	EFFECTS “Eko/Dly”	5
6	EEPROM	EFFECTS “Gate“	6
7	DRAM	EFFECTS “Chamber”	7

When the test is executed, the 7-segment displays will indicate that the test is “Running…”, followed by the Pass/fail status of the test.

If the test passed, the (Green) LEVEL -30dB LEDs will light.
If the test failed, the (Red) LEVEL Clip LEDs will light.

There are two options available when a test has failed during the Burn In loop:

1. Press the Bypass button to continue the Burn-in loop.

2. Press the Tap/Cancel button to run the failed test continuously.

Service Notes:

WARNING  :

Voltage Regulator
CAUTION: THE VOLTAGE REGULATOR (U25) GETS VERY HOT!
Always use caution when testing the unit with the Main PCB removed from the chassis, be sure to place a heatsink (HEATSINK,TO220,.75X.5X.5"H, Lexicon P/N 704-14132 or equivalent) onto the voltage regulator at U25 to dissipate excess heat, and protect it from reaching thermal shutdown.

Chapter 6 Theory of Operation

Main Board

Schematic Walkthrough

Sheet 1

This sheet shows the analog input circuitry (U1-U2), the analog output (U6), and the output mute circuitry (U7).

Input Stage

Separate unbalanced ¼" phone jacks (J1-J2) provide input for the left and right signals. A single input source will be routed to both left and right input stages if the right channel (J1) is the only one used. These jacks provide AC coupled chassis ground connections through integrated ground lugs. This AC coupling is provided via C26 and C45. These components effectively AC couple the analog ground plane to the chassis by way of the enclosure. This scheme is used to minimize AC hum loops from forming at the inputs.

Capacitors C26 and C47 provide protection from high frequency interference from entering or exiting the MPX200 via the input cables.

DC Blocking is incorporated by capacitors C29 and C48 in series with the input signal paths.

The input impedance for each channel is set by R7 and R22 (Right and Left channels, respectively). Each channel has an input impedance of 1M when used in Stereo mode, and a combined input impedance of 500K when used in Mono mode (Right channel only). This was incorporated as a concession to guitarists. Due to this relatively high input impedance, the unit is susceptible to noise pickup from radiating sources, particularly if the input cables are routed near the power supply of the unit, so care must be taken when routing cables into the unit. J1 and J2 short the input paths to ground when no input cables are plugged in. This prevents noise voltages from being generated by this high impedance.

D1 and D2 provide clamping protection of the input signal paths into U1 and U2, while R6 and R19 provide input current limiting to U1 and U2. The diodes ensure that the non-inverting inputs of the op-amps never see voltages more than 0.7V above or below the positive and negative supply rails.

One half of U1 and U2 are used as non-inverting amplifier stages. These first stage components provide a DC gain of 10.55dB. The input and feedback circuitry comprised of R5, R4, and C6 for the right channel and R21, R20, and C21 for the left channel form high pass filters shelving at 3kHz and 9kHz. This is the standard 15/50uS pre-emphasis curve. C5 and C20 provide closed loop frequency compensation for the input buffer stages.

C2 and C17 remove DC offset from the buffer output stages so that wiper noise from the Level potentiometer R1 is eliminated. R1 is a dual ganged pot. The mechanical frame of R1 ties into the analog ground plane on the PCB via R16 and makes contact with the front panel. R16 is currently not installed on the PCB, therefore direct connection of analog ground and earth ground is not implemented.

The wipers of R1 connect directly to the non-inverting inputs of the second half of devices U1 and U2. These are simple DC gain stages. The gain of each stage is 21.97dB set by R2/R3 for the right channel and R17/R18 for the left channel. Feedback capacitors C1 and C16 provide frequency compensation.

The outputs of these stages provide input to the CODEC circuitry on the next page. These are signals IN_LEFT and IN_RIGHT.

Output Stage and Muting

The output of the CODEC circuitry re-enters this page as signals OUT_LEFT and OUT_RIGHT.

Provisions are made for an additional low pass filter of these signals by installing capacitors in locations R45 and R33; additionally, the CODEC signal may be attenuated or “padded” by installing resistors in these locations, but these have not been implemented in the design. R33 and R45 are left as uninstalled locations.

C50 and C51 provide AC coupling of the OUT_RIGHT and OUT_LEFT signals. The AC side of these capacitors are connected to two analog switches comprised of two sections of device U7. These switches provide output muting during power up and power down conditions. When the MUTE/ signal at pins 9 and 10 of U7 is brought to a logic low, the output signals at pin 4 (Left channel) and pin 15 (Right channel) are internally switched to pins 5 and 2 respectively. These pins in turn are tied to analog ground, thereby providing a low impedance path to ground for the OUT_RIGHT and OUT_LEFT signals. Approximately 43dB of attenuation is achieved when the switch is in mute mode.

A dual op-amp (U6) and its associated circuitry comprise the output circuitry. Each stage is set to a fixed gain of 10.42dB by way of R50/R51 (Right channel) and R52/R53 (Left channel). R48 and R49 set the input impedance of the op-amp circuitry to 10K. C49 and C56 provide high frequency compensation for the op-amps; this keeps the amplifiers from breaking into spurious oscillation. This dual op-amp is powered by +/-10V unregulated supplies. In reality, because these supply voltages are unregulated, the actual measured voltages are more akin to +12V and -15V. This was done to afford the widest possible headroom for the output. C52 and C53 provide de-coupling for these supplies.

An output impedance of 75 ohms is developed by R59 and R79 for the right and left outputs respectively. These provide output current limiting protection.

The ¼” unbalanced output jacks (J3 and J4) are configured so that when only the right output is used (J3), the left and right signals are summed together to provide a monophonic output. The left jack J4) can support stereo headphones if J3 is unused. The right channel is provided on the tip and the left channel on the ring of a stereo phone jack. C63 and C73 provide RFI suppression at the output. Like the input jack pair, these jacks AC couple analog ground to chassis ground via C61 and C71 and the respective ground lugs on the jacks. This is again to prevent AC hum loops from forming at the outputs.

Although the output op-amp can drive high impedance (>100 ohms) headphones, for best results a headphone amplifier should be used for low impedance phones.

Sheet 2

This sheet shows the CODEC device (U5), the input signal DC bias circuitry (R14 and R15), the single-ended to differential input amplifiers (U3), and the differential to single ended output amplifiers (U4). Shown also are the various clock and control signals used by the CODEC.

Single-ended to differential converter

Each section of dual op-amp U3 is a unity gain inverting amplifier. Gains are fixed at 0dB by R8 and R9 for the right channel, and R23 and R24 for the left channel. The non-inverting inputs of each amplifier are tied to analog ground, creating a virtual ground at the junctions of the input and feedback resistors for each channel. Signals IN_RIGHT and IN_LEFT from the previous page are AC coupled into the these amplifiers by C7 and C22. Each phase of the differential output signal pairs are impedance balanced via R10/R11 for the right channel and R25/R26 for the left, and then AC coupled via C9/C10 and C24/C25 respectively. Each phase of the differential signal pairs are then DC biased via the resistors R12/R13 and R27/R28. This DC bias of 2.94V is provided by a resistive divider comprised of R14 and R15 while C12 and C13 de-couple this bias voltage to remove ripple and noise. Because the CODEC samples the input at 256fs, R10/R11/C41 and R25/R26/C42 form low pass filters. C9, C10, C24, and C25 simply provide AC coupling into the CODEC.

AK4528 CODEC

The AKM CODEC AK4528 is a high performance 24-bit A/D-D/A device which performs anti-alias filtering, analog to digital conversion, digital to analog conversion, and digital 15/50uS de-emphasis. Although it supports sampling rates up to 96kHz, the MPX200 only supports 44.1kHz sampling.

The ADC inputs are fully differential. The input signal range is scaled to the VREF pin. Nominally, this range is defined as (0.56 x VREF) Volts peak to peak. With VREF equal to 5V and a DC input offset voltage of 2.9V The output code of the ADC is 0x7FFFFF positive full scale and 0x800000 negative full scale. The data is in 2's complement form. The input is sampled at 64fs (2.8224 MHz with fs = 44.1kHz).

Serial data is clocked in on the rising edge of the bit clock and is aligned with the second bit clock following the leading edge of each transition in the LRCLK (FS). This alignment is determined by setting the serial data interface pins to support the I2S format. The Lexichip3 receive port (SDIN0) is configured to support this format.

During power down, the ADC, DAC, digital filters, and control registers are reset by signal PWR_DWN/. This is an active low signal and is provided by the Lexichip 3. The CODEC is brought out of power down mode when the clock signals LEX_256FS, LEX_FS/, and LEX_64FS/ are stable. It these clocks are not present, then the CODEC is placed back into power down mode. R99 provides a weak pull-down for PWR_DWN/.

During power down (PDN = 0), the ADC, DAC, digital filters, and control registers are reset. Upon power up (PDN = 1), the ADC initializes after a period of 516/fs. The DAC initializes after a period of 512/fs.

The DAC uses advanced multi-bit architecture and is configured to support the I2S format. The DAC runs from a 256fs MC. The Lexichip3 generates this. Data is clocked in on the rising edge of the 64fs clock and is aligned with the second bit clock following the leading edge of each transition of the fs clock. This alignment is determined by programming the Lexichip3 Serial Transmit Port (SDOUT0) to support I2S.

Digital de-emphasis is hardwired for 44.1kHz support. De-emphasis may be turned on or off by toggling the DEM0 pin either 1 (De-emphasis is off) or a 0 (De-emphasis is on). The XD9 port of the Lexichip3 is programmed to activate or de-activate digital de-emphasis.

C43 and C44 provide power supply de-coupling of the analog supply line and voltage reference of the AK4528 while C38 de-couples the digital supply line and output buffer supply pins. R46 DC couples the analog and digital supplies together while providing a measure of isolation of digital switching currents from leaking back into the analog supply.

C39 and C40 de-couple the VCOM pin of the CODEC. This pin is the bias voltage of the ADC inputs and the DAC outputs; this voltage is equal to VA/2.

Differential to Single-Ended Output Amplifiers

The analog outputs of the CODEC are full differential with a full-scale swing of (0.54 x VREF) volts peak to peak. This output signal is centered on 2.5V. Both sections of dual op amp U4 are configured as unity gain second order low pass filters with an Fc = 93.2kHz. These filters provide summing of the differential signals for each channel into single-ended signals. R30, R31, R32, R34, R35, R36, C30, C31, and C32 form the low pass filter for the right channel (OUT_RIGHT) while R38, R39, R40, R42, R43, R44, C35, C36, and C37 comprise the low pass filter for the left channel (OUT_LEFT). Both signals are referred back to page 1 to the Output and Mute circuitry. Regulated +/-5V rails power these op amps.

Sheet 3

This sheet shows the S/PDIF input and output circuitry, the Digital Audio Receiver, Program Select rotary encoder, and the glue logic necessary to implement these functions. The S/PDIF IO is implemented in a dual RCA phono jack.

S/PDIF Input

The S/PDIF input is brought in via one half of J5. The signal is terminated into 75Ω by R129, AC coupled by C103, and amplified by U18 (74HCU04). Current limiting resistor R127 and clamping diode D6 provide input protection. R126 and R128 force one section of U18 into a semi-linear mode of operation creating a gain stage that amplifies the low-level signal at the input to a CMOS logic level. The second section of U18 provides additional buffering of this signal. R122 is a provision added to the design to bypass this gain and buffer stage for higher level signals, but this provision has not been implemented. C108 and R146 are provisions for either AC or DC coupling the ground signals of the S/PDIF connector to chassis ground via mechanical contact with the chassis. Currently, the ground signals for the S/PDIF input and output are DC coupled via R146, with C108 left unpopulated.

S/PDIF Output

The S/PDIF OUT is generated by the Lexichip3 and buffered by two gate sections of U18. These two gates of U18 are connected in parallel to increase drive capability. The resistor combination of R123-R125 forms a voltage divider that attenuates the buffered signal to 500mVp-p. D5 clamps this voltage to +/- 0.7V. The resultant signal is AC coupled by C100 and C101 to the output section of J5. C102 prevents high frequency radiation from getting out onto the cable connected to S/PDIF out.

AK4112 Digital Audio Receiver

The digital audio receiver AK4112 (U13), which delivers a serial stream in I2S format to the Lexichip3, demodulates the amplified signal from the S/PDIF input circuitry. The signals V/TX, FS96, AUTO, and ERF allow software to determine the Validity, sample rate, PCM detection status, and error status detected by U13. The chip is hardwired to 24 bit I2S format, and it may be set as a timing master or slave by toggling the DIF1 signal (SP_MASTER). This is accomplished by programming the Lexichip3 PIOB_4 pin. When this signal is low, the receiver is in master mode; when 0, the receiver is set to slave mode. The MPX200 is always operated in slave mode. The receiver is hardwired to work in parallel mode, with the master clock source set to be the internal PLL. Master clock output MCK01 is hardwired to provide 256fs locked to the recovered clock from the input data stream. During a reset cycle, provided by the signal RESET/ tied to the PDN pin, All internal analog and digital circuits become inactive, along with all clocks. All internal control registers are held in reset also.

C88 and C89 provide power supply de-coupling for the Input Buffer supply pin. C85 and C86 de-couple the digital supply to the chip. C91 and C92 de-couple the analog supply to the chip. R110 provides a bias current for the analog circuitry internal to the AK4112.

R108 and R112 are provisions for alternative DC coupling of the recovered master clock from the AK4112 and also from it's buffered equivalent as provided by U15. This was done in order to address potential radiated emissions; if the product was found to be radiating beyond acceptable limits, R108 and R112 may be replaced by ferrite beads. It was found to not be necessary, so R108 and R112 are 0 ohm resistors.

This device is run off of 3.3 Volts DC. All the I/O on this device is 5 Volt tolerant.

U15 buffers the 256fs master clock and the Serial data to the Lexichip3. This buffer provides level translation between the 3.3V logic level of the Receiver to the 5V logic level of the Lexichip3. Series resistors R109 and R111 provide protection from signal over-and under-shoot, which can cause the unit to radiate high frequencies.

LRCLK and BICK provide 44.1 kHz frame clock (LEX_FS/) and 64fs (LEX_64FS/) when the receiver is in master mode. In slave mode, these pins become inputs and Lexichip3 provides the clocks.

U15 is a 4 bit wide read buffer that provides status of the AK4112 to the Z80 processor via the internal data bus. SP_STAT/ is an address-decoded chip select for this buffer.

Address: 0x4C01
Function: Digital Audio Receiver Status

Read Only

	Digital Audio Receiver Status				
ZD Bus Bits	**7:4**	**3**	**2**	**1**	**0**
Function	N/A	Auto	FS96	ERF	Validity

Auto:
= 1: AC-3 or MPEG Detect
= 0: No Detection

FS96:
= 1: Fs >= 88.2kHz
= 0: Fs <= 54 kHz

ERF: This bit is the logical OR of PLL, Parity, Biphase, and Frame Length status.
= 1: PLL unlocked, Biphase, Parity, or Frame Length error
= 0: No error

Validity: Direct status of validity bit.

U23 is an eight bit wide read buffer that provides status of the footswitch, rotary encoder, and front panel push button switches to the Z80 processor via the internal data bus. STAT_RD/ is an address-decoded chip select for this read buffer.

Address: 0x4C00
Function: Switch Status read
Read Only

	Switch Status				
ZD Bus bits	**7**	**6**	**5**	**4**	**3:0**
Signal	Foot_Bypass/	Foot_Tap/	Switch_Row1/	Switch_Row0/	ENC_3:0

Foot_Bypass/:

= 1: Foot_Bypass/ switch is not pressed
= 0: Foot_Bypass/ switch is pressed

Foot_Tap:

= 1: Foot_Tap/ switch is not pressed
= 0: Foot_Tap/ switch is pressed

Switch_Row1/:
This is the OR of the Bypass, Edit, and Tap/Cancel front panel switches. The actual switch status is column scan dependent.

= 1: One of the above three switches is pressed
= 0: None of the above switches have been pressed.

Switch_Row0/:
This is the OR of the Store, Compressor, and Load front panel switches. The actual switch status is column scan dependent.

= 1: One of the above three switches is pressed

= 0: None of the above switches have been pressed.

ENC_3:0:
This is a straight read of the rotary encoder switch SW1.

Possible values range from 0000 to 1111.

Resistors R158 through R161 provide pull-ups for signals ENC_3:0, ensuring that a switch open condition is properly read back as a logic '1'.

R172 and C121 are provisions for either AC or DC coupling the mechanical shell of SW1 to digital ground. In this instance, it is DC coupled through R172, and C121 is left unpopulated.

Sheet 4

This sheet shows the MIDI IO, the Footswitch circuitry, power-up reset circuit, and the front panel connector. The MIDI and footswitch connectors provide DC connection of the digital ground plane to chassis ground on the back panel.

MIDI I/O

The MPX200 MIDI interface complies with the MIDI specification. It incorporates 5-pin female DIN connectors for input, thru and out (J7 and J6). J6 is shared for thru and out, according to how the Lexichip3 is programmed. MIDI INPUT is brought in on J7 and is opto-coupled for ground isolation through U24. R164 provides current limit protection of U24 and D7 provides input voltage protection by clamping the input signal to no more than 0.7V at the input of U24. The output of U24 is open collector, necessitating pull-up resistor R163. R162 and C116 form a first order low pass filter that outputs a sinusoidal equivalent of the MIDI signal. This signal is then "squared up" by U14 and presented to the MIDI UART within the Lexichip3. The filter and U14 are essential in that the opto-isolator by itself does not provide sufficient drive capability to allow daisy chaining more than two or three units together.

The MIDI OUTPUT signal is generated by the Lexichip3 and is fed to current loop driver Q4 and out J6. FB4 and FB5 and the connector shield ground connection reduce RFI. R149 provides an input bias current to Q4 while C111 and C110 reduce RFI. C109 and R147 are provisions for AC or DC coupling the mechanical shell of J6 to chassis ground. Currently this is DC coupled through R147 with C109 left unpopulated. R150 and C112 provide a de-coupled supply voltage to the MIDI cable via FB5 and pin 4 of J6.

Footswitch

The tip and ring of the footswitch ¼" phone jack (J8) connect to FOOT_TAP/ and FOOT_BYPASS/, respectively, through current-limiting resistors R168 and R170. Capacitors C123 and C124 filter out RFI. D8 and D9 help protect from over voltage or static discharge. Pull-up resistors R169 and R171 default the non-active switch state to logic high. FOOT_TAP/ and FOOT_BYPASS/ are fed to U23 on the previous page, which allows software to determine the footswitch state. C119, C120, and R166 are provisions for AC or DC coupling the mechanical shell of J8 to chassis ground. Currently this is DC coupled through R166 with C119 and C120 left unpopulated.

Power Up Reset

The +10V_UNREG voltage controls reset signaling. If the voltage at the input of the +5VD regulator (U25 sheet 7) is high enough to create a 2 volt or greater drop across the regulator, then the differential between the voltage divider R60 and R61 at the emitter of Q3 and the regulated +5VD at the base of Q3 will be enough to turn on Q3. As Q3 turns on, it charges C66 through R62 and D3. The voltage across R63 and R62 goes from 0V to about +6V. The voltage divider formed by R62 and R63 presents a TTL compatible signal to the first section of U14, at which point it becomes inverted. The second stage of U14 re-inverts it back to an active low signal, thereby generating a master reset signal for the front panel PCB, Lexichip3,

and the AK4112A. R64 is a provision for bypassing the U14 circuitry, but it is not implemented in this design.

Front Panel Connector

The front panel connector is not precisely a connector. Rather, it is a 16 x 1 row of solder pads that accept a semi-rigid flat cable that solders directly to the Main PCB and the Front Panel PCB.

FB3 and C94 provide filtering of the power supply going up to the front panel. Because of the high current demand of the front panel board, and the multiplexing nature of LED activity, FB3 provides a high impedance to switching noise that would otherwise find it's way into the supply lines to critical circuitry on the main board. C94 provides a charge reservoir to meet the demand of the current supplied to the LEDs.

SWITCH_ROW1/ is a logical OR signal of the Bypass, Edit, and Tap/Cancel switches on the front panel.

SWITCH_ROW0/ is a logical OR signal of the Store, Compressor, and Load switches on the front panel.

ROW_REG[2:0]/ are address decoded strobes for three registers on the front panel board. Further enhancement and address mapping of these strobes will be provided in the walk-through for the Front Panel PCB.

FP_RESET/ is as the name implies; an active low reset signal for the front panel registers. R130 through R138 provide edge rate limitations of the data buss and reset signal going off the main PCB. This is done to aid in RFI elimination.

ZD[7:0] is an eight bit wide data bus that functions as a control for lighting the 60 LED segments that populate the front panel. This number includes each segment of three seven-segment displays installed on the front panel.

Sheet 5

This sheet shows the Z80 processor, memory interface, user program storage, flash ROM, and chip select buffers used throughout the design.

Z80, Memory, Flash, and User Program Storage

The Z80 (U19) handles all basic system control and user interface I/O operation. Normally, the Z80 clock ZCLK is derived from the Lexichip3 M_ZCLK pin, via multiplexor U9. However, when RESET/ is asserted, before the Lexichip3 is functioning, U9 feeds a clock signal generated by U14, R81, and C74. Resistors R80 provides protection from RFI. R82 is a provision for further RFI protection; currently all that is required is a 0 ohm resistor. Also during power up reset, U9 hardwires a logic low into the RST/ pin of the Z80; this ensures that the Z80 remains at a hard reset during this time. The Z80 interrupt signal ZINT/ is pulled high by R142 to ensure that the Z80 receives no false interrupt indications during power up. This is a weak pull-up and has no effect during normal operation. The Lexichip3 master clock (CLK_IN, pin 75), is driven by an 11.2896MHz crystal. All the system software and programs are stored in 256Kx8 Flash ROM (U20). Resistors R143 through R145 ensure that the default states of ROM_A16, ROM_A17, and ROM_EN/ are inactive; ROM_A[16:17] are pulled inactive low while ROM_EN/ is pulled inactive high. The Z80's memory is a 8Kx8 SRAM (U16). User programs are stored in a 4kx8 serial EEPROM (U8). The serial data line (SERIAL_DATA) is bi-directional. R66 prevents excessive current in either the EEPROM or the Lexichip3 during power-up, when both chips might drive the line. R67 provides pull-up for this data line while R65 provides a pull-up for the EEPROM_CLK. The audio memory for the Lexichip3 is provided by 1Mx16 DRAM (U17) Located on Sheet 6. Note that all address decoding (RAM_EN/, ROM_EN/, etc.) is done within the Lexichip3. That is the primary reason the Z80 cannot function if the Lexichip3 is improperly initialized at the rising edge of RESET/.

Chip Select Buffers

U22 currently is the only chip select buffer used on the MPX200. Provision has been made to add a second one (U21) in order to separate out read from write chip selects, but this has not been implemented. Resistor R154 guarantees that chip select signal REG_SEL/ is held in an inactive state during power up. R157 merely acts as an enable for the chip itself. Resistors R139 through R141 provide RFI protection by slowing down the edge rates of signals ROW_REG_0/, ROW_REG_1/, and ROW_REG_2/.

Signal REG_SEL/ qualifies each chip select at a base address of 0x4C00 with the three address lines ZA[2:0]. In other words, whatever the binary value of ZA[2:0], if it is added to 0x4C00 the address decode for each chip select output may be derived.

ZA[2:0] Value	Address	Active Chip Select
000	0x4C00	STAT_RD/
001	0x4C01	SP_STAT/
010	0x4C02	ROW_REG_0/
011	0x4C03	ROW_REG_1/
100	0x4C04	ROW_REG_2/
101	0x4C05	Test Point E7
110	0x4C06	Test Point E6
111	0x4C07	Test Point E8

Sheet 6

This sheet shows the all the impedimenta necessary to implement DSP algorithms. These are comprised of the Lexichip3, the Audio Memory, and the clock oscillator.

Lexichip3

Configuration resistors R83-R90 set the operating mode of the Lexichip3 via the internal data bus ZD[7:0] when the RESET/ is released. The resistors set this configuration constant as follows:

	ZD Bits				
	7	**6**	**5**	**4:2**	**1:0**
Resistor	R86	R83	R87	R84, R88, R89	R85, R90
Set	0	0	0	010	00
Function	CHIP_TRST	EXTMCX	EXTM	ZCLKSEL	HADEC

CHIP_TRST: The unidirectional output buffers are enabled for normal operation.

EXTMCX2: Source MCX2 (8X XTAL Frequency) from internal PLL..

EXTMC: Generate MC (Masterclock) Internally.

ZCLKSEL: Z80 ZCLK = PLL Clock Divided by 10 (ZCLK clock-tree output).

HADEC: Select Z80 Address Map 0 (More details below).

ADDRESS MAP 0
0000 - 3FFF 16K Common ROM (ZDEC0/)
4000 - 4BFF 3K Lexichip3 Internal Decodes*
4C00 - 4FFF 1K Expansion Area (ZDEC2/)
5000 - 5FFF 4K Common SRAM (ZDEC1/) (* note 3)
6000 - 7FFF 8K Bank-Swapped SRAM (1-16 Banks, 8KB - 128KB) (ZDEC1/)
8000 - FFFF 32K Bank-Swapped ROM (1-16 Banks, 32KB - 512KB) (ZDEC0/)

If any chip on the Z80 data bus erroneously drives the data bus during RESET/, the Lexichip3 will come up in the wrong mode and the Z80 will not function properly. Therefore, during RESET/, all the relevant chip

enables must be pulled high and the Z80 must be fed clocks to allow the resistors to work as designed. Proper initialization of the system is dependent on the static state of the data bus on power up. The PLL TEST Pins are diode clamped by D4 to RESET/. This ensures that the PLL is held in an inactive state until the reset cycle ends. R68, R76, and C67 form a reference network for the PLL. R73 and R74 provide weak pull-ups for SP_MASTER/ and SPDIF_OUT respectively. R92 and R100 provide weak pull-downs for MUTE/ and DE_EMPH/ respectively. These pull-down components ensure that these signals default to their active states during power up. Resistors R69, R70, R71, and R77 provide RFI protection by slowing down the edge rates of LEX_FS/, D/A_DATA, LEX_64FS/, and LEX_256FS respectively. R72 is a provision for further RFI protection. Currently all that is required is for this component to be a 0-ohm resistor. R75 provides a DC coupled power source to the internal PLL on the Lexichip3. C68 and C69 de-couple this supply line.

Audio Memory

The audio memory for the Lexichip3 is provided by 1Mx16 DRAM (U17). However, the MPX200 only uses 8 of the available 16 data bits, with the most significant byte pulled up by R114-R121. Effectively this DRAM is being used as a 1Mx8 device. Note that all address decoding (RAM_EN/, ROM_EN/, etc.) is done within the Lexichip3. That is the primary reason the Z80 cannot function if the Lexichip3 is improperly initialized at the rising edge of RESET/. The address bus and memory control signals provided by the Lexichip3 are series terminated by resistors R93 through R98 and R101 through R107. This is done to provide RFI protection. Since the most active signals on this bus are LEX_A0 and LEX_A1, these are the ones that will cause the most emission, therefore R93 and R101 are set to 180 ohms; this value effectively slows down the edge rates of these two signals. The remaining bus signals (LEX_A[2:9]) are less active and therefore do not require edge rate reduction; R94, R96 through R98, R102, R105 and R106 are set to 0 ohms. Control signals CAS/, RAS/ and WE/ require edge rate reduction due to their high level of activity. Therefore, R95, R103, and R104 are 180 ohms.

Master Clock Generator

Y1, C76, C77, and R91 comprise the master clock generator. Signal LEX_256FS is equal to the frequency generated here (11.2896MHz). Pins 74 and 75 on the Lexichip3 are essentially the output and input of a CMOS buffer, respectively.

Sheet 7

This sheet shows the power supply scheme used in the MPX200. It includes the circuitry used to derive +10VUN, +5VD, +5VA, +3.3VD, -10VUN, and -5VA as well as the rectifier circuit coming off the power transformer secondary. Bypass capacitors C65, C70, C75, C78-C82, C87, C90, C92, C95-C99, C105-C107, C113-C115, and C117 are distributed evenly throughout the PCB and provide Digital Power de-coupling. C4, C14, C19, C33, and C55 are distributed evenly throughout the analog section of the PCB and provide power supply de-coupling of the –5VA line. C3, C15, C18, C34, and C54 are distributed evenly throughout the analog section of the PCB and provide power supply de-coupling of the +5VA line.

+10VUN and -10VUN

+10VUN is derived from the half wave rectified voltage off of the transformer. Q2, R56, R57, C58, and C60 form a capacitance multiplier. The value of C60 is effectively multiplied by the HFE of Q2, thereby providing an ultra-clean and stable ripple filter and a large reservoir for charge.
Q1, R54, R55, C57 and C59 provide filtering and reserve in a similar manner for the -10VUN supply.

+5VD

U25, D11, and C131 provide a +5 Volt regulated supply for the entire digital domain in the system. Current draw through this device is very close to the limit of U25, so a heatsink must always be in place on this device, especially if the boards are powered up outside of the enclosure. Otherwise U25 will quickly go into thermal shutdown.

+5VA

This is a filtered and ferrite bead isolated version of the +5VD supply. The current demands on this rail are barely appreciable on U25. FB1 and C64 provide noise isolation and charge reserve for this rail, which is used to power much of the analog domain in the system.

+3.3VD

U12 provides a low current supply for the AK4112 (U13). This is the only device that requires a 3.3 Volt supply voltage.

-5VA

U11 and C84 regulate the half wave rectified voltage from the power transformer to -5 Volts. This rail is used to power most of the circuitry in the analog domain in the system.

Rectifier

D10, D12, C122, C127, and C128 comprise a classic half wave rectifier circuit of the power transformer secondary AC voltage. The positive side of the rectifier (D12, C127, and C128) uses a much larger filter capacitor scheme because the current draw from this side of the rectifier is much higher than on the negative side.

Sheet 8

This sheet shows the AC power entry, power transformer, voltage select switch, front panel power switch, and chassis grounding scheme.

Power is brought onto the PCB via IEC connector J9. Digital ground is tied to the Earth ground lug of this connector via R173. This same point ties the front panel to Earth by way of a keystone bracket that mechanically attaches to a threaded stud on the front panel. C130 provides a common mode filter across the LINE and NEUTRAL AC lines.

F1 is a 250mA slo-blo fuse in series with the LINE and power switch lines (J10 and J11).

SW2 is a voltage select switch that configures the dual winding interconnections on the power transformer (T1) primary. When in the 120 position, the windings are connected in parallel and the unit is suitable for use in countries where the line voltage is between 90VAC and 120VAC. When SW2 is in the 240 position, the windings are connected in series, and the unit is suitable for use in countries where the line voltage is between 220VAC and 240VAC.

The secondary windings of T1 are wired in series, with one end tied to power ground. This boosts the other end in voltage.

Front Panel Board

Schematic Walkthrough

Sheet 1

This sheet shows the front panel connector, the Octal Registers, and the column drivers used to activate the LEDs on the front panel.

Front Panel Connector

Just like on the Main PCB, this is not strictly speaking a connector. Rather, it is a 16 x 1 array of solder pads for the mounting of a semi-rigid ribbon cable. This is the only interface scheme between the Front and Main PCBs. This cable provides power (+5VD), ground (DGND), three address decoded register strobes

(ROW_REG_[2:0]/), a reset line (FP_RESET/), two front panel switch monitoring signals (SWITCH_ROW[1:0]/) and an eight bit data bus (FRNT_D[7:0]).

Octal Registers

The purpose of these registers (U2-U4) is to latch the data value presented by the Main Board depending upon which register is selected for activation by the decoded strobes. All LEDs are electrically arranged in a 21 row by 3-column matrix. These three octal registers access the rows and columns of that matrix. U3 and U4 perform the sole function of accessing sixteen of the matrix rows, while U2 accesses the remaining five rows and the three columns. The rows are connected to the LED cathodes while the columns are connected to the LED anodes. R4-R6 provide current limiting to the bases of Q1-Q3, while R1-R3 ensure that the transistors will turn off when they become inactive.

The outputs of U4 are series terminated with resistors R20-R27. These provide limiting of the forward current through each LED. The values were chosen to limit the current sinking demands of U4. The strobe for U4 is decoded from address 0x4C02. The following table illustrates the relationship between Data Bus and LED. Column division is readily implied by the table layout as well.

Address: 0x4C02
Write Only

		Active LED Cathodes		
Active Row	**Data Bus Bit**	**COLUMN_0**	**COLUMN_1**	**COLUMN_2**
LED_ROW0/	0	D23 (Dual Stereo)	D21 (Chorus)	DISP1 (Segment F)
LED_ROW1/	1	D32 (Threshold:EDIT)	D24 (Cascade)	DISP1 (Segment G)
LED_ROW2/	2	D25 (Mono Split)	D33 (Attack)	DISP1 (Segment E)
LED_ROW3/	3	D26 (Dual Mono)	D17 (Flange)	DISP1 (Segment D)
LED_ROW4/	4	D15 (Plate)	D27 (Mix)	DISP1 (Segment C)
LED_ROW5/	5	D12 (Chamber)	DISP2 (Segment A)	DISP1 (Segment B)
LED_ROW6/	6	D29 (EQ)	D5 (R_MID)	DISP1 (Segment A)
LED_ROW7/	7	D35 (Load Button LED)	DISP2 (Segment F)	D28 (Adjust)

U3 performs in exactly the same manner as U4. The series termination resistors are designated as R12-R19. The strobe for this register is decoded from address 0x4C03. As before, the column division may be implied by the table layout.
Address: 0x4C03
Write Only

		Active LED Cathodes		
Active Row	**Data Bus Bit**	**COLUMN_0**	**COLUMN_1**	**COLUMN_2**
LED_ROW8/	0	D11 (Compressor:EDIT)	DISP2 (Segment G)	D19 (Hall)
LED_ROW9/	1	D20 (Ambience)	DISP2 (Segment E)	D30 (Lvl/Bal)
LED_ROW10/	2	D38 (Store Button LED)	DISP2 (Segment D)	D13 (Gate)
LED_ROW11/	3	D14 (Echo/Delay)	DISP2 (Segment C)	D22 (Pitch/Detune)
LED_ROW12/	4	D2 (L_MID)	DISP2 (Segment B)	DISP1 (Decimal
LED_ROW13/	5	D4 (R_CLIP)	DISP2 (Decimal Pt)	D16 (Room)
LED_ROW14/	6	DISP3 (Segment F)	D7 (Threshold:	D31 (Ratio)
LED_ROW15/	7	DISP3 (Segment G)	D18 (Rotary/Tremolo)	D34 (Release)

U2 follows the same model as U3 and U4 for FRNT_D[4:0]. The series limiting resistors are designated as R7-R11. The address decode for this strobe is 0x4C04.
Address: 0x4C04
Write Only

		Active LED		
Active Row	**Data Bus**	**COLUMN_0**	**COLUMN_1**	**COLUMN_2**
LED_ROW16/	0	DISP3 (Segment E)	D1(L Clip)	D37 (Compressor Button
LED_ROW17/	1	DISP3 (Segment D)	D36 (Edit Button LED)	D3 (L_Signal)

LED_ROW18/	2	DISP3 (Segment C)	D8 (-3dB)	D42 (Bypass Button LED)
LED_ROW19/	3	DISP3 (Segment B)	D6 (R_Signal)	D9 (-10dB)
LED_ROW20/	4	DISP3 (Segment A)	D43 (Tap/Cancel Button	D10 (-20dB)

U2 data bits FRNT_D[7:5] are active high and they activate the three columns; the columns are connected to the LED anodes, so the column signals are by necessity active high. As can be surmised, a write must be done to this address whenever the software tries to turn on any LEDs at all. The data that is latched into this register for these data bits are inverted by three of the gates inside U1. The resultant inverted bits are then used to activate three transistors (Q1-Q3) that provide enough current to light the LEDs in each column. Since these transistors are PNP types, a second inversion takes place. It could be thought of as writing a logic 1 to any of these three bits and they are current boosted to drive the LED anodes. These bits are continuously written by software in a cyclical fashion; no more than one of these bits is active at any given time.

The next table illustrates the column arrangement as it pertains to these three data bits.
Address: 0x4C04
Write Only

	Data Bus Bits (FRNT_D[7:5])		
Active Row	**Bit 5 (Column 0)**	**Bit 6 (Column 1)**	**Bit 7 (Column 2)**
LED_ROW0/	D23 (Dual Stereo)	D21 (Chorus)	DISP1 (Segment F)
LED_ROW1/	D32 (Threshold:EDIT)	D24 (Cascade)	DISP1 (Segment G)
LED_ROW2/	D25 (Mono Split)	D33 (Attack)	DISP1 (Segment E)
LED_ROW3/	D26 (Dual Mono)	D17 (Flange)	DISP1 (Segment D)
LED_ROW4/	D15 (Plate)	D27 (Mix)	DISP1 (Segment C)
LED_ROW5/	D12 (Chamber)	DISP2 (Segment A)	DISP1 (Segment B)
LED_ROW6/	D29 (EQ)	D5 (R_MID)	DISP1 (Segment A)
LED_ROW7/	D35 (Load Button LED)	DISP2 (Segment F)	D28 (Adjust)
LED_ROW8/	D11	DISP2 (Segment G)	D19 (Hall)
LED_ROW9/	D20 (Ambience)	DISP2 (Segment E)	D30 (Lvl/Bal)
LED_ROW10/	D38 (Store Button LED)	DISP2 (Segment D)	D13 (Gate)
LED_ROW11/	D14 (Echo/Delay)	DISP2 (Segment C)	D22 (Pitch/Detune)
LED_ROW12/	D2 (L_MID)	DISP2 (Segment B)	DISP1 (Decimal Pt.)
LED_ROW13/	D4 (R_CLIP)	DISP2 (Decimal Pt)	D16 (Room)
LED_ROW14/	DISP3 (Segment F)	D7 (Threshold: Compressor)	D31 (Ratio)
LED_ROW15/	DISP3 (Segment G)	D18 (Rotary/Tremolo)	D34 (Release)
LED_ROW16/	DISP3 (Segment E)	D1 (L_Clip)	D37 (Compressor Button
LED_ROW17/	DISP3 (Segment D)	D36 (Edit Button LED)	D3 (L_Signal)
LED_ROW18/	DISP3 (Segment C)	D8 (-3dB)	D42 (Bypass Button LED)
LED_ROW19/	DISP3 (Segment B)	D6 (R_Signal)	D9 (-10dB)
LED_ROW20/	DISP3 (Segment A)	D43 (Tap/Cancel Button	D10 (-20dB)

De-coupling capacitors are distributed evenly throughout the front panel PCB and provide power supply de-coupling for the 5V digital line.

Sheets 2 and 3

These sheets show the non-button related LEDs. The previous section illustrates the row-column arrangement of these LEDs. No further discussion on this page is necessary.

Sheet 4

This sheet shows the arrangement of the Front Panel buttons and their respective LEDs. The LEDs have been covered in previous sections, and no further discussion will take place here.

Front Panel Switches

Like the LEDs, the switches are arranged in a row-column scheme. The arrangement is in a 3x2 architecture. Whenever a button is pressed, a software scan of the SWITCH_ROW[1:0]/ bits at address 0x4C00 determines which button was pressed. The Column signals used by the LEDs are used here as well. Each column signal is applied to a forward biased diode (D39-D41). The cathodes of these diodes each connect to two switches. The other sides of the switches are tied in groups of three to either SWITCH_ROW0/ or SWITCH_ROW1/.

The following table illustrates the arrangement of the switch matrix.

	Column_2	**Column_1**	**Column_0**
SWITCH_ROW0/	Bypass	Edit	Tap/Cancel
SWITCH_ROW1/	Store	Compressor	Load

Resistors R28 and R29 ensure that the SWITCH_ROW[0:1]/ signals are pulled active low.

Chapter 7 - Parts List

MPX200 MAIN BOARD ASSEMBLY

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
120-14142	ADHESIVE,EPOXY,THERM COND	0.00		U10 HEATSINK
200-12169	POT,RTY,5K15AX2,7MMFL,14,15L	1.00		R1
202-09794	RESSM,RO,0 OHM,0805	19.00		R72,82,94 R96-98,102,105-108 R112,146,147,156,165 R166,172,173
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	2.00		R128,149
202-09873	RESSM,RO,5%,1/10W,10K OHM	31.00		R65,67,73,74,76 R83-90,92,99,100 R113-121,142-145 R154,157
202-09894	RESSM,RO,5%,1/10W,1M OHM	3.00		R7,22,91
202-09897	RESSM,RO,5%,1/10W,470 0HM	2.00		R54,56
202-09899	RESSM,RO,5%,1/10W,47 OHM	12.00		R130-141
202-10466	RESSM,RO,5%,1/10W,20K OHM	4.00		R12,13,27,28
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	2.00		R168,170
202-10558	RESSM,RO,5%,1/10W,47K OHM	8.00		R81,126,158-161 R169,171
202-10559	RESSM,RO,5%,1/10W,100 OHM	4.00		R6,19,68,127
202-10569	RESSM,RO,5%,1/10W,10 OHM	1.00		R75
202-10597	RESSM,RO,5%,1/10W,180 OHM	12.00		R69-71,77,80,93,95 R101,103,104,109,111
202-10892	RESSM,RO,5%,1/10W,2K OHM	2.00		R55,57
202-11041	RESSM,RO,5%,1/10W,680 OHM	1.00		R66
202-11071	RESSM,RO,5%,1/4W,75 OHM	3.00		R59,79,129
202-11072	RESSM,RO,5%,1/4W,220 0HM	3.00		R148,150,164
202-11073	RESSM,RO,5%,1/4W,270 OHM	1.00		R163
202-11683	RESSM,RO,5%,1/10W,5.1 OHM	1.00		R46
202-12836	RESSM,RO,5%,1/10W,2.7K OHM	1.00		R162
202-14619	RESSM,RO,5%,1/10W,18K OHM	1.00		R110
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	2.00		R37,41
203-10581	RESSM,RO,1%,1/10W,3.32K OHM	1.00		R15
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	3.00		R48,49,62
203-10840	RESSM,RO,1%,1/10W,750 OHM	2.00		R4,20
203-10894	RESSM,RO,1%,1/10W,340 OHM	4.00		R10,11,25,26
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	1.00		R60
203-10991	RESSM,RO,1%,1/10W,1.40K OHM	2.00		R51,52
203-11075	RESSM,RO,1%,1/10W,95.3 OHM	1.00		R123
203-11079	RESSM,RO,1%,1/10W,715 OHM	2.00		R124,125
203-11083	RESSM,RO,1%,1/10W,49.9K OHM	1.00		R63
203-11723	RESSM,RO,1%,1/10W,4.75K OHM	13.00		R8,9,14,23,24,30-32 R36,40,42-44
203-11734	RESSM,RO,1%,1/10W,4.32K OHM	2.00		R3,18
203-12167	RESSM,RO,1%,1/10W,374 OHM	2.00		R2,17
203-12198	RESSM,RO,1%,1/10W,2.15K OHM	2.00		R50,53
203-12199	RESSM,RO,1%,1/10W,316 OHM	2.00		R5,21
203-12491	RESSM,RO,1%,1/10W,205 OHM	4.00		R34,35,38,39
203-13918	RESSM,THIN,.1%,1/10W,4.02K OHM	1.00		R61
240-00611	CAP,ELEC,22uF,16V,RAD	18.00		C2,7,9,10,12,17,22 C24,25,44,50,51,57 C58,68,85,88,92
240-00614	CAP,ELEC,47uF,16V,20%,RAD	2.00		C59,60
240-06611	CAP,ELEC,1000uF,25V,20%,RAD	1.00		C122
240-06886	CAP,ELEC,4.7uF,25V,20%,AX	1.00		C84
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	2.00		C64,94
240-12330	CAPSM,ELEC,2.2uF,35V,20%	1.00		C39
240-12848	CAP,ELEC,3300uF,16V,20%,RAD	2.00		C127,128
241-00654	CAP,TANT,22uF,16V,RAD	2.00		C66,131
244-00661	CAP,MYL,.047uF,5%,RAD,BOX	2.00		C6,21
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	2.00		C29,48
244-10768	CAP,MYL,.015uF,250V,INTL,.6SP	1.00		C130
244-14616	CAP,MYL,3300pF,100V,RAD,5%,BOX	2.00		C30,37

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
245-00596	CAP,CER,.005uF,1.6KV,Z5U	1.00		C11
245-09291	CAPSM,CER,470pF,50V,COG,5%	4.00		C31,32,35,36
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	3.00		C67,100,103
245-09895	CAPSM,CER,10pF,50V,COG,10%	3.00		C1,16,74
245-10416	CAPSM,CER,1000pF,50V,COG,5%	1.00		C116
245-10544	CAPSM,CER,220pF,50V,COG,5%	4.00		C26,45,61,71
245-10561	CAPSM,CER,100pF,50V,COG,5%	9.00		C5,8,20,23,49,56 C110-112
245-10562	CAPSM,CER,150pF,50V,COG,10%	6.00		C28,47,63,73,123,124
245-10976	CAPSM,CER,47pF,50V,COG,5%	2.00		C102,104
245-11625	CAPSM,CER,33pF,50V,COG,5%	2.00		C76,77
245-11949	CAPSM,CER,1500pF,50V,COG,5%	2.00		C41,42
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	44.00		C3,4,13-15,18,19,33 C34,38,40,43,52-55 C65,69,70,75,78-82 C86,87,89-91,93 C95-99,101,105-107 C113-115,117
270-06671	FERRITE CHOKE,2.5 TURN	2.00		FB1,3
270-11545	FERRITESM,CHIP,600 OHM,0805	2.00		FB4,5
300-10509	DIODESM,1N914,SOT23	2.00		D4,7
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	7.00		D1-3,5,6,8,9
300-11599	DIODESM,GP,1N4002,MELF	3.00		D10-12
310-01007	TRANSISTOR,2N3904	1.00		Q2
310-01008	TRANSISTOR,2N3906	1.00		Q1
310-10510	TRANSISTORSM,2N3904,SOT23	1.00		Q4
310-10565	TRANSISTORSM,2N3906,SOT23	1.00		Q3
330-10523	ICSM,DIGITAL,74HCU04,SOIC	1.00		U18
330-11990	ICSM,LEXICHIP3B,100PIN,PQFP	1.00		U10
330-12452	ICSM,DIGITAL,74VHCT244,SOIC	2.00		U15,23
330-12845	ICSM,DIGITAL,74HC157,SOIC	1.00		U9
330-14244	ICSM,DIGITAL,74VHCT138,SOIC	1.00		U22
330-14642	ICSM,DIGITAL,74VHCT14,SOIC	1.00		U14
340-10877	ICSM,LIN,4556,DUAL OP AMP,SOIC	1.00		U6
340-11573	ICSM,LIN,NJM4580,DUALOPAMP,SOP	4.00		U1-4
340-11576	ICSM,LIN,7905,-5V REG,TO263	1.00		U11
340-13540	IC,LINEAR,LM2940C,5V REG,TO220	1.00		U25
340-14643	ICSM,LIN,3.3V REG,LOPWR,SOT23	1.00		U12
345-14649	ICSM,RCVR,AK4112,24B,96k,VSOP	1.00		U13
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	1.00		U7
350-10545	ICSM,SRAM,8KX8,80NS,SOIC,50uA	1.00		U16
350-12637	ICSM,DRAM,1MX16,70NS,SOJ	1.00		U17
350-14158	ICSM,EEPROM,24C32,32K,SER,SOIC	1.00		U8
350-14748	ICSM,FLASH,2M,MPX200,V1.02	1.00		U20
355-12045	ICSM,CODEC,AK4528,24B,96k,VSOP	1.00		U5
365-09883	ICSM,uPROC,Z80,CMOS,10MHz,QFP	1.00		U19
375-02247	IC,OPTO-ISOLATOR,6N138	1.00		U24
390-12361	CRYSTALSM,11.2896MHz,PAR,HC49	1.00		Y1
440-14647	FUSE,5X20MM,SLO-BLO,.250A	1.00		F1
451-14648	SW,SL,2P2T,115/230V-SEL,PCRA	1.00		SW2
452-14617	SW,RTY,ENC,16POS,4BIT,GRY,20MM	1.00		SW1
470-14727	XFORMER,PCMT,115/230V,10V,1.9A	1.00		T1
510-07888	CONN,AC,3MC,PCRA,IEC,10A	1.00		J9
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	2.00		J6,7
510-11087	1/4"PH JACK,PCRA,3C,SW-TR,G,FT	2.00		J4,8
510-11548	1/4"PH JACK,PCRA,2C,SW-T,G,FT	3.00		J1-3
510-13149	CONN,RCA,PCRA,1FCGX2V,WH/RED,G	1.00		J5
600-02227	FUSE CLIP,20MM,PC	2.00		F1
630-14670	WSHR,FL,#4CLX1/4ODX1/32,NYL	2.00		J9 (AC CONN) BOTTOM OF PCB
640-07899	SCRW,4-40X1/2,PHN,PH,ZN	2.00		J9 (AC CONN) BOTTOM OF PCB
643-01732	NUT,4-40,KEP,ZN	2.00		J9 (AC CONN)
650-03970	POPRVT,1/8X1/8,REG PROT HD,SS	1.00		KEY1
675-09102	WIRE,22G,BLU,3.5",.187QDC/ST	1.00		J10
675-09103	WIRE,22G,BRN,3.5",.187QDC/ST	1.00		J11
675-14137	WIRE,18G,GRN/YEL,7",#6RING/SS	1.00		AC CONN TO FP
701-14147	BRACKET,KEYSTONE,633,.140DX2	1.00		KEY1
704-14132	HEATSINK,TO220,.75X.5X.5"H	1.00		U10

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
740-11287	LABEL,S/N,PCB,PRINTED	1.00		
740-14690	LABEL,FUSE,CAUTION,250MA/250V	1.00	•03/07/01	PCB NEAR FUSE

MPX200 FRONT PANEL BOARD ASSEMBLY

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	2.00		R28,29
202-09871	RESSM,RO,5%,1/10W,1K OHM	3.00		R1-3
202-10891	RESSM,RO,5%,1/10W,270 OHM	21.00		R7-27
202-11041	RESSM,RO,5%,1/10W,680 OHM	3.00		R4-6
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	4.00		C1-4
300-10509	DIODESM,1N914,SOT23	3.00		D39-41
310-10422	TRANSISTORSM,2N4403,SOT23	3.00		Q1-3
330-10522	ICSM,DIGITAL,74HC04,SOIC	1.00		U1
330-10536	ICSM,DIGITAL,74HC273,SOIC	3.00		U2-4
430-07325	LED,T1,RED,LITEON	1.00		D37
430-07326	LED,T1,GRN,LITEON	4.00		D35,36,38,43
430-14638	LED,T1,YEL,LITEON	1.00		D42
430-14644	LED,DSPLY,7SEG,RED,1DIG,.56"	3.00		DISP1-3
430-14673	LED,GRN,RECT,.197X.079	23.00		D2,3,5,6,12-30
430-14674	LED,YEL,RECT,.197X.079	1.00		D7
430-14675	LED,RED,RECT,.197X.079	10.00		D1,4,8-11,31-34
453-12166	SW,PBM,1P1T,6MMSQ,250GF	6.00		SW1-6
680-14618	CABLE,RIB,24-26AWG,16CX.1,2"L	1.00		J1

MPX200 MECHANICAL ASSEMBLY

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
100-01759	CHEM,HEATSINK COMP,SILICONE	0.00		REGULATOR U25
120-02023	ADHESIVE,SILICONE,RTV,CLEAR	0.00		SIDE PANELS
454-11095	SW,ROCKER,1P2T,6A@250,VERTSLIM	1.00		
550-11929	KNOB,.69D,6MM/FL,BLK,LINE	1.00		
550-11931	BUTTON,.24X.64,BLK,W/LT PIPE	6.00		
550-14168	KNOB,.85D,6MM/FL,BLK	1.00		
630-14688	SPCR,4-40X1-1/4,1/4HEX,NYL	3.00		MAIN BD
635-12831	SPCR,.14IDX.25ODX.375L,AL	3.00		FP BD TO FP
640-02377	SCRW,4-40X1/4,PNH,PH,BLK	5.00		SPCRS TO COVER (3); COVER TO FP (2)
640-02812	SCRW,4-40X3/8,PNH,PH,BLK	2.00		AC CONN TO COVER(1); REGULATOR TO CVR (1)
640-14115	SCRW,4-40X3/16,PNH,PH,NYL	3.00		SPCRS TO MAIN BD
641-10989	SCRW,TAP,AB,4X3/8,PNH,PH,BZ	5.00		COVER TO SIDES (4); RCA CONN (1)
641-12759	SCRW,TAP,AB,#2X1/4,PNH,PH,BZ	4.00		DIN CONN
643-01732	NUT,4-40,KEP,ZN	4.00		KEYSTONE TO FP (1); FP BD TO FP (3)
643-01732	NUT,4-40,KEP,ZN	2.00		AC CONN (1); REGULATOR U25 (1)
700-14724	COVER,MPX200	1.00		
702-14177	COVER,PROTECTIVE,PS,4.10X4.10	1.00		INSIDE TOP COVER.
702-14640	PANEL,SIDE,1.71X5.42,ABS	1.00		LEFT SIDE PANEL
702-14687	COVER,PROT,PS,4.1X4.1,W/HOLES	1.00		COVER, BOTTOM
702-14733	PANEL,FRONT,MPX200	1.00		
702-14744	PANEL,SIDE,1.71X5.42,ABS,HOLE	1.00		RIGHT SIDE PANEL
703-14736	LENS,8.45X1.10,MPX200	1.00		
720-14686	TAPE,FOAM,.032X.25X3,BLK	2.00		FRONT PANEL
720-14686	TAPE,FOAM,.032X.25X3,BLK	2.00		RIGHT SIDE PANEL
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1.00		INSIDE FP NEAR PWRSW
740-08558	LABEL,TUV CERTIFIED,BAYERN	1.00		OUTSIDE BOTTOM COVER
740-09538	LABEL,S/N,CHASSIS,PRINTED	1.00		REAR COVER
740-13573	LABEL,MFR ID,.9X.25,SILVER	1.00		REAR COVER

MPX200 POWER CORD OPTIONS

PART NO.	DESCRIPTION	QTY	EFFECTIVE • INACTIVE	REFERENCE
680-09149	CORD,POWER,IEC,10A,2M,NA,SVT	1.00		
680-08830	CORD,POWER,IEC,6A,2M,EURO	1.00		
680-10093	CORD,POWER,IEC,5A,2M,UK	1.00		

PART NO.	DESCRIPTION	QTY	EFFECTIVE •	INACTIVE	REFERENCE
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1.00			
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1.00			
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1.00			
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1.00			
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1.00			

MPX200 SHIPPING MATERIALS

PART NO.	DESCRIPTION	QTY	EFFECTIVE •	INACTIVE	REFERENCE
070-14692	GUIDE,USER,ERRATA,MPX200	1.00		•03/27/01	
070-14738	GUIDE,USER,MPX200	1.00			
730-14181	INSERT,FOAM,ENDCAP,1UX5.5	2.00			
730-14720	BOX,22X8X4,DSPLY,MPX200	1.00			
750-14739	CD,LIT,MULTI-LANG,MPX200	1.00			

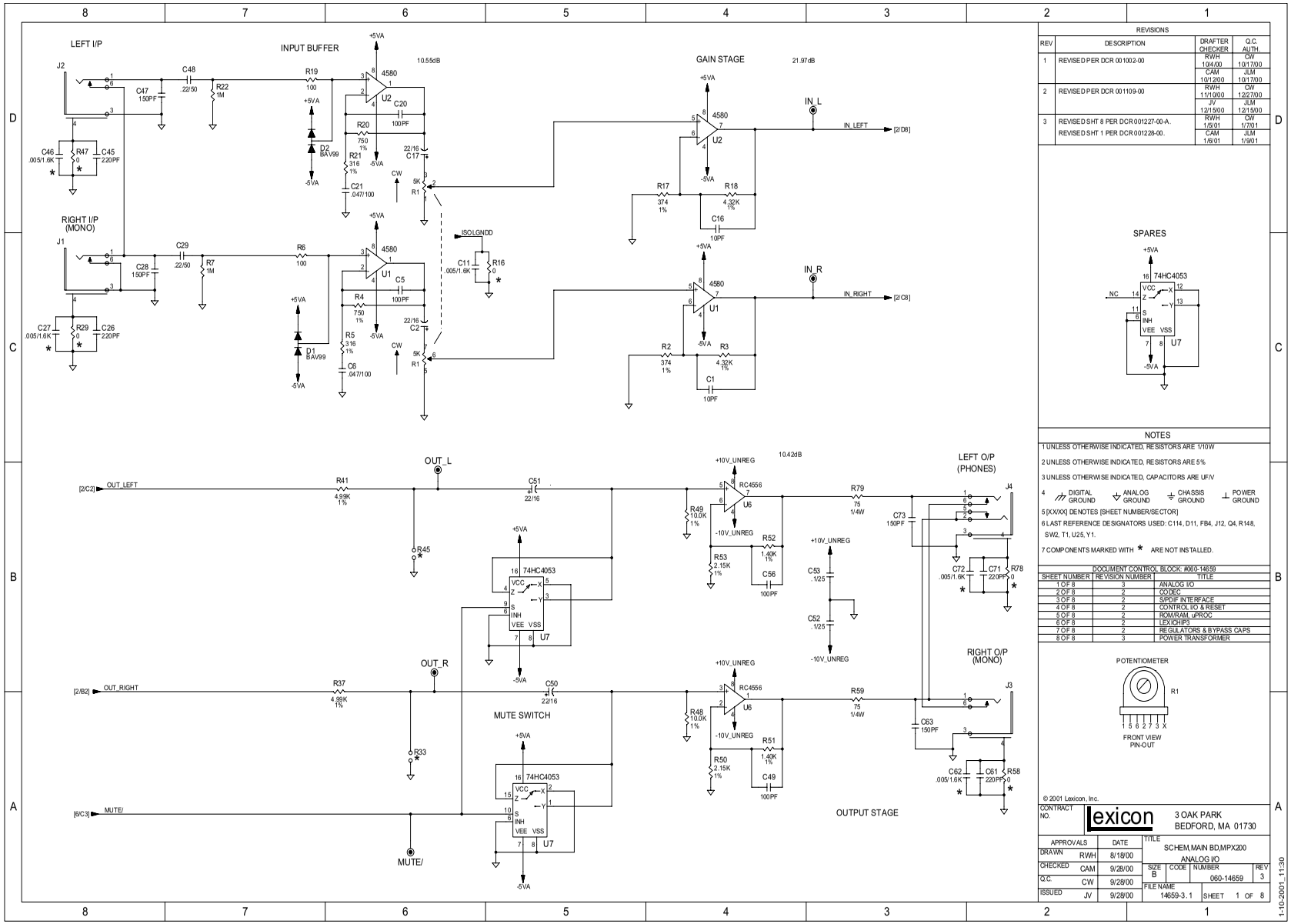
Chapter 8 Schematics and Drawings

Schematics:

060- 14659 SCHEM,MAIN BD,MPX200
060- 14669 SCHEM,FP BD,MPX200

Drawings:

Component Layout - Main Board, MPX200
Component Layout - Front Panel Board,MPX200
080-14718 ASSY DWG,CHASSIS,MPX200
080-14719 ASSY DWG,SHIPMENT,MPX200



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REVISED PER DCR 001002-00	RWH 1/04/00	CW 1/017/00
		CAM 10/12/00	JLM 10/17/00
2	REVISED PER DCR 001109-00	RWH 11/1/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00
3	REVISED SHT 8 PER DCR 001227-00-A. REVISED SHT 1 PER DCR 001228-00.	RWH 1/5/01	CW 1/7/01
		CAM 1/6/01	JLM 1/9/01

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C114, D11, FB4, J12, Q4, R148, SW2, T1, U25, Y1.

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

DOCUMENT CONTROL BLOCK: #060-14659

SHEET NUMBER	REVISION NUMBER	TITLE
1 OF 8	3	ANALOG I/O
2 OF 8	2	CODEC
3 OF 8	2	S/PDIF INTERFACE
4 OF 8	2	CONTROL I/O & RESET
5 OF 8	2	ROM/RAM, uPROC
6 OF 8	2	LEXICHIP3
7 OF 8	2	REGULATORS & BYPASS CAPS
8 OF 8	3	POWER TRANSFORMER

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

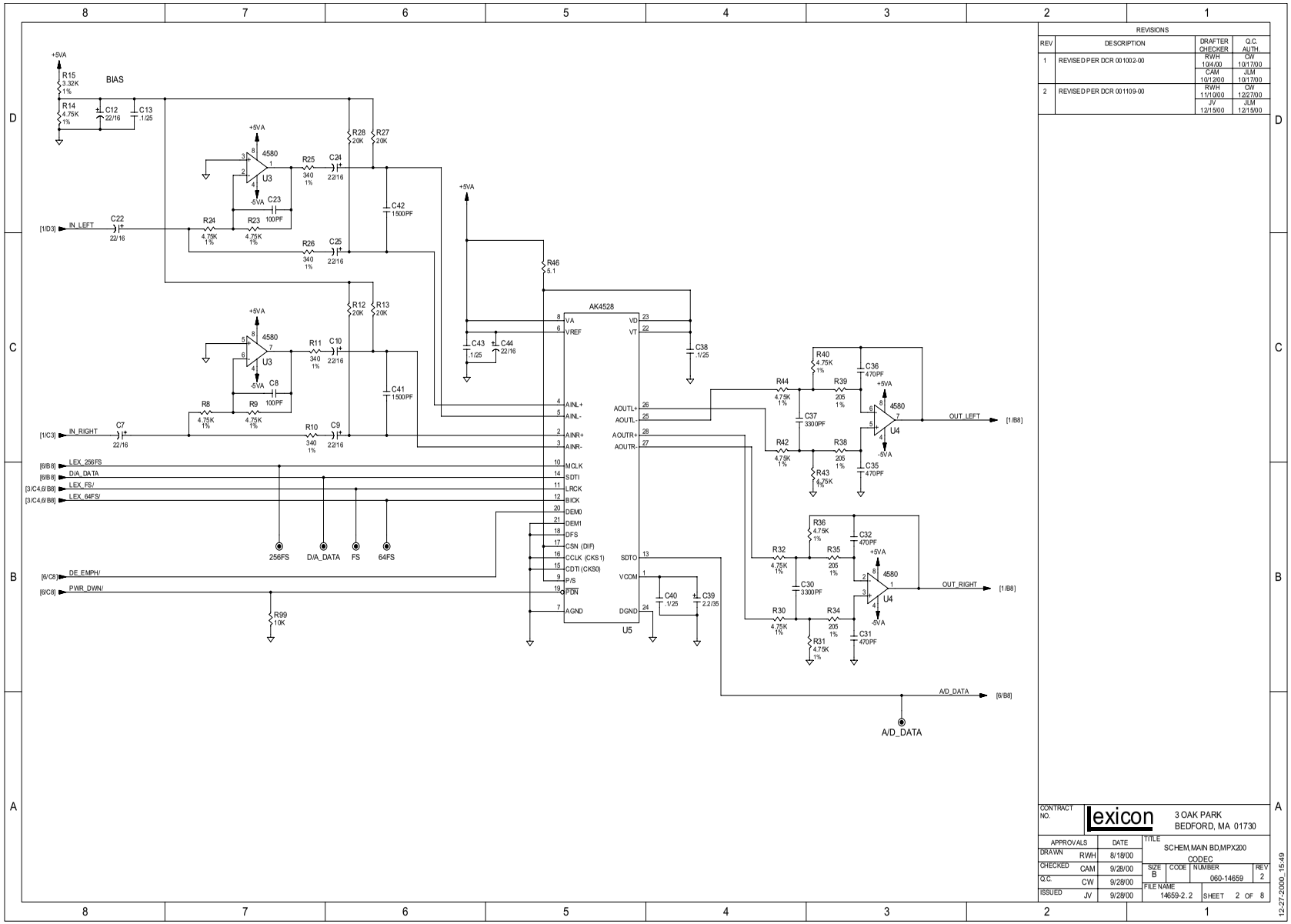
TITLE: SCHEM,MAIN BD,MPX200 ANALOG I/O

SIZE	CODE	NUMBER	REV
B		060-14659	3

FILE NAME: 14659-3.1 SHEET 1 OF 8

1-10-2001 11:30

Your Notes:



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		CAM 10/12/00	JLM 10/17/00
2	REVISED PER DCR 001109-00	RWH 11/10/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

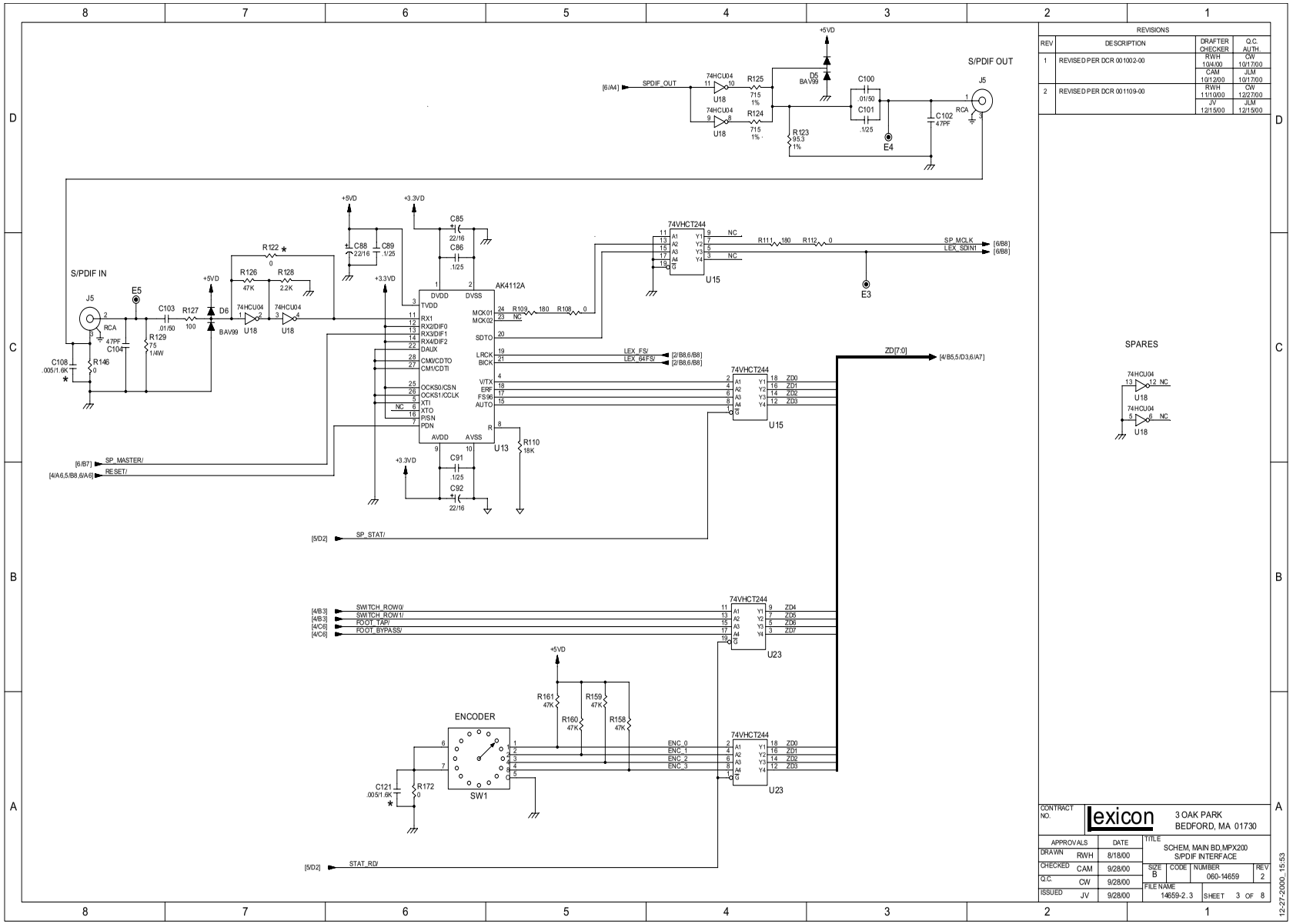
TITLE: SCHEM,MAIN BD,MPX200 CODEC

SIZE	CODE	NUMBER	REV
B		060-14659	2

FILE NAME: 14659-2.2 SHEET 2 OF 8

12-27-2000 15:49

Your Notes:



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		CAM 10/12/00	JLM 10/17/00
2	REVISED PER DCR 001109-00	RWH 11/10/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

TITLE: SCHEM, MAIN BD,MPX200 S/PDIF INTERFACE

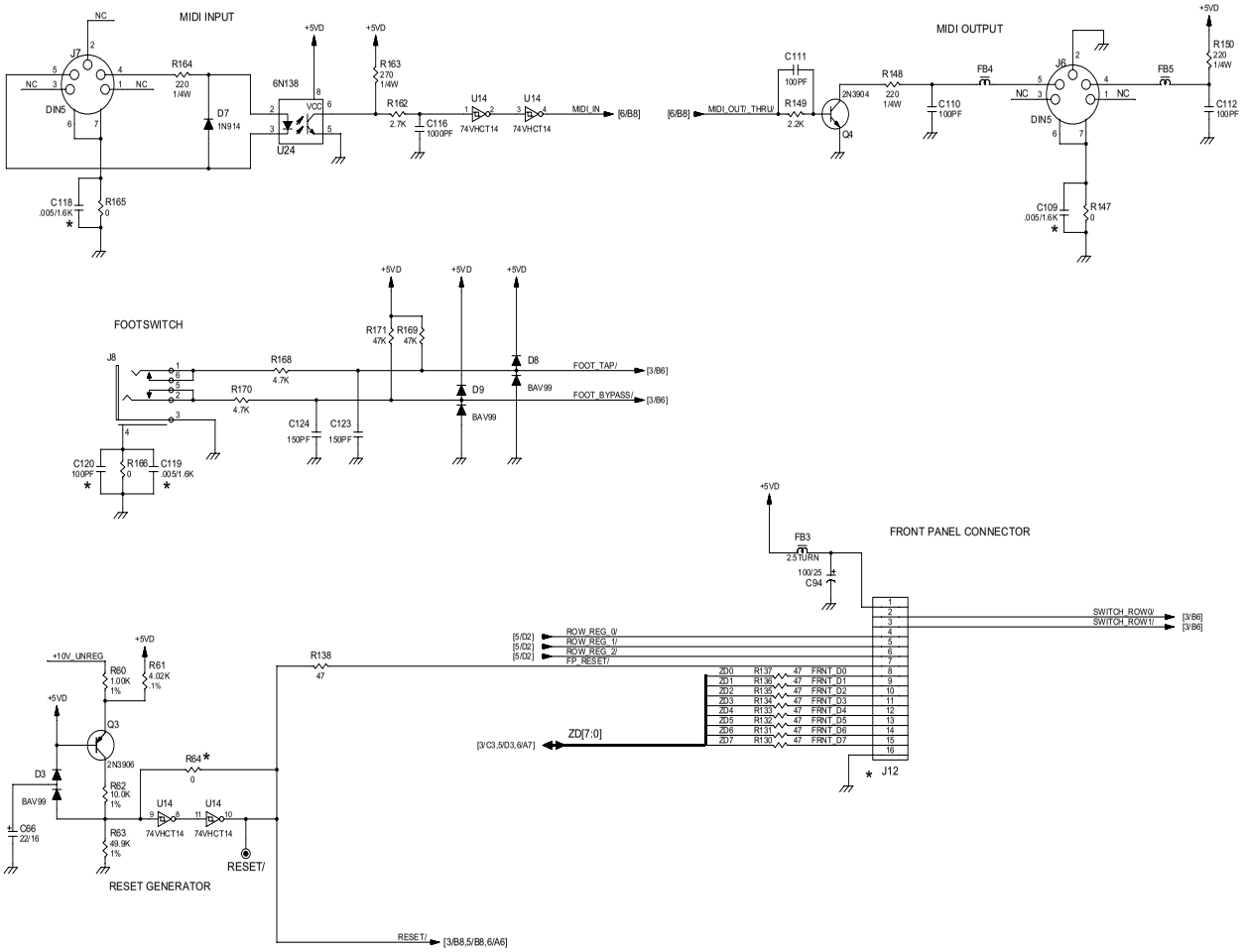
SIZE	CODE	NUMBER	REV
B		060-14659	2

FILE NAME: 14659-2.3

SHEET 3 OF 8

12-27-2000 15:53

Your Notes:



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2	REVISED PER DCR 001109-00	RWH 11/10/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

TITLE: SCHEM,MAIN BD,MPX200 CONTROL I/O & RESET

SIZE	CODE	NUMBER	REV
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FILE NAME: 14659-2.4 SHEET 4 OF 8

12-27-2000 15:53

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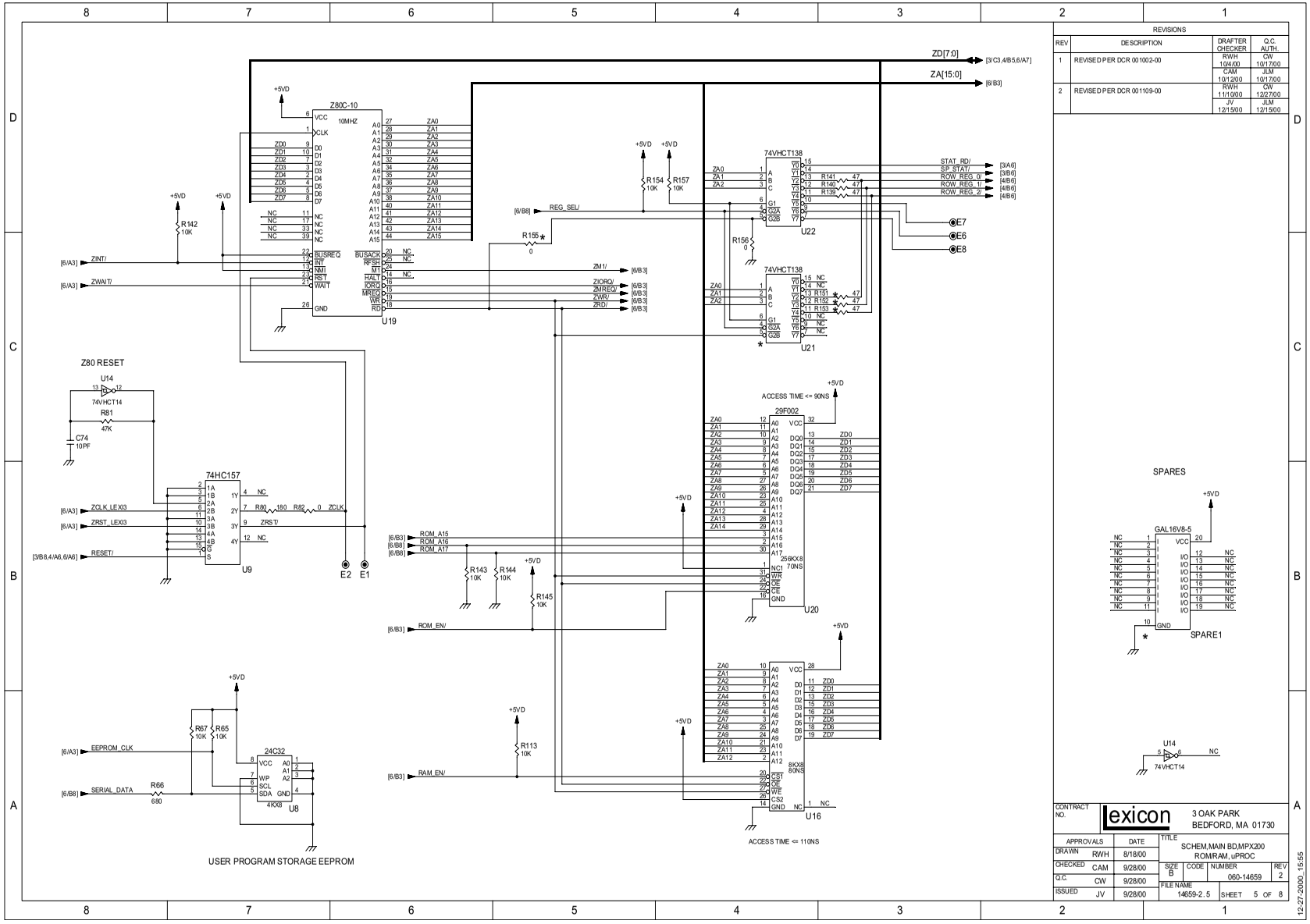
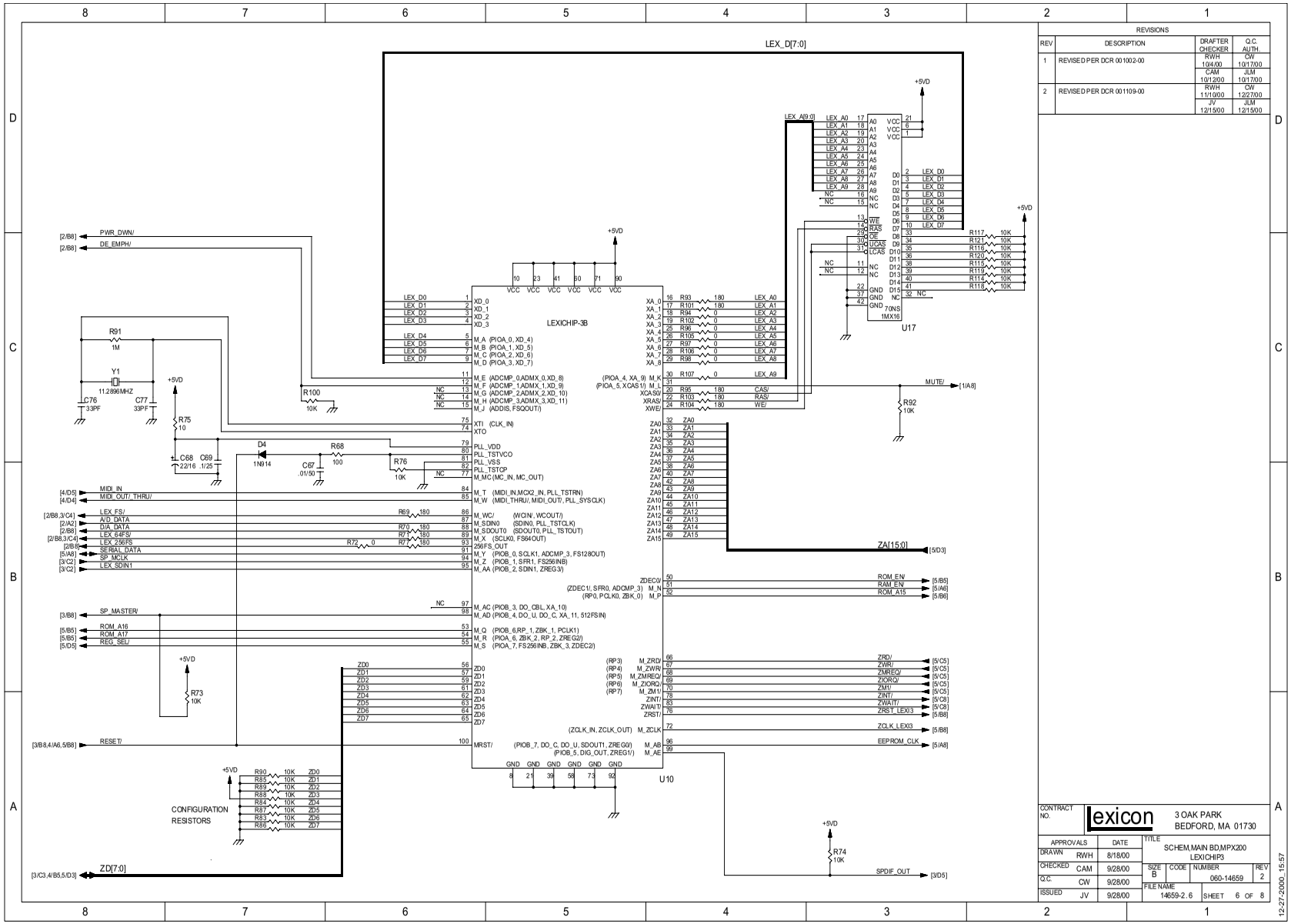

ZD[7:0]
[3/C3,4/B5,6/A7]
ZA[15:0]
[6/B3]
Z80C-10
10MHZ
U19
74VHCT138
U22
U21
REG_SEL/
[6/B8]
STAT_RD/
SP_STAT/
ROW_REG_0/
ROW_REG_1/
ROW_REG_2/
[3/A6]
[3/B6]
[4/B6]
[4/B6]
[4/B6]
E7
E6
E8
ZINT/
ZWAIT/
[6/A3]
ZM1/
ZIORQ/
ZMREQ/
ZWR/
ZRD/
[6/B3]
Z80 RESET
U14
74VHCT14
R81
47K
C74
10PF
74HC157
U9
ZCLK_LEXI3
ZRST_LEXI3
RESET/
[3/B8,4/A6,6/A6]
E2
E1
ACCESS TIME <= 90NS
29F002
U20
ROM_A15
ROM_A16
ROM_A17
[6/B8]
ROM_EN/
[6/B3]
R143
R144
R145
10K
8KX8 70NS
8KX8 80NS
U16
RAM_EN/
R113
ACCESS TIME <= 110NS
EEPROM_CLK
SERIAL_DATA
R67
R65
R66
680
24C32
4KX8
U8
USER PROGRAM STORAGE EEPROM
SPARES
GAL16V8-5
SPARE1
U14
74VHCT14
NC
REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1
REVISED PER DCR 001002-00
RWH 1/04/00
CW 10/17/00
CAM 10/12/00
JLM 10/17/00
2
REVISED PER DCR 001109-00
RWH 1/10/00
CW 12/27/00
JV 12/15/00
JLM 12/15/00
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS
DATE
DRAWN
RWH
8/18/00
CHECKED
CAM
9/28/00
Q.C.
CW
9/28/00
ISSUED
JV
9/28/00
TITLE
SCHEM,MAIN BD,MPX200
ROM/RAM, uPROC
SIZE
B
CODE
NUMBER
060-14659
REV
2
FILE NAME
14659-2.5
SHEET
5 OF 8
12-27-2000 15:55

Your Notes:



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REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
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		CAM 10/12/00	JLM 10/17/00
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		JV 12/15/00	JLM 12/15/00

CONTRACT NO.

lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

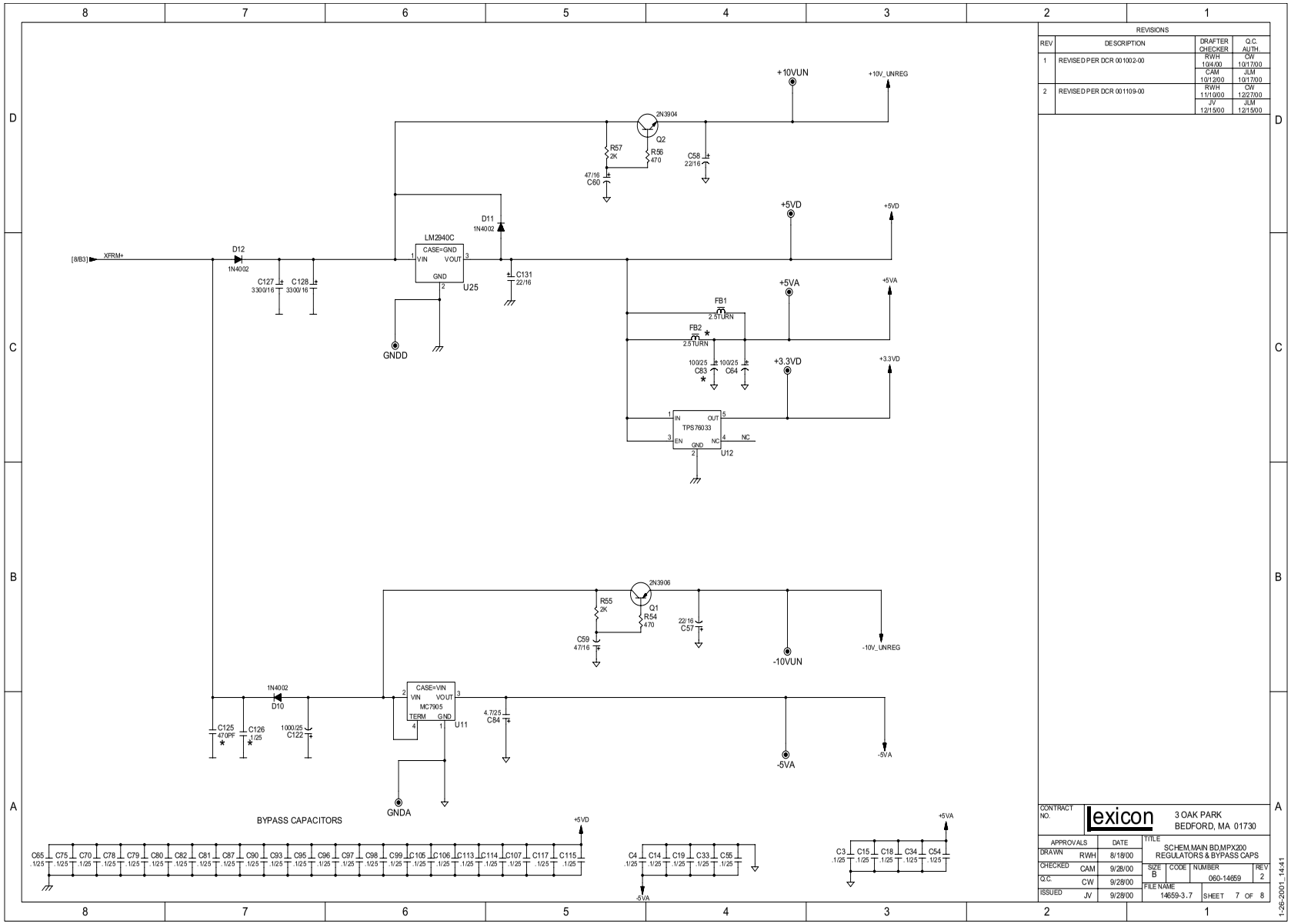
TITLE: SCHEM,MAIN BD,MPX200
LEXICHIP3

SIZE	CODE	NUMBER	REV
B		060-14659	2

FILE NAME: 14659-2.6 SHEET 6 OF 8

12-27-2000 15:57

Your Notes:



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REVISED PER DCR 001002-00	RWH 10/4/00	CW 10/17/00
		CAM 10/12/00	JLM 10/17/00
2	REVISED PER DCR 001109-00	RWH 11/10/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

TITLE
SCHEM,MAIN BD,MPX200
REGULATORS & BYPASS CAPS

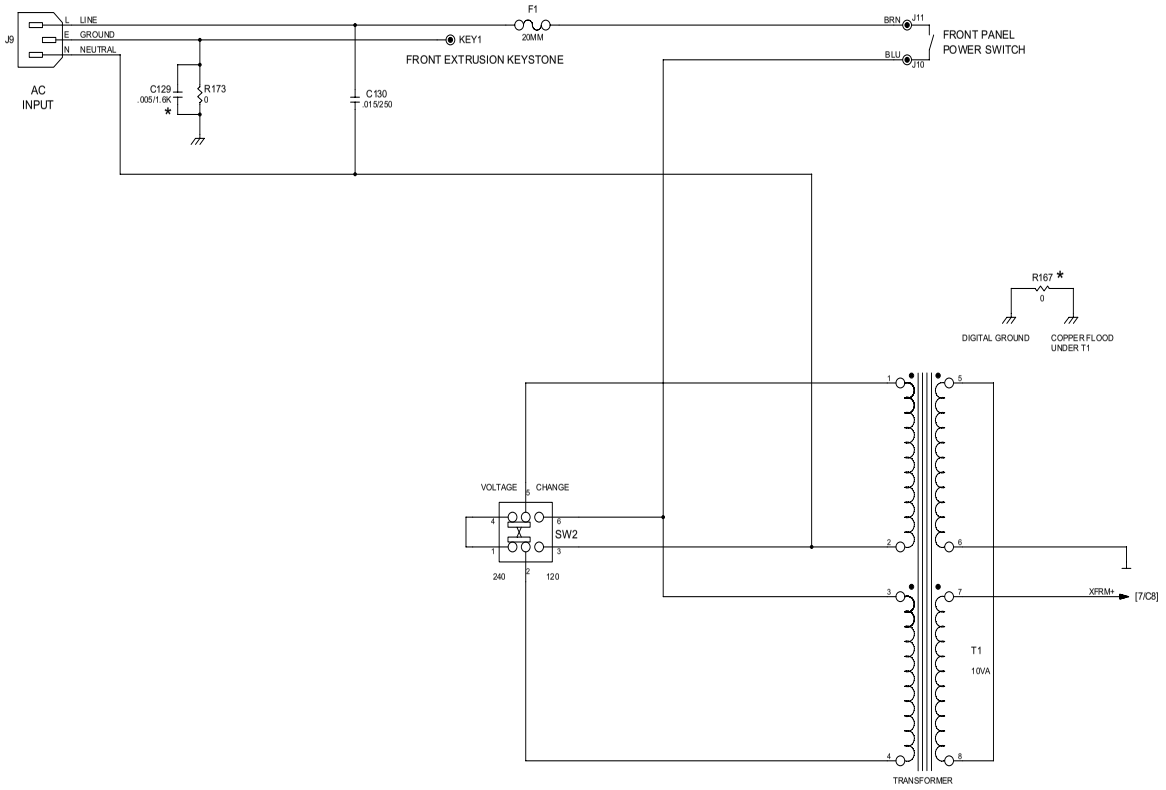
SIZE	CODE	NUMBER	REV
B		060-14659	2

FILE NAME 14659-3.7

SHEET 7 OF 8

1-26-2001_14:41

Your Notes:



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		CAM 10/12/00	JLM 10/17/00
2	REVISED PER DCR 001109-00	RWH 11/10/00	CW 12/27/00
		JV 12/15/00	JLM 12/15/00
3	REVISED PER DCR 001227-00-A	RWH 1/5/01	CW 1/7/01
		CAM 1/6/01	JLM 1/9/01

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/18/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

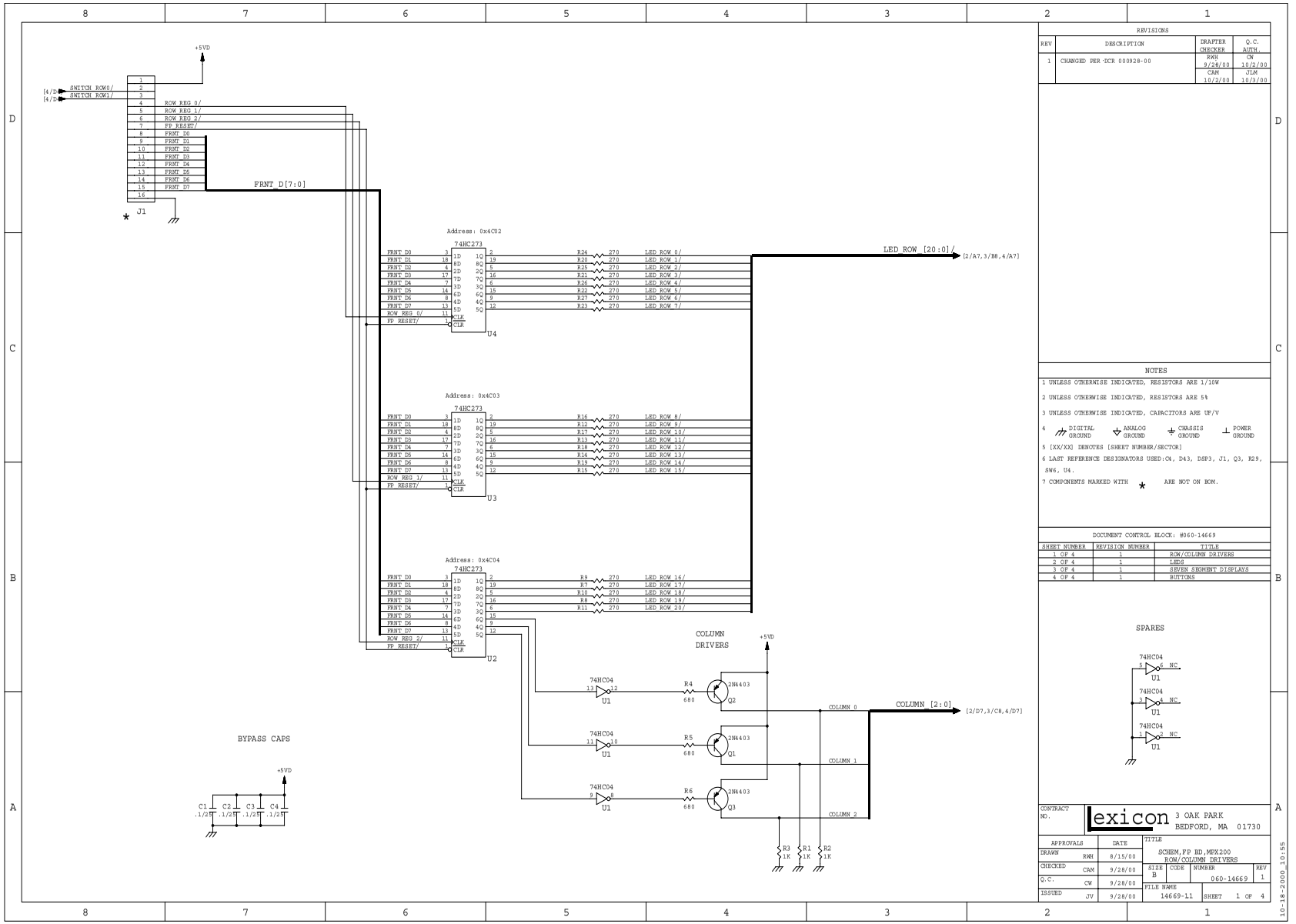
TITLE
SCHEM,MAIN BD,MPX200
POWER TRANSFORMER

SIZE	CODE	NUMBER	REV
B		060-14659	3

FILE NAME 14659-3.8 SHEET 8 OF 8

1-10-2001_11:31

Your Notes:



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REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 000928-00	RWH 9/28/00	CW 10/2/00
		CAM 10/2/00	JLM 10/3/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED:C4, D43, DSP3, J1, Q3, R29, SW6, U4.

7 COMPONENTS MARKED WITH * ARE NOT ON BOM.

DOCUMENT CONTROL BLOCK: #060-14669

SHEET NUMBER	REVISION NUMBER	TITLE
1 OF 4	1	ROW/COLUMN DRIVERS
2 OF 4	1	LEDS
3 OF 4	1	SEVEN SEGMENT DISPLAYS
4 OF 4	1	BUTTONS

SPARES

74HC04 U1 NC

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/15/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

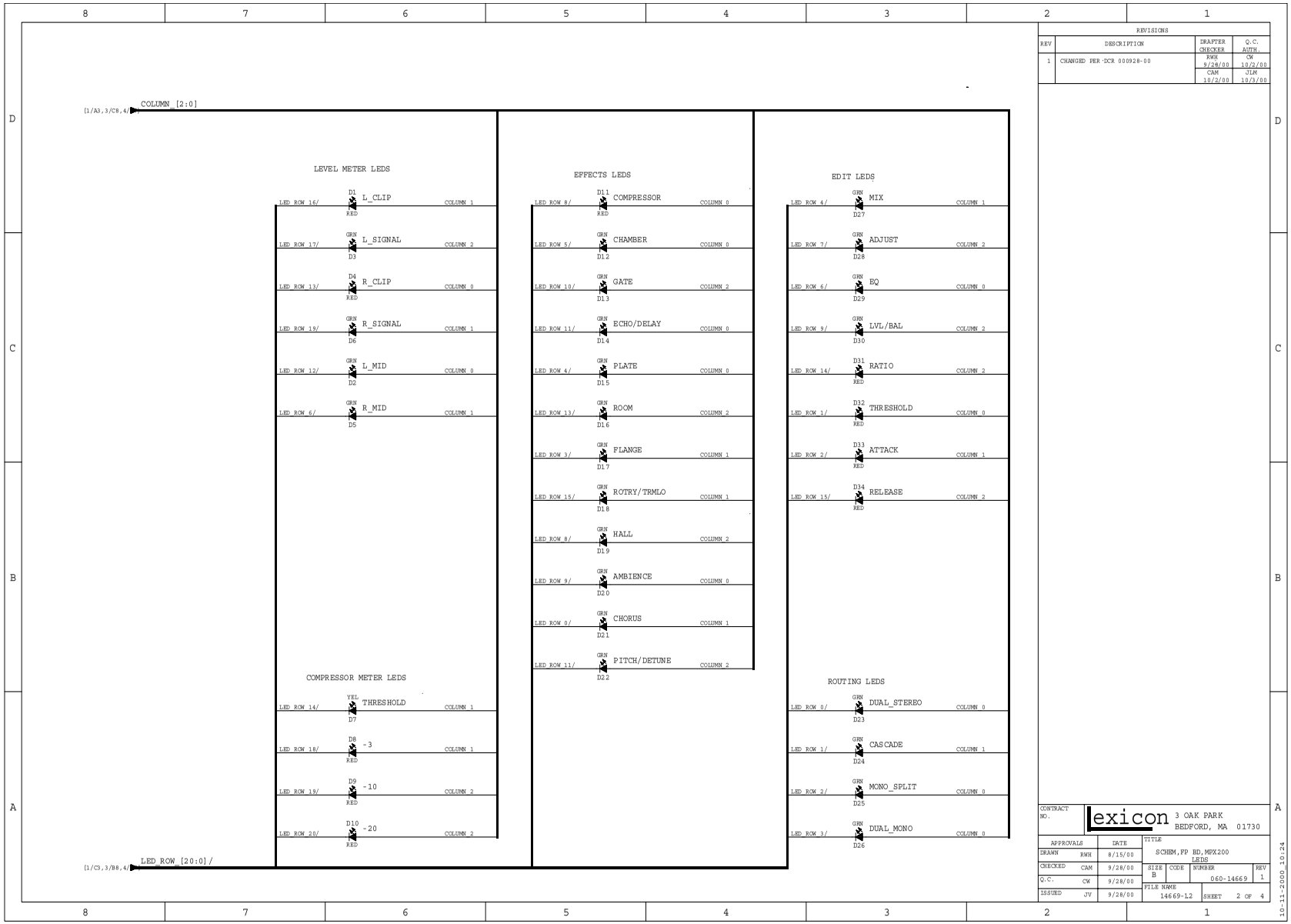
TITLE: SCHEM,FP BD,MPX200 ROW/COLUMN DRIVERS

SIZE B | CODE | NUMBER 060-14669 | REV 1

FILE NAME 14669-L1 | SHEET 1 OF 4

10-18-2000 10:55

Your Notes:



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REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
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		CAM 10/2/00	JLM 10/3/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/15/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

TITLE: SCHEM,FP BD,MPX200 LEDS

SIZE B | CODE | NUMBER 060-14669 | REV 1

FILE NAME 14669-L2 | SHEET 2 OF 4

10-11-2000 10:24

Your Notes:

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 000928-00	RWH 9/28/00 CAM 10/2/00	CW 10/2/00 JLM 10/3/00

[1/A3,2/D7,4/E3] COLUMN_[2:0]

[1/C3,2/A7,4/A5] LED_ROW_[20:0]/

MOST SIGNIFICANT DIGIT

DISP1

COLUMN_2		3	ANODE1
LED_ROW_0/		9	F
LED_ROW_1/		10	G
LED_ROW_2/		1	E
LED_ROW_3/		2	D
		8	ANODE2
LED_ROW_12/		5	DP
LED_ROW_4/		4	C
LED_ROW_5/		6	B
LED_ROW_6/		7	A

MIDDLE DIGIT

DISP2

COLUMN_1		3	ANODE1
LED_ROW_7/		9	F
LED_ROW_8/		10	G
LED_ROW_9/		1	E
LED_ROW_10/		2	D
		8	ANODE2
LED_ROW_13/		5	DP
LED_ROW_11/		4	C
LED_ROW_12/		6	B
LED_ROW_5/		7	A

LEAST SIGNIFICANT DIGIT

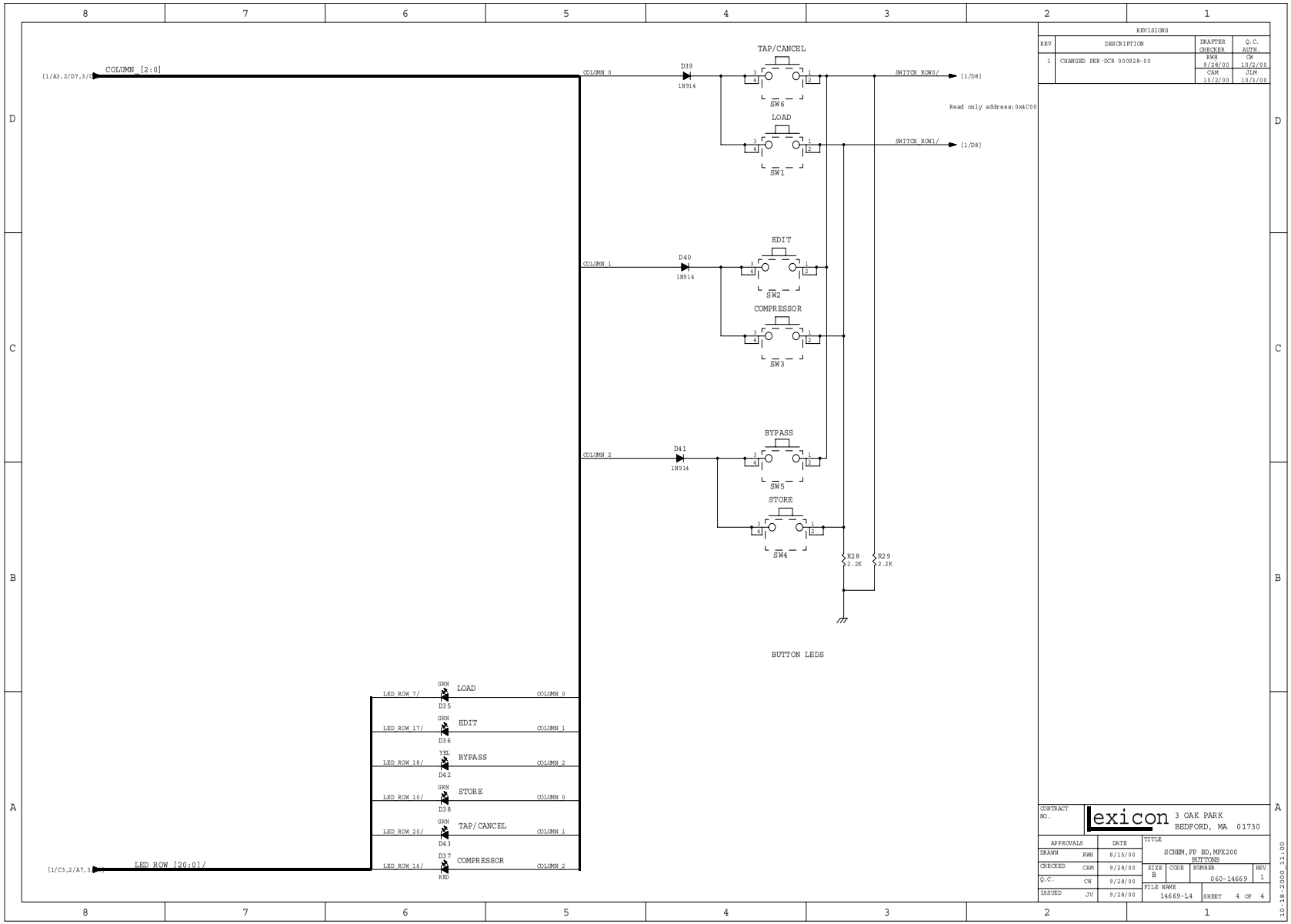
DISP3

COLUMN_0		3	ANODE1
LED_ROW_14/		9	F
LED_ROW_15/		10	G
LED_ROW_16/		1	E
LED_ROW_17/		2	D
		8	ANODE2
	NC	5	DP
LED_ROW_18/		4	C
LED_ROW_19/		6	B
LED_ROW_20/		7	A

CONTRACT NO.	lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE	
DRAWN RWH	8/15/00	SCHEM,FP BD,MPX200 SEVEN SEGMENT DISPLAYS	
CHECKED CAM	9/28/00	SIZE B / CODE / NUMBER 060-14669	REV 1
Q.C. CW	9/28/00		
ISSUED JV	9/28/00	FILE NAME 14669-L3	SHEET 3 OF 4

10-18-2000 10:57

Your Notes:



REVISIONS				
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.	
1	CHANGED PER DCR 000928-00	RWH 9/28/00	CW 10/2/00	
		CAM 10/2/00	JLM 10/3/00	

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	RWH	8/15/00
CHECKED	CAM	9/28/00
Q.C.	CW	9/28/00
ISSUED	JV	9/28/00

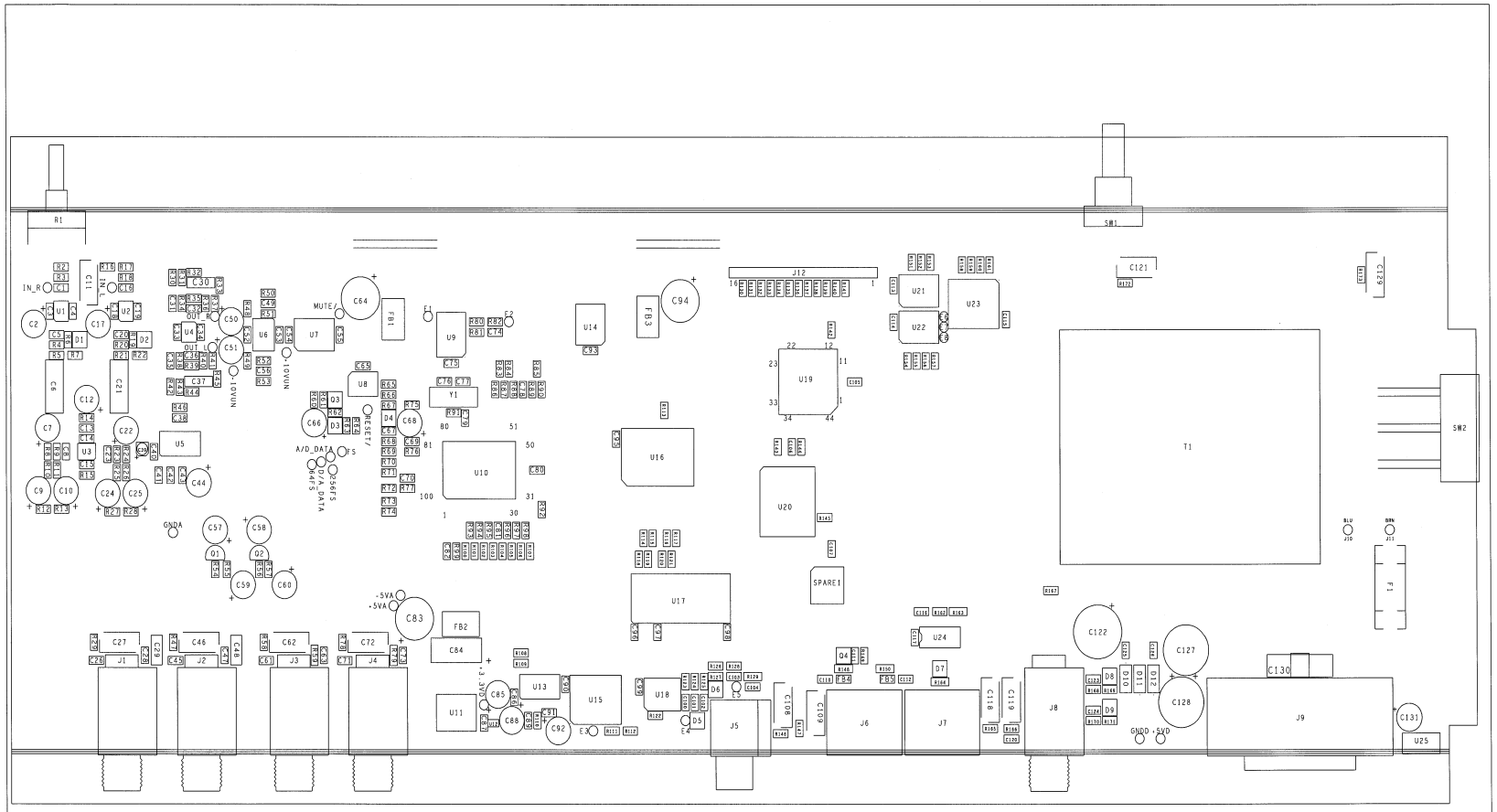
TITLE: SCHEM,PP BD,MPX200 BUTTONS

SIZE	CODE	NUMBER	REV
B		060-14669	1

FILE NAME: 14669-14 SHEET 4 OF 4

10-18-2000 11:00

Your Notes:



exicon

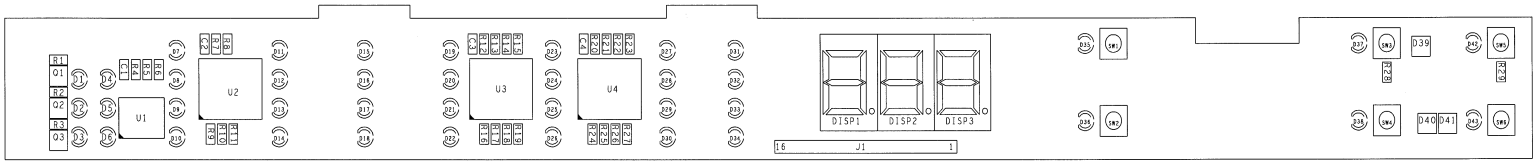
PC BD,MAIN,MPX200 COMPONENT LAYOUT

REV 4

SCALE N/A

SHEET 1 OF 1

Your Notes:



exicon

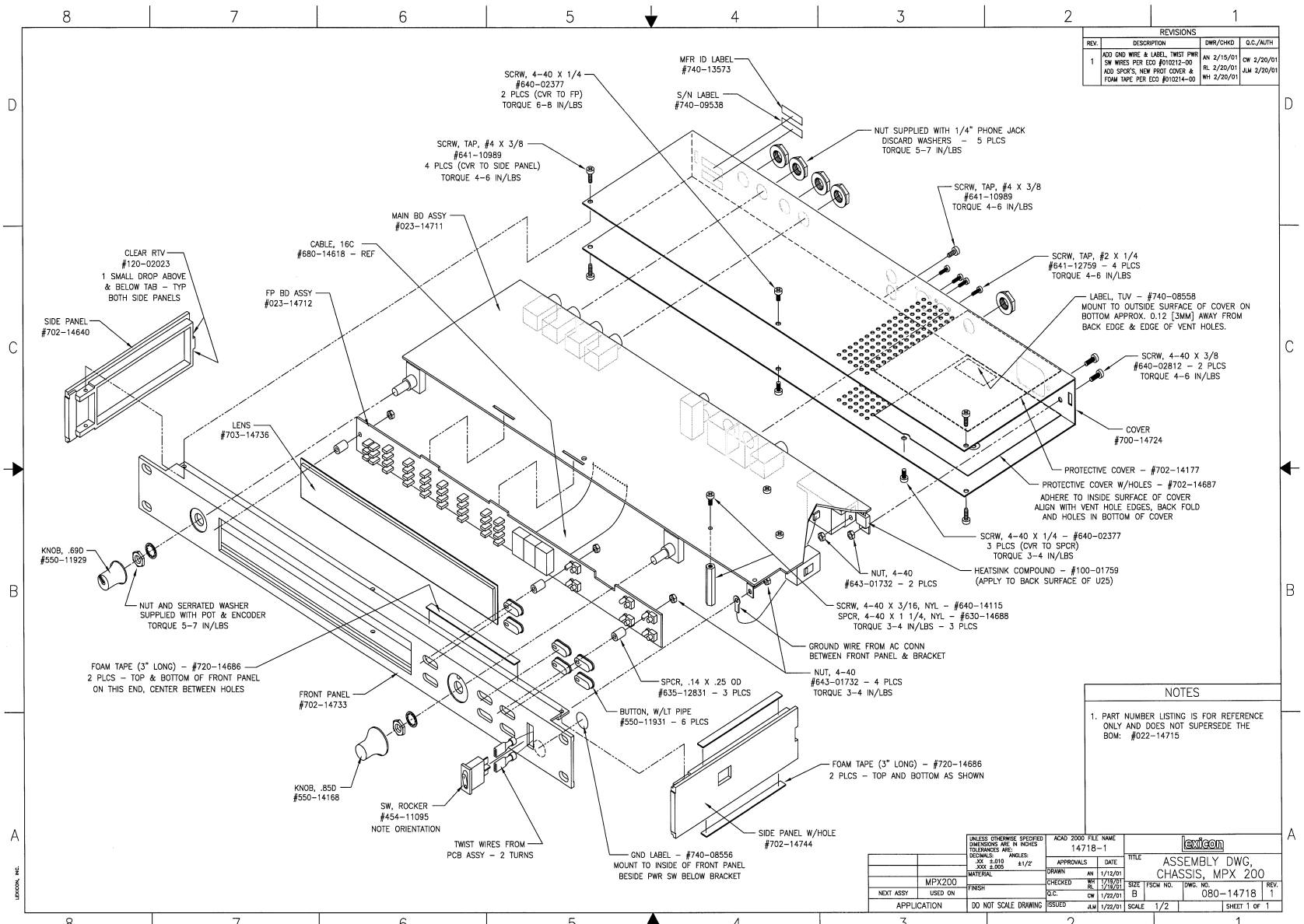
PC BD,FP,MPX200
COMPONENT LAYOUT

REV 1

SCALE N/A

SHEET 1 OF 1

Your Notes:



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD GND WIRE & LABEL, TWIST PWR SW WIRES PER ECO #010212-00 ADD SPCR'S, NEW PROT COVER & FOAM TAPE PER ECO #010214-00	AN 2/15/01 RL 2/20/01 WH 2/20/01	CW 2/20/01 JLM 2/20/01

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BOM: #022-14715

	MPX200		
NEXT ASSY	USED ON	FINISH	
APPLICATION		DO NOT SCALE DRAWING	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: ANGLES:
.XX ±.010 ±1/2°
.XXX ±.005
MATERIAL

ACAD 2000 FILE NAME
14718-1

APPROVALS		DATE
DRAWN	AN	1/12/01
CHECKED	WH RL	1/19/01 1/19/01
Q.C.	CW	1/22/01
ISSUED	JLM	1/22/01

Lexicon

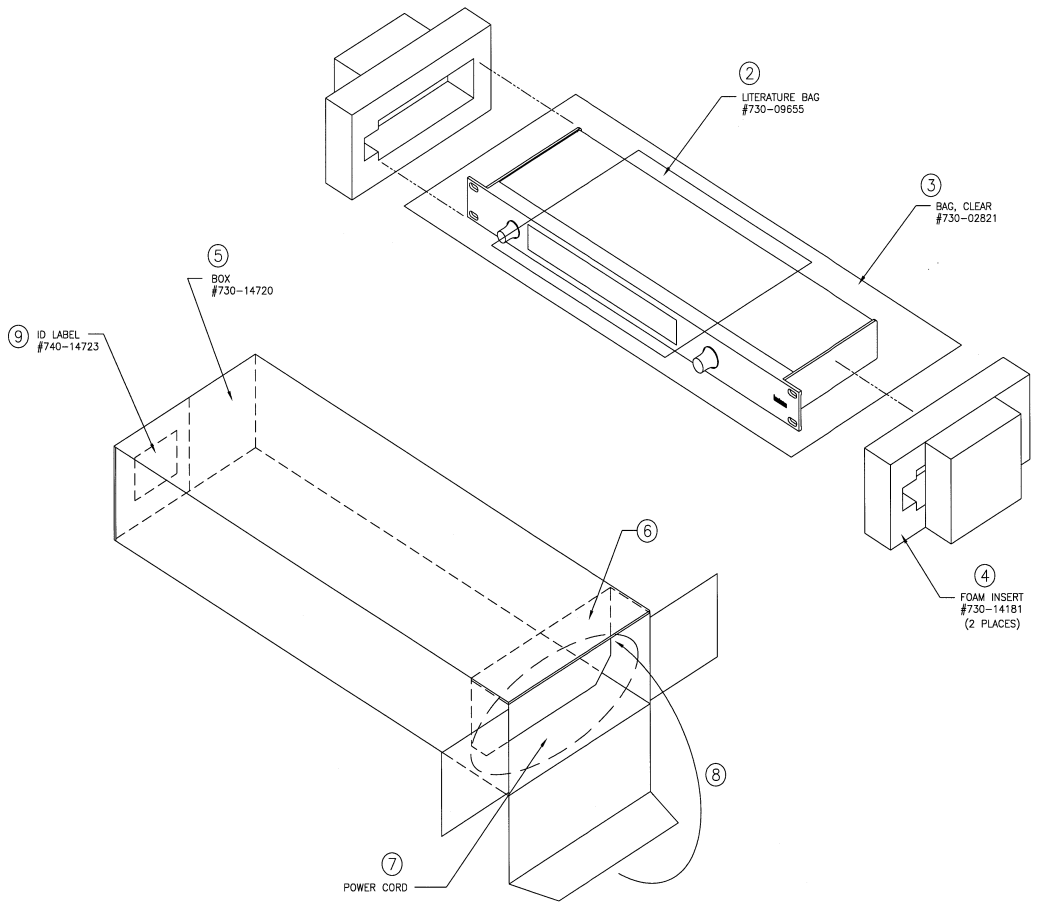
TITLE: ASSEMBLY DWG, CHASSIS, MPX 200

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14718	1

SCALE 1/2 SHEET 1 OF 1

LEXICON, INC.

Your Notes:



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL #022-14708.
2. PUT CD & LITERATURE IN BAG. REFER TO BOM FOR LIST AND SEQUENCE OF LATEST DOCUMENTATION PACKAGE. FOLD & TAPE BAG.
3. PUT UNIT (WITH LITERATURE BAG ON TOP) IN BAG, FOLD AND SEAL BAG SO ALL CREASES AND SECURING TAPE ARE ON THE BOTTOM OF THE UNIT.
4. PLACE FOAM INSERTS ON ENDS OF SEALED UNIT AS SHOWN.
5. FOLD UP END OF BOX WITH STRAIGHT RECTANGULAR FLAPS. TAPE WITH CLEAR TAPE.
6. SLIDE UNIT INTO BOX. FOLD DOUBLE SCORED FLAP INTO BOX AGAINST THE FOAM INSERT.
7. PLACE APPROPRIATE POWER CORD IN THE END CAVITY. SEE BOM FOR PART NUMBER.
8. FOLD IN SMALL SIDE FLAPS AND CLOSE END FLAP. TAPE WITH CLEAR TAPE.
9. PLACE ID LABEL ON END FLAP IN SPACE PROVIDED.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005	ACAD 2000 FILE NAME 14719-0
		MATERIAL	APPROVALS / DATE
		FINISH	DRAWN AN 12/3/00
	MPX200		CHECKED RH 1/18/01, JL 1/19/01
NEXT ASSY	USED ON		Q.C. CW 1/22/01
APPLICATION		DO NOT SCALE DRAWING	ISSUED JLM 1/22/01

lexicon

TITLE: ASSY DWG, SHIPMENT, MPX200

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14719	0

SCALE N/A SHEET 1 OF 1

LEXICON, INC.

Your Notes:

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