Section 6
Technical Data

page contents

Specifications

It is impossible to characterize the listening quality of even the simplest limiter or compressor on the basis of the usual specifications, because such specifications cannot adequately describe the crucial dynamic processes that occur under program conditions. Therefore, the only way to meaningfully evaluate the sound of an audio processor is by subjective listening tests.

Certain specifications are presented here to assure the engineer that they are reasonable, to help plan the installation, and to help make certain comparisons with other processing equipment. Some specifications are for features that are only available on the 2200-D.

Installation

Analog Audio Input

Configuration: Left and right.

Impedance: Electronically balanced 600Ω or >10kΩ load impedance, jumper-selectable.

Dynamic Range: >90dB.

Common Mode Rejection: ≥70dB at 50-60Hz. ≥45dB at 60Hz-15kHz.

Sensitivity: –20dBu to +20dBu to produce 10dB gain reduction at 1kHz, software- and jumper-adjustable.

Maximum Input Level: +27dBu.

Connector: XLR-type, female, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 (+) and 3 electronically balanced, floating and symmetrical.

A/D Conversion: 18-bit.

Filtering: RFI-filtered, with high-pass filter at 0.15Hz.

Analog Audio Output

Configuration: Left and right. Flat or pre-emphasized (at 50µs or 75µs), software-selectable.

Source Impedance: 30Ω, ±5%, electronically balanced and floating.

Load Impedance: 600Ω or greater, balanced or unbalanced. Termination not required.

Output Level: Adjustable from –20dBu to +20dBu into 600Ω or greater load, software-adjustable.

Output Noise Level: ≤–90.0dB (Bypass mode, de-emphasized, 20Hz-15kHz bandwidth, referenced to 100% modulation).

Crosstalk: ≤–70dB, 20Hz-15kHz.

Distortion: ≤0.05% THD (Bypass mode, de-emphasized, 20Hz-15kHz bandwidth).

Connector: XLR-type, male, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 (+) and 3 electronically balanced, floating and symmetrical.

Filtering: RFI-filtered.

Digital Audio Input (2200-D Only)

Configuration: Two-channel per AES/EBU-standard. 20-bit resolution.

Sampling rate: 25-55kHz, automatically-selected.

Connector: XLR-type, female, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 and 3 transformer balanced and floating.

Input Reference Level: Adjustable from 0dBFS to –20dBFS, software-controlled.

Digital Audio Output (2200-D Only)

Configuration: Two-channel AES/EBU-standard. 18-bit resolution. Software-controllable for flat, pre-emphasized to the selected processing pre-emphasis, J.17 pre-emphasized, or pre-emphasized to the selected processing pre-emphasis plus J.17 pre-emphasis.

Sampling rate: 32kHz, 44.1kHz, or 48kHz, software-selected.

Connector: XLR-type, male, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 and 3 transformer balanced and floating.

Status Bits: AES/EBU status bits are implemented to control pre-emphasis in the Orban 8208 digital Stereo Encoder.

Output Level Adjustment Output at 100% modulation, adjustable from 0dBFS to –22.8dBFS, software-controlled.

Composite Baseband Outputs

Configuration: Two (2) outputs, each with an independent output level control, output amplifier and connector.

Source Impedance: 0Ω voltage source or 75Ω (jumper-selectable), single ended, floating over chassis ground.

Load Impedance: 37Ω or greater. Termination not required.

Level (0Ω Source Impedance, 75Ω or higher Load Impedance): Adjustable 0.4Vp-p to 8.8Vp-p with front panel multi-turn output level controls, one per output.

Pilot Level: Adjustable from 8% to 10%, software-controlled.

Pilot Stability: 19kHz, ±0.5Hz (10° to 40° C).

D/A Conversion: 18-bit.

Signal-to-Noise Ratio: ≥85dB (Bypass mode, demodulataed, de-emphasized, 20Hz-80kHz bandwidth, referenced to 100% modulation, unweighted).

Distortion: ≤0.05% THD (Bypass mode, demodulated, de-emphasized, 20Hz-15kHz bandwidth, referenced to 100% modulation, unweighted).

Stereo Separation: At 100% modulation = 3.5Vp-p, >60dB, 30Hz-15kHz, >65dB typical at 1kHz; at 100% modulation = 1.0Vp-p, >50dB, 30Hz-15kHz.

Crosstalk (Linear): ≤–80dB, main channel to sub-channel or sub-channel to main channel) referenced to 100% modulation).

Crosstalk (Non-Linear): ≤–80dB, main channel to sub-channel or sub-channel to main channel) referenced to 100% modulation).

38kHz Suppression: ≥70dB; 75dB typical (referenced to 100% modulation).

76kHz and Sideband Suppression: ≥70dB; 80dB typical (referenced to 100% modulation).

Connector: BNC, floating over chassis ground. EMI-suppressed.

Maximum Load Capacitance: 0.047μF (0Ω source impedance).

Maximum Recommended Cable Length (0Ω Source Impedance): 100ft/30m RG-58A/U.

Filtering: RFI-filtered.

Remote Control Interface

Configuration: Eight opto-isolated inputs, user-programmable to select any eight of: User Presets, Factory Presets, Bypass, Tone, Exit Test (returns from Bypass or Tone), Stereo, Mono from Left, Mono from Right, Mono from Sum, Input Analog, Input Digital.

Control: Momentary or continuous low side contact closure. 10mA minimum sink current; 9VDC, 50mA rating.

Power Supply: Current-Limited 9VDC provided to facilitate use with contact closure.

Connector: DB-25, EMI-suppressed.

Filtering: RFI-Filtered.

Power

Voltage: 90-120VAC, 100-132VAC or 200-264VAC, 50-60Hz; 40VA.

Connector: IEC; detachable 3-wire power cord supplied. AC is EMI-suppressed.

Ground: Circuit ground is independent of chassis ground; can be isolated or connected with a rear panel switch.

Safety Standards: UL, CE, CSA.

Environmental

Operating Temperature Range: 32° to 122°F/0° to 50°C at nominal operating voltages.

Humidity: 0-95% RH, non-condensing.

Dimensions (W x D x H): 19" x 14.25" x 1.75"/48.3cm x 36.2cm x 4.5cm. 1 rack unit high.

Weight: 12 lbs/5.4kg.

Shipping Weight: 15 lbs/6.8kg.

Warranty

One Year, Parts and Labor: Subject to the limitations set forth in Orban's Standard Warranty Agreement.

Specifications are subject to change without notice.

Circuit Description

This section provides a detailed description of circuits used in the 2200/2200-D. It starts with an overview of the 2200/2200-D system, identifying circuit sections and describing their purpose. Then each section is treated in detail by first giving an overview of the circuits followed by a component-by-component description. Keywords are highlighted throughout the circuit descriptions to help you quickly locate the information you need.

Overview

The block diagram on page 6-35 illustrates the following overview of 2200/2200-D circuit sections.

The 16.384MHz Oscillator and System Clocking section provides the various clocks needed by the control, I/O and DSP circuits to carry out their functions.

The Control Circuits administrate control of the 2200/2200-D system.

The User Control Interface and LED Display Circuits section includes the connector, RF-filtering, and circuitry for the remote control inputs. It also includes circuitry for the front panel pushbutton switches, LED control status indicators, and LED Meters. The LED Meters measure various 2200/2200-D signal levels and display the results on six front panel 10-segment LED meters.

The L/R Input Circuits include the connectors and RF-filtering for the left and right audio inputs and the digital audio input, and the circuitry to interface these inputs to the digital processing.

The L/R Output Circuits include the connectors and RF-filtering for the left and right audio outputs and the digital audio output, and the circuitry to interface the digital processing to these outputs.

The Composite Output Circuits include the connectors and RF-filtering for the two composite outputs, and the circuitry to interface the digitally processed, stereo encoded signal to these outputs.

The DSP Circuits implement the bypass, test tone, audio processing, and stereo encoding functions using digital signal processing.

The Power Supply provides power for all 2200/2200-D circuit sections.

16.384MHz Oscillator and System Clocking

A synchronous clocking scheme is used on the 2200/2200-D to eliminate any asynchronous clocks operating in the sensitive regions of the L/R input A/D converter. A single 16.384MHz crystal oscillator provides the timing reference for all system digital clock signals. The only clocks that run asynchronous to this clock are the AES/EBU digital audio input related clocks and the 11.2896MHz free running crystal clock oscillator providing the

44.1kHz AES/EBU output sample rate (this does not fall within a sensitive region of the A/D). Synchronous counters are used to divide the 16.384MHz clock to produce the various clock signals for the system. A PLL circuit is used to synthesize an 18.432MHz clock for operating the host microprocessor and a 6.144MHz clock for providing the 48kHz AES/EBU output sample rate clock in addition to providing the AES/EBU input receiver with the ability to measure the input sample rate.

Component-Level Description:

The 16.384MHz digital output from crystal oscillator Y602 feeds the master clock (MCLK) inputs of both the input and the output SRC chips IC603 and IC615. The 16.384MHz clock also feeds flip-flop IC604, which divides by two to produce an 8.192MHz clock. The 8.192MHz clock feeds digital multiplexer chip IC610, which routes the 8.192MHz to AES/EBU digital audio transmitter chip IC616 when an internally generated 32kHz output sample rate is selected. The 8.192MHz clock is also sent to an 8-bit synchronous counter implemented in programmable logic array (PLA) IC613.

This counter divides down to obtain the lower frequency system clocks. All outputs of the PLA have their transitions coincident with the rising edge of the 8.192MHz clock. The 8.192MHz clock is inverted by buffers IC605-A, -B to provide clocks 8.192MHZA* and 8.192MHZB* that have falling edges coincident with the transitions of the lower frequency clocks. 8.192MHZA* feeds the bit clock of the inter-DSP communication links following buffers IC710-B, -D. 8.192MHZB* feeds the A/D input clock (256 x sample rate), the L/R output D/A master clock, and the input bit clock on both the L/R output D/A and the composite D/A.

The 2.048MHz clock output from IC613 feeds the PLL circuit made up of PLA IC618, 74HC4046 phase detector/VCO IC619 and associated components. The PLA first buffers the 2.048MHz signal, providing a clean 2.048MHz output at pin 12 used as the reference input to the PLL phase detector (IC619 pin 14). Of the three detectors included in the 74HC4046, the phase frequency detector (PFD) is used by the 2200/2200-D. The output of the phase detector (pin 13) feeds the loop filter made up of resistors R607, R608 and capacitor C605 that provide a single pole low-pass filter forming a second order loop. Pin 9 of IC619 is the input control voltage to the VCO. Resistor R614 eliminates subharmonic frequency modulation of the VCO caused by parasitic capacitance. Resistors R605 and R606 set the PLL's lock-in frequency range. A divide-by-nine counter is placed between the VCO output and the phase detector comparator input. This places the VCO output at 18.432MHz. The divide-by-nine is implemented by the PLA IC618 between pins 2 and 15. A 6.144MHz clock is derived at the counter's divide-by-three point and is provided at pin 17 of the PLA. The PLA provides a buffered 18.432MHz output at pin 14 which feeds Z-180 microprocessor IC100.

IC614-A, -D provide buffered clocks 2.048MHZA and 2.048MHZB for driving the EXTAL inputs (pin 27) of the DSP chips. Each buffer drives four DSP chips.

The 256kHz clock output of IC613 (pin 15) is required for the DSP-to-composite D/A interface. The 128kHz clock (pin 14) is used for the inter-DSP word clock. The 128kHz, 64kHz and 32kHz clocks are all used in the LCD backlight drive

circuit. The 32kHz clock is also used for the input word clock of both the output sample-rate converter (SRC) and the L/R output D/A. The 32kHz clock is used to generate DSP interrupt request signals (IRQBA, IRQBB) required for process timing and interchip synchronization. The circuit consisting of flip-flop IC612 and IC614-B, -C is required to ensure that the first falling edges of all IRQB signals are coincident. This synchronization occurs every time the unit is powered up and when there is a processing algorithm change. It is controlled by the Z-180 via pin 2 of latch IC611. The 32kHz clock is also used, along with IC313, in the A/D clock synchronizing circuit. This circuit makes the IRQB and the L/R clocks, both operating at 32kHz, phase synchronous. This ensures that the process-to-output buffer transfer internal to the DSP doesn't overlap the output buffer-to-peripheral transfer. The 8.192MHZB* clock that feeds the A/D input clock (IC312 pin 19) is internally divided down to produce a 32kHz word clock at IC312 pin 13 and a 2.048MHz bit clock at pin 14. These clocks are used to control the A/D-to-DSP serial interface and the input SRC-to-DSP serial interface.

AC terminations are used on various clocks throughout the board to improve signal integrity for sensitive devices.

Control Circuits

The control circuits process and execute user-initiated requests to the system. The source of these requests is the front panel buttons and the remote contact closures. These changes affect hardware function and/or DSP processing. The control circuits also send information to the LCD display, LED status, and LED meter circuits. A RAM chip stores code segments. For quick access, an EEPROM chip stores dynamic system state information. A ROM chip contains the executable form of 2200/2200-D DSP and Control software.

1. Microprocessor and Power Monitoring Circuit

A Z-180 microprocessor executes software code required to control the functionality of the 2200/2200-D. The EXTAL port of the Z-180 receives an 18.432MHz clock signal from the clock divider/PLL circuit and is internally divided down to 9.216MHz to provide the Z-180 system clock frequency. ROM contains control software for the Z-180. User system setup and other dynamic system state information that must survive power down is stored in non-volatile EEPROM. Power monitoring circuitry prevents data corruption by placing and holding the Z-180 in reset if AC mains power is insufficient.

The Z-180 communicates to the DSP through the synchronous serial data host port. When the DSP requires executable code, the Z-180 reads it from the ROM and sends it to the DSP. The Z-180 sends parameter control data to the DSP and receives status data from the DSP. If status from DSP is irregular, the Z-180 will place the 2200/2200-D hardware and DSP in a reset state and execute initialization procedures.

Component-Level Description:

The Z-180 is IC100. Watchdog timer/voltage monitor IC122 provides the system reset function. IC122 pin 7 monitors pulses generated every 1 second by the Z-180. If the Z-180 is not operating correctly to provide the pulses, IC122 will reset the Z-180. IC122 also monitors the voltage on the +5V source that supplies power to the 2200/2200-D digital electronics. When the +5V line is above the minimum operating voltage of +4.75V, R103 will pull RESET* high which allows the Z-180 to exit the reset condition. When the +5V line is below the minimum operating voltage, the open-collector output of IC122 pulls Z-180's RESET* low which puts the Z-180 into the reset condition, thereby preventing the Z-180 and the 2200/2200-D electronics from executing incorrectly due to low +5V line voltage.

Z-180 IC100 pins 55, 56, and 57 comprise the host serial data communication port. The Z-180 uses this port to communicate with the DSP IC700-IC707 via host port interface pins 26, 35, and 41; and with EEPROM IC107 via pins 2, 5, and 6. Communication is SPI type with Z-180 as master and DSP as slave.

2. RAM, ROM and EEPROM

A RAM chip provides temporary storage for Z-180 data and program code segments. A ROM chip provides permanent storage of the executable control software and the executable DSP software. System state information that must be maintained while the 2200/2200-D is powered down is stored in a EEPROM. The EEPROM does not lose data when the 2200/2200-D is powered down.

Component-Level Description:

IC104 decodes Z-180 memory addresses to access instructions to execute from ROM IC105 and to read or write data from 32KB RAM IC106. EEPROM IC107 is selected by latch IC611 pin 6.

3. Data Latches, Tri-State Data Buffers and Address Decoders

Digital logic decodes Z-180 I/O addresses, allowing the Z-180 to access RAM, ROM and EEPROM. The logic provides Z-180 data bus allocation by using latches and tri-state data buffers to allow other 2200/2200-D hardware to communicate to the Z-180. To control other hardware, the Z-180's data bus state is latched at the appropriate time, and the latched control signals are provided to other hardware. For the Z-180 to read information from other hardware, the Z-180's data bus is connected at appropriate times to other hardware's source signals through tri-state data buffers (e.g. IC120).

Component-Level Description:

Decoder IC104 allows the Z-180 to access ROM IC105 and RAM IC106. Decoders IC101, IC102, and IC103 allow the Z-180 to access all other

2200/2200-D hardware. The decoded outputs from IC101, IC102, and IC103 are used to latch the state of the Z-180 data bus at appropriate times with data latches IC202, IC205, IC207, IC303, IC305, IC609, IC611, IC708, and IC709, and to allocate the Z-180 data bus at appropriate times to various peripherals via tri-state data buffers IC120, IC204, and IC601. IC120 buffers or tri-states status information from the remote contact closure circuitry onto the Z-180 data bus. IC204 buffers or tri-states information from the user control interface onto the Z-180 data bus. IC601 buffers or tri-states status information from AES/EBU Receiver IC600 onto the Z-180 data bus.

User Control Interface and LED Display Circuits

The user control interface enables the user to control the functionality of the 2200/2200-D unit. A rear panel remote interface connector enables remote control of certain functions. Front panel pushbutton switches select between various operational modes and functions. Data latches detect and store the commands entered with these switches. Front panel status LEDs indicate the control status of the unit, and meter LEDs indicate signal levels and processing activity within the unit.

1. Remote Interface

A remote interface connector and circuitry enables remote control of certain operating modes; the 2200 has eight remote contact closure inputs.

A valid remote signal is a momentary pulse of current flowing through the particular remote signal pins. Current must flow consistently for 50msec for the signal to be interpreted as valid. Generally, the 2200/2200-D will respond to the most recent control operation whether it came from the front panel, or remote interface.

Component-Level Description:

J101 is a 25-pin D-connector that connects the remote control input signals. The connector incorporates a ferrite block to filter out RFI from the signals. The associated opto-isolators (e.g. IC110) isolate the inputs from the detector circuitry on the 2200/2200-D. The associated diodes (e.g. CR102) prevent the opto-isolators from breaking down under a reverse bias. The outputs of the opto-isolators are inverted and buffered (e.g. by IC118-A) and latched by tri-state data buffer IC120. When REMOTE* signal provided to IC120 pin 19 is brought low, IC120 places remote signals on the Z-180 data bus.

2. Switch Matrix and LED Indicators

Ten front panel pushbutton switches are arranged in a matrix, configured as two columns and six rows (the FUNCTION and CONTRAST keys have dedicated rows). These switches are the primary element of the physical user interface to the 2200/2200-D control software. The host microprocessor controls the system setup and function of the DSP according to the switch/rotary encoder entered commands, the AES Status bits from the Digital Input signal,

and the remote control interface status; and updates the LED control status indicators accordingly.

Component-Level Description:

S200-S208 and S210 are the front panel pushbutton switches. CR200-CR204 and CR206 are the front panel LED control status indicators. Via decoder IC102, the host microprocessor Z-180 periodically selects data latch IC202 (on the display board) to drive one of the two columns in the switch matrix low, then commands tri-state data buffer IC204 (also on the display board) to read its inputs to determine if any new information is being received from one or more of the switches in that column. If no switches are closed, pull-up resistors R202, R210-R213 pull the buffer inputs to +5V. The buffer, in turn, de-bounces the signals and places the appropriate word on the data bus for the Z-180 to read. The Z-180 transmits the updated information to data latch IC202 which directly drives the LED Control Status Indicators.

3. LED Meter Circuits

The meter LEDs are arranged in an 8x8 matrix, in rows and columns. Each row of LEDs in the matrix has a 1/8 duty cycle ON time. The rows are multiplexed at a fast rate so that the meters appear continuously illuminated. Via the serial port, the DSP sends meter data values to the Z-180, which alternately sends pairs of mapped 8-bit words to the data bus. One of the words, latched by a "row selector" latch, has a single rotating active bit to select one of the 8 rows. The other word, latched by a "column selector" latch, has active bits corresponding to those of the 8 LEDs in the selected row that are to be lit. The latched words control high-current Darlington transistor arrays which drive the LED matrix.

Component-Level Description:

The meter LED matrix consists of six 10-segment LED bargraph assemblies (CR208-CR213) and three discrete LEDs (CR214-CR216). IC208 contains eight Darlington transistors, each of which is connected to the cathodes of a "row" of the LEDs. Row selector latch IC207, controlled by the Z-180, alternately turns one of the eight transistors on, such that it will sink current through the LEDs selected by column selector latch IC205, also controlled by the Z-180. IC205 turns on the appropriate transistors inside current driver IC206 to drive the selected row of LEDs. IC206 gets its current from a storage capacitor fed directly by the power transformer's lower voltage secondary winding. Resistors RP200 function as current limiting resistors.

L/R Input Circuits

This circuitry interfaces the analog and digital audio to the DSP. The analog input stages scale and buffer the input audio level to match it to the analog-to-digital (A/D) converter. The A/D converts the analog input audio to digital audio. The digital input receiver accepts AES/EBU-format digital audio signals from the digital input connector, and transmits them

to the input sample rate converter (SRC). The digital audio from the A/D and SRC is transmitted to the DSP.

1. Analog Input Stages

The RF-filtered left and right analog input signals are each applied to a resistor load and a resistor pad. The pad and load are enabled or disabled by jumpers that are positioned by hand. The loaded and padded signal is applied to a floating-balanced amplifier that has an adjustable (digitally-controlled) gain. The gain is set by FET transistors and analog switches. The state of the FETs and switches is set by the outputs of a latch. The control circuits control the gain according to what the user specifies from the front panel controls by writing data to the latch. The gain amplifier output feeds a circuit that scales, balances, and removes DC from the signal. This circuit feeds an RC low-pass filter which applies the balanced signal to the analog-to-digital (A/D) converter.

Component-Level Description:

The left channel balanced audio input signal is applied to the filter/load/pad network made up of L300, L301, L302, L303, R300-R305, C323 and C324. J301 is a jumper that removes or inserts the optional 600Ω termination load (R300) on the input signal. J302 and J303 are the jumpers that remove or insert the resistive divider (R301-R303) that pads the input signal before it is applied to IC300, a differential amplifier. R306, R307, R310-R313, FETs Q300-Q301, and quad analog switch IC307 make up the circuit that sets the gain of IC300. The FETs, along with IC307, are used as switches to change the resistive paths in the circuit. The state of the FET switches is set by the outputs of digital latches IC304 and IC305. The latch outputs feed IC306, a quad comparator, which outputs 0V to turn on a FET and −15V to turn off a FET. The control circuit writes directly to IC307 to control the state of the switches on IC307. IC300 feeds IC302 and associated components. This stage balances the signal and attenuates by 3.5dB to scale the signal to the proper level for the analog-to-digital (A/D) converter. IC301-B and associated components comprise a servo amp to prevent DC from passing to the DSP. R334, R337, C302, and C303 make a simple RC filter necessary to filter high frequency energy that would otherwise cause aliasing distortion in the A/D converter. The corresponding right channel circuitry is functionally identical to that just described.

2. Stereo Analog-to-Digital (A/D) Converter

The A/D is a stereo, 18-bit sigma-delta converter, implemented on a dual-chip integrated circuit. The A/D oversamples the audio at 2.048MHz. It applies noise shaping, then it filters and decimates to a 32kHz sample rate. The samples are output in two's complement, 32-bit word, two-word frame serial format, with SPI compatible timing, MSbit first, and transmitted to the DSP. The 32kHz frame clock and 2.048MHz bit clock from the A/D function as master clocks for the 2200/2200-D input to the DSP. For more information on 2200/2200-D input clocking, please refer to "16.384MHz Oscillator and System Clocking."

Component-Level Description:

The balanced left analog input is applied to pins 3(+) and 4(-), and the balanced right analog input is applied to pins 26(+) and 25(-) of the A/D (IC312). The maximum differential signal that the A/D can accept is ±7.36Vpeak. The A/D samples the left and right inputs simultaneously at 64 times the 2200/2200-D sample rate of 32kHz. ICLKD, the master clock input of the A/D (pin 19), is fed an 8.192MHz clock providing the 2.048MHz input sample rate required. The A/D sends the digitized stereo audio to the first DSP chip (IC700) via its synchronous serial port formed by the data SDATA (pin 15), the bit clock SCLK (pin 14) and the word clock L/R* (pin 13). The SPI communication standard is used for this audio interface, with A/D as master and DSP IC700 as slave. The SPI format is: 32-bits/word, multiplexed stereo, word clock low represents left data present, MSB first, data transitions occur on rising edge of the bit clock, first 18 bits are valid, trailing bits are set low, MSB delayed one bit period from word clock edge. IC314 provides buffering to reduce the drive requirement of the on-board drivers on the A/D and to ensure that there are no overshoots or undershoots as a result of transmission line reflections that may degrade the performance of the A/D. IC109-D is required to invert the word clock to support the SPI interface.

3. Digital Input Receiver and Sample Rate Converter (SRC)

The digital input receiver accepts digital audio signals using the AES/EBU interface format (AES3-1992). The receiver and input sample rate converter (SRC) together will accept and sample-rate convert any of the “standard” 32kHz, 44.1kHz, 48kHz rates in addition to any digital audio sample rate within the range of 25kHz and 55kHz. The audio signal received is decoded by the AES receiver and sent to the SRC. The SRC converts the input sample rate to the 32kHz 2200-D system sample rate. Via a synchronous serial interface, the SRC sends the 32kHz sample rate audio to the DSP for processing.

Component-Level Description:

The differential digital input signal is received through a shielded 1:1 pulse transformer (T600). T600 has very low inter-winding capacitance, providing a high level of isolation for high frequency common mode interference. IC600 is a dedicated AES/EBU digital audio receiver integrated circuit. It contains a phase locked loop that recovers the clock and the synchronization information present in the AES/EBU signal. A Schmitt trigger at the input provides 50mV of hysteresis for added noise immunity. R600 provides a 110Ω input impedance per the AES/EBU specification.

The Z-180 provides the active high reset signal (AES_RST) to IC600 mode control pins 17, 18, and 23, via latch IC609 pin 6. This is used when the 2200-D is asked to respond to analog audio input. When in the reset state, the receiver holds all outputs inactive (except MCK pin 19).

IC600 pins 2 through 6 and pin 27 are an output latch that provides AES/EBU status information, selected by the STATSEL line. The information on this latch is provided to the Z-180 data bus via tri-state data buffer IC601. STATSEL signal

from IC611 pin 12 is applied to IC600 pin 16. When STATSEL is high, pins 2 through 6 and pin 27 contain information about the channel status bits. When STATSEL is low, pins 2 through 6 and pin 27 contain input sample rate and error information. The Z-180 reads these to determine if a valid AES/EBU signal and sample rate is present. CHSEL is used to select whether channel A or channel B status bits are present on IC600's output latch. When STATSEL is low, left channel status is made available, and when STATSEL is high, right channel status is made available.

Received AES audio is transmitted from the AES receiver to the input sample rate converter (SRC IC603), in the synchronous serial SPI format. The AES receiver is master and the SRC is slave. The AES receiver outputs data on pin 26, the bit clock on pin 12, and the frame clock on pin 11. The frame clock is inverted by IC605-F for compatibility with the SRC's input port. These signals are sent to the SRC serial input interface pins 3, 4, and 6 respectively.

The MCK clock output at pin 19 of the AES receiver chip has a frequency 256 times the input sample rate of the received signal. This is used to drive the output AES/EBU transmitter when an output sample rate that is synchronous to the input sample rate (external sync) is required.

The crystal oscillator (Y602) provides the SRC a master clock of 16.384MHz on pin 2. This MCLK frequency allows the input SRC to operate with input sample rates in the range of 8.192kHz (MCLK/2000) to 57kHz (MCLK/286). SRC_RST is an active low reset signal tied to pin 13 of the SRC. This signal is controlled by the Z-180 via pin 2 of latch IC609.

The MSDLY_I, BKPOL_I, and TRGLR_I pins of the SRC chip configure the chip for SPI format. Pin 1 of the SRC (GPDLYS) is tied high to minimize the chip's group delay to approximately 700µs as opposed to approximately 3ms, giving up some tolerance to variations in sample rates. Pin 28 (SETLSLW) is tied high to cause the SRC to settle slowly to changes in sample rates, resulting in the best rejection of sample rate jitter.

The sample rate converted output of the input SRC feeds the first DSP chip (IC700). The SRC output port and the DSP input port are both slaves, with clocks supplied by the L/R input A/D converter (IC312). The SRC generates DIG_IN (data) on pin 23, and receives the bit clock and the word clock on pins 26 and 24 respectively. An inverted version of this word clock is used by the DSP chip to conform with the SPI format it requires.

L/R Output Circuits

This circuitry interfaces the DSP to the analog and digital audio outputs. The digital audio from the DSP is transmitted to the digital-to-analog converter (D/A) and output sample rate converter (SRC). The digital-to-analog (D/A) converter converts the digital audio words generated by the DSP to analog output audio. The MDAC stages scale and buffer the D/A output signal to drive the analog output stages to the correct level. The analog output stages drive the analog output XLR connectors with a low impedance, floating balanced output. The digital output transmitter accepts the digital audio words from the output sample rate

converter (SRC) and transmits them in AES/EBU-format digital audio signals on the digital output connector.

1. Stereo Digital-to-Analog (D/A) Converter

The D/A is a single chip, stereo, 18-bit delta-sigma converter.

For information on 2200/2200-D system clocking, please refer to "16.384MHz Oscillator and System Clocking."

Component-Level Description:

IC400 is the digital-to-analog (D/A) converter for the left and right output signals. The synchronous serial input interface consists of the bit clock, data and latch enable pins that are configured for the SPI format via DIF0 and DIF1 pins (for details on SPI, see page 6-11). The processed digital output (ANLG_OUT) is provided by DSP IC706 on its SAI output port SDO0 (pin 47), and is received by the D/A on pin 18.

An 8.192MHz bit clock is provided from the system clock circuitry to both the DSP and the D/A chips. The DSP output data format is SPI (32 bits per word, two words per frame). DSP chip IC706 receives a 128kHz frame clock at its WST input (pin 50) that sets the word transfer rate to eight words per 32kHz period. The D/A receives a 32kHz clock at its LRCK input (pin 20). LRCK delineates the left and right samples used by the D/A; therefore the D/A uses the first sample received for the left output and the fifth sample for the right output. The DSP output samples are formatted to ensure that the D/A uses a left and right output pair that represent the simultaneously sampled analog input.

2. Analog Output Stages

The left and right analog signals emerging from the digital-to-analog (D/A) converter are each RC low-pass filtered and applied to an inverting amplifier having an adjustable (digitally-controlled) gain. The gain is set by an MDAC. The state of the MDAC is set by the outputs of a latch. The control circuits control the gain according to what the user specifies from the front panel controls by writing data to the latch. The gain amplifier feeds a programmable de-emphasis filter stage with its response digitally-controlled by JFET switches. The de-emphasis stage feeds a floating-balanced line driver, having a 30Ω, ±5% output impedance. The line driver outputs are applied to the RF-filtered left and right analog output connectors.

Component-Level Description:

The left channel signal emerging from the digital-to-analog (D/A) converter is RC low-pass filtered by R402 and C407 to remove high frequency images. It is then applied to an adjustable gain amplifier formed by VR400, R404-R406, C409, IC401, and IC402-A. These components form an inverting amplifier

circuit. IC401 is an 8-bit MDAC, which is a resistor ladder with a programmable resistance. The control circuit writes an 8-bit word directly to IC401, which has a latch on board to store the word. The word sets the resistance value between pin 15 and pin 1 of IC401. IC402-A forces pin 1 of IC401 to virtual ground. The resistance between pin 1 and pin 16 of IC401, and resistors R404-R406 and VR400 are in the feedback loop of IC402-A. C409 stabilizes this stage. VR400 is a factory gain trim to correct for tolerances in IC401, IC400, and the rest of the analog output circuits.

IC402-A feeds the stage consisting of IC402-B and associated components, which is a programmable de-emphasis filter. JFETs Q400 and Q401 are used to switch C410 and C411, respectively, in or out of the circuit. The state of the JFET switches is set by the outputs of IC305, a digital latch. The latch outputs feed IC407, a quad comparator, which outputs 0V to turn on a FET and –15V to turn off a FET. If neither of the JFETs are on, the circuit is a unity-gain inverting amplifier. The circuit becomes a first-order low-pass filter if one of the JFETs is turned on. If Q400 is on, capacitor C410 is in circuit to create a 75µs time constant. If Q411 is on, capacitor C401 is in circuit to create a 50µs time constant.

IC402-B feeds the stage consisting of IC403-A, IC403-B, IC408-A, and associated components, which is a floating-balanced line driver. The floating characteristic is achieved by complex cross-coupled positive and negative feedback between two 5532 opamps, and its operation is not readily explainable except by a detailed mathematical analysis. Opamps may be replaced; resistors are specially matched and should not be replaced. IC408-A, R444, R445, R447, and C419 comprise a servo amplifier which centers around ground the average DC level at output connector J400.

The balanced audio output signal is applied to the RF filter network made up of L400, L401, L402, and L403, and then to XLR connector J400.

The corresponding right channel circuitry is functionally identical to that just described.

3. Digital Sample Rate Converter (SRC) and Output Transmitter

An output sample rate converter (SRC) chip is used to convert the 32kHz 2200-D system sample rate to any of the standard 32kHz, 44.1kHz or 48kHz rates. A digital audio interface transmitter chip is used to encode digital audio signals using the AES/EBU interface format (AES3-1992). A synchronous serial interface is used for all inter-chip communication.

Component-Level Description:

The processed digital output (DIG_OUT) provided at the SAI output port SDO0 (pin 47) of DSP IC706 is received by asynchronous sample rate converter (SRC) IC615 pin 3. An 8.192MHz bit clock is provided from the system clock circuitry to both the DSP and the SRC chips. The DSP output data format is SPI (32 bits per word two words per frame). DSP chip IC706 receives a 128kHz frame clock at its WST input (pin 50) that sets the word transfer rate to eight words per 32kHz period. The SRC receives a 32kHz clock at its L/R*_I input (pin 6). L/R*_I delineates the left and right samples used by the SRC; therefore the SRC uses the

first sample received for the left input and the fifth sample for the right input. The DSP output samples are formatted to ensure that the SRC uses a left and right output pair that represent the simultaneously sampled analog input.

The crystal oscillator (Y602) provides the SRC a master clock of 16.384MHz on pin 2. This MCLK frequency allows the output SRC to operate with an output sample rate in the range between 30kHz and 57kHz (operation between 8kHz and 30kHz will result in a one sample delay between the left and right channels). SRC_RST is an active low reset signal tied to pin 13 of the SRC. This signal is controlled by the Z-180 via pin 2 of latch IC609.

The MSDLY_I, BKPOL_I, and TRGLR_I pins of the SRC chip configure the chip for SPI format. Pin 1 of the SRC (GPDLYS) is tied high to minimize the chip's group delay to approximately 700µs as opposed to approximately 3ms, giving up some tolerance to variations in sample rates. Pin 28 (SETLSLW) is tied high to cause the SRC to settle slowly to changes in sample rates, resulting in the best rejection of sample rate jitter.

The output side of the sample rate converter is tied directly to IC616, an AES/EBU digital audio transmitter integrated circuit. This interface uses the SPI format with the AES transmitter as master. The transmitter chip encodes the audio data it receives to the AES/EBU interface standard, and transmits it.

The SRC output sample rate and the sample rate that the AES/EBU transmitter transmits with is based on the MCK clock provided to pin 5 of IC616. This clock is received via digital multiplexer chip IC610 which is used to select one of four available clocks. Three free running clocks provide the standard sample rates of 32kHz, 44.1kHz and 48kHz when an internal sync is requested. These clocks run at a frequency that is 128 times the sample rate they represent. They have a frequency stability of ±100PPM. The fourth clock is the EXTMCK clock that is recovered from the AES/EBU receiver chip. This clock has a frequency of 256 times the input sample rate of the received signal. This is used to drive the output AES/EBU transmitter when an output sample rate is required that is synchronous to the input sample rate (external sync).

The inter-chip serial data format, the input MCK multiplication factor, and the output channel status data are controlled by the Z-180 via internal control registers and data memory accessed through the parallel port made up of the 5-bit address bus (pins 9-13), the 8-bit data bus (pins 1-4, 21-24) and the CS* and RD/WR* control pins (pins 14 and 16) of IC616.

The on-chip RS422 line driver provided by IC616 is a low skew, low impedance, differential output capable of driving a 110Ω transmission line with a 4Vp-p signal. Shielded 1:1 pulse transformer T601 transmits the differential digital output signal to XLR connector J601. T601 has very low inter-winding capacitance, providing a high level of isolation from high frequency common mode interference.

Composite Output Circuits

This circuitry provides several functions. It interfaces the digital stereo multiplex output from the stereo encoder DSP to a digital-to-analog (D/A) converter, which converts it to an analog signal. The low-pass reconstruction filter removes high frequency images from the D/A converter output and feeds the output buffers. Two output stages with separate level controls buffer the stereo multiplex signal and feed the composite output connectors.

1. Digital-to-Analog (D/A) Converter

The composite D/A is a single chip, 18-bit resistor ladder type. It has a single channel serial input that receives the digital stereo encoded output samples from the DSP.

Component-Level Description:

IC500 is the digital-to-analog converter for the stereo-encoded composite signal. The synchronous serial input interface consists of the bit clock, data and latch enable pins. DSP IC707 provides serial data (COMP_O) to pin 7 of the composite D/A.

An 8.192MHz bit clock is provided from the system clock circuitry to both the DSP and the D/A chips. The DSP output data format is 32-bits per word two words per frame, MSB first (first 24-bits are significant). DSP IC707 receives a 128kHz frame clock at its WST input (pin 50) that sets the word transfer rate to 256kHz. The D/A receives a 256kHz clock at its latch enable (LE) input (pin 6). The D/A uses the last 18-bits received prior to the falling edge of LE (last 18-bits are significant). Flip-flop IC604-A is used to invert and shift the 256kHz system clock to produce an LE signal that has a falling edge aligned with the 18th significant data bit.

Pin 9 is the analog voltage output of IC500. The voltage changes to the current sample value on the falling edge of the 256kHz clock. A full scale output is approximately ±3.0Vpeak, which corresponds to 141% modulation. C517 prevents slew-induced distortion.

2. Analog Reconstruction Filter

The reconstruction filter removes the ultrasonic energy “images” present at the D/A output. It is a passive seventh-order elliptic filter with a cutoff frequency of approximately xx70kHz and xx90dB stopband attenuation above xx203kHz.

Component-Level Description:

The reconstruction filter is a passive seventh-order LC ladder filter, realized by resistors R501, R502 and R504, capacitors C508-C512, C516, and C518, and inductors L500-L502. The frequency response of this filter cannot be measured by applying a swept sine wave at the 2200/2200-D analog inputs. This is because

the filter has bandwidth much larger than the analog-to-digital converter. The analog-to-digital converter band-limits the input to 16kHz. Stereo separation is a very sensitive function of the frequency and phase response of this filter in the frequency range of 20-53,000Hz.

The filter is buffered by non-inverting amplifier IC502-A and applied to the output stages. IC501-A is a DC servo to prevent DC from appearing at the composite outputs.

3. Composite Baseband Output Stages

The buffered filter output is applied to two power buffers each capable of driving two 75Ω loads in parallel.

Component-Level Description:

The stereo modulator output is fed into two separate output buffers. The first is made up by IC503-A and IC504. IC504 is a special high slew rate power buffer which is located within the overall amplifier feedback loop. It isolates IC503-A from the destabilizing effects of capacitive loads and also permits 75Ω loads to be driven without degradation. This line driver will drive up to ±1.5Vpeak into 0.047uF in parallel with 37.5Ω before significant nonlinear errors (increases in spurious components as observed on a baseband spectrum analyzer) or linear errors (noticeable deterioration of baseline flatness at 15kHz in the separation test mode) are apparent. Output level is adjusted by varying the feedback resistor VR500. The second output buffer made by IC505-A and IC506 is functionally identical to the one just described.

DSP Circuits

The DSP circuits consist of eight general purpose DSP chips that execute DSP software code to implement digital signal processing algorithms. The algorithms filter, compress, limit, and stereo encode the audio signal. The eight DSP chips, operating at 25 million instructions per second (MIPS) for a total of 200MIPS, provide the necessary signal processing. A 32kHz sampling rate is used. Two of the on-board serial audio interface (SAI) peripherals on each DSP chip are used to transfer data chip-to-chip at a 16.384Mbit/s rate maintaining a 24-bit word length. The DSP chips are cascaded, processing the audio serially. The first chip receives the analog input via the A/D chip and the digital input via the SRC chip. Input source selection is performed seamlessly, internal to the DSP chip.

During system initialization (which normally occurs when power is first applied to the 2200/2200-D), and when processing algorithms are changed, the Z-180 downloads the DSP executable code stored in the ROM, via the serial host interface (SHI) port of each DSP chip. Once a DSP chip begins executing its program, execution is continuous. The Z-180 provides the DSP program with parameter data, and extracts the front panel metering data from the DSP chips via this same SHI port.

The left and right analog and digital outputs are sent to the L/R output D/A and the output SRC chip via the SAI port of DSP chip IC706. The last DSP chip (IC707) outputs the composite audio signal on its SAI port where it is directed to the composite D/A.

Component-Level Description:

IC700 thru IC707 are the DSP chips. Do not attempt to remove these chips from the PCB. These chips should be removed only by the Orban service department. A chip can be ruined by static discharge or by damage to its delicate pins.

The EXTAL pin of each DSP chip receives a 2.048MHz clock. All DSP chips use their internal PLL to multiply this by 24 to operate the chip's internal oscillator (Fosc) at 49.152MHz. Each DSP chip is reset by the Z-180 via latch IC709. DSP mode configuration is controlled by the state of the MODA, MODB and MODC (pins 37, 38, 39) on each chip as the chip is brought out of reset. All DSP chips are configured to bootstrap via the SHI port. The MODB pin, which also serves as the IRQB input after leaving the reset state, is forced low prior to bringing the DSP chips out of reset.

Pins 26, 35, 41 and 42 comprise the DSP host port. Host port communication conforms to the SPI format with the Z-180 set-up as the master and the DSPs as slaves. The Z-180 generates the HOSTCK clock signal and provides it to SCK (pin 26) of each DSP. The Z-180 provides the data on the HOSTTX line tied to pin 41 of each DSP. The data output (pins 35) of each DSP have tri-state outputs that are wire-ORed to provide the data on the HOSTRX line sent to the Z-180. The Z-180 controls the slave select (SS*) (pin 42) of each DSP via latch IC708. The SS* pin is used to enable each of the slaved DSP SPI ports for transfer.

DSP IC700 pins 56 and 57 receive serial stereo audio from the digital and analog inputs. These are the two input ports of the synchronous serial audio interface (SAI) receiver internal to the DSP. The communication protocol is SPI with DSP as a slave, and L/R input A/D converter IC312 as master. Left and right data words, each of 32-bit length, constitute a frame. 18 significant bits are received from the analog input A/D and 20 significant bits are received from the digital input SRC. The two serial stereo audio streams are received simultaneously. Both inputs share the same frame clock, L*/R (32kHz) provided to DSP IC700 pin 55 and the same bit clock, SCK (2.048MHz) provided to DSP IC700 pin 51.

Communication between DSP chips IC700 (first) thru IC707 (last) is one-way, in series from the first to the last. Two of the on-board SAI peripherals on each DSP are used to transfer 8 words each per frame chip-to-chip. The SPI communication protocol (two 32-bit words per cycle of the word clock) is used with the DSPs as slaves, and the 2200/2200-D system clocking as master. Data is sent from the two transmit data port pins 46 and 47 of one chip to the next chip's receive data port pins 56 and 57. A 128kHz word clock is provided to the transmit pin 50 and the receive pin 55. An 8.192MHz bit clock is provided to the transmit pin 49 and the receive pin 51. The SAI links between DSPs are synchronized to each other (to align the SAI time slots) by making the first occurrence of all IRQBs coincident, (controlled by Z180 and external hardware) and having all DSPs initialize their SAI ports on the first reception of IRQB.

The “analog” and digital outputs are transferred respectively to the L/R output D/A and the output SRC from the second to the last DSP chip (IC706). These signals are identical except for any De-Emphasis, J.17 Pre-Emphasis, J.17 Emphasis makeup gain, or output attenuation (DO 100% level) applied to the digital output. The “analog” output is also passed on to the last DSP chip (IC707) for stereo encoding. (“Analog” refers to DSP signal that ultimately gets converted to analog.)

The composite FM stereo signal is output from the last DSP chip (IC707) via its SAI transmitter, formed by DSP IC707 pins 47, 49, and 50. A communication protocol compatible with the composite D/A (IC500) is used with the DSP and D/A as slave and the 2200/2200-D system clocking as master. The serial composite audio bit stream output on pin 47 feeds D/A IC500 pin 7. DSP IC707 pin 50 receives a 128kHz frame clock and pin 49 receives an 8.192MHz bit clock. Two consecutive composite audio data words, each of 32-bit length, constitute a frame.

Power Supply

The power supply converts an AC line voltage input to various power sources used by the 2200/2200-D. Five linear regulators provide ±15VDC and ±5VDC for the analog circuits and +5VDC for the digital circuits. An unregulated voltage powers the LED meters and the LED backlight on the LCD display.

Component-Level Description:

L1 is a power line filter that filters out RFI. F1 is a ½-amp “Slo-Blo” fuse. T1 is a dual-primary dual-secondary power transformer used to step down the input voltage for the ±15VDC analog and +5VDC digital supply regulators. Each primary winding has a Metal-Oxide Varistor (V1, V2) connected in parallel to suppress high-voltage spikes across the AC line. Rear panel switch S1 configures the primary windings either in parallel (for 115V ±15% line voltages) or series (for 230V ±15% line voltages).

T1 has two pairs of secondary windings for stepping down the AC line voltage. The lower voltage pair is configured in parallel, and feeds storage capacitors C15 and C19 through full-wave bridged rectifier diodes CR13, CR14, CR15, CR17 and CR18. C15 filters the rectified voltage for input to low-dropout linear voltage regulator IC5, which provides the +5VDC source used to power all of the digital circuits in the 2200/2200-D. C19 filters the rectified voltage to power the LED backlight on the LCD display, and the LED meters. Components Q1, Q2, R3-R7, and CR20 form a pulsed current source to illuminate the 25x2 LED array (the backlight on the LCD display). The signal LEDPULSE, a 32kHz pulse at ⅛ duty cycle, feeds the base of high-current Darlington transistor Q1. The feedback circuit consisting of Q2, CR20 and R3-R7 controls the magnitude of the signal LEDPULSE so as to limit Q1’s current pulses to about 1.5A (1/8 duty cycle). These current pulses illuminate the 25 x 2 LED array via keyed header J201, which attaches the LED array between the collector of Q1 and supply cap C19. The signal LEDPULSE is gated on for approximately one hour after the 2200 has last been powered up or a front panel button has last been pressed; otherwise, it is gated off. This drastically increases the lifetime of the LCD display and saves

about 2 Watts power. The LED meter circuits are described in “User Control Interface and LED Display Circuits.”

The higher voltage pair of transformer secondary windings is configured in series to form a single center-tapped winding. This winding is connected to rectifier diodes CR1-CR4 in a full-wave center tap configuration. C1 and C2 filter the rectified voltage for input to the voltage regulators IC1 and IC2. These regulators provide the +15VDC and −15VDC sources used to power most of the analog circuits in the 2200/2200-D. They also serve as the respective inputs to the voltage regulators IC3 and IC4. These regulators provide the +5VDC and −5VDC analog supplies for the converter chips, which draw only a modest amount of current.

Test points and supply bypass capacitors are placed throughout the PC board. S2 is the ground lift switch used to connect or lift 2200/2200-D circuit ground from chassis ground.

Parts List

Parts are listed by ASSEMBLY, then by TYPE, then by REFERENCE DESIGNATOR. Widely used common parts are not listed; such parts are described generally below (examine the part to determine exact value). See the following assembly drawings for locations of components.

SIGNAL DIODES, if not listed by reference designator in the following parts list, are:

Orban part number 22101-000, Fairchild (FSC) part number 1N4148, also available from many other vendors. This is a silicon, small-signal diode with ultra-fast recovery and high conductance. It may be replaced with 1N914 (BAY-61 in Europe).

(BV: 75V min. @ Ir = 5μA; Ir: 25nA max. @ Vr = 20V; Vf: 1.0V max. @ If = 100mA; trr: 4ns max.) See Miscellaneous list for ZENER DIODES (reference designator VRxx).

RESISTORS should only be replaced with the same style and with the exact value marked on the resistor body. If the value marking is not legible, consult the schematic or the factory. Performance and stability will be compromised if you do not use exact replacements.

Unless listed by reference designator in the following parts list, you can verify resistors by their physical appearance:

Metal film resistors have conformally-coated bodies, and are identified by five color bands or a printed value. They are rated at ⅛ watt @ 70°C, ±1%, with a temperature coefficient of 100 PPM/°C. Orban part numbers 20038-xxx through 20045-xxx, USA Military Specification MIL-R-10509 Style RN55D. Manufactured by R-Ohm (CRB-1/4FX), TRW/IRC, Beyschlag, Dale, Corning, and Matsushita.

Carbon film resistors have conformally-coated bodies, and are identified by four color bands. They are rated at ¼ watt @ 70°C, ±5%. Orban part numbers 20001-xxx, Manufactured by R-Ohm (R-25), Piher, Beyschlag, Dale, Phillips, Spectrol, and Matsushita.

Carbon composition resistors have molded phenolic bodies, and are identified by four color bands. The 0.090 x 0.250 inch (2.3 x 6.4 mm) size is rated at ¼ watt, and the 0.140 x 0.375 inch (3.6 x 9.5 mm) size is rated at ½ watt, both ±5% t numbers 2001x-xxx, USA Military Specification MIL-R-11 Style RC-07 (¼ watt) or RC-20 (½ watt). Manufactured by Allen-Bradley, TRW/IRC, and Matsushita.

Cermet trimmer resistors have ⅜-inch (9 mm) square bodies, and are identified by printing on their sides. They are rated at ½ watt @ 70°C, = ±10%, with a temperature coefficient of 100 PPM/°C. Orban part numbers 20510-xxx and 20511-xxx. Manufactured by Beckman (72P, 68W- series), Spectrol, and Matsushita.

Obtaining Spare Parts

Special or subtle characteristics of certain components are exploited to produce an elegant design at a reasonable cost. It is therefore unwise to make substitutions for listed parts. Consult the factory if the listing of a part includes the note “selected” or “realignment required.”

Orban normally maintains an inventory of tested, exact replacement parts that can be supplied quickly at nominal cost. Standardized spare parts kits are also available. When ordering parts from the factory, please have available the following information about the parts you want:

Orban part number
Reference designator (e.g., C3, R78, IC14)
Brief description of part
Model, serial, and “M” (if any) number of unit — see rear-panel label

To facilitate future maintenance, parts for this unit have been chosen from the catalogs of well-known manufacturers whenever possible. Most of these manufacturers have extensive worldwide distribution and may be contacted through their local offices. Addresses for each manufacturer’s USA headquarters are given on page 6-33.

MAIN BOARD ASSEMBLY

Capacitors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
C11-C62	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C65	Met. Polyester, 50V, 5%; 1.0uF	21445-510	PAN	ECQ-V1H105JZ		
C66-C78	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C82-C84	Alum., Radial, 25V, 10%; 10uF	21263-610	NIC	UKLIE101KPAANA		
C85-C90	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C91, C92	Alum., Radial, 25V, 10%; 10uF	21263-610	NIC	UKLIE101KPAANA		
C100, C101	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C102	Alum., Radial, 63V, -20% +100%; 2.2uF	21209-522	SPR	502D 225G063BB1C	PAN	
C103	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C200	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C201	Met. Polyester, 50V, 5%; 0.1uF	21445-410	PAN	ECQ-V1H104JZ		
C300	Met. Polyester, 50V, 5%; 0.1uF	21445-410	PAN	ECQ-V1H104JZ		
C301	Met. Polyester, 50V, 5%; 0.1uF	21445-410	PAN	ECQ-V1H104JZ		
C302-C305	Met. Polyester, 50V, 5%; .0047uF	21445-247	PAN	ECQ-B1H472 F1		
C306, C307	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C308	Tantalum, 10V, 10%; 100uF	21303-710	SPR	196D 107X9010PE4	MANY	
C309, C310	Met. Polyester, 50V, 5%; 0.22uF	21445-422	PAN	ECQ-V1H224JZ		
C311	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C312	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C313, C314	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C315	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C316-C319	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C320	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C321, C322	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C323-C326	Ceramic, Axial, 100V, 5%; 1000pF	21127-210	KEM	C410C102J1G5CA		
C400	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C401, C402	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C403	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C404, C405	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C406	Tantalum, 20V, 10%; 10uF	21305-610	SPR	196D 106X9020JA1	MANY	
C407, C408	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C409	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		

FOOTNOTES:
(1) See page 6-36 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Main Board Assembly - Capacitors.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Capacitors (continued)						
C410, C411	Mica, 500V, 1%; 1500pF	21022-215	CD	CD19-FD152F03	SAN	
C412	Ceramic, Axial, 100V, 5%; 10pF	21127-010	KEM	C410C100J1G5CA		
C413	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C414	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C415	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C416, C417	Mica, 500V, 1%; 1500pF	21022-215	CD	CD19-FD152F03	SAN	
C418	Ceramic, Axial, 100V, 5%; 10pF	21127-010	KEM	C410C100J1G5CA		
C419, C420	Met. Polyester, 50V, 5%; 0.1uF	21445-410	PAN	ECQ-V1H104JZ		
C500	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C501	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C503, C504	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C505	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C506	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C507	Tantalum, 35V, 10%; 1uF	21307-510	SPR	196D 105X9035HA1	MANY	
C508	Mica, 1500V, 5%; 390pF	21018-139	CD	CD15-FD391F03	SAN	
C509	Mica, 500V +1/2pF -1/2pF; 15pF	21017-015	CD	CD15-CD150D03	SAN	
C510	Mica, 500V, 1%; 820pF	21022-182	CD	CD19-FD821F03	SAN	
C511	Mica, 500V, 1%; 620pF	21022-162	CD	CD19FD621F03		
C512	Mica, 500V, 1%; 220pF	21018-122	CD	CD15-FD221F03	SAN	
C513, C514	Mica, 500V, 1%; 51pF	21018-051	CD	CD15ED510F03		
C515	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C516	Mica, 500V, 1%; 51pF	21018-051	CD	CD15ED510F03		
C517	Ceramic Disc, 100V, 5%; 68pF	21127-068	KEM	C410C680JICG5CA		
C518	Mica, 500V, +1/2pF -1/2pF; 33pF	21017-033	CD	CD15-CD330D03	SAN	
C519	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C520	Met. Polyester, 50V, 5%; 0.1uF	21445-410	PAN	ECQ-V1H104JZ		
C521, C522	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
C523	Ceramic, Axial, 100V, 5%; 680pF	21127-168	KEM	C410C681J1G5CA		
C524	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C525	Ceramic, Axial, 100V, 5%; 680pF	21127-168	KEM	C410C681J1G5CA		
C600	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C601	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C602	Met. Polyester, 50V, 5%; .047uF	21445-347	PAN	ECQ-V1H473JZ		
C603	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		

FOOTNOTES:
(1) See page 6-36 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Main Board Assembly - Capacitors.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Capacitors (continued)						
C604	Ceramic Disc, 100V, 5%; 150pF	21127-115	KEM	C410C151JIG5CA		
C606	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C607	Alum., Radial, 25V, 10%; 100uF	21263-710	NIC	UKLIE101KPAANA		
C608	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C609, C611	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C612, C613	Ceramic Disc, 100V, 5%; 33pF	21127-033	KEM	C410C330JIG5CA		
C800	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C801	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C802	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C803	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C804	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C805	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C806	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C807	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C808	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C809	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C810	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C811	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C812	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C813	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
C814	Met. Polyester, 50V, 5%; 0.01uF	21445-310	PAN	ECQ-V1H103JZ		
C815	Ceramic, 50V, 20%; 1uF	21131-410	MUR	GRM42-6Z5U104M50BD		
Diodes						
CR102-CR109	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
CR300-C307	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800	MANY	
Inductors						
L100	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50		(2)
L300	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L301	Inductor, RF Choke; 1.2mH	29503-000	MIL	73F123AF		
L302	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L303	Inductor, RF Choke; 1.2mH	29503-000	MIL	73F123AF		
L304	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200

Main Board Assembly - Capacitors, Diodes, Inductors.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Inductors (continued)						
L305	Inductor, RF Choke; 1.2mH	29503-000	MIL	73F123AF		
L306	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L307	Inductor, RF Choke; 1.2mH	29503-000	MIL	73F123AF		
L400, L401	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50	(2)	
L402, L403	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L404, L405	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50	(2)	
L406, L407	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L500	Inductor, Variable	29705-008	ORB			
L501	Inductor, Variable	29705-012	ORB			
L502	Inductor, Variable	29705-009	ORB			
L600-L603	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
L802-L804	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50	(2)	
Integrated Circuits						
IC100	Digital, Microprocessor	24822-000	ZI	Z8018010VSC		
IC101-IC104	Address Decoder	24899-000	MOT	MC74AC138D		
IC105	Digital, EPROM	24829-000	TI	TMS27C010A-10JL		
IC106	Digital, SRAM	24817-000	TOS	TC55257CPL-10		
IC107	Serial EEPROM	24898-000	NAT	NM25C04M8		
IC109	Digital, Inverter	24900-000	TI	SN74HC14AD		
IC110-IC117	Optoisolator, NPN	25003-000	SIE	SFH-601-1		
IC118, IC119	Digital, Inverter	24900-000	TI	SN74HC14AD		
IC120	Digital, Transceiver	24851-000	SIG	74HC245D		
IC122	Power Monitor/Watchdog	24872-000	MAX	1232CPA		
IC201	Digital, AND Gate	24850-000	MOT	MC74HC08AD		
IC300	Audio Preamp	24727-402	AD	SSM-2017P		
IC301	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC302	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC303	Digital, Latch	24857-000	MOT	MC74HC374ADW		
IC304	Digital, Octal Buffer	24902-000	MOT	MC74HC14AD		
IC305	Digital, Latch	24857-000	MOT	MC74HC374ADW		
IC306	Quad Comparator	24710-302	NAT	LM339		
IC307	Quad SPST Switches	24728-302	AD	ADG222		
IC308	Audio Preamp	24727-402	AD	SSM-2017P		

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Main Board Assembly - Inductors, Integrated Circuits.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Integrated Circuits (continued)						
IC309	Quad SPST Switches	24728-302	AD	ADG222		
IC310	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC311	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC312	Digital, A/D Converter	24643-000	CSC	CS5389KP-EP		
IC313	Digital, Flip-Flop	24858-000	TI	SN74HC74D		
IC314	Digital, AND Gate	24850-000	MOT	MC74HC08AD		
IC400	Digital, Stereo D/A Converter	24821-000	CSC	CS4328KP		
IC401	Digital, Multiplying DAC	24714-302	AD	AD7524JN		
IC402	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC403	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC404	Digital, Multiplying DAC	24714-302	AD	AD7524JN		
IC405	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC406	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC407	Quad Comparator	24710-302	NAT	LM339		
IC408	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC500	Digital, D/A Converter	24742-000	AD	AD1861N		
IC501	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC502, IC503	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC504	Power Buffer	24707-102	LT	LT1010CH		
IC505	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC506	Power Buffer	24707-102	LT	LT1010CH		
IC600	Digital, AES Receiver	24847-000	CSC	CS8412CS		
IC601	Digital, Transceiver	24851-000	SIG	74HC245D		
IC602	Digital, NAND Gate	24853-000	MOT	MC74HC00AD		
IC603	Digital, Sample Rate Conveter	24733-000	AD	AD1890JP		
IC604	Digital, Flip-Flop	24858-000	TI	SN74HC74D		
IC605	Digital, Inverter	24900-000	TI	SN74HC14AD		
IC606	Digital, AND Gate	24850-000	MOT	MC74HC08AD		
IC609	Digital, Latch	24857-000	MOT	MC74HC374ADW		
IC610	Digital, Multiplexer	24896-000	MOT	MC74HC153D		
IC611	Digital, Latch	24857-000	MOT	MC74HC374ADW		
IC612	Digital, Flip-Flop	24858-000	TI	SN74HC74D		
IC613	Digital, PAL	44032-100	ORB			
IC614	Digital, AND Gate	24850-000	MOT	MC74HC08AD		

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Main Board Assembly - Integrated Circuits.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Integrated Circuits (continued)						
IC615	Digital, Sample Rate Conveter	24733-000	AD	AD1890JP		
IC616	Digital, Audio Interface	24644-000	CRY	CS8401ACP		
IC618	PAL	44031-100	ORB			
IC619	Digital, PLL	24901-000	SIG	74HC4046AD		
IC700-IC707	Digital, DSP	24897-000	MOT	DSP56004FJ50		
IC708, IC709	Digital, Latch	24857-000	MOT	MC74HC374ADW		
IC710	Digital, AND Gate	24850-000	MOT	MC74HC08AD		
Resistors						
R100	Resistor, 1/4W; 0 OHM (Jumper)	20020-025	ROHM	JPW-02A		
R106, R124	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
R127	Resistors, MF, 1/2W, 1%; 300 OHM	20080-300	DAL	RNC55J		
R349	Resistor, 1/4W; 0 OHM (Jumper)	20020-025	ROHM	JPW-02A		
R411	Resistors, MF, 1/8W, 0.1%, 13.3K	20059-133	SEI	RN 1/8 13.3K .1%		
R412	Resistors, MF, 1/8W, 0.1%, 10.2K	20059-102	SEI	RN 1/8 10.2K .1%		
R413	Resistors, MF, 1/8W, 0.1%; 15.4 OHM	20056-154	DAL	RNC55J		
R415	Resistors, MF, 1/8W, 0.1%, 4.64K	20058-464	SEI	RN 1/8 4.64K .1%		
R416	Resistors, MF, 1/8W, 0.1%, 4.53K	20058-453	SEI	RN 1/8 4.53K .1%		
R417	Resistors, MF, 1/8W, 0.1%, 4.53K	20058-453	SEI	RN 1/8 4.53K .1%		
R418	Resistors, MF, 1/8W, 0.1%; 3.01K	20058-301	SEI	RN 1/8 3.01K .1%		
R419	Resistors, MF, 1/8W, 0.1%, 4.64K	20058-464	SEI	RN 1/8 4.64K .1%		
R420	Resistors, MF, 1/8W, 0.1%; 15.4 OHM	20056-154	DAL	RNC55J		
R421	Resistors, MF, 1/8W, 0.1%, 13.3K	20059-133	SEI	RN 1/8 13.3K .1%		
R422	Resistors, MF, 1/8W, 0.1%, 10.2K	20059-102	SEI	RN 1/8 10.2K .1%		
R430	Resistors, MF, 1/8W, 0.1%, 13.3K	20059-133	SEI	RN 1/8 13.3K .1%		
R431	Resistors, MF, 1/8W, 0.1%, 10.2K	20059-102	SEI	RN 1/8 10.2K .1%		
R432	Resistors, MF, 1/8W, 0.1%; 15.4 OHM	20056-154	DAL	RNC55J		
R435	Resistors, MF, 1/8W, 0.1%, 4.64K	20058-464	SEI	RN 1/8 4.64K .1%		
R436, R437	Resistors, MF, 1/8W, 0.1%, 4.53K	20058-453	SEI	RN 1/8 4.53K .1%		
R438	Resistors, MF, 1/8W, 0.1%; 3.01K	20058-301	SEI	RN 1/8 3.01K .1%		
R439	Resistors, MF, 1/8W, 0.1%, 4.64K	20058-464	SEI	RN 1/8 4.64K .1%		
R440	Resistors, MF, 1/8W, 0.1%; 15.4 OHM	20056-154	DAL	RNC55J		
R441	Resistors, MF, 1/8W, 0.1%, 13.3K	20059-133	SEI	RN 1/8 13.3K .1%		

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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200

Main Board Assembly - Integrated Circuits, Resistors.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Resistors (continued)						
R442	Resistors, MF, 1/8W, 0.1%, 10.2K	20059-102	SEI	RN 1/8 10.2K .1%		
R501	Resistors, MF, 1/8W, 0.1%; 3.57K	20058-357	DAL	RNC55J		
R502	Resistors, MF, 1/8W, 0.1%; 300OHM	20058-475	DAL	RNC55J		
R602, R603	Resistor, 1/4W; 0 OHM (Jumper)	20020-025	ROHM	JPW-02A		
VR500, VR501	Trimpot, Cermet, 20 Turn; 25K	20512-325	BEK	89PR25K	BRN	
Switches						
S209	Switch, Rotary, Encoder	26081-000	ORB			
Transistors						
Q300-Q303	Transistor, JFET/N	23402-101	NAT	J108		
Q400-Q403	Transistor, JFET/N	23406-101	NAT	J113	SIL	
Miscellaneous						
J101	Connector, D Type, 25-pin	27017-025	AD	JMDF-25S		
J300, J304	Connector, XLR, PC Mount, Female	27054-003	NEU	NC 3 FD-H		
J400, J401	Connector, XLR, PC Mount, Male	27053-003	NEU	NC 3 MD-H		
J600	Connector, XLR, PC Mount, Female	27054-003	NEU	NC 3 FD-H		
J601	Connector, XLR, PC Mount, Male	27053-003	NEU	NC 3 MD-H		
T600, T601	Transformer, Surface Mount	29015-000	ORB			
Y601	Crystal; 11.2896MHz	28071-000	ORB			
Y602	Oscillator; 16.384MHz	28074-001	ORB			

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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Main Board Assembly - Resistors, Swirtches, transistors Miscellaneous.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
POWER SUPPLY BOARD ASSEMBLY						
Capacitors						
	Alum, Radial, 16V; 6800uF	21255-000	PAN	ECOS1CA682AA		
	Alum, Radial, 35V; 1000uF	21256-000	PAN	ECEA1VGE102		
	Ceramic, Axial, 50V, 20%; 0.1uF	21129-410	KEM	C410C104M5UCA		
	Alum, Radial, 25V; 47uF	21206-747	PAN	ECEAIEU471		
	Alum., Radial, 25V, 10%; 100uF	21263-710	NIC	UKLIE101KPAANA		
Diode						
	Diode, Rectifier	22015-000	TAT	SBL-1630CT		
	Diode, Zener, 1W, 5%; 5.6V	22004-056	MOT	1N4734A		
	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
Integrated Circuits						
	Regulator, 5V	24321-000	LT	LT1086CK-5		
	D.C. Regulator, 15V Negative	24303-901	NAT	LM79M15AUC	TI,MOT	
	D.C. Regulator, 15V Positive	24304-901	NAT	LM78M15UC	TI,MOT	
	D.C. Regulator, 5V Positive	24307-901	NAT	LM78M05C	TI,MOT	
	D.C. Regulator, 5V Negative	24308-901	NAT	LM79M05C	TI,MOT	
Miscellaneous						
	Transformer, Power	55033-000	ORB			
	Varistor	22500-271	PAN	ERZ-C10DK271U		
	Switch, Slide, Mains voltage selector	26148-000	SW	EPS2-PC3		
	Switch, Slide, SPDT	26146-000	ECG	SSP1-S1-M7-Q-E-A		
	Filter, Line	28012-000	DEL	03ME1		
	Fuseholder, PC Mount	28112-001	LFE	345-101-01		
	Insulator, Silicone, Thermal (TO-3)	15023-001	CHM	60-11-4511-1674	Chomerics, Inc.	
	Fuse, 3AG, Slo-Blo, 1/2A	28004-150	LFE	313.500	BUS	
	Resistor, CF, 1/2W, 5%; 2.0 OHM	20021-920	ORB			
	Transistor, Power, NPN	23000-201	TI	TIP120		
	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Power Supply Board Assembly - Capacitors, Diodes, Integrated Circuits, Miscellaneous.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
FINAL ASSEMBLY						
Miscellaneous						
	Fuse, 3AG, Slo-Blo, 1/2A	~~28004-150~~	LFE	313.500	BUS	

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-FM 2200
Final Assembly - Miscellaneous.

Vendor Codes

AB Rockwell Allen-Bradley
625 Liberty Ave
Pittsburgh, PA 15222-3123

AD Analog Devices, Inc.
One Technology Way
PO Box 9106
Norwood, MA 02062-9106

AKG AKG Acoustics, Inc.
See Orban

AM Amphenol Corporation
358 Hall Avenue
Wallingford, CT 06492

BEK Beckman Industrial Corporation
4141 Palm Street
Fullerton, CA 92635-1025

BEL Belden Electronic Wire & Cable
PO Box 1980
Richmond, IN 47374

BRN Bourns, Inc
Resistive Components Group
1200 Columbia Avenue
Riverside, CA 92507

BUS Bussmann Division
Cooper Industries
PO Box 14460
St. Louis, MO 63178

CD Cornell-Dubilier Electronics
1700 Rte. 23 North
Wayne, NJ 07470

CRL Mepcopal/Centralab
See Mepcopal

CSC Crystal Semiconductor Corporation
4210-T. South Industrial Dr.
Austin, TX 78744

CTS CTS Corporation
907 North West Blvd.
Elkhart, IN 46514

CW CW Industries
130 James Way
Southampton, PA 18966

DBX dbx
A Harman International Company
8760 South Sandy Parkway
Sandy, UT 84107

DEL Delta Products Corp
3225 Laurel View Ct.
Fremont, CA 94538

DUR Duracell, Inc.
Berkshire Industrial Park
Bethel, CT 06801

ELSW Electro Switch
77 King Avenue
Weymouth, MA 02188

EMI Crompton Modutec
920 Candia Rd.
Manchester, NH 03109

EXR Exar Corporation
2222 Qume Dr.
PO Box 49007
San Jose, CA 95161-9007

FR Fair-Rite Products Corp.
PO Box J
Wallkill, NY 12589

FSC Fairchild Camera & Instr. Corp.
See National Semiconductor

GI General Instruments
Optoelectronics Division
See Quality Technologies

HA Harris Semiconductor
1301 Woody Burke Rd.
Melbourne, FL 32901

HO Hoyt Elect. Inst. Works
19 Linden St.
Penacook, NH 03303

HP Hewlett-Packard Co.
Components Group
640 Page Mill Road
Palo Alto, CA 94304

INS Intersil, Inc.
See Harris Semiconductor

ITW ITW Switches
An Illinois Tool Works Co.
6615 W. Irving Park Rd.
Dept. T
Chicago, IL 60634

KEM KEMET Electronics Corporation
Post Office Box 5928
Greenville, South Carolina 29606

KEY Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105

LFE Littlefuse
A Subsidiary of Tracor, Inc.
800 E. Northwest Hwy
Des Plaines, IL 60016

LT Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035

LUMX Lumex Opto/Components Inc.
292 E. Hellen Road
Palatine, IL 60067

MAL Mallory Capacitor Co.
7545 Rockville Rd.
PO Box 1284
Indianapolis, IN 46241

MAR Marquardt Switches, Inc.
2711-TR Route 20 East
Cazenovia, NY 13035

MAT Matsushita Electric Corp
of America
One Panasonic Way
Secaucus, NJ 07094

ME Mepcopal/Centralab
A North American Phillips Corp.
11468 Sorrento Valley Road
San Diego, CA 92121

MID Hollingsworth/Wearnes
1601 N. Powerline Rd.
Pampano, FL 33069

MIL J.W. Miller Division
Bell Industries
306 E. Alondra
Gardena, CA 90247

MOT Motorola Semiconductor
PO Box 20912
Phoenix, AZ 85036

MUR Murata Erie North America
2200 Lake Park Drive
Smyrna, GA 30080

NAT National Semiconductor Corp.
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95051

NEL Crystal Biotech
75 South Street
Hopkinton, MA 01748

NOB Noble U.S.A., Incorporated
5450 Meadowbrook Industrial Ct.
Rolling Meadows, IL 60008

OKI OKI Semiconductor
785 N. Mary Ave.
Sunnyvale, CA 94086-2909

OHM Ohmite Manufactoring Company
3601 Howard Street
Skokie, IL 60076

ORB Orban
A Harman International Company
1525 Alvarado Street
San Leandro, CA 94577

PAN Panasonic Industrial Company
Two Panasonic Way
7E-2T
Secaucus, NJ 07094

QT Quality Technologies, Inc.
610 North Mary Ave.
Sunnyvale, CA 94086

RAL Raltron Electronics Corp.
2315 NW 107th Ave.
Miami, FL 33172

RAY Raytheon Company
Semiconductor Division
350 Ellis Street
Mountain View, CA 94039

RCA RCA Solid State
See Harris Semiconductor

ROHM Rohm Electronics
3034 Owens Dr.
Antioch, TENN 37013

SAE Stanford Applied Engineering, Inc
340 Martin Avenue
Santa Clara, CA 95050

SAN Sangamo Weston Inc.
Capacitor Division
See Cornell-Dubilier

SCH ITT Schadow, Inc.
8081 Wallace Road
Eden Prairie, MN 55344

SIE Siemens Components Inc.
Heimann Systems Div.
186 Wood Avenue South
Iselin, NJ 08830

SIG Philips Components - Signetics
North American Phillips Corp.
811 E. Arques
Sunnyvale, CA 94088

SPR Sprague Electric Co.
41 Hampden Road
PO Box 9102
Manifold, MA 02048-9102

S.W. Seitchcraft
A Raytheon Company
5555 N. Elation Avenue
Chicago, IL 60630

AT Taiga America, Inc.
700 Frontier Way
Bensenville, IL 60106

TDK TDK Electronics Corporation
12 Harbor Park
Port Washington, NY 11050

TI Texas Instruments, Inc.
PO Box 655012
Dallas, TX 75265

TOS Toshiba America, Inc.
9740 Irvine Blvd.
Irvine, CA 92718

TRW TRW Electronics Components
Connector Division
1501 Morse Avenue
Elk Grove Village, IL 60007

VARO Micro Quality Semiconductor, Inc.
PO Box 469013
Garland, TX 75046-9013

WES Westlake
See Mallory Capacitor Co.

WIM Wima Division
2269 Saw Mill Rd.
Building 4C
PO Box 217
Elmsford, NY 10533

ZI ZILOG Inc.
210 Hacienda Ave.
Campbell, CA 95008

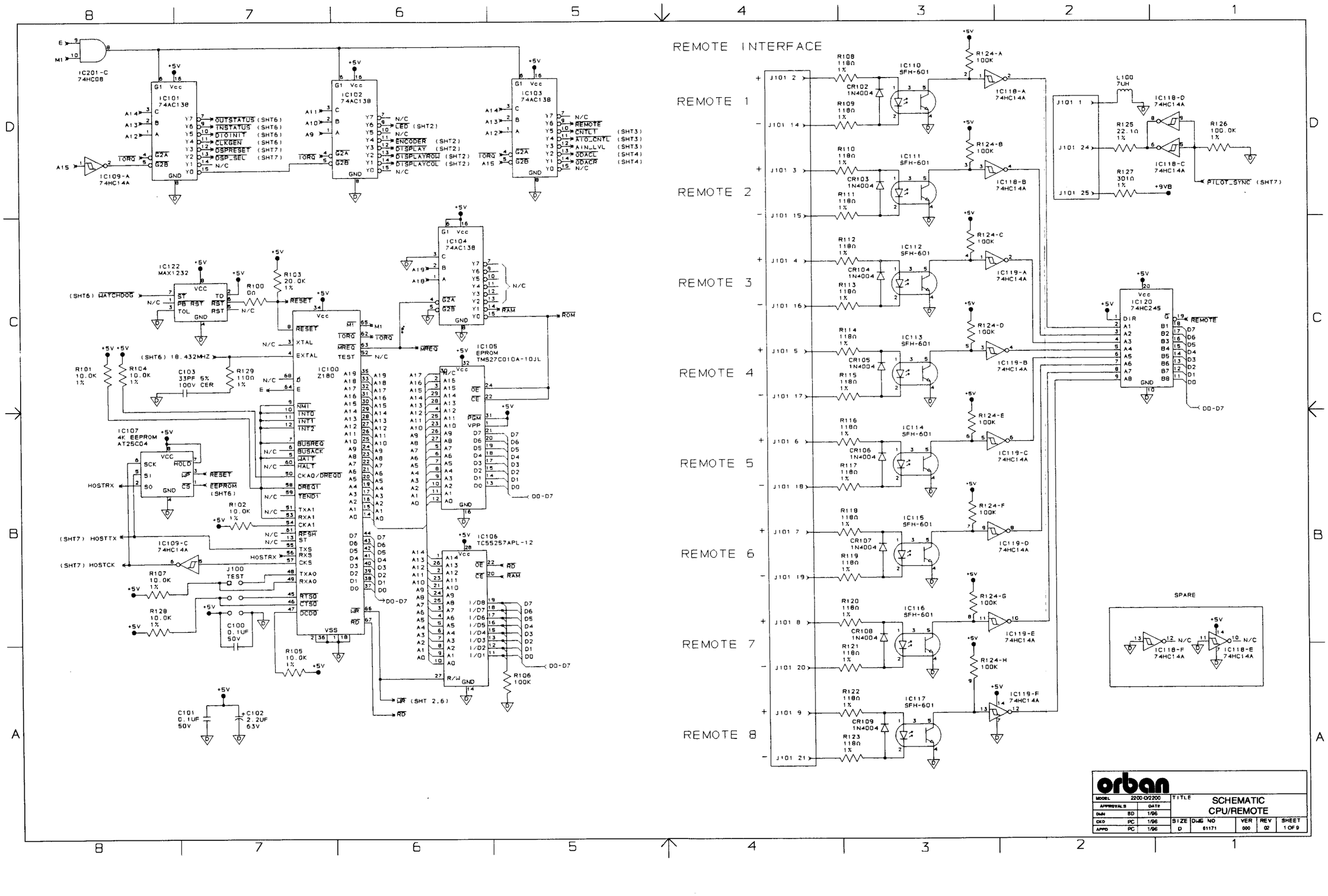
Schematics, Assembly Drawings

The following drawings are included in this manual:

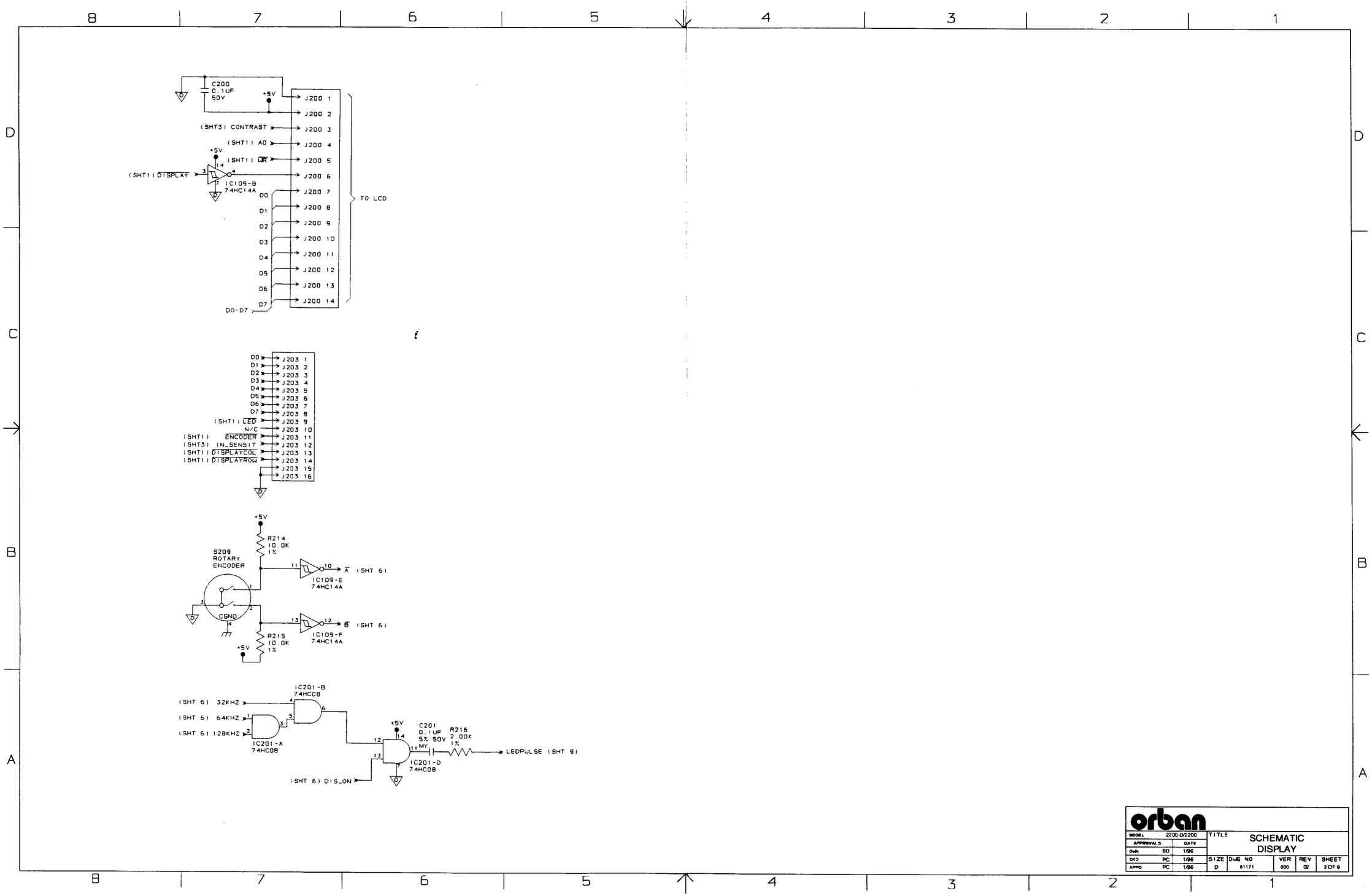
Page	Function	Circuit Board	Drawing
6-35	Block Diagram		Assembly Drawing
6-36	Audio Processing	Main	Assembly Drawing
6-37	CPU/Remote		Schematic 1 of 9
6-38	Display		2 of 9
6-39	Analog Input		3 of 9
6-40	Analog Output		4 of 9
6-41	Composite Output		5 of 9
6-42	Digital I/O		6 of 9
6-43	DSP 1		7 of 9
6-44	DSP 2		8 of 9
6-45	Power Distribution		9 of 9
6-46	Display, Controls	Display	Assembly Drawing
6-47	Display, Controls		Schematic 1 of 1
6-48	Power Supply	Power Supply	Assembly Drawing
6-49	Power Supply		Schematic 1 of 1
6-50	Power Supply (B)	Power Supply (B)	Assembly Drawing
6-51	Power Supply (B)		Schematic 1 of 1

These drawings reflect the actual construction of your unit as accurately as possible. Any differences between the drawings and your unit are almost undoubtedly due to product improvements or production changes since the publication of this manual.

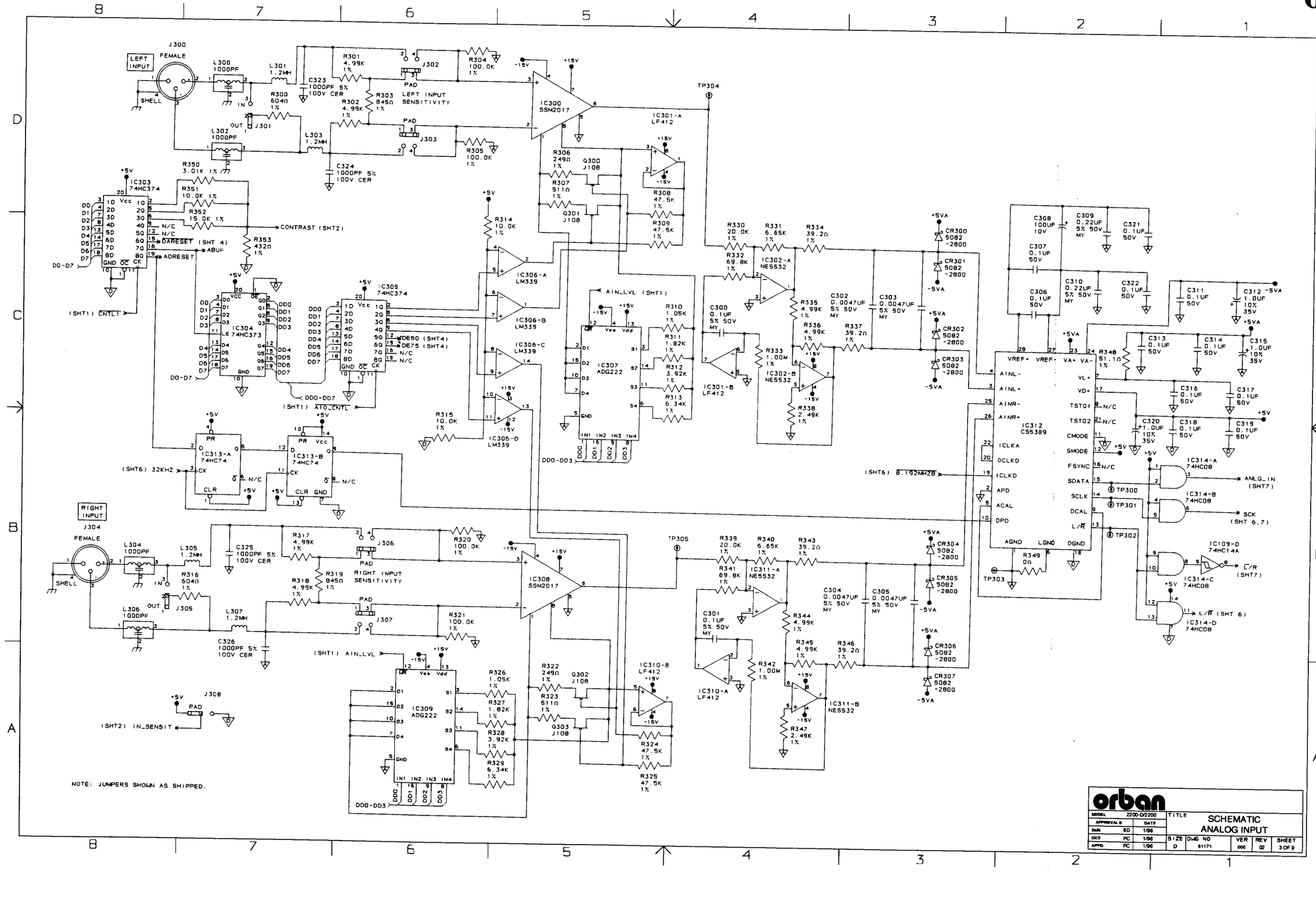
If you intend to replace parts, please read page 6-22

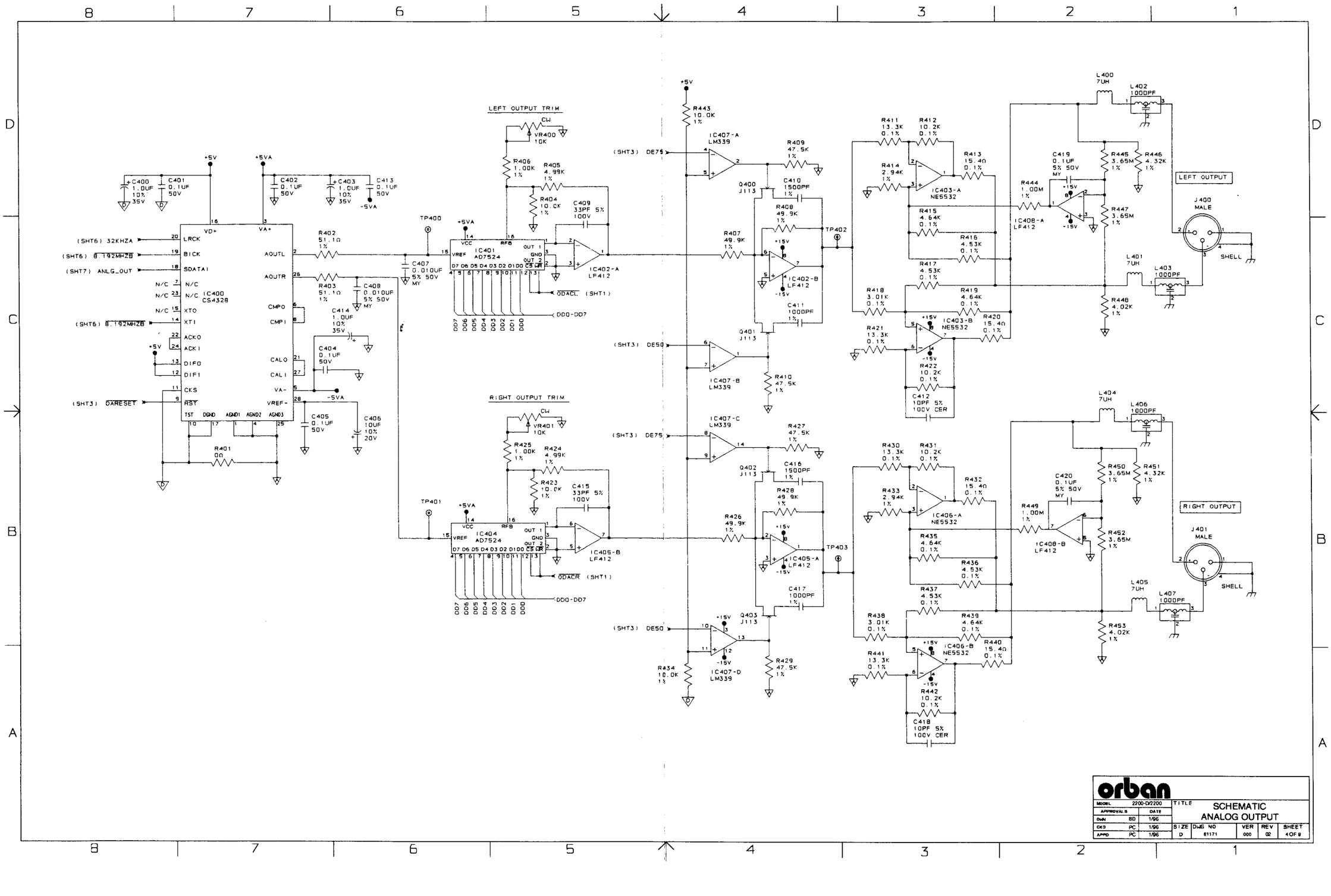


orban			
MODEL	2200-D/2200	TITLE	SCHEMATIC CPU/REMOTE
APPROVALS	DATE		
DWN	BD 1/96		
CKD	PC 1/96		
APPD	PC 1/96	SIZE D	DWG NO 61171
		VER 000	REV 02
		SHEET 1 OF 9	

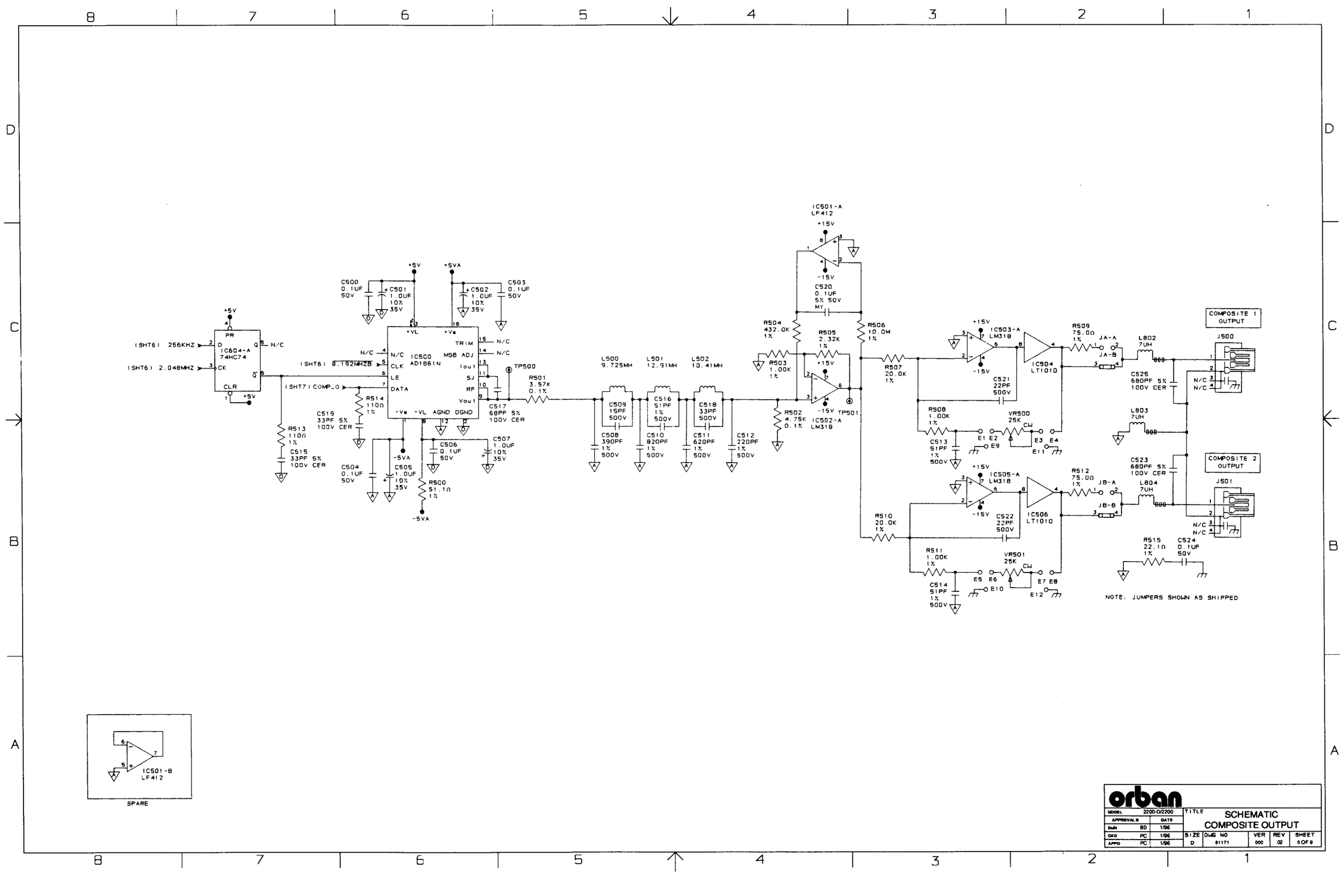


orban							
MODEL	2200-D/2200	TITLE	SCHEMATIC DISPLAY				
APPROVALS	DATE						
DWN	BD 1/96						
CKD	PC 1/96	SIZE	DWG NO	VER	REV	SHEET	
APPD	PC 1/96	D	81171	000	02	2 OF 9	


J300
LEFT INPUT
FEMALE
SHELL
L300 1000PF
L301 1.2MH
R300 604Ω 1%
IN
OUT
J301
L302 1000PF
L303 1.2MH
C323 1000PF 5% 100V CER
C324 1000PF 5% 100V CER
R301 4.99K 1%
R302 4.99K 1%
R303 845Ω 1%
J302
J303
PAD
LEFT INPUT SENSITIVITY
R304 100.0K 1%
R305 100.0K 1%
IC300 SSM2017
-15V
+15V
TP304
IC301-A LF412
R306 249Ω 1%
R307 511Ω 1%
Q300 J108
Q301 J108
R308 47.5K 1%
R309 47.5K 1%
R350 3.01K 1%
R351 10.0K 1%
R352 15.0K 1%
R353 432Ω 1%
+5V
IC303 74HC374
D0-D7
N/C
OARESET (SHT 4)
ADRESET
ABUF
CONTRAST (SHT2)
(SHT1) CNTLT
IC304 LE 74HC373
IC305 74HC374
DE50 (SHT4)
DE75 (SHT4)
DD0-DD7
(SHT1) ATO_CNTL
R314 10.0K 1%
IC306-A LM339
IC306-B LM339
IC306-C LM339
IC306-D LM339
R315 10.0K 1%
AIN_LVL (SHT1)
IC307 ADG222
R310 1.05K 1%
R311 1.82K 1%
R312 3.92K 1%
R313 6.34K 1%
R330 20.0K 1%
R331 6.65K 1%
R332 69.8K 1%
R334 39.2Ω 1%
IC302-A NE5532
IC302-B NE5532
IC301-B LF412
C300 0.1UF 5% 50V MY
R333 1.00M 1%
R335 4.99K 1%
C302 0.0047UF 5% 50V MY
C303 0.0047UF 5% 50V MY
R336 4.99K 1%
R337 39.2Ω 1%
R338 2.49K 1%
+5VA
-5VA
CR300 5082 -2800
CR301 5082 -2800
CR302 5082 -2800
CR303 5082 -2800
C308 100UF 10V
C309 0.22UF 5% 50V MY
C321 0.1UF 50V
C307 0.1UF 50V
C306 0.1UF 50V
C310 0.22UF 5% 50V MY
C322 0.1UF 50V
C311 0.1UF 50V
C312 1.0UF 10% 35V
C313 0.1UF 50V
C314 0.1UF 50V
C315 1.0UF 10% 35V
C316 0.1UF 50V
C317 0.1UF 50V
C318 0.1UF 50V
C319 0.1UF 50V
C320 1.0UF 10% 35V
R348 51.1Ω 1%
IC312 CS5389
VREF+ VREF- VA+ VA-
AINL- AINL+ AINR- AINR+
ICLKA OCLKD ICLKD APD ACAL DPD
VL+ VD+ TST01 TST02 CMODE SMODE FSYNC SDATA SCLK DCAL L/R
AGND LGND DGND
R349 0Ω
TP303
TP300
TP301
TP302
(SHT6) 8.192MHZB
IC314-A 74HC08
IC314-B 74HC08
IC314-C 74HC08
IC314-D 74HC08
IC109-D 74HC14A
ANLG_IN (SHT7)
SCK (SHT 6,7)
L/R (SHT7)
L/R (SHT 6)
IC313-A 74HC74
IC313-B 74HC74
(SHT6) 32KHZ
CLR
PR
RIGHT INPUT
J304
L304 1000PF
L305 1.2MH
R316 604Ω 1%
L306 1000PF
L307 1.2MH
C325 1000PF 5% 100V CER
C326 1000PF 5% 100V CER
R317 4.99K 1%
R318 4.99K 1%
R319 845Ω 1%
J306
J307
J305
R320 100.0K 1%
R321 100.0K 1%
RIGHT INPUT SENSITIVITY
(SHT1) AIN_LVL
IC309 ADG222
R326 1.05K 1%
R327 1.82K 1%
R328 3.92K 1%
R329 6.34K 1%
R322 249Ω 1%
R323 511Ω 1%
Q302 J108
Q303 J108
IC310-B LF412
IC310-A LF412
R324 47.5K 1%
R325 47.5K 1%
R339 20.0K 1%
R340 6.65K 1%
R341 69.8K 1%
R343 39.2Ω 1%
IC311-A NE5532
IC311-B NE5532
C301 0.1UF 5% 50V MY
C304 0.0047UF 5% 50V MY
C305 0.0047UF 5% 50V MY
R344 4.99K 1%
R342 1.00M 1%
R345 4.99K 1%
R346 39.2Ω 1%
R347 2.49K 1%
CR304 5082 -2800
CR305 5082 -2800
CR306 5082 -2800
CR307 5082 -2800
J308
PAD
(SHT2) IN_SENSIT
NOTE: JUMPERS SHOWN AS SHIPPED.
orban
MODEL 2200-D/2200
TITLE SCHEMATIC ANALOG INPUT
APPROVALS DATE
DWN BD 1/96
CKD PC 1/96
APPD PC 1/96
SIZE D
DWG NO 51171
VER 000
REV 02
SHEET 3 OF 9

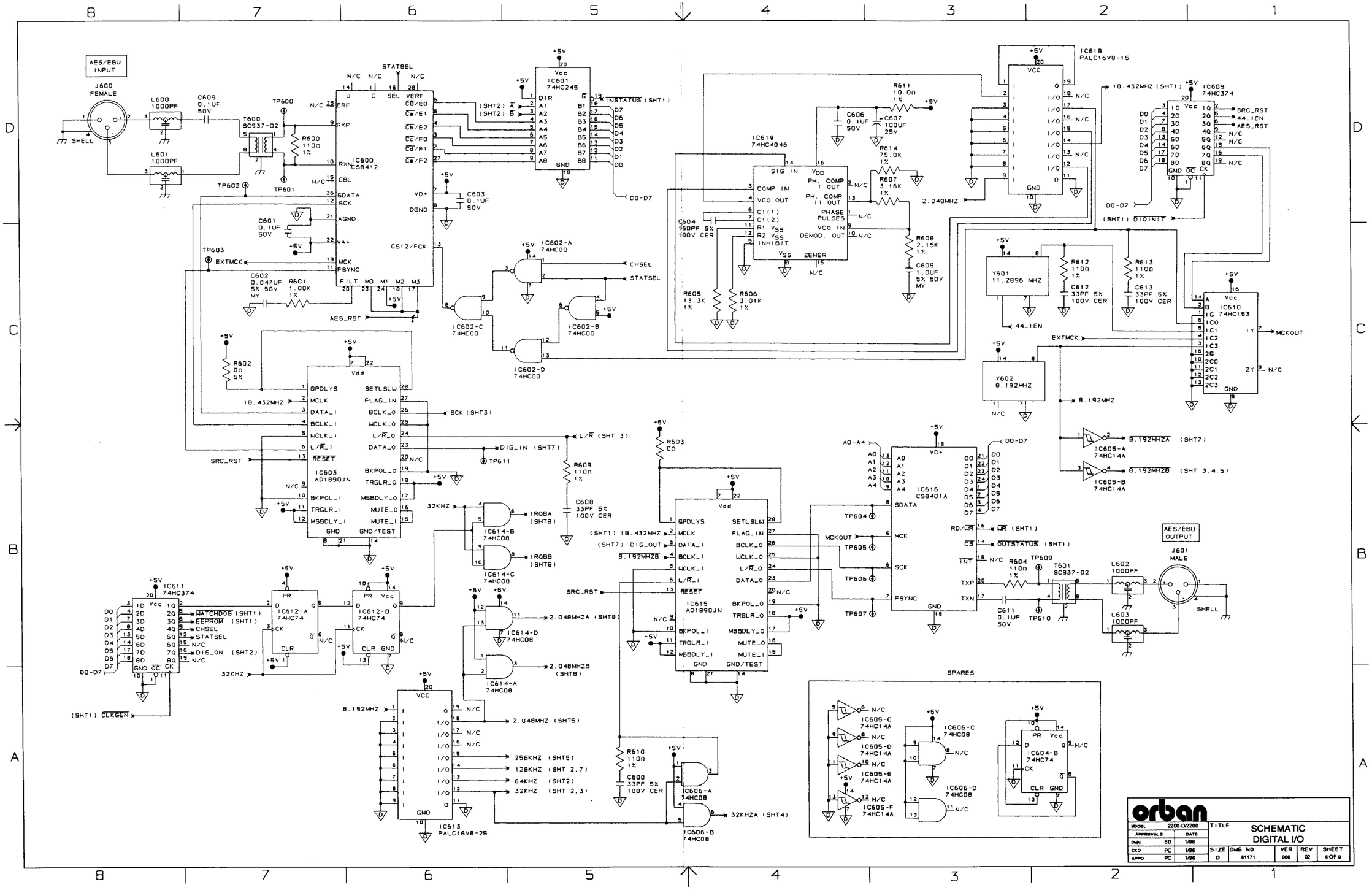


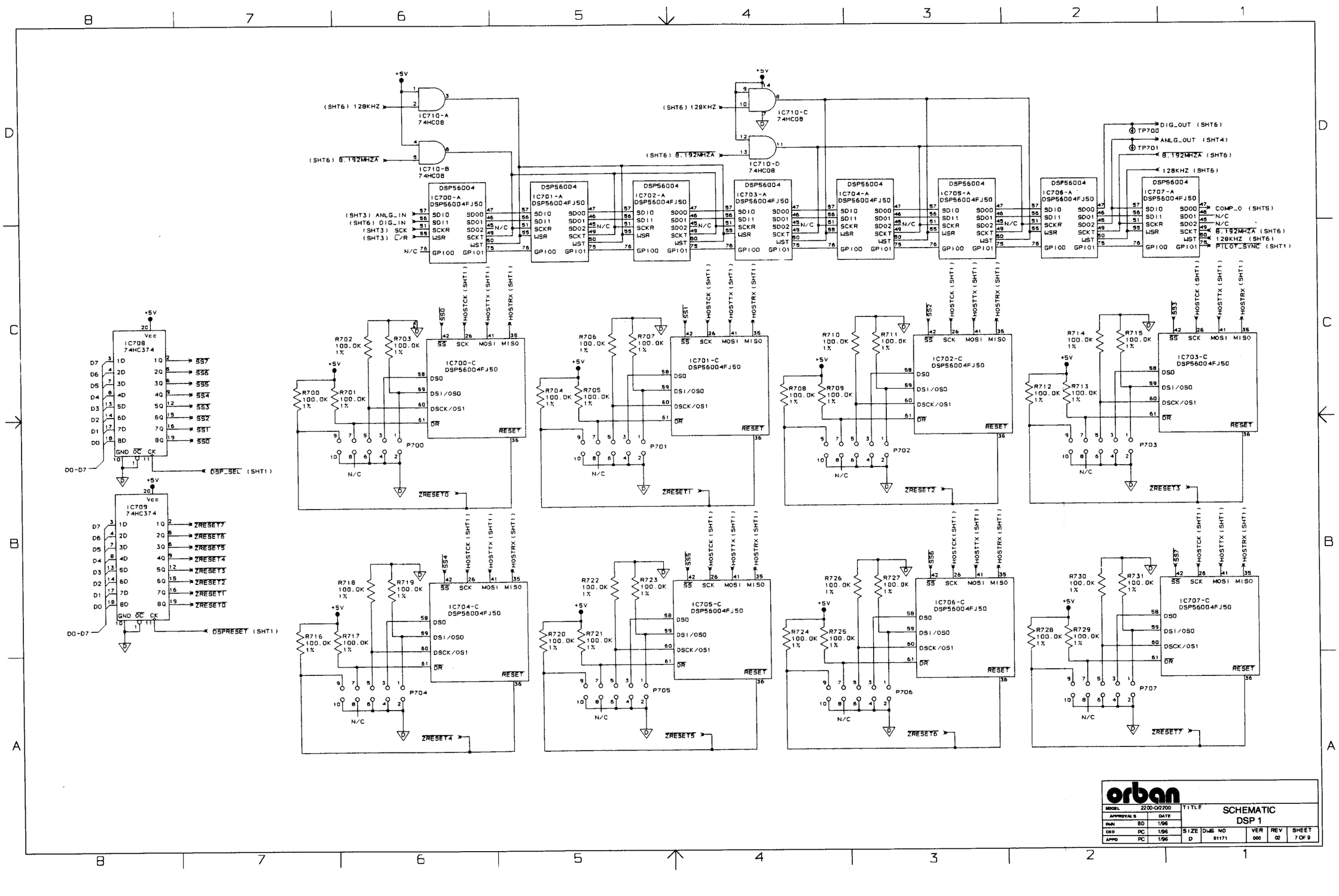
orban			
MODEL	2200-D/2200	TITLE	SCHEMATIC ANALOG OUTPUT
APPROVALS	DATE		
DWN	BD 1/96		
CKD	PC 1/96	SIZE D	DWG NO 61171 / VER 000 / REV 02 / SHEET 4 OF 8
APPD	PC 1/96		



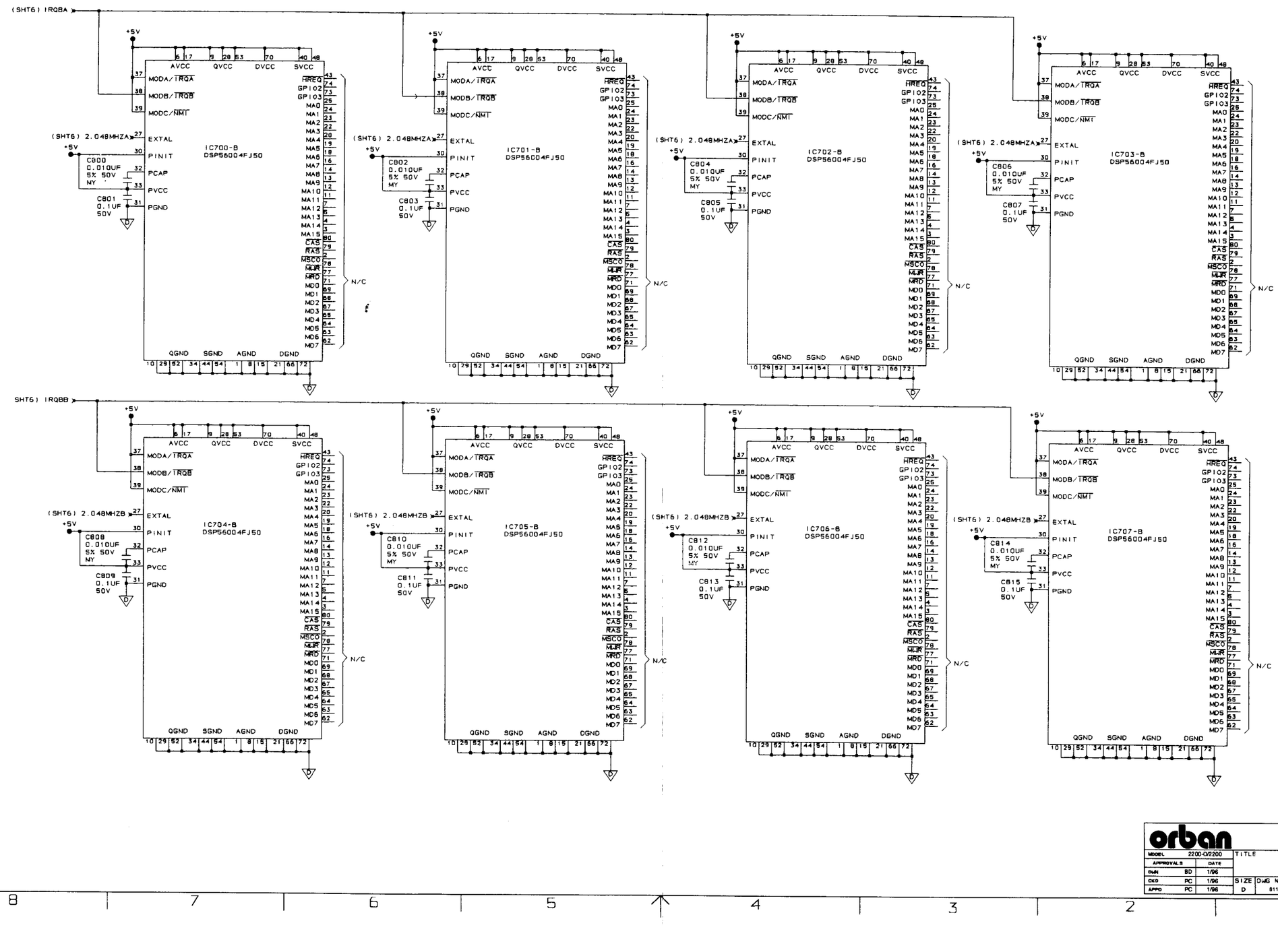
orban			
MODEL	2200-D/2200	TITLE	SCHEMATIC COMPOSITE OUTPUT
APPROVALS	DATE		
DWN BD	1/96		
CKD PC	1/96		
APPD PC	1/96		

SIZE	DWG NO	VER	REV	SHEET
D	81171	000	02	5 OF 9


AES/EBU INPUT
J600 FEMALE
SHELL
L600 1000PF
L601 1000PF
C609 0.1UF 50V
T600 SC937-02
TP600
TP601
TP602
R600 110Ω 1%
IC600 CS8412
N/C 25 ERF
9 RXP
10 RXN
N/C 15 CBL
26 SDATA
12 SCK
21 AGND
22 VA+
19 MCK
11 FSYNC
CS12/FCK
20 FILT
23 MO
24 M1
18 M2
17 M3
C601 0.1UF 50V
C602 0.047UF 5% 50V MY
R601 1.00K 1%
TP603
EXTMCK
AES_RST
STATSEL
N/C N/C N/C
14 U
1 C
16 SEL
28 VERF
6 CD/E0
5 CE/E1
4 CD/E2
3 CE/F0
2 CD/F1
27 CE/F2
IC601 74HC245
DIR
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
GND
(SHT2) A
(SHT2) B
INSTATUS (SHT1)
D7 D6 D5 D4 D3 D2 D1 D0
D0-D7
C603 0.1UF 50V
VD+
DGND
CHSEL
IC602-A 74HC00
IC602-B 74HC00
IC602-C 74HC00
IC602-D 74HC00
R602 0Ω 5%
18.432MHZ
GPDLYS
MCLK
DATA_I
BCLK_I
WCLK_I
L/R_I
RESET
Vdd
SETLSLW
FLAG_IN
BCLK_O
WCLK_O
L/R_O
DATA_O
BKPOL_O
TRGLR_O
MSBDLY_O
MUTE_O
MUTE_I
GND/TEST
IC603 AD1890JN
SCK (SHT3)
DIG_IN (SHT7)
TP611
L/R (SHT 3)
R609 110Ω 1%
C608 33PF 5% 100V CER
32KHZ
IRQBA (SHT8)
IRQBB (SHT8)
IC614-B 74HC08
IC614-C 74HC08
IC614-D 74HC08
IC614-A 74HC08
2.048MHZA (SHT8)
2.048MHZB (SHT8)
IC611 74HC374
WATCHDOG (SHT1)
EEPROM (SHT1)
CHSEL
STATSEL
N/C
DIS_ON (SHT2)
(SHT1) CLKGEN
IC612-A 74HC74
IC612-B 74HC74
PR
CLR
CLR GND
2.048MHZ (SHT5)
8.192MHZ
VCC
256KHZ (SHT5)
128KHZ (SHT 2.7)
64KHZ (SHT2)
32KHZ (SHT 2.3)
IC613 PALC16V8-25
R603 0Ω
(SHT1) 18.432MHZ
(SHT7) DIG_OUT
8.192MHZB
IC615 AD1890JN
R610 110Ω 1%
C600 33PF 5% 100V CER
IC606-A 74HC08
IC606-B 74HC08
32KHZA (SHT4)
IC619 74HC4046
SIG IN
COMP IN
VCO OUT
C1(1)
C1(2)
R1
R2
INHIBIT
VDD
PH. COMP I OUT
PH. COMP II OUT
PHASE PULSES
VCO IN
DEMOD. OUT
ZENER
C604 150PF 5% 100V CER
R605 13.3K 1%
R606 3.01K 1%
R611 10.0Ω 1%
C606 0.1UF 50V
C607 100UF 25V
R614 75.0K 1%
R607 3.16K 1%
2.048MHZ
R608 2.15K 1%
C605 1.0UF 5% 50V MY
IC618 PALC16V8-15
VCC
I/O
GND
18.432MHZ (SHT1)
IC609 74HC374
SRC_RST
44_1EN
AES_RST
(SHT1) DIGINIT
Y601 11.2896 MHZ
R612 110Ω 1%
C612 33PF 5% 100V CER
R613 110Ω 1%
C613 33PF 5% 100V CER
IC610 74HC153
MCKOUT
Y602 8.192MHZ
8.192MHZ
8.192MHZA (SHT7)
8.192MHZB (SHT 3,4,5)
IC605-A 74HC14A
IC605-B 74HC14A
IC616 CS8401A
A0-A4
SDATA
MCK
SCK
FSYNC
TP604
TP605
TP606
TP607
RD/WR
CS
OUTSTATUS (SHT1)
TXT
TXP
TXN
C611 0.1UF 50V
R604 110Ω 1%
TP609
TP610
T601 SC937-02
L602 1000PF
L603 1000PF
AES/EBU OUTPUT
J601 MALE
SPARES
IC605-C 74HC14A
IC605-D 74HC14A
IC605-E 74HC14A
IC605-F 74HC14A
IC606-C 74HC08
IC606-D 74HC08
IC604-B 74HC74
orban
MODEL 2200-D/2200
APPROVALS
DWN BD 1/96
CKD PC 1/96
APPD PC 1/96
TITLE
SCHEMATIC DIGITAL I/O
SIZE D
DWG NO 81171
VER 000
REV 02
SHEET 6 OF 9



orban			
MODEL	2200-D/2200	TITLE	SCHEMATIC DSP 1
APPROVALS	DATE		
DWN BD	1/96		
CKD PC	1/96	SIZE D	DWG NO 51171
APPD PC	1/96	VER 000	REV 02
		SHEET 7 OF 9	



orban			
MODEL	2200-D/2200	TITLE	SCHEMATIC DSP 2
APPROVALS	DATE		
DWN BD	1/96		
CKD PC	1/96		
APPD PC	1/96		
SIZE D	DWG NO 81171	VER 000	REV 02
		SHEET 8 OF 8	

TO POWER SUPPLY

J901 1 +5V
J901 2
J901 3
J901 4
J901 5
J901 6
J901 7
J901 8
J901 9
J901 10
J901 11
J901 12
J901 13
J901 14 +9VB
J901 15 LEDPULSE (SHT 2)
J901 16

TO POWER SUPPLY

J900 1 +5VA
J900 2
J900 3 -5VA
J900 4
J900 5 +15V
J900 6
J900 7 -15V
J900 8
J900 9
J900 10
J900 11
J900 12
J900 13
J900 14
J900 15
J900 16

C11 0.1UF 50V, C12 0.1UF 50V, C13 0.1UF 50V, C14 0.1UF 50V, C15 0.1UF 50V, C16 0.1UF 50V, C17 0.1UF 50V, C18 0.1UF 50V, C19 0.1UF 50V, C20 0.1UF 50V, C21 0.1UF 50V, C22 0.1UF 50V, C23 0.1UF 50V, C24 0.1UF 50V, C25 0.1UF 50V, C26 0.1UF 50V, C85 0.1UF 50V, C86 0.1UF 50V, C87 0.1UF 50V — +5V

C27 0.1UF 50V, C28 0.1UF 50V, C29 0.1UF 50V, C30 0.1UF 50V, C31 0.1UF 50V, C32 0.1UF 50V, C33 0.1UF 50V, C34 0.1UF 50V, C35 0.1UF 50V, C36 0.1UF 50V, C37 0.1UF 50V, C38 0.1UF 50V, C39 0.1UF 50V, C40 0.1UF 50V, C41 0.1UF 50V, C42 0.1UF 50V, C88 0.1UF 50V, C89 0.1UF 50V, C90 0.1UF 50V — +5V

C43 0.1UF 50V, C44 0.1UF 50V, C45 0.1UF 50V, C46 0.1UF 50V, C47 0.1UF 50V, C48 0.1UF 50V, C49 0.1UF 50V, C50 0.1UF 50V, C51 0.1UF 50V — +5V, TP1

+C82 10UF 10% 25V, C52 0.1UF 50V, C53 0.1UF 50V, C56 0.1UF 50V, C57 0.1UF 50V, C58 0.1UF 50V, C59 0.1UF 50V, C60 0.1UF 50V — +5V

TP901

+5VA: +C83 10UF 10% 25V, C61 0.1UF 50V, C62 0.1UF 50V

TP6: C92 10UF 10% 25V — -5VA

+15V: +C84 10UF 10% 25V, C66 0.1UF 50V, C67 0.1UF 50V, C68 0.1UF 50V, C69 0.1UF 50V, C70 0.1UF 50V, C71 0.1UF 50V — TP2, TP4, TP5

+C91 10UF 10% 25V, C73 0.1UF 50V, C74 0.1UF 50V, C75 0.1UF 50V, C76 0.1UF 50V, C77 0.1UF 50V, C78 0.1UF 50V — -15V, TP3

THE +5V AND DGND SIDES OF THESE HEADERS ARE ATTACHED TO INTERNAL FLOATING PLANES AND ARE NOT ELECTRICALLY CONNECTED TO +5V DIGITAL GROUND. THESE PLANES ARE CONNECTED TO CHASSIS GROUND VIA COPPER ON THE COMPONENT SIDE OF THE PCB.

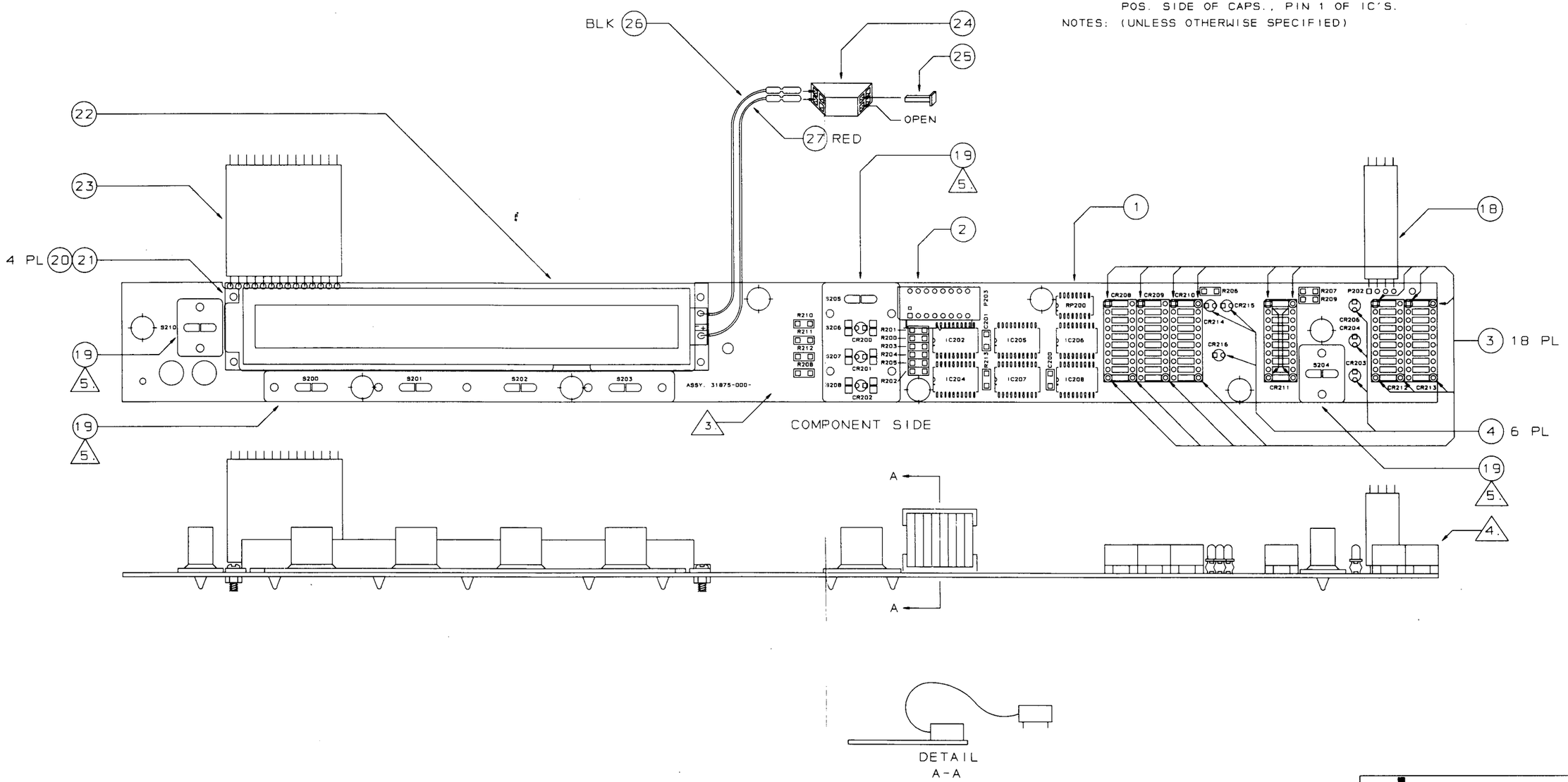
+5V J2 J3

orban

MODEL	2200-0/2200	TITLE	SCHEMATIC POWER DISTRIBUTION
APPROVALS	DATE		
DWN BD	1/96		
CKD PC	1/96	SIZE D	DWG NO 51171 / VER 000 / REV 02 / SHEET 9 OF 9
APPD PC	1/96		

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES POS. SIDE OF CAPS., PIN 1 OF IC'S.
2. REFERENCE SCHEMATIC DRAWING NO. 61182.000.01
3. ADD ASSEMBLY REVISION LEVEL IN SPACE PROVIDED.
4. TOP SURFACES OF CR208 THRU CR213 MUST BE FLUSH WITH ONE ANOTHER AND, AS A GROUP, MUST BE PARALLEL TO THE PRINTED CIRCUIT BOARD.
5. ITEM 19 IS AN ELASTOMER KEY PAD WHICH IS CUT INTO 4 PIECES.



orban							
MODEL	2200		TITLE	PCA DISPLAY 2200			
APPROVALS		DATE					
DRAWN	BD	3/96					
CKD	PC	3/96	SIZE C	DWG NO 31875	VER 000	REV 02	SHEET 1 OF 1
APPD	PC	3/96					

FROM POWER SUPPLY BOARD

P202 1
P202 2
P202 3
P202 4
+5V
+9VB

FROM MAIN BOARD

P203 1 D0
P203 2 D1
P203 3 D2
P203 4 D3
P203 5 D4
P203 6 D5
P203 7 D6
P203 8 D7
P203 9 LED
P203 10 N/C
P203 11 ENCODER
P203 12 IN_SENSIT
P203 13 DISPLAYCOL
P203 14 DISPLAYROW
P203 15
P203 16

+5V
C200 0.1UF 50V
C201 0.1UF 50V

R203 274Ω 1%
R204 274Ω 1%
R205 274Ω 1%
R206 274Ω 1%
R207 274Ω 1%
R209 274Ω 1%
R200 274Ω 1%
R201 274Ω 1%

CR200 YELLOW
CR201 YELLOW
CR202 YELLOW
CR203 GREEN
CR204 GREEN
CR206 GREEN

RECALL PRESET
MODIFY PROCESSING
SYSTEM SETUP
OUTPUT
INPUT
ENHANCE

IC202 74HC374
D0-D7
LED (SHT1)

SOFT 1 S200 — ESCAPE S205
SOFT 2 S201 — RECALL PRESET S206
SOFT 3 S202 — MODIFY PROCESSING S207
SOFT 4 S203 — SYSTEM SETUP S208
FUNCTION S204

R202 100.0K 1%
R210 100.0K 1%
R211 100.0K 1%
R212 100.0K 1%
R213 100.0K 1%

IC205 74HC374
DISPLAYCOL (SHT1)

IC206 UDN2982
RP200-A 180Ω
RP200-B 180Ω
RP200-C 180Ω
RP200-D 180Ω
RP200-E 180Ω
RP200-F 180Ω
RP200-G 180Ω
RP200-H 180Ω

IC207 74HC374
DISPLAYROW (SHT1)

IC208 ULN2803A

IC204 74HC245
DIR
(SHT3)IN_SENSIT
ENCODER (SHT1)
D0-D7

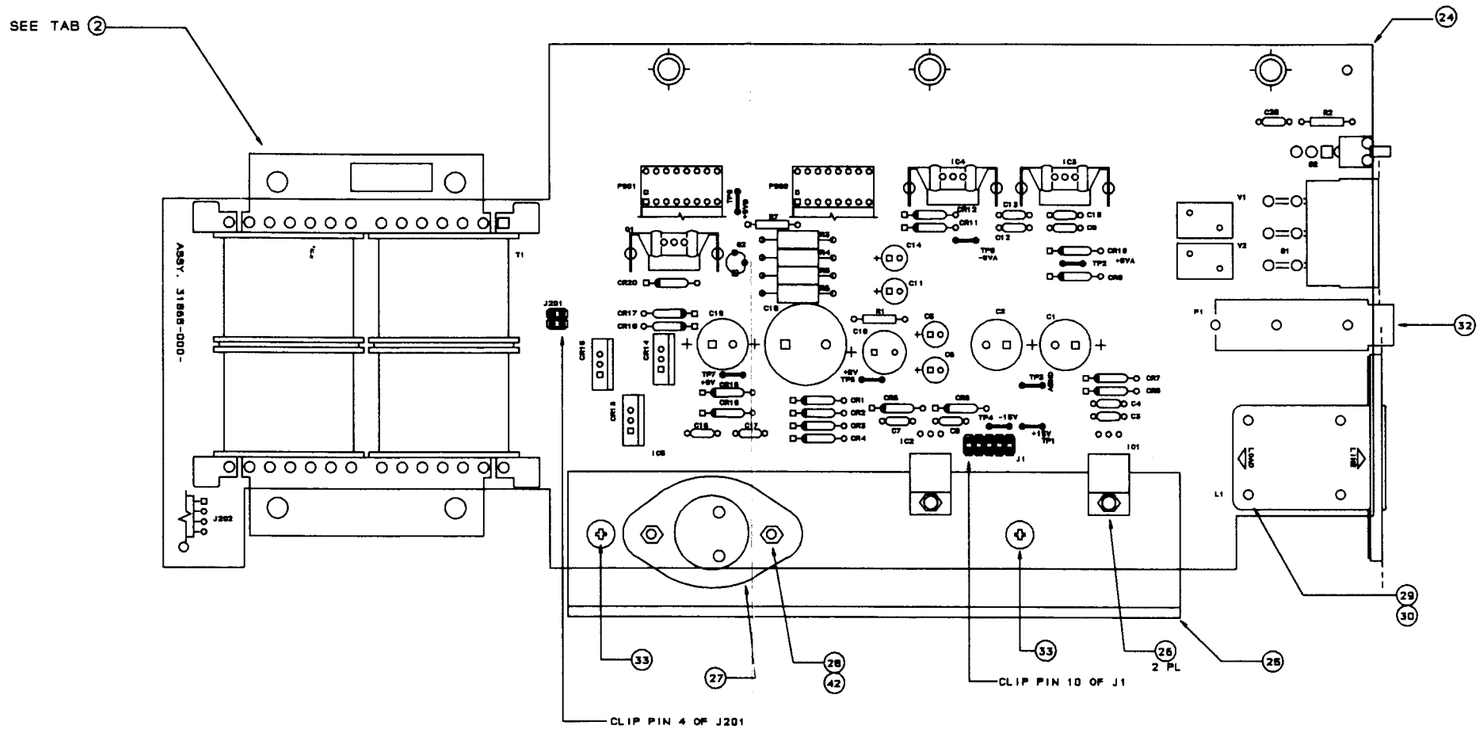
R208 100.0K 1%
CONTRAST
S210

CR208-A YELLOW	CR209-A YELLOW	CR210-A YELLOW	CR211-A RED	CR212-A RED	CR213-A RED	CR208-B YELLOW	CR209-B YELLOW
CR210-B YELLOW	CR211-B YELLOW	CR212-B YELLOW	CR213-B YELLOW	CR208-C YELLOW	CR209-C YELLOW	CR210-C YELLOW	CR211-C GREEN
CR212-C GREEN	CR213-C GREEN	CR208-D YELLOW	CR209-D YELLOW	CR210-D YELLOW	CR211-D GREEN	CR212-D GREEN	CR213-D GREEN
CR208-E YELLOW	CR209-E YELLOW	CR210-E YELLOW	CR211-E GREEN	CR212-E GREEN	CR213-E GREEN	CR208-F YELLOW	CR209-F YELLOW
CR210-F YELLOW	CR211-F GREEN	CR212-F GREEN	CR213-F GREEN	CR208-G YELLOW	CR209-G YELLOW	CR210-G YELLOW	CR211-G GREEN
CR212-G GREEN	CR213-G GREEN	CR208-H YELLOW	CR209-H YELLOW	CR210-H YELLOW	CR211-H GREEN	CR212-H GREEN	CR213-H GREEN
CR208-I YELLOW	CR209-I YELLOW	CR210-I YELLOW	CR211-I GREEN	CR212-I GREEN	CR213-I GREEN	CR208-J RED	CR209-J RED
CR210-J RED	CR211-J GREEN	CR212-J GREEN	CR213-J GREEN	CR214 YELLOW	CR215 YELLOW	CR216 RED	

HF LIMIT LEFT
HF LIMIT RIGHT
GATED

orban

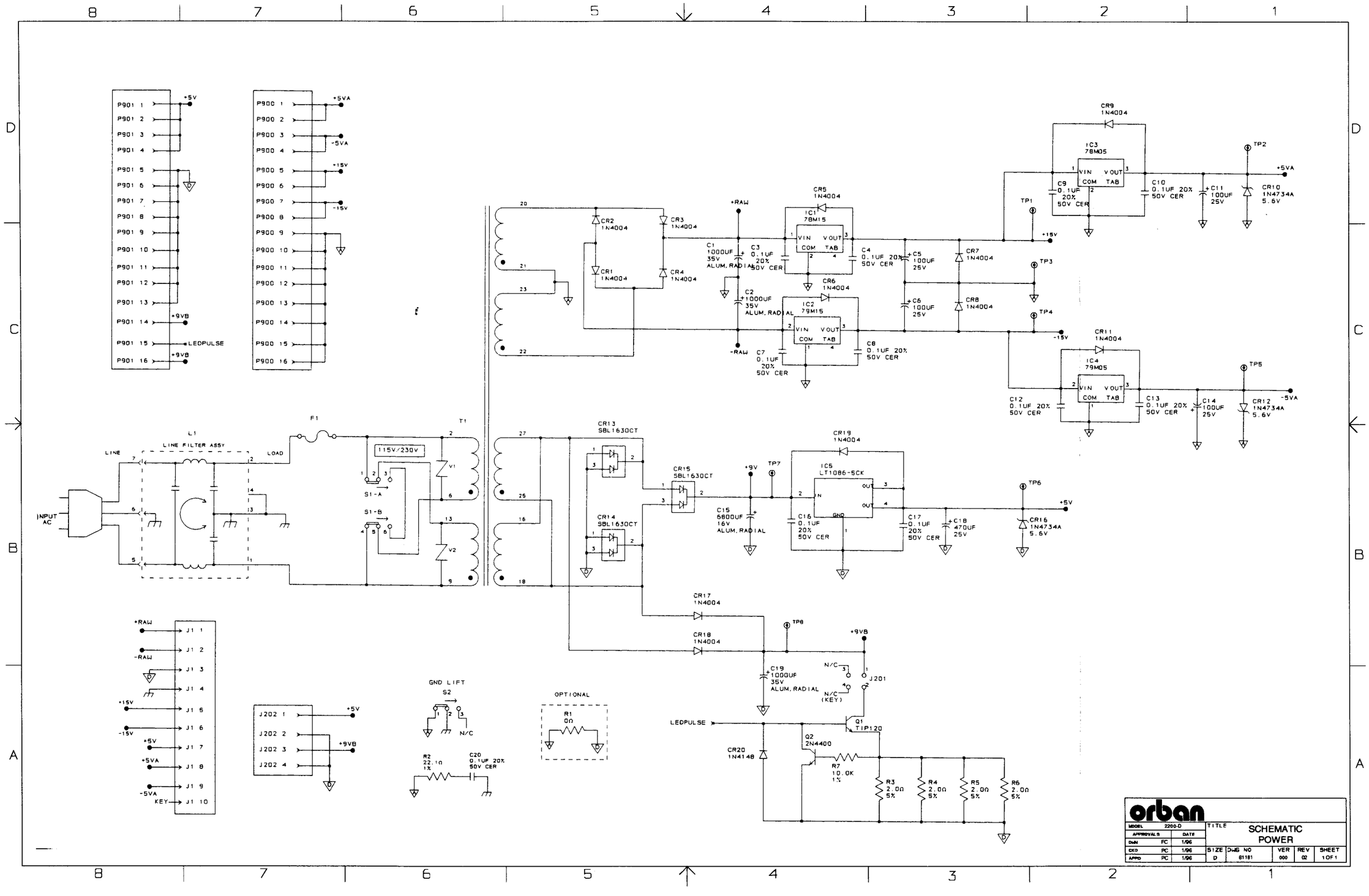
MODEL	2200-D	TITLE	SCHEMATIC DISPLAY			
APPROVALS	DATE					
DWN BD	1/96					
CKD PC	1/96	SIZE	DWG NO	VER	REV	SHEET
APPD PC	1/96	D	81182	000	01	1 OF 1



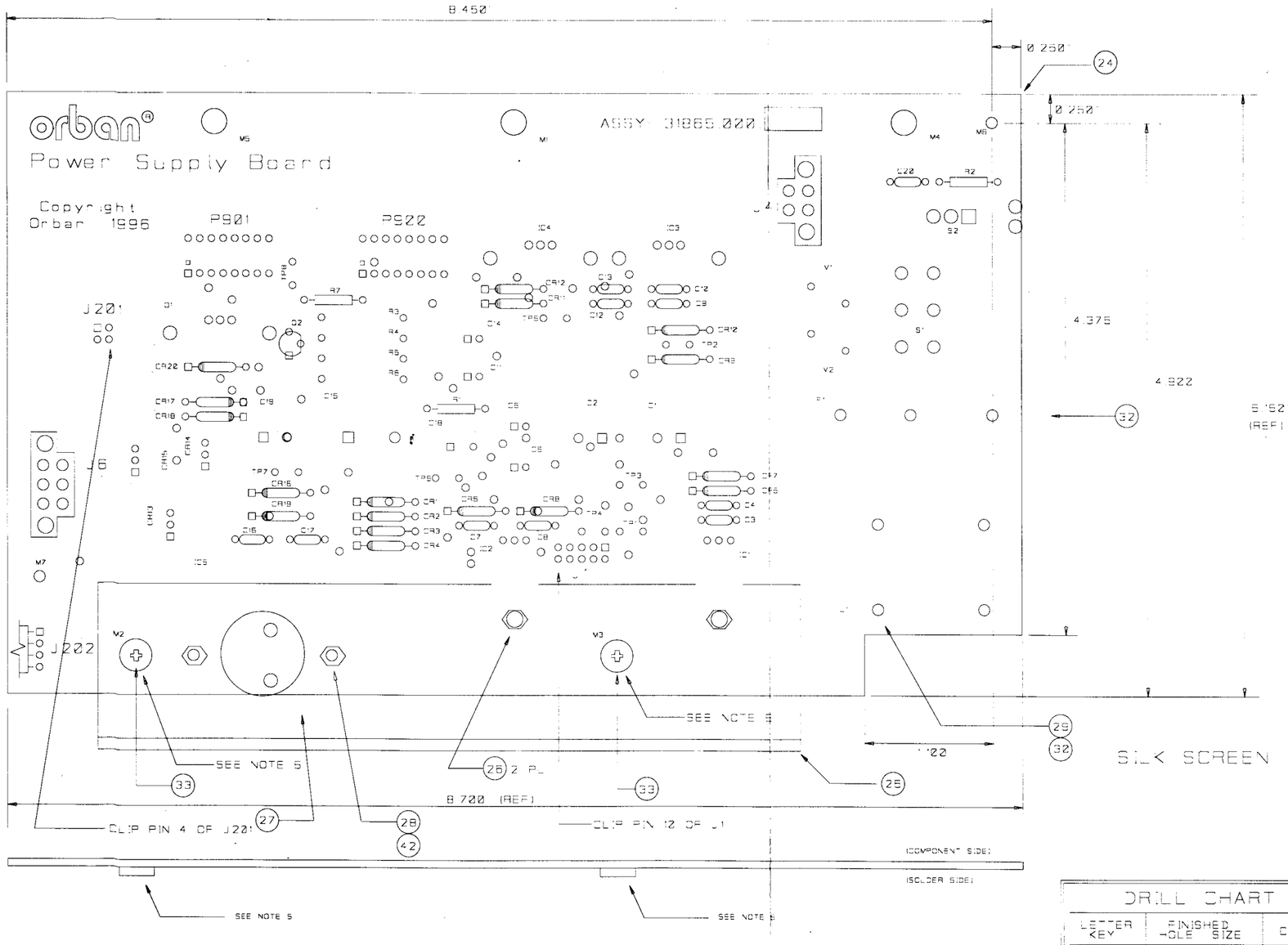
COMPONENT SIDE

TABULATION	
VER	XFMER
000	55033-000
001	55034-000

orban						
MODEL 2200-D/2200		TITLE PCA POWER SUPPLY, 2200				
APPROVALS	DATE					
DWN BD	3/98					
CKD PC	3/98	SIZE C	DWG NO 31865	VER 000	REV 02	SHEET 1 OF 1
APPD PC	3/98					



orban			
MODEL	2200-D	TITLE	SCHEMATIC POWER
APPROVALS	DATE		
DWN PC	1/96		
CKD PC	1/96	SIZE D	DWG NO 61181 / VER 000 / REV 02 / SHEET 1 OF 1
APPD PC	1/96		



7 BOARD MUST BE UL RECOGNIZED, IDENTIFIED WITH MFGR'S LOGO & TYPE DESIG. ETCHED IN ANY CLEAR AREA ON SOLDER SIDE

6 SILKSCREEN LEGEND COMPONENT SIDE, COLOR: WHITE.

5 INSTALL PEM FASTENER (KF2 - 440) 2 PLACES SOLDER SIDE AS SHOWN.

4 TRACE TOLERANCE: FINISHED BOARD TRACE WIDTHS MUST NOT VARY MORE THAN +/- 15% FROM FILM SUPPLIED.

3. USE LPI GREEN FOR SOLDERMASK, UL 94V-0, SMOBC, BOTH SIDES.

2. ALL HOLES PLATED THRU (EXCEPT NOTE **)

1. MATERIAL: 0.062 IN. THICK EPOXY GLASS FR-4, 2 OZ. EACH SIDE OUTER LAYERS.

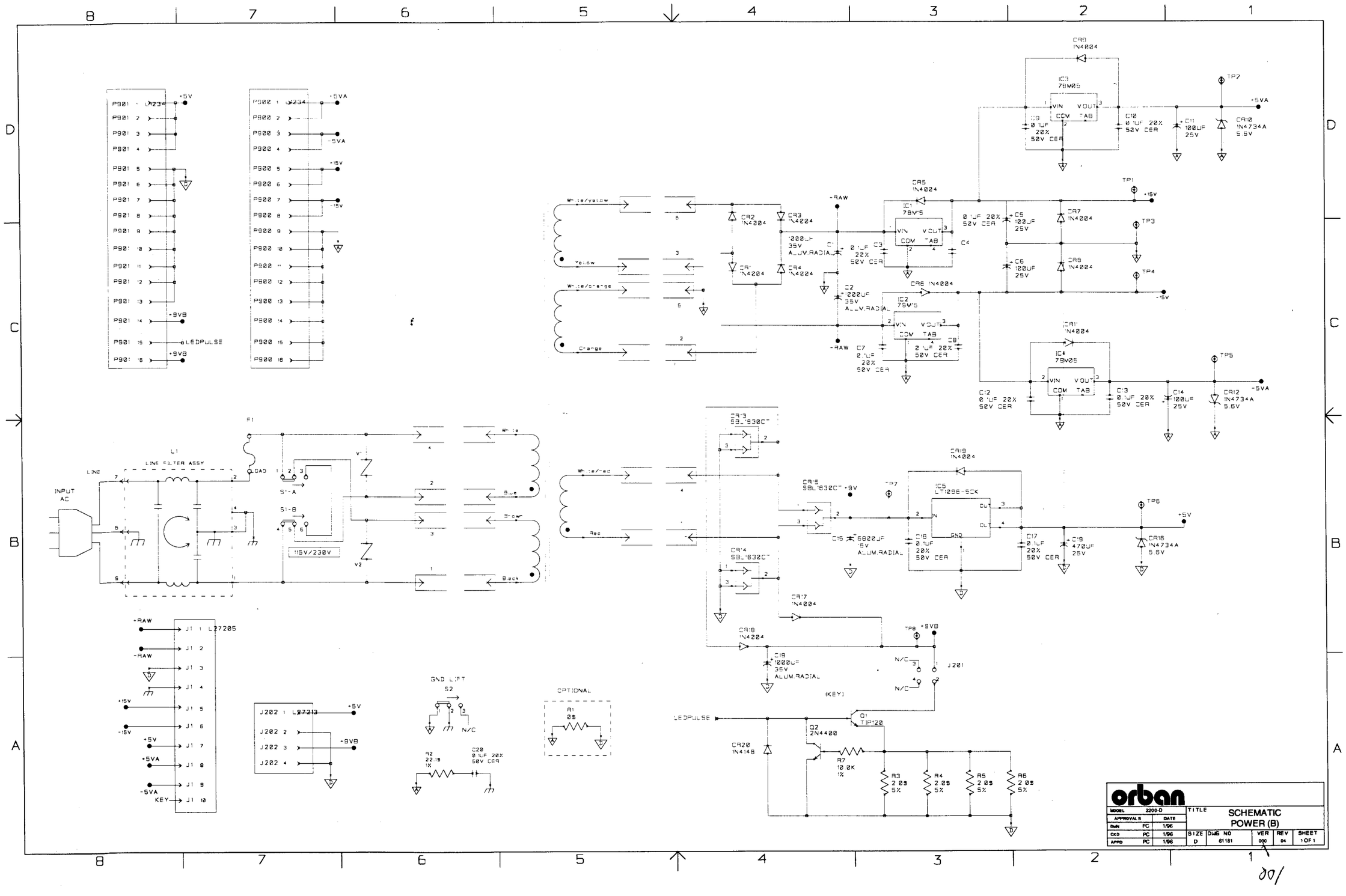
NOTES: (UNLESS OTHERWISE SPECIFIED)

DRILL CHART

LETTER KEY	FINISHED HOLE SIZE	COUNT
A	0.042"	253
B	0.055"	10
C	0.067"	17
D	0.077"	"
E	0.118"	10
F	0.125" *	2
G	0.141"	4
H	0.157"	3
J	0.166"	2

FINISHED SIZE AFTER PLATING +/- 0.003"
* 0.125" TOOLING HOLES NOT PLATED

orban			TITLE	PCA POWER SUPPLY (B), 2200				
MODEL	2200-D/2200							
APPROVALS		DATE						
DWN	BD	3/96						
CKD	PC	3/96	SIZE	DWG NO	VER	REV	SHEET	
APPD	PC	3/96	C	31865	000	04	1 OF 1	



orban		TITLE	SCHEMATIC POWER (B)
MODEL	2200-D		
APPROVALS	DATE		
DWN	FC 1/96		
CKD	PC 1/96	SIZE D	DWG NO 61181
APPD	PC 1/96	VER 000	REV 04
			SHEET 1 OF 1

001

Abbreviations

Some of the abbreviations used in this manual may not be familiar to all readers:

A/D (or A to D)	analog-to-digital converter
AES	Audio Engineering Society
AGC	automatic gain control
A-I	analog input
A-O	analog output
AT	“advanced technology” — IBM PC with 80286 or higher processor
BAL	balance
BBC	British Broadcasting Corporation
BNC	a type of RF connector
CALIB	calibrate
CIT	composite isolation transformer
CMOS	complementary metal-oxide semiconductor
COM	serial data communications port
D/A (or D to A)	digital-to-analog converter
dBm	decibel power measurement. 0dBm = 1mW applied to a specified load. In audio, the load is usually 600Ω.
dBu	decibel voltage measurement. 0dBu = 0.775V RMS. For this application, the dBm-into-600Ω scale on voltmeters can be read as if it were calibrated in dBu.
DI	digital input
DJ	disk jockey, an announcer who plays records in a club or on the air
DO	digital output
DOS	Microsoft disk operating system for IBM PC
DSP	digital signal processor
EBU	European Broadcasting Union
EBS	Emergency Broadcasting System (U.S.A.)
EMI	electromagnetic interference
ESC	escape
FCC	Federal Communications Commission (USA regulatory agency)
FDNR	frequency-dependent negative resistor — an element used in rc-active filters
FET	field effect transistor
FFT	fast Fourier transform
FIFO	first-in, first-out
G/R	gain reduction
HF	high-frequency

HP	high-pass
IC	integrated circuit
IM	intermodulation (or “intermodulation distortion”)
I/O	input/output
JFET	junction field effect transistor
LC	inductor/capacitor
LCD	liquid crystal display
LED	light-emitting diode
LF	low-frequency
LP	low-pass
LVL	level
MHF	midrange/high-frequency
MLF	midrange/low-frequency
MOD	modulation
N&D	noise and distortion
N/C	no connection
OSHOOT	overshoot
PC	IBM-compatible personal computer
PCM	pulse code modulation
PPM	peak program meter
RAM	random-access memory
RC	resistor/capacitor
REF	reference
RF	radio frequency
RFI	radio-frequency interference
RMS	root-mean-square
ROM	read-only memory
SC	subcarrier
SCA	subsidiary communications authorization — a non program-related subcarrier in the FM baseband above 23kHz (monophonic) or 57kHz (stereophonic)
S/P-DIF	Sony/Philips digital interface
TRS	tip-ring-sleeve (2-circuit phone jack)
THD	total harmonic distortion
TX	transmitter
µs	microseconds
VCA	voltage-controlled amplifier
VU	volume unit (meter)
XLR	a common style of 3-conductor audio connector
XTAL	crystal

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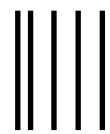

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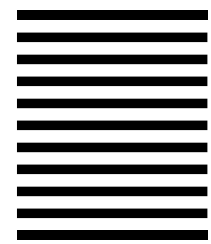

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