APPENDICES

APPENDIX A:

System Description

The purpose of this Appendix is to provide the installing engineer with an overview of system design, to answer questions and deal with uncertainties about various unconventional aspects of the design, and to provide the service technician with a moderately detailed overview of the system.

Each card is numbered. Reference will be made in each section to the number of the card on which the described circuitry is located.

The paragraphs in **Appendix B (CIRCUIT DESCRIPTION)** that correspond with topics in this Appendix have identical numbers and titles in order to expedite access to further information on a topic of interest.

REFER TO THE BLOCK DIAGRAM (page J-21)

1.a) Input Amplifier: (on Cards #3 and #4)

The audio is applied to an RFI suppression network and pad, the latter strappable for 0 or 20dB attenuation. The RFI-suppressed audio is then applied to a low-noise true instrumentation amplifier, whose "+" and "-" inputs are symmetrical and high impedance. The gain of this amplifier is adjustable from 0.88 to approximately 10.5 (a 21.5dB range). If this range does not yield the desired amount of gain reduction, then the input pad should be restrapped.

In order to avoid distortion due to imperfections in the large-value coupling capacitors that would be necessary, the input is DC-coupled. Therefore, only small amounts of differential DC should be applied to the input. Ordinarily, the input is fed by the output of a transformer or capacitively-coupled amplifier, and no difficulty should arise. Slight amounts of DC offset are eliminated in the 30Hz highpass filter following the input amplifier.

1.b) 30Hz Highpass Filter: (on Cards #3 and #4)

The output of the input buffer is applied to a third-order Chebychev highpass filter with 30Hz cutoff frequency (0.5dB down) and 0.5dB ripple. Unlike the identical filter in the old Model 8000A, this filter is not conveniently bypassable. It was felt that the advantages of this filter (i.e., elimination of modulation-wasting subsonic energy from turntable rumble and other sources, elimination of subsonic energy's introducing distortion by modulating the compressor control voltages, and prevention of destabilization and/or distortion introduction in exciters' AFC's) merited the filter's inclusion as a standard part of the system.

The cutoff frequency of the filter is sufficiently low that the only commonly-found musical instrument producing lower fundamental frequencies is the pipe organ. Most records cut off at 30Hz, and no rock-and-roll instruments have fundamentals below 40Hz.

The ringing introduced by the filter is insignificant. The ear is very insensitive to ringing in this frequency range. Further, the ringing is comparable to that introduced by a well-designed vented box loudspeaker with 30Hz cutoff.

If there seems to be an on-air problem with bass response, please don't blame this filter! First investigate such problems as obviously measurable bass rolloff in the chain up to OPTIMOD-FM 8100A/1, excess numbers of transformers in the audio chain, non-linear group delay in phone lines, and rising bass harmonic and IM distortion at program levels (which are, in general, at least 14 dB higher than tone level at "0" VU). The 30Hz highpass filter does not cause significant loss of bass "tightness", and certainly does not introduce "thinness".

1.c) Allpass Phase Scrambler And Preemphasis/Deemphasis (on Cards #3 and #4)

The FM medium has symmetrical positive and negative overload points (±100% modulation). Some music, and voice in particular, have highly asymmetrical waveforms. Therefore, maximum loudness consistent with the overload constraints of the FM medium is enhanced by processing waveforms to make their peaks more symmetrical.

In OPTIMOD-FM 8100A/1 this is achieved by a combination of the crossover network in the master/bass multiband compressor and a third-order non-minimum-phase filter. This crossover is 12dB/octave, and when its outputs are summed, it provides a single-order phase shift to complete the phase scrambler function.

The frequency response of the second stage of the phase scrambler is slightly peaked, and provides preemphasis into the multiband compressor to improve its accuracy. A deemphasis stage after the bands are summed restores flat response.

The phase scrambler is a low "Q" circuit which does not introduce ringing. Its audible effect is extremely subtle. It can be heard as a very slight change in the "sound" of some voices. Music, in general, is audibly unaffected. Despite the fact that square waves emerging from the scrambler no longer look like square waves, the purist should not fear that it is degrading audio quality. It is in fact significantly improving subjective distortion performance of the system.

2.a) Dual-Band "Master/Bass" Compressor: (audio on Cards #3 and #4; control on Card #5)

We feel that operating the third band of a conventional triband compressor independently of the rest of the bands yields very unnatural high frequency response when auditioned on high quality receivers. In addition, operating the low frequency band independently may result in unnatural frequency balances with certain music -- particularly "beautiful" or classical. For this reason, the multiband compressor in the 8100A/1 is quite dissimilar to a familiar triband unit, and offers unprecedented versatility in combination with very natural, unfatiguing sound.

The major part of the 8100A/1 compressor is the "Master" channel. This carries all program material above 200Hz. It is a feedback compressor, and its control voltage can be summed in a dB-linear manner (U.S. patent #4,249,042) with the control voltage developed by the "Bass" compressor to control the gain of the "Bass" VCA, which passes frequencies between 30 and 200Hz.

The summation is variable from none at all (in which case the "Master" and "Bass" bands operate independently, as in a conventional triband compressor) to unity gain (in which case the "Bass" channel always takes as much gain reduction as the

"Master" channel). In the latter "quasi-wideband" case, the feedback compressor control loop in the "Bass" channel is still active, and causes further gain reduction in the "Bass" VCA when program material with excessive bass energy is present. This avoids the pumping which would occur in a fully-wideband system if excess bass were to force gain reduction of the entire program.

2.b) Crossover and Bass Clipper: (on Card #3 and #4)

OPTIMOD-FM Model 8100A/1 employs a 12dB/octave crossover. The 12dB/octave configuration is simply two identical 6dB/octave filters in series, with the polarity of the "Bass" band inverted. It can be shown that the sum of the two outputs has a perfectly flat magnitude response, but exhibits an overall phase shift. This phase shift is purposely used as part of the "phase scrambler" to make peaks more symmetrical.

In OPTIMOD-FM Model 8100A/1, this crossover is realized as a "distributed crossover" (U.S. patent #4,249,042). This means that the first 6dB/octave section is before the VCA, and the second 6dB/octave section is after the VCA and the control voltage rectifier. The control voltage circuitry is therefore fed from a 6dB/octave crossover only.

The advantage of this configuration is that it permits insertion of a soft clipper immediately after the "Bass" VCA to eliminate overshoots which would otherwise intermodulate with the output from the "Master" VCA when the sum of "Bass" and "Master" is preemphasized and clipped. The second part of the "Bass" crossover is after the "Bass" clipper, thus lowpass-filtering the clipper output and rolling off harmonics and out-of-band IM introduced by the clipping process. In-band IM is negligible because of the relatively narrow bandwidth processed by the "Bass" channel.

The sum of the "Bass" and "Master" channels is applied to a deemphasis network to "undo" the preemphasis introduced in the phase scrambler circuitry (see **1.c**).

2.c) Voltage-Controlled Amplifier (VCA) Operation:

The voltage-controlled gain block used throughout OPTIMOD-FM Model 8100A/1 is a proprietary Class-A VCA which operates as a two-quadrant analog divider with gain inversely proportional to a current injected into the gain-control port. A specially-graded Orban IC contains two matched non-linear gain-control blocks with differential inputs and current outputs. The first of these is employed in the feedback loop of an opamp to perform the gain control function. The inputs of the first and second gain-control blocks are connected in parallel, and the output of the second block is a distortion-corrected current which is transformed into the desired gain-controlled voltage by means of an opamp current-to-voltage converter. For most gains, levels, and frequencies, THD is well under 0.1%. Overload-to-noise ratio (noise measured in a 20-20,000Hz band) is typically 90dB, and is constant with respect to gain and level.

2.d) Compressor Control Circuitry: (on Card #5)

Each compressor (left and right "Master" and left and right "Bass") feeds its own rectifier with threshold. The drive to the clippers following the compressors and preemphasis/hf limiters is determined by the setting of the CLIPPING control, which simultaneously adjusts all rectifier thresholds (and thus the average compressor output level). Left and right rectifier pairs (which have current-mode high-impedance outputs) are "OR"ed into individual timing circuitry for "Master" and "Bass" channels.

This timing circuitry is proprietary, and is located within sealed modules. The "Master" timing circuitry is most critical to achieving natural sound. It performs the following functions:

1) A peak limiting function with very fast recovery time for transient material;

2) A slower compression function whose recovery time is a function of gain reduction; and,

3) A recovery-delay function which provides extra smoothing of the gain control voltage to avoid low frequency distortion even with fast release times.

The recovery time of the compression function is adjustable in the "Master" band only by means of the RELEASE TIME control. In addition, a gating circuit radically slows the recovery time of the compression function if the input program level drops below a threshold adjustable by the GATE THRESHOLD control, thus preventing "noise swish-up" during pauses or low-level material.

The gain eventually recovers to maximum over a period of about two minutes. This prevents the unit from "going to sleep" permanently on, say, a quiet musical passage (below gating threshold) which follows a loud musical sforzando which has forced considerable gain reduction. (This effect, incidentally, is why we chose not to incorporate an expander into the AGC system -- such circuits tend to make musical mistakes like the one just described.)

The "Bass" timing circuitry is similar to the "Master" timing circuitry, and performs all of the same functions. Its time constants are optimized for most natural, dynamic sound.

Both timing circuits process the signal in logarithmic form, and have low-impedance outputs. The timing circuits drive exponential converters which provide control-current outputs for the "Master" and "Bass" VCA's. The BASS COUPLING control provides the ability to sum a controlled amount of the "Master" timing circuit output into the "Bass" exponential converter, where it sums with the output of the "Bass" timing circuit in a dB-linear manner.

Extensive gain reduction metering is provided. Since the outputs of the timing circuits are dB-linear, the gain reduction meters are provided with dB-linear scales.

The output of the "Master" timing module is applied to a peak detector which "holds" the fast-limiting component of the control voltage until the gain reduction meter ballistics have a chance to "catch up". The output of this peak detector drives the "Master" gain reduction meter, which shows the true peak value of the gain reduction.

The output of the "Master" timing module also drives a slewrate-limited amplifier which removes the fast limiting spikes from the voltage, and which drives the "compressor" meter to show the amount of slow compression occurring.

By subtracting the output of the slewrate-limited amplifier from the peak detector, the fast peaks only are derived. This difference signal feeds the "limiting" meter.

The output of the "Bass" timing circuitry contains a much smaller fast peak limiting component than does the output of the "Master" timing circuitry. No peak detection is necessary to assure accurate metering, and the output of the "Bass" timing circuitry thus drives its gain reduction meter directly.

3) Phase-Corrected Lowpass Filter/Preemphasis: (on Card #6)

After the outputs of the "Master" and "Bass" channels have been summed, they are passed to a filter which performs three functions:

1) It lowpass-filters the signal at 15kHz and 24dB/octave to prevent frequencies beyond the bandwidth of the system from unnecessarily activating the high frequency limiter or causing unnecessary IM distortion in the clipper;

2) It provides a standard FM preemphasis (75us or 50us, depending on Region -- see **Appendix G** if you wish to change the 8100A/1's preemphasis); and,

3) It provides phase correction to make the delay of the lowpass filter plus preemphasis approximately constant, thus minimizing the unavoidable increases in peak level resulting from the preemphasis and filtering functions.

The lowpass filter is designed to partially equalize the frequency response variations in the main 15kHz lowpass filter following in the FM Smart Clipper, thus providing flatter overall frequency response. The preemphasis is created by summing a second-order bandpass filter with the flat signal. The rising side of the filter slope provides the preemphasis; the falling side provides part of the lowpass filter function. The phase corrector is a fourth-order allpass filter, and is physically placed before the lowpass filter and preemphasis.

4) High Frequency Limiter: (on Card #6)

In order to perform the hf limiter function, a variable-gain stage is placed between the output of the bandpass filter creating the preemphasis (see 3 immediately above) and the amplifier which sums the bandpass filter output with the main signal. Thus high frequency limiting is effected by dynamically reducing the preemphasis as required.

The variable gain stage is realized by a junction FET operating as a voltage-controlled resistor, instead of by a VCA as in other processing functions within the 8100A/1. This simplification is possible because the high frequency limiters in the left and right channels are entirely independent, and need not track accurately together.

Each channel has its own rectifier and timing module. The timing in the hf limiter is considerably simpler than in the compressor sections because only fast dynamic filtering occurs; there is no "compression" function.

It should be noted that the 8100A/1 hf limiter is activated by high frequency energy only, as opposed to the old 8000A, whose hf limiter was sensitive to the peak level of the entire preemphasized signal. The 8100A/1's hf limiter therefore cannot be activated by, for example, low frequency overshoot components from the previous multiband compressor. This design improvement is possible because the 8100A/1's FM Smart Clipper permits considerably greater amounts of clipping than the clipping scheme in the 8000A without introducing audible distortion, thus rendering the hf limiter function far less critical and permitting substantial increases in perceived high frequency power output. The 8100A/1 hf limiter need not "know" about the actual peak level of the preemphasized signal -- only approximately how much hf energy is present.

A HIGH FREQUENCY LIMITING control available to the user adjusts the threshold of hf limiting over a range of approximately 3dB. The lowest threshold results in very little clipping on sinusoidal tone; the +3dB threshold results in moderate clipping of tone above approximately 2kHz. In most cases, users prefer operating this control in full "hard", which moves the threshold to the "+3dB" point and results in minimum hf limiting and maximum hf control by clipping, while still limiting hf energy which would otherwise cause disturbing distortion if it were clipped.

Operation of the hf limiter is metered by a simple comparator circuit which lights the appropriate front-panel HF LIMIT lamp if any hf limiting at all occurs. It is primarily useful to verify that the hf limiter circuit is operating properly.

5) FM Smart Clipper: (on Cards #8 and #9)

The 8100A/1 FM Smart Clipper (U.S. Patent #4,208,548) is a clipper circuit in which the threshold of clipping is varied dynamically as a function of the high frequency energy in the program, and in which a distortion-cancelling sidechain permits all clipping distortion below 2.2kHz to be reduced by at least 30dB. This results in cleanest sound on both high and low frequencies, and controls the classic distortion problems in preemphasized clippers, the most significant one being sibilance splatter.

It should be noted that it is normal for sinewaves to modulate less than 100% when applied to the 8100A/1 in its normal OPERATE mode. There are two principal reasons for this:

1) Some headroom is left between the threshold of the FM Smart Clipper and the threshold of the subsequent overshoot corrector in order to accommodate the distortion corrector signal. With sinewaves, no distortion corrector signal is produced. Thus, the headroom is not used, and full 100% modulation does not occur.

2) Sinewaves have a very low peak-to-average ratio and high loudness potential compared to program material of identical peak levels. The audio processing, in order to maintain natural sound quality, pushes sinewaves down in level as it would any other similar program material with low peak-to-average ratio. In general, any audio processor which produces 100% modulation on sinewaves tends to sound somewhat unnatural because this psychoacoustic factor has not been accounted for.

5.a) Clipper With Dynamic Threshold: (on Cards #8 and #9)

The clipper is a straightforward shunt clipper which is ordinarily biased with ±1.5 volts, thus providing a somewhat "soft" characteristic (but not nearly as soft as a pair of back-to-back unbiased diodes). The characteristic was chosen to obtain the best compromise between harmonic and IM distortion induced by clipping, when the IM-cancelling circuitry is considered.

The output of the bandpass filter in the high frequency limiter (see 4 above) feeds a rectifier with threshold. When high frequency energy exceeds this threshold, the clipper bias voltage is reduced to reduce the clipping threshold by approximately 1.0dB. The purpose of this threshold reduction is to provide headroom between the clipper threshold and the subsequent overshoot corrector threshold. This headroom accommodates the distortion corrector signal (see **5.c** below) which is needed to correct the IM distortion produced when large amounts of hf energy are clipped. If this headroom were not provided, the overshoot corrector would clip off the distortion corrector signal, thus negating its effect. On the other hand, when the input signal to the clipper contains predominantly low frequency energy, the distortion corrector loop is essentially ineffective. In this case, the absolute amount of clipping is minimized by raising the clipping threshold to approximately the threshold of the overshoot corrector.

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5.b) 15kHz Phase-Corrected Lowpass Filter: (on Cards #8 and #9)

The main clipped signal is applied to a 15kHz phase-corrected fifth-order Cauer lowpass filter to remove energy above 15kHz, particularly that induced by clipping. (Bear in mind that the unclipped signal was already filtered in the preemphasis lowpass filter.) The signal is also passed through a shelving deemphasis to help match the frequency response of this main signal path to the frequency response of the distortion-cancelling sidechain.

The delay of the 15kHz filter is equalized by means of a fourth-order allpass network to achieve minimum filter overshoot, and also to add sufficient delay to the main path so that the delay of the distortion-correcting sidechain can be matched.

5.c) Distortion-Cancelling Sidechain: (on Cards #8 and #9)

The clipper's output is subtracted from its input to derive the distortion introduced by the clipper. This distortion signal is applied to a 2.2kHz lowpass filter which matches both the frequency response and time delay of the main-path filter extremely closely throughout the 2.2kHz passband.

The output of this distortion-cancelling sidechain filter is summed into the output of the main-path filter. Distortion below 2.2kHz is cancelled by adding the filtered distortion signal to the main path. (Because the clipper's output was subtracted from its input, the actual distortion component -- which appears at the clipper's output -- is out-of-phase and thus cancels properly). The output of the 2.2kHz filter can be considered a smoothing signal. This signal increases the peak level of the summed signal somewhat. If the level increases beyond the 100% point, it is clipped by the subsequent overshoot corrector. In most cases, the level buildup is not very large because the distortion signal contains mostly high frequencies, and these are filtered out by the 2.2kHz lowpass filter, thus greatly reducing the level of the distortion signal before it is summed with the main signal.

The sum of the main-path and distortion signals is passed through a shelving preemphasis which is precisely complementary to the shelving deemphasis introduced in the main path, thus restoring overall flat response.

6) Frequency-Contoured Sidechain (FCS) Overshoot Compensator:
(on Cards #8 and #9)

The FCS overshoot compensator (U.S. Patent #4,460,871) is best thought of as a "bandlimited safety clipper". That is, it performs the function of clipping off overshoots from the earlier FM Smart Clipper, but does not produce out-of-band frequency components as a simple clipper would. If such components were produced, they would produce "aliasing distortion" when applied to the stereo generator and then decoded in a receiver. Simultaneously, the FCS overshoot compensator does not significantly increase low frequency IM products when compared to a simple clipper performing the same function -- a problem particularly characteristic of competing overshoot compensation circuits.

Briefly, the FCS overshoot compensator functions by deriving the overshoots from its input with a "center clipper" circuit, lowpass-filtering the overshoots with a fifth-order passive LC filter to remove out-of-band frequency components, and then mixing the filtered overshoots out-of-phase with a delayed version of the input signal. This delay, created by an encapsulated active allpass network, is identical to the delay in the overshoot filter, thus assuring that the input signal and filtered overshoots arrive in the same place at the same time.

If no filter were used, this process would be identical to clipping the input signal, and would create a "differential clipper". However, the overshoot filtering process reduces the peak level of the high frequency components of the overshoot by removing harmonics. To compensate for this loss of peak level (which would cause less than full cancellation of overshoot), the frequency response of the overshoot filter rises at 15kHz -- thus increasing the level of the high-frequency fundamental to compensate for the loss of harmonics. This is why the system is called "Frequency-Contoured Sidechain".

The final sum of input and out-of-phase filtered overshoot is passed through a third-order lowpass filter to provide further attenuation of unwanted high frequency energy. Phase correction is applied to the combination of this filter and the overshoot filter. (The phase response of the overshoot filter is identical to its matched main-path delay network -- thus the phase correction also corrects the response of the main-path delay network.) This phase correction makes the overall time delay through the entire FCS overshoot compensator approximately constant, and assures that the various filters within the compensator do not upset carefully controlled peak levels in unpredictable ways.

If any very unusual waveforms cause residual overshoots, these are dealt with in a safety clipper at the output of the FCS overshoot compensator system. However, the basic FCS overshoot compensator is so effective that this safety clipper is hardly ever active.

7.a) Stereo Generator -- General Principles: (on Card #7)

The 8100A/1 stereo generator uses the "matrix" approach to the generation of the composite baseband signal. That is, L+R (sum) and L-R (difference) are derived from the input signals, which have been bandlimited to 15kHz by the earlier circuitry. The L+R signal appears directly at the baseband output and occupies the frequency range from 30 to 15,000Hz; the L-R is first multiplied by a 38kHz sinewave to form a double-sideband suppressed-carrier subchannel occupying 23 to 53kHz, and is then summed into the baseband output. The final signal summed into the output is the 19kHz pilot subcarrier, which is phase-locked to the 38kHz subcarrier.

The two principal advantages to this approach (as opposed to the more common "switching" approach) are:

1) The L+R (which is usually the dominant component) is not subject to any switching or modulation process which may introduce distortion.

2) The baseband is derived by a multiplication process which ideally introduces no out-of-band frequency components. In the 8100A/1, spurious components are typically below 0.02% modulation. The baseband thus requires no lowpass filtering. Such a filter is often the most costly part of a conventional switching stereo generator, and necessary compromises in its design tend to degrade separation.

Stereo/mono mode switching is provided by FET switches driven by CMOS logic. In addition, there are two special "test" modes available. Each accepts a right-channel signal. The first creates an L+R signal to test main-channel-to-subchannel crosstalk; the second creates an L-R signal to test subchannel-to-main-channel crosstalk.

The pilot subcarrier and 38kHz subcarrier are generated by precise circuitry which incorporates several feedback loops to assure stability of the stereo generator parameters with time and temperature.

The block diagram (p. J-21) depicts the major subsystems in the stereo generator and should help clarify the discussion below.

7.b) 19kHz Oscillator: (on Card #7)

The 19kHz oscillator employs a 19kHz crystal operated in series-mode to provide positive feedback around an opamp. The oscillator produces a sinewave with well under 0.1% distortion using no other tuned circuits than the crystal itself. To avoid oscillator saturation and distortion, the loop gain of the oscillator is adjusted by a FET whose resistance is controlled by an AGC feedback loop which senses the output level of the oscillator and corrects it as necessary to sustain linear oscillation.

The oscillator can be squelched in mono mode by shorting out the positive feedback through the crystal with an FET switch.

7.c) 19kHz Doubler: (on Card #7)

The output of the 19kHz oscillator is turned into a 38kHz square wave by means of a biased dual comparator. The comparator is biased so that it changes state every time the 19kHz sine wave goes through 45, 135, 225, and 315 degrees. The amplitude of the 38kHz square wave is adjusted by varying the voltage on the "strobe" inputs of the comparator; the 38kHz AGC servo adjusts this level, and thus the level of the filtered 38kHz sinewave.

7.d) 38kHz Filter and Phase Shifter: (on Card #7)

The 38kHz square wave output from the comparator is filtered into a sinewave with less than 0.02% distortion by means of an active filter cascaded with a passive filter. The active filter is a high-"Q" resonator whose center frequency is controlled by a FET activated by the phase-locked-loop circuitry (see **7.f**). By tuning this resonator slightly around the resonance point, its phase shift is significantly affected. This provides the phase control to lock the 19kHz and 38kHz together with correct phase as required for proper operation of the stereo decoder.

A passive third-order Cauer filter attenuates residual distortion in the output of the 38kHz active resonator to achieve the final distortion specification. It is very important that the 38kHz applied to the multiplier be as clean as possible, as every remaining harmonic component will be multiplied by the L-R audio to create out-of-band suppressed-carrier subchannels around each of the harmonics.

7.e) 38kHz AGC Loop: (on Card #7)

Maintaining high separation depends upon precisely controlling the ratio between L+R and L-R gain. Since the L-R is multiplied by the 38kHz sine, the gain of the L-R is directly proportional to the amplitude of the 38kHz sine. This amplitude must be highly stable, or separation will drift with time and temperature.

The 38kHz sine is derived by hi-"Q" filters which can drift. In addition, the PLL circuitry will cause gain variations in the 38kHz active bandpass filter. It is clear, therefore, that a closed-loop servo system must be used to stabilize the 38kHz sine level.

To do this, the filtered 38kHz sine is applied to a high-gain comparator. The other comparator input is connected to a reference voltage derived from the SEPARATION control. The servo forces the peak level of the 38kHz sine to be identical to this reference voltage. The output of the comparator is filtered, buffered, and then connected to the "strobe" inputs of the 38kHz doubler dual comparator, which has the effect of controlling the output level of the comparator, thus closing the AGC loop.

7.f) 38kHz Phase-Locked Loop (PLL): (on Card #7)

The relative phase between the 19kHz pilot and the 38kHz subcarrier must be precisely controlled to achieve optimum separation. This is achieved by detecting the phase between the 19kHz output of the pilot oscillator and the filtered 38kHz sine, and by activating a tuning FET in the 38kHz active resonator which tunes this

resonator slightly to either side of resonance, thus adjusting the filter's phase shift to achieve the exact phase desired at the output of the passive filter.

The phase detector is a biased dual comparator which is essentially insensitive to the level of its 38kHz input, but which is quite sensitive to the (highly controlled) level of its 19kHz input. The output of the phase detector eventually feeds a true integrator. This makes the PLL a "type-1" servo system, and results in zero steady-state phase error regardless of loop gain.

7.g) Stereo Modulator: (on Card #7)

The stereo modulator derives the L-R in a differential amplifier whose common-mode rejection can be precisely trimmed to null main-channel-to-subchannel crosstalk. The L-R output of the differential amplifier is applied to the input of a VCA which is almost identical to the VCA's used in the audio processing. (See **2.c** for further information.)

The gain control port of the VCA is fed by the sum of the 38kHz sine and a DC current which biases the gain control port to prevent the control current from ever becoming negative. (The VCA can only accommodate single-polarity control currents.) This DC bias means that the output of the VCA contains two components: the desired product of the input L-R and the 38kHz, and an undesired product of the DC and the input L-R, which is simply L-R. This latter component (which is subchannel-to-main-channel crosstalk) is cancelled by feeding some of the L-R around the VCA out-of-phase. Final sub-to-main null is achieved by slightly adjusting the gain of the VCA.

The VCA produces a small second harmonic (76kHz) feedthrough component (typically 70dB below 100% modulation without correction). This is cancelled by applying a small amount of 38kHz to the input of the VCA, where the 38kHz is multiplied by itself to produce a second-harmonic component which is out-of-phase with the 76kHz VCA feedthrough. When the 76 KHZ NULL trimmer is properly adjusted, stable cancellation of more than 80dB is possible.

The pilot, and a DC component to cancel DC offsets at the output of the generator (thus rendering an output coupling capacitor unnecessary) are also summed into the output of the VCA. This mix, which is desired only in <u>stereo</u> mode, is switched into the summing junction of the output opamp through a JFET switch.

L+R is derived by passively mixing the L and R inputs, and then by introducing the sum into the summing junction of the output opamp of the stereo generator. FET switches are provided to turn each channel individually ON or OFF, and also to change gain in <u>mono</u> mode. In <u>mono</u>, an individual channel (either L or R) feeds the output opamp by itself. Its gain into the output must therefore be increased 6.84dB so it can produce 100% peak modulation.

7.h) (not used)

7.i) (not used)

7.j) (not used)

7.k) Mode Switching Logic: (on Card #7)

The 8100A/1 stereo generator has three switch-selected modes of operation. Two are special test modes, and are used only when making stereo performance verification measurements. The first of these facilitates measurement of main-to-sub crosstalk by switching the signal applied to the right stereo generator input into both left and right stereo generator inputs. Since this test signal is also applied to the L-R differential amplifier, this mode can also be used to null the stereo generator's internal MAIN-TO-SUB CROSSTALK NULL.

The second mode facilitates the measurement of sub-to-main crosstalk by injecting the signal on the right channel input line into the L-R differential amplifier. The stereo generator is arranged such that this test mode can also be used when adjusting the stereo generator's internal SUB-TO-MAIN CROSSTALK NULL trimmer.

The normal mode is operate. In this mode, three sub-modes are available by remote control or by switching the front-panel STEREO/MONO switch.

The first is stereo, and simply generates a normal stereo baseband output from the signals on the left and right stereo generator input lines.

The second and third sub-modes are mono left and mono right. These take the inputs on the left and right stereo generator input lines respectively, and apply them directly to the stereo generator output amplifier with sufficient gain to scale peaks to 100% modulation.

A CMOS three-state latch using three NAND gates "remembers" the logic state. The three hard-switched modes are also integrated into the logic system, principally by means of two CMOS exclusive-OR gates. Note also that in order to permit stereo crosstalk measurements, the sub-mode logic is forced into stereo when either of the crosstalk test modes is entered.

The schematic diagram for the stereo generator (Card #7) contains a truth table that shows the state of each JFET switch in each of five operating conditions: main-to-sub test, sub-to-main test, stereo operate, mono left operate, and mono right operate. Further understanding of the operation of the logic and switching system in the 8100A/1 stereo generator may be obtained by studying this table.

8) Power Supplies:

Primary power for the 8100A/1 circuitry comes from a highly regulated ±15 volt power supply. The main supply is +15 volts. This is created by means of a 723C IC regulator with current-boosted output, current limiting, and overvoltage protection using a zener diode and fast-blo fuse.

The -15 volt supply is essentially a current-boosted opamp in a unity-gain inverting configuration which "amplifies" and inverts the +15 V supply, thus "tracking" it. The -15 volt supply is also current-limited and overvoltage protected. Both +15 and -15 supplies are located on a non-plug-in card mounted on the inside of the rear chassis apron. This apron is also used as a heat sink for the regulator power transistors.

The 711C comparators used in the stereo generator require +12/-6 volt supplies. These are created by locally dropping the main +15 volt supply through three

forward-biased silicon diode junctions (to create the +12), and by means of local resistive voltage dividers from -15 to ground (to create the -6). In addition, a number of local ±14 volt supplies exist. These are created by means of single diode drops from the ±15 volt main power supply, with local capacitive decoupling. Their purpose is to decouple noise from the main power supply.

Bias supplies are also required for the diode clippers in the audio processing. There are two such supplies; the first creates approximately ±1.2 volts (for Cards #3 and #4), while the second creates ±4.2 volts (for Cards #8 and #9). Both supplies use a pair of opamps. The first is a unity-gain voltage-follower whose input is a temperature-compensated voltage created by a resistor/diode network; the second is a unity-gain inverter which creates the complementary negative voltage.

APPENDIX B:

Circuit Description

The following section provides an extremely detailed description of the circuitry used in OPTIMOD-FM on the component level.

It may be wise to read **Appendix A** first, and to consult the block diagram on p. J-21. Referring to the appropriate Schematics and Parts Locator Drawings in **Appendix J** will help you to follow the text and will aid component-level troubleshooting.

In those cases where the circuitry is duplicated in the left and right channels, only the left channel circuit and component designators will be discussed.

1.a) Input Amplifier: (on Cards #3 and #4)

The input is applied to the RF filter chamber, and there encounters an RF filter and 10K bridging pad R303, R304, R305. Strapping R305 into the pad introduces 20dB loss, which is the normal condition of the pad.

The output of the pad is connected to a low-noise true instrumentation amplifier consisting of IC301A, IC301B, IC302A, and associated resistors. R306, R307 provide bias current for IC301, which is a low-noise bipolar-input dual IC opamp. R308, R311 are feedback resistors for the two sections of IC301. The differential gain is controlled by the series resistance of R310 and GAIN control R309. The common-mode gain of the IC301 pair is 1.

The differential output of IC301A and IC301B is converted to a single-ended output and the common mode component of the output is nulled by means of differential amplifier IC302A and associated resistors. R316 adjusts the balance of the resistor network to assure maximum common-mode 60Hz rejection.

NOTE

Nearby lightning strikes may induce sufficient energy into the 8100A/1's audio input wiring to pass through the RFI protective networks and destroy IC301 or IC401. If the 8100A/1 is installed in a lightning-prone location, it is advisable to keep spare NE5532's in stock. Installation of varistors between each side of the audio input lead and earth may help prevent such problems. IC301 is socketed, and is thus easily replaced.

1.b) 30Hz Highpass Filter: (on Cards #3 and #4)

The non-bypassable 30Hz highpass filter IC302B, C303, C304, C305, R317, R318, R319 is a third-order Chebychev filter with 0.5dB passband ripple (nominal) and a ripple bandwidth (i.e., -0.5dB frequency) of 30Hz. It is realized as a unity gain Voltage-Controlled Voltage-Source (VCVS) active filter. This filter is non-inverting, has a gain of exactly 0dB in the passband, and uses positive feedback to "sharpen up" the response around the cutoff frequency. Most modern books on active filters extensively discuss this type of filter. (See for example -- Wong and Ott: Function Circuits. New York, McGraw-Hill, 1976, pp. 230-231.)

1.c) Allpass Phase Scrambler and Preemphasis/Deemphasis: (on Cards #3 and #4)

This filter contains a single-order allpass filter IC303A, R320, R321, R322, C306 followed by a second-order non-minimum-phase peaking equalizer IC303B, R323, R324, R325, R326, R327, C307, C308. The phase response of the first section varies from 0 to 180 degrees as a function of frequency, while the phase response of the second section varies from 0 to 360 degrees as a function of frequency. The amplitude response of the first section is flat; the amplitude response of the second section is broadly peaked at approximately 200Hz.

To restore flat response, a complementary dipping-equalizer section is inserted after the two bands of the dual-band compressor have been recombined. This circuit consists of IC307A, R359, R360, R361, R362, R363, C319, C320. Its gain far from 200Hz is -1.76dB, and it exhibits a second-order dip centered at 200Hz.

2.a) Dual-Band "Master/Bass" Compressor (General): (on Cards #3, #4, and #5)

The dual-band compressor consists of an audio path and control circuitry. We will first discuss the audio path generally. Details of the VCA operation and control circuitry operation are found immediately below in sections **2.c, 2.d,** and **2.e.**

2.b) Crossover And Bass Clipper (on Cards #3 and #4)

The crossover consists of 12dB/octave sections. The first 6dB/octave filter is located before the VCA, the second after. Since the input to the control rectifiers is taken from the VCA outputs, the control-voltage crossover is 6dB/octave.

The first 200Hz highpass section for the "Master" compressor is filter C309, R328. The second 200Hz highpass section is C318, R357. The first 200Hz lowpass section for the "Bass" channel is R342, R343, C314. The second lowpass section for the "Bass" channel is R367, R366, R365, C321.

A clipper, consisting of biased diodes CR303, CR304, and resistors R367, R366, is located before the second lowpass section. Thus the second lowpass section rolls off harmonics created by clipping.

In order to force the "Master" and "Bass" channels to add correctly, the polarity of the "Bass" VCA is inverted by using the appropriate inputs of IC309B (compare with IC305B).

2.c) Voltage-Controlled Amplifier VCA Operation:

NOTE

This section contains a general description of the voltage-controlled amplifier circuitry used through the 8100A/1, including the multiplier in the stereo generator. The "Master" VCA will be specifically described.

The basic operation of the VCA depends on a precisely-matched pair of gain-control blocks with differential voltage inputs and current-source outputs. The gain of each block is controlled by means of a control current.

If used alone, one such gain-control block would introduce considerable distortion. Therefore, the first of the two matched blocks IC305A is used as the feedback element in a high-quality operational amplifier, IC304. The second of the matched blocks IC305B is then driven by the predistorted output of IC304. To provide more detail: The output of IC304 is first attenuated by R334, R335, C311, and then applied to the input of the feedback element IC305A. The output of IC304 is predistorted as necessary to force the current output of IC305A to precisely and linearly cancel the audio input into the "virtual ground" summing junction of IC304. This same predistorted voltage is also connected to the input of IC305B. Thus the output of IC305B is an undistorted current, which is converted to a voltage in current-to-voltage converter IC306A, R341, R376, C312. The output of IC306A is the output of the VCA.

Because IC305A is in the feedback loop of IC304, the gain of the VCA is inversely proportional to the gain of IC305A. Thus if the control current is applied to the control port of IC305A (through R333), then the VCA behaves like a two-quadrant analog divider. However, if the control current is applied to the control port of IC305B, then the gain of the VCA is directly proportional to the gain of IC305B, and the VCA behaves like a two-quadrant multiplier. The VCA is used in the "divider" mode in the "Master" and "Bass" VCA's, and in the "multiplier" mode in the stereo generator.

In the case of the "Master" VCA, a fixed current is applied to the control port of IC305B through R339, R340, CR301 to fix the gain of IC305B. CR301 provides temperature compensation.

Second-harmonic distortion is introduced by differential offsets in either IC305A or IC305B. This distortion is cancelled by applying a nulling voltage directly to the input of IC305B by means of resistor network R336, R337, R338.

If the VCA is not perfectly balanced, "thumps" due to control current feedthrough can appear at the output. These are equivalent to multiplying the control current by DC. If a correct DC offset is applied to the VCA input, then this equivalent DC multiplication can be nulled to zero and the "thumps" eliminated. Such an adjustable DC offset is provided by R331, R332.

R329, R330, C310 are frequency-compensation components to prevent the VCA from oscillating supersonically.

2.d) Compressor Control Circuitry: (on Card #5)

The output of the "Master" VCA is applied to a voltage in/current out fullwave rectifier-with-threshold, IC503A, IC504, R505, R506, R507, C502, CR502. This is essentially an opamp with discrete class-B output stage. A bias voltage of -12V on the "+" input of IC503A holds the voltage at this opamp's "-" input at -12V by feedback and provides appropriate bias conditions for the rectifier to prevent saturation. R507 determines the rectifier's transconductance. C502 provides DC blocking between the nominal ground potential of the input side of R507 and the -12 volts at IC503A's "-" input.

A negative-going voltage at the input side of R507 pulls current away from the "AC virtual ground" at IC503A's "-" input. An equal current must therefore flow into "-" input by turning on the NPN transistor whose base is connected to the output of IC503A. Because of the class-B biasing, this assures that the PNP whose base is connnected in parallel to the NPN is off.

A collector current essentially equal to the NPN's emitter current flows into the NPN from the output terminal of the rectifier. Part of this current comes from the rectifier load; part comes from the fixed collector current of the top PNP transistor. This PNP creates the threshold of limiting by saturating and diverting all class-B output stage collector current away from the load until the output stage current exceeds the nominal PNP collector current. When the output stage current exceeds the PNP collector current, the PNP comes out of saturation, and the difference between the PNP collector current and the rectifier output current is delivered to the rectifier's load. The PNP transistor's collector current is fixed by its emitter resistor R505, and by its base voltage (determined by the setting of the CLIPPING control, R542). The CLIPPING control thus varies the collector current of the PNP, and therefore the threshold of limiting. In PROOF mode, CR502 and R506 parallel R505, increasing the collector current, and raising the limiting threshold by approximately 14dB.

If the voltage at the input side of R507 goes positive, then the bottom PNP transistor turns on, and its neighboring NPN turns off. The collector current of the PNP is inverted by the dual NPN current mirror, and the current mirror output is summed into the output port of the rectifier, where it is also subject to the action of the PNP threshold transistor as described immediately above.

The output of the left "Master" rectifier is "OR"ed with the output of the right "Master" rectifier by means of two diodes: CR501 & CR504. Because the output of the each rectifier is in the form of a current, voltage drops across the "ORing" diodes do not affect the accuracy of the rectifier.

The output of the "OR" circuit is applied to a proprietary circuit which computes the VCA control voltage. Release time control for the slow "compressor" function is provided by R508, R509. A JFET switch Q501 is provided to radically slow the compression release, thus essentially freezing the gain when ordered to do so by the gating circuitry (described immediately below). 22-megohm resistors across the gating FET'S create a slow "leak" in the gating function which permits to gain to fully recover over a period of approximately two minutes.

The output of the control voltage module varies between 0 volts (maximum gain) and approximately -10 volts (minimum gain=maximum gain reduction). Thus release is inhibited by applying a voltage of greater than +10 volts to the anode of CR503 which forces Q501 off. Release is enabled by applying a voltage of less than -10 volts to the anode of CR503. This reverse-biases CR503, and Q501 is forced on by R510's forcing Q501's gate to be at the same potential as its source.

The output of the release time module is a low impedance voltage source. It is applied to exponential converter circuit IC501, IC502, R501, R502, C501 through pad R503, R504. The collector current of either matched transistor in IC502 is an almost perfect exponential function of its base-emitter voltage. The scaling factor of the converter is stabilized by forcing a constant current through the left-hand transistor by means of IC501. This current is determined by the current injected into IC501's "-" input through R502. The base of the left-hand transistor is grounded; the

emitters of the matched transistors are connected. Thus, assuming a perfect match between transistors, the collector currents of the two transistors will be equal if the base of the right transistor is grounded. Varying the base voltage on the right-hand transistor varies its collector current exponentially about the nominal current in the left-hand transistor. This nominal current determines the quiescent (no-gain-reduction) gain in the VCA's. The current output at the collector of the right-hand transistor is connected to a matched pair of resistors, one of which feeds the gain control port of the left VCA, and the other of which feeds the gain control port of the right VCA. This is a "current divider" and is analogous to the familiar resistive voltage divider.

The operation of the "Bass" control loop is essentially identical to the operation of the "Master" control loop. The only essential difference is that provision is made to mix "Master" control voltage into the input of the "Bass" exponential converter through BASS COUPLING control R521, and R518. When R521 is fully clockwise, the "Bass" exponential converter is being fed as much "Master" control signal as the "Master" exponential converter. In the absence of output from the "Bass" release time module, "Bass" and "Master" VCA's will thus track exactly.

Because the "Bass" rectifier is always connected to the output of the "Bass" VCA, exceptionally strong bass will exceed the threshold of bass limiting and cause an output from the "Bass" release time module, thus momentarily decreasing the gain of the "Bass" VCA below that of the "Master" VCA. This is the low-frequency equivalent of familiar high frequency limiting.

(**NOTE:** The "multiband feedback compressor with crosscoupling into dB-linear VCA's" concept is protected by U.S. patent # 4,249,042.)

2.e) Gain Reduction Metering:

Gain reduction metering in the "Master" band is provided by three meters.

The first, TOTAL G/R, is driven by a peak detector IC512, R530, C508, CR511. C508 captures negative-going peaks and discharges slowly through R530. To avoid being loaded by the meter, C508 is buffered by voltage-follower IC512B. The discharge time of C508 is sufficiently slow to permit the mechanical movement of the TOTAL G/R meter to rise to the actual peak level of the gain control voltage, thus accurately displaying it.

COMPRESSION is indicated by passing the output of the release time module through a grossly overcompensated 301A opamp IC511 connected as a voltage follower. The 2.2uF compensation capacitor C507 so limits the slew rate of IC511 that only the slow component of gain reduction is permitted to drive the COMPRESSION meter.

The LIMITING meter is connected differentially between the outputs of IC511 and IC512B. It thus indicates the fast component of gain reduction as the difference between the slow component and the peak-held TOTAL component.

"Bass" band gain reduction metering reads the sum of the "Master" and "Bass" control voltages through R519, R520, in the same proportions that are applied to the input of the "Bass" exponential converter. In the interests of simplicity, the "Bass" TOTAL G/R metering signal is not electronically conditioned.

2.f) Gating Circuitry: (on Card #5)

The gating detector consists of a peak detector followed by a comparator. IC opamps are employed for both functions.

The left and right input signals are summed in R538, R539, and lowpass-filtered at 3kHz by means of C510. The lowpass-filtered sum is amplified by means of non-inverting amplifier IC513B, whose gain is variable from 0 to approximately 40dB by means of R537, the GATE THRESHOLD control. Low frequency response of IC513B is rolled off with C511 to prevent low-frequency noise from inhibiting the gate.

The positive peak output of IC513B is detected by CR514 and C503. R536 determines the recovery time of this peak detector.

The output of the peak detector is applied to comparator IC513A. R533, R534 create a reference voltage of +1.9 volts. If the output of the peak detector exceeds this value, then the output of IC513A is driven towards the negative power supply, and the gate is inhibited. Otherwise, the output of IC513A rests close to the positive power supply, and the gate is enabled. In this condition, the GATE LED is lit by current supplied through R531, CR512.

Hysteresis to assure clean switching is provided by positive feedback through R532.

In PROOF mode, CR513 applies +15 volts to the "-" input of IC513A to inhibit the gate, thus permitting all VCA's to recover to full gain.

3) Phase-Corrected Lowpass Filter/Preemphasis: (on Card #6)

Phase correction for the preemphasis and fourth-order lowpass filter associated with it is provided by a fourth-order allpass filter IC601, R601, R602, R603, R604, R605, R606, R607, R608, R609, C601, C602, C603, C604. The overall magnitude response of the filter between the card input and the filter output at IC601B is flat, gain is 0dB, and the phase response varies from 0 to 720 degrees. The operation of the filter is difficult to explain in words, and is best left to a mathematical analysis.

The fourth-order lowpass filter is in fact quasi-fourth-order. The first section of the filter is generated by a conventional second-order multiple-negative feedback active lowpass filter IC602A, R610, R611, R612, C605, C606. (See, for example, Wong and Ott: Function Circuits, op. cit.). However, the second section has been combined with the preemphasis, and transformed from a purely lowpass form to a peaking bandpass equalizer.

To understand this, imagine first a preemphasis cascaded with a 12dB/octave lowpass filter. As frequency is increased, the response will first rise at 6dB/octave, following the preemphasis. However, when the cutoff frequency of the lowpass filter is encountered, the response will reverse itself and fall at 6dB/octave indefinitely.

This is similar to the response of a peaking equalizer. However, when the response of the peaking equalizer falls, it does not fall indefinitely, but only until it reaches unity gain again. Nevertheless, we can choose a peaking equalizer whose rising side matches the rising side of our original preemphasis-plus-lowpass-filter to very close tolerances.

The falling side, after deemphasis, represents the stopband of the filter. Thus, when considered as a totality, the response of the entire fourth-order filter will, instead of falling indefinitely at 24dB/octave, fall for approximately 20dB after cutoff at 24dB/octave, and at 12dB/octave thereafter.

4.a) Differential Preemphasis and HF Limiter: (on Card #6)

The advantage of transforming the lowpass filter as described in the previous section is that it permits us to create the preemphasis differentially, by summing the output of bandpass filter IC602B, R614, R615, R617, C607, C608 with the filter's input. The summation occurs in IC605A. The output of IC602B is passed through a variable-gain stage, realized with FET IC603A, and low-noise non-inverting amplifier IC604. By varying the gain with which the output of IC602B is summed with its input, a high frequency limiter is realized.

Ordinarily, IC603A is pinched off, thus producing maximum gain and full preemphasis. However, as the gate voltage on IC603A is reduced toward ground, the resistance of IC603A decreases, thus decreasing the gain of voltage divider R619, R620, IC603A and reducing the preemphasis.

The polarity reversal in IC602B requires that a compensating polarity reversal occur in the summing process. IC605A is thus non-inverting for the bandpass signal, and inverting for the main signal. In addition, R616 feeds some of the output of IC602B around the variable-gain stage out-of-phase. This permits complete cancellation of the preemphasis despite the inability of the FET variable-gain stage to achieve total cutoff.

4.b) HF Limiter Control Circuitry: (on Card #6)

The high frequency limiter control circuitry is very similar to the compressor control circuitry described in **2.d** above. The output of the bandpass filter only is applied to the rectifier-with-threshold, which is identical to the ones used in the compressor control circuitry. Similarly, the output of the rectifier is connected to a proprietary release-time module, and the threshold-of-limiting adjustment and PROOF mode G/R defeat are also substantially identical to previously described circuits.

The output of the module, unlike the outputs of the release time modules in the compressor control circuitry, is high impedance. It drives the high impedance gate of FET IC603A through R625.

Gain reduction is indicated by a simple ON/OFF LED indicator, driven by IC606A. FET BIAS adjustment R626 determines the quiescent gate voltage of IC603A, assuring pinchoff under conditions of no limiting. This voltage is applied through release time resistor R627 to the "-" input of IC606A. This input will be pulled in the negative direction when gain reduction occurs.

The output of R626 is also applied to the "+" input of IC606A through R628. R629 pulls this "+" input slightly more negative than the output of R626 to hold the output of IC606A negative during conditions of no gain reduction. However, as soon as the "-" input of IC606A is pulled slightly less positive by the occurence of gain reduction, the output of IC606A goes positive and lights the HF LIMIT lamp through R630 and Q601, used as a zener diode.

5.a) Clipper With Dynamic Threshold: (on Cards #8 and #9)

The threshold of the first clipper CR801, CR802 is varied dynamically to make best use of the distortion-cancelling circuitry. When the clipper input signal contains substantial high frequency energy, then the threshold of clipping is lowered approximately 1.0dB to permit the difference-frequency IM distortion-cancelling signal to sum with the output of the main 15kHz lowpass filter without excessive clipping in the subsequent overshoot corrector. However, when the clipper input signal contains predominantly low frequencies, then the clipper threshold is raised to minimize the amount of low frequency clipping which occurs.

This is achieved by using the rectified output of IC602B (the high frequency bandpass filter employed differentially in the preemphasis filter) to control the clipper threshold. The output of IC602B feeds a rectifier-with-threshold IC806B, IC807 (and associated circuitry) whose operation is identical to the rectifier-with-threshold already described in **2.d.** This rectifier feeds a RC filter R844, R847, R848, CR807, C826. R844 determines the attack time of the circuit in conjunction with C826. The recovery time is determined by the series combination of R847 and R848.

If the high frequency energy present at the input to the rectifier is insufficient to overcome its threshold, then the "+" input of IC808A is held at ground by R847, R848. If output current flows into the rectifier, then C826 is pulled negative through CR807. If the voltage across C826 attempts to go more negative than approximately -13 volts, the rectifier will saturate and limit the voltage swing to this value. The voltage divider R847, R848 attenuates this 13 volt variation such that it causes a voltage variation of -0.2v at the output of IC808A, thus changing the threshold of clipping by approximately 1.0dB.

A 1.5 volt quiescent bias for the clipper diodes is provided by passing the output of a voltage divider through CR808 to R846. IC808A then acts as a unity-gain inverting amplifier for the voltage at CR808's anode. CR808 temperature-compensates the threshold of clipping by reducing the clipper bias voltage as the voltage drop across the diodes increases (with temperature variation). The final diode bias voltage at the output of IC808A is thus the sum of the quiescent voltage contributed by the circuitry connected to the "-" input of IC808A, and the voltage variation contributed by the circuitry connected to the "+" input of IC808A.

IC808B is connected as a unity-gain inverting amplifier, and provides a complementary negative bias for CR802.

It is important to understand that this scheme results in sinewaves not hitting 100% modulation in OPERATE mode. This occurs for two reasons. First, the dynamic response of the previous multiband compressor section is such that steady-state 1kHz sinewaves reach about 60% modulation if the CLIPPING control is adjusted to 12:00. This is a direct consequence of the natural loudness balances produced by this processing. Because sinewaves have a very low peak-to-average ratio compared with speech or music, their peak level must be reduced to prevent them (or similar program material) from being unnaturally loud and giving the processing an artificial, strained quality.

Second, a certain amount of headroom is left between the threshold of the first clipper and the threshold of the overshoot compensator to accommodate the distortion corrector signal and overshoots in the 15kHz lowpass filter without performing excessive, non-distortion-cancelling clipping in the overshoot corrector.

Because of the previously mentioned characteristics of the multiband compressor, sinewaves below about 2.5kHz are not ordinarily clipped; thus, no distortion-corrector signal is produced. However, varying the clip threshold does make better use of available headroom than would be the case if the clipper were always left at the "-1.0dB" threshold to which it switches in the presence of substantial high frequency energy.

It is important to note that despite (in reality, because of) this behavior with sinewaves, extremely high loudness is obtainable with speech or music because the processor's behavior is optimized for these signals.

5.b) 15kHz Phase-Corrected Lowpass Filter: (on Cards #8 and #9)

The signal from the hf limiter is applied through R801 to clipper CR801, CR802. The clipper output is applied to inverting amplifier IC801A through R802.

The output of IC801A (the clipped signal) is filtered by fifth-order Cauer lowpass filter R806, R807, C801, C802, C803, C804, C805, C806, C807, L801, L802, to remove high frequency energy generated by clipping which would otherwise induce "aliasing" distortion in the stereo generator. This lowpass filter is realized as a "passive ladder" for maximum stability. The filter's response is nominally +0, -0.6dB from 0 to 15.4kHz, with a sharp rolloff thereafter. There are two notches, the first of which occurs at 19kHz to provide extra protection for the pilot tone.

The load resistor for the filter, R807, is connected not to true ground, but to the "virtual ground" of the summing junction of IC801B. IC801B is an inverting, frequency selective amplifier, whose feedback network R808, R809, C808 provides a 2dB shelving rolloff. The purpose of this rolloff is to match the gentle rolloff of the 2.2kHz sidechain filter (see **5.c)** so that the distortion is correctly cancelled.

The output of IC801B feeds a differential sidechain which creates a fourth-order allpass function when its output is correctly summed with the output of IC801B (i.e., the main signal). This allpass function does not change the frequency response of the 15.4kHz lowpass filter, but does add phase shift as necessary to make the overall time delay of the 15.4kHz filter plus allpass network more constant than the time delay of the 15.4kHz filter alone.

Basically, this phase corrector sidechain consists of a pair of active inverting bandpass filters built around IC802A, IC802B. The IC802A filter is driven by the output of IC801B through R815. Its output is summed into summing amplifier IC803B through R817.

The second bandpass filter (associated with IC802B) is driven by both the main signal (through R814) and the output of the first bandpass filter IC802A (through R818). The output of IC802B sums into IC803B through R820.

The third input to IC803B is the main signal (through R810). The fourth (and final) input is the output of the 2.2kHz sidechain distortion-cancelling filter (through R822).

To restore flat response, the frequency response of this summation is boosted by passing the signal through a shelving filter complementary to the one realized in the feedback network of IC801B. The shelving boost is created by the R811, R812, R813, C809 in the feedback network of IC803B.

The output of IC803B is the output of the Smart Clipper. Because it contains substantial overshoots, it is connected to the FCS overshoot compensator (see **6** below).

5.c) 2.2kHz Distortion-Cancelling Filter Sidechain: (on Cards #8 and #9)

The distortion-cancelling sidechain takes the difference between the input and output of the clipper (which is the distortion added by the clipper). It then lowpass-filters this difference at 2.2kHz (thus substantially reducing the peak level), and finally sums the difference back into the main signal (at IC803B) to cancel clipping-induced distortion below 2.2kHz.

If no clipping occurs, the signal at the input side of R801 is equal and opposite to the signal at the output of inverting amplifier IC801A and no differential signal is produced. Because of the polarity reversal in IC801A, the difference between the input signal and the clipped output is derived by a simple summation through R804, R805.

This signal (our desired difference signal) feeds filter C814, L803, A1, whose magnitude and phase, when cascaded with additional rolloff R821, R822, C815, match the magnitude and phase of the phase-corrected 15.4kHz lowpass filter (see **5.b** above) from 0 to 2.2kHz. IC803A is a unity-gain buffer to drive this final rolloff network, the output of which is directly summed into IC803B.

6) Frequency-Contoured Sidechain (FCS) Overshoot Compensator:
(on Cards #8 and #9)

Overshoots are derived from the input signal by center clipper IC804A, R823, R824, R825, R826, CR803, CR804. This circuit is a differential amplifier which subtracts the output of a clipper from the clipper's input. This clipper consists of Schottky diodes biased with approximately ±4.2v, and is therefore substantially "harder" than the first clipper (associated with IC801A).

If the output of IC804A were simply added to its input, the sum would be a clipped signal; a "differential clipper" would be created. However, the output of IC804A contains clipper-induced high frequencies which could cause "aliasing" in the stereo generator. The output of IC804A is therefore lowpass-filtered by passive 15kHz ladder filter R828, R829, C816, C817, C818, L804, L805, before being added back into the input signal to cancel overshoots. This filter has a response that rises 4dB at 15kHz. This makes up for the loss of high frequencies which would otherwise reduce the peak level of the overshoots emerging from the filter. To compensate, the fundamental levels around 15kHz are increased by the frequency-contouring.

(**NOTE:** This "Frequency-Contoured Sidechain" overshoot compensation scheme is protected by U.S. Patent #4,460,871.)

The filter has phase shift. To assure correct addition of the filtered overshoot, the input signal is delayed in a modular phase shift network, A1, which whose amplitude response is flat, but which accurately matches the phase response of the sidechain filter throughout its passband. A1 is also equipped with a summing input for the overshoot signal, which appears at the output of IC804B.

The time delay of this network is not constant at all frequencies. The output of A1 is thus passed through allpass network IC805A, R831, R832, R833, R834, C819, C820 to create constant time delay from the input of the overshoot compensator system to its output. The allpass network has a flat amplitude response, but frequency-dependent phase response. (This network is designed to also compensate for the non-constant group delay of the following third-order lowpass filter).

The output of IC805A is passed through a composite capacitor (consisting of two aluminum electrolytics back-to-back, bypassed by a polycarbonate) to remove accumulated DC offsets. Recent research has indicated that this sort of composite structure minimizes the audible degradation caused by passing audio signals through polar capacitors with high dielectric absorption.

This capacitor is necessary because a differential DC offset between the left and right channels translates into a DC L-R component which, if not nulled, results in a fixed 38kHz component in the stereo generator output. This is equivalent to lack of 38kHz subcarrier suppression. Whatever fixed DC offset that is found at the output of the left and right audio processing channels is ordinarily nulled out by stereo generator alignment control R714. However, drifts in the differential offset in the order of 40mV can reduce the 38kHz suppression to less than the -40dB minimum specified by most government broadcast authorities.

The signal then passes through a third-order active 15kHz lowpass filter IC805B, R836, R837, R838, R839, C822, C823, C824 to provide further reduction of any remaining out-of-band energy above 19kHz.

Finally, to catch any slight errors made by the overshoot compensator, the signal is applied to safety clipper R840, R841, CR805, CR806. The basic overshoot compensator is extremely effective; thus, the safety clipper is virtually never active and no additional filtering is included after its output.

The output of the safety clipper is buffered by IC806A, which ordinarily drives the stereo generator. The output of IC806A (which is the audio processing output) also appears at the rear-panel TEST jacks when the rear-panel switch is in NORM.

7.a) Stereo Generator (General): (on Card #7)

The principles of operation of the stereo generator have already been discussed in **Appendix A.** The detailed operation of each of the sub-systems in the stereo generator will be discussed below.

7.b) 19kHz Oscillator: (on Card #7)

The crystal oscillator employs an AGC loop to enable linear oscillation. The output of the oscillator, IC705, is a 19kHz sinewave with typically less than 0.07% harmonic distortion.

The output of IC705 is reduced in level by voltage divider R747, R748 to avoid overdriving crystal Y701. Oscillation can be suppressed by turning JFET Q709 ON (by applying 0 volts to its gate), thus shorting R747 and virtually eliminating drive to Y701. Y701 operates in its series-resonant mode as a positive feedback element into the "+" input of IC705. Simultaneously, negative feedback is taken around IC705

through R742. The effective gain of IC705 is determined by the resistance between the "-" input of IC705 and ground. This resistance is the sum of R741 and the drain-source resistance of JFET Q708, operated here as a voltage-controlled resistor whose resistance is controlled by its source-gate voltage. As will be seen below, this voltage is determined by the 19kHz crystal oscillator AGC loop.

C709 prevents significant DC offsets from being developed at the output of IC705.

Approximately one-half of the AC source-drain voltage of Q708 is fed back into its gate through R743, R744, C710 to cancel second-harmonic distortion which would otherwise be introduced by Q708.

The positive peak output level of IC705 is sampled by comparator IC706, whose "+" input is biased to a DC reference voltage of +2.92 volts. If the peak output of IC705 attempts to exceed this level, IC706 turns on and charges C711 (towards -15 volts) through R749 and CR701. This voltage is coupled to the gate of gain-control FET Q708 through R744, thus closing the AGC loop.

Recovery time for the AGC loop is determined by R745. CR702 internally clamps IC706 to reduce saturation effects and speed its response time. C712 is a power-supply bypass capacitor.

7.c) 19kHz Doubler: (on Card #7)

The 19kHz output of IC705 is applied to both halves of dual comparator IC707. A -2.09 volt bias voltage is applied to pin 5 through R752, R753; a +2.09 volt bias is applied to pin 2 through R754, R755. The voltages and polarities are arranged so that each time the 19kHz sine passes through 45 degrees + (n x 90 degrees) (n=1,2,3...), the output of IC707 switches from high to low, or vice-versa. Its output is thus a 38kHz square wave 90 degrees out-of-phase with its 19kHz input. The <u>low</u> level at IC707's output is approximately -0.5 volts; the <u>high</u> level is controlled by the voltage applied from the output of IC709A to strobe terminals 9 and 13 of IC707. As will be seen below (see **7.e**), this closes the AGC loop which controls the amplitude of the 38kHz sinewave derived by filtering the output of IC707.

7.d) 38kHz Filter And Phase Shifter: (on Card #7)

The squarewave output of IC707 is connected to a high-"Q" "Q-enhanced" active bandpass resonator IC711, R775, R776, R777, R778, R779, R780, C718, C719, Q711, employing both positive and multiple-negative feedback to minimize sensitivity to component drifts and tolerances. The nominal "Q" of the resonator is 40.

This resonator is tuned by a control voltage applied to the gate of Q711, a JFET operating as a voltage-controlled resistor. Varying the resistance of Q711 varies both the center frequency and "Q" of the resonator. As will be seen below (see **7.f**), voltage control is derived from the Phase-Locked-Loop (PLL) circuit.

If the sum of the resistance of R777 and Q711 becomes too low (below about 780 ohms, nominally), then IC711 will oscillate at approximately 38kHz and produce a reasonably pure sinewave output. The circuit has been designed with considerable safety margin to prevent this from happening as long as all passive components in the circuit approach their specifications for temperature stability and long-term

drift. However, oscillation might occur if, for example, one of the components in the circuit were to exhibit severe drift. If this oscillation occurs, it can cause considerable confusion because the oscillation is easily mistaken by a service technician for the desired 38kHz component. Yet the oscillation is not precisely locked to the 19kHz pilot, is not controllable by the 38kHz AGC loop, and cannot be suppressed by turning off the 19kHz oscillator.

The output of IC711 contains perhaps 0.5% THD. To create a 38kHz sinewave in which all spurii are down at least 80dB, the output of IC711 is connected to a passive third-order elliptical lowpass filter R781, C720, C721, C722, L701. This filter is essentially flat to 38kHz, and provides substantial rejection for all harmonics. It exhibits a notch at 114kHz (third harmonic).

The output of the passive filter is buffered by IC712. Note that not all opamps of the generic type specified will work satisfactorily in this socket, and that the factory checks each opamp to make sure that its second harmonic (76kHz) distortion remains greater than 80dB below the 38kHz level.

Recalling that the 38kHz output of IC707 is 90 degrees out-of-phase with the 19kHz pilot, note that the total phase shift through both active and passive filters has been designed to create the necessary additional 90 degree shift to bring the 38kHz back into the proper phase relationship with the 19kHz pilot. This relationship is precisely maintained despite drifts in the filters by means of the 38kHz PLL circuit.

7.e) 38kHz AGC Loop: (on Card #7)

The output of the 38kHz passive filter is buffered by IC712. IC712's output is connected to the "-" input of IC710 .

IC710 is used as a comparator. Its "+" input is connected to the wiper of R772 (L-R GAIN), which provides a DC reference voltage for IC710. If the peak voltage of the 38kHz sine at the output of IC712 attempts to rise above the DC reference voltage at the "+" input of IC710, then IC710 will produce a negative-going output which discharges C715 through CR703 and R765. Under conditions where IC710 is non-conductive, the quiescent voltage on C715 is set at approximately +6VDC by means of voltage divider R763, R764. These resistors also determine the recovery time of the AGC loop.

C715 is buffered by means of unity-gain voltage follower IC709A. The output of IC709A is applied to the "strobe" inputs of IC707, thus adjusting the amplitude of the 38kHz square wave output from IC707 and completing the feedback loop.

7.f) 38kHz Phase-Locked Loop (PLL): (on Card #7)

The 38kHz output of IC712 is applied to the "+" input of one-half of dual comparator IC708 (used as a phase detector). The "-" input is grounded. The output of this "38kHz" half of IC708 is therefore a symmetrical 38kHz squarewave.

The output of the 19kHz oscillator IC705 is applied to the "-" input of the other half of IC708. The "+" input of this "19kHz" half is biased at +1.69VDC by means of voltage divider R759, R760. The output of the 19kHz half of IC708 is thus an asymmetrical 19kHz square wave.

The outputs of the two halves of IC708 are "OR"ed together. The output of IC708 is thus a 38kHz pulse whose duty cycle depends on the phase relationship between the 19kHz and 38kHz.

This pulse's baseline is approximately -0.5VDC; its peak is approximately +4.5VDC. The pulse is level-shifted by passage through C714, and then coupled to switching transistor Q710 to turn it on and off.

When Q710 is on, it saturates and essentially connects R767 to the +15V supply. The other side of R767 is connected to the "-" input of inverting integrator IC709B. Feedback forces this "-" input to be within a few millivolts of ground. Thus, when Q710 is on, exactly 1 mA flows into the summing junction of IC709B and is integrated by IC709B in conjunction with feedback capacitor C716. When Q710 is off, essentially no current flows. CR706 prevents the output of IC709B from going more than 0.7V positive, thus protecting C716 and Q711.

The feedback loop is closed by connecting the output of IC709B to the gate of Q711. Varying the voltage at the gate of Q711 varies its resistance, thus retuning 38kHz resonator IC711 and associated components (see **7.d** above) and changing the phase shift through IC711.

Current is removed from the IC709B summing junction through R768 and R769 (PILOT PHASE). Because of the integrator, the average current into the summing junction of IC709B must be zero. Otherwise, the output of IC709B would eventually go to the "+" or "-" power supply rails and saturate.

Feedback from the output of IC709B thus adjusts the phase shift in IC711 (and thus the duty cycle of the current pulses through R767) until the average current into the "-" input of IC709B is zero. The amount of current removed from the "-" input of IC709B is adjusted by the operator (by means of R769) until the desired phase relationship between the 19kHz pilot and 38kHz output of IC712 is achieved.

Once adjusted, the stability of this relationship is primarily dependent upon the stability of phase detector IC708. The 38kHz side is referenced to ground. Therefore, changes in the amplitude of the 38kHz input will have virtually no effect upon the duty cycle of the output of the 38kHz side of IC708. However, the duty cycle of the 19kHz side of IC708 is highly dependent upon maintaining the amplitude of the 19kHz constant. Ordinarily, this is effectively done by means of the 19kHz oscillator AGC loop (see **7.b**). A failure in this loop can therefore cause drifts both in pilot level and pilot phase.

In addition, leakage in Q710 can cause instability problems, particularly if the leakage changes with time and/or temperature.

7.g) L-R Amplifier: (on Card #7)

The difference signal is derived by means of differential amplifier IC701 and associated components. The left input is applied to R707, which is the inverting (-) input of the differential amplifier. The right channel is applied to R708, which is the non-inverting (+) input of the differential amplifier.

Trimpot R709 (MAIN-SUB CROSSTALK) adjusts the non-inverting gain of the amplifier without affecting the inverting gain. This permits precise cancellation of

common-mode (L+R) input components, and thus allows the linear main-channel to subchannel crosstalk (which represents L+R components which have leaked into the subchannel) to be nulled.

The non-inverting gain of the differential amplifier is switched from +1 to +2 by turning off Q705 (by placing -15V on its gate). Ordinarily, the amplifier requires a gain of +1. However, in the SUB-TO-MAIN crosstalk test mode, the amplifier must take a gain of +2 to create the same peak modulation level that a given input level would create in the NORMAL operating mode.

7.h) 38kHz Doubly-Balanced Modulator: (on Card #7)

The operation of the modulator is very similar to the operation of the voltage-controlled amplifiers used in the audio processing section, and the reader should first refer to **2.c** above.

The essential difference between operation of the audio VCA's and operation of the 38kHz modulator is that the audio VCA's are operated in a divider mode, and the 38kHz modulator is operated in a multiplier mode. Thus control current in IC703B is varied to perform the multiplication function.

Control current in IC703B is the sum of a bias current (through R727) and a 38kHz modulating current which is coupled through R726 and DC blocking capacitor C704. (Pin 3 of IC703B ordinarily sits at approximately -13.5V). The bias current is necessary because pin 3 can only accept control currents of one polarity. However, it also means that the 38kHz modulator multiplies its L-R input times a constant, thus passing some L-R directly without modulating it by 38kHz. This feedthrough component (which undergoes a phase reversal when passing through the modulator) is cancelled by feeding in-phase L-R around the modulator through R734. Final adjustment of the feedthrough cancellation (which is equivalent to nulling subchannel to main-channel crosstalk) is effected by slightly trimming the bias current in IC703A by means of R717 (SUB-MAIN CROSSTALK), thus varying the gain of the modulator. (**NOTE:** This adjustment will also affect L-R gain and thus separation. If for some reason R717 is adjusted, R772 will also have to be slightly trimmed.)

Cancellation of the residual 76kHz second-harmonic output of the modulator (which results from unavoidable non-linearities) is effected by passing a very small amount of 38kHz from R725 (76KHZ NULL) through R723 into the "-" input of IC703B. This component is multiplied in IC703B by the main 38kHz component to create a 76kHz component of correct amplitude and phase to cancel the basic 76kHz feedthrough in the modulator.

The basic feedthrough is in the order of -70dB; this circuit typically reduces it to slightly below -80dB. It can therefore be seen that the circuit is not terribly critical, and moderate drifts with time and temperature will not result in difficulties.

The circuit affects only the 76kHz component, and not sidebands which appear around it due to L-R modulation. These sidebands are a function of (1) basic modulator non-linearity, and (2) any residual second harmonic appearing in the 38kHz modulator input (from the output of IC712).

If the 76kHz sidebands have excessive energy, they can interfere with SCA service. In most production units, these sidebands are down -75dB or more below 100% with pure L or R modulation, and will of course disappear with pure L+R, since no audio is applied to the modulator in this case. This performance is far better than required to fully protect an SCA. If interference to SCA suddenly develops, and a spectrum analyzer connected directly to the composite output of the 8100A/1 reveals high levels of 76kHz sidebands, then the most likely sources of difficulty are IC703 itself, or else substantial second-harmonic distortion at the output of IC712. IC703 is a specially selected and graded device, and replacements must be obtained from the Orban factory. (**NOTE:** Replacement of IC703 requires a complete stereo generator realignment as detailed in **Appendix E**).

The output of IC703B is in the form of a current. This is converted to a voltage by means of output summing amplifier IC704.

Q706 switches the "stereo" components onto IC704's summing junction depending on whether the 8100A/1 is in "stereo" or "mono" mode. These "stereo" components include the output of IC703B, the L-R cancellation component from R734, the 19kHz pilot, and a DC offset null current.

The pilot is summed through R733 from the wiper of PILOT INJECTION trimmer R731. The DC offset component is summed through R729, R730 from the wiper of DC OFFSET trimmer R726. C705 bypasses any power supply noise.

The purpose of the DC offset adjust is to render an output coupling capacitor unnecessary. Such a capacitor would have to be a very large polar electrolytic (approximately 470uF or greater). Not only would such a capacitor compromise low frequency separation slightly, but its existence would also tend to compromise the extreme transparency of the basic 8100A/1 signal path, since recent research has indicated that such capacitors audibly degrade sound quality.

7.i) L+R/Mono Path: (on Card #7)

The L+R component at the output of the 8100A/1 is created by passively mixing L and R, and then by summing the mixture into IC704. L and R pass through precision-matched resistors R701 and R702 and then through switching FET's Q701, Q702. When driver transistors Q703, Q704 are off, the gates of Q701, Q702 are connected to their drains through R703, R704, thus holding Q701, Q702 on. When Q703, Q704 turn on, they turn off the left or right channels respectively by pulling the gates of Q701, Q702 close to -15 volts and turning Q701, Q702 off.

The sum is attenuated by virtue of R701 and R702's being the top of a voltage divider, the bottom of which is the resistor network R735, R736, R737. R735 is simply the summing resistor into IC704. The attenuation of the overall voltage divider is controlled by adjusting the resistance of its lower leg. This is done by turning Q707 on or off. In stereo mode, Q707 is on and results in highest attenuation. In mono mode, the attenuation must be reduced by 6.84dB to permit a single channel (without pilot) to modulate the transmitter to 100%. This is achieved by replacing the very low on-resistance of Q707 with the higher resistance of R737.

7.j) Output Summing Amplifier: (on Card #7)

Little need be said about this amplifier which has not been stated above. IC704 is a conventional inverting summing amplifier. Its gain is adjusted by means of its feedback resistor, OUTPUT ATTENUATOR R738. IC704 is a fast 518-type amplifier, and is somewhat prone to instability when loaded with capacitive loads such as coax. To isolate the amplifier from such loads, R739 is placed between the output of IC704 and the 8100A/1's composite output. The source impedance of the composite output is thus 470 ohms regardless of the setting of R738.

7.k) Mode Switching Logic: (on Card #7)

The three basic logic states -- stereo, mono left, and mono right -- are "remembered" by three CMOS NAND gates in IC714. The output of each gate is connected to an "output bus" through a 47K isolation resistor R783, R784, R785 to permit pulling a given output bus down without damaging its associated gate. "Negative logic" is used; a sub-mode is ON when its output bus is at -15V, and OFF when its output bus is at ground. The two inputs of each gate are connected to the two output busses of the other two gates. Thus, if either of the other gates is ON, the gate in question is held OFF. However, if the output bus associated with the gate in question is externally pulled ON, the other two gates are pulled OFF; thus the gate in question is latched ON. Logic switching is effected by momentarily switching any of the gate output busses to -15V; this is done by forcing the transistors in optoisolators IC715, IC716, IC717 to conduct by passing current through their LED's (remote control), by operating the momentary front-panel STEREO/MONO switch, or by the power-up circuit, which uses R786, C723, and CR712 to hold a selected output line at -15 for a fraction of a second after powerup.

Failures in the logic will almost certainly be due to failures of IC713-IC717, or to failures in the JFET switching transistors. All of these components can be freely replaced as necessary without readjustments.

Note that the phototransistors in IC715-IC717 have had their base leads (pin 6) cut off flush with the IC package. This is because the base lead is extremely sensitive to leakage currents, and condensing moisture is quite sufficient to cause false switching. It is therefore extremely important that the base lead be cut off if any of these optoisolators are ever replaced.

Essentially no further circuit description is required, as most of the circuitry is integrated onto the CMOS logic chips. The discussion of operational principles supplied in **7.k** of **Appendix A,** plus examination of the truth table found on the schematic for Card #7, should suffice to permit full understanding of the operation of the logic. (Some readers may be unfamiliar with the Exclusive-OR gate, IC713. This logic element operates such that its output is at -15 volts when its inputs are the same, and at 0 volts when its inputs are different.)

8.a) Unregulated Power Supply: (on chassis outside RF-tight enclosure)

The unregulated power supply is wholly conventional. It consists of a dual-primary transformer T101, two full-wave rectifiers CR101, CR102 and CR103, CR104, and two energy storage capacitors C101, C102.

T101's primary may be switched for 115 volt operation by paralleling its two primaries, or for 230 volt operation by connecting its two primaries in series. RF filtering is provided on the AC line by means of FL101. In addition, VHF and UHF RF is filtered from the unregulated DC supply lines as they enter the main chassis by means of C103, C104, C105, C106, C107, L101, L102. The RF suppression scheme divides the chassis into three major sections. The section to the left contains the AC wiring and the unregulated power supply, and is assumed to contain some RF. The main chassis, to the right, uses RF suppression on each line entering or leaving the area, and is thus RF-free. The RF filter box, on the rear panel, interfaces the audio input and output lines with the outside world. It contains the input pads. Its connections to the main RF-tight compartment are all RF-filtered.

8.b) +15 Volt Regulator: (on Card #1 -- rear chassis apron)

The +15 volt regulator is the main reference for all other voltages in the OPTIMOD-FM system. It employs a 723C IC voltage regulator IC101 in conjunction with an external series-pass transistor Q101. This transistor is mounted on the rear apron of the chassis, which serves as a heat sink.

The 723C contains a reference voltage source, an opamp (externally compensated by means of C109 to prevent oscillation), and a current limiting transistor. The reference voltage (nominally +7.15 volts) is developed at pin 6. C108 filters high frequency noise from the reference voltage. The reference voltage is directly connected to the non-inverting input of the internal opamp, pin 5. Voltage divider R105, R106, R107 develops a precise fraction of the output voltage of the regulator at the wiper of R106. R106 adjusts this fraction. The wiper of R106 is connected to the inverting input of IC101's internal opamp. Negative feedback thus forces the voltage at the wiper of R106 to be equal to the reference voltage. Thus the output voltage of the regulator is always the reference voltage divided by the voltage divider gain.

The output current flowing through Q101 develops a voltage drop across R103. When the current exceeds approximately 3/4 amp, said voltage drop is sufficient to turn on the current-limit transistor inside IC101, whose base-emitter junction is connected to pins 2 and 3 of IC101. The current-limit transistor then shunts base drive current from the external series-pass transistor Q101 and prevents damage due to overheating.

If a catastrophic failure in the +15 volt regulator causes it to lose control over its output voltage, the rest of the circuitry must be protected against the full unregulated voltage, or the entire system will be severely damaged. This protection is provided by zener diode VR101, CR105, and 1 amp fast-blo fuse F102.

In the event that the regulator loses control of the output voltage, VR101 will conduct and limit the output voltage to approximately 16.5 volts, which will not damage the system. Extremely large amounts of current will flow in VR101. However, before VR101 is damaged, this current will blow F102, thus disconnecting the circuitry from the unregulated supply. VR101's clamping action will also prevent the negative tracking supply from going any higher than -16.5 volts. If the regulator is operating properly, the current limiting circuitry will prevent F102 from blowing even if the regulator output is short-circuited.

Under certain unusual circumstances, the regulator may lose control of its output voltage, yet the current limiting circuit may still work. If this occurs, F102 will not blow, and VR101 will overheat and burn out. Fortunately, its failure mode is a short-circuit. It will therefore still protect the OPTIMOD-FM circuitry even in this exceptional circumstance.

8.c) -15 Volt Regulator: (on Card #1 -- on rear chassis apron)

The -15 volt regulator is an operational amplifier containing a discrete power-booster output stage with current limiting. It "amplifies" the output of the +15 volt regulator by -1, thus producing a -15 volt tracking supply. Shutdown of the +15 volt supply (due to current limit conditions or to a fault which blows F102) will also result in the -15 volt supply's shutting down.

The basic opamp is IC102; its input resistor R109 and feedback resistor R108 are equal-valued, resulting in a gain of -1 ±2%. IC102's negative supply comes from the unregulated -22 volt supply. The common-mode range of the 301A opamp includes the positive power supply, thus permitting operation with IC102's positive supply at ground. Under normal operating conditions, the "+" input of IC102 is grounded, and its "-" input is within 10mV of ground.

Q103 and Q102 form a conjugate emitter follower which can boost the output current of IC102 to more than 3/4 amp. The basic emitter follower is Q103; Q102 is connected in a 100% negative feedback configuration to boost the current output capability of Q103.

Q104 is a current-limit transistor. If the -15 volt supply is called upon to deliver more than 3/4 amp, sufficient voltage drop (approximately 0.6 volts) will occur across R104 to turn on Q104, thus shunting drive current away from Q103 into the load and protecting Q102/Q103 from burnout. Under these conditions, IC102 is protected by internal current limiting circuitry.

C113 frequency-compensates the -15 volt supply to protect it against high frequency oscillations. R102 increases the circuit's immunity to leakage in Q103.

The rest of the circuitry is protected against a catastrophic failure of the -15 volt regulator by means of zener clamp VR102, CR106, and fuse F103. The operation of this circuit is identical to the operation of the corresponding circuit in the +15 volt regulator (see **8.b**).

8.d) Miscellaneous Voltage Supplies:

The operation of these supplies is extremely straightforward. No further explanation beyond that given in **Appendix A** is required.

APPENDIX C:

User Access

ROUTINE ACCESS

The first part of this Appendix describes how to access those parts of OPTIMOD-FM ordinarily involved in setup, adjustment, or alignment. (The second part of the Appendix provides information on the disassembly techniques necessary to access the balance of the circuitry.)

a) User Adjustments: To access the user adjustments, open the small access door using the key furnished. This will reveal all user-adjustable controls.

b) Line Fuse, Power Switch, and Line Voltage Selector: These are accessed by swinging down the entire front panel, which is hinged at the bottom. To avoid damage, this should be done only with the small access door locked. Using the 5/64" hex wrench supplied, remove the three hex-socket screws at the top of the front panel and carefully swing the panel out and down.

c) Circuit Cards: First, swing the front panel down (see **b**). You must then remove the subpanel by first loosening four DZUS fasteners by turning each one-quarter turn counterclockwise with a long 3/16" or 1/4" slotted-blade screwdriver. Taking care not to stress the flat cable beneath it, tilt the top of the subpanel outward and leftward to clear the upper chassis lip and the door support bail at the right. The PC cards may now be removed from their slots.

**** This procedure is directly reversible with cautions:

-- The subpanel should always be replaced to protect the cards from RFI.

-- DZUS fasteners turn only 1/4-turn. Don't force them, lest they be damaged in a way that is very time-consuming to repair.

NOTE

OPTIMOD-FM Model 8100A/1 shares chassis components with other Orban products. In the 8100A/1, the first available card slots are not used, and there is no Card #2. The power supply regulator card is Card #1 (which is mounted on the rear panel).

SERVICE ACCESS

General Cautions: These apply to all the procedures described below.

-- For best RFI protection, replace all screws and tighten normally to achieve firm contact.

-- If screws are lost, replace them with screws of the same length, since longer screws may cause mechanical interference or internal short circuits.

> The installation and servicing instructions in this manual are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the Operating Instructions unless you are qualified to do so. Refer all servicing to qualified personnel.
>
> (per UL 813)

-- Most screws used in OPTIMOD-FM are binding head to achieve secure fastening without lockwashers. If a pan head screw is substituted, use an internal star lockwasher to retain this security.

-- Plating on all screws is Cadmium type II. Almost any other plating is acceptable unless corrosive atmosphere is present.

a) Cover Removal: Removing the top or bottom covers is tedious because thirty screws must be removed. (The large number of screws is necessary to achieve an RF-tight seal.) Luckily, most service access can be achieved without removing either cover! Specific instructions for doing this are found below.

If you wish to remove either cover, simply remove all thirty screws.

**** This procedure is directly reversible with cautions:

-- When replacing a cover, align it as closely as possible with the corresponding holes, and start all screws. After all screws have been started, tighten all screws to normal tightness, "inland" screws first.

b) Access To Area Behind Rear Panel: If the covers are still in place, they needn't be removed.

Remove eight screws holding the top cover to the flange of the rear panel. Remove the corresponding eight screws from the bottom cover. The rear panel will remain solidly in place.

Set the chassis, bottom cover down, on a pad on a table. Allow 6" (15cm) between the rear panel of the chassis and the table edge. Unplug the power cord.

Now remove three groups of three screws which are circled in black on the rear panel.

VERY carefully and slowly, pull the rear panel about 3/4" (2cm) toward you, and tilt the top edge down until the rear panel is horizontal and resting on the table.

CAUTION

Watch for snags in the internal wiring, and for any stress on the ceramic feedthrough capacitors on the divider wall or input filter box. These capacitors are very fragile and difficult to replace.

**** This procedure is directly reversible with cautions:

-- When positioning the rear panel over the corresponding holes, make sure that no wires are pinched under the flanges. Start, but do not tighten all nine screws. Observe the areas where the flanges on the rear panel meet the flanges on the side panels. Adjust the rear panel so that the flanges line up in order to provide a flat mounting surface for the cover when tightened.

c) Access To RF Filter Card: First open the rear panel (procedure **b** above).

Remove the four screws holding the Input Filter Box to the rear panel. **VERY** carefully and slowly, tilt the metal box back to vertical, taking care to avoid snagging the internal wiring and stressing the ceramic feedthrough capacitors.

This will reveal the internal circuit card, which is attached to the rear panel by four #4-40 screws. While this card can be removed for component replacement, it is easier (though less workmanly) to clip out the defective component from the topside and to install its replacement by tack-soldering to the old leads.

**** This procedure is directly reversible with cautions:

-- If components have been replaced, make sure that reassembly will not result in crushing of the component against the rear panel.

-- Tilt the box back to horizontal (so it rests against the rear panel) very slowly and carefully. Watch for wire snags and dress wires appropriately. Make sure that no wires are crushed under the flange.

d) Access To Unregulated Power Supply Chamber: If the covers are not already removed, remove the five cover screws which attach the top cover to the flange of the side panel. Remove the corresponding five screws from the bottom cover.

Open the front panel.

Remove the shoulder screw that attaches the door-support bail to the left chassis wall. Note that there is a nylon washer between the bail and chassis wall to prevent scraping.

Turn the chassis so that the left wall is facing you. Remove the left rack flange by removing the six unrecessed screws.

Remove the three screws that attach the rear panel to the main (steel) side panel.

Remove the remaining six screws and gently lift off the side panel by pulling outward.

**** This procedure is directly reversible with cautions:

-- Position the steel side panel and start, but do not tighten, all nine screws. Observe the areas where the flanges meet the rear panel and internal bulkhead, and align the flanges so that the covers will seat on a flat mounting surface.

e) Removal Of Card #1 (The DC Regulator) From Rear Panel And Power Transistor Replacement: Because the removal procedure is complex, this card was designed to permit many servicing operations to be performed without removing the card from the chassis.

The plastic transistors and some capacitors are socketed in very tiny sockets pressed into the card. IC's are conventionally socketed. Many unsocketed components can be replaced from the topside by tack-soldering the new component to the lead stubs of an old clipped-out component.

If the card must be removed, do it as follows:

CAUTION

The rear panel serves as a heat dissipator for the power transistors. Proper contact is necessary to insure sufficient transistor cooling. Please follow instructions carefully.

Remove the four press-fit plastic plugs on the power transistor covers with a pair of chain-nose pliers. This will reveal the transistor mounting screws. Remove the four screws holding the power transistors.

VERY carefully and slowly pull each transistor from its socket. If, as you do this, the silicone rubber insulator tends to stick to the panel, release it from the panel such that it sticks to the bottom of the transistor instead. After you remove each transistor, press its insulator back in close contact with it pending reinstallation.

NOTE

These insulators form themselves to the bottom surface of each transistor. Since they take a "set", they should not be interchanged or reversed. If you have to replace a power transistor, you may re-use the insulator if it is in good condition. With care, it will re-form itself as necessary. Otherwise, use a conventional mica insulator and white silicone heat-conducting compound.

Open the rear panel (procedure **b**). With the transistors removed, it is possible to release the circuit card from its plastic post mounts by squeezing the tangs in each of the four corners to permit pulling the card off the posts.

**** This procedure is directly reversible with cautions:

-- See the discussion above regarding heat-conduction insulators.

-- The screws mounting the transistors should be tightened evenly. For best thermal contact, tighten each screw a small amount, alternating between screws. Tighten securely, but not enough to damage the threads in the sockets.

-- Note that there must be a split lockwasher under each screwhead to accommodate thermal cycling.

-- The Thermalloy plastic cover does not attach in a conventional or readily obvious way. It rides on the circumference of the special split lockwasher and does not (and should not) become captured under the head of the screw. Consequently, the cover may be slightly loose even after screws are tightened securely. This is normal, and should not (and cannot) be corrected.

-- Be sure to reinstall the press-fit plugs that cover the screwheads.

APPENDIX D:

Field Audit-of Performance Procedure

GENERAL

This Appendix provides instructions enabling Model 8100A/1 users to check the performance of their units using test equipment likely to be found in a well-equipped radio station. This procedure is a starting point for detecting and diagnosing a problem that you believe is caused by the 8100A/1. It is also useful in routine maintenance, and can be used at Proof time to check routine equipment performance, thus providing more data than the Proof alone provides. By its nature, it is limited in scope to discovering static problems. A dynamic problem in the AGC circuitry (caused by the failure of a timing module on Card #5, for example) would not tend to be discovered by performing these tests.

For this reason, measurements must always be complemented by listening. If you are well-acquainted with the "sound" of the 8100A/1 as adjusted for your format, then faults that develop will ordinarily be readily detectable by ear.

If audio problems develop, many engineers immediately tend to blame their processing. However, as is the case with any processing, faults in the audio equipment preceding OPTIMOD-FM will be magnified by the action of the processing. Program material that is marginally distorted at the 8100A/1 input, for example, is likely to be unlistenable by the time it emerges from the output when aggressive processing is used. In addition, be sensitive to possible defects in the monitoring equipment; verify that a problem can be observed on at least two receivers before pushing the panic button.

D

REQUIRED EQUIPMENT

a) Audio Oscillator. An ultra-low-distortion type like the Sound Technology 1710B is preferred. However, a Heathkit or Eico-type oscillator (such as Heath IG-72) can be used to obtain approximate results, provided that residual distortion has been verified to be below 0.1%.

b) Noise and Distortion (N&D) Test Set. Once again, a high-performance type like the Sound Technology is preferred, but not required.

c) General-Purpose Oscilloscope. DC-coupled, dual-trace, with at least 5mHz vertical bandwidth. This is used to monitor the output of the N&D Test Set, and also to check the stereo generator.

d) Type-Approved Stereo Monitor. The Stereo Monitor will be directly connected to the 8100A/1 baseband output, and its associated FM monitor is therefore not required.

AUDIO PROCESSING

It is often more convenient to make measurements on the bench, away from high RF fields which might otherwise affect results. For example, in a high RF field, it is very difficult to accurately measure the very low THD produced by a properly-operating 8100A/1 at most frequencies. However, in an emergency situation (is there any other kind?!), it is usually possible to do measurements under high-RF conditions which will reveal many of the grosser faults which could develop in the 8100A/1 circuitry.

The audio processing section of the 8100A/1 can be measured independently of the stereo generator by using the rear-panel TEST JACKS as the point to which measuring equipment is connected. The following procedure assumes that all test excitations are applied to the rear-panel main audio input terminals, and that all responses are measured at the TEST JACKS.

a) Standard Control Setup: Record the normal settings of the controls so that they can be reset after the measurements have been completed. Then set the controls as follows:

L and R Input Attenuators:	0
Clipping:	+2
Release Time:	10
Bass Coupling:	10
Gate Threshold:	0
H-F Limiting:	0

b) Skeleton Proof: This should be performed for both left and right channels.

1) Place both PROOF/OPERATE switches in PROOF.

2) Connect a low-distortion audio oscillator to the 8100A/1 input. Set the frequency to 15kHz, and adjust the oscillator output level to produce 3.3V rms at the 8100A/1 output.

3) Connect the input of the N&D test set to the 8100A/1 output through a 75us (or 50us, if that is your country's standard) deemphasis network. (If the N&D set has its own deemphasis available, this is obviously not necessary.)

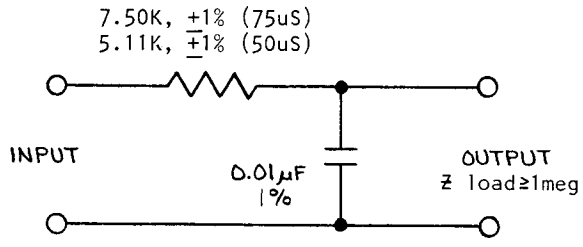

Fig. D-1:

4) Now measure the frequency response by measuring the oscillator output required to produce 3.3V rms (an internal level corresponding to 100% modulation) at the 8100A/1 output at 50, 100, 400, 1000, 5000, 10,000, and 15,000 Hz. If you use the AC voltmeter in the N&D Test Set to measure oscillator and/or 8100A/1 output levels, bear in mind that the 75us deemphasis network must not be used for these measurements.

5) Since the frequency response test requires you to readjust the oscillator output level at each frequency to produce 100% modulation at the 8100A/1 output, it is often convenient to measure the THD @ 100% modulation at the same time that you measure frequency response. If you are using the the N&D Test Set's AC voltmeter in the frequency response test, remember that you must connect the 75us deemphasis network to the N&D meter input for the THD measurements only.

6) Plot the results of the frequency response measurement on a standard 75us (or 50us) preemphasis graph like FCC #73.333 (USA). The points should be within ±0.75dB of the standard preemphasis.

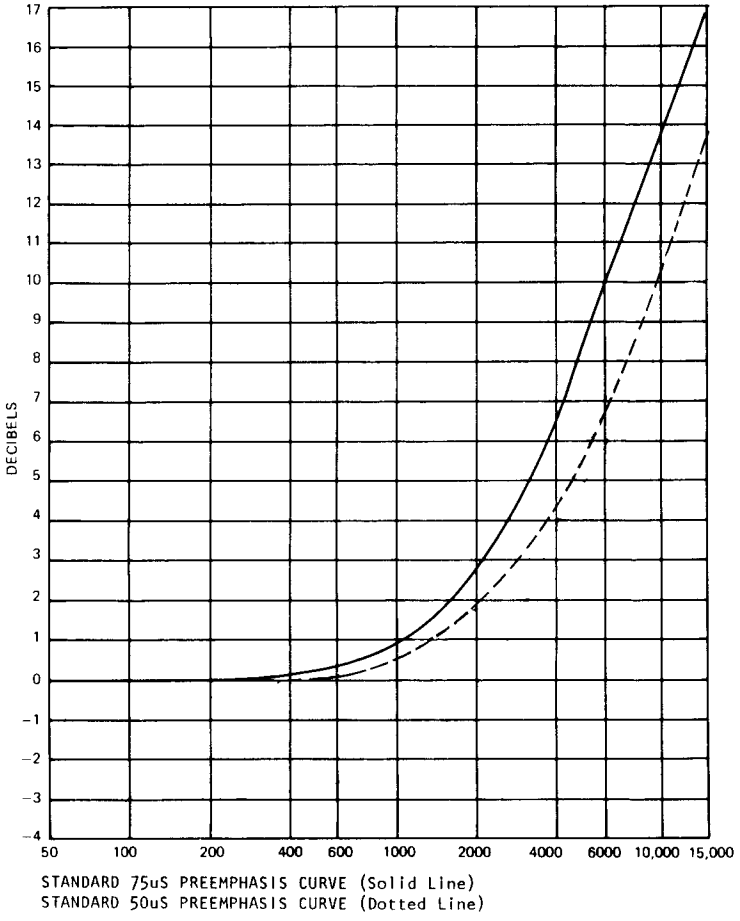

Fig. D-2: Preemphasis Graph

7) The deemphasized THD should not exceed 0.05% at any frequency. In many cases, results will be determined entirely by the quality of oscillator and distortion analyzer available, and/or by the presence of RF fields which might affect the instruments.

(A more accurate frequency response evaluation can be performed by sweeping the system with a test set like the Tektronix 5L4N Spectrum Analyzer/Tracking Generator. If the station has such equipment, see paragraph 6.c of **Appendix E** for further information.)

8) **Noise:** Short both 8100A/1 inputs, and measure the deemphasized noise at the 8100A/1 output through the 75us deemphasis network. It should not exceed -63dBm. (Note that hum or buzz due to test equipment grounding problems and/or high RF fields may result in falsely high readings. If the output of the N&D set is monitored with a scope, problems like this should be immediately apparent.)

c) Operate-Mode Measurements: These measurements evaluate certain static characteristics of the 8100A/1 in its normal OPERATE mode. Normal measurements given herein are provided for service guidance only, and are not guaranteed. As in the PROOF mode measurements above, these measurements should be repeated for both left and right channels.

1) Reconnect the audio oscillator to the 8100A/1 input. Switch both 8100A/1 PROOF/OPERATE switches to OPERATE. Be sure that operating controls are standardized as described in (a) above. Set the oscillator frequency to 1kHz, and adjust the oscillator output level to produce 10dB G/R as read on the MASTER G/R meter on the 8100A/1 front panel.

2) Verify that the 8100A/1 VU meter reads 0 VU $\pm$0.5VU in the COMPRESSOR OUT position.

3) Measure the 8100A/1 output level and THD for each frequency indicated in the table below, and compare your results with the typical readings provided.

Table D-1

50Hz	2.05V rms; less than 0.1% THD
500Hz	2.14V rms; less than 0.1% THD
3kHz	2.50V rms; approx. 2.1% THD
12kHz	2.30V rms; less than 0.1% THD

The increase in THD at 3kHz is caused by a combination of factors, including the "standard" control settings (which are atypical of operating settings), and the fact that this distortion is the result of slight clipping permitted by the Smart Clipper circuitry. The distortion-cancelling clipper in the 8100A/1 exploits the fact that the ear is quite insensitive to very high frequency harmonic distortion (the major distortion component in the 3kHz test is third-harmonic at 9kHz), and is far more disturbed by low-frequency IM distortion. At 12kHz, all clipper-induced harmonic distortion is filtered out by the 15kHz lowpass filters.

Excessive THD at 50Hz not present in the PROOF-mode test is ordinarily caused by problems in the bass timing module on Card #5. Excessive THD at 500Hz is often caused by problems in the master timing module on Card #5. (See paragraph **2.d** of **Appendix B**).

Atypical THD at 3kHz can be caused by several factors. Excessively high THD can be caused by a failure in the HF limiter on Card #6 (see paragraphs **4.a** and **4.b** in **Appendix B**). Excessively low THD can be caused by excessive action of the HF limiter, or by failure in the dynamic clipper-threshold adjustment circuitry (see paragraph **5.a** of **Appendix B.**)

4) Now turn the H-F LIMITING control to 10. Sweep the oscillator frequency up from 1kHz, and determine what frequency first turns the front-panel H-F LIMITING lamp ON. This frequency is typically 1.6kHz.

Steps (5) and (6) below provide a first-order test of the dynamics of the timing circuitry in the compressor. However, there are many possible faults which these tests will not detect. These must be diagnosed by more sophisticated tests at the factory.

5) Turn the BASS COUPLING control to "0". Set the oscillator frequency to 5kHz, and adjust the oscillator output level to produce 15dB G/R as indicated on the MASTER G/R meter. Switch the COMPRESSOR PROOF/OPERATE switch to PROOF and measure the time required for the MASTER G/R meter to fall from 15dB to 5dB indicated G/R. This time should be 6 seconds, ±1.5 seconds.

6) Change the oscillator frequency to 50Hz and turn the oscillator's output level control all the way down. Restore the COMPRESSOR PROOF/OPERATE switch to OPERATE, and advance the oscillator output level until the 8100A/1 BASS G/R meter reads 15dB G/R. Switch the COMPRESSOR PROOF/OPERATE switch to PROOF, and measure the time required for the BASS G/R meter to fall from 15dB to 5dB indicated G/R. This time should be 3 seconds, ±0.75 second.

This concludes tests of the audio processing circuitry.

STEREO GENERATOR

This test procedure requires only the use of an audio oscillator, the station's stereo monitor, and an oscilloscope. It has been our experience that the 8100A/1 stereo generator is far more stable than most monitors. Therefore, accurate measurement and adjustment of separation and pilot phase is best done with an oscilloscope. Crosstalk, 38kHz suppression, and pilot parameters cannot be conveniently measured on a scope, and must therefore be measured on the stereo monitor.

a) Stereo Performance Measurements

1) Connect the oscillator to the right-channel 8100A/1 audio input. Connect the stereo monitor to the 8100A/1 baseband (BNC) output.

2) Place both PROOF/OPERATE switches in PROOF. Place the rear-panel TEST/NORMAL switch in NORMAL. Turn the PILOT ON/OFF switch ON. Place the 8100A/1 CROSSTALK TEST switch in OPERATE. Connect an AC VTVM to the right channel TEST JACK on the rear panel. Set the oscillator frequency to 1kHz, and adjust the oscillator output level to produce 3.3V rms at the right TEST JACK.

3) Set the 8100A/1 OUTPUT ATTEN fully CW. Adjust the stereo monitor input sensitivity to produce an indication of 100% modulation on the right channel. (If this cannot be achieved, readjust the 8100A/1 OUTPUT ATTEN appropriately.)

4) **Crosstalk:** Use the stereo monitor to measure main-channel-to-subchannel and subchannel-to-main-channel crosstalk at 50, 400, and 15,000 Hz at 100% modulation. Use the 8100A/1 CROSSTALK TEST switch to produce the appropriate signals. (The CROSSTALK TEST switch takes the right channel input signal and uses this signal to create pure L+R [main-to-sub] or pure L-R [sub-to-main] modulation.) Note that because of preemphasis, substantial adjustment must be made in the oscillator output level to keep the modulation percentage constant as frequency is varied. Verify that crosstalk does not exceed -40dB at any frequency. (**NOTE:** Typically, you will be measuring the performance of the stereo monitor in this test. Only a baseband spectrum analyzer is sufficiently selective to accurately measure the 8100A/1 stereo generator's crosstalk performance.)

5) **38kHz Suppression:** Return the 8100A/1 CROSSTALK TEST switch to OPERATE. Modulate the right channel to 100% at 7.5kHz. Use the stereo monitor to verify that the 38kHz subcarrier suppression exceeds -40dB.

6) **Separation:** Connect the oscilloscope to the 8100A/1 baseband output. DO NOT USE AN ATTENUATOR PROBE; this may compromise the accuracy of the measurement. Trigger the scope externally from the oscillator. Turn the 8100A/1 PILOT switch OFF. Leave the oscillator connected to the right 8100A/1 audio input. Set the scope's vertical sensitivity to 0.5V/div, and DC-couple the input.

Set the oscillator frequency to 1kHz, and adjust the oscillator output level and the scope sweep rate to produce a scope pattern that looks like Fig. E-4 (in **Appendix E**). Separation is measured by determining the flatness of the baseline. If the 8100A/1 has been tweaked to compensate for a given exciter/RF amplifier/antenna system, then the baseline might not be quite flat. You must decide at this point whether to retain the current adjustment (for the sake of expediency) or whether to readjust the SEPARATION control (to determine the amount of separation which the system is capable of providing). If the baseline is almost flat, this implies that no fault has occurred in the stereo generator, and further tests are not required.

If you wish to measure separation, first expand the scope vertical scale to 50mV/div. Next adjust the 8100A/1 SEPARATION control to secure the flattest possible baseline. The separation is then calculated by the formula: $S=20\log(D/4)$, where S is the separation in dB, and D is the peak-to-peak deviation of the baseline from flatness (in volts).

Measure the left-into-right and right-into-left separation at 50Hz, 1kHz, 5kHz, and 15kHz, alternately driving the left and right channels and shorting the undriven channel.

The separation should be greater than 45dB, 50-15,000Hz, and is typically better than 60dB. (60dB is the practical limit of resolution for the oscilloscope separation measurement technique.)

7) **Pilot Phase:** Connect the oscillator to the 8100A/1 right audio input. Turn the pilot ON, and place the CROSSTALK TEST switch in SUB-TO-MAIN. Adjust the oscillator frequency to 1kHz (non-critical). You should see a scope pattern like Fig. E-5 (**Appendix E**). Expand the scope display to examine the zero-crossing region (Fig. E-6). The "tips" of the pilot should be exactly horizontal and level if the pilot phase is theoretically perfect. If the pilot phase has been tweaked to accommodate a particular exciter/RF amplifier/antenna system, then slight deviations from perfect flatness may be noted. Gross deviations imply a failure in the Phase-Locked Loop system (see paragraph **7.f** in **Appendix B** for troubleshooting hints).

Return the 8100A/1 CROSSTALK TEST switch to OPERATE.

b) Remote Control And Logic Verification

This procedure tests the operation of the rear-panel remote control terminals, and also verifies that the stereo generator switching logic is producing correct switching. To activate a remote control terminal, ground its "-" terminal to the "circuit ground" terminal on the rear-panel barrier strip, and momentarily jumper its "+" terminal to the "+22V" terminal on the barrier strip.

1) Connect the oscillator to the 8100A/1 right audio input. Switch the front-panel STEREO/MONO switch to STEREO. Verify that the front-panel STEREO light is lit, and that the stereo monitor indicates normal separation. Adjust the 8100A/1 PILOT INJECTION control as necessary to produce 9% pilot. Adjust the oscillator output level until the stereo monitor indicates 100% TOTAL MODULATION.

2) Switch the 8100A/1 into the MONO RIGHT mode by means of the rear-panel remote control terminal. Verify that the STEREO lamp on the front panel goes out, that the pilot disappears, and that the TOTAL MODULATION is 100% ±3%.

3) Disconnect the oscillator from the right channel input, and connect it to the left channel input. Verify that the TOTAL MODULATION reads 0%.

4) Switch the 8100A/1 into STEREO mode by means of the rear-panel remote control terminals. Verify that the front-panel STEREO lamp is on. Readjust the oscillator level as necessary to produce 100% TOTAL MODULATION.

5) Switch the 8100A/1 into MONO LEFT mode by means of the rear-panel remote control terminals. Verify that the STEREO lamp on the front panel goes out, and that the TOTAL MODULATION is 100% ±3%.

6) Disconnect the oscillator from the left channel input, and reconnect to the right channel input. Verify that the TOTAL MODULATION reads 0%.

c) Optional Performance Measurements Using Spectrum Analyzer

If a baseband spectrum analyzer like the Tektronix 5L4N is available, certain other stereo performance specifications can be readily verified.

Modulate the right channel to 100% at 5kHz (use the stereo monitor previously calibrated in step (a) to determine percent modulation). Observe the stereo generator output spectrum by bridging the spectrum analyzer input across the 8100A/1 baseband output. Expected spectrum components in the band from 50-53,000Hz are as follows:

1) 5kHz at 6.8dB below 100% modulation
2) 19kHz at 20.9dB below 100% modulation (for 9% injection)
3) 33kHz at 12.8dB below 100% modulation
4) 43kHz at 12.8dB below 100% modulation

All other components are spurious. Verify that the following conditions are met:

1) All spurious components between 50-53,000Hz should be better than 75dB below 100% modulation, with the exception of 38kHz. 38kHz should be better than 50dB below 100% modulation.

2) 76kHz should be better than 75dB below 100% modulation.

3) The sidebands of 76kHz (71 and 81kHz) should be better than 70dB below 100% modulation.

4) 114kHz and its sidebands should be better than 70dB below 100% modulation.

5) 152kHz and its sidebands should be better than 75dB below 100% modulation.

6) All other spurious should be better than 80dB below 100% modulation.

APPENDIX E:

Field Alignment Procedure and Specification

GENERAL

The following section describes how to align and calibrate OPTIMOD-FM Model 8100A/1 in the field. It is included primarily for purposes of reference, as routine alignment is neither necessary nor desirable due to the high stability of the circuitry.

WARNING!

THE AVERAGE RADIO STATION HAS NEITHER THE NECESSARY EXPERIENCE NOR THE REQUISITE TEST EQUIPMENT TO SUCCESSFULLY COMPLETE THIS PROCEDURE. IF CALIBRATION IS NECESSARY, WE STRONGLY RECOMMEND THAT THE CARD IN QUESTION BE RETURNED TO THE FACTORY FOR CALIBRATION BY OUR EXPERIENCED TECHNICIANS, WHO HAVE ACCESS TO SPECIAL TEST FIXTURES AND A SUPPLY OF EXACT-REPLACEMENT SPARE PARTS. ONLY IN AN EMERGENCY SITUATION SHOULD AN ATTEMPT BE MADE TO ALIGN AND CALIBRATE OPTIMOD-FM MODEL 8100A/1 IN THE FIELD.

The factory aligns each card independently to a standard, so that cards will be completely interchangeable. However, the user does not have access to the special test fixtures necessary to complete independent alignment of the cards. The user thus must use his own OPTIMOD-FM Model 8100A/1 chassis as a test fixture, and align the entire unit as a system.

This section is organized on a card-by-card basis. Cards should be calibrated in the same order as their order in the signal path, from input to output. This will occur naturally if the instructions in this section are followed in order from beginning to end. If a card later in the signal path is aligned while an earlier card is misaligned, the later card may not be correctly aligned, even if the instructions for that card are followed conscientiously.

Before commencing alignment, remove OPTIMOD-FM Model 8100A/1 from its normal rack mounting location and place it on the test bench away from RF fields. Jumper the chassis and circuit grounds together on the rear-panel barrier strip.

REQUIRED TEST EQUIPMENT

The following test equipment (or close equivalents) is required. It is assumed that the technician is thoroughly familiar with the operation of this equipment.

a) Digital Voltmeter, accurate to ±0.1%
b) Oscilloscope, dual-trace, triggered-sweep, with 5mHz or better vertical bandwidth
c) Ultra-Low Distortion Sinewave Oscillator/THD Test Set/AC VTVM (Sound Technology 1700B or 1710B)

The installation and servicing instructions in this manual are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the Operating Instructions unless you are qualified to do so. Refer all servicing to qualified personnel.

(per UL 813)

d) Low Frequency Spectrum Analyzer with Tracking Generator (Tektronix 5L4N plug-in with 5111 Bistable Storage Mainframe)
e) A 137K 1% resistor
f) A 243K 1% resistor
g) Six 6" alligator-to-alligator jumper leads
h) A 1uF ±20% film capacitor (voltage unimportant)

REFER TO THE FOLD-OUT SCHEMATICS AND PARTS LOCATOR IN **APPENDIX J.**

CARD #1 (POWER SUPPLY)

a) Measure the voltage across C111 (or other convenient point on the +15 volt bus) with the DVM. Adjust R106 until the DVM reads +15.00 volts.

b) Measure the voltage across C112 (or other convenient point on the -15 volt bus). Make sure that the voltage is between -14.85 and -15.15 volts. If it is not, refer to **Appendix B (CIRCUIT DESCRIPTION),** paragraph **8.c** for troubleshooting hints.

BEFORE ALIGNING EACH CARD AS DESCRIBED IN THE INSTRUCTIONS BELOW, REMOVE THE CARD OF INTEREST FROM ITS SLOT AND PLUG THE EXTENDER INTO THE EMPTY CARD SLOT. PLUG THE CARD INTO THE CARD EXTENDER. THIS WILL GIVE YOU ACCESS TO THE ALIGNMENT TRIMMERS AND TEST POINTS.

CARDS #3 and #4 (INPUT BUFFER/ INPUT CONDITIONING FILTER/ COMPRESSOR AUDIO PATH)

a) Remove Cards #3, #4 and #5 from their slots. Plug the extender board into the Card #3 slot. Cards #3 and #4 will both be aligned on this extender, one at a time, without moving it from the Card #3 slot.

b) Plug Card #3 into the extender board.

c) Connect one side of a 137K 1% resistor, and one side of a 243K 1% resistor to a convenient ground point (like the chassis) by means of jumper leads. Using two more jumper leads, connect the other side of the 137K resistor to the side of R333 away from IC305, and connect the other side of the 243K resistor to the side of R348 away from IC309. These external resistors now force reference gain-control currents into IC305A and IC309A respectively: 97uA into the "Master" VCA and 55uA into the "Bass" VCA.

d) Connect the chassis ground of the oscillator to the chassis of the 8100A/1. Connect the low side of the oscillator output to the chassis of the 8100A/1. Using a pair of jumper leads, connect the high side of the oscillator output to both the "+" input of IC301A and the "+" input of IC301B. This provides common-mode excitation for the input differential amplifier.

e) Set the oscillator frequency to 60Hz, and the oscillator output to 0 dBm. Observe TP1 (pin D at the card connector) with the AC VTVM adjusted so that the common-mode feedthrough is readily observed. Adjust R316 (CMRR) to null it. The nulled level of the 60Hz should be less than -60dBm.

f) Connect the low side of the oscillator output to the "-" terminal of the left-channel audio input of the 8100A/1. Connect the high side of the oscillator output to the "+" terminal. Set the oscillator output frequency to 5kHz and the oscillator output level to produce -15dBm at the output of IC302B (pin V of the card connector).

g) Observe the output of IC307A (pin K of the card connector) with the AC VTVM, and adjust R376 (MASTER VCA GAIN) to produce +2.0dBm at this point.

h) Readjust the oscillator frequency to 35Hz. If necessary, readjust the output level of the oscillator until it is identical to the oscillator output level produced at 5kHz.

i) Adjust R377 (BASS VCA GAIN) until the AC VTVM indicates +2.0dBm. The gains of both "Master" and "Bass" VCA's are now standardized, assuring card interchangeability.

NOTE: The following distortion and balance adjustments are made without disturbing the resistors jumpered into place in the steps above.

j) Without disturbing the oscillator output level, set its frequency to 5kHz. Switch the AC VTVM into its distortion-measuring mode, and measure the THD. Adjust R336 (MASTER DIST NULL) to null the THD. It should not exceed 0.04% if a noise-limiting 80kHz lowpass filter is employed in the measurement.

CAUTION!

Any stray audio picked up on the leads of the 137K jumper resistor will cross-multiply with the desired signal in the VCA, and will produce second-harmonic distortion which cannot be nulled with the MASTER DIST NULL control. It may be necessary to bypass the R333 side of the 137K resistor to ground with a tantalum capacitor larger than 5uF and 15VDC. Ground the "+" terminal of the capacitor.

k) Set the oscillator frequency to 50Hz. Measure the THD as above, and adjust R351 (BASS DIST NULL) to null it. It should not exceed 0.04%.

l) Remove the oscillator from the 8100A/1 input. Ground the low side of the oscillator output to the 8100A/1 chassis and, using a pair of jumper leads, connect the high side of the oscillator output through a 1uF film capacitor to the side of R333 away from IC305. (The 137K resistor is already connected to this point. Don't disturb it.) Set the output frequency of the oscillator to 100Hz, and its level to produce approximately 0.55V rms at its output. Observe the output of IC307A with the AC VTVM at high gain. You will see a distorted feedthrough component from the oscillator. Adjust R331 (MASTER VCA BALANCE) to null the feedthrough.

m) Move the lead from the 1uF capacitor from R333 to the corresponding side of R348. Do not disturb the resistor already connected to this point. Set the oscillator output to approximately 0.35V rms. Continue to observe the output of IC307A, and adjust R346 (BASS VCA BALANCE) to null the feedthrough component observed.

n) Remove all jumper leads connected to Card #3, and remove Card #3 from the extender.

o) Insert Card #4 in the extender (still in slot #3), and repeat steps **c - n.**

CARD #5 (COMPRESSOR CONTROL/ GATING DETECTOR)

IMPORTANT

Before embarking on this procedure, be sure that Cards #3 and #4 have been standardized according to the alignment procedure above, or are in their original factory-aligned condition.

a) Connect oscillator to the 8100A/1's left input, high side to "+", low side to "-".

b) Pull Card #3 halfway out and connect the AC VTVM to TP1. TP1 may be readily accessed at the end of R323 closest to the edge of the board.

Reinsert Card #3. Make sure that Card #4 is also in its slot. (If only one card is inserted, all gain control current will be diverted to the VCA's in that card, reducing the gain 6dB below its correct value.)

c) Extend Card #5 on the extender.

d) Set the oscillator frequency to 5kHz; set its output level to produce -15dBm at Card #3 TP1.

e) Switch the Compressor PROOF/OPERATE switch (on Card #5) to PROOF and allow the gain to settle for at least one minute.

f) While you are waiting, reconnect the AC VTVM to the output of IC307A on Card #3. This point can be readily accessed at the upper end of R364 by pulling the card halfway out, and reinserting it as above.

g) Adjust R501 (MASTER GAIN CAL) on Card #5 until +2.0dBm is observed on the AC VTVM.

h) Set the oscillator frequency to 35Hz. Be sure that the oscillator output level is the same as it was @5kHz.

i) Adjust R514 (BASS GAIN CAL) on Card #5 until the AC VTVM reads +2.0dBm.

j) Remove Card #5 from the extender, and restore Card #5 to its slot.

CARD #6 (PREEMPHASIS/ HF LIMITER)

This card serves both left and right channels. The procedure below is performed twice; once for the left channel and once for the right. When the reference designator of an alignment trimmer is specified, the reference designators for both left and right channel trimmers will be given in order, with the right in parentheses.

a) Extend Card #6. Place both PROOF/OPERATE switches in PROOF. Turn R626 and R660 (FET BIAS) fully clockwise to guarantee that the FET's in IC603 will be fully pinched-off.

b) Connect the output of the tracking generator in the 5L4N spectrum analyzer to the left (right) audio input of the 8100A/1.

c) The PREEMPHASIS trimmers are used to adjust the entire 8100A/1 for best conformance to the standard FM preemphasis. Place the rear-panel NORMAL/TEST slide switch in NORMAL. This connects the output of the audio processing to the rear-panel TEST JACKS. Now connect the TEST JACK corresponding to the channel which you are aligning to a precision 75us (or 50us) deemphasis network. Connect the output of the 75us deemphasis network to the input of the 5L4N spectrum analyzer.

(To make a 75us network, connect a 7.50K 1% metalfilm resistor between the input and output of the network. Then connect a 0.01mfd 1% capacitor between the output of the network and ground. This network should be loaded by no less than 1 megohm, or its accuracy will be degraded. To make a 50us network, use a 4.99K 1% metalfilm resistor instead of a 7.50K.)

d) Set the 5L4N for a 0-20kHz sweep (2kHz/div). Set its input sensitivity to -10dBV in dB mode. Set the vertical sensitivity to 2dB/division, and set the output level of the tracking generator to obtain an on-screen trace. (You may have to readjust the 8100A/1 INPUT ATTEN if gain is insufficient.)

e) You are now sweeping the entire 8100A/1 system, including the complex filters in Cards #8 and #9. Adjust R618(652) to achieve maximally flat response, similar to Fig. E-1. The response should be ±0.75dB or better, 50-15,000Hz.

Fig. E-1: Overall Deemphasized System Response

f) Now turn R626(660) (FET BIAS) slowly counterclockwise until the swept response just begins to roll off. Back off until no rolloff is observed, and go a little further for safety.

g) Repeat steps (d) through (f) for the right channel.

h) Connect the 8100A/1 input to the oscillator.

i) Observe the output of IC605A(611A) with the distortion meter. Set the oscillator frequency to 10kHz, and the oscillator level to produce +10dBm at the output of IC605A(611A).

j) Turn R678 (HF LIMIT THRESH--front-panel control) fully CW. Turn the LIMITER PROOF/OPERATE switch (on Card #6) to OPERATE. The 10kHz level should go down to approximately +6dBm. Now adjust R631(665) (DIST NULL) to minimize THD. Bear in mind that you are observing a preemphasized signal, and that THD will be even lower after deemphasis. Even without deemphasis, THD is typically less than 0.1%.

k) Repeat steps (i) and (j) for the right channel.

l) Observe the junction of R669 and R670 with a high-impedance (10 megohm or greater) DC DVM. Adjust R671 (OVERSHOOT COMPENSATION THRESHOLD) until the DVM reads +4.50VDC.

m) Return Card #6 to its slot.

CARD #8 and #9 (FM SMART CLIPPER/ FCS OVERSHOOT COMPENSATOR)

This procedure is performed twice -- once for Card #8, and once for Card #9. Only Card #8 will be referenced.

a) Extend Card #8.

b) Connect the oscillator to the left 8100A/1 input. Place both PROOF/OPERATE switches in PROOF. Connect the AC VTVM to the input of Card #8 (input side of R801). Set the oscillator frequency to 100Hz, and set the oscillator output level until -4.3dBm is observed on the VTVM.

c) Observe the left rear-panel TEST JACK with the AC VTVM with the rear-panel NORMAL/TEST switch in NORMAL. Adjust R841 (SAFETY CLIPPER THRESH) to produce 0dBm at the TEST JACK. This sets a standard gain of +4.3dB through the card.

d) **OPTIONAL PERFORMANCE VERIFICATION** Of Filters In FM Smart Clipper

1) Connect the output of the 5L4N tracking generator to TP1 of Card #8 (pin L on the card connector). Connect the input of the 5L4N to the left rear-panel TEST JACK. Observe the swept response with the 5L4N vertical span at 10dB/div, with 20-20kHz log frequency sweep. The swept response shows the response of the Smart Clipper to clipping-induced distortion components only. Note the high amount of rejection below 2.2kHz, and the very steep slope at 2.2kHz (see Fig. E-2).

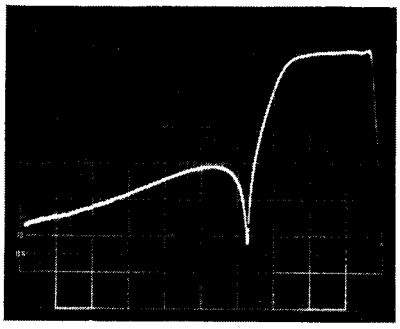

Fig. E-2: Distortion Cancellation Response

If this swept response does not resemble Fig. E-2, then there is a fault in either the filters or phase correctors between the card input and the output of IC803B. This test is both fast and sensitive because accurate cancellation demands accurate matching of the phase and amplitude responses of both the phase-corrected 15kHz lowpass filter and the distortion-cancelling filter. If any circuitry is faulty, then the cancellation will not occur accurately.

2) Measure the clipper bias voltages at the outputs of IC808A and IC808B. These should be approximately ±1.5VDC with no signal. (**NOTE:** The temperature-compensation circuitry will cause this bias voltage to change slightly with temperature to keep the clipping threshold constant.)

e) **OPTIONAL PERFORMANCE VERIFICATION** Of FCS Overshoot Corrector

1) Connect the oscillator to the junction of R806 and L801 (this provides a convenient injection point that bypasses the first clipper).

2) Place the LIMITER PROOF/OPERATE switch (on Card #6) in OPERATE.

3) Observe the left rear-panel TEST JACK with a scope. Set the oscillator frequency to 100Hz, and advance the oscillator output level until clipping just barely occurs. Measure the oscillator output, and verify that it is approximately 0.63V rms. (The "clipping" is the action of the overshoot corrector. If this clipping doesn't occur, then there is a fault in the overshoot corrector sidechain.)

4) Increase the oscillator output 4dB. Substantial clipping should occur. Now sweep the oscillator frequency upward, and verify that the peak level of the output waveform never exceeds the "flat-top" level of the 100Hz clipped sinewave by more than 0.7dB, and that this 0.7dB peak occurs at approximately 4.4kHz. At this frequency, the waveform should resemble a filtered square wave with two equal cycles of ringing on the top and bottom of the wave (Fig. E-3). If substantially more than 0.7dB overshoot occurs, particularly if the ringing is not symmetrical, then suspect problems in the filters or phase-shift networks associated with the FCS circuit.

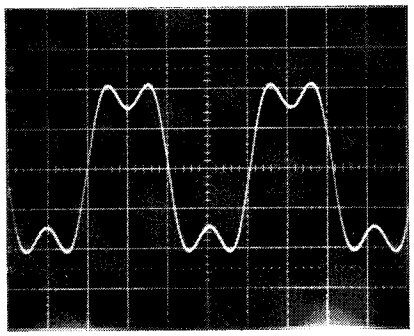

Fig. E-3: 5kHz Overdriven FCS Output

CARD #7 (STEREO GENERATOR)

The stereo generator circuitry is essentially independent of the preceding audio processing circuitry. This alignment procedure can therefore be performed regardless of whether the audio processing circuitry has been correctly aligned.

When the rear-panel NORMAL/TEST switch is in TEST, the two TEST JACKS on the rear panel can serve as audio inputs to the stereo generator. In order to assure correct operation of the stereo generator, these jacks must be driven by a source impedance of less than 10 ohms. This means that a standard 600-ohm audio oscillator cannot be employed without a buffer amplifier. Although such an amplifier can be easily built with a few IC opamps, it is more convenient in the field to use the final buffer amplifiers on the #8 and #9 Cards to provide the correct driving impedance, and to leave the NORMAL/TEST switch in NORMAL. You must also place the LIMITER PROOF/OPERATE switch (on Card #6) in PROOF.

The oscillator is readily interfaced to the cards by clipping an alligator-to-alligator jumper lead to the CR805, CR806 side of R840 (on Card #8), and doing the same to Card #9. These two jumper leads then serve as audio inputs to the stereo generator. Ordinarily, the connection will be made by temporarily removing the cards from their slots, clipping the jumpers on, and then replacing the cards in their slots. This way, they will not interfere with the extended #7 Card.

IMPORTANT

If the test procedure requires that only <u>one</u> channel be driven, <u>ground</u> the other jumper lead to avoid picking up crosstalk which could affect stereo generator adjustments.

WARNING!

IF THE ALIGNMENT CONTROLS ARE ADJUSTED IN THE ORDER SPECIFIED, NO INTERACTION BETWEEN ADJUSTMENTS WILL OCCUR. HOWEVER, IF ADJUSTMENTS ARE MADE IN RANDOM SEQUENCE, SEVERE INTERACTION CAN OCCUR, AND EARLIER ADJUSTMENTS MAY BE DESTROYED! TO AVOID TROUBLE, GO "BY THE BOOK".

a) Extend Card #7, and switch the pilot ON. Connect the input of the 5L4N spectrum analyzer to the 8100A/1 baseband output. Set the 5L4N input attenuator to -10dBV, and display in the 10dB/div log mode. The frequency sweep should be 0-100kHz linear. Set the 8100A/1 OUTPUT ATTEN until the 19kHz pilot reads -30dBV (two divisions from the top of the screen). Then switch the pilot OFF. (100% modulation is now indicated by signals reaching the top of the screen.)

b) **Modulator Distortion Null:** Place the stereo generator CROSSTALK TEST switch in OPERATE. Connect the oscillator to the right channel input (jumper lead from Card #9). Set the oscillator frequency to 5kHz, and advance the oscillator output level until the 38kHz sidebands read 12dB below the top of the screen. You will see several spurious components, including a second-harmonic distortion component at 10kHz, and subchannel second-harmonic components at 28 and 48kHz. Adjust R720 (DIST NULL) to minimize the amplitude of these components. It is ordinarily possible to get them below the bottom of the display (better than 80dB below 100% modulation).

c) **Low Frequency Sub-to-Main Crosstalk Null:** Place the CROSSTALK TEST switch in SUB-TO-MAIN. The 5kHz component you see on the spectrum analyzer is sub-to-main crosstalk. Adjust R717 (SUB:MAIN XTALK) to null the 5kHz as much as possible.

d) **15kHz Sub-to-Main Crosstalk Null:** Change the oscillator frequency to 15kHz. The crosstalk will ordinarily increase. Additional 15kHz crosstalk is nulled with a small piston trimmer capacitor across R712.

e) **76 kHz Null:** Return the CROSSTALK TEST switch to OPERATE. Set the oscillator frequency to 5kHz. Adjust R725 (76 KHZ NULL) to null the 76kHz component. Usually it is possible to get it below the bottom of the screen (better than -80dB below 100% modulation).

f) **76kHz Sideband Specification Verification:** Observe the sidebands ±5kHz about 76kHz, and verify that they are better than 70dB down (-75dB typical). If the sidebands do not meet specification, refer paragraph **7h** in **Appendix B** for troubleshooting hints.

g) **38kHz Null:** Adjust R714 (38 KHZ NULL) to null the 38kHz subcarrier. It is typically possible to achieve better than -70dB short-term suppression, and -60dB long-term suppression.

NOTE

Putting the CROSSTALK TEST switch in either TEST mode will compromise the 38kHz suppression somewhat (although it will never deteriorate above -40dB). Do not be disturbed if you observe this; in this alignment step, you have just nulled the 38kHz in normal operating mode as is correct.

h) **Main-to-Sub Crosstalk Null:** Place the CROSSTALK TEST switch in MAIN-TO-SUB. Adjust R709 (MAIN:SUB XTALK) to null the sidebands observed ±5kHz from 38kHz. Long-term suppression achievable exceeds 70dB.

i) **DC Offset Null:** Connect a DVM to the baseband output of 8100A/1, and observe the DC voltage. (You could also use a DC-coupled scope.) Temporarily suppress the audio oscillator output (or disconnect the oscillator and ground the jumper leads going to Cards #8 and #9.) Switch the CROSSTALK TEST switch to OPERATE, and be sure that the stereo generator is in STEREO mode (i.e., that the front-panel STEREO lamp is lit.) Now adjust R728 (DC OFFSET NULL) until the DC output voltage is 0V.

NOTE

The next part of the Alignment Procedure contains instructions for adjusting the User Controls for an "ideal" stereo output. At the time that the 8100A/1 is installed in a real system, these controls often are slightly readjusted from their "ideal" setting to compensate for variations in exciters, RF amplifiers, and antennas.

j) **Separation:** Connect the audio oscillator to the #8 Card jumper lead, and ground the #9 Card jumper lead as before. Connect the scope to the 8100A/1 baseband output through a wire or coax. DO NOT USE AN ATTENUATOR PROBE; these probes often have midband phase shift (due to slight imperfections in their frequency compensation circuitry) which will compromise the accuracy of the separation adjustment.

Trigger the scope externally from the oscillator. Adjust the scope sensitivity to 0.5V/div, and input coupling to "DC". Adjust the 8100A/1 OUTPUT ATTEN control for maximum output (fully CW). Set the oscillator frequency to 1kHz, and adjust the oscillator output level until the baseband output is 4V p-p.

Now adjust R772 (SEPARATION) to achieve the flattest possible baseline. Fig. E-4 shows the correct adjustment. To make the final adjustment accurately, expand the vertical scale by a factor of ten by changing the scope vertical sensitivity to 50mV/div.

To approximately measure the separation, use the formula: $S=20\log(D/4)$, where S is the separation in dB, and D is the peak-to-peak deviation of the baseline from perfect flatness, in volts. Ordinarily, the separation from 50-15,000 Hz will be essentially unmeasureable (better than -60dB).

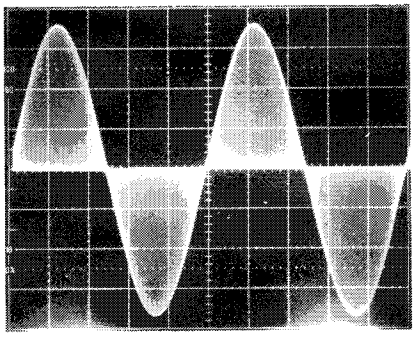

Fig. E-4: Separation

It is desirable to measure both right-into-left and left-into-right separation. If the earlier CROSSTALK adjustments were correctly performed, left-into-right and right-into-left separation should both null at the same setting of R772.

k) **Pilot Phase:** Connect the audio oscillator to the jumper lead going to Card #9, and ground the jumper lead going to Card #8. Place the CROSSTALK TEST switch in SUB-TO-MAIN. Adjust the oscillator frequency to a convenient frequency (non-critical) around 1kHz. Turn the pilot ON.

You will see a scope display similar to Fig. E-5. Expand the scope display by increasing the vertical sensitivity until it looks like Fig. E-6. Now adjust R769 (PILOT PHASE) until the "tips" of the pilot are exactly horizontal and level.

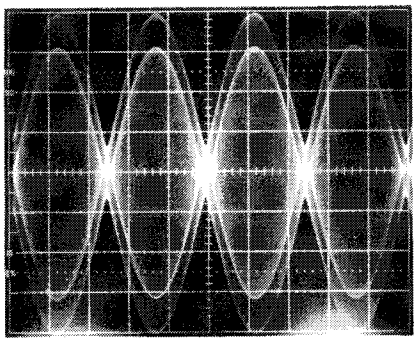

Fig. E-5: Pilot Phase

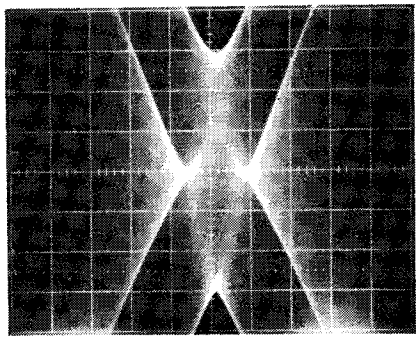

Fig. E-6: Pilot Phase, 10x

l) **Final 38kHz Suppression Check:** Remove the two jumper leads from Cards #8 and #9. Grounding and/or connecting the oscillator to these cards may have slightly affected the DC offset at the points to which the jumper leads were connected. Since the stereo generator is DC-coupled after these points, differential DC offset here translates as a DC-coupled L-R component (i.e., a constant 38kHz component). Now that offset conditions are entirely normal, turn the CROSSTALK TEST switch to OPERATE and adjust R714 (38KHZ NULL) if necessary to renull the 38kHz subcarrier.

m) Remove Card #7 from the extender, and reinstall Card #7 in its slot.

This concludes the Field Alignment Procedure for the entire 8100A/1 system. Insert the extender board in its slot, and replace the subpanel, being sure that all four Dzus fasteners are fully tightened for RF suppression. Close the front door, and fasten with its three screws. Remove the jumper between chassis and circuit grounds, unless it is ordinarily used in your installation.

OPTIMOD-FM Model 8100A/1 is now ready for reinstallation in the station.

l) **Final 38kHz Suppression Check:** Remove the two jumper leads from Cards #8 and #9. Grounding and/or connecting the oscillator to these cards may have slightly affected the DC offset at the points to which the jumper leads were connected. Since the stereo generator is DC-coupled after these points, differential DC offset here translates as a DC-coupled L-R component (i.e., a constant 38kHz component). Now that offset conditions are entirely normal, turn the CROSSTALK TEST switch to OPERATE and adjust R714 (38KHZ NULL) if necessary to renull the 38kHz subcarrier.

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