Section 6
Technical Data

page contents

6-2 Specifications

6-9 Circuit Description

6-9 Motherboard
6-10 Analog I/O Card
6-15 Stereo Encoder Card
6-19 DSP Cards
6-21 Control Card
6-23 Display Board
6-25 Power Supply
6-25 Input Filter Board
6-26 D-Connector Board

6-27 Parts List

6-28 Obtaining Spare Parts
6-44 Vendor Codes

6-45 Schematics, Assembly Drawings

6-81 Abbreviations

Specifications

It is impossible to characterize the listening quality of even the simplest limiter or compressor on the basis of the usual specifications, because such specifications cannot adequately describe the crucial dynamic processes that occur under program conditions. Therefore, the only way to meaningfully evaluate the sound of an audio processor is by subjective listening tests.

Certain specifications are presented here to assure the engineer that they are reasonable, to help plan the installation, and to help make certain comparisons with other processing equipment.

Performance

Specifications for measurements from analog left/right input to stereo composite output and to analog left/right output are as follows:

Frequency Response (All structures, measured below gain reduction and clipping thresholds, high-pass filter off): Follows standard 50µs or 75µs pre-emphasis curve ±0.20dB, 5Hz-15kHz. Analog left/right output can be user-configured for flat or pre-emphasized output.

Noise: Output noise floor will depend upon how much gain the processor is set for (LIMIT DRIVE, AGC DRIVE, TWO-BAND DRIVE, and/or MULTI-BAND DRIVE), gating level, equalization, noise reduction, etc. It is primarily governed by the dynamic range of the A/D Converter, which has a manufacturer-specified overload-to-noise ratio of 97dB. The dynamic range of the digital signal processing is 144dB.

Total System Distortion (De-Emphasized, 100% Modulation): <0.01% THD, 20Hz-1kHz rising to <.05% at 15kHz.<0.02% SMPTE IM Distortion.

Total System Separation: >65dB, 20Hz-15kHz; 70dB typical.

Polarity (PROTECTION, TWO-BAND PURIST or BYPASS Structure): Absolute polarity maintained. Positive-going signal on input will result in positive-going signal on output.

Installation

Analog Audio Input

Configuration: Left and right.

Impedance: 600Ω or 10kΩ load impedance, electronically balanced, jumper-selectable.

Common Mode Rejection: >70dB at 50-60Hz. >45dB at 60Hz-15kHz.

Sensitivity: –40dBu to +20dBu to produce 10dB gain reduction at 1kHz.

Maximum Input Level: +27dBu.

Connector: XLR-type, female, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 and 3 electronically balanced, floating and symmetrical.

Analog Audio Output

Configuration: Left and right. Flat or pre-emphasized.

Source Impedance: 30Ω, ±5%, electronically balanced and floating.

Load Impedance: 600Ω or greater, balanced or unbalanced. Termination not required.

Maximum Output Level: +23.7dBu into 600Ω or greater, balanced load.

Connector: XLR-type, male, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 and 3 electronically balanced, floating and symmetrical.

Digital Input and Output (Optional)

Configuration: Two-channel AES/EBU-standard.

Sampling rate: 32kHz (8200D/32) or 32kHz, 44.1kHz, and 48kHz (8200D/SRC).

Connector: XLR-type, female, EMI-suppressed. Pin 1 Chassis Ground, Pins 2 and 3 transformer balanced and floating.

SCA Subcarrier Input

Configuration: Subcarrier input sums into composite baseband outputs.

Input Impedance: 600Ω.

Sensitivity: 1.0Vp-p for 10% modulation of main carrier.

Connector: BNC, floating over chassis ground. EMI-suppressed.

Composite Baseband Outputs

Configuration: Two (2) outputs, each with independent OUTPUT level control, output amplifier and connector.

Source Impedance: 0Ω voltage source or 75Ω (jumper-selectable), single ended, floating over chassis ground.

Load Impedance: 37Ω or greater. Termination not required.

Level (0Ω Source Impedance, 75Ω or higher Load Impedance): Adjustable 0-8Vp-p with multi-turn OUTPUT LEVEL control.

Connector: BNC, floating over chassis ground. EMI-suppressed.

Maximum Recommended Cable Length (0Ω Source Impedance): 100ft/30m RG-58A/U. Maximum permitted load capacitance 0.047μF.

Pilot Reference Output

Configuration: Buffered square-wave reference for RDS or other subcarrier services.

Source: HCMOS logic level output, 0-5V peak.

Connector: On Remote Control Interface. DB-25, EMI-suppressed.

Remote Computer Interface

Configuration: RS-232 and RS-422 interfaces to connect to IBM PC-compatible computers, directly or via modem, for remote control and metering.

Minimum Hardware: 386 computer or compatible with hard disk drive, 4MB RAM, VGA grayscale or color display, DOS 3.3 or higher, Micosoft® Windows™ 3.1 or higher, and Hayes-compatible modem (2400 baud rate, V.42bis data compression).

Optimum Hardware: Pentium® or 486 computer with hard disk drive, 8MB RAM, VGA color display, DOS 5.0 or later, Micosoft® Windows™ 3.1 or later, and Hayes-compatible modem (9600 baud rate, V.42bis data compression).

Connector — RS-232: DB-9, EMI-suppressed.

Connector — RS-422: DB-9, EMI-suppressed.

Remote Control Interface

Configuration: Eight (8) analog or digital inputs. User-programmable to select any eight of: user presets, factory presets, stereo, mono left, mono right, SC1 modulation reduction, SC2 modulation reduction, TX1 overshoot modulation reduction, TX2 overshoot modulation reduction, clock reset, EBS tone, exit test, input analog, input digital.

Voltage: 6-24VAC or DC, momentary or continuous, optically-isolated. Current-Limited 12VDC provided to facilitate use with contact closure.

Connector: DB-25, EMI-suppressed.

Power

Requirements: Switch-selectable on the rear panel, 90-130VAC or 180-260VAC, 50-60Hz; 55VA.

Connector: IEC; detachable 3-wire power cord supplied. AC is EMI-suppressed.

Ground: Circuit ground is independent of chassis ground; can be isolated or connected with a rear panel switch.

Safety Standards: IEC65, UL, CSA.

Dimensions

Dimensions (WxHxD): 19in/48.3cm wide, 7in/17.8cm high, 15in/38.1cm deep. 4 rack units.

Environmental

Operating Temperature Range: 32-122°F/0-50°C

Humidity: 0-95% RH, non-condensing.

Setup and Operation

Help Features

HELP Button: Available at all times. Push HELP, and a message will tell you what you are looking at on the screen, what can be done and how to do it. Press each button and the message will tell you the function of that button.

System Setup (I/O CALIB)

Function: Initial setup.

Controls: Studio chassis yes/no (defeats AGC), Pre-emphasis 50µs or 75µs, meter select VU or PPM, analog input clip level, analog input reference level, analog input balance, analog outputs flat or pre-emphasized, analog output level, input meters indicate ref/clip, modulation type, pilot on/off, clock sync to AC line/crystal, reduction of modulation for SC1 ON, reduction of modulation for SC2 ON, reduction of modulation for OSHOOT TX1 ON, reduction of modulation for OSHOOT TX2 ON; if Digital I/O is present: input A or D, digital input ref level.

Quick Setup

Function: Guided screen-by-screen setup for all required setup adjustments.

On-Screen Metering

Metering can be switched to indicate gain reduction (G/R) or input/output levels (I/O).

Gain reduction (G/R): Shows gain reduction of AGC, compressors, high-frequency limiters, and gate on/off, as appropriate to the programmable processing structure selected.

Input/Output (I/O): Left input (dB), right input (dB), left output (dB), right output (dB), composite output (% modulation).

Pilot: 7.5-10%, in 0.5% steps.

Preset Programming

Function: Save processing settings for recall from the front panel, by remote control, by remote computer or by Automatic Preset Switching.

Number of User Presets: 32.

Test Presets

BYPASS preset: No processing; audio is digitized and low-pass filtered only. Adjustable gain (–18 to +15dB).

TONE Preset: Frequency programmable 30Hz-15kHz. Level programmable 0-121% total modulation. Modulation type (L,R, L+R, L–R, MONO L, MONO R), Pilot ON/OFF.

Automatic Preset Switching

Function: Changes presets on a programmed event schedule.

Programming: Date (specific date, time, function) or daily (specific day or days of the week, time, function).

Events: Up to 99 events.

Pascode Security

Function: To prevent unauthorized adjustment of controls by persons without pascodes.

Number of Pascodes: 10.

Access: Each Pascode can be programmed to permit or deny access via front panel or computer to RECALL PRESET, RECALL TEST PRESETS, MODIFY PROCESSING, OBSERVE METERS and PRESET NAMES, PROGRAM AUTOMATION (Automatic Preset Switching), PROGRAM SYSTEM SETUP and PROGRAM SET PASCODE.

Remote Control with Orban 8200PC Remote Control Software

Metering: Same as On-Screen Metering, above.

Control: All user-adjustable processing parameters, Preset functions and System Setup.

Circuit Characteristics

Analog-To-Digital Converter

(A/D Converter subject to change as technology improves.)

Device: Analog Devices AD1879.

Performance: >97dB dynamic range (overload-to-noise ratio).

Digital Signal Processing

Device: Motorola DSP56001.

Performance: 24-bit processing. 144dB internal dynamic range.

Digital Input Conditioning

Subsonic Filter: Switchable in/out third-order Chebychev with 30Hz cutoff and 0.5dB passband ripple; −0.5dB @ 30Hz, −10.5dB @ 20Hz, −31.5dB @10Hz.

Time Dispersion Network: All-pass network to make speech more symmetrical to reduce processing distortion. (Normal Two-Band and Multi-Band structures only.)

Digital Output Conditioning

Passband Response: Typically +0, −0.26dB to 15kHz.

Stopband Rejection (Referenced to 100% Modulation): To reduce spectrum in stereo composite baseband above 57kHz to <−75dB.

Digital-To-Analog Converter

Device: Analog Devices AD1864.

Performance: 18-bit. 4X oversampled output. Linear-phase reconstruction filters.

Pilot

Frequency: 19kHz.

Stability: ±0.005%. See “Ultrastable Pilot” on page 1-9.

Injection: Adjustable, 7.5-10%.

Stereo Baseband Encoder

(Test signals applied to analog inputs of stereo baseband encoder.)

Noise (De-Emphasized, Referenced to 100% Modulation): <–100dB, 20Hz-15kHz.

Distortion (De-Emphasized, 100% Modulation): <0.006% THD, 20Hz-15kHz; <0.010% SMPTE Intermodulation Distortion.

Stereo Separation: >65dB, 20Hz-15kHz; 70dB typical.

Crosstalk — Linear (Referenced to 100% Modulation): <–80dB, main channel to subchannel or subchannel to main channel.

Crosstalk — Non-linear (referenced to 100% modulation): <–80dB, main channel to subchannel or subchannel to main channel.

38kHz Subcarrier Suppression (Referenced to 100% Modulation): >70dB; 75dB typical.

76kHz and Sideband Suppression (Referenced to 100% Modulation): >70dB.

CIT25 Composite Isolation Transformer

Ground loops are a problem in some transmitter plants. A ground loop among OPTIMOD-FM and one or more exciters may occur, causing an increase in hum and noise. This is especially likely when OPTIMOD-FM is installed some distance from the exciter.

The Composite Isolation Transformer provides the solution. Designed to be installed adjacent to each exciter, it provides ground isolation between the OPTIMOD-FM composite output and the exciter, and presents OPTIMOD-FM with a balanced floating load.

Performance

Frequency Response: +0.01, –0.03dB, 30Hz-53kHz.

Group Delay: Deviation from linear phase <±0.3°, 30Hz-53kHz.

Separation: >50dB, 50Hz-15kHz.

Gain: Adjustable from full attenuation to 0dB.

Installation

Location

Location : As close to FM exciter as practical.

Interconnect Between OPTIMOD-FM and Transformer

Interface at OPTIMOD-FM: Adapter cable, BNC male to 3-pin XLR-type male cable connector supplied.

Cable: Two-conductor foil-shielded audio cable, Belden 8451 or equivalent. Maximum length 100ft/30m, user-supplied. 3-pin XLR-type male and female cable connectors supplied.

Composite Baseband Input

Connector: 3-pin XLR-type female. Pin 1 capacitively-coupled to chassis ground, Pins 2 and 3 transformer balanced, floating and symmetrical.

Maximum Level: 4Vp-p.

Composite Baseband Output

Connector: BNC, shell insulated from chassis ground.

Interconnect Between Transformer and Exciter

Maximum Recommended Cable Length: 6ft/1.8m RG-58A/U cable or similar, to avoid excessive RF pick-up on cable. 2ft/.6m cable supplied.

Exciter Input: 1kΩ or greater; 1000pF or less. Replace 50Ω or 75Ω termination resistor, if present, with 1kΩ resistor, supplied.

Dimensions

Dimension: 7in/17.8cm wide, 3in/7.6cm high, 1.72in/4.4cm deep.

Warranty

One Year, Parts and Labor: Subject to the limitations set forth in Orban's Standard Warranty Agreement.

Specifications subject to change without notice.

Circuit Description

This section provides a detailed description of each circuit used in the 8200. It starts with an overview of the 8200 system, identifying all the circuit boards and describing their purpose. Then each board is treated in detail by first giving an overview of the circuits followed by a component-by-component description.

1. Overview

The 8200 has 9 types of circuit boards: Mother, Analog I/O, Stereo Encoder, DSP (digital signal processing), Control, Display, Power Supply, Input Filter and D-Connector.

The block diagram on page 6-46 illustrates the following overview of 8200 circuit boards.

The Motherboard contains no active circuitry and serves only to connect all the other boards together properly.

The Analog I/O Card provides the circuitry to interface the analog audio inputs and outputs to the digital processing.

The Stereo Encoder Card generates the composite output signal.

The DSP Cards implement the audio processing using digital signal processing. The 8200 has slots for four DSP Cards. The base unit is shipped with two DSP Cards. The Multi-Band structure requires a third board. A fourth slot is provided for future options.

The Control Card administrates control of the 8200 system.

The Display Board provides circuitry for the LCD display, push buttons, front panel knobs.

The Power Supply Board provides power for all 8200 boards.

The Input Filter Board provides the connectors and RF filtering for the left and right audio inputs and outputs, the digital audio input and output, the two composite outputs, and the SCA input.

The D-Connector Board provides the connectors, RF filtering, and circuitry for the remote control inputs, RS-232 interface, and RS-422 interface.

Motherboard

The Motherboard is used to connect all parts of the 8200 system together. Only connectors are mounted to it. It is a four layer board with nearly all signal traces on the outer two layers. The inner layers contain ground and power connections.

Under no circumstances should you try to replace any components on this board. Soldering or desoldering can permanently damage the inner layers and ruin the board.

Analog I/O Card

1. Overview

The Analog I/O Card provides the circuitry to interface analog audio to and from the DSP Cards. The input buffer scales the input audio level to match it to the audio processor. The analog-to-digital (A/D) converter converts the analog input audio to digital audio. The digital audio is transmitted to the DSP Cards. The DSP Cards transmit the processed digital audio output back to the Analog I/O Card. The digital output audio is converted to an analog signal by the digital-to-analog (D/A) converter. The low-pass reconstruction filters remove high frequency images from the D/A converter output and feed the output buffer. The output buffer is made up of a programmable gain amplifier, a programmable time constant de-emphasis filter, and a balanced output buffer. The board also provides logic circuitry to generate the system sample rate clocks and interface the board to the Control Card and DSP Cards.

2. Input Buffer

The signal enters the input buffer in balanced form. It comes from the Input Filter Board via the Motherboard. The signal is applied to a resistor load and a resistor pad. The pad and the load are enabled or disabled by jumpers that are positioned by hand. The loaded and padded signal is applied to a balanced amplifier that has an adjustable gain. The gain is set by FET transistors and analog switches. The state of the FETs and switches is set by the outputs of a latch. The Control Card controls the gain according to what the user specifies from the front panel controls by writing data to the latch. The balanced amplifier output feeds a servoed buffer which feeds an RC low-pass filter applying the signal to the analog-to-digital converter.

Component-level description:

The balanced audio input signal is applied to the pad and load network made up of R200, R203, R204 and R205-7. JA is a jumper that removes or inserts a 600Ω termination load on the input signal. JB is a jumper that removes or inserts a resistive divider that pads the input signal before being applied to IC15, a balanced amplifier. R215-222, FETs Q202-203, and IC14, a quad analog switch, make up the circuit that sets gain of IC15. The FETs are used as switches along with IC14 to change the resistive paths in the circuit. The state of the FET switches is set by the outputs of IC19, a digital latch. The latch outputs feed IC7, a quad comparator, which outputs 0V to turn on a FET and −15V to turn off a FET. The Control Card writes data directly to IC14 to control the state of the switches on IC14. IC8 and IC9 buffer and gain-scale the signal prior to its application to the A to D converter.

3. Analog-to-Digital Converter (A/D)

The A/D is a single chip, stereo, 18-bit sigma-delta type converter. The A/D oversamples the audio at 2.048MHz. It applies noise shaping, then it filters and decimates to a 32kHz sample rate. The samples are output in twos complement format and transmitted to the DSP Cards.

Component-level description:

The right analog input is applied to pin 13. Pin 26 is a 8.192MHz clock input used by the chip to oversample the input. Pins 3 and 25 place the A/D in its slave mode allowing it to rum form an external bit and L/R clock. Pin 27 is the serial data output. Both the left and right samples are multiplexed on to it and synchronized to the 2.048MHz clock. The left sample starts on the rising edge of the L/R clock.

4. Digital-to-Analog Converter

The D/A is a single chip, stereo, 18-bit resistor ladder type. It has two synchronous serial inputs that receive the left and right audio samples from the DSP Cards. A NAND gate outputs a signal to clock the data in. A 128kHz clock signal controls the timing of when the output switches between analog sample output voltages.

Component-level description:

IC39 is the digital-to-analog converter. Pins 15 and 10 are the left and right serial data inputs from the DSP Cards. Pin 12 is a gated 6.75MHz clock input from the DSP Cards that clocks in the serial data. Pins 11 and 14 receive a 128kHz clock input. Pins 17 and 8 are the left and right voltage outputs. The voltages change to the current sample value on the falling edge of the 128kHz clock. A full scale output is approximately 3.0 Volts peak. IC40 is a NAND gate that processes the bit clock and word clock supplied by the DSP Cards.

5. Reconstruction filter

The reconstruction filter is a 5th order elliptic filter with 90dB stopband attenuation at 113kHz. It filters the ultrasonic energy "images" present at the D/A output. There are two filters, one each for the left and right signals.

Component-level description:

The reconstruction filter is an active RC analog of a passive LC ladder filter, realized by resistors, capacitors, and frequency-dependent negative resistors (FDNRs). An FDNR is realized with a dual opamp, three resistors, and two capacitors. When the passive LC filter is transformed into an active RC filter, inductors become resistors, resistors become capacitors, and capacitors become FDNRs.

Each FDNR resonates with a series resistor to create a notch in the frequency response of the filter. This is analogous to a series LC circuit to ground. The notches are located in the "stopband" (beyond 15kHz).

The frequency response of the filter CANNOT be measured by applying a swept sine wave at the 8200 analog inputs. This is because the filter has bandwidth much larger than the analog-to-digital converter. The analog-to-digital converter band limits the input to 16kHz. To test the filter response, see step 3, page 4-23.

6. Output Buffer

The output buffer buffers the output of the reconstruction filters in three stages. The first stage of the output buffer is an inverting amplifier with gain programmable by the Control Card. The second stage is a programmable de-emphasis filter. The de-emphasis response is controlled by JFET switches. The third stage is a balanced floating line amplifier. It has a 30Ω, ±5% output impedance.

Component-level description:

The first stage is a programmable gain inverting amplifier formed by R170, R171, C132, IC12 and IC5a. IC12 is an 8-bit MDAC, which is a resistor ladder with a programmable resistance. The Control Card writes an eight-bit word to the chip which has a latch on board to store the value and set the resistance. The resistance determines the gain. The output at pin 1, IC5a feeds the second stage, a programmable de-emphasis filter. It is formed by IC5b, Q102, Q103, and the associated resistors and capacitors. Q103 and Q102 are JFET transistors used to switch C127 or C126 in or out of the circuit. If none of the JFETs are on, the circuit is a unity-gain inverting amplifier. With capacitor C127 in circuit, it becomes a first-order low-pass filter with a 75µs time constant. With capacitor C126 in circuit, it becomes a first-order low-pass filter with a 50µs time constant. The fourth stage is a balanced floating line amplifier formed by IC6 and IC13. The 412 opamp used in the balanced output module is a low-offset servo amplifier which centers the average DC level at the (+) and (–) outputs of the module around ground. The floating characteristic is achieved by complex cross-coupled positive and negative feedback between two 5532 opamps, and its operation is not readily explainable except by a detailed mathematical analysis. Opamps may be replaced; resistors are specially matched and should not be replaced.

7. Logic Circuitry

The Control Card reads and writes data from and to the Analog I/O Card. The control logic section decodes the address lines and enables the proper latch to be read from or written to.

Component-level description:

IC37 compares the slot address hard-wired into the Motherboard with the address lines A8-11. If the address lines match the slot address, IC37, pin 6 is asserted and partially enables the address decoder IC28. The address bits A3-5 feed IC28 to select one of eight output signals to assert low. The eight outputs are used to select various devices that the Control Card reads from and writes to. The output buffer MDACs and the input buffer's analog switches and latch require further decoding to be selected. This is accomplished by IC27, a three-to-eight decoder.

8. Clock logic

A crystal oscillator provides the timing reference for all signals related to the system sample rate. Divider circuitry produces the various signals used by the system. Logic is used to gate the sample rate clocks and serial input data. A latch provides for the control of a variety of functions.

A crystal oscillator circuit generates an 8.192MHz clock that provides the reference for all signals related to the sample rate of the system. The 8.192MHz is first divided by two to 4.096MHz. The 4.096MHz signal feeds the A/D, which divides that by two and produces a 2.048MHz clock. The 2.048MHz clock is divided further to generate the 128kHz, 64kHz, and 32kHz signals. Those signals are inverted to make the signals 128kHz and 64kHz. The signals 32kHz, 64kHz, and 128kHz are gated and buffered to make the signals 1 x frameclock, 2 x frameclock, and 4 x frameclock. These signals are gated "on" at the rising edge of the 128kHz signal just prior to the falling edge of the 32kHz signal. This is necessary because any one of these signals can be used by the DSP Cards to generate interrupts on a falling edge and the first interrupt must occur simultaneously with all DSP chips. The 64kHz signal is also gated to make the signal IFRAME. IFRAME marks the start of sample words transmitted from the A/D to the DSP Cards. It is gated "on" so that two words of data are transmitted to the DSP Cards before they start processing.

Component-level description:

Y1, IC33a, and IC33b make up an 8.192MHz square wave oscillator. IC35a divides it to 4.096MHz. The A/D chip, IC20, divides it by two to 2.048MHz which feeds IC34. IC34, IC32, and IC31 are set up as dividers and produce clock signals down to the sample rate, 32kHz. IC41 and IC42a are used to create two control signals that drive IC43, a quad "AND" gate. The "AND" gates act as switches for signals that drive the DSP Cards. IC36 is a 74HC244 buffer that connects the sample rate clocks and the serial input data to the DSP Cards. The buffer is enabled by bit 2 of latch IC30. The Control Card writes to this latch and clears the bit if it selects the Analog I/O Card as the source of sample rate clocks and input data. IC30 also provides control of other circuits. Bit 1 is set high to start a DSP algorithm. Bit 3 is set high to select a 50µs de-emphasis. Bit 4 is set high to select a 75µs de-emphasis. Bit 7 is set high to select J.17 de-emphasis. Bit 8 is set high to calibrate the A/D chip.

Stereo Encoder Card

1. Overview

The 8200 Stereo Encoder Card combines the left and right processed audio signals into one composite signal. A single composite signal is needed to feed an external FM exciter for FM broadcast.

The composite signal is made up of four elements. The first two are the main channel and the subchannel. The main channel is the L+R baseband signal. The subchannel is the L–R signal, double-sideband suppressed-carrier modulated with a 38kHz subcarrier frequency. The third is the pilot tone. It is a 19kHz sine wave in phase with the 38kHz subcarrier. The fourth is the optional SCA subcarrier which must be generated externally with an SCA generator and connected to the 8200's SCA input.

> There may be more than one SCA subcarrier in the frequency range of 57 to 100kHz in the baseband. For example, there might be a 57kHz subcarrier for digital paging or RDS, a 67kHz subcarrier, and 92kHz subcarrier.

The main channel, the subchannel, the pilot tone, and the SCA are added to form the composite signal. Two output buffers with separate level controls provides two composite outputs.

The subchannel would ideally be produced by an ideal multiplier circuit that multiplies the L–R signal by a 38kHz sine wave. The 8200's Hadamard-Transform Stereo Baseband Encoder closely approximates an ideal multiplier by a switching technique. The L–R signal is passed through two analog switches whose outputs are summed together. These switches are turned on and off by pulse trains produced by a Read Only Memory (ROM). The ROM controls the switches so that all harmonics of 38kHz prior to the 7th harmonic are cancelled. By comparison to a conventional switching modulator, performance requirements of the output low-pass filter (to remove harmonics above 98kHz) are greatly eased, and excellent separation and spurious rejection can be obtained from a relatively modest filter.

The stereo pilot tone is generated by multiplying a DC voltage by three individual pulse trains from the ROM with three analog switches. Harmonics up to the 14th are cancelled. The resulting waveform is passed through the same low-pass filter as the stereo subchannel, ensuring correct phasing between the pilot tone and stereo subcarrier. JFET switches driven by CMOS logic are controlled by the Control Card. The switches alter the circuitry to facilitate stereo/mono mode switching and to provide the two "test" modes, main-channel-to-subchannel crosstalk and subchannel-to-main-channel crosstalk.

2. Stereo Modulator

The L and R signals are applied to a differential amplifier, which produces the L–R signal. The L–R signal is applied to a buffer amplifier. This amplifier has a DC servo that eliminates virtually all the DC offset that might have accumulated in earlier circuitry. (DC offset must be eliminated because it otherwise translates into loss of subcarrier suppression after modulation.) The L–R buffer output is applied to two analog switches, which modulate the L–R signal by the subcarrier.

The L and R signals are summed together to form the L+R signal. The L+R signal is summed with the L–R signal and servoed. This servo forces the DC at the outputs of the analog switches to be equal to zero, further reducing any subcarrier leakage. A separation control adjusts the amplitude of the L+R signal, permitting the L+R and L–R to be mixed with equal gains, thus maximizing separation.

The analog switches effectively multiply their inputs by +1 or 0, depending on whether the switches are on or off. Thus, the L–R signal is multiplied not only by the subcarrier, but also by an average DC voltage. Therefore, a substantial undesired baseband L–R component appears at the output of the analog switches. This is cancelled by mixing L–R that is out-of-phase into the output of the switches. The sub-to-main crosstalk trimmer maximizes cancellation.

Equal (+) and (–) DC voltages are applied in parallel to three pairs of analog switches to generate the pilot tone. The amplitude of the pilot tone is determined by the DC voltage level. The pilot tone is turned off by reducing the DC voltage to zero.

High order harmonics generated in the switching process are eliminated by a fifth-order passive elliptic filter followed by a group delay corrector. The corrector group delay is adjusted with the 15kHz separation trimmer to maximize overall separation. Separation of 70dB is theoretically possible with this filter design.

The filter output is applied to two power buffers each capable of driving two 75Ω loads in parallel. The external SCA input is mixed into these buffers.

Component-level description:

The L and R signals are applied to differential amplifier IC1a. This produces the L–R signal which is buffered by IC1b. IC3a is a DC servo to remove DC offsets. CR1 and CR2 are clamping diodes to protect the analog switch IC10 from being driven beyond its ±5V range. In mono mode the switching signals S0 and S1 stay at 0V and thereby turn off the subchannel.

IC8a and IC8b provide (+) and (–) reference voltages for the pilot tone generator. These voltages are applied to analog switches within IC11 and IC12. When mono mode is selected, the “PILOTEN” signal at R48 changes from +5VDC to 0V and the pilot reference voltage is reduced to 0V. The pilot switching waveforms P0, P1, P2, and P3 applied to IC11 and IC12 are also removed in mono mode. The L and R signals are summed by inverting amplifier IC2a. The JFET Q9 is “on” in stereo mode and the amplifier has unity gain. In mono mode, Q9 turns off and the

amplifier gain increases by 6.9dB to use modulation headroom otherwise used by the subchannel and the pilot. JFETs Q2 and Q3 select the left or right signal as the source in mono mode. The output of IC2a is summed with the L–R signal by inverting amplifier IC2b. R37 adjusts the L+R gain to maximize separation. R35 adjusts the gain of the L–R signal to minimize sub-to-main crosstalk. IC4a is a DC servo that prevents DC from appearing at the outputs of analog switches IC10, IC11, and IC12.

L1, L2, C6-C11, and C25 form a passive fifth-order elliptic filter with a cutoff frequency of approximately 70kHz. This is buffered by non-inverting amplifier IC5 and applied to all-pass group-delay corrector IC6.

The stereo modulator output and externally generated SCA signal are summed into two separate output buffers. The first is made up by IC15 and IC16. IC16 is a special high slew rate power buffer which is located within the overall amplifier feedback loop. It isolates IC15 from the destabilizing effects of capacitive loads and also permits 75Ω loads to be driven without degradation. This line driver will drive up to 1.5V peak into 0.047μF in parallel with 37.5Ω before significant nonlinear errors (increases in spurious components as observed on a baseband spectrum analyzer) or linear errors (noticeable deterioration of baseline flatness at 15kHz in the separation test mode) are apparent. Output level is adjusted by varying the feedback resistor R66. The second output buffer made by IC26 and IC27 is functionally identical to the one just described.

3. Switching Waveform Generator

A crystal oscillator generates a clock signal that is divided to a lower frequency, which drives a counter. The counter addresses a Read Only Memory (ROM). The ROM's data outputs drive the analog switches synchronized to the subcarrier.

Component-level description:

Y1, IC24a, and IC24b form a 4.864MHz square wave oscillator. IC23a and IC23b divide this clock down to 1.216MHz which drives IC22, a dual binary counter. The four least significant bits of the counter output form an address for ROM IC31. The address counts from 0000B to 1111B and is then reset back to 0000B to repeat the process. The counter only provides half the word that addresses the ROM. The other four are provided by half the outputs of IC17, a latch. The Control Card writes to this latch. The four bits address different blocks of the ROM and control whether the pilot and subcarrier are on. IC18 (a latch) buffers the ROM data output and ensures that the signals appearing at the output are changing state in precise synchronism with the clock edges. This ensures high spectral purity of the subcarrier and pilot tone.

4. Mode Switching Logic

The 8200 Stereo Encoder operates in several modes. These modes are changed by altering the circuitry with a mechanical switch and various JFET switches. The microprocessor operating system sets the mode based upon three things: the state of the mechanical switch, the remote control interface status, and selections made by the user through the operating system. The 8200 Stereo Encoder has a manual switch that switches between three operating modes: operate, sub-to-main crosstalk, and main-to-sub crosstalk. The two latter are used only when making stereo performance verification measurements. When in the "operate" mode, there are three sub-modes possible: stereo, mono left, or mono right. These are changed by the remote control interface or by the user's selecting the sub-mode from the front panel operating system. Table 1 shows the state of each JFET switch in the system under all the operating modes and sub-modes.

Component-level description:

Switch S1a switches the right input to the sum and difference amplifiers IC1a and IC2a. The other half of the switch, S1b, switches one pole to 0V and leaves the other two poles to be pulled up to +5V. The Control Card reads the state of these three signals through the buffer IC21. That way, the Control Card knows which mode the user is selecting and can control the JFET switches properly. The Control Card sets the JFET switches by writing to latch IC17. The logic level outputs of IC17 drive the comparators on IC13 and IC14. The comparators' outputs are 0V or −15V to turn the JFET switches on or off, respectively. A +5V signal output from IC17 makes the comparator output −15V and thus turns the JFET switch off.

Table 1: JFET Switch States (Under Operating Modes and Sub-Modes)

		LFET	RFET	LGAIN	SUM FET	STM FET	DIF FET
OPERATE	STEREO	ON	ON	ON	ON	ON	ON
	MONO L	ON	OFF	ON	OFF	ON	OFF
	MONO R	OFF	ON	ON	OFF	ON	OFF
SUB-TO-MAIN		OFF	OFF	OFF	ON	OFF	ON
MAIN-TO-SUB		ON	ON	ON	ON	ON	ON

5. Composite Metering

The composite signal prior to the output buffers is applied to a peak detector circuit. Its output feeds an 8-bit analog-to-digital converter which measures the signal level. The Control Card reads the level value from the analog-to-digital converter and translates the data to the front panel LCD display.

Component-level description:

IC32 is an 8-bit analog-to-digital converter. R133, C92, and CR20 create a 1.2V reference used by IC32 to determine the input level seen at pin 16. IC32 has eight data outputs that are connected to the Control Card. The outputs are normally tri-stated and are enabled by the signal at pin 2.

DSP Cards

1. Overview

The DSP Cards use general purpose DSP chips that use software programs to implement digital signal processing algorithms. The algorithms filter, compress, and limit the audio signal. Each board has three DSP chips on it. Each DSP chip has two FIFO buffer circuits associated with it: one for transmitting data to another DSP chip, the other for receiving data from another DSP chip. The DSP chips are cascaded with the FIFO circuits between them to interface the DSP chips. The DSP chips are cascaded so that the first generates output to the second which generates output to the third. The first receives input from the third DSP chip on a separate DSP Card. The third DSP chip generates output to the first DSP chip on a separate DSP Card. The DSP chip communication is through a FIFO interface. The FIFO is 24 bits wide and 16 words deep. The FIFO is dual ported so that reads and writes can occur simultaneously. The control logic interfaces the DSP chips and the interrupt logic with the Control Card. The Control Card reads from and writes to the DSP chips through the DSP chip host ports. The board has two latches on it that the Control Card writes to. The latch output bits are used to reset the DSP chips and to control how the DSP chips are synchronized to the sample rate clocks.

Component-level description:

IC9, IC15, and IC30 are the DSP chips. The chips can be ruined by static discharge or by damage to their delicate pins.

2. FIFO Buffers

A FIFO buffer is used by a DSP chip to write data to another DSP chip. There are three FIFO buffers on a DSP Card. Each FIFO buffer is paired with a DSP chip. The FIFO/DSP pairs are cascaded in a line. The first FIFO is written to by a DSP chip on a previous DSP Card, if there is one. The first DSP chip reads from the first FIFO and writes to the second FIFO. The second DSP chip reads from the second FIFO and writes to the third FIFO. The third DSP chip reads from the third FIFO and writes to the first FIFO on the next DSP Card, if there is one. A FIFO buffer is made up of three 74HC373 latches and six 74HC40105 4X16 FIFOs. The 74HC373s latch the data from the DSP chip writing to the FIFO buffer. The 74HC373 outputs are shifted into the 74HC40105 FIFO chips. The DSP chip that reads from the buffer reads the data from the 74HC40105 FIFO chips and shifts it out.

3. Control Logic

The control logic decodes the address lines and selects the proper device for the Control Card to read from or write to.

Component-level description:

IC45 is an address magnitude comparator used to decode the board address. It compares the address bits A8-11 with the slot address from the Motherboard. If they match, the comparator output, pin 6, partially enables IC42, a 74HC138 3-to-8 line address decoder. It decodes the address bits A3-5 to select one of three DSP chips or one of two latches. IC42 is fully enabled when the Control Card asserts the E signal high at pin 6. When that happens, one of its eight outputs goes low and provides a control signal to the device being addressed.

4. DSP Reset and Interrupt Logic

The Control Card writes to two latches on the DSP Card that reset the DSP chips and control four multiplexers. The multiplexers select which of three signals is connected to the IRQB pin on each DSP chip. The IRQB pin is an interrupt request pin that is negative edge-triggered. When the DSP chip detects an interrupt, it runs its algorithm on the current audio sample. The multiplexers are necessary because the algorithms are designed to run at one of three rates: 32kHz, 64kHz, or 128kHz.

Component-level description:

IC44 is the reset control latch. It is a 74HC373 transparent latch. It is written to by the Control Card to initiate hardware resets on the DSP chips. Only the four least significant bits are used. When IC4 is not being written to, its outputs are tri-stated and pulled high by the pull-up resistors R2–5. Three of the outputs are connected to the reset pin on each DSP chip which is active low.

When the Control Card writes to the reset latch, IC44, the outputs are briefly enabled and the DSP chips will be reset if the Control Card has written a low logic level. The outputs of IC44 also connect to inverters on IC41. The inverted signals connect to pin 1 on IC36, 37, 38 and 40. If the Control Card resets the DSP chips, pin 1 on IC36, 37, 38 and 40 goes high and tri-states pin 7 on IC36, 37, 38 and 40. This is necessary to make the DSP chips boot properly. The purpose of IC36, 37, 38 and 40 is described below. The three signals 1 x frameclock, 2 x frameclock, and 4 x frameclock are 32kHz, 64kHz, and 128kHz clock signals respectively. ICs 36, 37, 38 and 40 are 74HC253B multiplexers that select which of the three frameclock signals interrupt each DSP chip. IC43 is a 74HC373 latch that supplies four pairs of logic signals to address the multiplexers. The address signals are applied to pins 14 and 2 of the 74HC253B. The selected input is output at pin 7. IC36's output is not connected to anything and is a spare IC.

Control Card

1. Overview

The Control Card processes and executes all user initiated requests to the system. This includes changes to the DSP processing such as program change and modifications through the front panel keyboard, the serial port, and the eight remote contact closures. The Control Card also provides the housekeeping functions like the real time clock, gain reduction and input/output metering, analog signal path setup levels, and security password functions.

2. Power Monitoring Circuit

The +5 volt supply voltage is monitored to ensure it is within the correct operating range.

The system $\overline{\text{RESET}}$ is activated if the +5V supply drops below the minimum acceptable voltage. Battery voltage is also monitored to ensure it is above its minimum operating voltage.

Component-level description:

Voltage comparator IC11 provides the system reset function. The 5-volt source is divided by resistors R202 and 203 and compared to the 1.2V voltage reference created by R204 and CR200. When the 5V line is above the 4.8V minimum operating voltage, timing network R210 and C207 will begin to charge to 5V. Inverters IC13c and IC13d buffer the signal and $\overline{\text{RESET}}$ goes high, enabling the Z180 $\overline{\text{RESET}}$ input.

Battery voltage is buffered by IC11a with stabilizing network R208 and C206, divided by R209 and R211, and compared to the 1.2V reference by IC11b. The output of IC11b goes low when the battery voltage falls below 2.4V. This signal

is read periodically by the Z180 through buffer IC12 to detect acceptable battery voltage.

CR201 and CR202 switch the Vbat line between 5V and battery 3V to retain real time clock and RAM data retention during mains voltage outages.

Security Reset Switch is debounced by R216 and C208 and buffered by IC13e.

This signal is read periodically by the Z180 through buffer IC12 to detect if security should be disabled.

3. Microprocessor and Input/Output Circuit

A Z-180 microprocessor runs the software required to provide the functions described above. Crystal Y100 connected to the XTAL port of the Z180 oscillates at 12.288MHz and is internally divided down to 6.144MHz to provide the system clock frequency.

Module M1 contains control software for the Z180. IC15 and IC9 decode Z180 memory addresses to select M1 to access instructions to execute. User presets and system setup information are stored in both RAM IC22 and the module to enable board swapping without losing data.

IC10 decodes I/O addresses to select real time clock circuitry, host port buffers IC19, IC26, and IC20, remote contact closures, ROM.

4. Real Time Clock Circuit

IC1 with crystal oscillator Y101 provides time, date and alarm functions. Vbat is used for supply voltage to allow continued operation when AC mains power is removed. The Z180 accesses IC1 with decoder IC10 and timing circuitry IC3, IC4, IC6, and IC8. IC2 is a data buffer and IC14 is an address latch between the Z180 and IC1. Pin 8 of IC3 goes low for read and pin 11 of IC3 goes low for write operations. A Z180 interrupt is generated by IC1 every 0.5 second with pin 19 going low. The Z180 will then read the current data from IC1. Pin 22 of IC1 and R108 with C102 is held high by Vbat. This port will go low and is then internally latched should Vbat go low, interrupting timing updates.

5. Host Port Interface

The Z180 communicates to the Analog I/O, Stereo Encoder, and the DSP Cards through the host port. IC19, IC26, and IC20 buffer the address and data bus with control signals HOST, E, RD, and WR. The host port can be selected as a standard I/O mapped device with pin 14 of IC10.

The Z180 sends the signal processing software required by the DSP Cards through the host port. IC10 pin 9 selects buffers IC19, IC26, and IC20 and address generating components IC5, IC6, IC7, and IC8. The address generating circuit modifies the port address and allows speedier memory transfers for DSP function changes like recalling a different processing structure.

Display Board

1. Overview

The Display Board supports the front panel keys, LCD display, and rotary encoder. The keys are configured in a switch matrix circuit controlled by the Control Card. The LCD display has its own special purpose driver IC, RAM, and address and data buffers and support circuitry. The rotary encoder circuit includes filtering components, a pulse counter and buffers.

2. Switch Matrix

The switch matrix is configured as two columns and six rows. Decoder IC15 selects latch IC16 to drive one of the two columns low. Decoder IC15 then selects buffer IC17 which reads the six rows to determine if one or more of the switches in that column are closed. If no switches are closed, pull-up resistors R204D-R204I drive the buffer inputs to +5 volts. The HELP key has a dedicated row so that it can be read in combination with any other key.

3. Rotary Encoder

The rotary encoder provides two pulsed outputs when it is rotated. The outputs are out of phase so that direction can be determined. The Z180 on the Control Card reads the switch circuitry approximately every 4 milliseconds to check if any switches or the rotary encoder have been turned.

Component-level description:

IC9a and IC9b buffer and invert the rotary encoder outputs. Flip-flop IC8a is clocked and the output goes low to indicate the encoder has been turned. IC9c, IC9d, IC9e, and IC9f with associated resistors and capacitors provide filtering so that the directional phase information can be determined. The output of IC8b will go high if the encoder is turned to clockwise and will go low if turned counter-clockwise. The output is read by buffer IC17. Pulse counter IC19 counts how far the encoder was turned. IC19s output is buffered by IC18.

4. Display circuit

The LCD display uses a special purpose display driver to interface to the LCD and to refresh the display data. The Z180 microprocessor on the Control Card writes display data to a static RAM on the Display Board. The display driver IC uses this data to refresh and update the LCD. Data and address latches allow the Z180 and the display driver to access the current display data.

Component-level description:

Display driver IC4 uses crystal Y100 to generate its clock frequency. IC4 is selected by the Control Card with signal DISPLAY. IC4 is initialized on power-up. All updates to the LCD are done through RAM IC3 with data and address latches IC1, IC2, IC13, and IC14. IC11c, IC11d, and IC10a decode the READ, WRITE, and MDISPLAY signals to determine if the Control Card is requesting a read or write operation. Asynchronous RAM access between the Control Card and LCD driver IC4 is accommodated with logic circuitry IC5, IC6, IC7, IC11, and IC12.

5. LCD display

The LCD is a 128-by-256-dot graphics display incorporating a florescent backlight. Screen saver circuitry for the backlight helps extend its lifetime. The backlight's voltage source is a 300V 30kHz AC signal and requires caution to avoid user injury. All components described below other than the LCD unit reside on the Display Board.

Component-level description:

The LCDs power and control signals connect to the Display Board with a 14-pin connector. The LCD unit consists of the display and an integral control circuit board containing the driver circuitry for each screen element. The output of the front panel CONTRAST control provides the LCD operating voltage of approximately −8 volts. Adjusting this voltage will change the optimum viewing angle of the LCD. The backlight's power is generated by power inverter A100. The inverter's +12 volt power source is switched on or off with Q100, R100, and R101 by bit 7Q of latch IC16. Diode CR100 protects transistor Q100 against reverse bias voltages.

Power Supply

The power supply converts an AC line voltage input to various power sources used by the 8200. It consists of three main parts: the Regulator Board, the Finger Board, and the Switching Power Supply. The Regulator Board circuitry supplies power to the 8200 analog circuits. The Finger Board is used to connect the power signals to the Motherboard. The switching power supply supplies power to the 8200 digital circuits. Other than a full replacement, the switching power supply is not intended to be serviced.

Component-level description:

L1 is a power line filter that filters out RFI. T1 is a conventional power transformer used to step down the input voltage for the ±15VDC supply. S2 is a switch used to select between a 115V or 230V power source. CR1 is a full wave rectifier. C1, C2, C5, and C6 smooth and condition the rectified voltage signal for input to the voltage regulators, IC1 and IC2. The regulators output the +15V and −15V sources used to power the analog circuits in the 8200.

The Finger Board holds the test points and bypass capacitors before connecting the power signals to the Motherboard.

Input Filter Board

The Input Filter Board serves as a mount for the audio input and output connectors, the AES/EBU connectors, the composite outputs and the SCA input. It provides RFI filtering for all the above inputs and outputs.

D-Connector Board

The D-Connector Board holds the connectors and circuitry for the RS-232, RS-422, and remote control interfaces.

Component-level description:

The RS-232 interface is comprised of J1, IC1, and IC2. J1 is a 9-pin D-connector. IC1 and IC2 provide logic circuitry to interface the RS-232 signals with the microprocessor on the Control Card.

The RS-422 interface consists of J2, IC3, IC4 and associated resistors. J2 is a 9-pin D-connector. IC3 and IC4 provide logic circuitry to interface the RS-422 signals with the microprocessor on the Control Card.

J3 is a 25-pin D-connector that connects the remote control input signals. The associated resistors and capacitors filter out RFI from the input signals. The associated optoisolators (e.g. IC12) isolate the inputs from the detector circuitry on the Control Card. The associated diodes prevent the optoisolators from breaking down under a reverse bias.

S1 is the ground lift switch used to connect or lift circuit ground from chassis ground.

Parts List

Parts are listed by ASSEMBLY, then by TYPE, then by REFERENCE DESIGNATOR. Widely used common parts are not listed; such parts are described generally below (examine the part to determine exact value). See the following assembly drawings for locations of components.

SIGNAL DIODES, if not listed by reference designator in the following parts list, are:

Orban part number 22101-000, Fairchild (FSC) part number 1N4148, also available from many other vendors. This is a silicon, small-signal diode with ultra-fast recovery and high conductance. It may be replaced with 1N914 (BAY-61 in Europe).

(BV: 75V min. @ Ir = 5μA; Ir: 25nA max. @ Vr = 20V; Vf: 1.0V max. @ If = 100mA; trr: 4ns max.) See Miscellaneous list for ZENER DIODES (reference designator VRxx).

RESISTORS should only be replaced with the same style and with the exact value marked on the resistor body. If the value marking is not legible, consult the schematic or the factory. Performance and stability will be compromised if you do not use exact replacements.

Unless listed by reference designator in the following parts list, you can verify resistors by their physical appearance:

Metal film resistors have conformally-coated bodies, and are identified by five color bands or a printed value. They are rated at ⅛ watt @ 70°C, ±1%, with a temperature coefficient of 100 PPM/°C. Orban part numbers 20038-xxx through 20045-xxx, USA Military Specification MIL-R-10509 Style RN55D. Manufactured by R-Ohm (CRB-1/4FX), TRW/IRC, Beyschlag, Dale, Corning, and Matsushita.

Carbon film resistors have conformally-coated bodies, and are identified by four color bands. They are rated at ¼ watt @ 70°C, ±5%. Orban part numbers 20001-xxx, Manufactured by R-Ohm (R-25), Piher, Beyschlag, Dale, Phillips, Spectrol, and Matsushita.

Carbon composition resistors have molded phenolic bodies, and are identified by four color bands. The 0.090 x 0.250 inch (2.3 x 6.4 mm) size is rated at ¼ watt, and the 0.140 x 0.375 inch (3.6 x 9.5 mm) size is rated at ½ watt, both ±5% t numbers 2001x-xxx, USA Military Specification MIL-R-11 Style RC-07 (¼ watt) or RC-20 (½ watt). Manufactured by Allen-Bradley, TRW/IRC, and Matsushita.

Cermet trimmer resistors have ⅜-inch (9 mm) square bodies, and are identified by printing on their sides. They are rated at ½ watt @ 70°C, = ±10%, with a temperature coefficient of 100 PPM/°C. Orban part numbers 20510-xxx and 20511-xxx. Manufactured by Beckman (72P, 68W- series), Spectrol, and Matsushita.

Obtaining Spare Parts

Special or subtle characteristics of certain components are exploited to produce an elegant design at a reasonable cost. It is therefore unwise to make substitutions for listed parts. Consult the factory if the listing of a part includes the note “selected” or “realignment required.”

Orban normally maintains an inventory of tested, exact replacement parts that can be supplied quickly at nominal cost. Standardized spare parts kits are also available. When ordering parts from the factory, please have available the following information about the parts you want:

Orban part number
Reference designator (e.g., C3, R78, IC14)
Brief description of part
Model, serial, and “M” (if any) number of unit — see rear-panel label

To facilitate future maintenance, parts for this unit have been chosen from the catalogs of well-known manufacturers whenever possible. Most of these manufacturers have extensive worldwide distribution and may be contacted through their local offices. Addresses for each manufacturer’s USA headquarters are given on page 6-44.

ANALOG BOARD ASSEMBLY

Capacitors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
C98,99	Ceramic,Disc, 1KV, 10%; 12pF	21112-012	MEP	120K20S2L		
C100-102	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C103-107	Met. Polyester, 63V, 5%; 0.1uF	21442-410	MAL	168104J63A	WIM	
C108,109	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C110	Met. Polyester, 63V, 5%; 0.1uF	21442-410	MAL	168104J63A	WIM	
C111-113	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C114	Mica, 500V, 1%; 2400pF	21022-224	CD	CD19-FD242F03	SAN	
C115-118	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C119,120	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C121	Mica, 500V, 1%; 2400pF	21022-224	CD	CD19-FD242F03	SAN	
C122	Mica, 500V, 1%; 1500pF	21022-215	CD	CD19-FD152F03	SAN	
C123	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN	
C124,125	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C126	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN	
C127	Mica, 500V, 1%; 1500pF	21022-215	CD	CD19-FD152F03	SAN	
C128,129	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C130,131	Met. Polyester, 63V, 5%; 0.1uF	21442-410	MAL	168104J63A	WIM	
C132,133	Mica, 500V, +1/2pF -1/2pF; 33pF	21017-033	CD	CD15-CD330D03	SAN	
C134,135	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C136,137	Met. Polyester, 100V, 10%; 0.0056uF	21441-256	WES	160C 562K630	SIE,WIM	
C200,201	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C202,203	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C213	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C216	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C217,218	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C220	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C224-227	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C300-303	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C304	Met. Polyester, 100V, 10%; 0.01uF	21441-310	WES	160C 103K630	SIE,WIM	
C305,306	Mica, 500V +1/2pF -1/2pF; 39pF	21017-039	CD	CD15-CD390D03	SAN	
C307,308	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C400	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C401	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Capacitors (continued)						
C402	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C403-408	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C410-412	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C413	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C414	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C415,416	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C596-601	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C617	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C801	Polypropylene, 50V, 2.5%; 100pF	21702-110	NOB	CQ15P1H101GPP	WES,WIM	
C804-806	Polypropylene, 50V, 2.5%; 100pF	21702-110	NOB	CQ15P1H101GPP	WES,WIM	
C807-810	Ceramic, 100V, 5%; .01uF	21125-310	MUR	RPE113C0G103J110V	KEM	
C811,812	Tantalum, 20V, 10%; 10uF	21305-610	SPR	196D 106X9020JA1	MANY	
C813,814	Ceramic, 50V, 5%; 4700pF	21124-247	CRL	CN30C472J245	KEM	
C815	Tantalum, 20V, 10%; 10uF	21305-610	SPR	196D 106X9020JA1	MANY	
C817-820	Tantalum, 20V, 10%; 10uF	21305-610	SPR	196D 106X9020JA1	MANY	
C821,822	Ceramic Disc, 25V, 20%; 0.01uF	21106-310	CRL	UK25-103	MUR, SPR	
Diodes						
CR400,401	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
Integrated Circuits						
IC1	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC2	Quad SPST Switches	24728-302	AD	ADG222		
IC3	Audio Preamp	24727-302	AD	SSM-2017		
IC4,5	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC6	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC7	Quad Comparator	24710-302	NAT	LM339		
IC8,9	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC10	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC11,12	Digital, Multiplying DAC	24714-302	AD	AD7524JN		
IC13	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC14	Quad SPST Switches	24728-302	AD	ADG222		
IC15	Audio Preamp	24727-302	AD	SSM-2017		
IC16,17	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Integrated Circuits (continued)						
IC18	Quad Comparator	24710-302	NAT	LM339		
IC19	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC20	Digital, A/D Converter	24730-000	AD	AD1879		
IC21	D.C. Regulator, 5V Negative	24308-901	NAT	LM79M05C	TI,MOT	
IC22	D.C. Regulator, 5V Positive	24307-901	NAT	LM78M05C	TI,MOT	
IC23	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC24-26	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC27,28	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
IC29	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC30	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC31,32	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC33	Digital, Hex Inverter	24572-302	NAT	74HC04N	TI	
IC34,35	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC36	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC37	Digital, Magnitude Comparator	24574-302	SIG	74HC85N	TI	
IC38	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC39	Digital, Audio DAC	24824-302	AD	AD1864		
IC40	Digital, NAND Gate	24585-000	RCA	CD74HC132E	TI	
IC41,42	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC43	Digital, AND Gate	24576-302	RCA	CD74HC08		
IC44	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
Miscellaneous						
Y1	Crystal; 8.192 MHz	28052-001	NEL	NE-18-8.192MHz		
Resistors						
R109a,b	Resistor Set, MF; 2.00K	28520-002	ORB			3
R111a,b	Resistor Set, MF; 2.00K	28520-002	ORB			3
R126a,b	Resistor Set, MF; 2.00K	28520-002	ORB			3
R128a,b	Resistor Set, MF; 2.00K	28520-002	ORB			3
R136a,b	Resistor Set, MF; 13.3K/10.2K	28522-003	ORB			3
R139a,b	Resistor Set, MF; 4.64K/4.53K	28522-005	ORB			3
R146a,b	Resistor Set, MF; 13.3K/10.2K	28522-003	ORB			3
R148a,b	Resistor Set, MF; 4.53K/3.01K	28522-004	ORB			3

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Resistor (continued)						
R153a,b	Resistor Set, MF; 13.3K/10.2K	28522-003	ORB			3
R156a,b	Resistor Set, MF; 4.64K/4.53K	28522-005	ORB			3
R163a,b	Resistor Set, MF; 13.3K/10.2K	28522-003	ORB			3
R165a,b	Resistor Set, MF; 4.53K/3.01K	28522-004	ORB			3
Transistors						
Q100-105	Transistor, JFET/N	23406-101	NAT	J113	SIL	
Q200-203	Transistor, JFET/N	23402-101	NAT	J108		
Q400-402	Transistor, Signal, PNP	23002-101	MOT	2N4402	FSC	
CONTROL BOARD ASSEMBLY						
Capacitors						
C100,101	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
C102,103	Mica, 500V, 1%; 100pF	21018-110	CD	CD15-FD101F03	SAN	
C200-202	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C203-205	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C206	Alum., Radial, 50V, -20% +100%; 47uF	21208-647	SPR	502D 476G050CD1C	PAN	
C207	Alum., Radial, 63V, -20% +100%; 2.2uF	21209-522	SPR	502D 225G063BB1C	PAN	
C208	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C209	Alum., Radial, 63V, -20% +100%; 2.2uF	21209-522	SPR	502D 225G063BB1C	PAN	
C210	Ceramic Disc, 25V, 20%; 0.1uF	21106-410	CRL	UK25-104	MUR	
C211-214	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C300-311	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C313	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C316,317	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR200	Diode, Voltage Reference	22081-112	NAT	LM385	MOT	
CR201,202	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800	MANY	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Integrated Circuits						
IC1	Digital, RAM, RTA	24809-302	MOT	MC146818A		
IC2	Digital, Tranceiver	24570-302	NAT	MM74HC245N	TI	
IC3	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC4	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC5	Digital, Binary Counter	24583-302	RCA	CD74HC393		
IC6	Digital, Hex Inverter	24572-302	NAT	74HC04N	TI	
IC7	Digital, AND Gate	24576-302	RCA	CD74HC08		
IC8	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC9,10	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
IC11	Quad Comparator	24710-302	NAT	LM339		
IC12	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC13	Digital, Schmitt Trigger Inverter	24582-302	MOT	74HC14A		
IC14	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC15	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
IC16	Digital, Hex Inverter	24572-302	NAT	74HC04N	TI	
IC17	Digital, Schmitt Trigger Inverter	24582-302	MOT	74HC14A		
IC18	Digital, MPU	24813-302	ZI	Z8018006PSC		
IC19	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC20	Digital, Tranceiver	24570-302	NAT	MM74HC245N	TI	
IC22	Digital, RAM	24811-302	TOS	TC5565APL15L		
IC25,26	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
Miscellaneous						
None	Battery Holder, Coin Cell	28031-000	KEY	106		
B200	Coin Cell, Lithium; 3V	28041-000	DUR	DL2032	GE	
Y100	Crystal; 12.288 MHz	28055-000	RAL	A-12.288-5		
Y101	Oscillator; 32.768 KHz	28056-000	NEL	HS426-32.768MHz		
Resistors						
R100,101	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
R105-107	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
R200	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
R215	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Switches					
S1	Switch, MOM.; SPST	26302-001	SCH	D6-01-01		
D-CONNECTOR BOARD ASSEMBLY						
	Capacitors					
C1-16	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C17	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C18,19	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C20	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C21,22	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C23	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C24,25	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
	Diodes					
CR1-8	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
	Inductors					
L1	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50		(2)
	Integrated Circuits					
IC1	Digital, Quad Line Driver	24661-302	NAT	DS14C88N		
IC2	Digital, Quad Line Receiver	24662-302	NAT	DS14C89A		
IC3	Digital, Quad Line Drivers	24717-302	MOT	SN75174N		
IC4	Digital, Quad Line Receivers	24718-302	MOT	SN75175N		
IC5-12	Optoisolator, NPN	25003-000	SIE	SFH-601-1		
	Miscellaneous					
FB1-18	Ferrite Bead, with wire	29506-001	FR	2743001111		
	Switches					
S1	Switch, Slide; SPDT	26142-000	ITW	124-230-020		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
DSP BOARD ASSEMBLY						
Capacitors						
C1,2	Alum., Radial, 63V, -20% +100%; 22uF	21209-622	SPR	502D 226G063CC1C	PAN	
C3-40	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Integrated Circuits						
IC1	Digital, NOR Gate	24581-302	SIG	74HC02N	TI	
IC2	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC3	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC4-6	Digital, Register	24578-302	SIG	74HC40105N		
IC7	Digital, NOR Gate	24581-302	SIG	74HC02N	TI	
IC8	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC9	Digital, DSP	24835-000	MOT	DSP56001FC27		
IC10,11	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC12-14	Digital, Register	24578-302	SIG	74HC40105N		
IC15	Digital, DSP	24835-000	MOT	DSP56001FC27		
IC16	Digital, NOR Gate	24581-302	SIG	74HC02N	TI	
IC17	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC18-20	Digital, Register	24578-302	SIG	74HC40105N		
IC21	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC22-24	Digital, Register	24578-302	SIG	74HC40105N		
IC25	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC26-28	Digital, Register	24578-302	SIG	74HC40105N		
IC29	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC30	Digital, DSP	24835-000	MOT	DSP56001FC27		
IC31-33	Digital, Register	24578-302	SIG	74HC40105N		
IC34,35	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC36-38	Digital, Multiplexer	24579-302	SIG	74HC253BN	TI	
IC39	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC40	Digital, Multiplexer	24579-302	SIG	74HC253BN	TI	
IC41	Digital, Hex Inverter	24572-302	NAT	74HC04N	TI	
IC42	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
IC43,44	Digital, Latch	24577-302	SIG	74HC373N	TI	
IC45	Digital, Magnitude Comparator	24574-302	SIG	74HC85N	TI	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Miscellaneous					
Y1	Oscillator; 27 MHz	28054-000	NEL	HS-350-27.000		
FINGER BOARD ASSEMBLY						
	Capacitors					
C12	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C13	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C14	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C15	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C16	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C17	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C18	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C19	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C20	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C21	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C22	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C23	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C26	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C27	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C28	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C29	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C30	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C31	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
C32	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C33	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
FRONT PANEL ASSEMBLY						
Miscellaneous						
	LCD Display	42025-000	ORB			
INPUT FILTER BOARD ASSEMBLY						
Capacitors						
C2-5	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
Inductors						
L1-4	Inductor, RF Choke; 1.2mH	29503-000	MIL	73F123AF		
L5-13	Inductor, RF Choke; 7uH	29501-004	OHM	Z-50		(2)
L14-21	Filter, EMI, W/INDUCT, 50V,470PF	29509-147	TAI	LC471M1RO		
L22-25	Filter, EMI, W/BEAD, 50V,1000PF	29508-210	TAI	STB102KB		
Miscellaneous						
FB1	Ferrite Bead, with wire	29506-001	FR	2743001111		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
MAIN DISPLAY BOARD ASSEMBLY						
Capacitors						
C100,101	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
C200,201	Mica, 500V, 1%; 270pF	21018-127	CD	CD15-FD271F03	SAN	
C300-302	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C303-327	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR100	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
Integrated Circuits						
IC1,2	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC3	Digital, RAM	24811-302	TOS	TC5565APL15L		
IC4	Digital, LCD Controller	24723-000	OKI	MSM62556GS		
IC5	Digital, Schmitt Trigger Inverter	24582-302	MOT	74HC14A		
IC6-8	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC9	Digital, Schmitt Trigger Inverter	24582-302	MOT	74HC14A		
IC10	Digital, AND Gate	24576-302	RCA	CD74HC08		
IC11	Digital, Quad OR Gate	24571-302	NAT	MM74HC32N	TI	
IC12	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC13,14	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC15	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
IC16	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC17,18	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC19	Digital, Binary Counter	24583-302	RCA	CD74HC393		
IC20	Digital, Quad 2-Input NAND	24559-302	RCA	74HCT132E	TI	
Miscellaneous						
Y100	Crystal; 4.9152 MHz	28051-003	MID	C1700		
Modules						
A100	Digital, Inverter, DC to AC	24722-000	TDK	CXAM10L		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Resistors					
R104	Pot, Single; 500 OHM (5050)	20747-000	ORB			Linear
R204	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
	Transistors					
Q100	Transistor, Power, NPN; TO-220	23604-201	TI	TIP122	RCA	
MISCELLANEOUS						
	Miscellaneous					
	Extender Card 48/48	31510-002				
	Line Cord, CEE	28102-002	BEL	17500	MANY	
POWER SUPPLY CHASSIS						
	Integrated Circuits					
IC1	D.C. Regulator, 15V Positive	24304-901	NAT	LM78M15UC	TI,MOT	
IC2	D.C. Regulator, 15V Negative	24303-901	NAT	LM79M15AUC	TI,MOT	

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REGULATOR BOARD ASSEMBLY

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Capacitors						
C1	Alum., Axial, 40V, -10% +100%; 1000uF	21224-810	SIE	B41010-1000-40	PAN	
C2	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C3	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C4	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C5	Alum., Axial, 40V, -10% +100%; 1000uF	21224-810	SIE	B41010-1000-40	PAN	
C6	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C7	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S		
C8	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR1	Diode, Bridge, 200V, 1A	22301-000	VARO	VE-27	GI	
CR2,3	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
Inductors						
L1	Filter, Line	28012-000	DEL	03ME1		
Miscellaneous						
F1	Fuse, 3AG, Slo-Blo, 1/2A	28004-150	LFE	313.500	BUS	Domestic
F1	Fuse, Type T, 1/4A	28025-125	LFE	218.250		European
F2	Fuse, 3AG, Slo-Blo, 4A	28004-240	LFE	313.004		Domestic
F2	Fuse, Type T, 2A	28025-220	LFE	218.002		European
F3,4	Fuse, Type T, 1/2A	28025-150	LFE	218.500		European
PS1	Switcher, Power Supply	42026-000	ORB			
T1	Transformer, Power; 51VCT	55015-000	ORB			
V1	Varistor; 430V	22500-431	PAN	ERZ-C10DK431		
Resistors						
R1-3	Resistor, 1/4W; 0 OHM (Jumper)	20020-025	ROHM	JPW-02A		
Switches						
S1	Switch, Push-Push; DPST	26118-000	SCH	NE18-2AEESP		
S2	Switch, Slide, Mains voltage selector	26143-000	SW	EPS2-PC3		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

STEREO GENERATOR BOARD ASSEMBLY

Capacitors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)
C1	Mica, 500V, +1/2pF -1/2pF; 5pF	21017-005	CD	CD15-CD050D03	SAN
C2,3	Ceramic, Trim.; 0.5pF-3pF	21811-000	ME	2502AOR503V	
C5	Met. Polyester, 100V, 10%; 0.22uF	21441-422	WES	160D224K100	SIE
C6	Mica, 500V, 1%; 510pF	21022-151	CD	CD19-FD511F03	SAN
C7	Mica, 500V +1/2pF -1/2pF; 15pF	21017-015	CD	CD15-CD150D03	SAN
C8	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN
C9	Mica, 500V, +1/2pF -1/2pF; 47pF	21017-047	CD	CD15-CD470D03	SAN
C10	Mica, 500V, +1/2pF -1/2pF; 33pF	21017-033	CD	CD15-CD330D03	SAN
C11	Mica, 500V, 1%; 470pF	21022-147	CD	CD19-FD471F03	SAN
C12	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE
C13,14	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN
C15	Mica, 500V, +1/2pF -1/2pF; 10pF	21017-010	CD	CD15-CD100D03	SAN
C16	Polypropylene, 50V, 2.5%; 0.01uF	21702-310	NOB	CQ15P1H103GPP	WES
C19	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C20	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE
C21,22	Mica, 500V, 1%; 1500pF	21022-215	CD	CD19-FD152F03	SAN
C23,24	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN
C25	Mica, 500V, +1/2pF -1/2pF; 3pF	21017-003	CD	CD15-CD030D03	SAN
C40,41	Mica, 500V +1/2pF -1/2pF; 39pF	21017-039	CD	CD15-CD390D03	SAN
C42,43	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C44	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S	
C45,46	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C47	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S	
C48,49	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C50	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S	
C51,52	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C53	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S	
C54,55	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C56	Alum., Radial, 25V, -20% +100%; 100uF	21206-710	PAN	ECE-A1EV101S	
C57-60	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C61,62	Met. Polyester, 100V, 10%; 0.01uF	21441-310	WES	160C 103K630	SIE,WIM
C63-84	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM
C90	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
Capacitors (continued)						
C91	Mica, 500V, 5%; 150pF	21020-115	CD	CD15-FD151J03	SAN	
C92	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR1,2	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800	MANY	
CR5,6	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
CR7-10	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800	MANY	
CR20	Diode, Voltage Reference	22081-112	NAT	LM385	MOT	
Inductors						
L1	Inductor, Variable	29705-004	ORB			
L2	Inductor, Variable	29705-005	ORB			
Integrated Circuits						
IC1,2	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC3,4	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC5-7	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC8	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC10-12	Digital, 2-Channel Multiplexer	24562-302	NAT	MM7HC4053		
IC13,14	Quad Comparator	24710-302	NAT	LM339		
IC15	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC16	Power Buffer	24707-102	LT	LT1010CH		
IC17,18	Digital, Octal Flip-Flop	24553-302	NAT	MM74HC374		
IC19	D.C. Regulator, 5V Positive	24307-901	NAT	LM78M05C	TI,MOT	
IC20	D.C. Regulator, 5V Negative	24308-901	NAT	LM79M05C	TI,MOT	
IC21	Digital, Buffer	24568-302	NAT	MM74HC244N	TI	
IC22	Digital, Up-Counter	24508-302	RCA	CD4520BE		
IC23	Digital, Dual Flip-Flop	24567-302	RCA	CD74HC74N	SIG	
IC24	Digital, Hex Inverter	24572-302	NAT	74HC04N	TI	
IC25	Digital, Magnitude Comparator	24574-302	SIG	74HC85N	TI	
IC26	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC27	Power Buffer	24707-102	LT	LT1010CH		
IC28,29	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC31	Digital, PROM	44001-002	ORB			

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Integrated Circuits (continued)					
IC32	Digital, Converter	24726-302	AD	AD7576JN		
IC34	Digital, Line Decoder	24569-302	NAT	MM74HC138N	TI	
	Miscellaneous					
Y1	Crystal; 4.864 MHz	28052-002	NEL	NE-18-4.864MHz		
	Resistors					
R37	Trimpot, Cermet, 20 Turn; 1K	20512-210	BEK	89PR1K	BRN	
R50	Trimpot, Cermet, 20 Turn; 5K	20512-250	BEK	89PR5K	BRN	
R66	Trimpot, Cermet, 20 Turn; 25K	20512-325	BEK	89PR25K	BRN	
R72	Trimpot, Cermet, 20 Turn; 25K	20512-325	BEK	89PR25K	BRN	
R102	Resistor, 1/4W; 0 OHM (Jumper)	20020-025	ROHM	JPW-02A		
R103	Resistor Network, SIP; 100K	20221-101	BEK	L10-1C104		
	Switches					
S1	Switch, Rotary; 2P3T	26205-000	ELSW	080-020330NX		
	Transistors					
Q1-5	Transistor, JFET/N	23403-101	NAT	J111	INS	
Q8	Transistor, Signal, PNP	23002-101	MOT	2N4402	FSC	
Q9	Transistor, JFET/N	23403-101	NAT	J111	INS	
Q10	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
Q30,31	Transistor, JFET/N	23403-101	NAT	J111	INS	
SWITCH BOARD ASSEMBLY						
	LED					
None	LED, Green	25107-002	MAT	LN322GP		
	Switches					
S5	Switch, Rotary, Encoder	26080-000	CLA	600EN-128-CBL		

FOOTNOTES:
(1) See page 6-26 for Vendor abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

Vendor Codes

AB Rockwell Allen-Bradley
625 Liberty Ave
Pittsburgh, PA 15222-3123

AD Analog Devices, Inc.
One Technology Way
PO Box 9106
Norwood, MA 02062-9106

AKG AKG Acoustics, Inc.
See Orban

AM Amphenol Corporation
358 Hall Avenue
Wallingford, CT 06492

BEK Beckman Industrial Corporation
4141 Palm Street
Fullerton, CA 92635-1025

BEL Belden Electronic Wire & Cable
PO Box 1980
Richmond, IN 47374

BRN Bourns, Inc
Resistive Components Group
1200 Columbia Avenue
Riverside, CA 92507

BUS Bussmann Division
Cooper Industries
PO Box 14460
St. Louis, MO 63178

CD Cornell-Dubilier Electronics
1700 Rte. 23 North
Wayne, NJ 07470

CRL Mepcopal/Centralab
See Mepcopal

CSC Crystal Semiconductor Corporation
4210-T. South Industrial Dr.
Austin, TX 78744

CTS CTS Corporation
907 North West Blvd.
Elkhart, IN 46514

CW CW Industries
130 James Way
Southampton, PA 18966

DBX dbx
A Harman International Company
8760 South Sandy Parkway
Sandy, UT 84107

DEL Delta Products Corp
3225 Laurel View Ct.
Fremont, CA 94538

DUR Duracell, Inc.
Berkshire Industrial Park
Bethel, CT 06801

ELSW Electro Switch
77 King Avenue
Weymouth, MA 02188

EMI Crompton Modutec
920 Candia Rd.
Manchester, NH 03109

EXR Exar Corporation
2222 Qume Dr.
PO Box 49007
San Jose, CA 95161-9007

FR Fair-Rite Products Corp.
PO Box J
Wallkill, NY 12589

FSC Fairchild Camera & Instr. Corp.
See National Semiconductor

GI General Instruments
Optoelectronics Division
See Quality Technologies

HA Harris Semiconductor
1301 Woody Burke Rd.
Melbourne, FL 32901

HO Hoyt Elect. Inst. Works
19 Linden St.
Penacook, NH 03303

HP Hewlett-Packard Co.
Components Group
640 Page Mill Road
Palo Alto, CA 94304

INS Intersil, Inc.
See Harris Semiconductor

ITW ITW Switches
An Illinois Tool Works Co.
6615 W. Irving Park Rd.
Dept. T
Chicago, IL 60634

KEM KEMET Electronics Corporation
Post Office Box 5928
Greenville, South Carolina 29606

KEY Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105

LFE Littlefuse
A Subsidiary of Tracor, Inc.
800 E. Northwest Hwy
Des Plaines, IL 60016

LT Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035

LUMX Lumex Opto/Components Inc.
292 E. Hellen Road
Palatine, IL 60067

MAL Mallory Capacitor Co.
7545 Rockville Rd.
PO Box 1284
Indianapolis, IN 46241

MAR Marquardt Switches, Inc.
2711-TR Route 20 East
Cazenovia, NY 13035

MAT Matsushita Electric Corp
of America
One Panasonic Way
Secaucus, NJ 07094

ME Mepcopal/Centralab
A North American Phillips Corp.
11468 Sorrento Valley Road
San Diego, CA 92121

MID Hollingsworth/Wearnes
1601 N. Powerline Rd.
Pampano, FL 33069

MIL J.W. Miller Division
Bell Industries
306 E. Alondra
Gardena, CA 90247

MOT Motorola Semiconductor
PO Box 20912
Phoenix, AZ 85036

MUR Murata Erie North America
2200 Lake Park Drive
Smyrna, GA 30080

NAT National Semiconductor Corp.
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95051

NEL Crystal Biotech
75 South Street
Hopkinton, MA 01748

NOB Noble U.S.A., Incorporated
5450 Meadowbrook Industrial Ct.
Rolling Meadows, IL 60008

OKI OKI Semiconductor
785 N. Mary Ave.
Sunnyvale, CA 94086-2909

OHM Ohmite Manufactoring Company
3601 Howard Street
Skokie, IL 60076

ORB Orban
A Harman International Company
1525 Alvarado Street
San Leandro, CA 94577

PAN Panasonic Industrial Company
Two Panasonic Way
7E-2T
Secaucus, NJ 07094

QT Quality Technologies, Inc.
610 North Mary Ave.
Sunnyvale, CA 94086

RAL Raltron Electronics Corp.
2315 NW 107th Ave.
Miami, FL 33172

RAY Raytheon Company
Semiconductor Division
350 Ellis Street
Mountain View, CA 94039

RCA RCA Solid State
See Harris Semiconductor

ROHM Rohm Electronics
3034 Owens Dr.
Antioch, TENN 37013

SAE Stanford Applied Engineering, Inc
340 Martin Avenue
Santa Clara, CA 95050

SAN Sangamo Weston Inc.
Capacitor Division
See Cornell-Dubilier

SCH ITT Schadow, Inc.
8081 Wallace Road
Eden Prairie, MN 55344

SIE Siemens Components Inc.
Heimann Systems Div.
186 Wood Avenue South
Iselin, NJ 08830

SIG Philips Components - Signetics
North American Phillips Corp.
811 E. Arques
Sunnyvale, CA 94088

SPR Sprague Electric Co.
41 Hampden Road
PO Box 9102
Manifold, MA 02048-9102

S.W. Seitchcraft
A Raytheon Company
5555 N. Elation Avenue
Chicago, IL 60630

AT Taiga America, Inc.
700 Frontier Way
Bensenville, IL 60106

TDK TDK Electronics Corporation
12 Harbor Park
Port Washington, NY 11050

TI Texas Instruments, Inc.
PO Box 655012
Dallas, TX 75265

TOS Toshiba America, Inc.
9740 Irvine Blvd.
Irvine, CA 92718

TRW TRW Electronics Components
Connector Division
1501 Morse Avenue
Elk Grove Village, IL 60007

VARO Micro Quality Semiconductor, Inc.
PO Box 469013
Garland, TX 75046-9013

WES Westlake
See Mallory Capacitor Co.

WIM Wima Division
2269 Saw Mill Rd.
Building 4C
PO Box 217
Elmsford, NY 10533

ZI ZILOG Inc.
210 Hacienda Ave.
Campbell, CA 95008

Schematics, Assembly Drawings

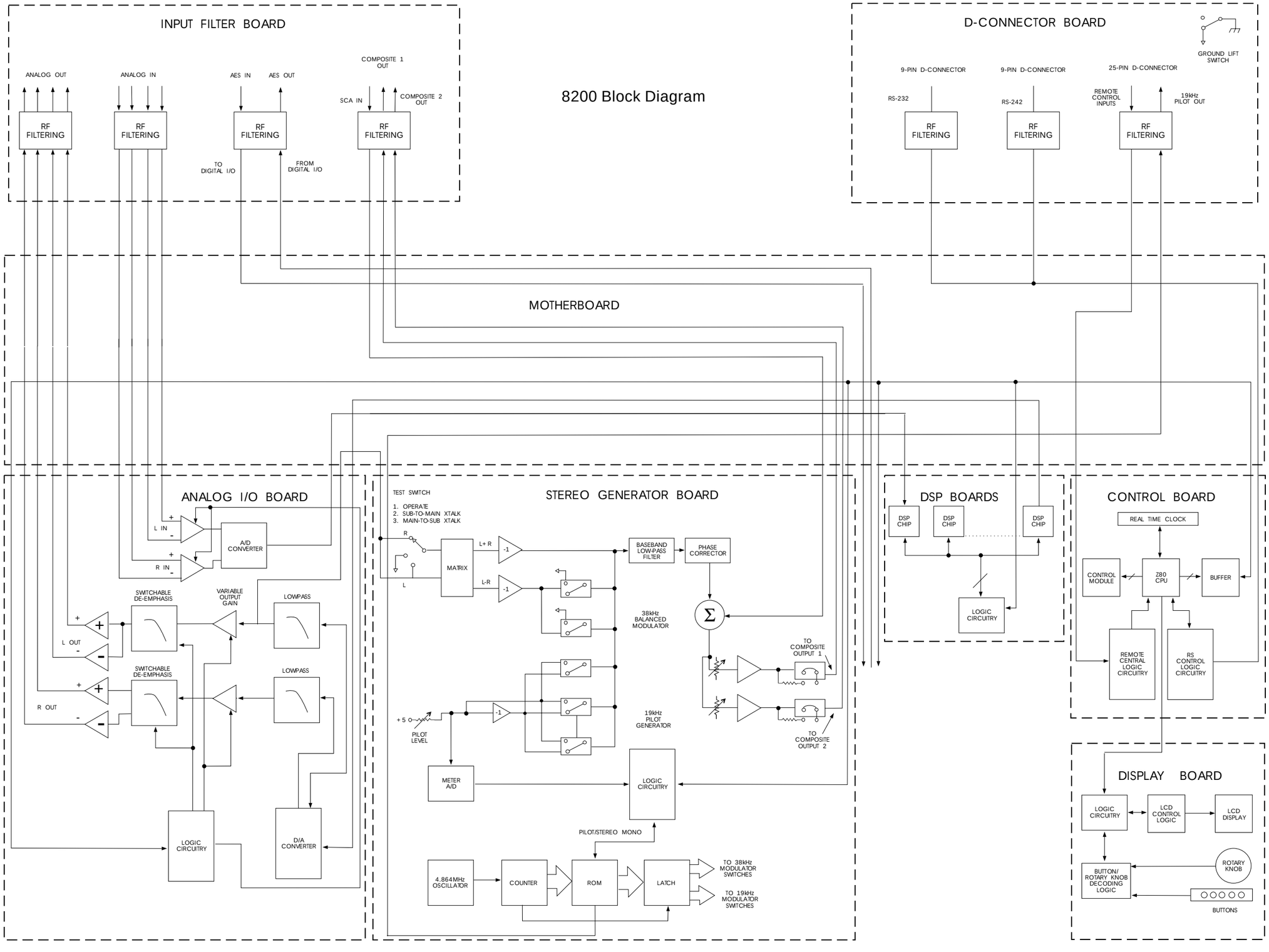
The following drawings are included in this manual:

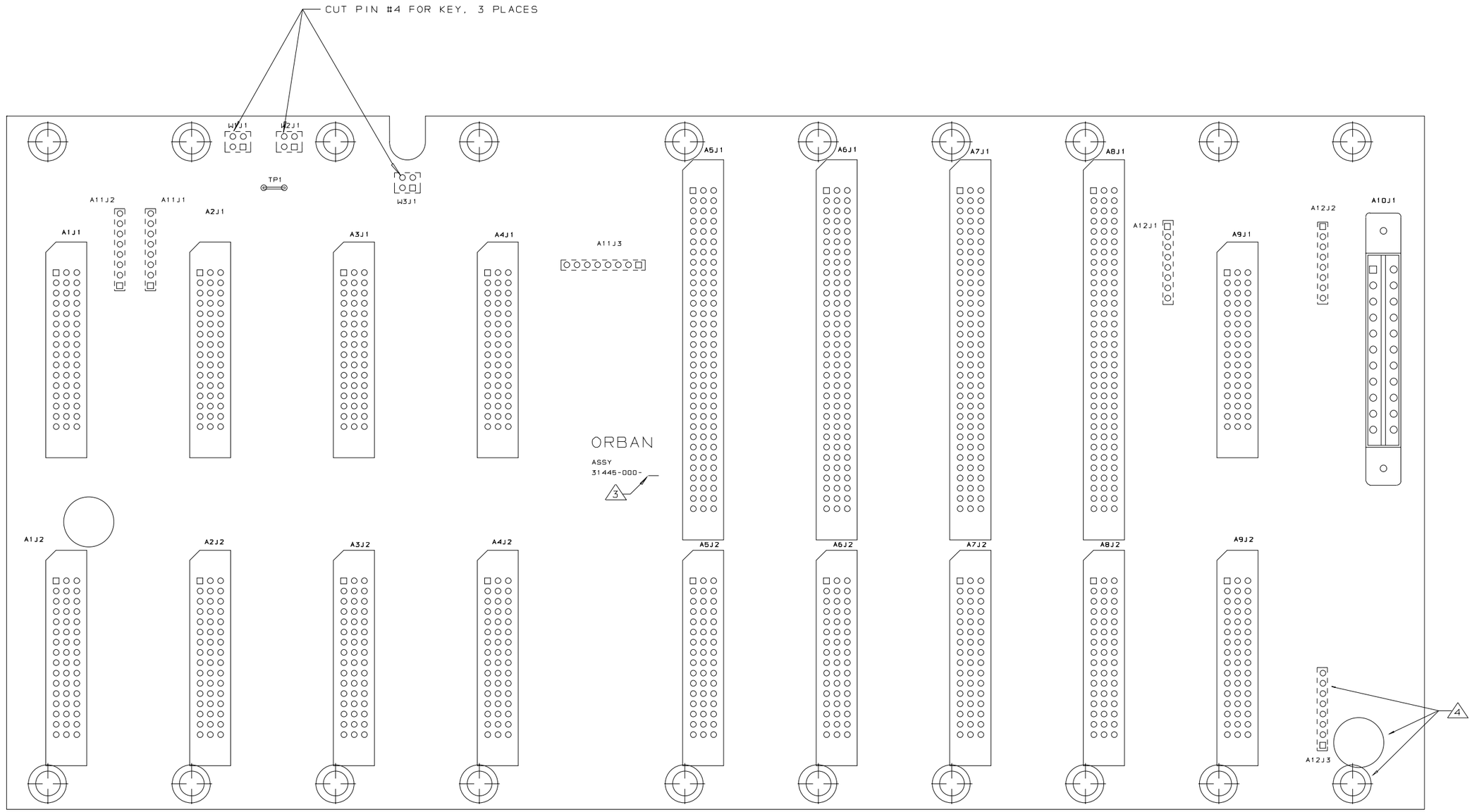
Page	Circuit Board	Drawing
6-46	Block Diagram	Assembly Drawing
6-47	Mother	Assembly Drawing
6-48	Mother	Schematic 1 of 5
6-49		2 of 5
6-50		3 of 5
6-51		4 of 5
6-52		5 of 5
6-53	Control	Assembly Drawing
6-54	Control	Schematic 1 of 2
6-55		2 of 2
6-56	DSP	Assembly Drawing
6-57	DSP	Schematic 1 of 4
6-58		2 of 4
6-59		3 of 4
6-60		4 of 4
6-61	Analog I/O	Assembly Drawing
6-62	Analog I/O	Schematic 1 of 4
6-63		2 of 4
6-64		3 of 4
6-65		4 of 4
6-66	Stereo Encoder	Assembly Drawing
6-67	Stereo Encoder	Schematic 1 of 3
6-68		2 of 3
6-69		3 of 3
6-71	Display	Assembly Drawing
6-72	Display	Schematic 1 of 2
6-73		2 of 2
6-74	Regulator	Assembly Drawing
6-75	Regulator	Schematic
6-76	Input Filter	Assembly Drawing
6-77	Input Filter	Schematic
6-78	D-Connector	Assembly Drawing
6-79	D-Connector	Schematic

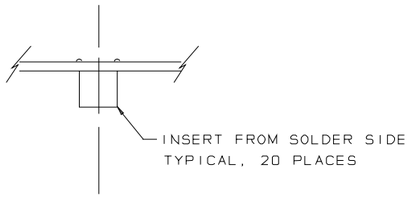
These drawings reflect the actual construction of your unit as accurately as possible. Any differences between the drawings and your unit are almost undoubtedly due to product improvements or production changes since the publication of this manual.

If you intend to replace parts, please read page 6-27

8200 Block Diagram







COMPONENT SIDE

5. CONNECTORS SHOWN AS DASHED LINES TO BE MOUNTED ON SOLDER SIDE OF PCB AFTER WAVE SOLDER OF COMPONENT SIDE CONNECTIONS.

4. MASK ALL MOUNTING HOLES AND HOLES FOR SOLDER SIDE CONNECTORS BEFORE WAVE SOLDERING.

3. MARK ASSEMBLY REVISION LEVEL IN SPACE PROVIDED

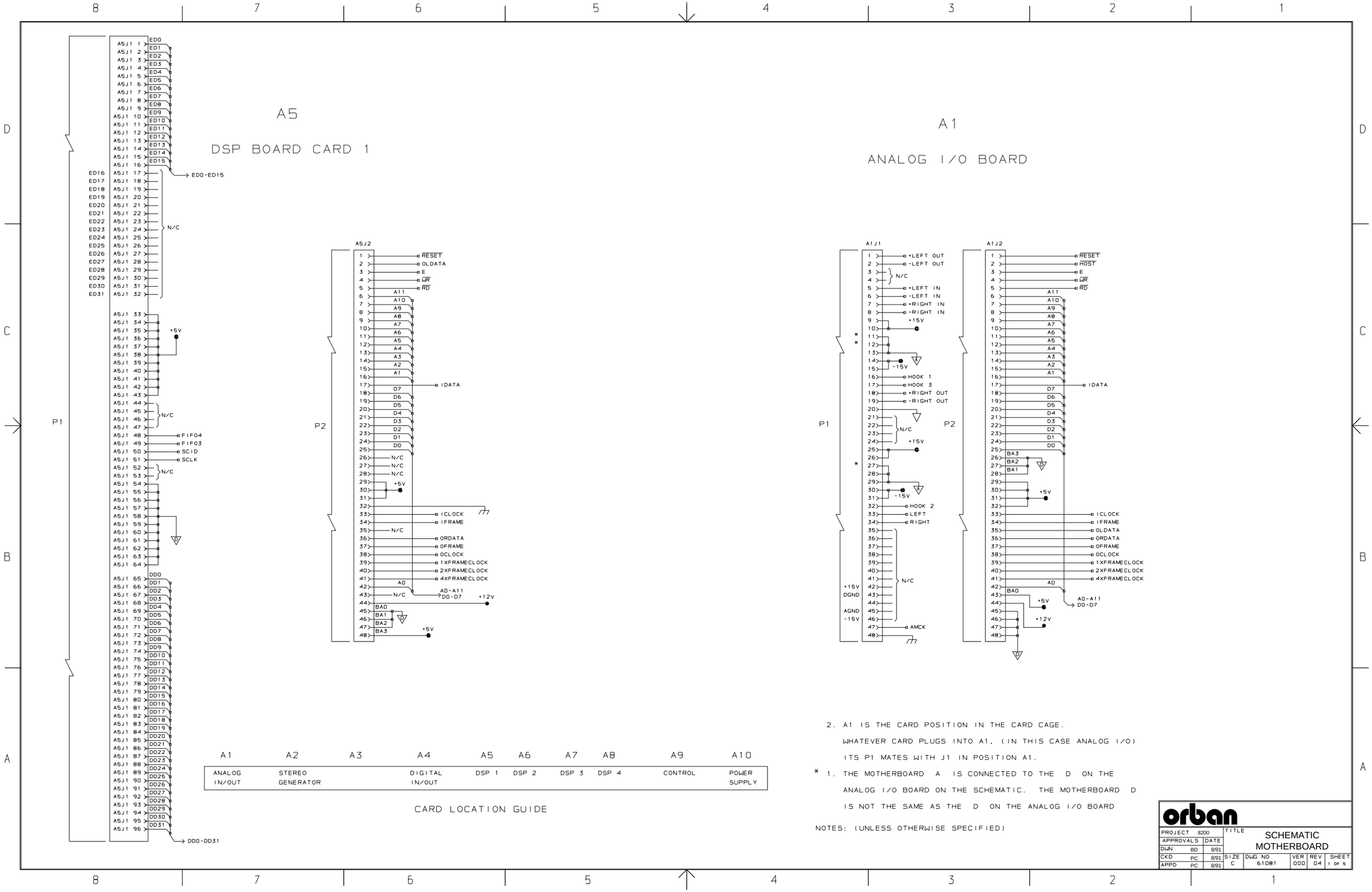
2. REFERENCE SCHEMATIC DRAWING NO. 61081

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

MODEL	8200		TITLE	PCB ASSEMBLY MOTHERBOARD				
APPROVALS		DATE						
DWN	BD	5/91						
CKD	MJ	5/91	SIZE	DWG NO	VER	REV	SHEET	
APPD	MJ	5/91	C	31445	000	02	1 OF 1	


A5
DSP BOARD CARD 1
A5J1 1 ED0
A5J1 2 ED1
A5J1 3 ED2
A5J1 4 ED3
A5J1 5 ED4
A5J1 6 ED5
A5J1 7 ED6
A5J1 8 ED7
A5J1 9 ED8
A5J1 10 ED9
A5J1 11 ED10
A5J1 12 ED11
A5J1 13 ED12
A5J1 14 ED13
A5J1 15 ED14
A5J1 16 ED15
ED0-ED15
ED16 A5J1 17
ED17 A5J1 18
ED18 A5J1 19
ED19 A5J1 20
ED20 A5J1 21
ED21 A5J1 22
ED22 A5J1 23
ED23 A5J1 24
ED24 A5J1 25
ED25 A5J1 26
ED26 A5J1 27
ED27 A5J1 28
ED28 A5J1 29
ED29 A5J1 30
ED30 A5J1 31
ED31 A5J1 32
N/C
A5J1 33
A5J1 34
A5J1 35 +5V
A5J1 36
A5J1 37
A5J1 38
A5J1 39
A5J1 40
A5J1 41
A5J1 42
A5J1 43
A5J1 44
A5J1 45
A5J1 46
A5J1 47
N/C
A5J1 48 FIF04
A5J1 49 FIF03
A5J1 50 SCID
A5J1 51 SCLK
A5J1 52
A5J1 53
N/C
A5J1 54
A5J1 55
A5J1 56
A5J1 57
A5J1 58
A5J1 59
A5J1 60
A5J1 61
A5J1 62
A5J1 63
A5J1 64
DD0
A5J1 65 DD1
A5J1 66 DD2
A5J1 67 DD3
A5J1 68 DD4
A5J1 69 DD5
A5J1 70 DD6
A5J1 71 DD7
A5J1 72 DD8
A5J1 73 DD9
A5J1 74 DD10
A5J1 75 DD11
A5J1 76 DD12
A5J1 77 DD13
A5J1 78 DD14
A5J1 79 DD15
A5J1 80 DD16
A5J1 81 DD17
A5J1 82 DD18
A5J1 83 DD19
A5J1 84 DD20
A5J1 85 DD21
A5J1 86 DD22
A5J1 87 DD23
A5J1 88 DD24
A5J1 89 DD25
A5J1 90 DD26
A5J1 91 DD27
A5J1 92 DD28
A5J1 93 DD29
A5J1 94 DD30
A5J1 95 DD31
A5J1 96
DD0-DD31
P1
P2
A5J2
1 RESET
2 OLDATA
3 E
4 WR
5 RD
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
IDATA
D7
D6
D5
D4
D3
D2
D1
D0
N/C
+5V
ICLOCK
IFRAME
N/C
ORDATA
OFRAME
OCLOCK
1XFRAMECLOCK
2XFRAMECLOCK
4XFRAMECLOCK
A0
N/C
A0-A11
D0-D7
+12V
BA0
BA1
BA2
BA3
+5V
A1
ANALOG I/O BOARD
A1J1
1 +LEFT OUT
2 -LEFT OUT
3
4
N/C
5 +LEFT IN
6 -LEFT IN
7 +RIGHT IN
8 -RIGHT IN
9 +15V
10
11
12
13
14 -15V
15
16 HOOK 1
17 HOOK 3
18 +RIGHT OUT
19 -RIGHT OUT
20
21
22
23
24
25
26
27
28
29
30 -15V
31
32 HOOK 2
33 LEFT
34 RIGHT
35
36
37
38
39
40
41
42
43
44
45
46
47 AMCK
48
+15V
DGND
AGND
-15V
N/C
+15V
N/C
A1J2
1 RESET
2 HOST
3 E
4 WR
5 RD
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
IDATA
D7
D6
D5
D4
D3
D2
D1
D0
BA3
BA2
BA1
+5V
ICLOCK
IFRAME
OLDATA
ORDATA
OFRAME
OCLOCK
1XFRAMECLOCK
2XFRAMECLOCK
4XFRAMECLOCK
A0
BA0
+5V
+12V
A0-A11
D0-D7
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
ANALOG IN/OUT
STEREO GENERATOR
DIGITAL IN/OUT
DSP 1
DSP 2
DSP 3
DSP 4
CONTROL
POWER SUPPLY
CARD LOCATION GUIDE
2. A1 IS THE CARD POSITION IN THE CARD CAGE.
WHATEVER CARD PLUGS INTO A1, (IN THIS CASE ANALOG I/O)
ITS P1 MATES WITH J1 IN POSITION A1.
* 1. THE MOTHERBOARD A IS CONNECTED TO THE D ON THE
ANALOG I/O BOARD ON THE SCHEMATIC. THE MOTHERBOARD D
IS NOT THE SAME AS THE D ON THE ANALOG I/O BOARD
NOTES: (UNLESS OTHERWISE SPECIFIED)
orban
PROJECT 8200
APPROVALS DATE
DWN BD 8/91
CKD PC 8/91
APPD PC 8/91
TITLE
SCHEMATIC
MOTHERBOARD
SIZE C
DWG NO 61081
VER 000
REV 04
SHEET 1 OF 5

A6

DSP BOARD CARD 2

A6J1

P1

A6J1 1 DD0
A6J1 2 DD1
A6J1 3 DD2
A6J1 4 DD3
A6J1 5 DD4
A6J1 6 DD5
A6J1 7 DD6
A6J1 8 DD7
A6J1 9 DD8
A6J1 10 DD9
A6J1 11 DD10
A6J1 12 DD11
A6J1 13 DD12
A6J1 14 DD13
A6J1 15 DD14
A6J1 16 DD15
A6J1 17 DD16
A6J1 18 DD17
A6J1 19 DD18
A6J1 20 DD19
A6J1 21 DD20
A6J1 22 DD21
A6J1 23 DD22
A6J1 24 DD23
A6J1 25 DD24
A6J1 26 DD25
A6J1 27 DD26
A6J1 28 DD27
A6J1 29 DD28
A6J1 30 DD29
A6J1 31 DD30
A6J1 32 DD31 → DD0-DD31

A6J1 33
A6J1 34
A6J1 35 +5V
A6J1 36
A6J1 37
A6J1 38
A6J1 39
A6J1 40
A6J1 41
A6J1 42
A6J1 43
A6J1 44 N/C
A6J1 45
A6J1 46
A6J1 47

A6J1 48 FIF03
A6J1 49 FIF02
A6J1 50 SCID
A6J1 51 SCLK
A6J1 52 N/C
A6J1 53 N/C
A6J1 54
A6J1 55
A6J1 56
A6J1 57
A6J1 58
A6J1 59
A6J1 60
A6J1 61
A6J1 62
A6J1 63
A6J1 64

A6J1 65 CD0
A6J1 66 CD1
A6J1 67 CD2
A6J1 68 CD3
A6J1 69 CD4
A6J1 70 CD5
A6J1 71 CD6
A6J1 72 CD7
A6J1 73 CD8
A6J1 74 CD9
A6J1 75 CD10
A6J1 76 CD11
A6J1 77 CD12
A6J1 78 CD13
A6J1 79 CD14
A6J1 80 CD15
A6J1 81 CD16
A6J1 82 CD17
A6J1 83 CD18
A6J1 84 CD19
A6J1 85 CD20
A6J1 86 CD21
A6J1 87 CD22
A6J1 88 CD23
A6J1 89 CD24
A6J1 90 CD25
A6J1 91 CD26
A6J1 92 CD27
A6J1 93 CD28
A6J1 94 CD29
A6J1 95 CD30
A6J1 96 CD31 → CD0-CD31

A6J2

P2

1 RESET
2 N/C
3 E
4 WR
5 RD
6 A11
7 A10
8 A9
9 A8
10 A7
11 A6
12 A5
13 A4
14 A3
15 A2
16 A1
17 IDATA
18 D7
19 D6
20 D5
21 D4
22 D3
23 D2
24 D1
25 D0
26 N/C
27
28
29
30 +5V
31
32
33 ICLOCK
34 IFRAME
35 N/C
36 N/C
37 N/C
38 N/C
39 1XFRAMECLOCK
40 2XFRAMECLOCK
41 4XFRAMECLOCK
42 A0
43 N/C +12V → A0-A11, D0-D7
44
45 BA0
46 BA1 +5V
47 BA2
48 BA3

A2

STEREO GENERATOR BOARD

A2J1

P1

1 COMPOSITE OUTPUT1
2 COMP1 GND
3 SCA IN
4 -4.2V
5 RIGHT
6 LEFT
7 L-R
8 -(L-R)
9 HOOK 4
10 HOOK 3
11 +15V
12
13
14 -15V
15
16 HOOK 1
17 COMPOSITE OUTPUT2
18 COMP2 GND
19 SCA GND
20 +4.2V
21 HOOK 6
22 HOOK 5
23
24 FIF04
25 +15V
26
27
28
29
30 -15V
31
32 HOOK 2
33 ED0
34 ED1
35 ED2
36 ED3
37 ED4
38 ED5
39 ED6
40 ED7
41 ED8
42 ED9
43 ED10
44 ED11
45 ED12
46 ED13
47 ED14
48 ED15 → ED0-ED15

DELAYED RIGHT
DELAYED LEFT

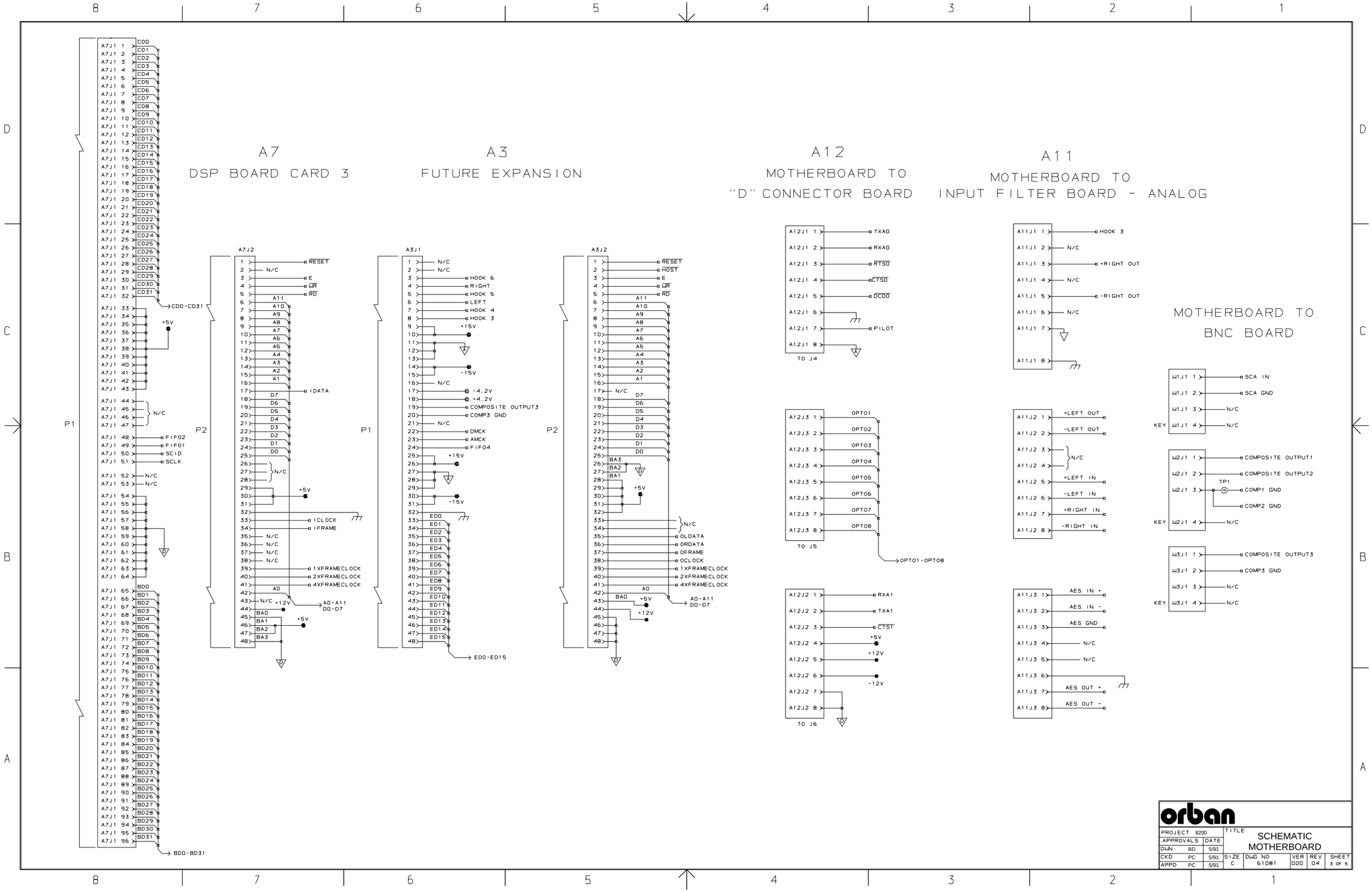
A2J2

P2

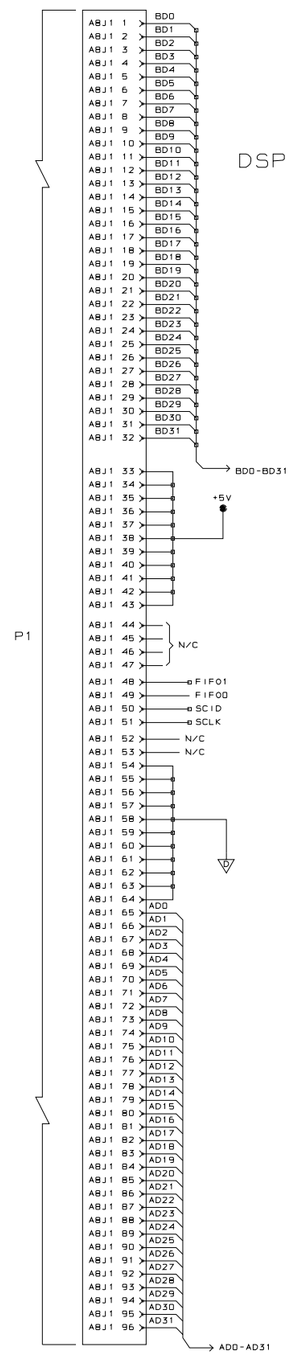
1 RESET
2 HOST
3 E
4 WR
5 RD
6 A11
7 A10
8 A9
9 A8
10 A7
11 A6
12 A5
13 A4
14 A3
15 A2
16 A1
17 N/C D7
18 D6
19 D5
20 D4
21 D3
22 D2
23 D1
24 D0
25 BA3
26 BA2
27 BA1
28
29
30 +5V
31
32
33 PILOT
34 N/C
35 OLDATA
36 ORDATA
37 OFRAME
38 OCLOCK
39 1XFRAMECLOCK
40 2XFRAMECLOCK
41 4XFRAMECLOCK
42 A0
43 BA0
44 +12V → A0-A11, D0-D7
45
46
47
48

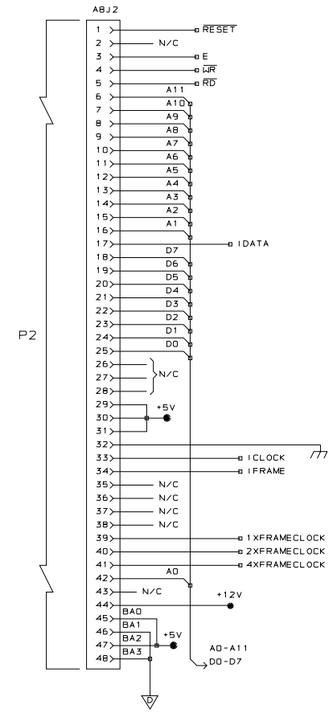
orban

PROJECT 8200		TITLE	SCHEMATIC MOTHERBOARD				
APPROVALS	DATE						
DWN BD	5/91						
CKD PC	5/91	SIZE C	DWG NO 61081	VER 000	REV 04	SHEET 2 OF 5	
APPD PC	5/91						

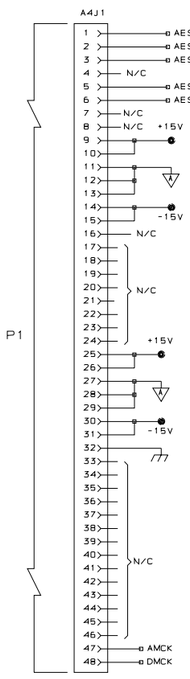

A7
DSP BOARD CARD 3
A3
FUTURE EXPANSION
A12
MOTHERBOARD TO
"D" CONNECTOR BOARD
A11
MOTHERBOARD TO
INPUT FILTER BOARD - ANALOG
MOTHERBOARD TO
BNC BOARD
A7J1 1 CD0
A7J1 2 CD1
A7J1 3 CD2
A7J1 4 CD3
A7J1 5 CD4
A7J1 6 CD5
A7J1 7 CD6
A7J1 8 CD7
A7J1 9 CD8
A7J1 10 CD9
A7J1 11 CD10
A7J1 12 CD11
A7J1 13 CD12
A7J1 14 CD13
A7J1 15 CD14
A7J1 16 CD15
A7J1 17 CD16
A7J1 18 CD17
A7J1 19 CD18
A7J1 20 CD19
A7J1 21 CD20
A7J1 22 CD21
A7J1 23 CD22
A7J1 24 CD23
A7J1 25 CD24
A7J1 26 CD25
A7J1 27 CD26
A7J1 28 CD27
A7J1 29 CD28
A7J1 30 CD29
A7J1 31 CD30
A7J1 32 CD31
CD0-CD31
A7J1 33
A7J1 34
A7J1 35 +5V
A7J1 36
A7J1 37
A7J1 38
A7J1 39
A7J1 40
A7J1 41
A7J1 42
A7J1 43
A7J1 44
A7J1 45 N/C
A7J1 46
A7J1 47
A7J1 48 FIFO2
A7J1 49 FIFO1
A7J1 50 SCID
A7J1 51 SCLK
A7J1 52 N/C
A7J1 53 N/C
A7J1 54
A7J1 55
A7J1 56
A7J1 57
A7J1 58
A7J1 59
A7J1 60
A7J1 61
A7J1 62
A7J1 63
A7J1 64
A7J1 65 BD0
A7J1 66 BD1
A7J1 67 BD2
A7J1 68 BD3
A7J1 69 BD4
A7J1 70 BD5
A7J1 71 BD6
A7J1 72 BD7
A7J1 73 BD8
A7J1 74 BD9
A7J1 75 BD10
A7J1 76 BD11
A7J1 77 BD12
A7J1 78 BD13
A7J1 79 BD14
A7J1 80 BD15
A7J1 81 BD16
A7J1 82 BD17
A7J1 83 BD18
A7J1 84 BD19
A7J1 85 BD20
A7J1 86 BD21
A7J1 87 BD22
A7J1 88 BD23
A7J1 89 BD24
A7J1 90 BD25
A7J1 91 BD26
A7J1 92 BD27
A7J1 93 BD28
A7J1 94 BD29
A7J1 95 BD30
A7J1 96 BD31
BD0-BD31
P1
P2
A7J2
1 RESET
2 N/C
3 E
4 R/W
5 RD
6 A11
7 A10
8 A9
9 A8
10 A7
11 A6
12 A5
13 A4
14 A3
15 A2
16 A1
17 IDATA
18 D7
19 D6
20 D5
21 D4
22 D3
23 D2
24 D1
25 D0
26
27 N/C
28
29
30 +5V
31
32
33 ICLOCK
34 IFRAME
35 N/C
36 N/C
37 N/C
38 N/C
39 1XFRAMECLOCK
40 2XFRAMECLOCK
41 4XFRAMECLOCK
42 A0
43 N/C +12V
44 A0-A11
45 BA0 D0-D7
46 BA1 +5V
47 BA2
48 BA3
A3J1
1 N/C
2 N/C
3 HOOK 6
4 RIGHT
5 HOOK 5
6 LEFT
7 HOOK 4
8 HOOK 3
9 +15V
10
11
12
13
14 -15V
15
16 N/C
17 -4.2V
18 +4.2V
19 COMPOSITE OUTPUT3
20 COMP3 GND
21 N/C
22 DMCK
23 AMCK
24 FIF04
25 +15V
26
27
28
29
30 -15V
31
32
33 ED0
34 ED1
35 ED2
36 ED3
37 ED4
38 ED5
39 ED6
40 ED7
41 ED8
42 ED9
43 ED10
44 ED11
45 ED12
46 ED13
47 ED14
48 ED15
ED0-ED15
A3J2
1 RESET
2 HOST
3 E
4 R/W
5 RD
6 A11
7 A10
8 A9
9 A8
10 A7
11 A6
12 A5
13 A4
14 A3
15 A2
16 A1
17 N/C
18 D7
19 D6
20 D5
21 D4
22 D3
23 D2
24 D1
25 D0
26 BA3
27 BA2
28 BA1
29
30 +5V
31
32
33 N/C
34
35 OLDATA
36 ORDATA
37 OFRAME
38 OCLOCK
39 1XFRAMECLOCK
40 2XFRAMECLOCK
41 4XFRAMECLOCK
42 A0
43 BA0 +5V
44 A0-A11
45 +12V D0-D7
46
47
48
A12J1 1 TXA0
A12J1 2 RXA0
A12J1 3 RTS0
A12J1 4 CTS0
A12J1 5 DCD0
A12J1 6
A12J1 7 PILOT
A12J1 8
TO J4
A12J3 1 OPTO1
A12J3 2 OPTO2
A12J3 3 OPTO3
A12J3 4 OPTO4
A12J3 5 OPTO5
A12J3 6 OPTO6
A12J3 7 OPTO7
A12J3 8 OPTO8
TO J5
OPTO1-OPTO8
A12J2 1 RXA1
A12J2 2 TXA1
A12J2 3 CTS1
A12J2 4 +5V
A12J2 5 +12V
A12J2 6 -12V
A12J2 7
A12J2 8
TO J6
A11J1 1 HOOK 3
A11J1 2 N/C
A11J1 3 +RIGHT OUT
A11J1 4 N/C
A11J1 5 -RIGHT OUT
A11J1 6 N/C
A11J1 7
A11J1 8
A11J2 1 +LEFT OUT
A11J2 2 -LEFT OUT
A11J2 3
A11J2 4 N/C
A11J2 5 +LEFT IN
A11J2 6 -LEFT IN
A11J2 7 +RIGHT IN
A11J2 8 -RIGHT IN
A11J3 1 AES IN +
A11J3 2 AES IN -
A11J3 3 AES GND
A11J3 4 N/C
A11J3 5 N/C
A11J3 6
A11J3 7 AES OUT +
A11J3 8 AES OUT -
W1J1 1 SCA IN
W1J1 2 SCA GND
W1J1 3 N/C
KEY W1J1 4 N/C
W2J1 1 COMPOSITE OUTPUT1
W2J1 2 COMPOSITE OUTPUT2
TP1
W2J1 3 COMP1 GND
COMP2 GND
KEY W2J1 4 N/C
W3J1 1 COMPOSITE OUTPUT3
W3J1 2 COMP3 GND
W3J1 3 N/C
KEY W3J1 4 N/C
orban
PROJECT 8200
APPROVALS DATE
DWN BD 5/91
CKD PC 5/91
APPD PC 5/91
TITLE
SCHEMATIC
MOTHERBOARD
SIZE C
DWG NO 61081
VER 000
REV 04
SHEET 3 OF 5

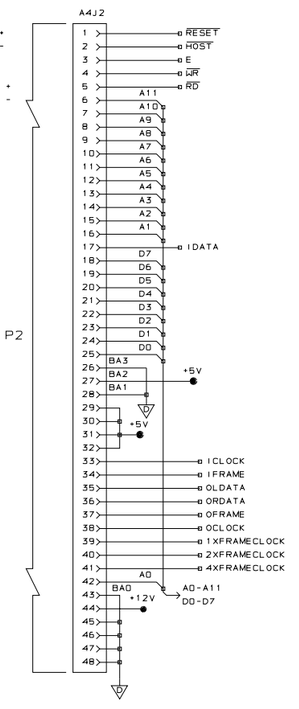
A8
DSP BOARD CARD 4





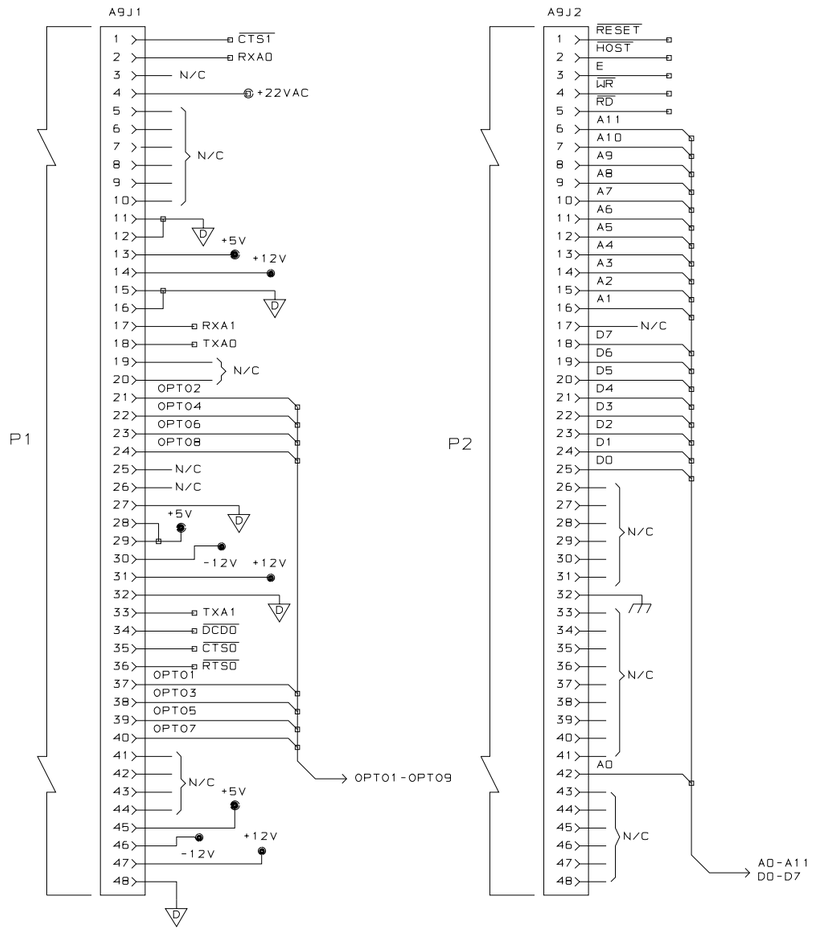
A4
DIGITAL I/O BOARD



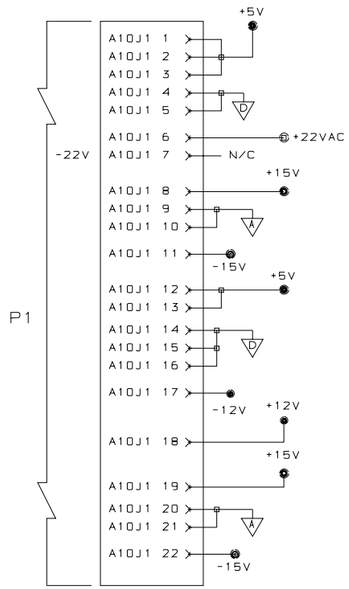


orban							
PROJECT 8200		TITLE	SCHEMATIC MOTHERBOARD				
APPROVALS	DATE						
DWN BD	8/91						
CKD PC	8/91	SIZE C	DWG NO 61081	VER 000	REV 04	SHEET 4 OF 5	
APPD PC	8/91						

A9
CONTROL BOARD

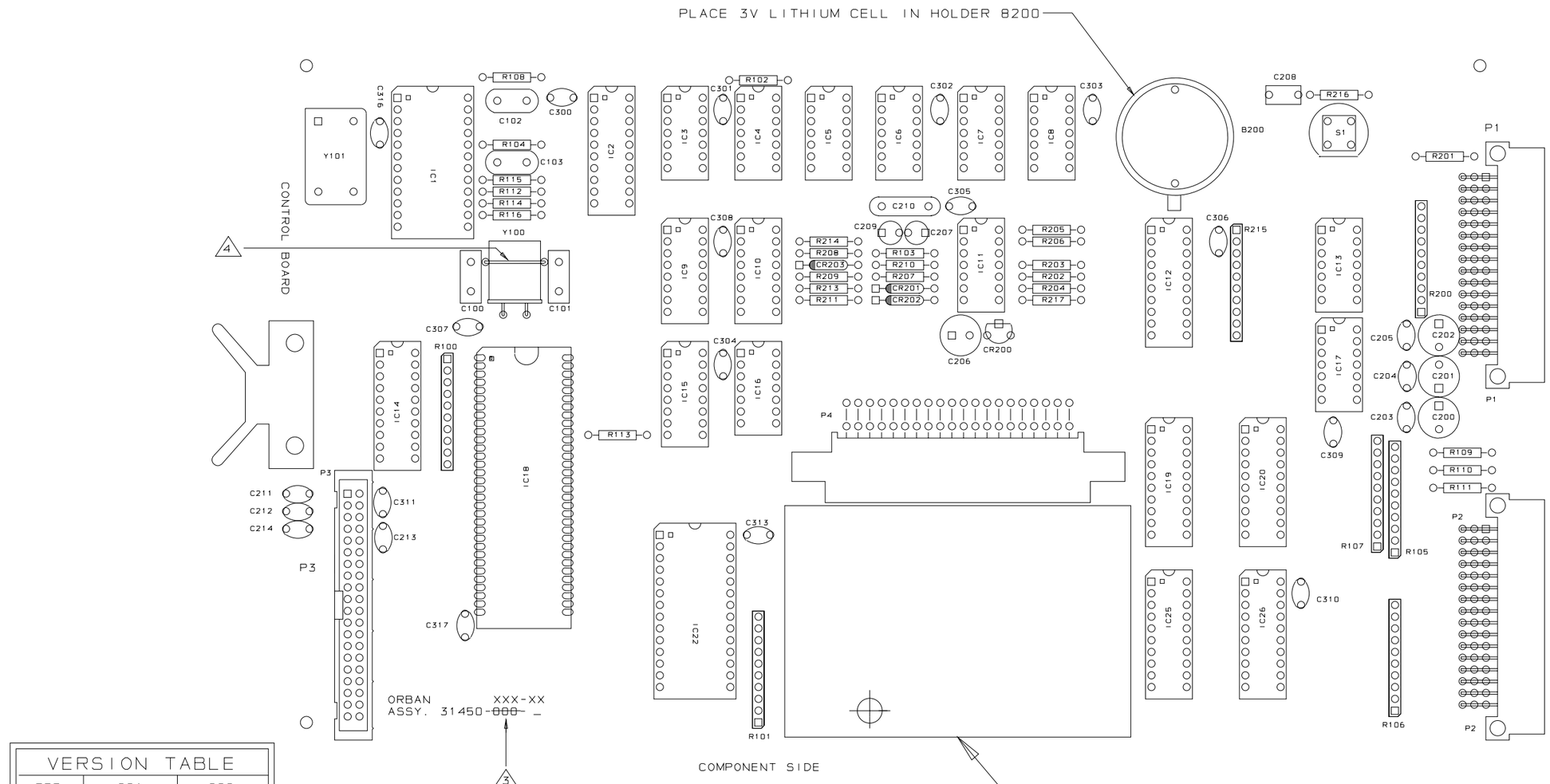


A10
POWER SUPPLY



orban

PROJECT 8200			TITLE SCHEMATIC MOTHERBOARD				
APPROVALS		DATE					
DWN	BD	5/91					
CKD	PC	5/91	SIZE C	DWG NO 61081	VER 000	REV 04	SHEET 5 OF 5
APPD	PC	5/91					



VERSION TABLE		
REF	-001	-002
IC 9	74HC138	74AC138
IC 15	74HC138	74AC138
IC 18	6MHz	10MHz
Y100	12.288MHz	18.432MHz

4 GROUND STRAP REQ'D FOR VER-001 (6MHz) ONLY

3 LINE OUT OLD ASSY NO. VERSION
MARK IN APPROPRIATE VERSION & REVISION LEVEL

2. REFERENCE SCHEMATIC DRAWING NO. 61082

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

MODEL	8200		TITLE	PCB ASSEMBLY CONTROL CARD				
APPROVALS		DATE						
DWN	BD	12/91						
CKD	PC	12/91	SIZE	DWG NO	VER	REV	SHEET	
APPD	PC	12/91	C	31450	000	08	1 OF 1	

P2
HOST CONNECTOR
NON-CONNECTED PINS

P2 17
P2 26
P2 27
P2 28
P2 29
P2 30
P2 31
P2 33
P2 34
P2 35
P2 36
P2 37
P2 38
P2 39
P2 40
P2 41
P2 43
P2 44
P2 45
P2 46
P2 47
P2 48
N/C

IC15 74HC138
IC9 74HC138
IC10 74HC138
G1 Vcc GND
A17 A16 A15 A14 A13 A12
G2A G2B
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
N/C
MDISPL1
MDISPLAY
CE3
BATTERY
REMOTE
DTSPLAY
TO SHT2
OE2

IC18 Z180
Vcc GND
RESET XTAL EXTAL CLK E
NMI INT0 INT1 INT2
BUSREQ BUSACK WAIT HALT
CKA0/DREQ0 DREQ1 TEND1
TXA1 RXA1 CKA1 RFSH ST TXS RXS/CTS1 CKS TXA0 RXA0 RTS0 CTS0 DCD0
A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
MT IORQ MREQ WR RD
CE1
C100 22PF 500V
C101 22PF 500V
Y100 12.288 MHZ
R100 100K
R113 47K 5%
P1 33 P1 17 P1 1 P1 18 P1 2 P1 36 P1 35 P1 34
P1 3 P1 5 P1 6 P1 7 P1 8 P1 9 P1 10 P1 19 P1 20 P1 25 P1 26 P1 41 P1 42 P1 43 P1 44
P1
I/O CONNECTOR
48-PIN

IC22 RAM TC5565
VBAT Vcc GND
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
OE CE1 CE2 R/W RESET
D7 D6 D5 D4 D3 D2 D1 D0
R101 100K
IC16-A 74HC04
IC16-B 74HC04
CE2

P4
TO SOLDER SIDE
EDGE CONNECTOR
CONTROL BOARD PROGRAM MODULE

P4 1 P4 3 P4 5 P4 7 P4 9 P4 11 P4 13 P4 15 P4 17 P4 19 P4 21 P4 23 P4 25 P4 27 P4 29 P4 31 P4 33 P4 35 P4 37 P4 39
CE3 RD EEBSY A8 A11 D5 D6 OE2 A3 A1 D0 A6 A7 A15 D3 CE1 D1 D2

P4
TO COMPONENT SIDE
EDGE CONNECTOR
CONTROL BOARD PROGRAM MODULE

P4 2 P4 4 P4 6 P4 8 P4 10 P4 12 P4 14 P4 16 P4 18 P4 20 P4 22 P4 24 P4 26 P4 28 P4 30 P4 32 P4 34 P4 36 P4 38 P4 40
A17 WR A13 A9 A10 D4 CE2 A5 A4 A2 A0 N/C N/C A12 A14 D7 MREQ A16

VERSION TABLE		
REF	-001	-002
IC 9	74HC138	74AC138
IC 15	74HC138	74AC138
IC 18	6MHz	10MHz
Y100	12.288MHz	18.432MHz

DELETE MODULE SIGNAL NAMES FOR USE IN MANUAL

HOST
TIME
MHOST
IORQ
MREQ
WR
RD
RESET
CE1
CE2
CE3
D0-D7
A0-A7

IC6-A 74HC04
IC5-A 74HC393
IC6-B 74HC04
IC6-C 74HC04
IC6-D 74HC04
IC6-E 74HC04
IC6-F 74HC04
IC7-A 74HC08
IC7-B 74HC08
IC7-C 74HC08
IC7-D 74HC08
IC8-A 74HC32
IC8-B 74HC32
IC8-C 74HC32
IC8-D 74HC32
IC3-A 74HC32
IC3-B 74HC32
IC3-C 74HC32
IC4-A 74HC74
IC4-B 74HC74
R102 100K 5%
R103 100K 5%

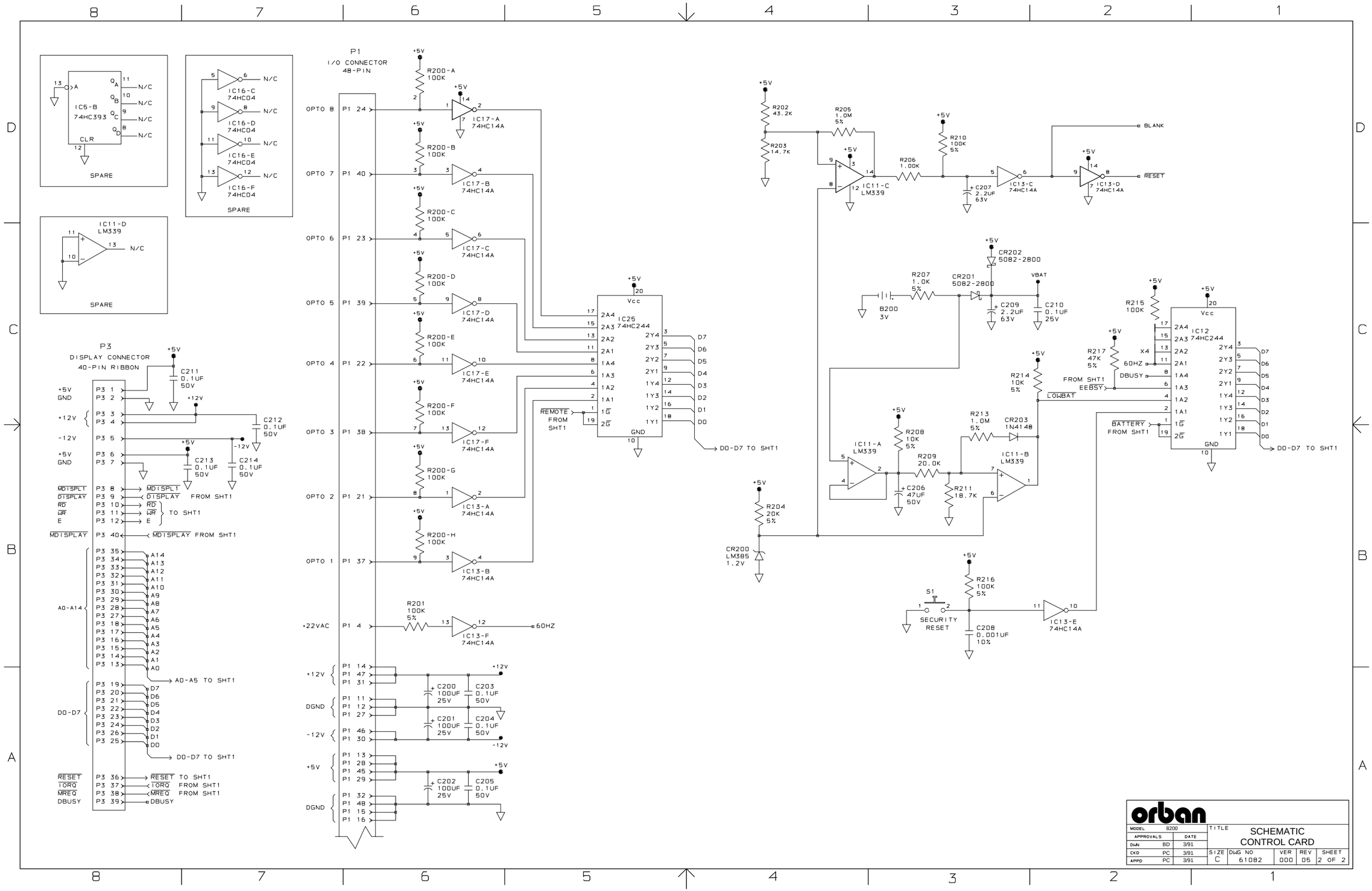
IC14 74HC244
IC19 74HC244
IC26 74HC244
IC2 74HC245
IC20 74HC245
R105 100K
R106 100K
R107 100K
R109 47K 5%
R110 47K 5%
R111 47K 5%
R112 100Ω 5%
R114 10K 5%
R115 10K 5%
R116 10K 5%
C103 100PF 1%

P2 S 1
HOST CONNECTOR
48-PIN

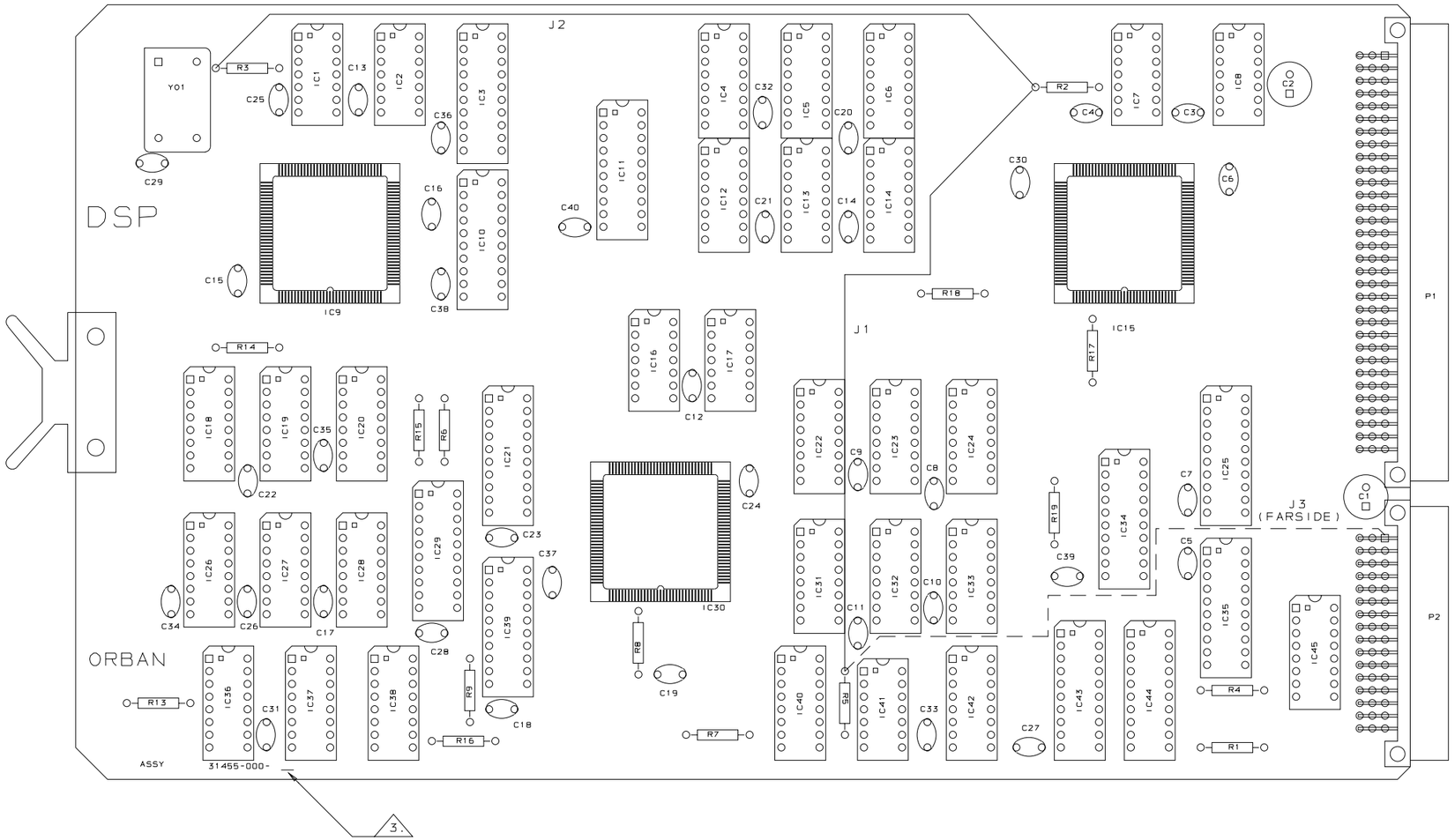
P2 2 HOST
P2 3 E
P2 4 WR
P2 5 RD
P2 6 A11
P2 7 A10
P2 8 A9
P2 9 A8
RESET P2 1
P2 10 A7
P2 11 A6
P2 12 A5
P2 13 A4
P2 14 A3
P2 15 A2
P2 16 A1
P2 42 A0
P2 18 D7
P2 19 D6
P2 20 D5
P2 21 D4
P2 22 D3
P2 23 D2
P2 24 D1
P2 25 D0

IC1 DS MC146818A
VDD VSS
AS CS R/W RESET STBY
OSC1 OSC2 CKOUT CKFS SQW PS IRQ MOT
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
R104 100K 5%
R108 100Ω 5%
C102 100PF 1%
Y101 32.768KHZ

orban		TITLE	SCHEMATIC CONTROL CARD			
MODEL	8200					
APPROVALS	DATE					
DWN BD	3/91					
CKD PC	3/91	SIZE	DWG NO	VER	REV	SHEET
APPD PC	3/91	C	61082	VER	05	1 OF 2



orban			
MODEL	8200	TITLE	SCHEMATIC CONTROL CARD
APPROVALS	DATE		
DWN BD	3/91		
CKD PC	3/91	SIZE C	DWG NO 61082
APPD PC	3/91	VER 000	REV 05
		SHEET 2 OF 2	



COMPONENT SIDE

COMPONENT SIDE

3. MARK ASSEMBLY REVISION LEVEL IN SPACE PROVIDED

2. REFERENCE SCHEMATIC DRAWING NO. 61083-000-05

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES POS. SIDE OF CAPS., PIN 1 OF IC'S

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

MODEL	8200		TITLE	PCB ASSEMBLY DSP CARDS				
APPROVALS		DATE						
DWN	BD	10/93						
CKD	MJ	6/93	SIZE	DWG NO	VER	REV	SHEET	
APPD	MJ	6/93	C	31455	000	06	1 OF 1	

P2 (FROM MOTHERBOARD)
48 PIN CONNECTOR PLUG

J1-J3 ARE JUMPER WIRE, ADD TO THE ASSEMBLY.

J3 J2 J1

IC42 74HC138 — IC45 74HC85 — IC41-A 74HC04 — IC41-B 74HC04 — IC41-C 74HC04 — IC41-D 74HC04 — IC41-E 74HC04 — IC41-F 74HC04

IC44 74HC373 — IC43 74HC373

IC40 74HC253B — IC36 74HC253B — IC37 74HC253B — IC38 74HC253B

IC8-C 74HC32 — IC8-D 74HC32

Y01 27 MHZ OSCILLATOR

R1 10.0K 1% — R2 47.5K 1% — R3 47.5K 1% — R5 47.5K 1% — R4 10.0K 1%

BA3	P2 48	
BA2	P2 47	
BA1	P2 46	
BA0	P2 45	
A6	P2 11	HA6
A7	P2 10	HA7
E	P2 3	
A0	P2 42	HA0
A1	P2 16	HA1
A2	P2 15	HA2
A3	P2 14	HA3
A4	P2 13	HA4
A5	P2 12	HA5
A8	P2 9	HA8
A9	P2 8	HA9
A10	P2 7	HA10
A11	P2 6	HA11
WR	P2 4	
RESET	P2 1	
RD	P2 5	
	P2 26	
	P2 27	
	P2 28	
	P2 29	
+5V	P2 30	
	P2 31	
CHASSIS GND	P2 32	
	P2 35	N/C
OLDATA	P2 2	STDL TO SHEET 3
ORDATA	P2 36	STDR TO SHEETS 2 & 4
OFRAME	P2 37	OFRAME TO SHEET 4
OCLOCK	P2 38	OCLOCK TO SHEET 4
D0	P2 25	HD0
D1	P2 24	HD1
D2	P2 23	HD2
D3	P2 22	HD3
D4	P2 21	HD4
D5	P2 20	HD5
D6	P2 19	HD6
D7	P2 18	HD7
I DATA	P2 17	SRD
I CLOCK	P2 33	SCO
I FRAME	P2 34	SC1
	P2 39	1XFRAMECLOCK
	P2 40	2XFRAMECLOCK
	P2 41	4XFRAMECLOCK
	P2 43	N/C
+12 V	P2 44	N/C

3 HA0-HA2

8 HD0-HD7

HOST BUS TO SHEETS 2,3 & 4

HEN3 TO SHEET 4
HEN2 TO SHEET 3
HEN0 TO SHEET 2

RESET0 TO SHEET 2
RESET2 TO SHEET 3
RESET3 TO SHEET 4

1XFRAMECLOCK
2XFRAMECLOCK
4XFRAMECLOCK

IRQB0 TO SHEET 2
IRQB2 TO SHEET 3
IRQB3 TO SHEET 4

SERIAL INPUT BUS TO SHEETS 2,3 & 4

CLOCK TO SHEETS 2,3 & 4

orban

MODEL	8200	TITLE	SCHEMATIC DSP CARDS
APPROVALS	DATE		
DsN SG	3/90		
CKD PC	3/90		
APPD PC	3/90		

SIZE	DWG NO	VER	REV	SHEET
B	61083	000	05	1 OF 4

P1 (FROM MOTHERBOARD)

96-PIN CONNECTOR

B17 P1 49

R19 47.5K 1%

IC16-A 74HC02

R6 10.0K 1%

B18 P1 50 SCID

B19 P1 51 SCLK

SCI BUS TO SHEETS 3 & 4

C25 P1 89 ID24
C26 P1 90 ID25
C27 P1 91 ID26
C28 P1 92 ID27
C29 P1 93 ID28
C30 P1 94 ID29
C31 P1 95 ID30
C32 P1 96 ID31
N/C

C1 P1 65 ID0
C2 P1 66 ID1
C3 P1 67 ID2
C4 P1 68 ID3
C5 P1 69 ID4
C6 P1 70 ID5
C7 P1 71 ID6
C8 P1 72 ID7
C9 P1 73 ID8
C10 P1 74 ID9
C11 P1 75 ID10
C12 P1 76 ID11
C13 P1 77 ID12
C14 P1 78 ID13
C15 P1 79 ID14
C16 P1 80 ID15
C17 P1 81 ID16
C18 P1 82 ID17
C19 P1 83 ID18
C20 P1 84 ID19
C21 P1 85 ID20
C22 P1 86 ID21
C23 P1 87 ID22
C24 P1 88 ID23

IC25 74HC373: ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7 → AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
IC34 74HC373: ID8 ID9 ID10 ID11 ID12 ID13 ID14 ID15 → AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15
IC35 74HC373: ID16 ID17 ID18 ID19 ID20 ID21 ID22 ID23 → AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23
IC24 74HC40105: AD0 AD1 AD2 AD3
IC23 74HC40105: AD4 AD5 AD6 AD7
IC22 74HC40105: AD8 AD9 AD10 AD11
IC33 74HC40105: AD12 AD13 AD14 AD15
IC32 74HC40105: AD16 AD17 AD18 AD19
IC31 74HC40105: AD20 AD21 AD22 AD23

IC16-C 74HC02

IC17-A 74HC32

IC17-B 74HC32

IC16-D 74HC02

AFIFOW TO SHEET 3

IC17-E 74HC32

SPARE

IRQBD FROM SHEET 1

SCI BUS

R7 47.5K 1%

R8 47.5K 1%

IC16-B 74HC02

RESETD FROM SHEET 1

CLOCK FROM SHEET 1

IL VCC

IL GND

IC30 DSP56001FC27

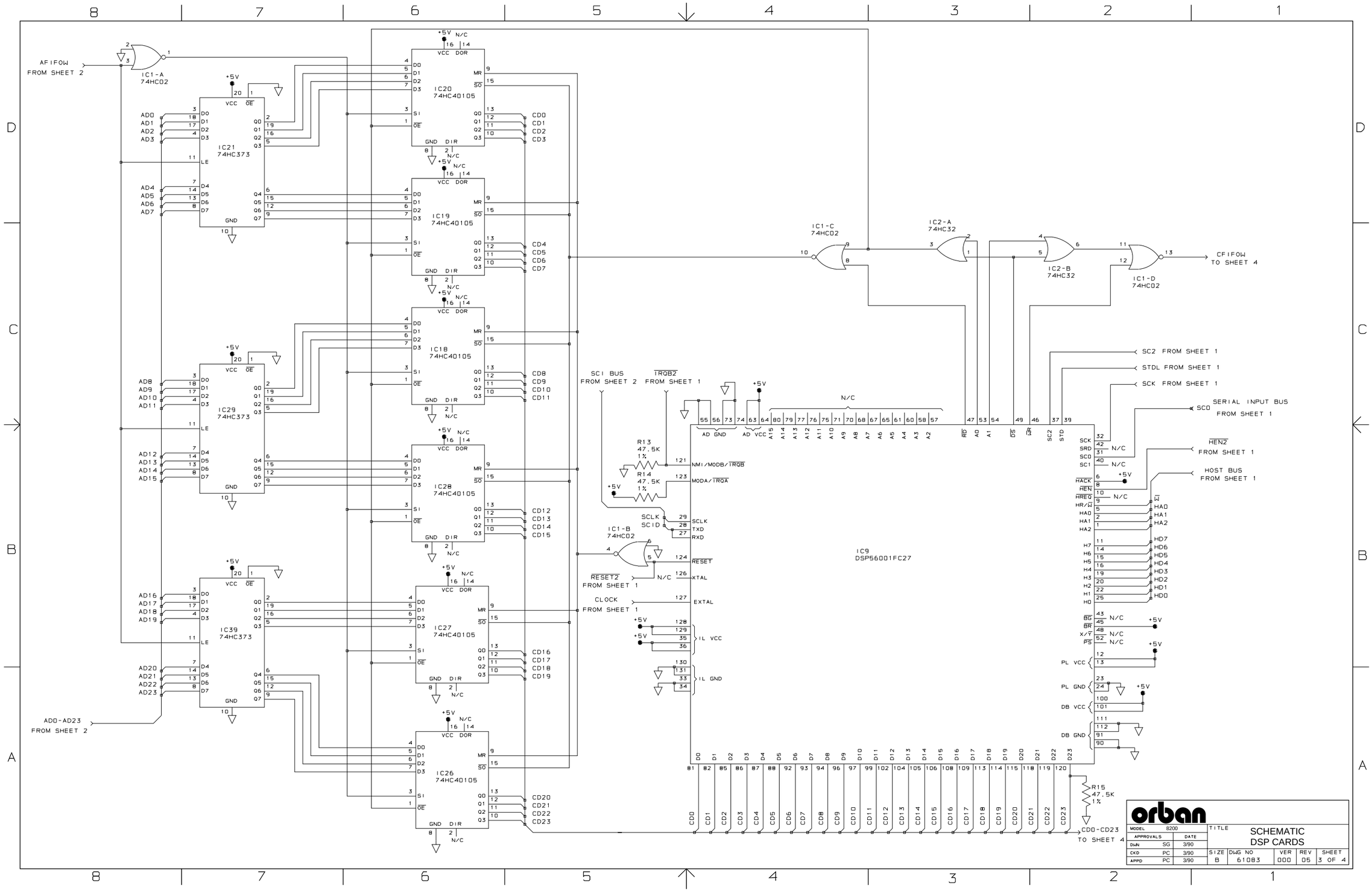
SC2 FROM SHEET 1
STDR FROM SHEET 1
SCK FROM SHEET 1
SERIAL INPUT BUS FROM SHEET 1
HENO FROM SHEET 1
HOST BUS FROM SHEET 1

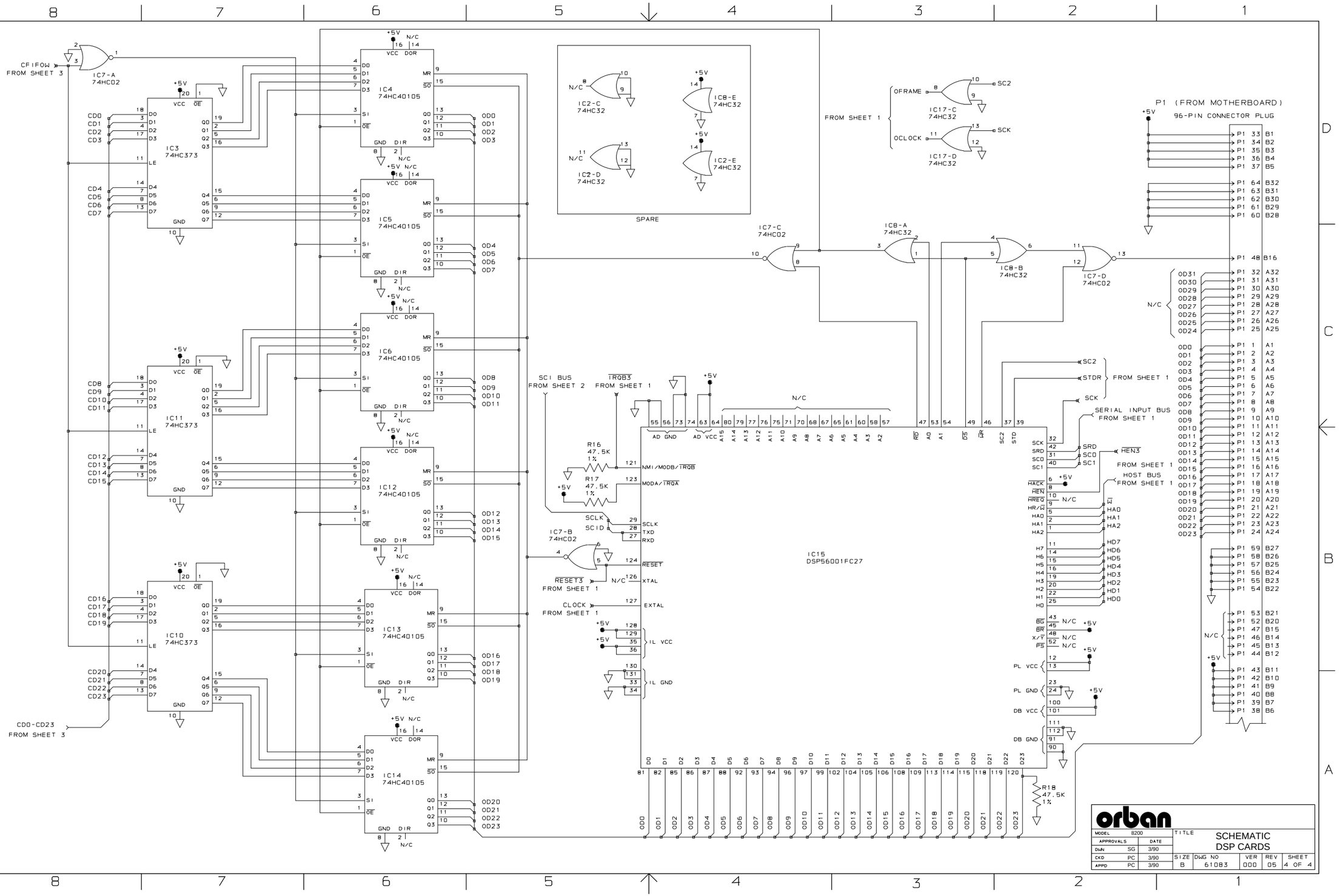
PL VCC
PL GND
DB VCC
DB GND

R9 47.5K 1%

AD0-AD23 TO SHEET 3

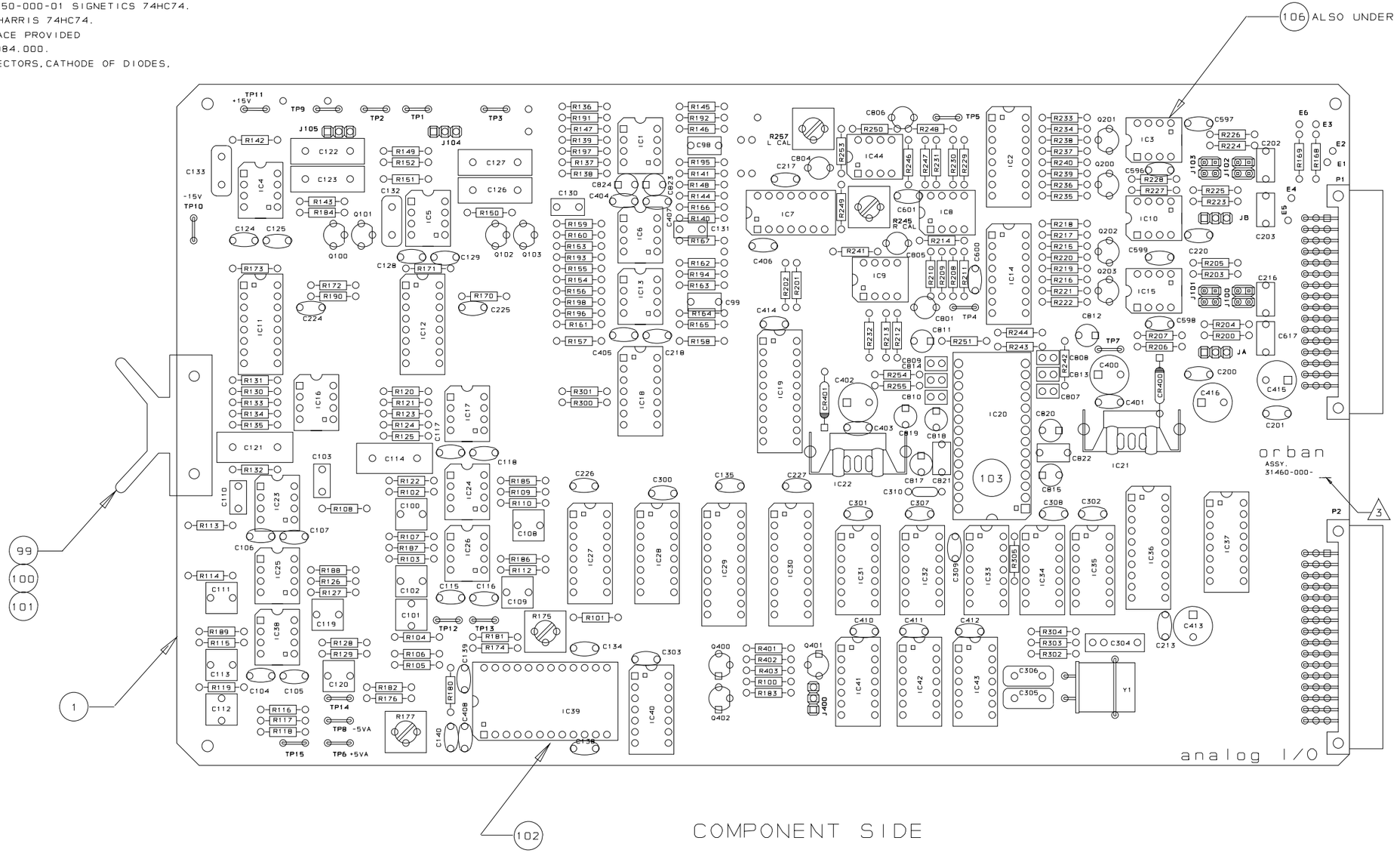
orban			
MODEL 8200		TITLE	SCHEMATIC DSP CARDS
APPROVALS	DATE		
DSN SG	3/90		
CKD PC	3/90		
APPD PC	3/90		
SIZE B	DWG NO 61083	VER 000	REV 05
			SHEET 2 OF 4


AFIFOW FROM SHEET 2
IC1-A 74HC02
IC21 74HC373
IC20 74HC40105
IC19 74HC40105
IC18 74HC40105
IC29 74HC373
IC28 74HC40105
IC39 74HC373
IC27 74HC40105
IC26 74HC40105
AD0-AD23 FROM SHEET 2
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
CD8
CD9
CD10
CD11
CD12
CD13
CD14
CD15
CD16
CD17
CD18
CD19
CD20
CD21
CD22
CD23
IC1-C 74HC02
IC2-A 74HC32
IC2-B 74HC32
IC1-D 74HC02
CFIFOW TO SHEET 4
SC1 BUS FROM SHEET 2
IRQB2 FROM SHEET 1
R13 47.5K 1%
R14 47.5K 1%
IC1-B 74HC02
RESET2 FROM SHEET 1
CLOCK FROM SHEET 1
IL VCC
IL GND
IC9 DSP56001FC27
SC2 FROM SHEET 1
STDL FROM SHEET 1
SCK FROM SHEET 1
SERIAL INPUT BUS
SCO
FROM SHEET 1
HEN2
FROM SHEET 1
HOST BUS
FROM SHEET 1
PL VCC
PL GND
DB VCC
DB GND
R15 47.5K 1%
CD0-CD23 TO SHEET 4
orban
MODEL 8200
TITLE
SCHEMATIC DSP CARDS
APPROVALS
DATE
DSN SG 3/90
CKD PC 3/90
APPD PC 3/90
SIZE B
DWG NO 61083
VER 000
REV 05
SHEET 3 OF 4


CFIFOW FROM SHEET 3
IC7-A 74HC02
IC3 74HC373
IC4 74HC40105
IC5 74HC40105
IC6 74HC40105
IC11 74HC373
IC12 74HC40105
IC10 74HC373
IC13 74HC40105
IC14 74HC40105
CD0-CD23 FROM SHEET 3
SPARE
IC2-C 74HC32
IC2-D 74HC32
IC8-E 74HC32
IC2-E 74HC32
FROM SHEET 1
OFRAME
OCLOCK
IC17-C 74HC32
IC17-D 74HC32
SC2
SCK
IC7-C 74HC02
IC8-A 74HC32
IC8-B 74HC32
IC7-D 74HC02
P1 (FROM MOTHERBOARD)
96-PIN CONNECTOR PLUG
SC1 BUS FROM SHEET 2
IRQB3 FROM SHEET 1
R16 47.5K 1%
R17 47.5K 1%
IC7-B 74HC02
RESET3 FROM SHEET 1
CLOCK FROM SHEET 1
IC15 DSP56001FC27
IL VCC
IL GND
N/C
AD GND
AD VCC
SERIAL INPUT BUS FROM SHEET 1
HOST BUS FROM SHEET 1
HEN3 FROM SHEET 1
PL VCC
PL GND
DB VCC
DB GND
R18 47.5K 1%
orban
MODEL 8200
TITLE
SCHEMATIC DSP CARDS
APPROVALS DATE
DWN SG 3/90
CKD PC 3/90
APPD PC 3/90
SIZE B
DWG NO 61083
VER 000
REV 05
SHEET 4 OF 4

NOTES: (UNLESS OTHERWISE SPECIFIED)

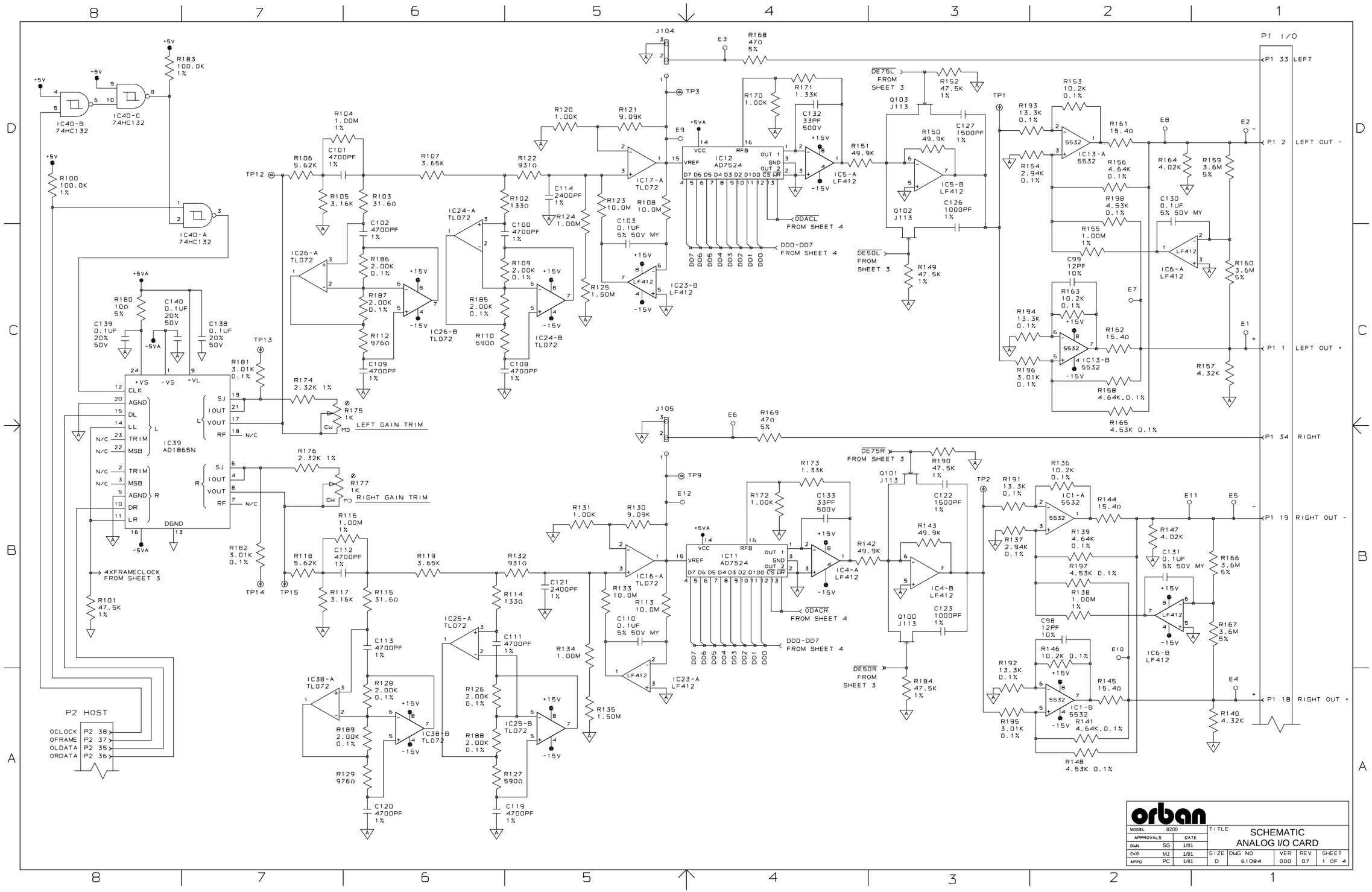
1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS
2. REFERENCE SCHEMATIC DRAWING NO. 61084.000.
3. MARK ASSEMBLY REVISION LEVEL IN SPACE PROVIDED
4. IC 31, IC32, IC34, & IC35 ARE P/N 24650-000-01 SIGNETICS 74HC74. DO NOT LOAD WITH P/N 24567-302-01 HARRIS 74HC74.

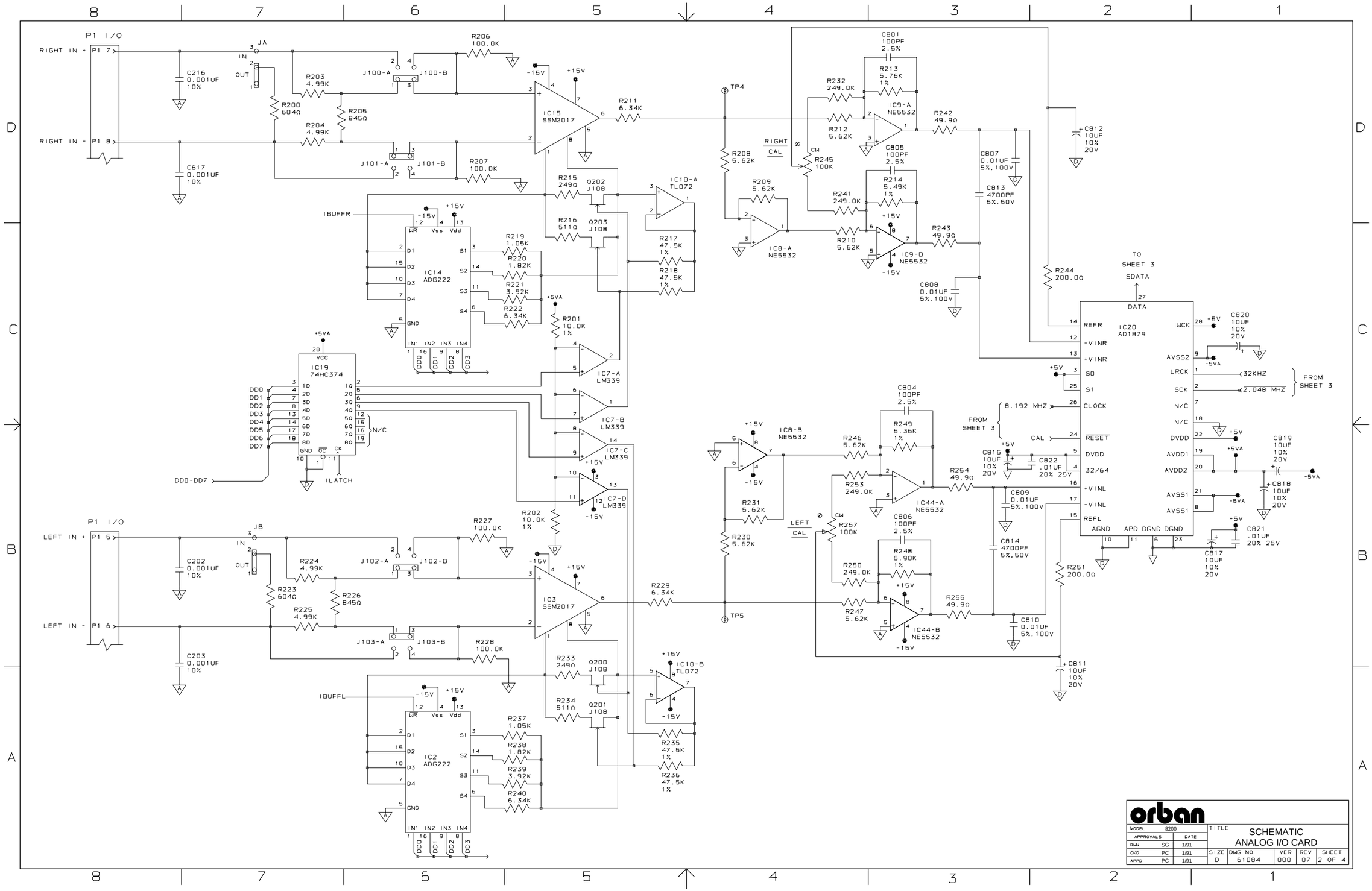


JUMPER SETTINGS

JA		JB		J101		J100		J103		J102		J104		J105		J400	
10K BRIDGING	600Ω TERMINATE	10K BRIDGING	600Ω TERMINATE	+27 TO +4 dBv PEAK	+6 TO -17 dBv PEAK	+27 TO +4 dBv PEAK	+6 TO -17 dBv PEAK	+27 TO +4 dBv PEAK	+6 TO -17 dBv PEAK	+27 TO +4 dBv PEAK	+6 TO -17 dBv PEAK	8200	8282	8200	8282	+27 TO +4 dBv PEAK	+6 TO -17 dBv PEAK
1 2 3	1 2 3	1 2 3	1 2 3	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	3 1 / 4 2	1 2 3	1 2 3	1 2 3	1 2 3	3 2 1	3 2 1

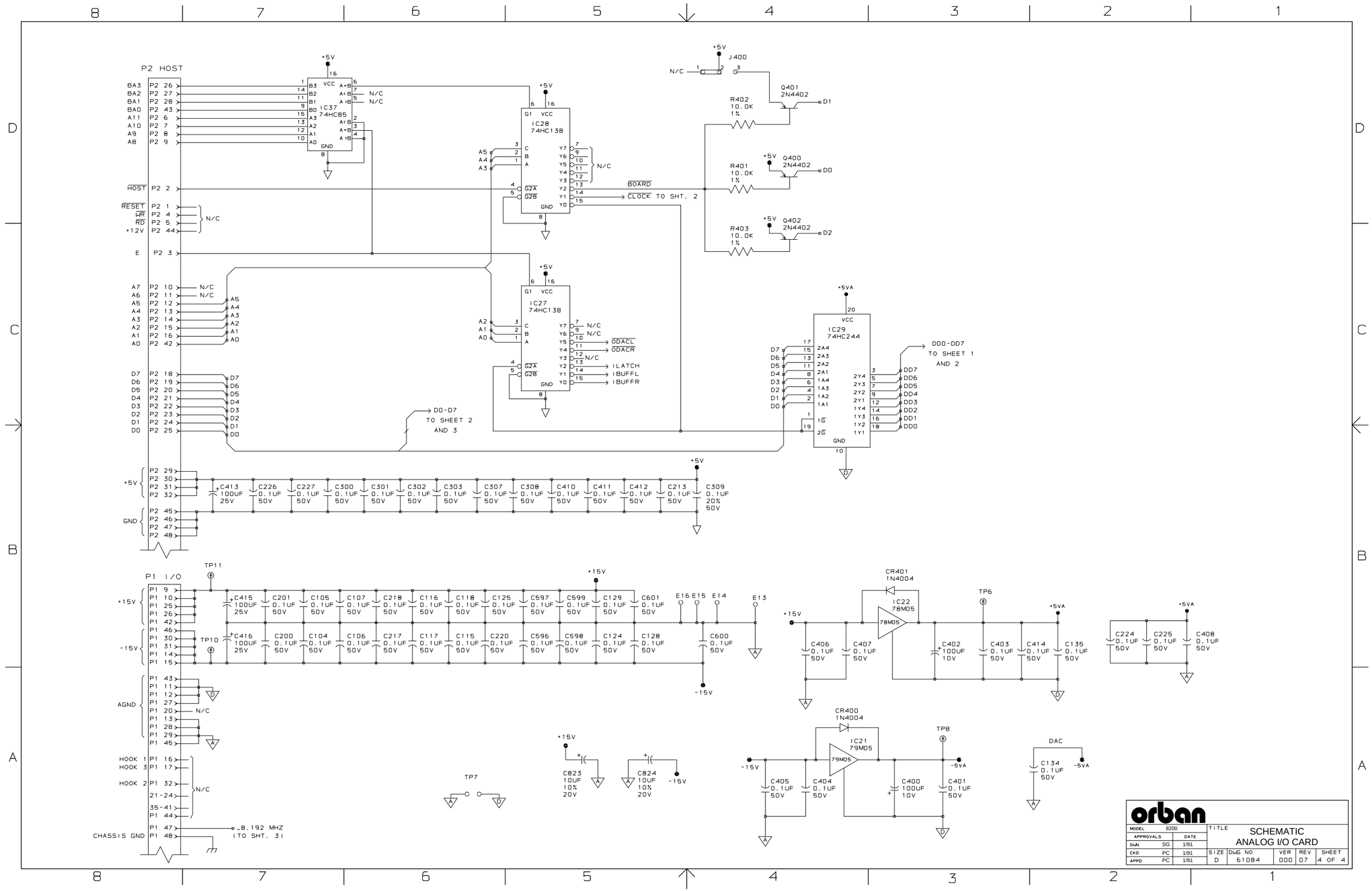
orban			TITLE	PCB ASSEMBLY ANALOG I/O CARD		
MODEL	8200					
APPROVALS		DATE				
DWN	SG	5/91				
CKD	MJ	5/91	SIZE C	DWG NO 31460	VER 000	REV 10
APPD	MJ	5/91				SHEET 1 OF 1


P1 I/O
P1 33 LEFT
P1 2 LEFT OUT -
P1 1 LEFT OUT +
P1 34 RIGHT
P1 19 RIGHT OUT -
P1 18 RIGHT OUT +
P2 HOST
OCLOCK P2 38
OFRAME P2 37
OLDATA P2 35
ORDATA P2 36
IC40-B 74HC132
IC40-C 74HC132
IC40-A 74HC132
IC39 AD1865N
IC12 AD7524
IC17-A TL072
IC16-A TL072
IC26-A TL072
IC26-B TL072
IC24-A TL072
IC24-B TL072
IC25-A TL072
IC25-B TL072
IC38-A TL072
IC38-B TL072
IC23-B LF412
IC23-A LF412
IC5-A LF412
IC5-B LF412
IC4-A LF412
IC4-B LF412
IC6-A LF412
IC6-B LF412
IC13-A 5532
IC13-B 5532
IC1-A 5532
IC1-B 5532
LEFT GAIN TRIM
RIGHT GAIN TRIM
4XFRAMECLOCK FROM SHEET 3
ODACL FROM SHEET 4
ODACR FROM SHEET 4
DD0-DD7 FROM SHEET 4
DE75L FROM SHEET 3
DE50L FROM SHEET 3
DE75R FROM SHEET 3
DE50R FROM SHEET 3
orban
MODEL 8200
APPROVALS DATE
DWN SG 1/91
CKD MJ 1/91
APPD PC 1/91
TITLE
SCHEMATIC
ANALOG I/O CARD
SIZE D
DWG NO 61084
VER 000
REV 07
SHEET 1 OF 4

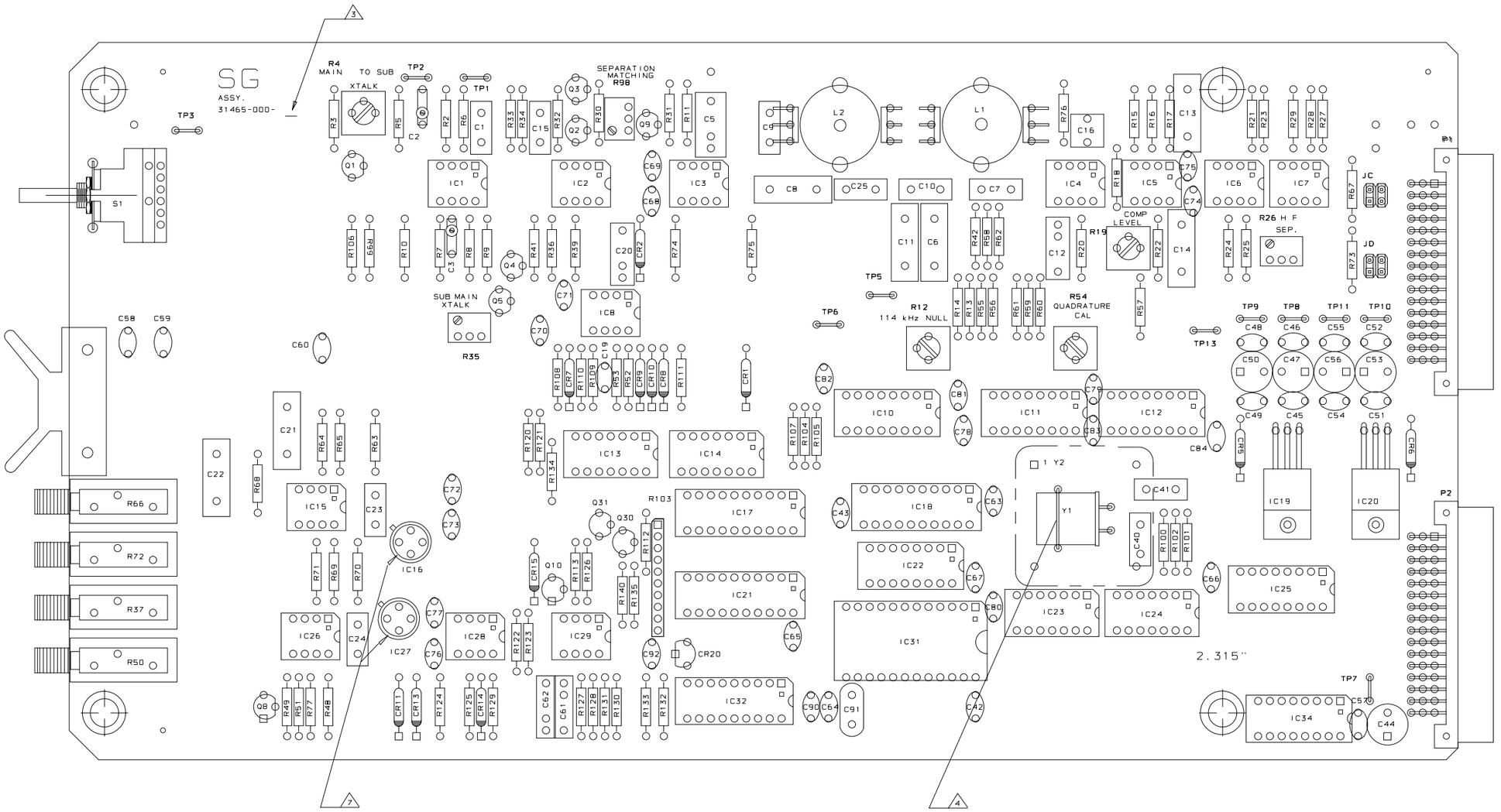

P1 I/O
RIGHT IN + P1 7
RIGHT IN - P1 8
JA
IN
OUT
C216 0.001UF 10%
C617 0.001UF 10%
R200 604Ω
R203 4.99K
R204 4.99K
R205 845Ω
J100-A
J100-B
J101-A
J101-B
R206 100.0K
R207 100.0K
IC15 SSM2017
+15V
-15V
R211 6.34K
TP4
R208 5.62K
RIGHT CAL
CW
R245 100K
R209 5.62K
IC8-A NE5532
R241 249.0K
R210 5.62K
IC9-A NE5532
IC9-B NE5532
C801 100PF 2.5%
R213 5.76K 1%
R232 249.0K
R212 5.62K
C805 100PF 2.5%
R214 5.49K 1%
R242 49.9Ω
R243 49.9Ω
C807 0.01UF 5%,100V
C813 4700PF 5%,50V
C808 0.01UF 5%,100V
+C812 10UF 10% 20V
R244 200.0Ω
TO SHEET 3
SDATA
IBUFFR
IC14 ADG222
R215 249Ω
Q202 J108
R216 511Ω
Q203 J108
IC10-A TL072
R217 47.5K 1%
R218 47.5K 1%
R219 1.05K
R220 1.82K
R221 3.92K
R222 6.34K
+5VA
R201 10.0K 1%
IC7-A LM339
IC7-B LM339
IC7-C LM339
IC7-D LM339
IC19 74HC374
DD0-DD7
ILATCH
N/C
IC20 AD1879
REFR
-VINR
+VINR
SO
S1
CLOCK
RESET
DVDD
32/64
+VINL
-VINL
REFL
AGND
APD
DGND
DGND
WCK
AVSS2
LRCK
SCK
N/C
N/C
DVDD
AVDD1
AVDD2
AVSS1
AVSS1
DATA
32KHZ
2.048 MHZ
FROM SHEET 3
8.192 MHZ
C820 10UF 10% 20V
C819 10UF 10% 20V
C818 10UF 10% 20V
C821 .01UF 20% 25V
C817 10UF 10% 20V
C815 10UF 10% 20V
C822 .01UF 20% 25V
C804 100PF 2.5%
R249 5.36K 1%
R246 5.62K
R253 249.0K
IC44-A NE5532
R254 49.9Ω
C809 0.01UF 5%,100V
C814 4700PF 5%,50V
R231 5.62K
R230 5.62K
LEFT CAL
R257 100K
R250 249.0K
R248 5.90K 1%
R247 5.62K
IC44-B NE5532
R255 49.9Ω
C810 0.01UF 5%,100V
R251 200.0Ω
C811 10UF 10% 20V
P1 I/O
LEFT IN + P1 5
LEFT IN - P1 6
JB
C202 0.001UF 10%
C203 0.001UF 10%
R223 604Ω
R224 4.99K
R225 4.99K
R226 845Ω
J102-A
J102-B
J103-A
J103-B
R227 100.0K
R228 100.0K
R202 10.0K 1%
IC3 SSM2017
R229 6.34K
TP5
R233 249Ω
Q200 J108
R234 511Ω
Q201 J108
IC10-B TL072
R235 47.5K 1%
R236 47.5K 1%
IBUFFL
IC2 ADG222
R237 1.05K
R238 1.82K
R239 3.92K
R240 6.34K
DD0-DD7
orban
MODEL 8200
TITLE
SCHEMATIC
ANALOG I/O CARD
APPROVALS
DRN SG 1/91
CKD PC 1/91
APPD PC 1/91
SIZE D
DWG NO 61084
VER 000
REV 07
SHEET 2 OF 4

R302 10.0K 1%
R303 10.0K 1%
C304 0.010UF 5% 50V MY
IC33-A 74HC04
IC33-B 74HC04
C310 100PF 5% 100V CER
8.192MHZ
8.192 MHZ TO SHEET 2
R304 1.00K 1%
Y1 8.192 MHZ
C306 39PF 500V
C305 39PF 500V
IC33-F 74HC04
-8.192 MHZ TO SHEET 4
R305 22Ω 5%
IC35-A 74HC74
IC35-B 74HC74
4.096MHZ TO SHEET 2
2.048 MHZ TO SHEET 2
IC34-A 74HC74
IC34-B 74HC74
IC32-A 74HC74
IC32-B 74HC74
IC31-A 74HC74
IC31-B 74HC74
32KHZ
TO SHEET 2
128KHZ
IC33-C 74HC04
64KHZ
IC33-D 74HC04
IC42-B 74HC74
N/C
IC16-B TL072
IC17-B TL072
+15V
-15V
IC40-D 74HC132
N/C
SPARE
R300 10.0K 1%
R301 10.0K 1%
IC18-D LM339
DE75R TO SHEET 1
IC18-A LM339
IC18-B LM339
IC18-C LM339
DE50L
DE75L
DE50R
TO SHEET 1
IC30 74HC374
D0
D1
D2
D3
D4
D5
D6
D7
N/C
IC33-E 74HC04
CAL TO SHEET 2
D0-D7 FROM SHEET 4
CLOCK FROM SHEET 4
IC41-A 74HC74
IC41-B 74HC74
IC42-A 74HC74
32KHZ
64KHZ
128KHZ
IC43-A 74HC08
IC43-B 74HC08
IC43-C 74HC08
IC43-D 74HC08
IC36 74HC244
SDATA
2.048 MHZ
4XFRAMECLOCK TO SHT. 1
P2 HOST
P2 41 4XFRAMECLOCK
P2 40 2XFRAMECLOCK
P2 39 1XFRAMECLOCK
P2 34 IFRAME
P2 17 IDATA
P2 33 ICLOCK
N/C

orban			
MODEL	8200	TITLE	SCHEMATIC ANALOG I/O CARD
APPROVALS	DATE		
DWN SG	1/91		
CKD PC	1/91	SIZE D / DWG NO 61084 / VER 000 / REV 07 / SHEET 3 OF 4	
APPD PC	1/91		



MODEL	8200
TITLE	SCHEMATIC ANALOG I/O CARD
APPROVALS	DATE
DWN SG	1/91
CKD PC	1/91
APPD PC	1/91
SIZE	D
DWG NO	61084
VER	000
REV	07
SHEET	4 OF 4



7. INSTALL AKG P/N 15051-000-01 BEFORE SOLDER FLOWING

6. ON FAB SIDE OF BOARD ADD (1) COAX CABLE FROM E1 TO E4 WITH E5 AS GND
AND ADD (1) COAX CABLE FROM E3 TO E2 WITH E6 AS GND

5. Y2 SHOWN FOR FUTURE USE ONLY

4. SOLDER RETAINING WIRE TO CRYSTAL.

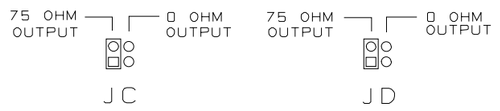
3. MARK ASSEMBLY REVISION LEVEL IN SPACE PROVIDED

2. REFERENCE SCHEMATIC DRAWING NO. 61085.

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES.
POS. SIDE OF CAPS., PIN 1 OF ICS

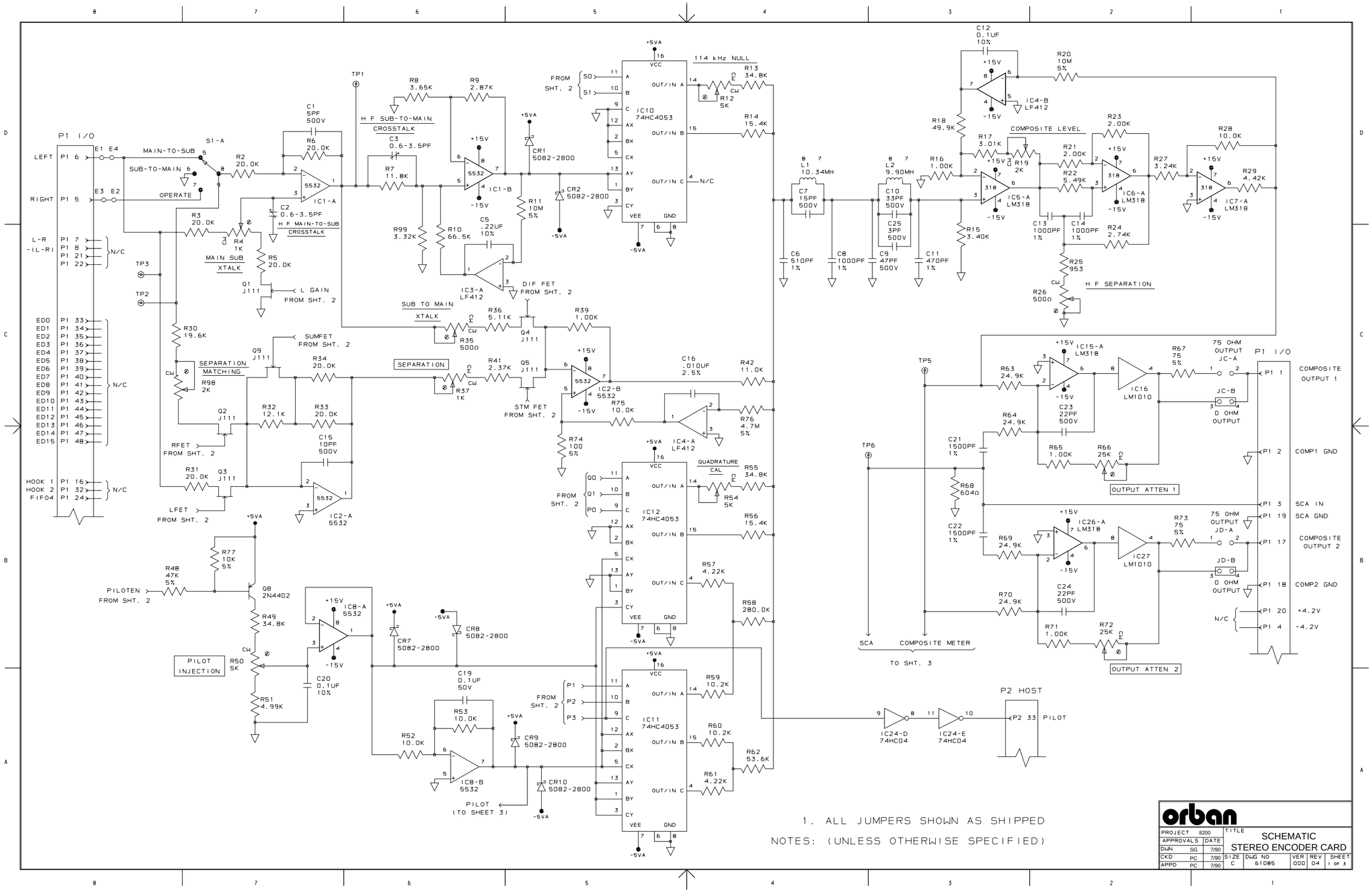
NOTES: (UNLESS OTHERWISE SPECIFIED)

COMPONENT SIDE



JUMPERS
(SHOWN AS SHIPPED)

orban							
MODEL 8200			TITLE	PCB ASSEMBLY STEREO GENERATOR			
APPROVALS		DATE					
DWN	SG	8/91					
CKD	MJ	8/91	SIZE C	DWG NO 31465	VER 000	REV 06	SHEET 1 OF 1
APPD	MJ	8/91					


P1 I/O
LEFT P1 6
RIGHT P1 5
E1 E4
E3 E2
MAIN-TO-SUB
SUB-TO-MAIN
OPERATE
S1-A
R2 20.0K
R3 20.0K
R4 1K
R5 20.0K
MAIN SUB XTALK
C1 5PF 500V
C2 0.6-3.5PF
H F MAIN-TO-SUB CROSSTALK
IC1-A 5532
TP1
R6 20.0K
R8 3.65K
R9 2.87K
H F SUB-TO-MAIN CROSSTALK
C3 0.6-3.5PF
R7 11.8K
IC1-B 5532
+15V
-15V
+5VA
CR1 5082-2800
CR2 5082-2800
-5VA
R99 3.32K
R10 66.5K
R11 10M 5%
C5 .22UF 10%
IC3-A LF412
DIF FET FROM SHT. 2
Q1 J111
L GAIN FROM SHT. 2
TP3
TP2
L-R P1 7
-(L-R) P1 8
P1 21
P1 22
N/C
ED0 P1 33
ED1 P1 34
ED2 P1 35
ED3 P1 36
ED4 P1 37
ED5 P1 38
ED6 P1 39
ED7 P1 40
ED8 P1 41
ED9 P1 42
ED10 P1 43
ED11 P1 44
ED12 P1 45
ED13 P1 46
ED14 P1 47
ED15 P1 48
HOOK 1 P1 16
HOOK 2 P1 32
FIF04 P1 24
R30 19.6K
SEPARATION MATCHING
R98 2K
Q9 J111
SUMFET FROM SHT. 2
R34 20.0K
Q2 J111
R32 12.1K
R33 20.0K
C15 10PF 500V
RFET FROM SHT. 2
R31 20.0K
Q3 J111
LFET FROM SHT. 2
IC2-A 5532
SUB TO MAIN XTALK
R35 500Ω
R36 5.11K
Q4 J111
R39 1.00K
SEPARATION
R37 1K
R41 2.37K
Q5 J111
STM FET FROM SHT. 2
IC2-B 5532
R75 10.0K
C16 .010UF 2.5%
R42 11.0K
R74 100 5%
IC4-A LF412
R76 4.7M 5%
FROM SHT. 2
SO
S1
IC10 74HC4053
VCC
GND
VEE
114 kHz NULL
R13 34.8K
R12 5K
R14 15.4K
OUT/IN A
OUT/IN B
OUT/IN C
N/C
C7 15PF 500V
C6 510PF 1%
C8 1000PF 1%
L1 10.34MH
L2 9.90MH
C10 33PF 500V
C25 3PF 500V
C9 47PF 500V
C11 470PF 1%
R16 1.00K
R15 3.40K
C12 0.1UF 10%
R20 10M 5%
R18 49.9K
R17 3.01K
COMPOSITE LEVEL
R19 2K
IC4-B LF412
R23 2.00K
R21 2.00K
R22 5.49K
IC5-A LM318
IC6-A LM318
R28 10.0K
R27 3.24K
R29 4.42K
IC7-A LM318
C13 1000PF 1%
C14 1000PF 1%
R24 2.74K
R25 953
R26 500Ω
H F SEPARATION
TP5
IC15-A LM318
R63 24.9K
C23 22PF 500V
IC16 LM1010
R67 75 5%
75 OHM OUTPUT JC-A
JC-B
0 OHM OUTPUT
COMPOSITE OUTPUT 1
R64 24.9K
C21 1500PF 1%
R65 1.00K
R66 25K
OUTPUT ATTEN 1
R68 604Ω
C22 1500PF 1%
IC26-A LM318
R69 24.9K
C24 22PF 500V
IC27 LM1010
R73 75 5%
75 OHM OUTPUT JD-A
JD-B
0 OHM OUTPUT
R70 24.9K
R71 1.00K
R72 25K
OUTPUT ATTEN 2
TP6
SCA
COMPOSITE METER
TO SHT. 3
P1 1 COMPOSITE OUTPUT 1
P1 2 COMP1 GND
P1 3 SCA IN
P1 19 SCA GND
P1 17 COMPOSITE OUTPUT 2
P1 18 COMP2 GND
P1 20 +4.2V
P1 4 -4.2V
N/C
PILOTEN FROM SHT. 2
Q8 2N4402
R48 47K 5%
R49 34.8K
R50 5K
PILOT INJECTION
R51 4.99K
R77 10K 5%
IC8-A 5532
C20 0.1UF 10%
CR7 5082-2800
CR8 5082-2800
C19 0.1UF 50V
R53 10.0K
R52 10.0K
IC8-B 5532
CR9 5082-2800
CR10 5082-2800
PILOT (TO SHEET 3)
FROM SHT. 2
P1
P2
P3
IC11 74HC4053
R59 10.2K
R60 10.2K
R62 53.6K
R61 4.22K
QUADRATURE CAL
R55 34.8K
R54 5K
R56 15.4K
R57 4.22K
R58 280.0K
Q0
Q1
P0
IC12 74HC4053
IC24-D 74HC04
IC24-E 74HC04
P2 HOST
P2 33 PILOT
1. ALL JUMPERS SHOWN AS SHIPPED
NOTES: (UNLESS OTHERWISE SPECIFIED)
orban
PROJECT 8200
TITLE
SCHEMATIC
STEREO ENCODER CARD
APPROVALS
DATE
DWN SG 7/90
CKD PC 7/90
APPD PC 7/90
SIZE C
DWG NO 61085
VER 000
REV 04
SHEET 1 OF 3

P2 HOST

WR P2 4
RD P2 5
OLDATA P2 35
ORDATA P2 36
OFRAME P2 37
OCLOCK P2 38
1XFRAMECLOCK P2 39
2XFRAMECLOCK P2 40
4XFRAMECLOCK P2 41
+12V P2 44 — N/C

Y2 4.864 MHZ — N/C

IC24-B 74HC04 — R101 1.0K 5% — IC24-A 74HC04

R100 33.2K

Y1 4.864 MHZ

C40 39PF 500V

C41 39PF 500V

DGND

R102 0Ω

IC23-A 74HC74

IC23-B 74HC74

IC22 CD4520BE

IC31 32K PROM

IC18 74HC374 — S0 S1 Q0 Q1 P0 P1 P2 P3 — TO SHT. 1

SPARE — IC24-F 74HC04

CR11 1N4148 — PILOTEN TO SHT. 1

IC13-C LM339 — COMP FET — R112 20K 5% — TO SHEET 3

IC13-D LM339 — PILOT FET — R113 20K 5%

IC14-A LM339 — LFET — R104 20K 5%

IC14-B LM339 — RFET — R105 20K 5%

IC14-C LM339 — L GAIN — R106 20K 5%

IC14-D LM339 — SUMFET — R107 20K 5%

IC13-A LM339 — STM FET — R108 20K 5%

IC13-B LM339 — DIF FET — R109 20K 5%

TO SHT. 1

R110 100K 5%

R111 100K 5%

BA3 P2 26
BA2 P2 27
BA1 P2 28
BA0 P2 43
A11 P2 6
A10 P2 7
A9 P2 8
A8 P2 9

IC25 74HC85

RESET P2 1 — N/C
HOST P2 2 — N/C

E P2 3 — IC24-C 74HC04

A0 P2 42
A1 P2 16
A2 P2 15
— N/C

IC34 74HC138

A5 A4 A3

Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 — N/C

METER

BUSY (FROM SHEET 3)

P2 14 — A3
P2 13 — A4
P2 12 — A5 — A3-A5

A6 P2 11
A7 P2 10
— N/C

P2 17 — N/C

P2 18 — D7
P2 19 — D6
P2 20 — D5
P2 21 — D4
P2 22 — D3
P2 23 — D2
P2 24 — D1
P2 25 — D0

P2 34 — N/C — D0-D7

R103-A 100K
R103-B 100K
R103-C 100K
R103-D 100K
R103-E 100K
R103-F 100K
R103-G 100K
R103-H 100K

IC21 74HC244

IC17 74HC374 — D0 D1 D2 D3 D4 D5 D6 D7 — 12 PROM — 19 SROM

C58 0.1UF 50V

C59 0.1UF 50V

C60 0.1UF 50V

S1-B

OPERATE

SUB-TO-MAIN

MAIN-TO-SUB

D0-D7

P2 29
P2 30
P2 31
P2 32

TP7

C44 100UF 25V

C42 0.1UF 50V

C43 0.1UF 50V

C57 0.1UF 50V

C63 0.1UF 50V

C65 0.1UF 50V

C66 0.1UF 50V

C67 0.1UF 50V

C80 0.1UF 50V

P2 45
P2 46
P2 47
P2 48

C64 0.1UF 50V

+5V +5VA +15V -15V

orban

PROJECT 8200		TITLE
APPROVALS	DATE	SCHEMATIC
DWN SG	7/90	STEREO ENCODER CARD
CKD PC	7/90	SIZE C — DWG NO 61085 — VER 000 — REV 04 — SHEET 2 OF 3
APPD PC	7/90	

SPARE

IC3-B LF412

FROM SHT. 1

COMP FET

COMPOSITE METER

SCA

PILOT FET

PILOT

1.2V

Q30 J111

Q31 J111

R120 100.0K

R121 100.0K

R134 4.12K

R135 7.15K

R140 402.0K

R122 49.9K

R123 10.0K

R124 105.0K

R125 93.1K

R126 2.0K 5%

CR13 1N4148

CR14 1N4148

CR15 1N4148

IC28-A LF412

IC28-B LF412

IC29-A LF412

IC29-B LF412

+15V

-15V

N/C

Q10 2N4400

C61 0.01UF 10%

C62 0.01UF 10%

R127 22M 5%

R128 22M 5%

R129 100 5%

R130 100.0K

R131 5.62K

METER (FROM SHEET 2)

D0-D7 (FROM SHEET 2)

IC32 AD7576

Vdd MODE AGND AIN CLK CS RD D7 D6 D5 D4 D3 D2 D1 D0 Vref BUSY DGND

+5V

+5VA

C90 0.1UF 25V

C91 150PF 5%

C92 0.1UF 25V

R132 150.0K

R133 3.3K 5%

1.2V

CR20 LM385 1.2V

BUSY (TO SHEET 2)

P1 I/O

+15V: P1 9, P1 10, P1 25, P1 26

CHASSIS GND: P1 23

GND: P1 11, P1 12, P1 13, P1 27, P1 28, P1 29

-15V: P1 14, P1 15, P1 30, P1 31

SHIELD

TP8 TP9 TP10 TP11 TP13

CR5 1N4004

CR6 1N4004

IC19 78M05

IC20 79M05

-5VA

C45 0.1UF 50V

C46 0.1UF 50V

C47 100UF 25V

C48 0.1UF 50V

C49 0.1UF 50V

C50 100UF 25V

C51 0.1UF 50V

C52 0.1UF 50V

C53 100UF 25V

C54 0.1UF 50V

C55 0.1UF 50V

C56 100UF 25V

C68 0.1UF 50V

C69 0.1UF 50V

C70 0.1UF 50V

C71 0.1UF 50V

C72 0.1UF 50V

C73 0.1UF 50V

C74 0.1UF 50V

C75 0.1UF 50V

C76 0.1UF 50V

C77 0.1UF 50V

C78 0.1UF 50V

C79 0.1UF 50V

C81 0.1UF 50V

C82 0.1UF 50V

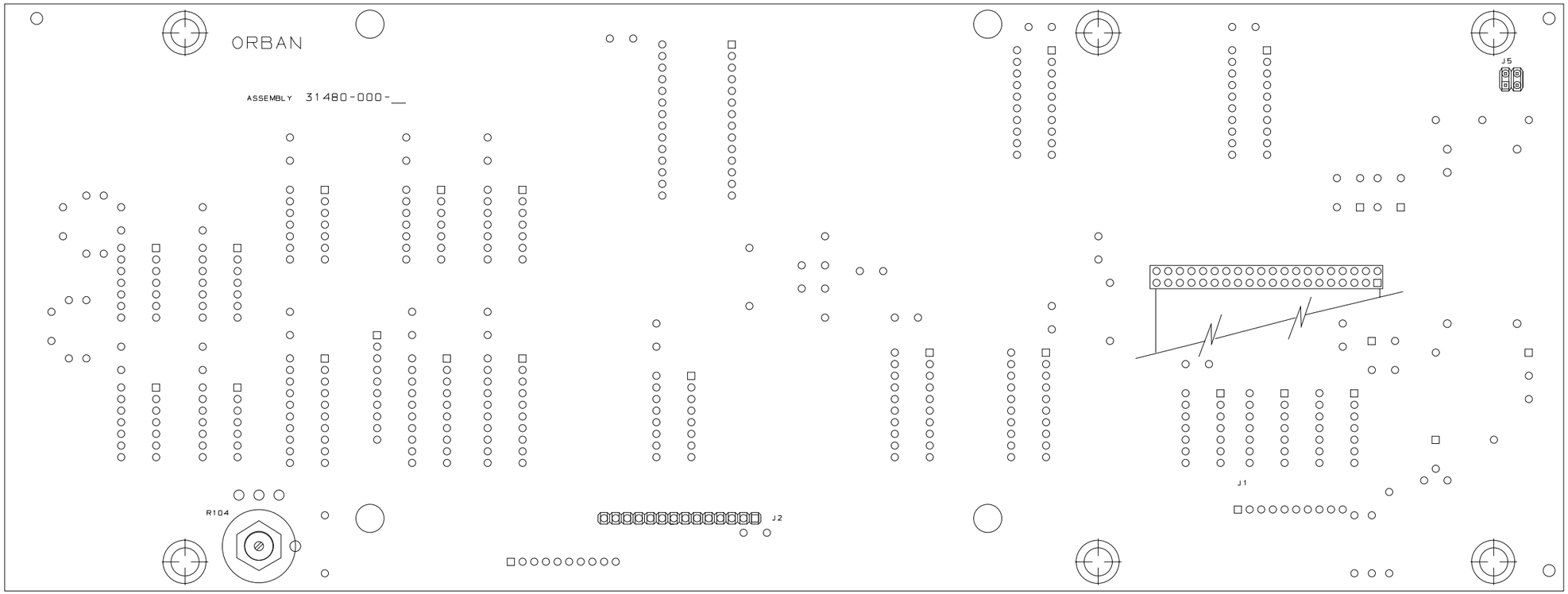
C83 0.1UF 50V

C84 0.1UF 50V

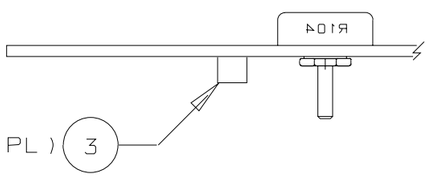
orban

PROJECT 8200		TITLE	SCHEMATIC STEREO ENCODER CARD				
APPROVALS	DATE						
DWN SG	7/90						
CKD PC	7/90	SIZE C	DWG NO 61085	VER 000	REV 04	SHEET 3 OF 3	
APPD PC	7/90						

This Page Intentionally Left Blank.

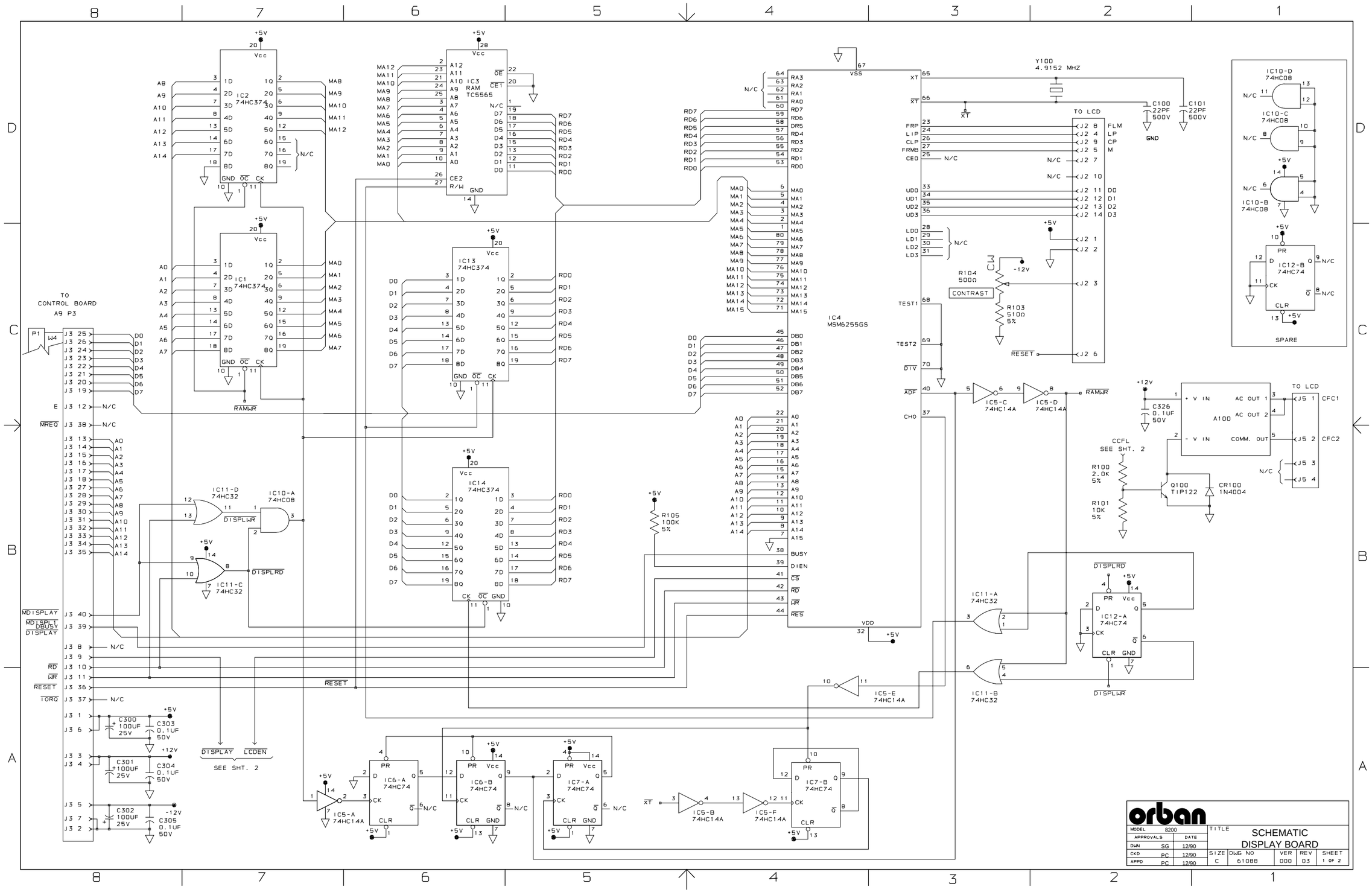


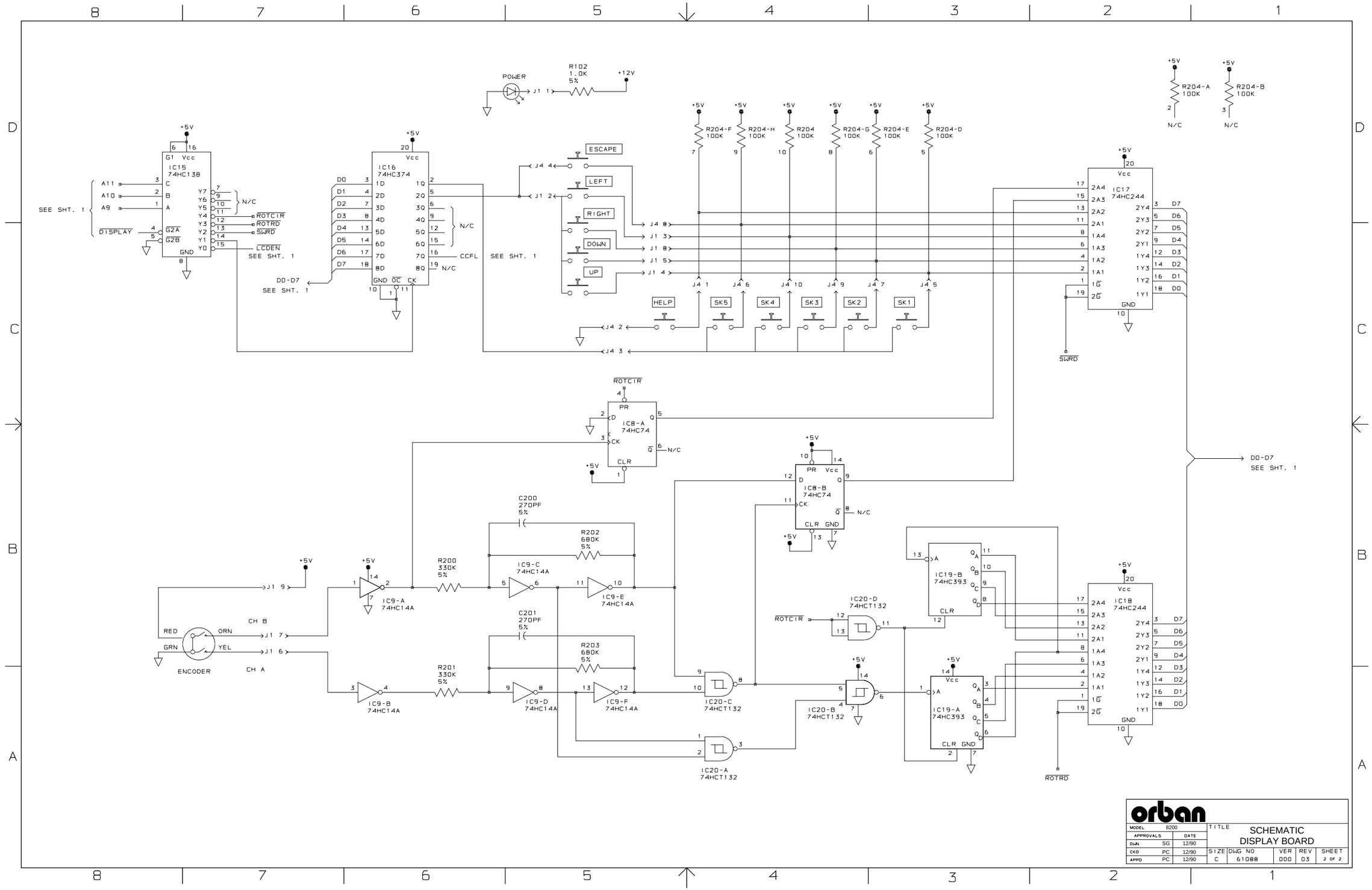
COMPONENT SIDE



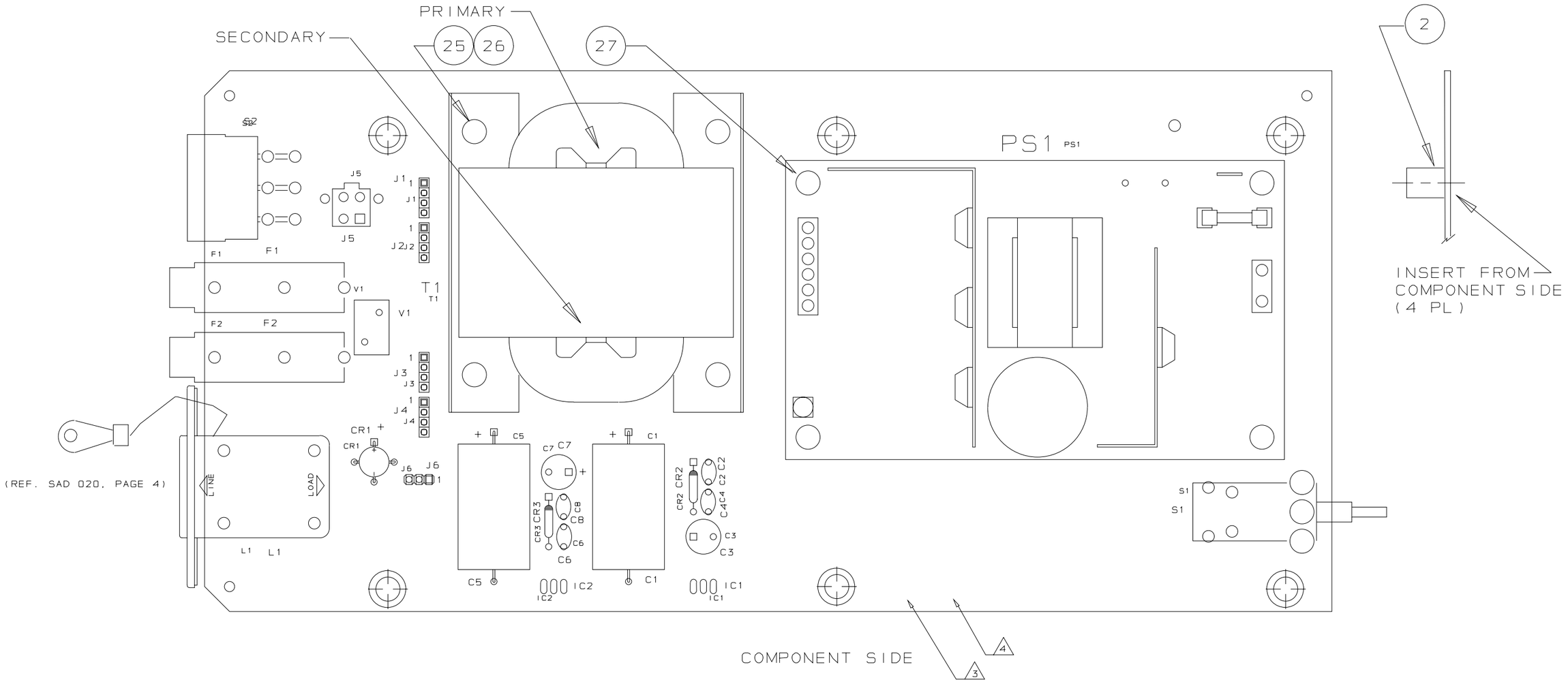
STANDOFF (4 PL) 3

orban								
MODEL 8200			TITLE PCB ASSEMBLY MAIN DISPLAY BOARD					
APPROVALS	DATE							
DWN SG	3/91							
CKD MJ	3/91	SIZE	DWG NO	VER	REV	SHEET		
APPD MJ	3/91	C	31480	000	05	1 OF 1		


TO CONTROL BOARD A9 P3
P1
W4
J3 25
J3 26
J3 24
J3 23
J3 22
J3 21
J3 20
J3 19
J3 12
J3 38
J3 13
J3 14
J3 15
J3 16
J3 17
J3 18
J3 27
J3 28
J3 29
J3 30
J3 31
J3 32
J3 33
J3 34
J3 35
J3 40
J3 39
J3 8
J3 9
J3 10
J3 11
J3 36
J3 37
J3 1
J3 6
J3 3
J3 4
J3 5
J3 7
J3 2
D0
D1
D2
D3
D4
D5
D6
D7
E
MREQ
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
N/C
MDISPLAY
MDISPLL
DBUSY
DISPLAY
RD
WR
RESET
IORQ
+5V
+12V
-12V
C300 100UF 25V
C303 0.1UF 50V
C301 100UF 25V
C304 0.1UF 50V
C302 100UF 25V
C305 0.1UF 50V
IC2 74HC374
IC1 74HC374
RAMWR
IC3 RAM TC5565
IC13 74HC374
IC14 74HC374
IC11-D 74HC32
IC10-A 74HC08
IC11-C 74HC32
DISPLWR
DISPLRD
DISPLAY
LCDEN
SEE SHT. 2
IC4 MSM6255GS
VSS
VDD
BUSY
DIEN
CS
RD
WR
RES
RA3
RA2
RA1
RA0
DR5
DR4
DR3
DR2
DR1
DR0
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Y100 4.9152 MHZ
XT
C100 22PF 500V
C101 22PF 500V
GND
TO LCD
FRP
LIP
CLP
FRMB
CE0
UD0
UD1
UD2
UD3
LD0
LD1
LD2
LD3
FLM
LP
CP
M
J2 8
J2 4
J2 9
J2 5
J2 7
J2 10
J2 11
J2 12
J2 13
J2 14
J2 1
J2 2
J2 3
J2 6
R104 500Ω
CONTRAST
R103 5100 5%
TEST1
TEST2
DIV
ADF
CH0
IC5-C 74HC14A
IC5-D 74HC14A
IC10-D 74HC08
IC10-C 74HC08
IC10-B 74HC08
IC12-B 74HC74
SPARE
C326 0.1UF 50V
A100
AC OUT 1
AC OUT 2
- V IN
COMM. OUT
J5 1
J5 2
J5 3
J5 4
CFC1
CFC2
CCFL SEE SHT. 2
R100 2.0K 5%
R101 10K 5%
Q100 TIP122
CR100 1N4004
R105 100K 5%
IC11-A 74HC32
IC12-A 74HC74
IC11-B 74HC32
IC5-E 74HC14A
IC6-A 74HC74
IC6-B 74HC74
IC7-A 74HC74
IC7-B 74HC74
IC5-A 74HC14A
IC5-B 74HC14A
IC5-F 74HC14A
orban
MODEL 8200
TITLE SCHEMATIC DISPLAY BOARD
APPROVALS DATE
DWN SG 12/90
CKD PC 12/90
APPD PC 12/90
SIZE C
DWG NO 61088
VER 000
REV 03
SHEET 1 OF 2



orban			
MODEL	8200	TITLE	SCHEMATIC DISPLAY BOARD
APPROVALS	DATE		
DWN SG	12/90		
CKD PC	12/90	SIZE C	DWG NO 61088
APPD PC	12/90	VER 000	REV 03
		SHEET	2 OF 2



4 MARK VERSION NUMBER IN SPACE PROVIDED (CIRCUIT SIDE).

3 MARK ASSEMBLY REVISION LEVEL IN SPACE (PROVIDED

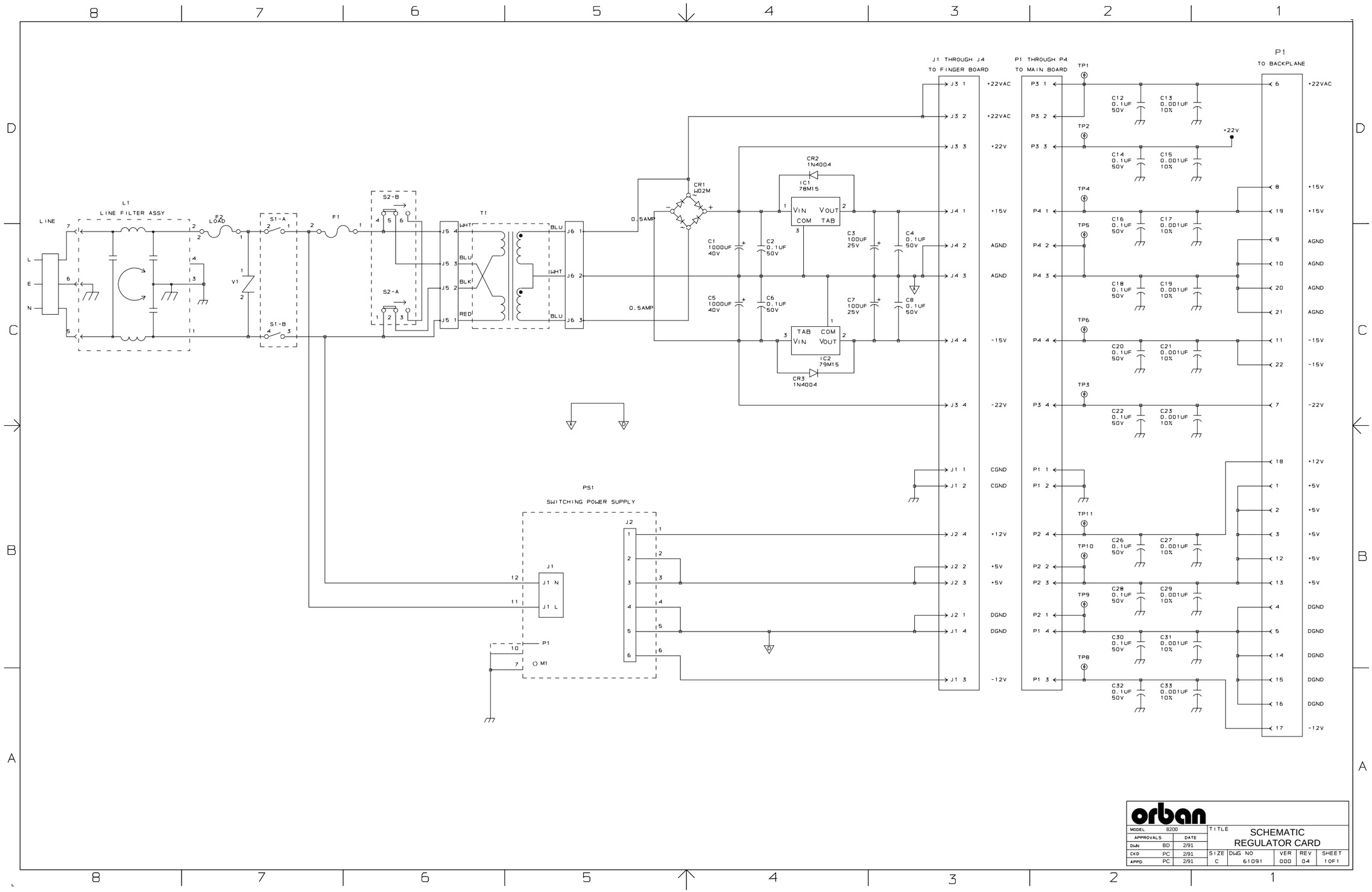
2. REFERENCE SCHEMATIC DRAWING NO. 61091.

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS

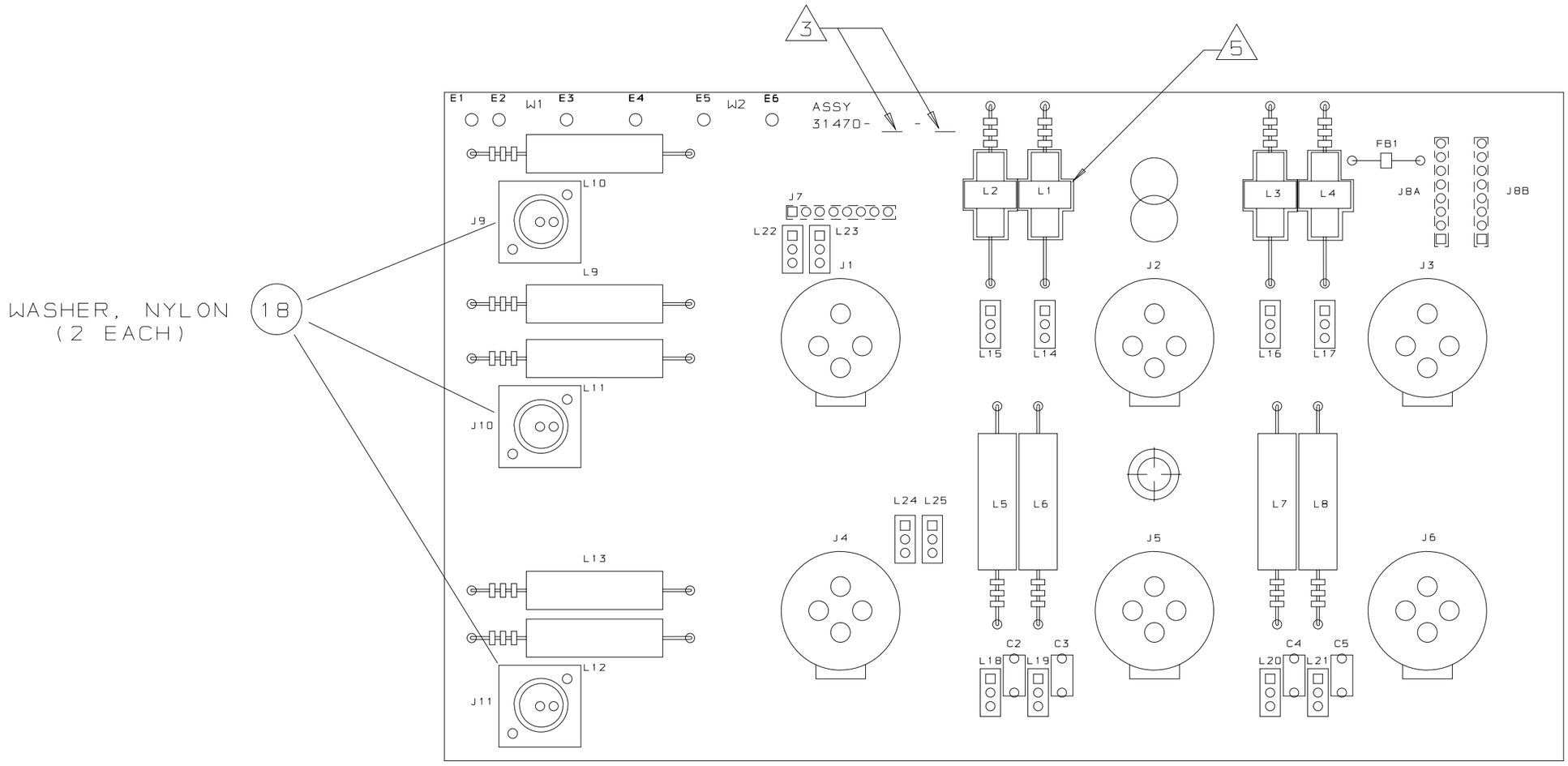
NOTES: (UNLESS OTHERWISE SPECIFIED)

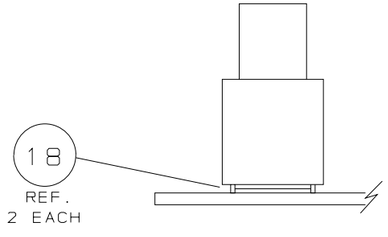
orban

MODEL	8200	TITLE	PCB ASSEMBLY REGULATOR CARD
APPROVALS	DATE		
DWN BD	2/91		
CKD MJ	9/91	SIZE C	DWG NO 31495 / VER 000 / REV 05 / SHEET 1 OF 1
APPD MJ	9/91		



orban			TITLE	SCHEMATIC REGULATOR CARD			
MODEL	8200						
APPROVALS		DATE					
DWN	BD	2/91					
CKD	PC	2/91	SIZE	DWG NO	VER	REV	SHEET
APPD	PC	2/91	C	61091	000	04	1OF1





5. INSTALL 1/2" DIA X 1" SHRINK TUBE TO L1, L2, L3 &L4 BEFORE SOLDER FLOWING.

4. J7, J8A & J8B TO BE MOUNTED FROM SOLDER SIDE OF BOARD.

3. MARK ASSEMBLY VERSION AND REVISION LEVEL IN SPACE PROVIDED

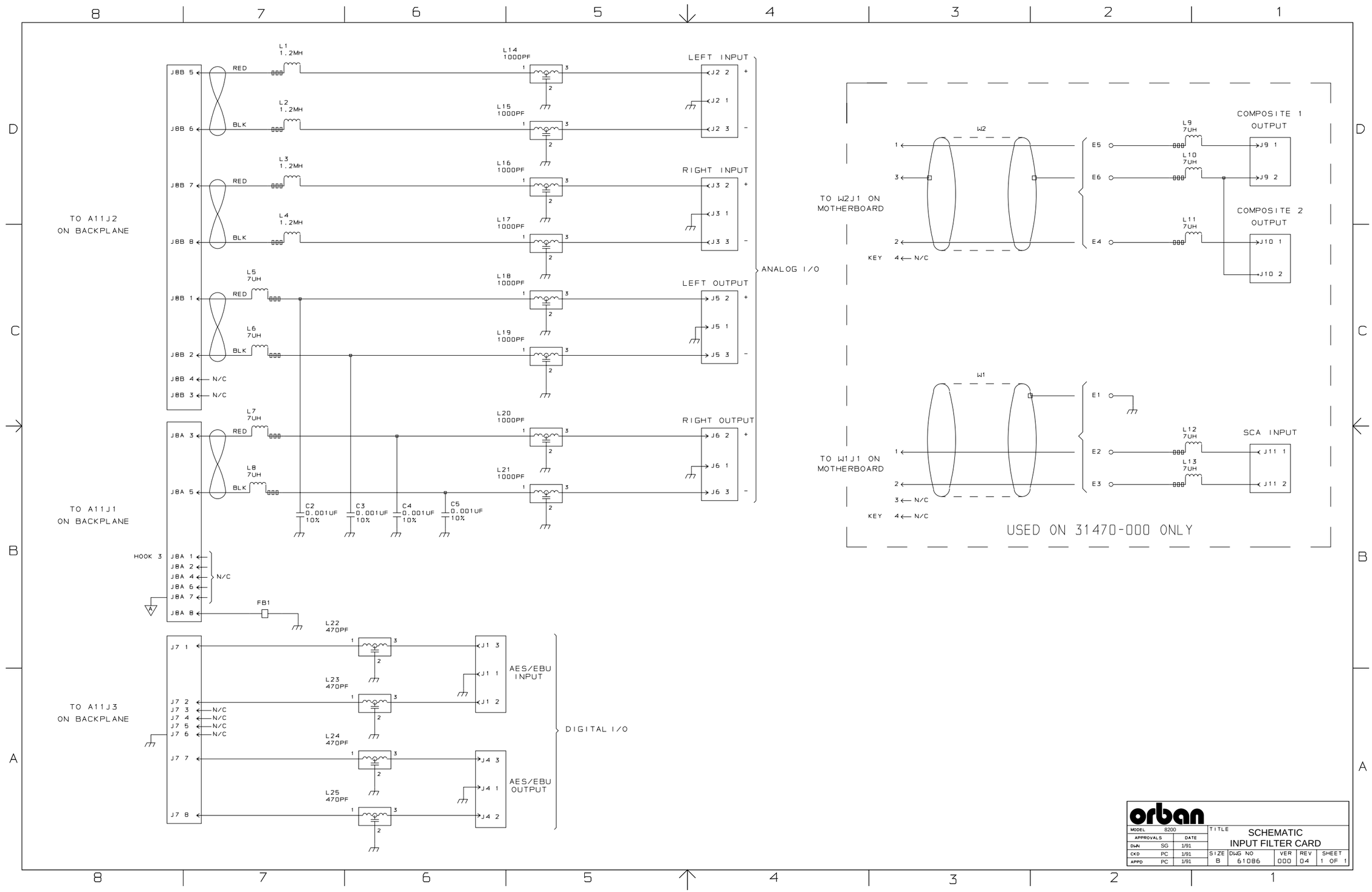
2. REFERENCE SCHEMATIC DRAWING NO.

1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

MODEL	8200		TITLE	PCB ASSEMBLY INPUT FILTER CARD			
APPROVALS		DATE					
DWN	BD	10/91					
CKD	MJ	10/91	SIZE	DWG NO	VER	REV	SHEET
APPD	MJ	10/91	C	31470	000	04	1 OF 1


TO A11J2
ON BACKPLANE
J8B 5
J8B 6
J8B 7
J8B 8
J8B 1
J8B 2
J8B 4 ← N/C
J8B 3 ← N/C
RED
BLK
L1 1.2MH
L2 1.2MH
L3 1.2MH
L4 1.2MH
L5 7UH
L6 7UH
L7 7UH
L8 7UH
L14 1000PF
L15 1000PF
L16 1000PF
L17 1000PF
L18 1000PF
L19 1000PF
L20 1000PF
L21 1000PF
LEFT INPUT
RIGHT INPUT
LEFT OUTPUT
RIGHT OUTPUT
J2 2
J2 1
J2 3
J3 2
J3 1
J3 3
J5 2
J5 1
J5 3
J6 2
J6 1
J6 3
ANALOG I/O
J8A 3
J8A 5
C2 0.001UF 10%
C3 0.001UF 10%
C4 0.001UF 10%
C5 0.001UF 10%
TO A11J1
ON BACKPLANE
HOOK 3
J8A 1
J8A 2
J8A 4
J8A 6
J8A 7
J8A 8
N/C
FB1
TO A11J3
ON BACKPLANE
J7 1
J7 2
J7 3 ← N/C
J7 4 ← N/C
J7 5 ← N/C
J7 6 ← N/C
J7 7
J7 8
L22 470PF
L23 470PF
L24 470PF
L25 470PF
J1 3
J1 1
J1 2
J4 3
J4 1
J4 2
AES/EBU INPUT
AES/EBU OUTPUT
DIGITAL I/O
TO W2J1 ON MOTHERBOARD
W2
1
3
2
KEY 4 ← N/C
E5
E6
E4
L9 7UH
L10 7UH
L11 7UH
COMPOSITE 1 OUTPUT
COMPOSITE 2 OUTPUT
J9 1
J9 2
J10 1
J10 2
TO W1J1 ON MOTHERBOARD
W1
1
2
3 ← N/C
KEY 4 ← N/C
E1
E2
E3
L12 7UH
L13 7UH
SCA INPUT
J11 1
J11 2
USED ON 31470-000 ONLY
orban
MODEL 8200
APPROVALS DATE
DWN SG 1/91
CKD PC 1/91
APPD PC 1/91
TITLE
SCHEMATIC
INPUT FILTER CARD
SIZE B
DWG NO 61086
VER 000
REV 04
SHEET 1 OF 1

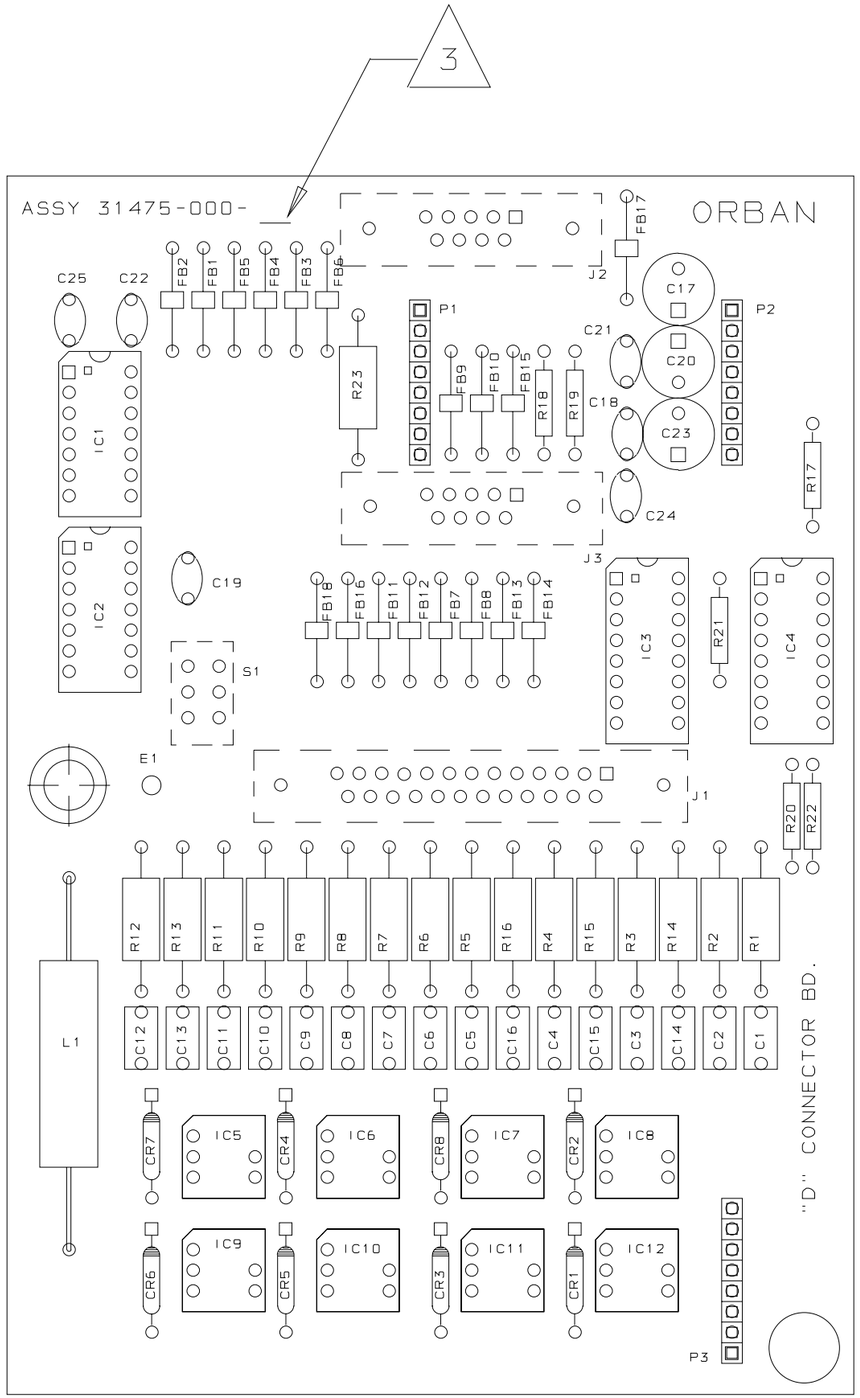
4. S1, J1, J2 & J3 ARE INSTALLED ON CIRCUIT SIDE OF BOARD.

3. MARK ASSEMBLY REVISION LEVEL IN SPACE PROVIDED

2. REFERENCE SCHEMATIC DRAWING NO.

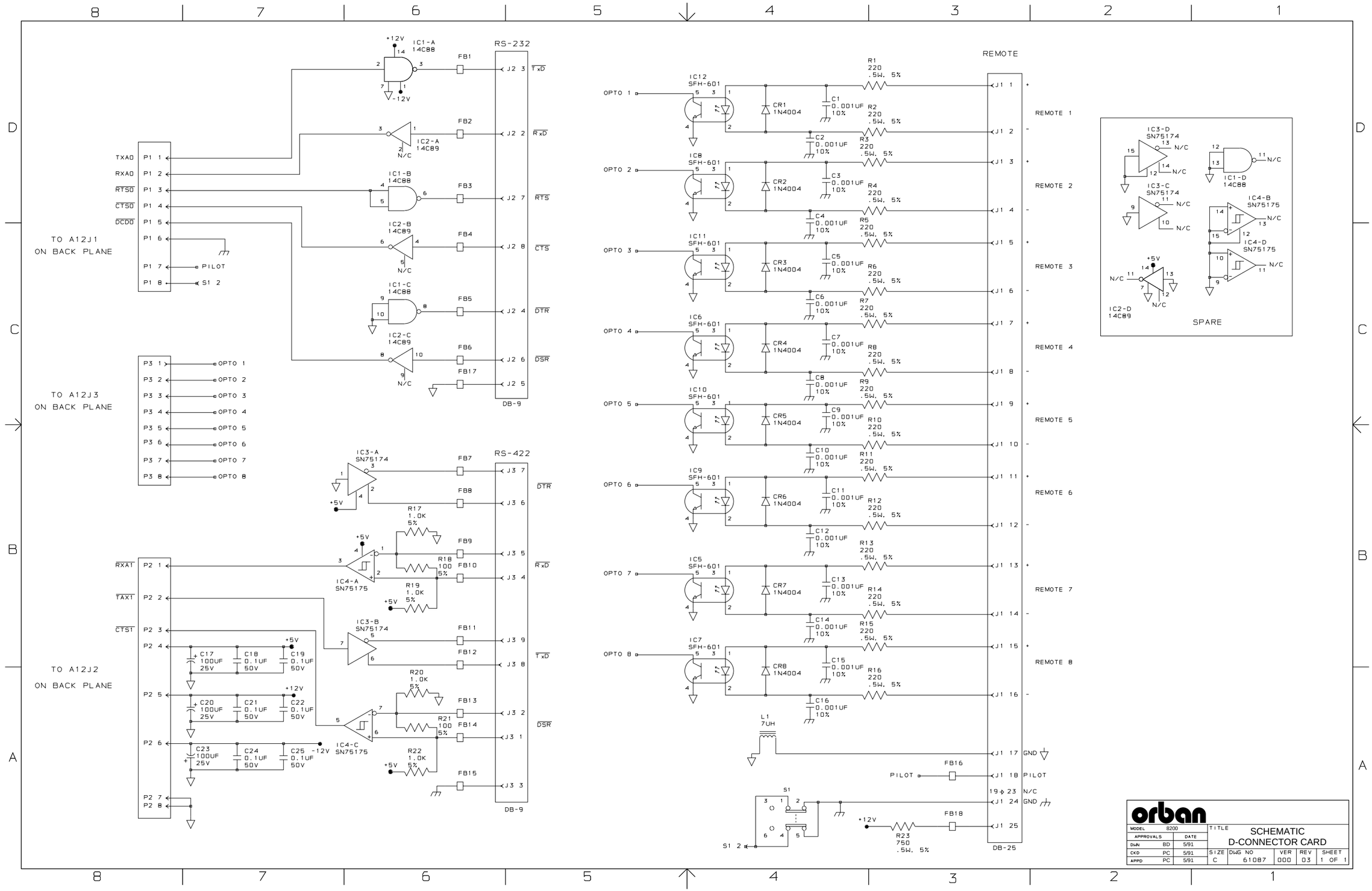
1. SQUARE PADS INDICATE PIN 1 OF CONNECTORS, CATHODE OF DIODES, POS. SIDE OF CAPS., PIN 1 OF ICS

NOTES: (UNLESS OTHERWISE SPECIFIED)



COMPONENT SIDE

orban						
MODEL 8200			TITLE	PCB ASSEMBLY D-CONNECTOR CARD		
APPROVALS	DATE					
DWN BD	5/91					
CKD MJ	5/91	SIZE C	DWG NO 31475	VER 000	REV 03	SHEET 1 OF 1
APPD MJ	5/91					



orban			
MODEL	8200	TITLE	SCHEMATIC D-CONNECTOR CARD
APPROVALS	DATE		
DsN	BD 5/01		
CKD	PC 5/01		
APPD	PC 5/01	SIZE C / DWG NO 61087 / VER 000 / REV 03 / SHEET 1 OF 1	

This Page Intentionally Left Blank.

Abbreviations

Some of the abbreviations used in this manual may not be familiar to all readers:

A/D (or A to D)	analog-to-digital converter
AES	Audio Engineering Society
AGC	automatic gain control
A-I	analog input
A-O	analog output
AT	“advanced technology” — IBM PC with 80286 or higher processor
BAL	balance
BBC	British Broadcasting Corporation
BNC	a type of RF connector
CALIB	calibrate
CIT	composite isolation transformer
CMOS	complementary metal-oxide semiconductor
COM	serial data communications port
DA (or D to A)	digital-to-analog converter
dBm	decibel power measurement. 0dBm = 1mW applied to a specified load. In audio, the load is usually 600Ω.
dBu	decibel voltage measurement. 0dBu = 0.775V RMS. For this application, the dBm-into-600Ω scale on voltmeters can be read as if it were calibrated in dBu.
DI	digital input
DJ	disk jockey, an announcer who plays records in a club or on the air
DO	digital output
DOS	Microsoft disk operating system for IBM PC
DSP	digital signal processor
EBU	European Broadcasting Union
EBS	Emergency Broadcasting System (U.S.A.)
EMI	electromagnetic interference
ESC	escape
FCC	Federal Communications Commission (USA regulatory agency)
FDNR	frequency-dependent negative resistor — an element used in rc-active filters
FET	field effect transistor
FFT	fast Fourier transform
FIFO	first-in, first-out
G/R	gain reduction
HF	high-frequency

HP	high-pass
IC	integrated circuit
IM	intermodulation (or “intermodulation distortion”)
I/O	input/output
JFET	junction field effect transistor
LC	inductor/capacitor
LCD	liquid crystal display
LED	light-emitting diode
LF	low-frequency
LP	low-pass
LVL	level
MHF	midrange/high-frequency
MLF	midrange/low-frequency
MOD	modulation
N&D	noise and distortion
N/C	no connection
OSHOOT	overshoot
PC	IBM-compatible personal computer
PCM	pulse code modulation
PPM	peak program meter
RAM	random-access memory
RC	resistor/capacitor
REF	reference
RF	radio frequency
RFI	radio-frequency interference
RMS	root-mean-square
ROM	read-only memory
SC	subcarrier
SCA	subsidiary communications authorization — a non program-related subcarrier in the FM baseband above 23kHz (monophonic) or 57kHz (stereophonic)
S/P-DIF	Sony/Philips digital interface
TRS	tip-ring-sleeve (2-circuit phone jack)
THD	total harmonic distortion
TX	transmitter
µs	microseconds
VCA	voltage-controlled amplifier
VU	volume unit (meter)
XLR	a common style of 3-conductor audio connector
XTAL	crystal

User Feedback

Please use this form to send us your comments and suggestions regarding this product or manual. Cut out and fold this page — or make a copy.

← First Fold

Cut Along This Line ↓

Second Fold →

Thank You.

Model #: _____

Serial #: _____

Date of comments: _____

Would you like a reply?

We welcome your suggestions to improvements to either the product or the manual. Our Customer Service may use the information you provide to help others. We do not sell or pass on to other companies information provided from this form and we will not use your name for advertising or promotion.

Your Name: _____

Organization: _____

Address: _____

City, State/Province: _____

Country: _____ Mail Code: _____

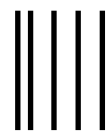
Telephone: _____

Telex: _____ FAX: _____

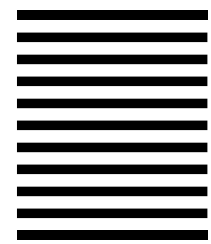
FIRST, FOLD THIS SIDE IN.

FOLD HERE

FOLD HERE



NO POSTAGE
NECESSARY IF
MAILED IN THE
UNITED STATES



BUSINESS REPLY MAIL

FIRST CLASS MAIL PERMIT NO 2445 SAN LEANDRO CA

POSTAGE WILL BE PAID BY ADDRESSEE

ATTN CUSTOMER SERVICE
Orban A DIVISION OF AKG ACOUSTICS INC
1525 ALVARADO STREET
SAN LEANDRO CA 94577–9810 USA

FOLD HERE

FOLD HERE

SECOND, FOLD THIS SIDE OVER. TAPE CLOSED — DO NOT STAPLE.