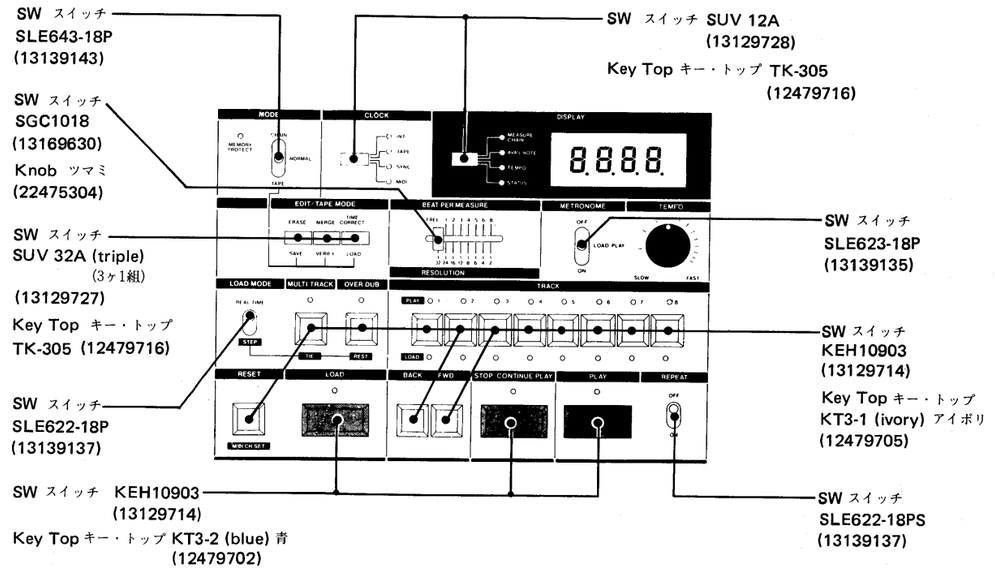
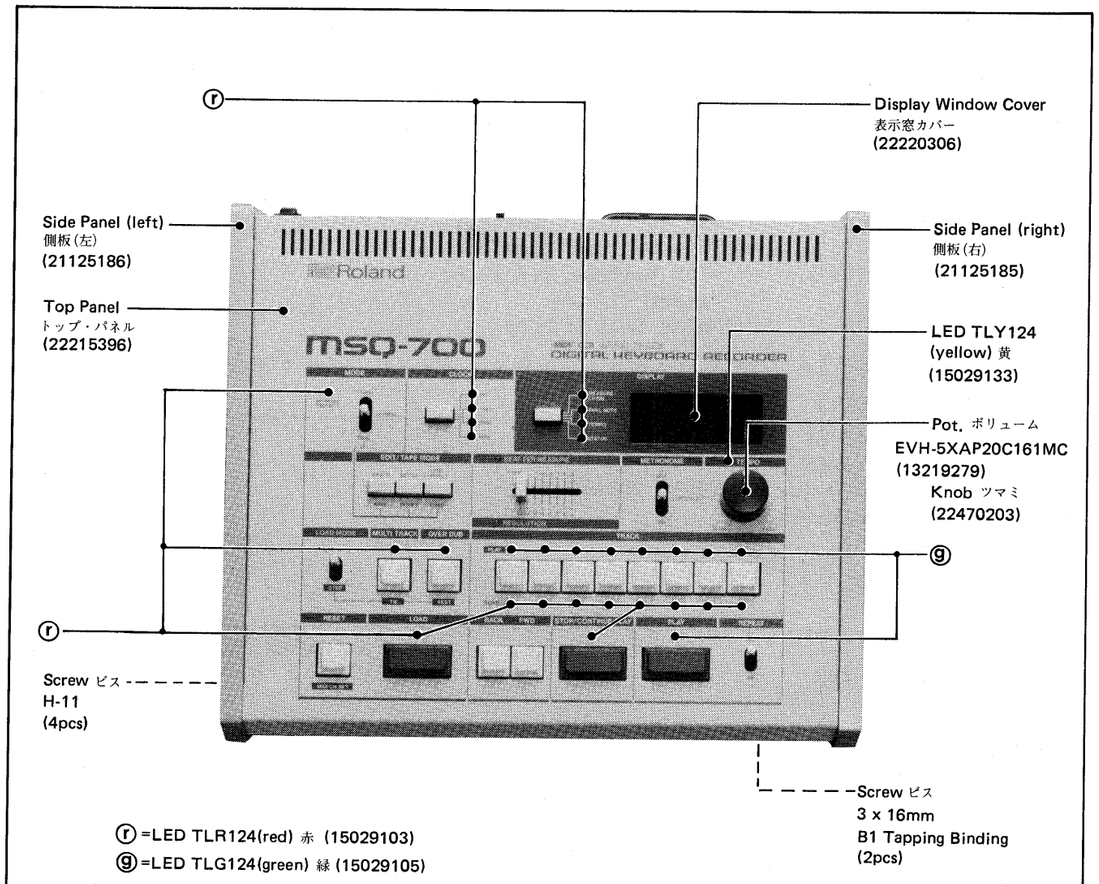
MSQ-700 SERVICE NOTES

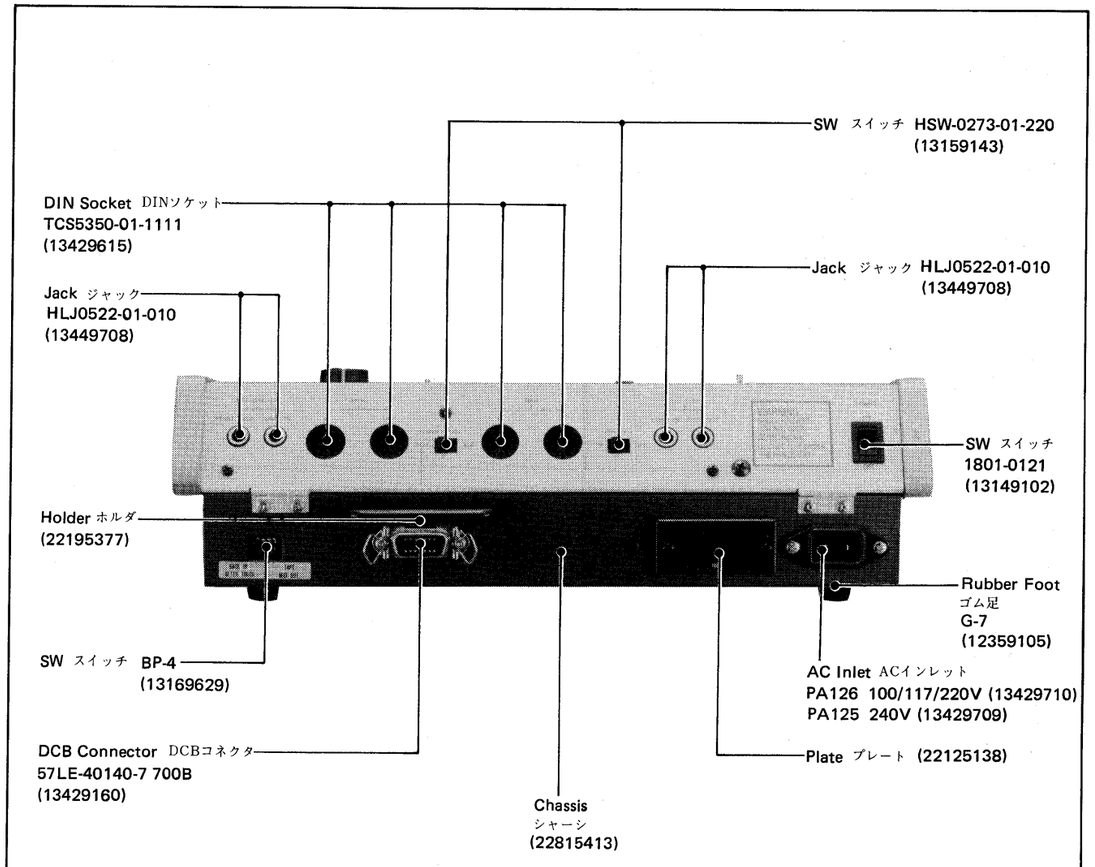
First Edition

SPECIFICATIONS

Memory Capacity	:	Approx. 6500 steps (one note/step)
Tape Interface	:	3200 baud
Power Consumption	:	13W (100V) 14W (117–240V)
Dimensions	:	346(W) x 328(D) x 108(H)mm 13-5/8(W) x 12-15/16(D) x 4-1/4 in
Weight	:	5 kg/11-1/8 lb







PARTS LIST

22215396	Top	Panel	トップ・パネル	
22815413	Bottom	Chassis	シャーシ	
21125186	Side (left)	Panel	側板(左)	
21125185	Side (right)	Panel	側板(右)	
22125138	Plate プレート		電圧切換カバー	voltage selector cover
12479705	KT3-1 (ivory)	Key Top	キー・トップ(アイボリ)	
12479702	KT3-2 (blue)	Key Top	キー・トップ(青)	
12479716	TK-305	Key Top	キー・トップ	
22470203		Knob	ツマミ	TEMPO
22475304		Knob	ツマミ	BEAT PER MEASURE
22220306	Cover カバー	Display Window	表示窓	
12359105	G-7	Rubber Foot	ゴム足	

SWITCH スイッチ

13149102	1801-0121	see-saw	シー・ソー		power
13129727	SUV 32A	Key (triple)	キー (3ヶ1組)	SW5-7	panel board
13129728	SUV 12A	Key	キー	SW3,4	panel board
13169630	SGC1018	Slide Code	スライド	SW26	panel board
13129714	KEH10903	Key	キー	SW9-24	panel board
13139135	SLE623-18P	Lever	レバー	SW8	panel board
13139137	SLE622-18PS	Lever	レバー	SW2,25	panel board
13139143	SLE643-18P	Lever	レバー	SW1	panel board
13159143	HSW-0273-01-220	Slide	スライド	SW1,2	jack board
13169629	BP-4	Dip	ディップ	SW1	main board
13169628	BS-4	Dip	ディップ	SW2	main board
13169503	ESE-3711				voltage selector

JACK ジャック

13449708	HLJ0522-01-010	6.5mm dia.

SOCKET ソケット

13429710	PA126	AC Inlet	100/117/220V	ACインレット
13429709	PA125	AC Inlet	240V	ACインレット
13429615	TCS5350-01-1111		DIN Socket	DINソケット
13429160	57LE-40140-7700B(D3)		DCB Socket	DCBソケット
13429520	IC99-24#2 (28 pin)		IC Socket	ICソケット

POTENTIOMETER ボリューム

13219279	EVH-5XAP20C16	1MC		TEMPO
13299101	EVTR4SA00B14	10KB	Main Board	半固定 trimmer
13299103	EVTR4SA00B24	22KB	Main Board	半固定 trimmer
13299136	RVF8P01-503	50KB	Panel Board	半固定 trimmer

PCB ASSEMBLY 基板完成品

7931907000	Panel Board (pcb 22915866)	パネル基板
7931906000	Main Board (pcb 22915863)	メイン基板
7931908000	Jack Board (pcb 22915867)	ジャック基板
7931905100	Power Supply Board 100/117V (pcb 22915864)	電源基板
7931905400	Power Supply Board 220/240V (pcb 22915864)	電源基板

IC

15179111P0	LH-0080A	CPU Z-80
15179177	M5L8041A	CPU (Program mask type)
15179333	TMM2016P/D	16K NMOS-RAM
15179335	HM6264LP-15	64K Static RAM
15179647	2764-647	PROM (Programed Type-A for MSQ-700)
15179648	2764-648	PROM (Programed Type-B for MSQ-700)
15179178	LH-0086A	Z-80 Serial Input/Output Controller
15159703	M54529P	5 unit 320mA Transistor Array with Strobe
15159702	M54563P	8 unit 500mA Darlington Transistor Array
15179179	M5L8243A	I/O Port Extention Interface
15179110	M5L8253P-5	Programmable Interval Timer
15179128	M5L8255	Programmable Peripheral Interface
15159105	TC4013	Dual D-type F.F.
15159116	TC4069UBP	Hex Inverter
15159303	TC4584BP	Hex Schmitt Trigger
15169347	74LS32	Quadruple 2-Input Positive OR Gate
15169327	74LS367	Hex Bus Driver with 3-State Outputs
15169311B0	M74LS74AP	Dual D-type Positive Edge-Triggered F.F. with Set and Reset (Mitsubishi only)
15169334	74LS05	Hex Inverter with Open Collector Outputs
15169304	74LS04	Hex Inverter
15169341	74LS14	Hex Schmitt Trigger Inverter
15159505	40H004	Hex Inverter
15159506	40H138	3-to-8 Line Decoder/Demultiplexer
15159525	40H139	Dual 2-to-4 Line Decoder/Demultiplexer
15159526	40H153	Dual 4-to-1 Line Data Selector/Multiplexer
15159519	40H157	Quad 2-to-1 Line Data Selector/Multiplexer
15159527	40H163	Synchronous 4-Bit Binary Counter
15159524	40H245	Octal Bidirectional Bus Buffer
15189105	μPC4558	OP Amp
15189118	TL-082	J-FET Input OP Amp
15199106NH	μPC7805H	+5V Voltage Regulator
15199118NO	μPC7815H	+15V Voltage Regulator
15199102NO	μPC7915H	-15V Voltage Regulator
15219109	555	Timer
15219105	LM565	Phase Locked Loop

TRANSISTOR トランジスタ

15129114	2SC1815-GR	
15119113	2SA1015-GR	
15129815	2SD880-0 (or 15129816 2SD880-Y)	
15139103	2SK30ATM-GR	FET
15129143	DTC124A	(抵抗内蔵) (With built-in resistor)

DIODE ダイオード

15019236	W-02	ブリッジ整流器	bridge rectifier
15019208	1SR35-200	整流器	rectifier
15019137	DAP401	アレイ	array
15019103	1S2473		
15019628	05Z5.6U	ツェナー	zener
15029103	TLR124 (red)赤		LED
15029105	TLG124 (green)緑		LED
15029133	TLY124 (yellow)黄		LED
15029141	LT8001P		LED
15029157	LB-602VK-2-1		7 segment LED

CERAMIC RESONATOR 発振子

12389728	KMFC1034T	Ceralock 8MHz	メイン基板 main board
12389800	KMFC1005T1	Ceralock 6MHz	パネル基板 panel board

PHOTO COUPLER フォト・カプラ

15229712	PC900

TRANSFORMER, COIL トランスフォーマ, コイル

22455367U0	Power Transformer	100-240V 電源トランス	
2244021500	SN8D-500	コイル	coil
12449229	FKOB-160MH15	コイル	coil

FUSE ヒューズ

12559331	GGS 0.8A/250V UL	Primary	1次側	100/117V
12559508	CEE T250mA/250V	Primary	1次側	220/240V
12559521	CEE T1.6A/250V	Secondary	2次側	220/240V

RESISTOR ARRAY 抵抗アレイ

13910113	RGSD 4-103K	10KJ x 4
13919305	RM 4-472J	4.7K x 4
13919303	RM8-333J	
13919302	RM8-102J	

CAPACITOR コンデンサ

13529108	RPE132F104Z50V		ceramic
13569153	CQ09S-1H-22000-J05		styrol
13639193S0	35MV470H	470μF/35V	electro (SANYO only)
13529104	DE7150F472MVA1	SEMKO,UL,SEV,VDE Marking	C1,C2
13529110	DSS310-55B222M	EMI reduction	panel board
13529105	DSS310-55D223S	EMI reduction	jack board

HOLDER ホルダー

22195426	(RESET/LOAD/BACK/FWD/STOP/PLAY Key Switch)
22195427	(MULTI TRACK/OVER DUB/TRACK 1-8 Key Switch)

PIEZOELECTRIC BUZZER 圧電ブザー

12389711	PKM-24-4A0

AC CORD SET ACコード・セット

13439825	DC-320-J01	100V
13439812F0	UC704-J01	117V
13439813F0	EC210-J06	220V
13439817F0	EC702-J05	240V
13439814F0	SC-415-J06	240V 3P

CONNECTOR コネクタ

13439123	5045-07A 7 pin
13439124	5045-08A 8 pin
13439125	5045-09A 9 pin
13439126	5045-10A 10 pin

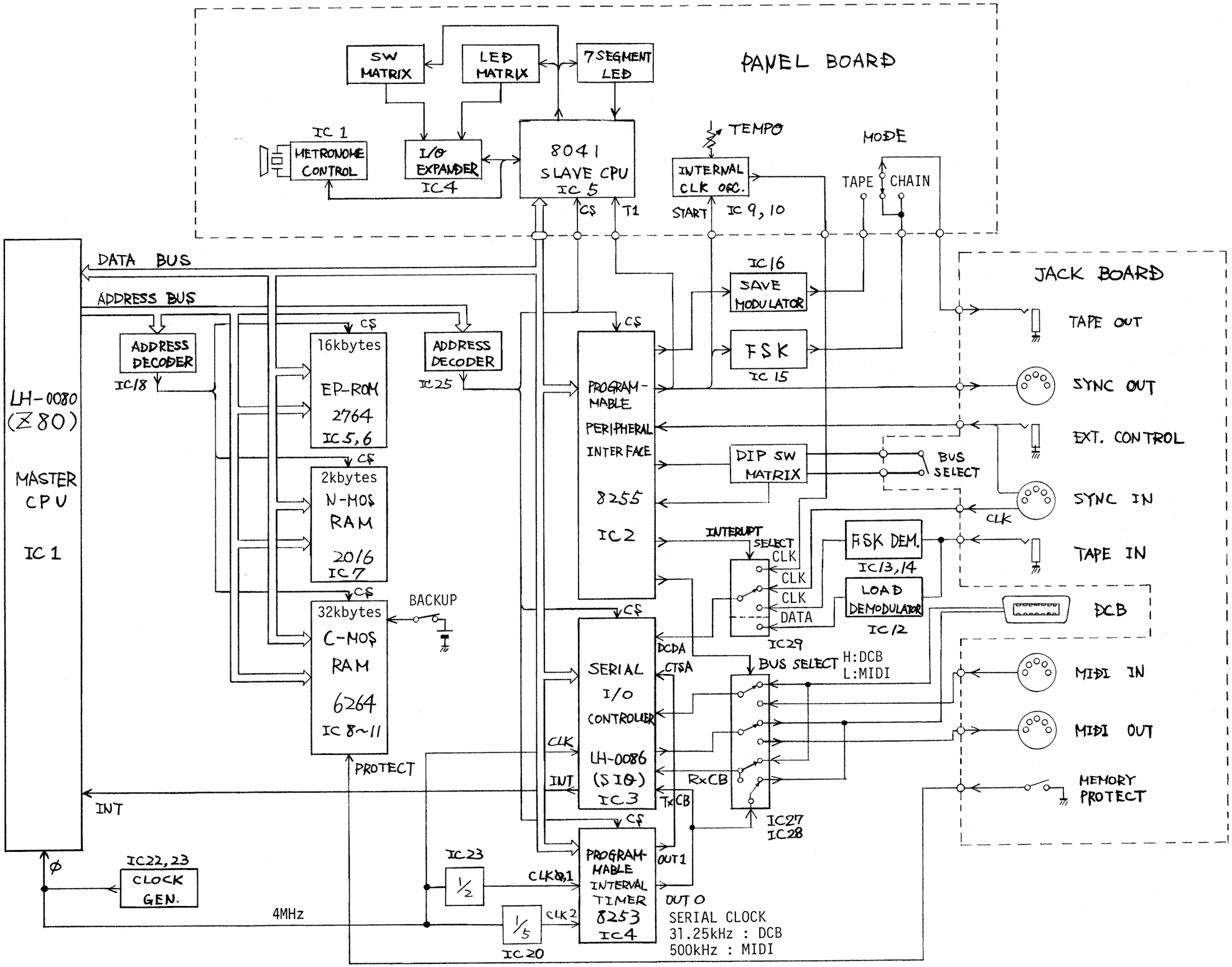
MASK マスク

22240402	スライドSW	slide SW
22240409	レバーSW	lever SW
22245130	通気スリット	air vent
22245131	ジャック、スライドSW	jack,slide SW

OTHERS その他

12569140	ER-6	Lithium Battery	リチウム電池
12199519	TF-758	Fuse Holder	ヒューズ・ホルダ
22195377	Holder ホルダー	DCB Protect Bar (black)	DCB保護棒(黒)
12469119	FH-30	Heat Sink ヒート・シンク	power supply board IC1
22815414	Jack Chassis ジャック・シャーシ		
13129719	CH32801A	Guide Pin	SW KEH10903
12479714	CK42602A	Shock Absorber	KT3-2
	H-11	Screw ビス	side panel

BLOCK DIAGRAM



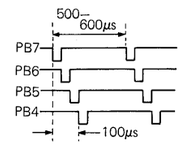
CIRCUIT DESCRIPTIONS

General Description

As can be seen from the block diagram Master CPU IC1 on the Main board performs most of the tasks, except for memories, through various I/O ports and interfaces. Although there is another CPU IC5(Slave) on the Panel board, the master CPU treats it as one of the I/O ports, as being an intelligent I/O. The tasks of these devices (Port and Interface) are summarized as below.

IC2 8255 Programmable Peripheral Interface
MAIN BOARD

SW1 (BUS SLCT: Jack Brd)

Port A (in)	PA7	pin37	IC4-2 overflow	H: overflow
	PA6	pin38	Memory protection	H: protect ON
	PA5	pin39	DIP SW SW2	L: SW ON
	PA4	pin40	DIP SW SW1-2 SW1-3 SW1 (BUS SLCT. Jack Brd.)	L: SW ON
	PA3	pin1	Pedal 2 Punch in	L: pedal ON
	PA2	pin2	Pedal 1 START/STOP	L: pedal ON
	PA1	pin3	DIN SYNC CONTINUE	L: active
	PA0	pin4	DIN SYNC START/STOP	L: active
Port B (out)	PB7	pin25	DIP SWITCH SCANNING 	
	PB6	pin24		
	PB5	pin23		
	PB4	pin22		
	PB3	——	NC	
	PB2	——	NC	
	PB1	pin19	Data to tape (SAVE)	
	PB0	pin18		
Port C (out)	PC7	pin10	BUS Select	L: MIDI, H: DCB
	PC6	pin11	INTERRUPT Select B	
	PC5	pin12	INTERRUPT Select A	
	PC4	pin13	INTERRUPT Disable	H: Disable
	PC3	pin17	FSK control	Negative Logic
	PC2	pin16	DIN SYNC CONTINUE	
	PC1	pin15	DIN SYNC START/STOP	
	PC0	pin14	DIN SYNC CLOCK	

INTERRUPT SELECT CODE

PC6	PC5	PC4	INTERRUPT SOURCE
L	L	L	CLK INTERNAL
L	H	L	CLK SYNC IN
H	L	L	CLK TAPE (FSK)
L	L	H	CLK MIDI (no connection)
H	H	L	DATA TAPE (LOAD/VERIFY)
H	H	H	NO SELECTION

IC3 LH-0086 Serial I/O Controller (SIO)
MAIN BOARD

LH-0086 contains two channels which are fully independent and can operate separately.

CHANNEL A

Configured as an interrupt controller.
The main task includes generation of Tempo Clock in cooperation with IC4 for use in LOAD or PLAY mode.

CHANNEL B

Serves as a Serial Interface.
Enables the MSQ-700 to communicate with the DCB or the MIDI equipped instrument.

IC4 8253 Programmable Internal Timer
MAIN BOARD

Contains three counters.

COUNTER 0

Used in MODE 3: Square Wave Rate Generator.
Generates Transmit and Receive clocks for SIO IC3. The output is either:

31.25kHz in DCB mode or
500kHz in MIDI mode

COUNTER 1, COUNTER 2

COUNTER 1 Operates in MODE 3.
Generates square waves 2.5 times Tempo input clock in frequency.
Also generates 250us wide wave in TAPE SAVE mode for use as transmit clock.

COUNTER 2 Operates in MODE 0.
Counts 800kHz input clocks at Tempo Clock intervals.

Both counters, in conjunction with IC3 channel A, multiply Tempo clocks by 5.

IC5 8041 Slave CPU
PANEL BOARD

As an intelligent I/O the CPU performs most of the tasks besed on its self-judgement upon receiving information from the master CPU. However, the slave CPU does not make use of Panel switch reading data, it only sends the data to the master CPU, and lights up LEDs (except 7-seg LED ---- Display) under the instruction of the Master CPU.
Since the Slave CPU does not have enough ports to cover its peripherals it employs IC4 as an expander I/O.

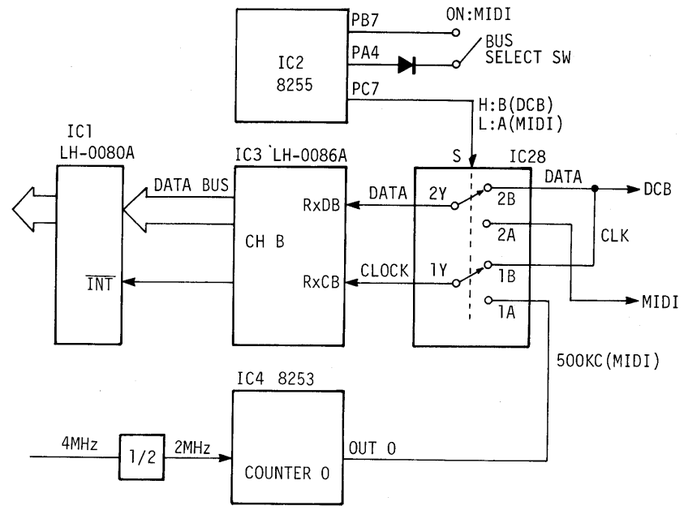
Detailed Description

SERIAL DATA TRANSFER

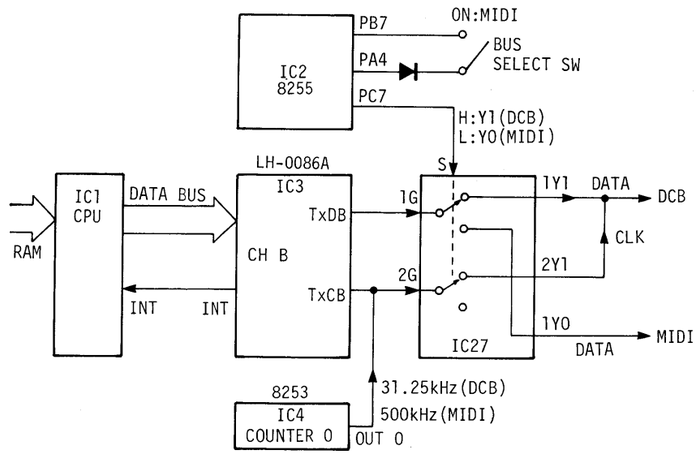
Data transfer between MSQ-700 and DCB or MIDI equipped device is accompolished via the arrangement shown here in the functional block diagrams. The difference between MIDI and DCB in data format requires different mode of Channel B of the IC3 respectively. IC27 and IC28 switch between modes of channel B as well as bus connections according to a bus selection code from PC7 of IC2 which in turn changes its output based on a switch read made on BUS SELECT on the rear panel as follows.

BUS SELECT	IC2 PA4	IC2 PC7
DCB	H	H
MIDI	L	L

RECEIVING MODE

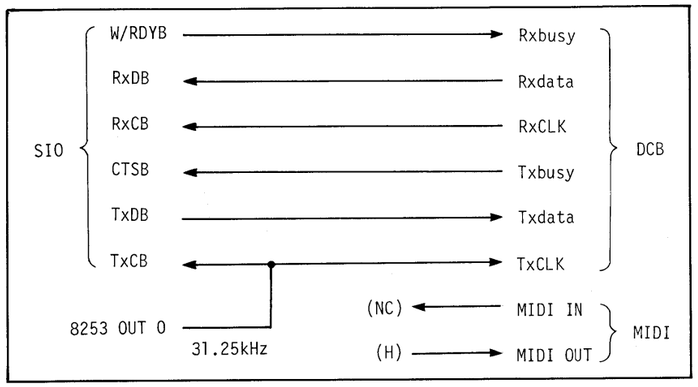


TRANSMITTING MODE



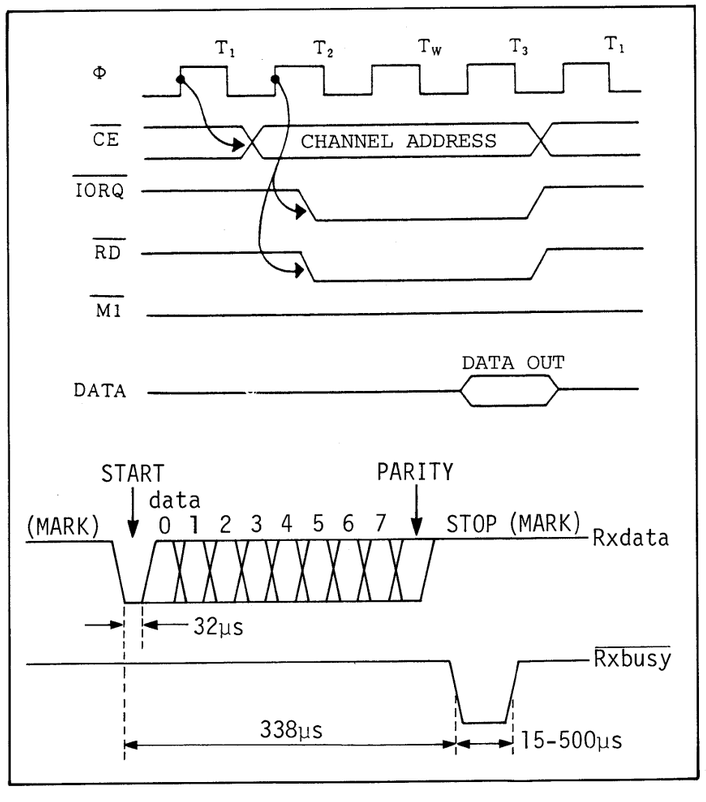
DCB

In the DCB mode, connection between DCB and IC3 is as shown below.



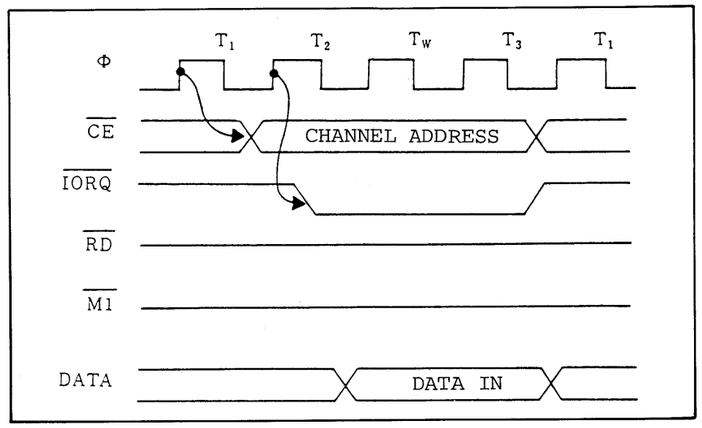
RECEIVING MODE

When channel B receives a one byte data, IC3 turns W/RDYB (RxBUSY) LOW. When the channel B receive buffer becomes full, the IC3 informs the CPU via INT that it has received data. The CPU issues acknowledge by placing a low on MI and IORQ lines respectively, and the INT is turned back to high.
Then the CPU reads the one byte parallel data with low CE, IORQ and RD.
Completion of data read from the receive buffer enables IC3 to return RxBUSY back to high.



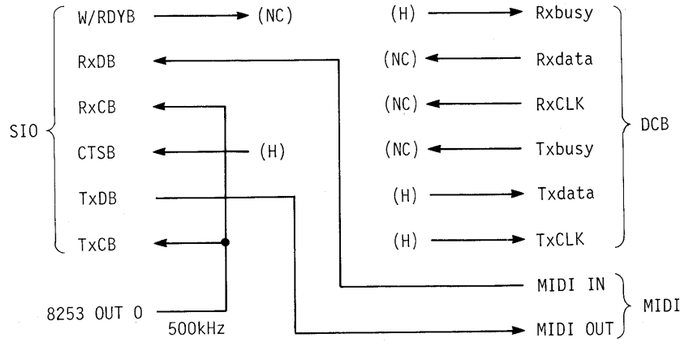
TRANSMITTING MODE

The IC3 informs the CPU via INT the status of transmit buffer and TxBUSY from DCB, and accepts one byte parallel data from the CPU in much the timing in Receiving mode, but on high RD and only when TxBUSY is inactive (H at DCB connector) and the buffer is empty. The IC3 transmits the data in serial format at 31.25K baud, the rate which is determined by the OUT 0 of IC4.



MIDI

In MIDI mode connection to channel B of IC3 becomes as follows:



RECEIVING MODE

In receiving MIDI data, IC3 samples a one byte serial data on 500kHz, which 16 times 31.25kHz. Then it interrupts the CPU so that the CPU can read the data from the IC3 receive buffer. Recognizing $\overline{INT}$, the CPU acknowledges it with $\overline{MI}$ and $\overline{IORQ}$, then reads the data by turning the following pins of IC3 low: 35 (CE),36 (IORQ) and 32 (RD). See the timing chart in DCB RECEIVING MODE.

TRANSMITTING MODE

IC3 requires IC1 with $\overline{INT}$ to send a one byte data when its transmit buffer is empty. IC1 writes data into IC3 with the timing shown in the timing chart in DCB TRANSMITTING MODE.

TEMPO CLOCK

Once accommodated in the master CPU, tone data are stored into memories in the format below; whether they are coming from DCB or MIDI.

Time	Key Event (e.g. ON)	Key Velocity	Time	Key Event (e.g. OFF)
1 byte	1 byte	1 byte	1 byte	1 byte

For storing one complete ON and OFF of a note, 5 bytes are necessary. Although key velocity data is not included in DCB, dummy value is added to have compatibility with MIDI for simplified data processing.
The topic to be discussed here is by what means the length of note (or rest) is measured and stored in memories. In the MSQ-700, time is referenced to tempo clock, that is, the value of a note or rest is expressed in the number of clocks; on the 120 clocks per quarter note basis. These clocks are referred to as CLK120 in the MSQ-700.

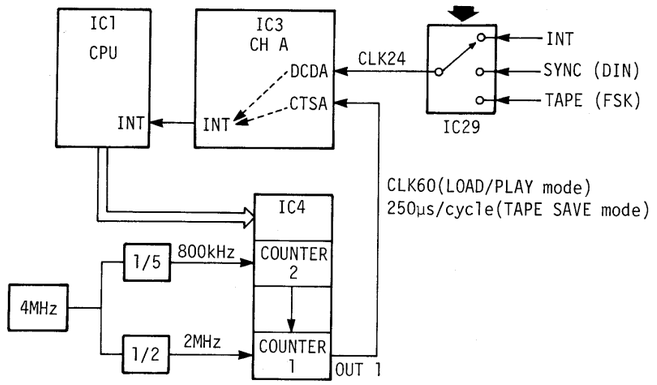
CLOCK SOURCES

Four clock sources are made available to the MSQ-700: INT (internal), TAPE (FSK), MIDI and SYNC (DIN SYNC); all these clocks are defined as CLK24. This measns that 24 of these clocks are equal to a quarter note in length. However, as mentioned above, the number of clocks that equals a quarter note is 120 in the memory section. Thus, CLK24 has to be multiplied by 5.
The reason for the use of CLK120 is to have higher time resolution of tone data; the higher the clock frequency, the higher the time resolution can be obtained for the same note length.

CLOCK SOURCE SELECT

The selection of source made from the front panel through CLOCK button is detected by the Slave CPU and IC4, causing the Master CPU to place Interrupt Select code through IC2 port C.

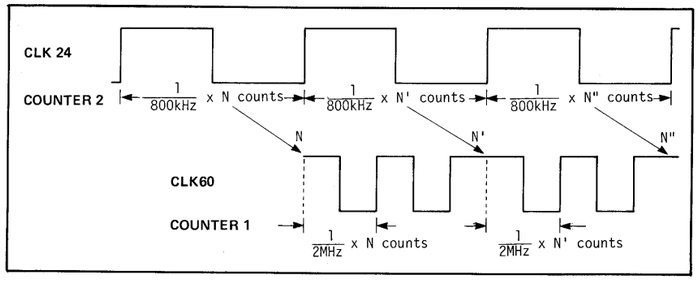
IC2 PORT			CLOCK SOURCE
PC6	PC5	PC4	
L	L	L	INT
L	H	L	SYNC (DIN)
H	L	L	TAPE (FSK)
L	L	H	MIDI (no connection)



NOTE: MIDI clocks are not fed through IC29, but contained in the MIDI data and are selected by the program. Once selected, MIDI clocks are processed by the CPU the same way as clocks from the other sources.

CLOCK MULTIPLICATION

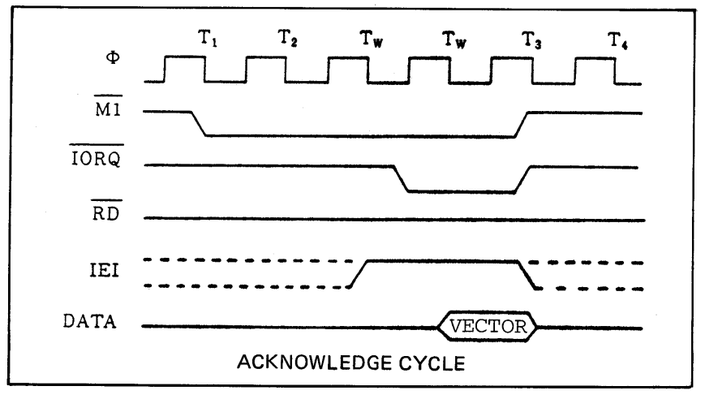
IC3 develops INT on every edge of CLK24 applied to DCDA terminal.The CPU ignores INT occuring on the falling edge of CLK24. Upon recognizing INT corresponding to the rising edge of CLK24, the CPU reads and resets the counter 2 in IC4 which in turn restarts counting. The CPU sets the counter 2 counts into counter 1 which generates rectangular whose frequency 2.5 times that of CLK24 in proportion to the ratio of the clocks coming to both counters respectively:800kHz to 2MHz -- CLK24 x 2.5 = 60. Hereafter, call this CLK60. When this CLK60 is applied to CTSA, IC3 generates INT on every edge; this time the CPU appreciates all the INTs and recognizes a chain of INTs as CLK120.

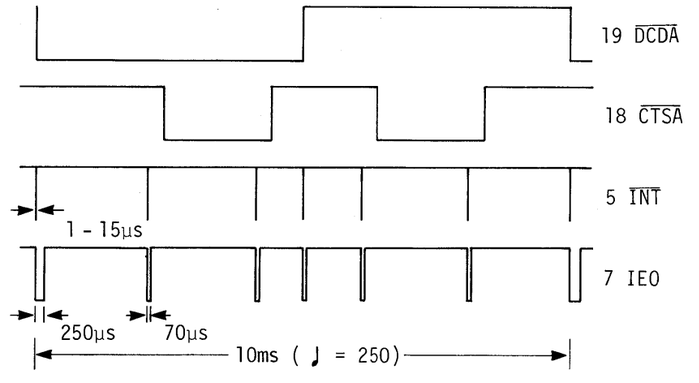


BRIEF REVIEW OF IC3 FUNCTION

By observing some terminals, conversation between IC1 and IC3 via INT line is examined as exampled below.
This illustration has channel A representative with Internal Clock OSC selected as an interrupt source. For clarification on the scope,no signal should be connected to channel B (MIDI and DCB busses).
When IC3 receives a square wave at DCDA or CTSA, it turns INT terminal low on every edge.
Upon receiving INT, IC1 acknowledges it by pulling MI and IORQ to low, causing IC3 to turn INT back to high. While the CPU is performing a set of specified operations preprogrammed to handle each interrupt, IC3 keeps IEO (Interrupt Enable Out pin 7) low.

If INT is continuously high, IC3 is suspective, it may not recognize the Internal Clock.
If INT is continuously low, this time IC1 is suspectable; failing to recognize the interrupt from IC3.
If IEO remains low, it is signaling that the CPU cannot exit the routine involved with interrupt. CPU, ROM, RAMs should be checked.





SYNC

Tempo clocks have been discussed in the previous paragraphs. But with the MSQ-700 linked to external unit(s), synchronization of start/stop and tempo is another important consideration.
With Roland SYNC system (especially SYNC using DIN socket-- referred to as DIN SYNC), the first tempo clock must be generated (or fed to slave) after 5-10ms of a START signal. INT CLOCK OSC on the Panel board works to meet this specification. When the MSQ-700 is "started" with CLOCK set at INT, IC2 PC1 (Main board) goes low, which is inverted at pin 6 of IC26 and resets INT CLOCK OSC. After approxmately 5ms the OSC restarts oscillation. The low from PC1 is also inverted at TR7 collector and applied to DIN SYNC socket as a START signal. After approximately 5ms the first clock is output from IC2 PC0 and routed to the DIN SYNC socket.

SYNC (DIN SYNC)

When SYNC is selected from the front panel, START signal will be applied to PA0 of IC2 while clocks are to be fed to DCDA of IC3 after 5-10ms.

MIDI

The master CPU recognizes start when it receives start message(1111 1010) through MIDI bus and puts it into effect if CLOCK on the panel is set at MIDI. The CPU recognizes tempo clock via MIDI timing clock message. However, if clock message comes too short after a start signal, the CPU will fail to read the first clocks.
The CPU processes timing clocks just the same as it does for clocks from INT pins;the CPU converts timing clocks into CLK120 via counter 2, counter 1 and channel A loop.

TAPE

With TAPE selected by the CLOCK on the front panel, the CPU recognizes start signal whenever generated internally or externally and will recognize the pulse from the FSK DEMO as a tempo clock. This implies that some misinterpretaion might be made at the CPU if "START" is made before the leader tone comes from the tape. The FSK DEMO is liable to generate a pulse upon receiving a noise or leader tone; this pulse is then might be recognized as the first tempo clock by the CPU. To avoid this from happining, the CPU must be fed with "START" while the leader tones are being applied.

SYNC OUT

In PLAY or LOAD mode, the MSQ-700 provides tempo clock for MIDI, TAPE SYNC and DIN SYNC outputs. These outputs are, of course, the duplication of clock source that is selected from the front panel. With external clock source selected, output on these sockets delay behind the input 200us which is required for the software to complete the necessary job.

TAPE SYNC (FSK)

Clocks for TAPE OUT are routed from IC2 PC3 though TR4 to TR2 which, as it is turned ON or OFF, shifts the frequency of TAPE SYNC SIGNAL GENERATOR between 1.3kHz and 2.1kHz.

IC2	TR2	IC15 FREQ.
H	OFF	1.3kHz
L	ON	2.1kHz

During the leader period 1.3kHz is generated.

Memory

RAMs 6264 IC8–IC11
MAIN BOARD

The total memory capacity of these RAMs add up to 32k bytes that are used for storing note data. These memories are divided into 128 blocks by 256 bytes. Of 128 blocks, one block is reserved for cordinating RAM memory itself and for storing CHAIN PLAY data.
Consequently, memories can be used for tone data are: 32778 -256 = 32512 bytes.
As mentioned ealier, one note (ON/OFF) needs 5 bytes (2 bytes for time, 2 for Key events and 1 for Velocity). Thus, 32512/5 (byte) ≒ 6,500 is the maximum tone number under ideal conditions -- BENDER or After Toutch can be memorized with sacrification of tone data in MIDI mode.

MEMORY BLOCK

As explained above,one memory block consists of 256 bytes, this is a minimum unit which can be handled in storing and reading in the MSQ-700.This conception should be remembered when plural track loading is intended.
Data slightly exceeding 256 bytes requires complete 2 blocks.

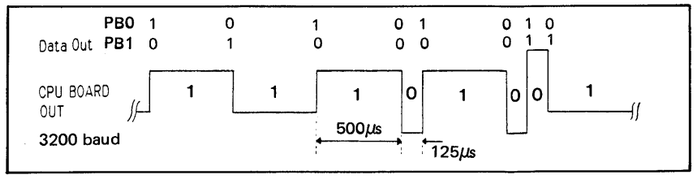
BATTERY BACK-UP

BACK UP switch on the rear panel is turned OFF at the factory for a long battery life. RAM intitialization is made upon turning ON of the power with PROTECT OFF, and the RAM control table is written into the RAM by the CPU. Necessary information on Initialization, Protect and Error is found on the MSQ-700 Owner's Manual.

CMT

OUTPUT TO TAPE (SAVE)

During the leader period 1kHz signal is placed from PB0 and PB1 of IC2. When in data saving, IC4 counter 1 generates 250us rectangular which is applied to the CPU via INT terminals. The Master CPU uses this INT as a time reference in producing data codes. For each data 1 or 0, the CPU selects one of two codes to have 1's and 0's distinguishable when they are interleaved with the same bits and are converted to analog signals.



INPUT FROM TAPE (LOAD)

Data from the tape is first smoothed and shaped up by IC12 and fed to IC29 INTERRUPT SELECTOR which connects the data to DCDA of IC3 when MODE is placed at TAPE. The serial data is fed in the form of INT chain to the master CPU where the data is converted into parallel format and stored into RAM memories.

VERIFY

Data from the tape are fed to the master CPU just the same as in TAPE LOAD mode except that data are compared with RAM stored data for verification.

METRONOME

Control of metronome is done by the Slave CPU IC5 on the Panel board. There are two metronome modes according to the setting of METRONOME on the panel.

LOAD OR PLAY MODE

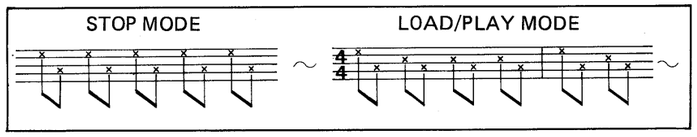
IC5 sounds metronome upon receiving "RUN" information from the Master CPU on the Main Board.

ON MODE

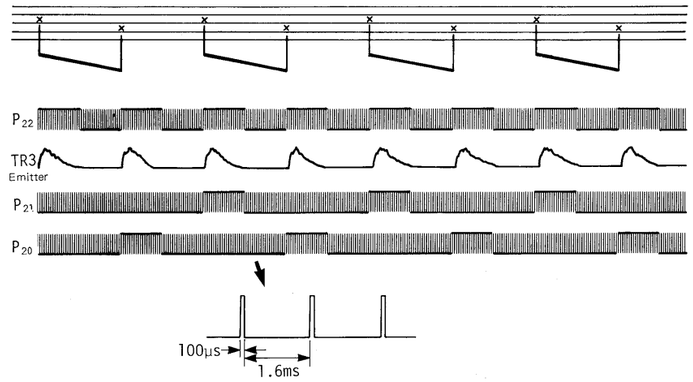
IC5 constantly drives the metronome circuit. In either mode IC5 outputs metronome drive pulse from P22 at an 8th note rate in synchronous with T1 coming from PC0 of IC2 on the Main board.

PITCH CONTROL

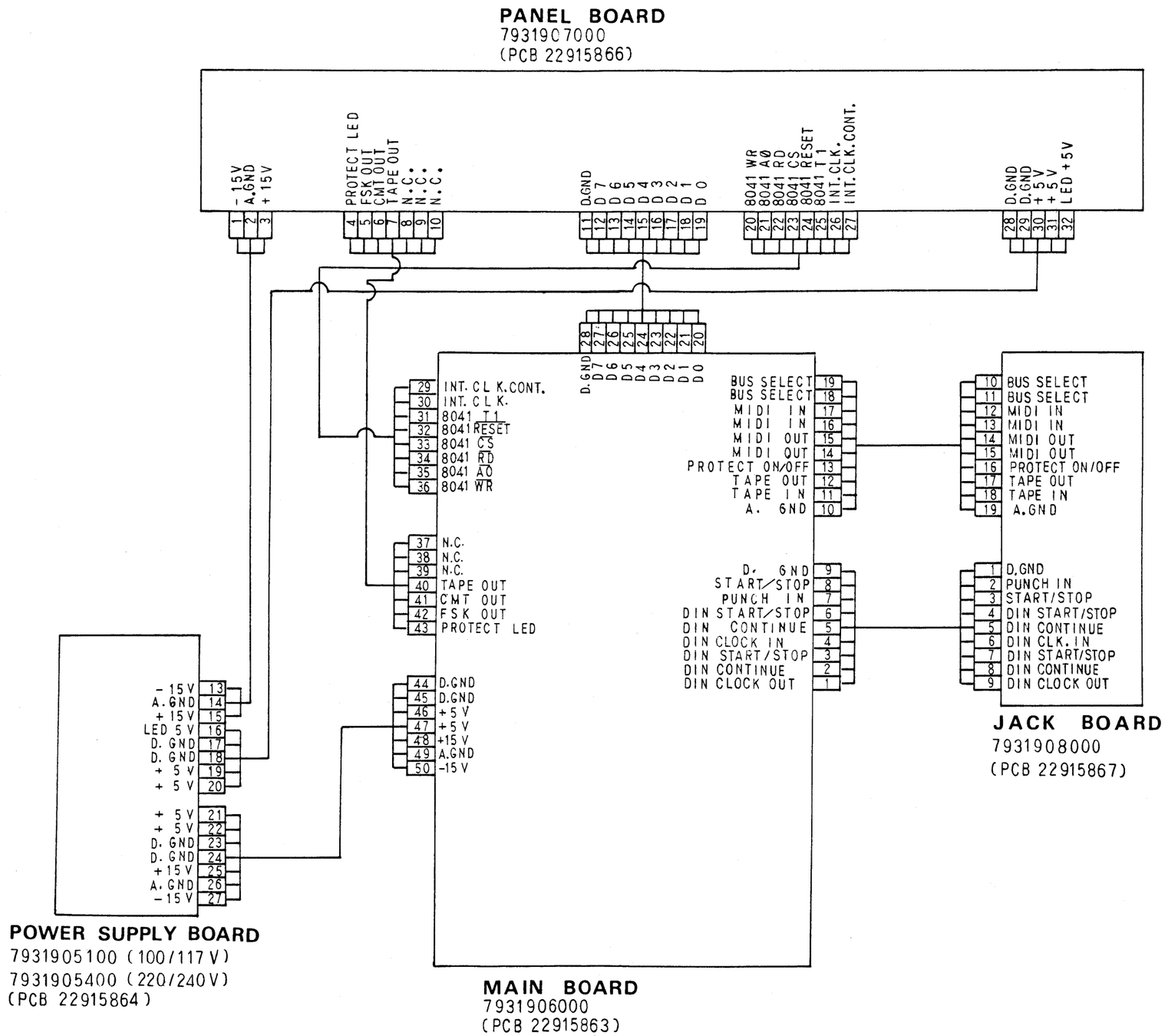
IC5 can provide two different click-pitch patterns: one for PLAY or LOAD, and one for ON. This is done by varying capacitance value at pin 2 of IC1 with P20 and/or P21 outputs.



As can be seen from the timing chart below, IC5 also outputs data for IC4--- 100us-width pulse at every 1.6ms. To prevent metronome signals from entering IC4, IC5 turns PROG low only for 100us at 1.6ms intervals.
On the contrary, these 100us pulses are filtered out before reaching metronome circuitry.



INTERCONNECTION

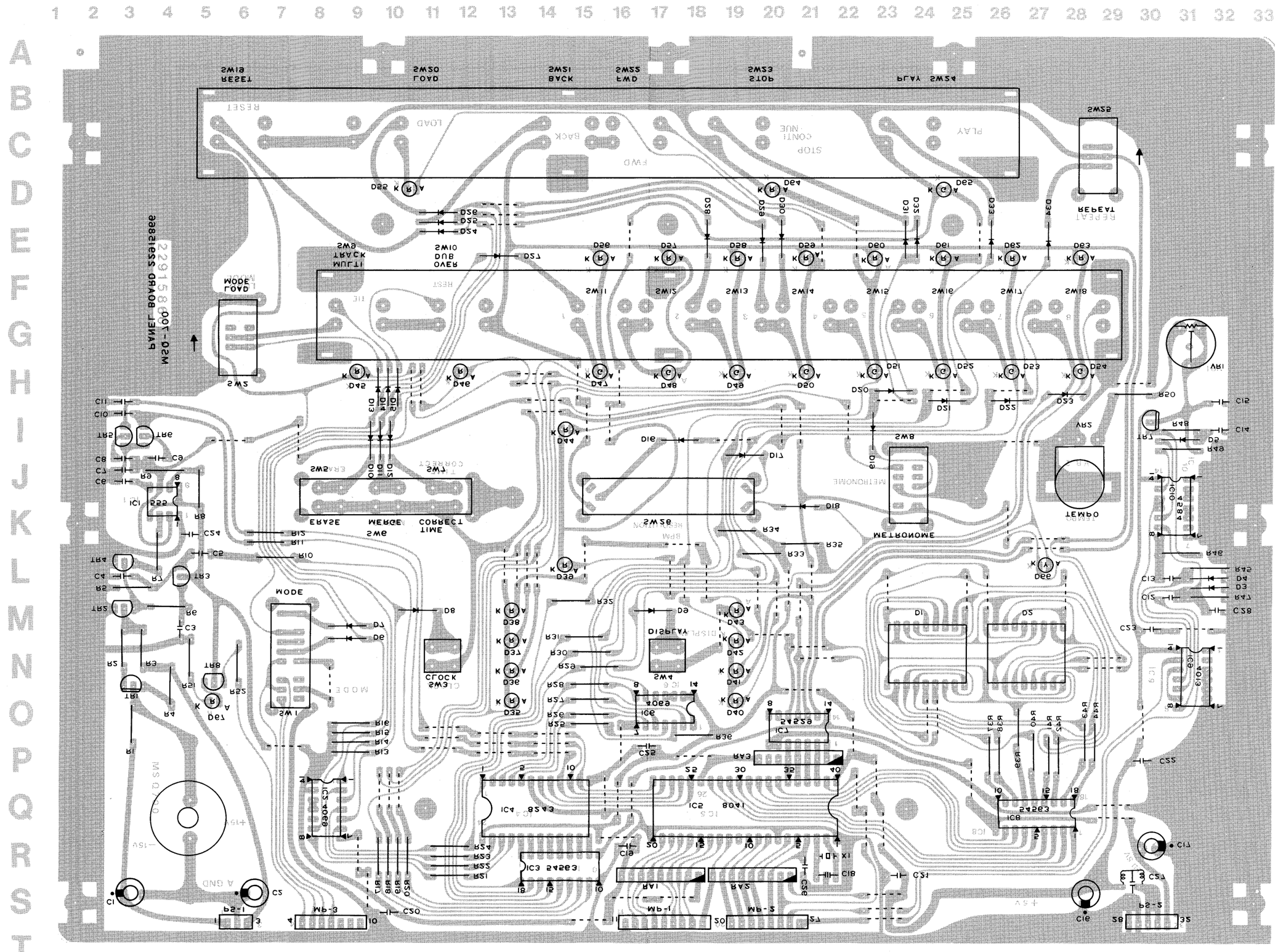


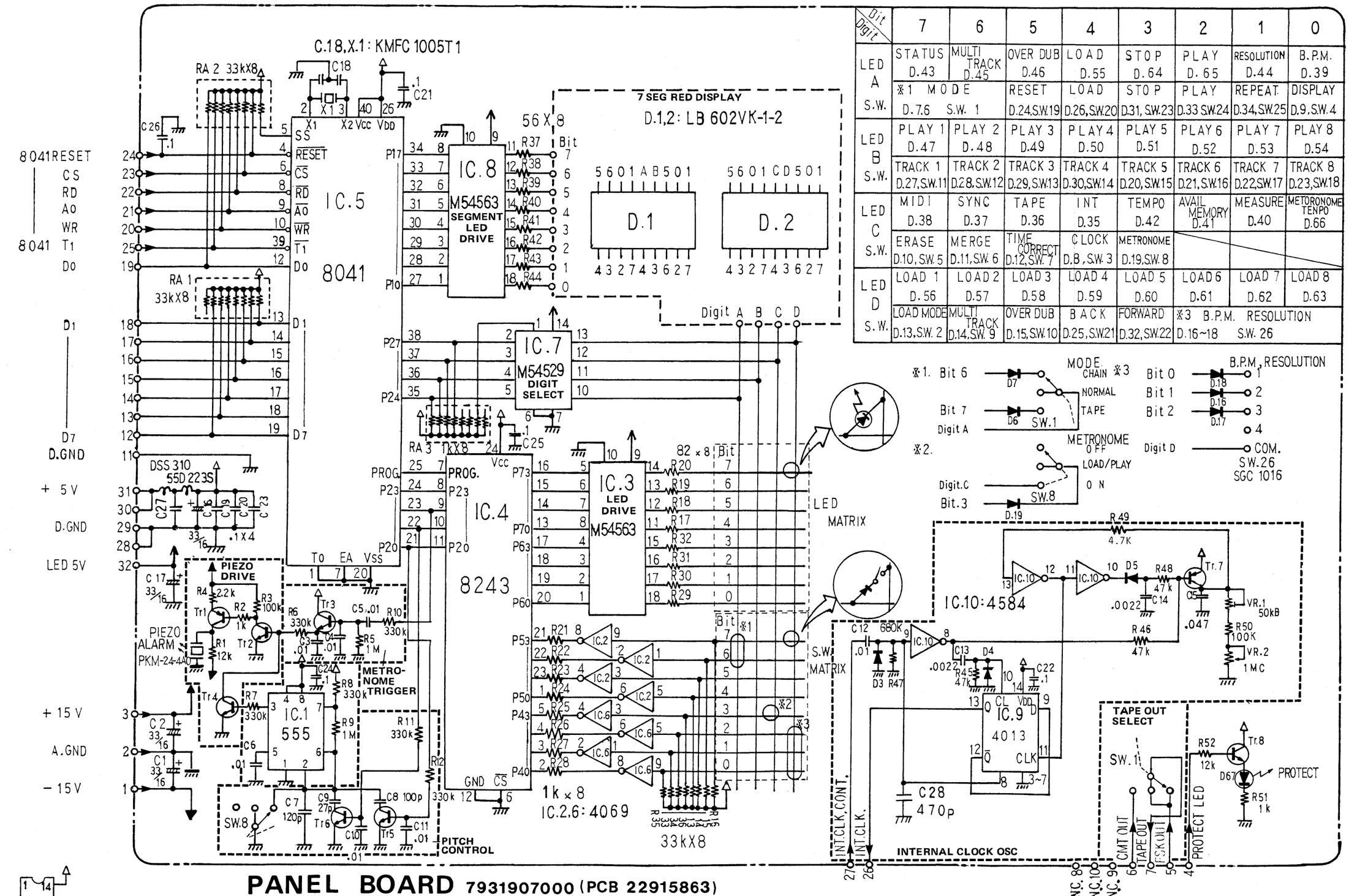
PANEL BOARD

7931907000

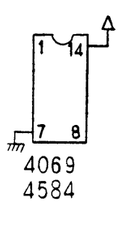
(pcb 22915866)

View from foil side





Bit / Digit	7	6	5	4	3	2	1	0
LED A S.W.	STATUS D.43	MULTI TRACK D.45	OVER DUB D.46	LOAD D.55	STOP D.64	PLAY D.65	RESOLUTION D.44	B.P.M. D.39
	※1 MODE D.7,6 S.W. 1		RESET D.24,S.W.19	LOAD D.26,S.W.20	STOP D.31, S.W.23	PLAY D.33 S.W.24	REPEAT D.34,S.W.25	DISPLAY D.9, S.W. 4
LED B S.W.	PLAY 1 D.47	PLAY 2 D.48	PLAY 3 D.49	PLAY 4 D.50	PLAY 5 D.51	PLAY 6 D.52	PLAY 7 D.53	PLAY 8 D.54
	TRACK 1 D.27, S.W.11	TRACK 2 D.28, S.W.12	TRACK 3 D.29, S.W.13	TRACK 4 D.30, S.W.14	TRACK 5 D.20, S.W.15	TRACK 6 D.21, S.W.16	TRACK 7 D.22, S.W.17	TRACK 8 D.23, S.W.18
LED C S.W.	MIDI D.38	SYNC D.37	TAPE D.36	INT D.35	TEMPO D.42	AVAIL MEMORY D.41	MEASURE D.40	METORONOME TENPO D.66
	ERASE D.10, S.W. 5	MERGE D.11, S.W. 6	TIME CORRECT D.12, S.W. 7	CLOCK D.8, S.W. 3	METRONOME D.19, S.W. 8			
LED D S.W.	LOAD 1 D.56	LOAD 2 D.57	LOAD 3 D.58	LOAD 4 D.59	LOAD 5 D.60	LOAD 6 D.61	LOAD 7 D.62	LOAD 8 D.63
	LOAD MODE D.13, S.W. 2	MULTI TRACK D.14, S.W. 9	OVER DUB D.15, S.W.10	BACK D.25, S.W.21	FORWARD D.32, S.W.22	※3 B.P.M. RESOLUTION D.16~18 S.W. 26		



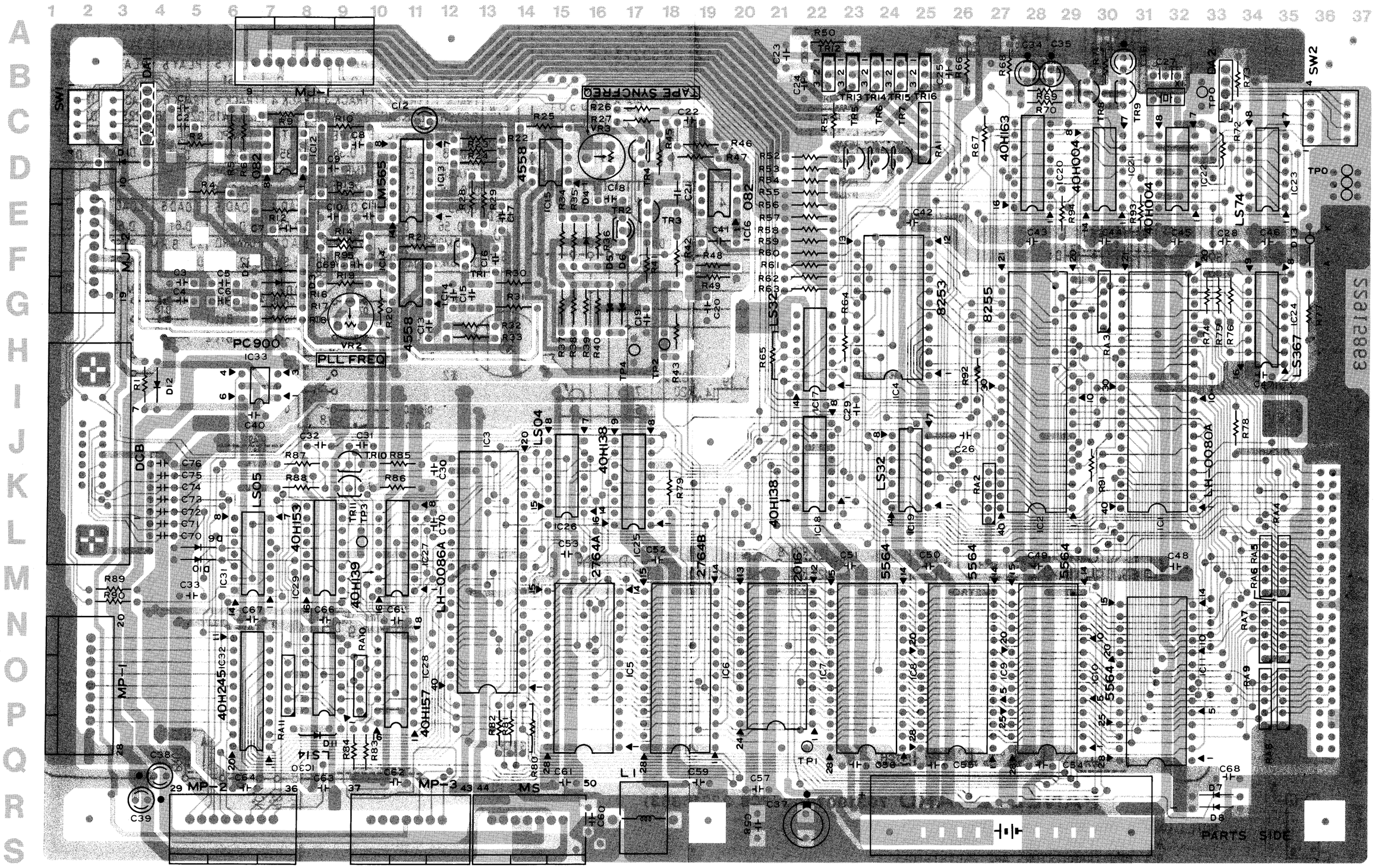
PANEL BOARD 7931907000 (PCB 22915863)

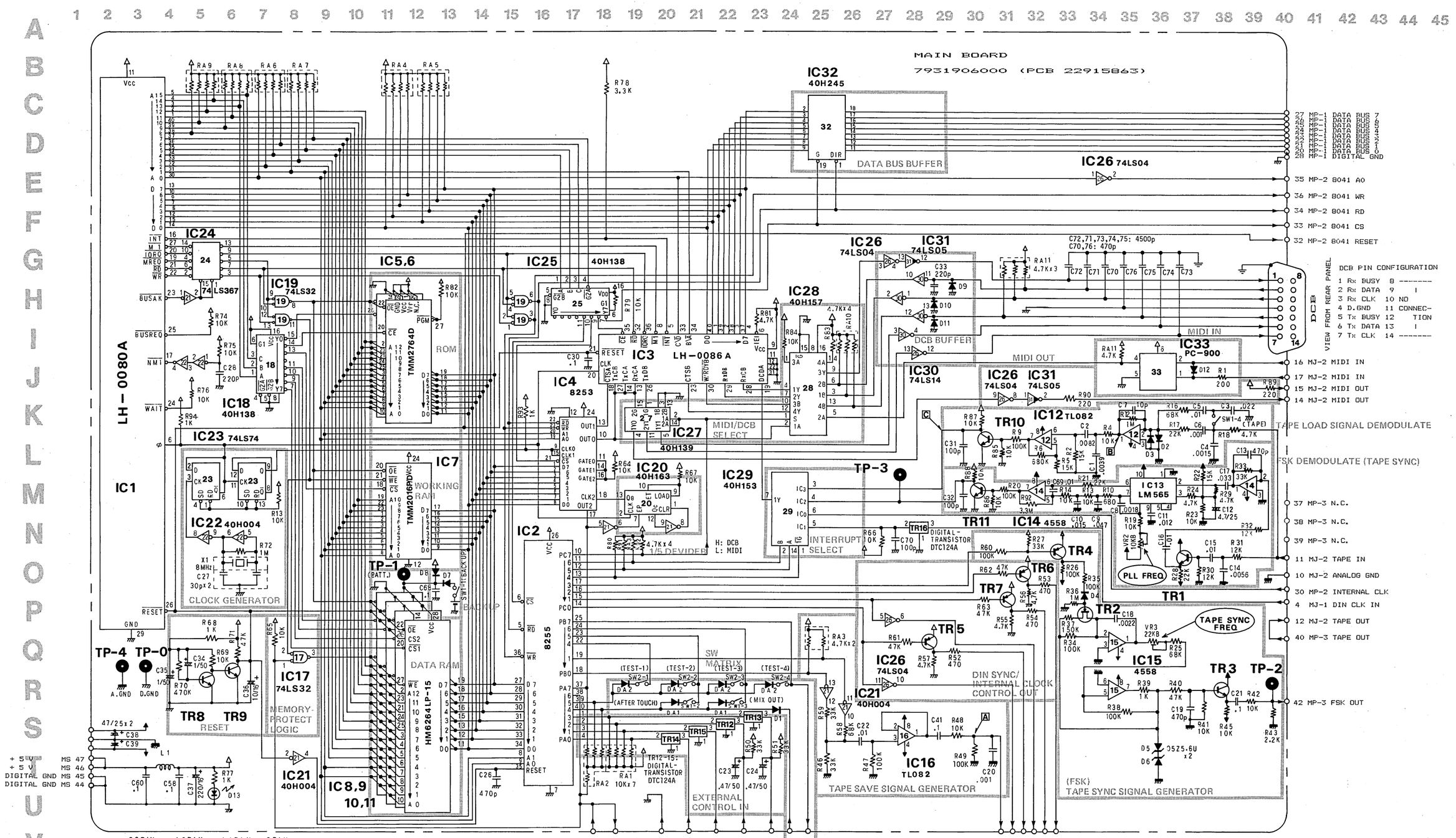
NOTE: UNLESS OTHERWISE SPECIFIED
ALL PNP TRANSISTORS ARE 2SA1015(GR)
ALL NPN TRANSISTORS ARE 2SC1815(GR)
ALL DIODES ARE 1S2473
HIGHEST NUMBER: IC10,TR8,D67,C28
R52,RA3,VR2,L2

MAIN BOARD

7931906000

(pcb 22915863)



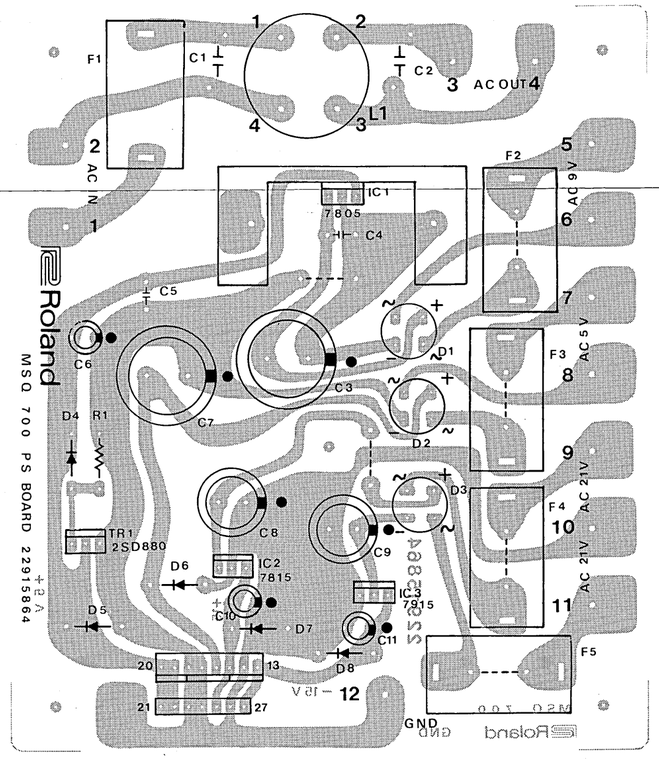


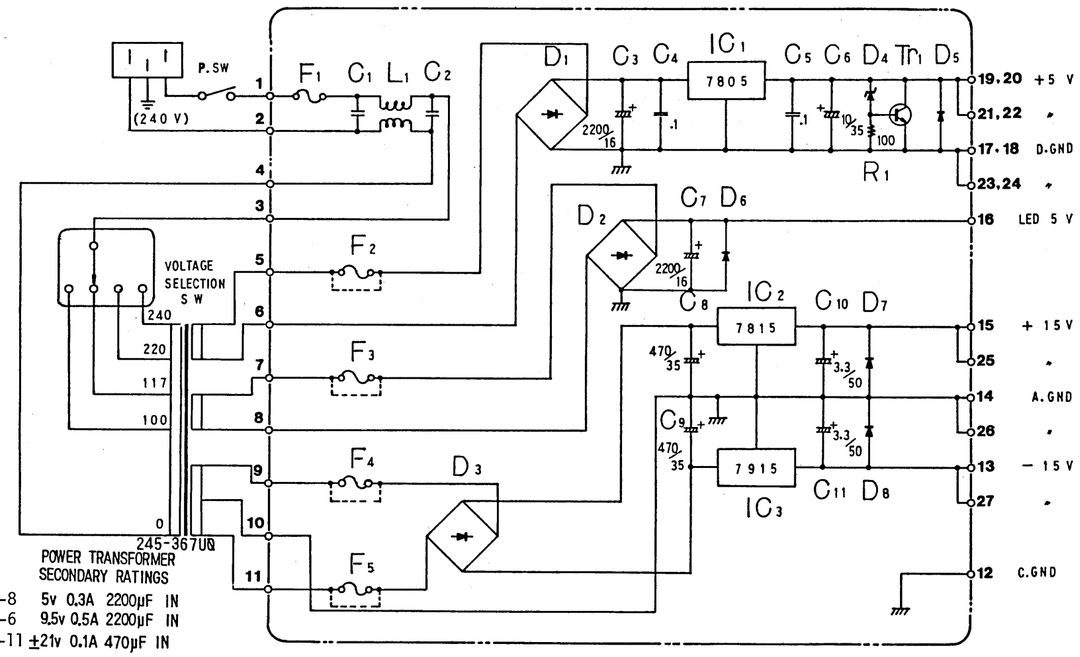
NOTE1: UNLESS OTHERWISE SPECIFIED
ALL PNP TRANSISTORS ARE 2SA1015(GR)
ALL NPN TRANSISTORS ARE 2SC1815(GR)
ALL FET: ARE 2SK30ATM(GR)
ALL DIODES ARE 1S2473
VACANT NUMBER:
C54,55,56 : VR1 : R3,7,8,11,14,15
HIGHEST NUMBER:
IC 33 : TR 11 : DA 2 : D 13 : C 70
R 92 : RA 11

NOTE2: X1+ C27 ==> CERAMIC RESONATOR (KMFC1034T)
L1 : COIL SN8D-500
TR12-TR16 : DIGITAL TRANSISTOR DTC124A
SW1,SW2 : DIP SW
C41 : MYLAR
C18 : STYROL
C68:RPE132F104Z50V
BATTERY:ER-6(LITHIUM)

POWER SUPPLY BOARD

7931905100 (pcb 22915864) 100/117V
7931905400 (pcb 22915864) 220/240V





IC1 μPC 7805H
IC2 " 7815H
IC3 " 7915H
Tr1 2SD880
C1,2 DE7150F472MVA1
L1 FK0B160MH15
D1,2,3 W-02
D4 05Z5.6U
D5,6,7,8 1SR35-200

100/117V
F1: GGS-0.8AUL
F2-5: JUMPER

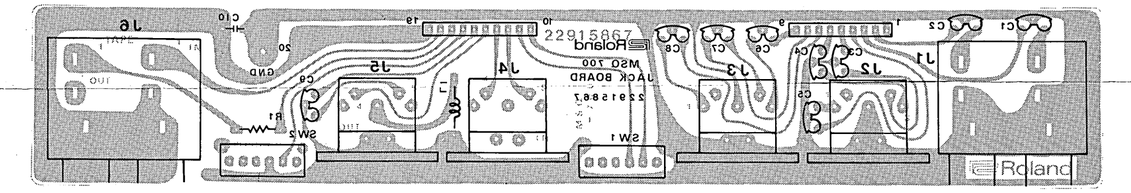
220/240V
F1,4,5: CEE-T250MA
F2,3 : CEE-T1.6A

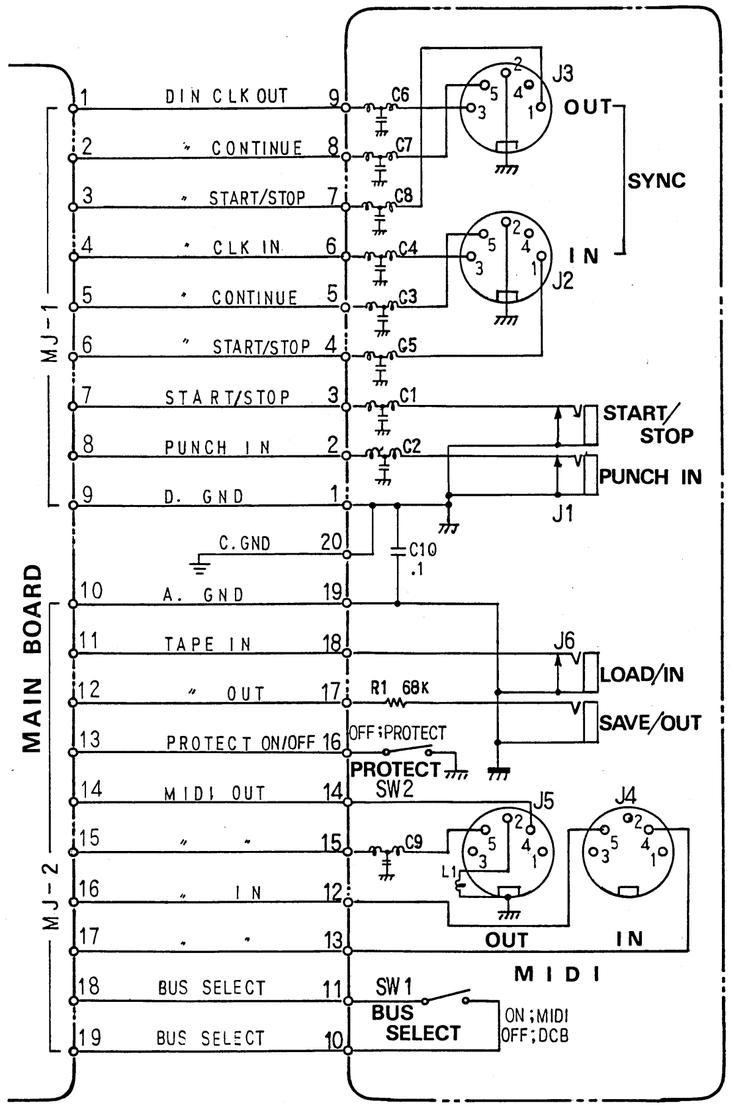
POWER SUPPLY BOARD
7931905100 (100/117V)
7931905400 (220/240V)
(PCB 22915864)

JACK BOARD

7931908000
(pcb 22915867)

View from foil side





C1,2,3,4,5,6,7,8,9:
DSS310-55B222M
EMI FILTERS

L1:ELE-A120KA

JACK BOARD 7931908000
(PCB 22915867)

TESTING & ADJUSTING

TEST MODE

MSQ-700 is furnished with TEST software that can be evoked when the unit is in the TEST mode.

ENTERING TEST MODE

While pressing RESET and STOP simultaneously, turn the power ON.
OR
Place SW2 (on the Main Board) into ON and turn the power ON.
The panel will display "CHECK" showing that the unit is now in the Test mode.The display will change to and stay at the TEST number while a test sequence is running.

1. BEAT PER MEASURE

1-1. Press TRACK No.1. The display will change to No.1 and PLAY No.1 LED (green) will light.

1-2. Slide B/MEASURE knob by steps in the order from 1 to 8. The LOAD LEDs (red) should light from 1 to 8 respectively as step proceeds.

2. DIP SWITCH READING

2-1. Press TRACK No.2; display will change to 2 and PLAY No.2 LED will light.

2-2. Place BUS SELECT switch on the rear panel into MIDI; LOAD No.1 will light. Turn the selector to DCB; the No.1 will go off.

2-3. In the simillar manner test the DIP switches on the Main Board.

TRACK NO.	DIP SWITCH
1	BUS SELECT (ON:MIDI)
2	SW1-2
3	SW1-3
4	NONE
5	SW2-4
6	SW2-3
7	SW2-2
8	SW2-1

3. EXTERNAL CONTROLS READING

3-1. Press TRACK No.3; display will change to 3 and PLAY No.3 will light.

3-2. The LOAD LEDs 5-8 should be lit when an appropriate control signal is applied to the jack respectively.

TRACK	SOCKET
5	EXT CONTROL PUNCH IN (+5v or open)
6	EXT CONTROL START/STOP (+5V or open)
7	SYNC CONTINUE (+5V)
8	SYNC START/STOP (+5V)

4. RAM CHECKING

4-1. Turn PROTECT to OFF.

4-2. Press TRACK No.4; display will change to 4 and PLAY No.4 will light.

4-3. The display will read "Good" after 5 seconds when the RAMs are kept intact.

4-4. The display will read "Err" if any RAM is defective; the LOAD LED corresponding to the RAM will blink. However, if all of the four LEDs are blinking at the same time, circuits common to the RAMs should be checked.

TRACK NO.	IC NO.
1	7
2	8
3	9
4	10

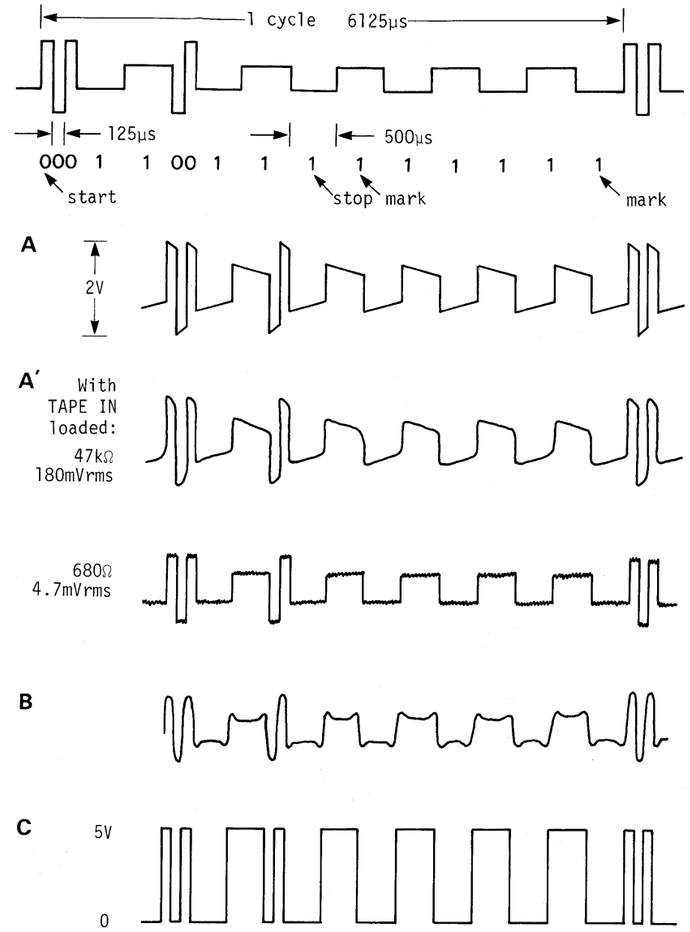
5. SERIAL IN/OUT

5-1. Connect MIDI IN and MIDI OUT together; Press TRACK No.5; Display will change to 5; PLAY No.5 will light; LOAD LEDs will blink at random.
The Display will change to "Good" after 7 seconds when the circuits are intact.

5-2. The display will indicate "Err" if the circuits are defective or if the cable beween the sockes are loosely connected.

CHECKING CMT INTERFACE

1. Connect the oscilloscope to SAVE OUT (or the point A in the Main Board schematic diagram).
2. Place the mode into TAPE.
3. While pressing CLOCK,tap VERIFY. The display will read "Hrch" and the waveforms in the figure belelow will be displayed on the scope.
4. Save the data to the tape.
5. Connect the scope to the point C or B in the shematic diagram.
6. Load data and observe the oscilloscpe; the waveforms should be as shown below.



ADJUSTMENTS

1. TEMPO Panel Board

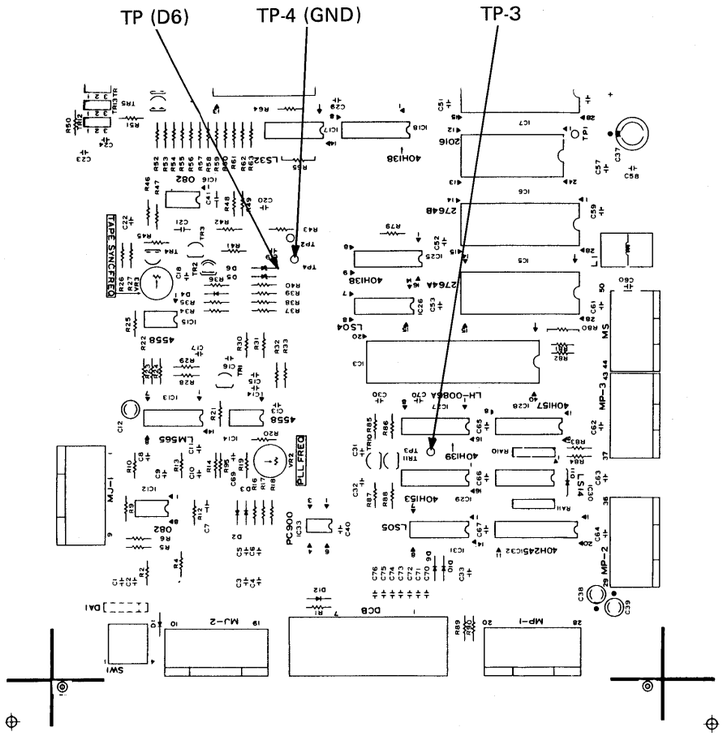
PANEL CONTROLS:

MODE : NORMAL	CLOCK: INT
DISPLAY: TEMPO	TEMPO: FAST

1-1. Adjust VR1 so that the display reads 265.
1-2. Turn TEMPO fully counterclockwise(SLOW) and verify that the reading is below 30.

2. TAPE SYNC FRQ. Main Board

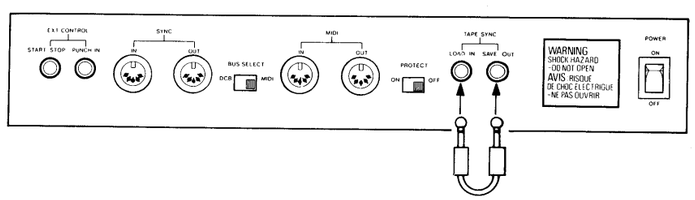
2-1. Connect the scope or frequency counter to TP(D6).
2-2. Adjust VR3 for 1.3kHz+/-20%(0.77ms).



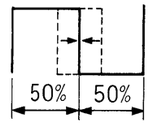
3. PLL FREQ. (FSK DEMO.) Main Board

PANEL CONTROLS:
BEAT PER MEASURE: 1 MODE: NORMAL
CLOCK: INT

CAUTION: This adjustment must follow the 2 TAPE SYNC FRQ.



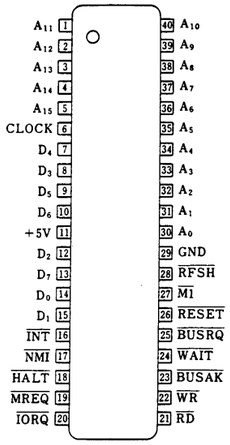
3-1. Connect the scope to TP-3.
3-2. Press LOAD and adjust VR2 for a 50% duty cycle.



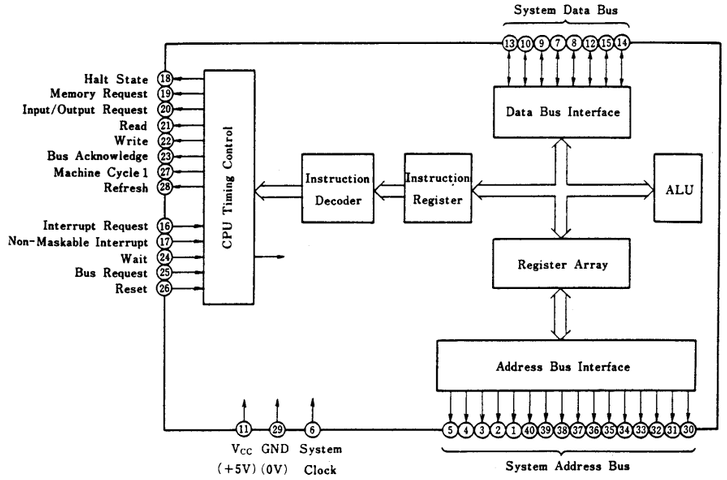
IC DATA

LH0080A

Terminal Connections (Top View)

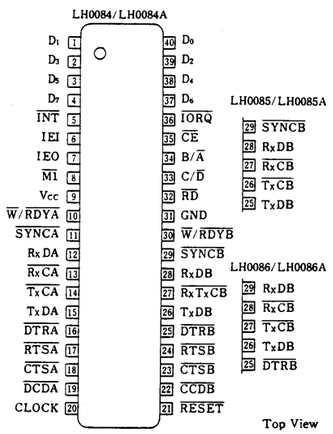


Block Diagram



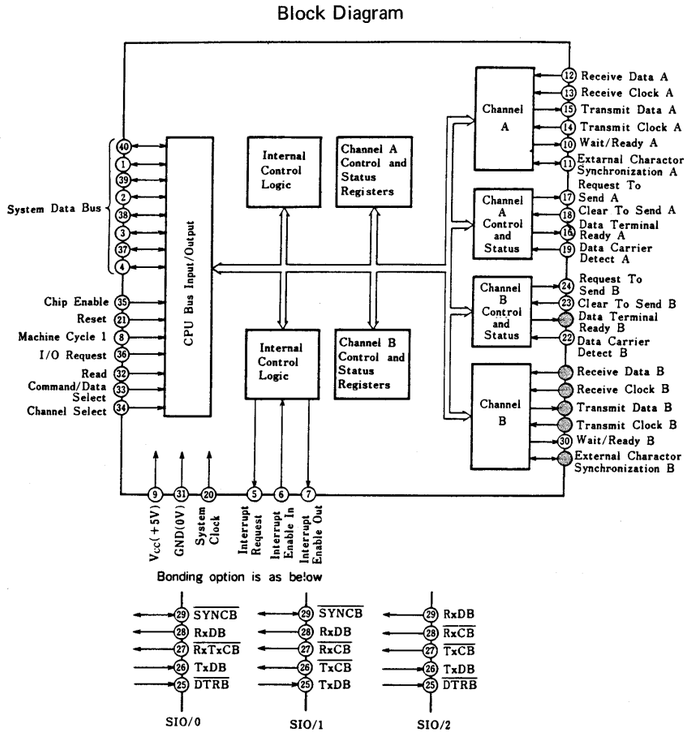
LH0086A

Terminal Connections (Top View)



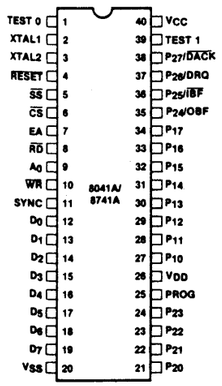
Top View

Block Diagram



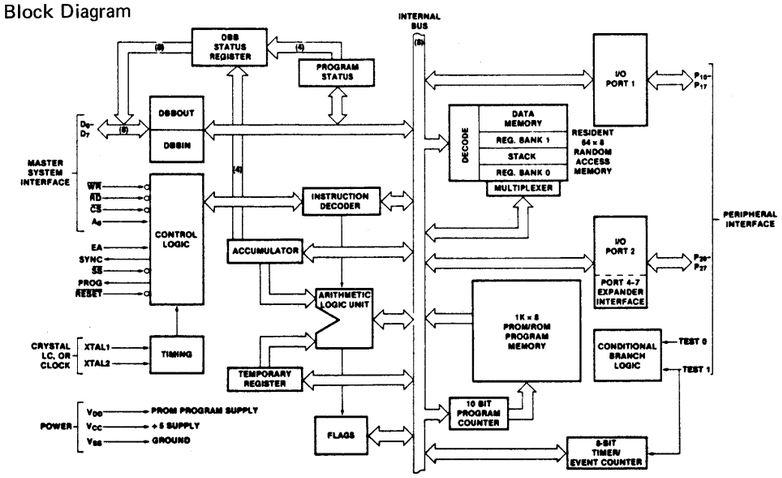
M5L8041A

Pin Configuration



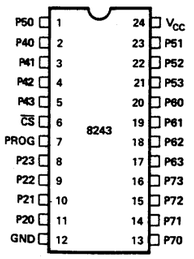
(Top View)

Block Diagram



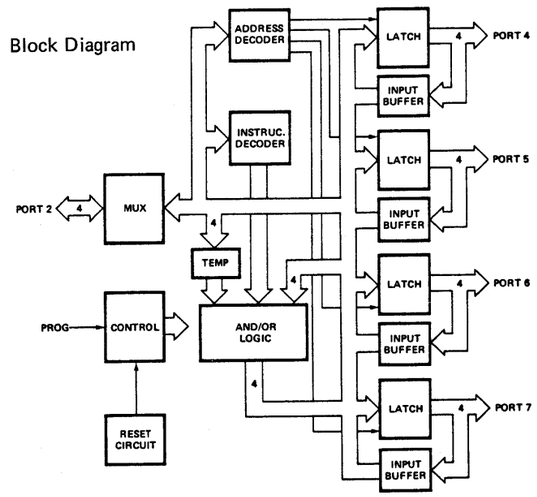
M5L8243A

Pin Configuration



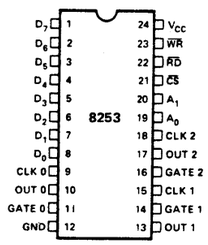
(Top View)

Block Diagram



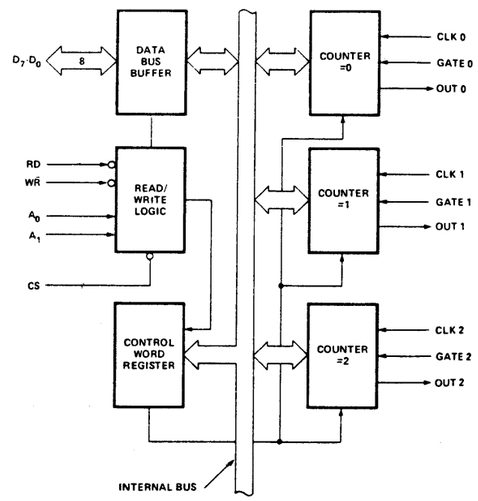
M5L8253

Pin Configuration



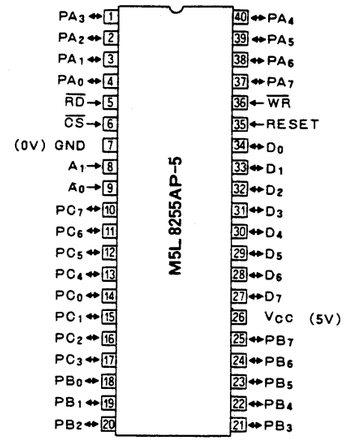
(Top View)

Block Diagram



M5L8255

Pin Configuration (Top View)

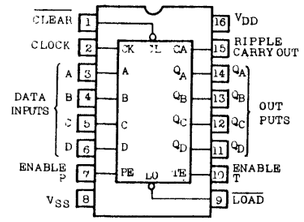


Basic Operation

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

40H163

Pin Configuration



(Top View)

Truth Table

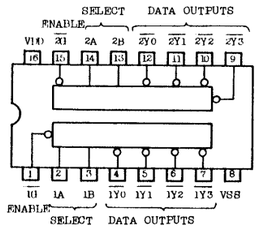
INPUTS									OUTPUTS				
CLEAR	LOAD	ENABLE P	ENABLE T	CLOCK	DATA INPUTS A	B	C	D	DATA OUTPUTS Q_A	Q_B	Q_C	Q_D	RIPPLE CARRY OUT
*	*	L	*	↓	Don't Care				No change				L
*	*	H	*	↓	Don't Care				No change				Able
L	*	*	*	◇	Don't Care				All Reset				L
H	*	L	L	↑	Program Data				Program Output				L
H	*	H	L	↑	Program Data				Program Output				Able
H	*	L	H	↑	Don't Care				No count				L
H	L	H	H	↑	Don't Care				No count				Able
H	H	H	H	↑	Don't Care				Count up				Able

* Don't care

◇ { TC40H160P/161P Don't Care
TC40H162P/163P Sync on rising edge of CLOK

40H139

Pin Configuration



(Top View)

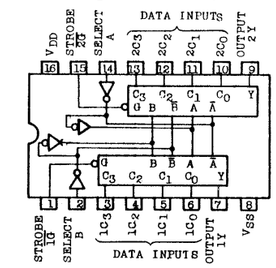
Truth Table

INPUTS			OUTPUTS			
ENABLE $\overline{G}$	SELECT A	B	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	※	※	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

※= Don't care

40H153

Pin Configuration (Top View)



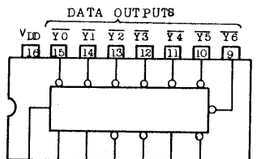
Truth Table

INPUTS							OUTPUT
SELECT A	B	DATA C_0	C_1	C_2	C_3	STROBE $\overline{G}$	Y
※	※	※	※	※	※	H	L
L	L	L	※	※	※	L	L
L	L	H	※	※	※	L	H
H	L	※	L	※	※	L	L
H	L	※	H	※	※	L	H
L	H	※	※	L	※	L	L
L	H	※	※	H	※	L	H
H	H	※	※	※	L	L	L
H	H	※	※	※	H	L	H

※= Don't Care

40H138

Pin Configuration



(Top View)

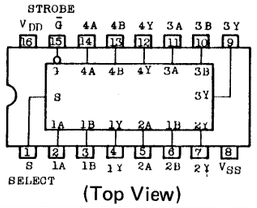
Truth Table

INPUTS						OUTPUTS							
ENABLE G1	$\overline{G2A}$	$\overline{G2B}$	SELECT A	B	C	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Don't care

40H157

Pin Configuration



(Top View)

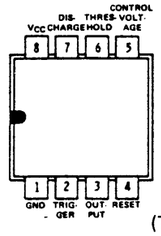
Truth Table

INPUTS				OUTPUTS	
STROBE	SELECT	DATA		H157P	H158P
$\overline{G}$	S	A	B	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

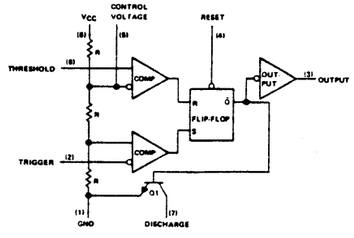
X=Don't Care

555

Pin Configuration

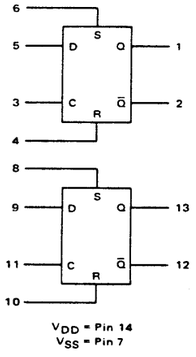


(Top View)



TC4013

Block Diagram



VDD = Pin 14
VSS = Pin 7

Truth Table

INPUTS				OUTPUTS	
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

No Change

X = Don't Care
† = Level Change

MIDI IMPLEMENTATION

March 30, 1984

1. RECOGNIZED RECEIVE DATA

1.1 Memorized messages when in LOAD mode

Status	Second	Third	Description	
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF	*1,2
1001 nnnn	0kkk kkkk	0000 0000	Note OFF	*1
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON	*1
1010 nnnn	0kkk kkkk	0vvv vvvv	Polyphonic Key Pressure	*3,4
1011 nnnn	0ccc cccc	0vvv vvvv	Control Change	*3,5
1100 nnnn	0ppp pppp		Program Change	*3
1101 nnnn	0vvv vvvv		Channel Pressure	*3,4
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Wheel Change	*3
1011 nnnn	0111 1010	0vvv vvvv	Local Control	*3

1.2 Recognized only

Status	Second	Third	Description	
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF	*6
1011 nnnn	0111 1100	0000 0000	OMNI OFF	*7
1011 nnnn	0111 1101	0000 0000	OMNI ON	*7
1011 nnnn	0111 1110	0000 0000	MONO ON	*7
1011 nnnn	0111 1111	0000 0000	POLY ON	*7

1.3 Recognized messages for sync.

Status	Description	
1111 1000	Timing Clock	*8
1111 1010	Start	
1111 1011	Continue	
1111 1100	Stop	

NOTES:
*1 kkkkkkk = 9 thru 120 (real), 0 thru 127 (recognized).
*2 When in STEP LOAD mode, note OFF velocity is ignored (memorized as 1001nnnn, 0kkkkkkk, 00000000).
*3 Memorized when in REAL TIME LOAD mode.
*4 When AFTER TOUCH switch on the rear panel is ON.
*5 ccccccc = 0 thru 121.
*6 When all notes are not OFF, this unit creats OFF for all ON notes.
*7 Recognized as only an ALL NOTES OFF.
*8 When the CLOCK switch is set to MIDI.

2. TRANSMITTED DATA

2.1 All memorized messages when in PLAY mode.

2.2 All received messages. *1

2.3 Internally originated messages.

Status	Second	Third	Description	
1111 1000			Timing Clock	
1111 1010			Start	
1111 1011			Continue	
1111 1100			Stop	
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF	*2
1011 nnnn	0111 1100	0000 0000	OMNI OFF	*3
1011 nnnn	0111 1111	0000 0000	POLY ON	*3

NOTES:
*1 When MIX OUT switch is ON. (In PLAY mode, received Mode Messages are not transmitted.)
*2 When all notes turn OFF.
*3 On power up or when BUS SELECT switch is set to MIDI, these MODE MESSAGES are transmitted for all channels.

GENERAL PRECAUTIONS ON MIDI CONNECTION

Although all MIDI instruments function to MIDI specification, some precautions must be taken for satisfactory operation.
This is mainly due to MIDI revision. One of primary procedures to be correctly followed is setting of "Channel Mode" otherwise MIDI function fails from the beginning. Also remember that MIDI information is effective only when receiving device can recognize a given message and has software and hardware that duplicate function defined by the message.
On power up most Roland products complying with MIDI specification 1.0 default to OMNI ON, POLY. On the contrary, they transmit OMNI OFF and POLY mode messages from MIDI OUT jack. The reason is as follows.

Receiving instrument must be reset to OMNI OFF mode when it is to accormodate voice messages sent over the channel to which it is currently assigned while other voice messages are present in other channels. (Example. a system consists of one master and more than one slave, each assigned to different channel.) However, some instruments are incapable of changing modes on the front panel and need external OMNI OFF message.

To cure this problem a system including such instruments as slaves should be configured as below.

MASTER (1st slave)	SLAVE(s)
capable of producing OMNI OFF message (or POLY, see NOTES) 1. on panel or other means at desired time 2. on power up	incapable of turning to OMNI OFF mode by itself

In the above combination:

1. Slave must be powered ON before the master is turned ON. (When the second slave connects to MIDI OUT of the first slave, it is the first to be turned ON.)

2. Master and Slave(s) must be set in the same channel since mode messages will be recognized by the slave only when set in the channel to which the slave's receiver has been assigned.

NOTES:
1. Roland products with preliminary MIDI turn to OMNI OFF upon receiving POLY mode ON.

2. MSQ-700 sends OMNI OFF and POLY ON messages on power-up in all channels.