SDE-2000 SERVICE NOTES

First Edition

SPECIFICATIONS

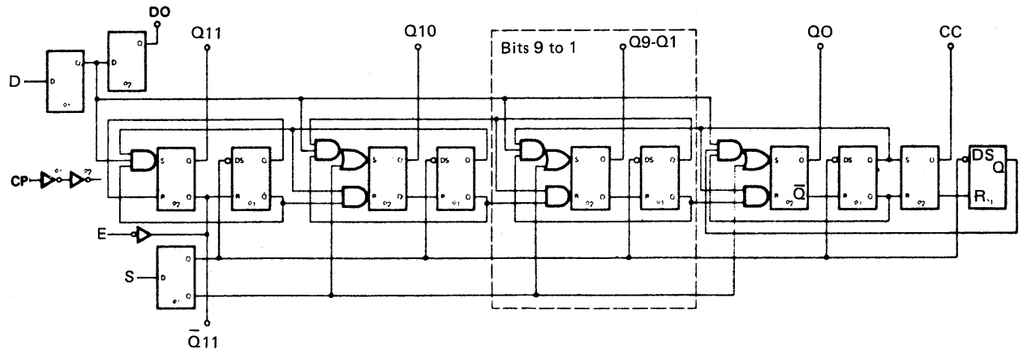
*** DIGITAL DELAY * SDE-2000**

Input	Level	+4 dBm (+29 dBm max) –20 dBm (+5 dBm max)
	Impedance	56kΩ
Output	Level	+4 dBm (+18 dBm max) into 600Ω load –20 dBm (–8 dBm max) into 10kΩ load
	Impedance	100Ω at +4 dBm position 650Ω at –20 dBm position, Mixed 550Ω at –20 dBm position, Delay
Feedback	Send	Level : +4 dBm (+16 dBm max) Impedance : 100Ω
	Return	Level : +4 dBm (+19 dBm max) Impedance : 78kΩ
CV In	Modulation CV	Operation Voltage : 0 to +10V (±20V, allowable) Impedance : 90kΩ
General Performance	Delay Time	0 to 320 ms 0 to 640 ms (in 1 ms steps)
	Delay Accuracy	±0.5%
	Frequency Response	10 Hz to 100 kHz +0, –1 dB at Direct 10 Hz to 16 kHz +0.5, –3 dB at Delay, 0 to 320 ms 10 Hz to 7.2 kHz +0.5, –3 dB at Delay, 0 to 640 ms
	Signal to Noise Ratio (IHF A) at rated input & output	90 dB, Direct 90 dB, Delay
	Dynamic Range (IHF A)	Greater than 112 dB, Direct 90 dB, Delay
	Total Harmonic Distortion at rated input & output Ref. 1 kHz	Less than 0.05%, Direct 0.08% typ, 0.2% max, Delay
Power Consumption	27W(117V), 30W(220V, 240V)	
Dimensions	482(W) x 47(H) x 355(D) mm (19 x 1.85 x 14 in.) 19" (EIA-1U) rack mount	
Weight	5.5kg (12 lbs.)	

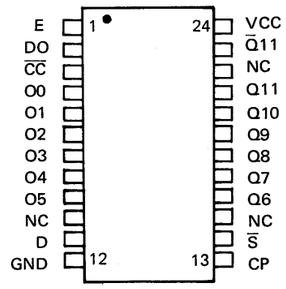
Am25L04

Low-Power, Twelve-Bit Successive Approximation Registers

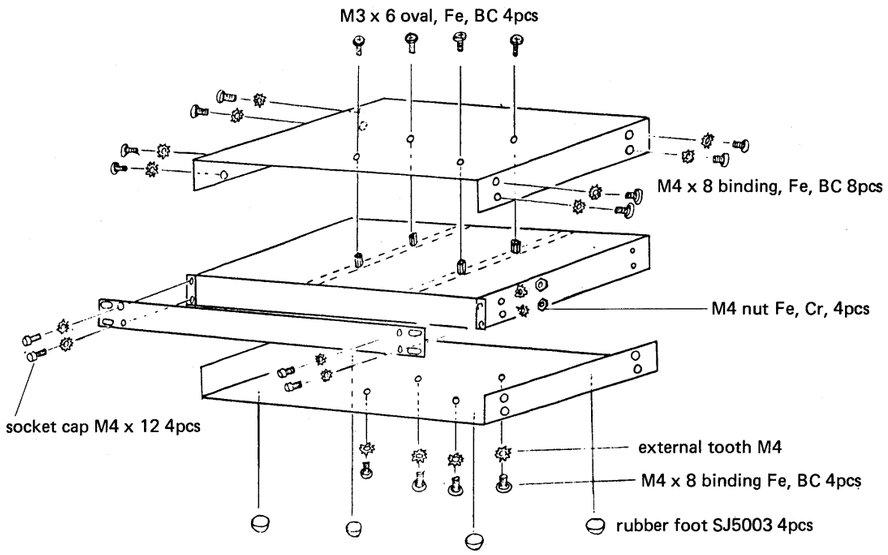
LOGIC DIAGRAMS

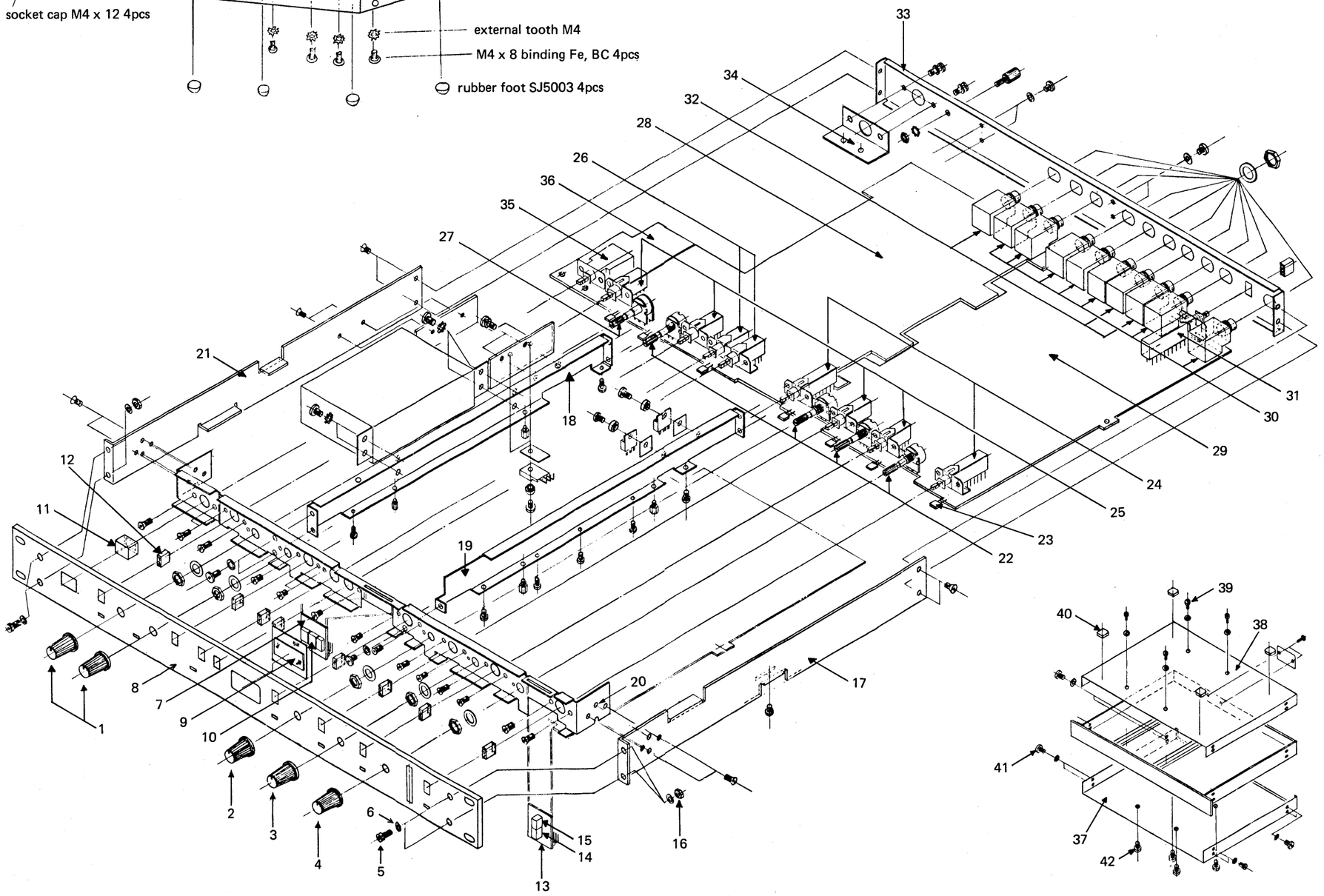


CONNECTION DIAGRAM
Top View



The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and s set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. The device accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output (and the DO output) when the clock goes from LOW-to-HIGH. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration. The register is reset by holding the S (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state Q11 LOW, and all the remaining register outputs HIGH. The CC (Conversion Complete) signal is also set HIGH at this time. After the clock has gone HIGH resetting the register, the S signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q11 register bit and the Q10 register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the Q10 register bit and Q9 is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the CC signal goes LOW, and the register is inhibited from further change until reset by a Start-signal.





1. Knob N-176 (2247017600)
2. Knob N-175 (2247017500)
3. Knob N-174 (2247017400)
4. Knob N-173 (2247017300)
5. Hex Socket Cap 4 x 12mm Fe, BC
6. Internal Tooth Washer M4 Fe, BC
7. Front Panel N-278B (2221027802)
8. DISPLAY BOARD OP4114-130 (7411413002)
9. Escutcheon N-302 (2222030200)
10. LED TLR312 (15029125)
11. Button N-506 (2247050600)
12. Button N-514 (12470514)
13. LEVEL METER BOARD OP4114-120 (7411412001)
14. LED (red) LD-002RB (15029106)
15. LED (green) LD-002GB (15029107)
16. Hex Nut M4 Fe, Cr
17. Chassis N-289 (2281028900)
18. Chassis N-300 (2281030000)
19. Chassis N-288 (2281028800)
20. Chassis N-287 (2281028700)
21. Power Transformer
    PT-N-250N (22450250NO) 100V
    PT-N-251C (22450251CO) 117V
    PT-N-252D (22450252DO) 220/240V
22. Pot. EVH-6PAP30B54-50kB (13219337)
23. LED GL-9PR2 (15029128)
24. Push Switch N-318 SUF-12 (13129318)
25. Push Switch N-317 SUF-12 (13129317)
26. Push Switch N-528 SUF-22 (13129528)
27. Pot. EWK-ENAP30A15-100kA (13219338)
28. CPU BOARD GL4114-090 (7411409012)
29. EFFECT BOARD ET4114-060 (7411406010)
30. Jack HLJ-1315-01-100 (13449222)
31. Push Switch N-319 SUF-12 (13129319)
32. Jack HLJ-1315-01-010 (13449221)
33. Rear Panel N-279 (2221027900)
34. Holder N-234 (2219023400)
35. Power Switch
    SDG-5P001 (13129101) 100V, 220/240V
    SDG-5P001 CSA (13129102) 117V
36. PRIMARY FUSE BOARD
    PS4114-141 (7411414100) 100V
    PS4114-143 (7411414300) 117V
    PS4114-144 (7411414400) 220/240V
37. Top Cover N-182 (2202018200)
38. Bottom Cover N-181 (2202018100)
39. Screw 4 x 8mm binding Fe, BC
40. Base N-313 (22350313)
41. Screw 4 x 6mm binding Fe, BC
42. Screw 3 x 6mm oval Fe, BC

PARTS LIST

CASE

2221027802	Front Panel	N-278B
2221027900	Rear Panel	N-279
2219023400	Holder	N-234
2281030000	Chassis	N-300
2281028700	Chassis	N-287
2281028800	Chassis	N-288
2281028900	Chassis	N-289
2202018200	Top Cover	N-182
2202018100	Bottom Cover	N-181
22350313	Base	N-313
2222030200	Escutcheon	N-302

KNOB, BUTTON

2247017300	Knob	N-173 ORN
2247017400	Knob	N-174 YEL
2247017500	Knob	N-175 GRN
2247017600	Knob	N-176 BLU
12470514	Button	N-514
2247050600	Button	N-506

SWITCH

13129317	SUF-12	N-317 push
13129318	SUF-12	N-318 push
13129319	SUF-12	N-319 push
13129528	SUF-22	N-528 push
13129101	SDG-5P001	push power 100V, 220/240V
13129102	SDG-5P001 CSA	push power 117V
2224011500	Dust Cover N-115	
12439206	PRBD-4 reed relay	

JACK

13449221	HLJ-1315-01-010 w/switch
13449222	HLJ-1315-01-100

TRANSFORMER, COIL

22450250N0	PT-N-250N	100V
22450251C0	PT-N-251C	117V
22450252D0	PT-N-252D	220/240V
22440211O0	OSC Coil	24M-067-333

PCB

7411406010	EFFECT BOARD	ET4114-060 (pcb 2291050402)
7411409012	CPU BOARD	GL4114-090 (pcb 2291050500)
7411413002	DISPLAY BOARD	OP4114-130 (pcb 2291050600)
7411412001	LEVEL METER BOARD	OP4114-120 (pcb 2291050700)
7411414100	PRIMARY FUSE BOARD	PS4114-141 (pcb 2291050800) 100V
7411414300	PRIMARY FUSE BOARD	PS4114-143 (pcb 2291050800) 117V
7411414400	PRIMARY FUSE BOARD	PS4114-144 (pcb 2291050800) 220/240V

POTENTIOMETER

13219337	EVH-6PAP30B54-50kB	
13219338	EWK-ENAP30A15-100kA	
13299111	H1051A009-2.2kB	trimmer
13299113	H1051A011-4.7kB	trimmer
13299114	H1051A013-10kB	trimmer
13299117	H1051A019-100kB	trimmer

FUSE

12559105	SGA0001 1A 100/117V
12559106	SGA0002 2A 100/117V
12559510	CEE T400mA 220/240V
12559521	CEE T1.6mA 220/240V
12199519	Fuse Holder TF-758

IC

15179127	μPD-8049C	Single Component 8-Bit Microcomputer
15179310	μPD-416	16K Dynamic RAM
15219119	Am2504	12-Bit Successive Approximation Registers
15179606J0	Am27S19	256-Bit Generic Series Bipolar PROM
15169301H0	HD74LS00P	Quad 2 Input NAND
15169301H0	HD74LS83P	4-Bit Binary Full Adders
15169345H0	HD74LS83P	4-Bit Binary Full Adders
15169332H0	HD74LS157P	2 to 1 Data Selectors
15169322H0	HD74LD174P	Hex D-FFs
15169344	HD74LS257P	Quad 3 State 2 to 1 Data Selectors
15169325B0	M74LS393P	Dual 4-Bit Binary Counters
15169102X0	HD7406P	Hex O.C. Inverters
15169325B0	M74LS273P	Octal D-FFs
15169331X0	SN74LS244N	Octal 3 State Bus Buffers
15159307H0	HD14511B	BCD-to-Seven Segment Latch/Decoder/Driver
15189118	TL-082	OP Amp
15189105	μPC4558C	OP Amp
15219108	NE570N	Compander
15189111	LM311N	Voltage Comparators
15219120	Am6012DC	D/A Converter
15159115H0	HD14066BP	Quad Bilateral Switch
15219116	IR2E02	LED Driver
15199106F0	μA7805UC	Three Terminal Voltage Regulator
15199104F0	μA7812UC	Three Terminal Voltage Regulator
15199115	MC79L05CP	−5V Voltage Regulator

TRANSISTOR

15119803	2SB628-R
15119111	2SA970-GR
15119112	2SA1015-Y
15119113	2SA1015-GR
15129114	2SC1815-GR
15129115	2SC1815-Y
15129120	2SC2240-GR
15129817	2SD880-GR

FET

15139103	2SK30ATM-GR
15139106	2SK117-GR

DIODE

15019120	1S2473	
15019208	1SR-35	
15019216	GM-3Z	rectifier stack
15019236	W-02	rectifier stack
15019525	RD5.6E	zener
15029106	LD-002RB	LED (red)
15029107	LD-002GB	LED (green)
15029125	TLR-312	LED
15029128	GL-9PR2	LED
150192490X	KV-1226-X	variable-capacitance diode
or		
150192490Y	KV-1226-Y	variable-capacitance diode
12389804	CSA11.00MT	ceramic resonator
12389805	CSC300	thermocompensation capacitor

RESISTOR

13910101	RM8-472K	4.7K x 8 array
13839610F0	MO-4P 5W	cement
13769141D0	CRB-25FX	470 metal oxide
13769155D0	CRB-25FX	1.8k metal oxide
13769160D0	CRB-25FX	3k metal oxide
13769163D0	CRB-25FX	3.9k metal oxide
13769173D0	CRB-25FX	10k metal oxide
13769175D0	CRB-25FX	12k metal oxide
13769177D0	CRB-25FX	15k metal oxide

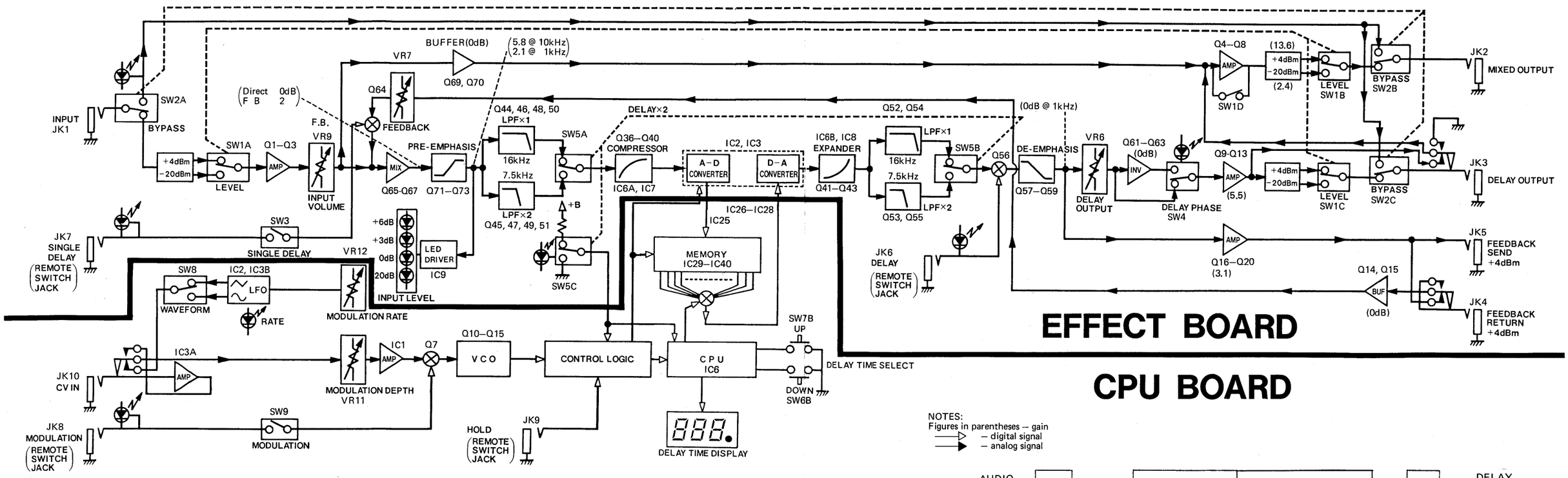
CAPACITOR

13549884M0	ECQM6103MZ .01μF	polypropylene 100V
13589455M0	ECQ-U2A103MF .01μF	polypropylene 220/240V
13589456M0	ECQ-U1A103MC .01μF	polypropylene 117V
13619711N0	CS15E1V4R7K1S 4.7μF	tantalum
13619803N0	CS15E1VR22K1STPD .22μF	tantalum
13619807N0	CS15E1VO10K1STPD 1μF	tantalum
13639154M0	ECEA1CS102 1000μF	electro.
13639155M0	ECEA1CS222 2200μF	electro.
13639174M0	ECEA1ES102 1000μF	electro.
13639194M0	ECEA1VS102 1000μF	electro.
13639281O0	MKH 100V 1μF	metalized
13649103M0	ECEA1CN100SB 10μF	bi-polar, electro.

OTHERS

2246043000	Heat Sink N-430	
13429142	Connector Housing EMC-S0560	5P
13429143	Connector Housing EMC-S0760	7P
13429144	Connector Housing EMC-S1060	10P
2341027900	Connector-Wiring Assy N-279	5P
2341028000	Connector-Wiring Assy N-280	7P
2341028100	Connector-Wiring Assy N-281	10P
2215050300	Long Nut 18.0mm	
2215052400	Boss Nut M3 x 8mm	

SDE-2000 BLOCK DIAGRAM



SDE-2000 Brief Description of Operation

In ordinary delay and echo machines, device used to record sound information is mostly tape, BBD or CCD. Unlike these, however, the SDE-2000 employs the device of RAM. The recording method here is the one called the PCM (pulse-coded-modulation). In this, the sound signals are sampled at first, which then amplitude-converted to the digital form suitable for storing on RAM. The mechanism employed in this SDE-2000 for the signal delay system could easily be understood through comparison with that of the tape method, as follows. (See Fig. A)

- The medium which corresponds to the tape is a set of RAMs.
- Think that the heads rotates clockwise along the tape. The speed is reduced to 1/2 when the unit is set to "DELAY x 2" (position to mean the delay time is doubled).
- In the figure, the position (A) as pointed out by R.H. is the RAM write address and that of P.B.H. (C) is of the read address. The variable length (D) as being the difference of the two becomes the required delay time.
  Note that, in this arrangement the position B is having more important meaning than D in handling the RAM addresses. The reason: The delay time which is firstly set on the Control Panel determines the address (B). With this B being added onto A, the address (C) is decided. On appearance, the read address (C) looks like rather in such a position as moving ahead. The fact is, the larger the value of B, the "shorter" becomes the delay time (D).

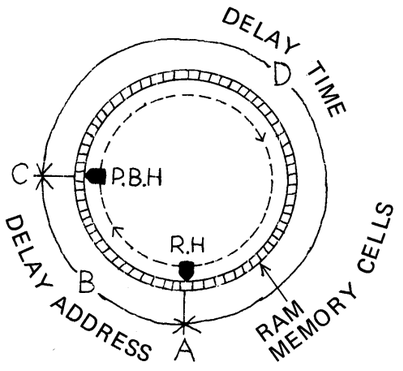
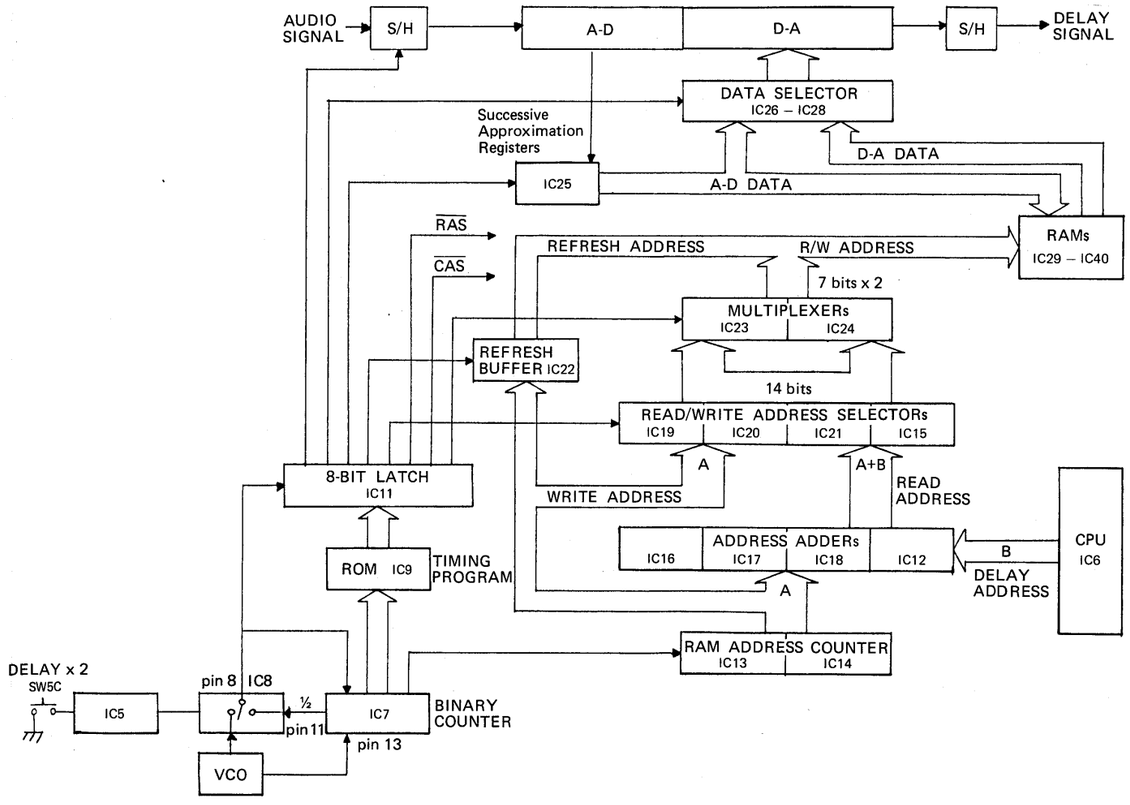


Fig. A

NOTES:
Figures in parentheses — gain
— digital signal
— analog signal



RECORD/PLAYBACK BLOCK

- The term of signal modulation through LFO or by means of external control voltage is in effect meant for just having the rotary speed of the heads varied in different degrees.

- Change in the head speed requires the corresponding changes on the access time to the memory cells and the duration of the signal being held on the heads (i.e. the time during which the read/write proceeds and the time for changing the data required on each – packing density).
  To meet these requirements, all the logic circuits (including the "heads" and CPU) are being operated on timing given by the clocks generated in VCO. When VCO fails to generate, all these circuits also cease operation.

CPU BORD

CLOCK GENERATOR

- **LFO (IC2, IC3B):**

  On Pin 1 of IC2A, square waves of 30Vp-p are produced. These waves are converted to triangle waves by IC2B, and again to sine waves through IC3B. When there is no external control (CV IN) applied, SW8 selects either one of these triangle or sine waves to transfer them through VR11 to the input pin 2 of IC1 on the CV LINEARIZER circuit.

- **CV IN (JK10, IC3A):**

  IC3A makes the input signals to be level shifted and expanded of the range, too. For instance, when external input (CV IN) is swinging from 0V to +10V, the voltage level to appear at the pin 1 is also being changed from –12V to +12V accordingly.
  When JK10, which incorporates a switch, is engaged, not only it works to disable the output of the LFO but also gives effect on the function of the delay time display circuit. More detail will be discussed when we come to the Display Circuit.

- **CV LINEARIZER (IC1A, D3 – D6):**

  The varactor (variable capacitance diode) KV-1 used on VCO (VCO will be discussed on the next paragraph) is the one having non-linear characteristics on its response to the applied voltage variation. The output of this CV LINEARIZER is therefore made to compensate it by having itself the curve that they both together can make a linear characteristic response.
  The FET switch Q7 functions to inhibit the modulation when a delay time is on the process of being set (SW6B and/or SW7A in off period).

- **VCO (Q10 – Q15):**

  Q10, Q11 and Q14 are the oscillation circuit. The frequency is under the control of the CV derived from Pin 7 of IC1. For instance:
  CV = +2V .... 0.35 MHz CV = ±0V .... 1.56 MHz
  CV = –12V .... 2.34 MHz

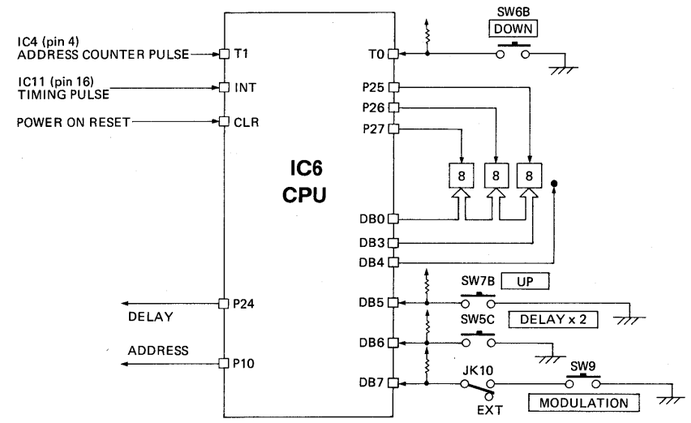
  Q13, D1 and D8 make the thermocompensation circuit for KV-1 (Note: the varactor tends to vary its capacitance with changes in temperature).

  Q15 is an AGC (automatic gain control). It functions to maintain VCO output amplitude constant through the frequency range.

  Q12 is used to make the VCO's output level compatible with TTL.

  Given these of the VCO clock timing, IC7 of the binary counter proceeds with execution of the program written on IC9. When the delay range, SW5C, is set to "DELAY x 2", the interval between the pulses adjacent to each other comes to be doubled.

DELAY ADDRESS, DELAY TIME DISPLAY



- CPU outputs the address (of B in Fig. A), with which the RAM memory cells can be accessed and the stored data be read out on a delayed time corresponding to the time setting on the Control Panel. CPU also performs all other operations related to the Delay Time Display.

  In about 5 sec after the power is turned on, the potential at the pin CLR goes high (H). The CPU then outputs such bits as having the delay address to go 0 (all pins to H) and the delay time to 0 ms. Thereafter, the CPU continues its operation in response to the instructions or data given on each respective pin or pins. Timing controls on them all are given by way of coincidence with the pulse application onto the pin INT.

  When SW6B (DOWN) and/or SW7B (UP) are in the push-closed state, CPU is to output the delay time address with the length proportional to the time length of SW6B and/or SW7B being kept depressed.

  CPU also outputs from the pins P25-P27 and DB0-DB3 the delay time display data, the product of an address as above multiplied by the time period between neighoring pulses applied from the Address Counter to the pin TI.
  These display data are then to be modified as follows in accordance with the status of the following two switches. Note that, during these operations, the delay address itself (B in Fig. A) is kept on as being set without any change.

- When SW5C is pushed in and placed at "DELAY x 2", the value of the data becomes halved (x 1/2).

- When JK10 is engaged and the associated jack switch becomes turned off (DB7 goes high), the display data will be changed successively in accordance with the change of the CV coming in onto EXT IN.

- If JK10 is left blank and MODULATION SW9 is placed at ON, the output from DB4 will become zero (0) and the DOT LED is turned OFF.

RAM ADDRESS

- **RAM ADDRESS COUNTER (IC13, IC14):**

  This address counter functions to increment the RAM address in synchronous with the clock sent from IC7 of the Binary Counter.

- **RAM READ ADDRESS ADDER (FULL ADDER) (IC12, IC16 – IC18):**

  The adder performs the arithmatic operation to add the value of B onto the write address A so as to get the address value with which the RAM cells can be accessed on a delayed timing corresponding to D in Fig. A.

- **ADDRESS SELECTOR (DATA SELECTOR) (IC15, IC19 – IC21):**

  This is to select either the address A or A+B in accordance with the mode selected to either READ or WRITE.

- **RAM ADDRESS MULTIPLEXER (IC23, IC24):**

  Since μPD416 is an RAM of 16K bits (16,384 = 2^{14} bits), a total 14-line address bus is required to make access to all of the memory cells.
  In μPD416, however, all cells are accessed by way of two addresses of ROW and COLUMN of 7 bits each. These addresses are output on a common bus on a time sharing basis in 2 times of 7 bits each.

ANALOG TO DIGITAL CONVERTER

The A to D conversion used in the SDE-2000 is a variation of Successive Approximations (SA) comprising an A-D converter, comparator and successive approximation registers; its process is slightly different from the conventional method as follows.

* Negative logic D-A conversion
* Comparator does not compare D-A output directly with the input signal. It compares voltage difference between input signal and D-A output with the fixed (zero) voltage (see Fig. 3).

To avoid confusion, a brief review of common SA method is in order.
In its simplest form, a conventional SA consists of a comparator, flip-flops and flip-flop set/reset control as shown in Fig. 1A.

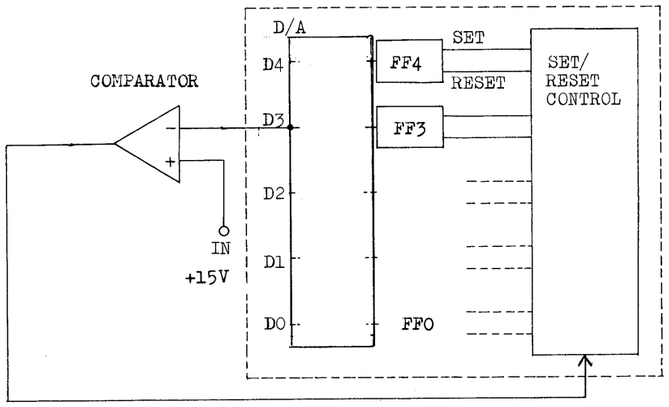


Fig. 1A

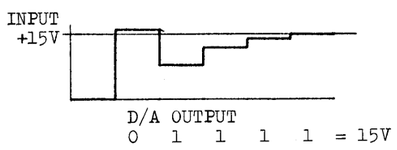


Fig. 1B

Assume that the system measures input voltages up to 31V with 5 bits, 1 bit/V resolution, for easier calculation. Initially, all FFs are reset, then FF4 is set which produces the most significant DC voltage (16V) at D4, which is in turn compared with input voltage (example, 15V). The comparator output goes low, resetting FF4, D4 goes 0 volts. FF3 is set in the same manner and delivers 8V at D3, exactly one-half the voltage of D4. The comparator output is high and FF3 remains set. Next, FF2 is set and total voltage (8V + 4V) from two FFs is now compared with the input voltage. The process is repeated for the remaining FFs. The state of the FFs after comparision against input voltage represents the digital value of the input signal. **(Fig. 1B)**

DUPLICATING THE PRECEDING PROCESS THROUGH A-D PORTION OF THE SDE-2000 CIRCUITRY

The voltage graph in Fig. 3A is an inverted image of Fig. 1B. When the most significant register in IC25 is set, it delivers low output (0 volts). Bits 01111 are sent via DATA SELECTOR to D-A converter IC3. With this data applied IO pin of IC3 draws from IC5 output the current which developes 15V across R87 (3K ohms). $\overline{IO}$ pin also draws from S/H output the current corresponding to inverted 01111 or 10000, causing voltage drop of 16V across R79 (3K ohms). The variation of currents at IO and $\overline{IO}$ pins is complementary, that is, the amount of current flowing into IC3 is always constant; when IO pin draws more current, $\overline{IO}$ pin decreases the same amount. (Differential Output Currents)
Voltage at (–) pin of IC2 becomes –1V (15V – 16V), changing its output to H, resetting D11 in IC25 – D11 changes from L to H. After all MSB 5 registers have been subtracted from input signal and tested against 0V, the configuration of registers will be 10000 = 16 (V). Why is 16V data proportional to 15V input? 16 volts is what will be developed across R87 and D-A output will be 31V – 16V = 15V.
Since comparator wants to know only relative voltage difference between the input pins, absolute voltage value is not necessary at (–) pin of IC2. Diodes keep the voltage range within diode drops (±0.6V).

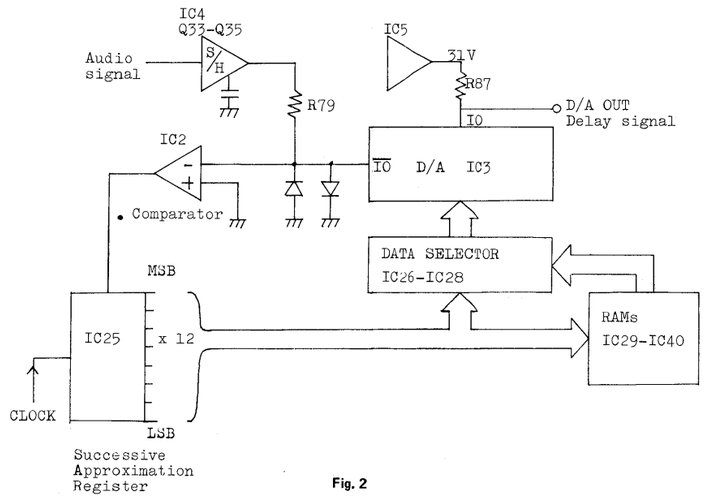


Fig. 2

NOTES:

In actual system, input signal ranges from 0V to 12V and is A-Ded with 12 bits, resolution is $12V/2^{12}$, approximate 3mV. In this example MBS 5 bits only are used and input signal is 15V as before.

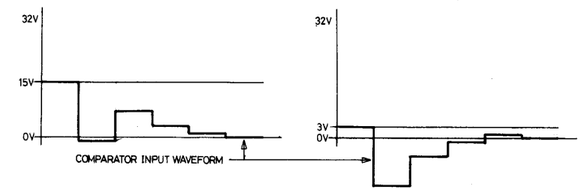


Fig. 3A

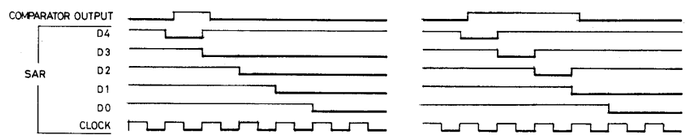
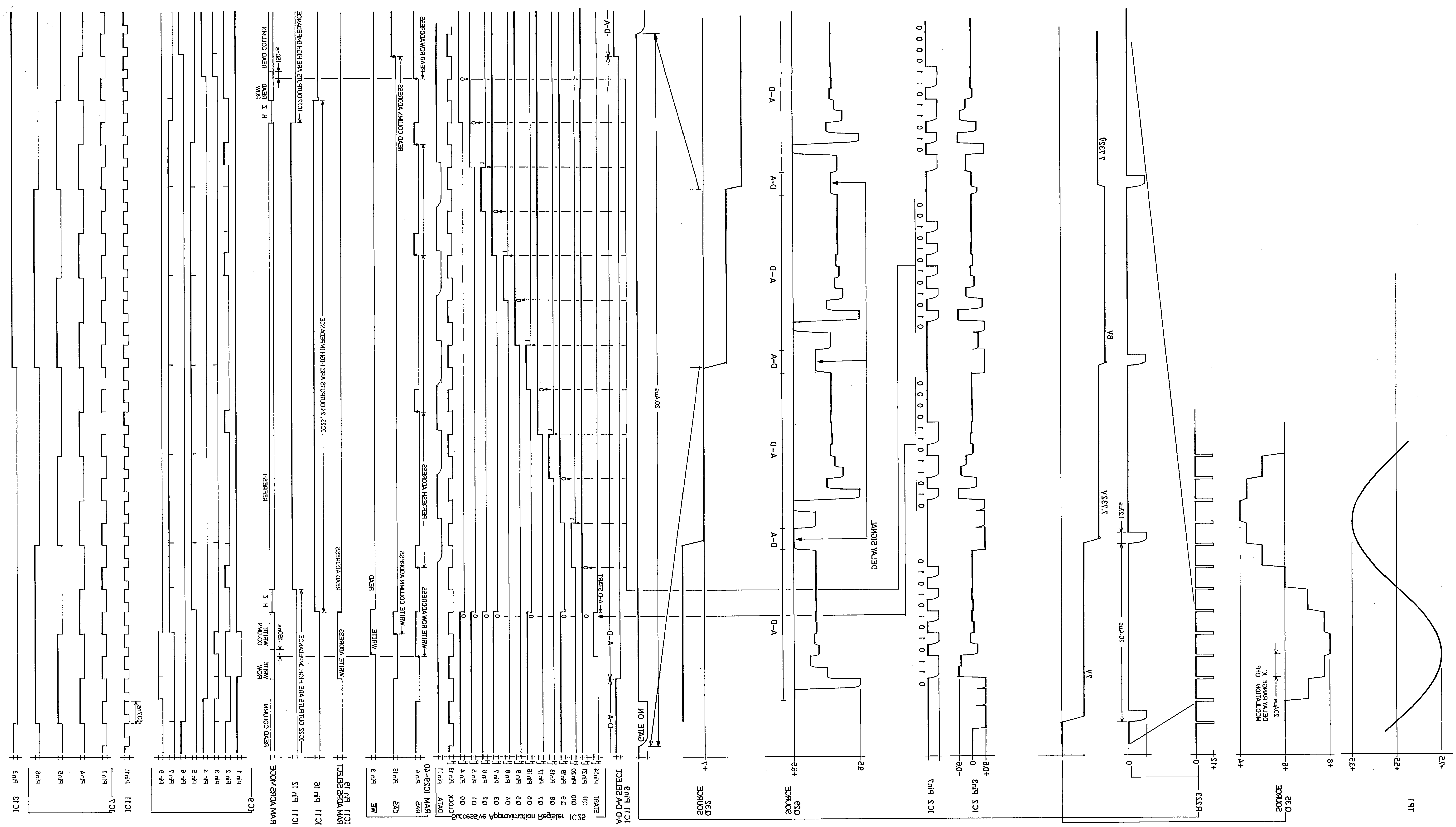


Fig. 3B



CPU BOARD

EFFECT BOARD

DISPLAY BOARD

RED LINE
AUDIO SIGNAL

Unless otherwise specified all diodes are IS2473

All npn transistors on CPU board are 2SC1815(GR)

All pnp transistors on CPU board are 2SA1015(GR)

Unless otherwise specified all diodes are IS2473

SWITCH ADDRESSES

SW	1	2	3	4	5	6	7	8	9
A	E, 2	B, 2	I, 2	J, 37	C, 19	K, 5	L, 5	M, 2	L, 2
B	C, 37	C, 38			I, 31	T, 27	T, 27		
C	E, 37	E, 38			P, 29				
D	D, 28								

	100 / 117 V	220 / 240V
F1	SGA 2A	CEE 16AT
F2	SGA 1A	CEE400mAT
F3,F4	SGA 1A	CEE400mAT

	100V	117V	220 / 240V
F5	SGA1A	SGA1A	CEE400mAT
C1	ECQM6103MZ	ECQM6103MZ	ECQU2A103MF
SW1	SDS-5P001	SDS-5P001	SDS-5P001
T1	2450250N	2450251C	2450250D0

CPU BOARD GL4114-090 (7411409012)(pcb 2291050500)

L1 SAMPLING CLK FREQ

DISPLAY BOARD

OP4114-130

(7411413002)

(pcb 2291050600)

LEVEL METER BOARD

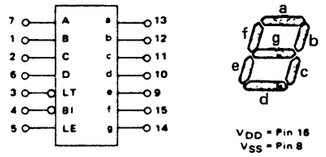
OP4114-120

(7411412001)

(pcb 2291050700)

HD14511B
TC4511P

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

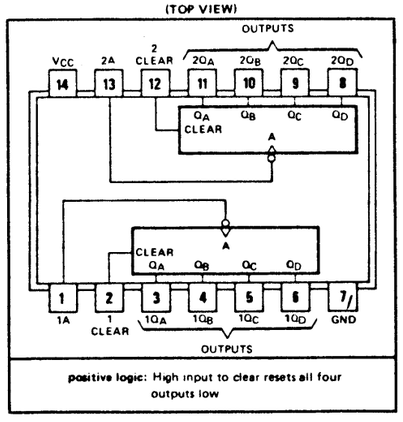
INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*	*	*	*	*	*	*	*

X = Don't Care
*Depends upon the BCD code previously applied when LE = 0

M74LS393P

DUAL 4-BIT DECADE AND BINARY COUNTERS

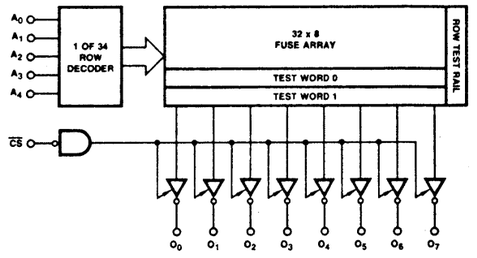
(TOP VIEW)



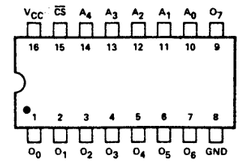
positive logic: High input to clear resets all four outputs low

Am27S19
256-Bit Generic Series Bipolar PROM

BLOCK DIAGRAM



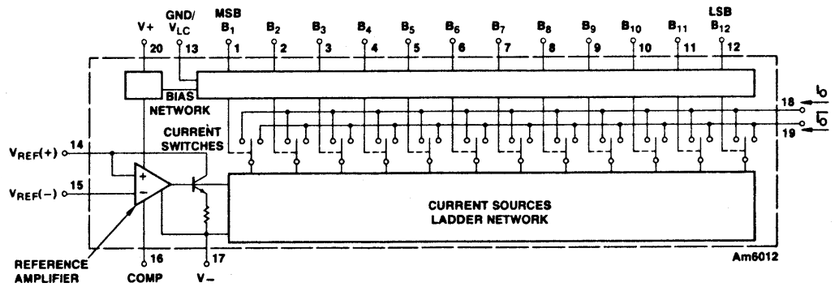
CONNECTION DIAGRAM
Top View



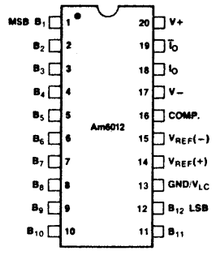
Three-state, standard 32 x 8 Schottky read only memory with a fusible link at each memory location stroring a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit. After programming, stored information is read on outputs O_0 – O_7 by applying unique binary addresses to A_0 – A_4 and holding the chip select input, CS, at a logic LOW. If the chip select input goes to a logic HIGH, O_0 – O_7 go to the off or high impedance state.

Am6012
12-Bit High-Speed Multiplying D/A Converter

FUNCTIONAL DIAGRAM

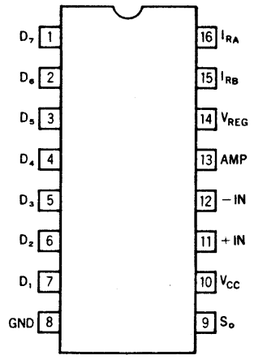


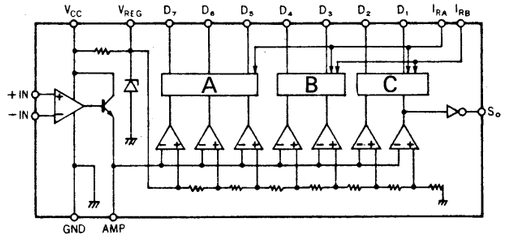
CONNECTION DIAGRAM – Top View



12-bit monotonicity	
Differential current outputs	
Differential nonlinearity	±0.025%
Full scale current	4mA

7-SEGMENT DRIVER

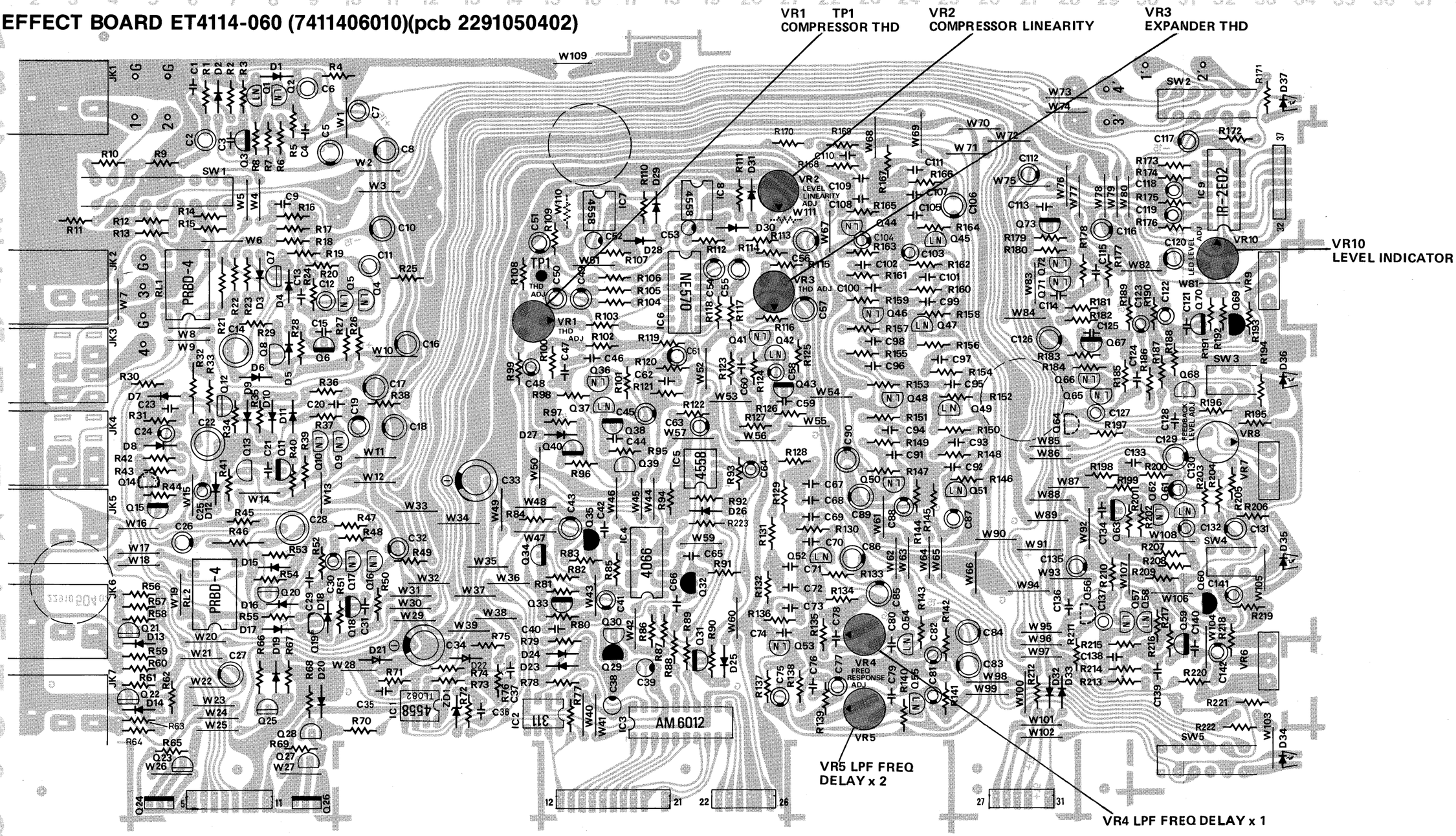


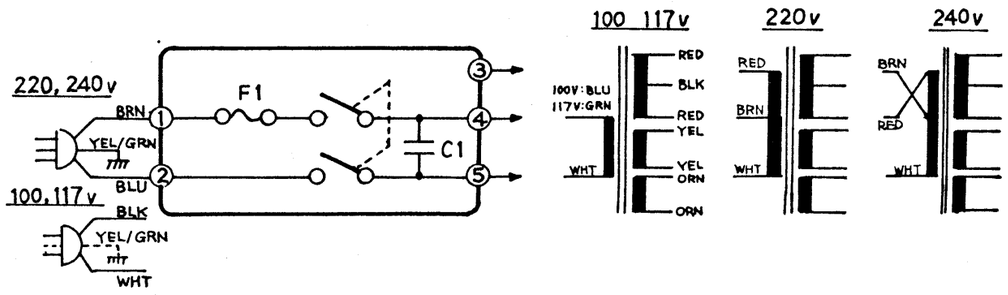


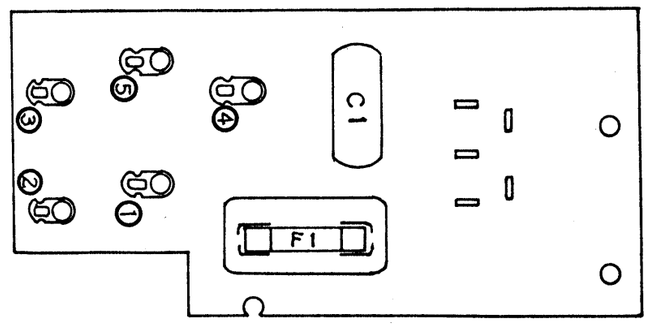
VREG	reference voltage output
IRA	current setting 1
IRB	current setting 2
SO	signal detect out
A, B, C	constant current sources

Ladder resistors connecting to 7 comparators provide reference voltages for each (+) input of comparators. The voltages are supplied from internal source and are in VU steps.
When the voltage on (–) pin of a comparator exceeds (+) input, the comparator turns the constant current source on, enabling the LED to be driven.

EFFECT BOARD ET4114-060 (7411406010)(pcb 2291050402)







PRIMARY FUSE BOARD

PS4114-141 (7411414100) 100V

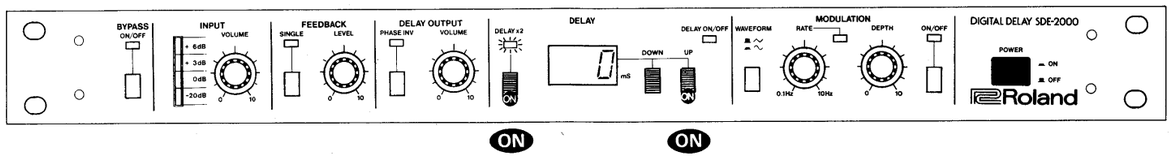
PS4114-143 (7411414300) 117V

PS4114-144 (7411414400) 220/240V

(pcb 2291050800)

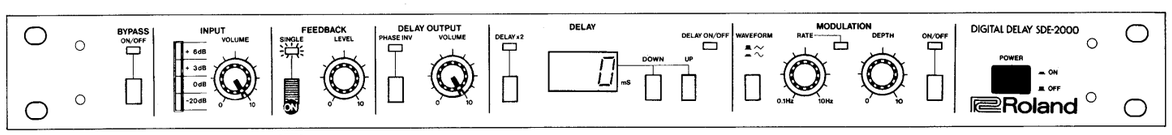
ADJUSTMENT

SAMPLING CLOCK FREQUENCY

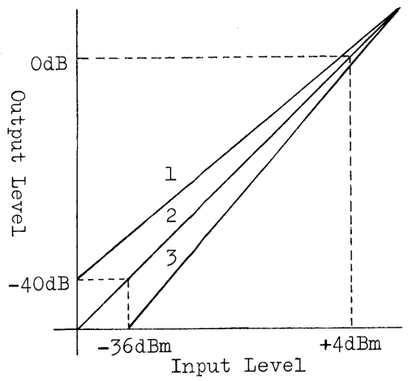


1. Turn power on 2-3 minutes before starting adjustments, for warmup.
2. DELAY on. DELAY x 2 on. While holding DELAY UP, push DOWN until the longest time is displayed.
3. Using non-magnetic (prefarable) tool, adjust L1 on CPU board for 668±3 (ms) display.
4. Push DELAY x 2 (off) for the next adjustment.

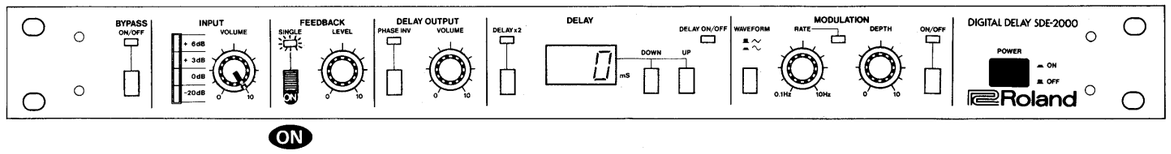
COMPRESSOR LEVEL LINEARITY



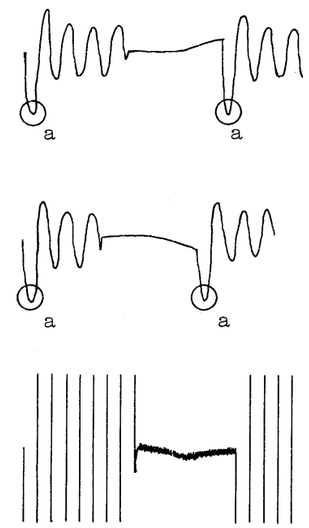
1. Connect audio generator (AG) to INPUT jack and voltmeter (VTM) to DELAY OUTPUT jack.
2. Place UNIGAIN at +4dBm.
3. Set AG for +4±0.2dBm, 1kHz, sine wave. Note the reading on VTM.
4. Reset AG for −36±0.2dBm.
5. Adjust VR2 on Effect board for a VTM reading 40+0/−0.3dB below the reading noted at step 3.
6. Repeat step 2. Reading may differ from that has been. Repeat steps 2 thru 5 until no further adjustment is necessary.



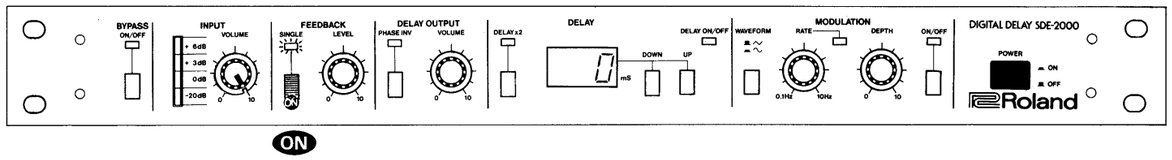
COMPRESSOR TOTAL HARMONIC DISTORTION



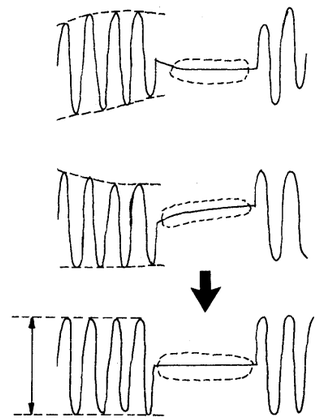
1. Place UNIGAIN at −20dBm.
2. Connect scope to TP-1 on Effect board. Set scope for AC couple, 2V/div, 1ms/div.
3. Connect AG to INPUT jack. Set for 1kHz, sine, burst tone (4 — 0 — 4 cycles); set the level for more or less clipping at peak a.
4. Reset scope V for 0.1V/div.
5. Adjust VR2 so that DC level is straight.
6. While rotating INPUT VOLUME 0 — 10 — 0 repeatedly, adjust VR1 for minimum level drift on DC line.



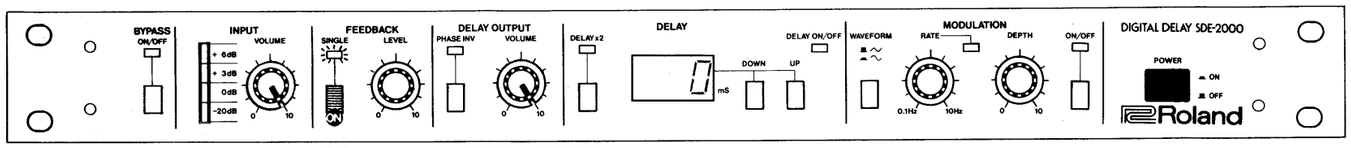
EXPANDER TOTAL HARMONIC DISTORTION



1. Place UNIGAIN at −20dBm.
2. AG setting: Follow preceeding paragraph.
3. Connect scope (DC couple, 1V/div. 1ms/div) to DELAY OUT jack.
4. Adjust VR3 for straight, drift-free DC line.
5. Reset scope for 2mV/div.
6. While rotating INPUT VOL 0 — 10 — 0 repeatedly, adjust VR3 so that DC line moves in parallel with horizontal graticule as VOL travels.



LPF FREQUENCY RESPONSE



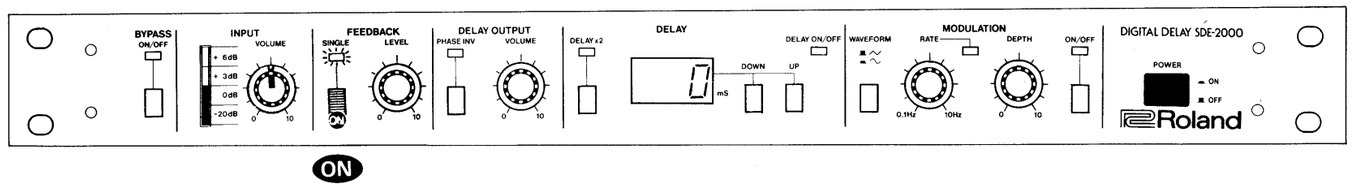
DELAY x 1

1. Place UNIGAIN at +4dBm.
2. AG to INPUT jack: set for −20±0.1dBm, 1.4kHz, sine.
3. VTM to DELAY OUT jack; note the reading.
4. Reset AG for −20±0.1dBm, 14kHz, sine.
5. Adjust VR4 so that VTM reading is 0 to 0.3dB less than that noted at step 3.

DELAY x 2

1. Push DELAY x 2.
2. Reset AG for 1kHz, keep its output to the above mentioned level.
3. Note VTM reading.
4. Reset AG for 5kHz, keep the level constant.
5. Adjust VR5 so that VTM reading is 0 to 0.3dB less than that of step 3.

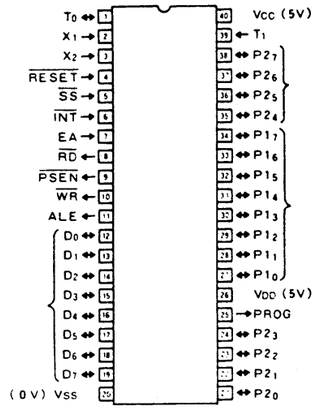
INPUT LEVEL INDICATOR

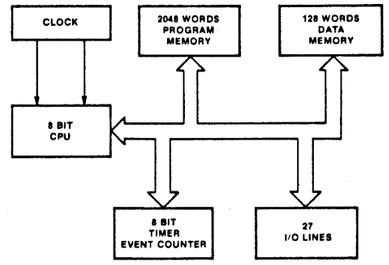


1. Place UNIGAIN at −20dBm.
2. AG to INPUT jack; set for −20dBm, 1kHz, sine.
3. Turn VR10 until INPUT 0dB segment lights up.

μPD-8049C

SINGLE-CHIP 8-BIT MICROCOMPUTER

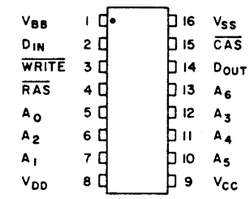




μPD416

16,384 X 1-BIT DYNAMIC RAM

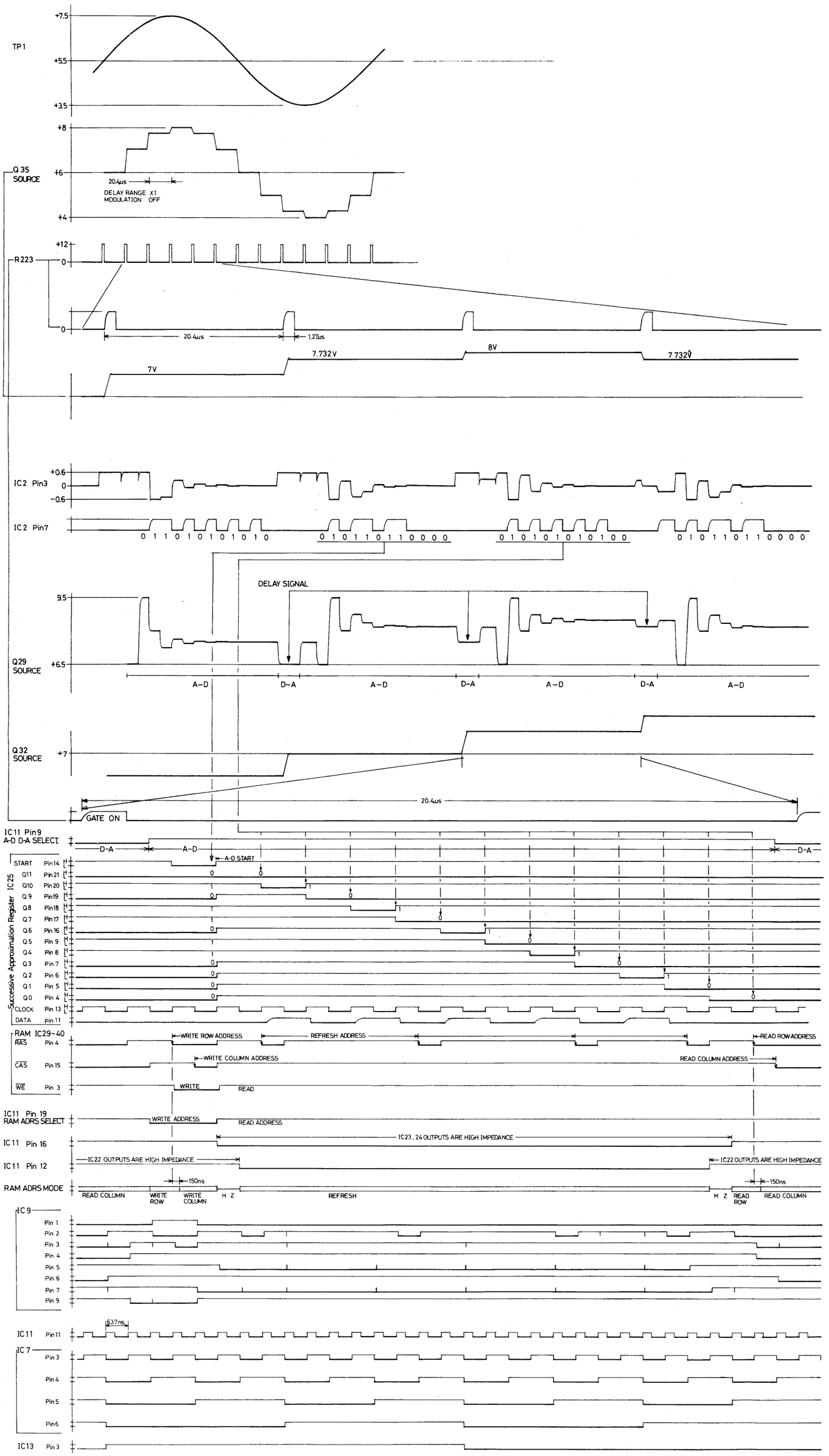
PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WRITE}$	READ/WRITE INPUT
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (−5V)
		V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

The RAS loads the row address and the CAS loads the column address. Both address signals share 7 input lines. Active cycles are initiated when RAS goes low, and standby mode is entered when RAS goes high. The three-sate output buffer turns on when the column access time has elapsed and turns off after CAS goes high. Input and output data are the same polarity.


TP1
+7.5
+5.5
+3.5
Q35 SOURCE
+8
+6
+4
20.4μs
DELAY RANGE X1
MODULATION OFF
R223
+12
0
20.4μs
1.27μs
7V
7.732V
8V
7.732V
IC2 Pin3
+0.6
0
-0.6
IC2 Pin7
0 1 1 0 1 0 1 0 1 0 1 0
0 1 0 1 1 0 1 1 0 0 0 0
0 1 0 1 0 1 0 1 0 1 0 0
0 1 0 1 1 0 1 1 0 0 0 0
DELAY SIGNAL
Q29 SOURCE
9.5
+6.5
A-D
D-A
A-D
D-A
A-D
D-A
A-D
Q32 SOURCE
+7
20.4μs
GATE ON
IC11 Pin9
A-D D-A SELECT
D-A
A-D
A-D START
D-A
Successive Approximation Register IC25
START Pin14
Q11 Pin21
Q10 Pin20
Q9 Pin19
Q8 Pin18
Q7 Pin17
Q6 Pin16
Q5 Pin9
Q4 Pin8
Q3 Pin7
Q2 Pin6
Q1 Pin5
Q0 Pin4
CLOCK Pin13
DATA Pin11
RAM IC29~40
RAS Pin4
CAS Pin15
WE Pin3
WRITE ROW ADDRESS
REFRESH ADDRESS
READ ROW ADDRESS
WRITE COLUMN ADDRESS
READ COLUMN ADDRESS
WRITE
READ
IC11 Pin19
RAM ADRS SELECT
WRITE ADDRESS
READ ADDRESS
IC11 Pin16
IC23, 24 OUTPUTS ARE HIGH IMPEDANCE
IC11 Pin12
IC22 OUTPUTS ARE HIGH IMPEDANCE
IC22 OUTPUTS ARE HIGH IMPEDANCE
RAM ADRS MODE
150ns
150ns
READ COLUMN
WRITE ROW
WRITE COLUMN
H Z
REFRESH
H Z
READ ROW
READ COLUMN
IC9
Pin 1
Pin 2
Pin 3
Pin 4
Pin 5
Pin 6
Pin 7
Pin 9
637ns
IC11 Pin11
IC7
Pin 3
Pin 4
Pin 5
Pin 6
IC13 Pin 3