Manual No. TN610-0

MODEL 610
SIX-TRAK

PRELIMINARY SERVICE DATA

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GENERAL DESCRIPTION

The 610 is a "hybrid" synthesizer and sequencer containing a 4-MHz Z-80A microcomputer with 16 kbytes of EPROM, 6 kbytes of non-volatile RAM, MIDI interface, thirteen-bit DAC, control voltage (CV) demultiplexer, six-voice analog synthesizer, and automatic tuning circuitry.

The computer has three main functions. First, the memory stores "programs," which are sets of control data which "patch" an instrumental timbre or effect. Because of the completely independent voice control lines, each voice can have a distinct program. Second, the memory stores the multi-track sequences. Third, the computer participates in some of the synthesis. Most significantly, the three independent ADSR envelopes for each voice are calculated by the computer. The six independent LFOs are also synthesized by the computer. All modulation is mixed in software and integrated into the appropriate CV outputs to each voice.

(Schematic Sheet A)

POWER SUPPLY

When power is off, Vnv battery BT301 supplies 2.9V, which D108 drops to 2.2V. This is sufficient to hold the non-volatile memory (three 6116s).

Vnv also powers U113 in the power detect circuit, and U114 in the RAM protect circuit. U113-3 is high because both inputs are low (since power is off). This high is applied directly to U113-9, and to U113-8 through D112. U113-10 -RESET is therefore low (true). The CPU will remain reset until this line goes high (false). Inverting -RESET, U113-4 is high. In other words, -PWR ON is also false. This signal keeps all U114 gate outputs high, preventing the RAM contents from being altered.

When power is switched on, D109 and D110 rectify the peak to appear across divider R112/R113. When the divided voltage exceeds the CMOS high threshold of 3.5V, U113-13 goes low. Input U113-9 goes low immediately. Pin 8, however, is held high by the (Vnv) charge on C1243, which begins to discharge through R124. After about one second, pin 8 falls low enough so U113-10, -RESET can go high, enabling the CPU. -PWR ON goes low, enabling RAM access.

D104 and D105 rectify the transformer secondary to produce +Vunreg. C105 is the filter. Vunreg only operates the DAC reference buffer, U111 (a 5532 shown in two places on the left of sheet B). U103 through D102 overrides Vnv, providing standard operating voltage for the RAMs. D103 biases the common terminal of U103 0.6V above ground. This sets an output of +5.6V. But D102 drops this back to +5V. Under this condition, D108 prevents the regulator voltage from charging the (non-rechargable) lithium battery.

U158 is a low-current +15V supply for the DAC. U106 supplies +5V to the synthesizer. U107 provides -6.5V. R1199 and C1101 prevent the positive regulator from latching up when the negative supply charges first.

SYSTEM CLOCK

The system clock is generated by Y101 8-MHz crystal and two inverters wired as a simple RC oscillator. The three miscellaneous gates which buffer the clock also allow it to be switched off, and a factory test clock to be inserted. The 4-MHz output of divider U134 clocks the CPU. R142 is needed to convert TTL-to-NMOS levels.

In addition, two slower clocks are generated. The 2-MHz output drives WAIT gate U123-10, and two of three 8253 counter sections in U133. One of these sections, U133-17, divides further, to 200 Hz (5 ms.), for the interrupt clock (discussed below). The other section, U133-15 (on sheet B), is the Total Time counter which will be explained in conjunction with the tune circuitry.

Returning to divider U134, the 500 kHz output drives the UART, U137, which divides it internally to the MIDI clock rate of 31.25 kBaud. It also clocks U16-9 non-maskable interrupt (NMI) flip-flop (FF), as discussed below.

CPU/MEMORY

With power on and the clock running, when -RESET goes high, the CPU's program counter is initialized to memory address 0000H (Hex). To read this first instruction from U128 ROM, a signal is needed to differentiate the ROM from the RAMs and other devices connected to the data buss. When address line A14 is low, U142-8 will go low when -MREQ goes low. -MREQ is a signal from the CPU which indicates that the address bus holds a valid memory address. This enables the ROM to put the instruction on the data buss. (Although using the 2764 -CE input would reduce power consumption, -OE was used for maximum memory access speed.)

To select the RAMs, signals are generated by U125 Memory Address Decoder. With A14 high, if A12 is low, -RAM 0/1 will be low. With -PWR ON true, U114-6 is low. Therefore if A11 is low, U119 is enabled. If A11 is high, U151-10 is low, so U117 is selected. U112 is enabled when -RAM 2 is low. Returning to the decoder, -RFSH indicates that the address bus holds a valid refresh address. Applied to G1, this signal is used to disable the decoder whenever this is the case.

All EPROM operations are memory-read. The transfer of data from CPU to RAM is enabled by the -WR (write) line being true. The opposite direction, from RAM to CPU, is enabled by -RD (read).

The uppermost memory-mapped device is U137 UART, which has two control registers that need to be accessed. These are decoded somewhat differently from the other memory locations. The combination of A0, A13, A14, A15 define the read and write addresses. -MREQ enables the device. Gate U140-11 clocks the Enable input either with WR or RD. The RC-delay provided to -RD through U141-4 is needed to interface this 6800-system part to the Z-80A.

I/O

I/O (input/output) interface follows similar principles as memory interface. The address lines define ports which are validated by -IORQ (instead of -MREQ). -IORQ (CPU pin 20) connects to U124 output decoder which is similar to the memory decoder. With regard to I/O, -WR defines an output to a latch which may drive the DAC, or determine the distribution of the resulting CV, or activate the tune system. -RD true defines an input operation, typically from data bus drivers which hold data from the control panel, or the tune system. Only if -RD and -IORQ are both low, U123-1 is high, enabling U129-3 to follow the state of A3. With A3 high, input strobes -CS19 and -CS1A are produced when A0 and A1 are high, repectively. R176 is needed to interface LS to CMOS levels.

Timer U133 is selected with A3 low, while its internal registers are selected by A0/A1. When -WR and -IORQ are low, U142-11 clocks the -WR input. When U123-1 is high, U123-4 clocks the -RD input. The timer is I/O mapped because it is too slow to run memory-mapped in this system. (I/O inserts an automatic WAIT state.) An additional WAIT state is also inserted by U123-13 (to CPU pin 24) when both -IORQ and the 2-MHz clock are low. This corrects the phase of the of the 8253 accesses relative to the 2-MHz clock, to meet the 'write access-to-clock" setup time requirement of the 8253.

Before detailing the I/O driver and latch functions, it is appropriate to conclude the microcomputer discussion with the interrupt system.

INTERRUPT SYSTEM

To accomplish its real-time tasks such as playing sequences, updating Sample/Holds, calculating the envelopes, LFOs, and current Glide values, the Six-Trak microcomputer is interrupt-driven at a constant rate. The Z-80 has two interrupt inputs: -INT, and -NMI (Non-Maskable Interrupt). The first is constantly clocked, the second is used only for MIDI.

U113-17, the 8253 section which forms the Interrupt Clock, was briefly mentioned above. This third of the device is programmed to divide, producing the 7-ms -INT signal through U141-6. Normally each 7-ms pulse forces the CPU to calculate all CVs and update the DAC outputs to the voices. This gives the envelopes a basic resolution of 7 ms. Because this interrupt is "maskable," there are some rare occasions during which -INT is ignored. In the "background period" between the end of the interrupt routine and the next interrupt, the CPU refreshes the LEDs, reads the ADC, and reads the control panel. Interrupt processing takes about 4½ ms. This leaves a 2½-ms "background" period for other, non-critical tasks.

MIDI

U137 UART in concert with U146-9 NMI Flip-Flop (FF) allows the external system to control the Six-Trak with MIDI data. The interface operates at 31.25 kBaud, which is obtained by internally dividing the 500 kHz TxC and RxC inputs (U137-3 and -4) by 16. When the UART is idle and waiting for (Rx) data, its pin 7, -IREQ, is pulled high by R166. Each 500-kHz pulse to U146-11 clocks this high through to the CPU U132-17 (-NMI), where it has no effect. But when a complete serial byte has been received,

-IREQ goes low, indicating that the UART receive register is holding data. This data needs to be retrieved immediately so that the next byte can be received. -IREQ will take at most 2 us (1/500 kHz) to be clocked through to the CPU -NMI input. When the CPU sees this negative edge, it completes its current instruction then branches to the routine which handles UART input.

When finished with the interrupt routine, the CPU resets the NMI Flip-Flop by toggling the -NMI CLR bit from U148-7 Control Latch. (Whenever the CPU is unable to process the UART, for example, for short periods (less than 42 usec) when tuning, it inhibits the NMI FF with this bit.) Then the processor internally loads the input byte into a software FIFO and returns to background or interrupt processing. At some later time in the background routine, the FIFO is unloaded and the data processed. (It is during the unloading and processing that normal real-time clock interrupts are disabled.)

U137 MIDI UART allows two microcomputers to communicate sequence and program information. As the keyboard or sequencer is played this data is converted to the MIDI protocol and sent to the UART one byte at a time, for transmission to any receiver which may be connected. The MIDI standard hardware is a 5-mA current loop, designed especially to prevent the formation of audio ground loops which can develop in complex systems.

The UART converts parallel bytes written to its memory-mapped transmit register into serially-formatted bytes consisting of a start bit, 8 data bits (D0 to D7), and a stop bit. Transmitter data out is buffered by U129-6, which can sink up to 16 mA. If transmit data is low, current flows from +5V through R194, over pin 4 of both connectors, through R148 and optoisolator LED U143, and returns over connector pins 5. D113 protects the receiver from reverse-polarity spikes. The output of the optoisolator is normally pulled high by R147. But with the LED on, the isolater switch turns on, sending a low to the UART receiver input. Notice that while the MIDI OUT jack is grounded to the chassis, MIDI IN is not. This allows the cables to provide their shielding services without creating ground loops.

(Sheet B)
DAC AND CV DEMULTIPLEXER

We now turn to the circuitry which produces control voltages (CVs) for the synth voices. U105 and U104, two 6-bit latches, drive U110 DAC, but most CVs only receive six-bit resolution provided by the more-significant latch, U104. When -CS09 goes low, U105 latches data off of the buss. When -CS0A goes low, U104 is selected instead. The two 2K resistors are for LS to CMOS interface. The DAC has an 8-V total range, from -4V to +4V. For increased tuning accuracy, the multiplexer acts as a thirteenth, most-significant DAC "sign" bit, by selecting either the 0 to -4V, or 0 to +4V polarities.

R128 and R129 form a 4-V divider, stabilized by C128, C117, and buffered by U111-7 to provide a +4-V reference to the DAC. U156 Inverting DAC Buffer converts the DAC current output to a 0 to -4V range (all zeroes = 0V, all ones = -4V). This range is sampled by the X0 input of the U108 multiplexer. When X0 is selected, Vdac output at U108-3 ranges from 0 to -4V.

U111-1 is an inverting 1:1 amp which reverses the polarity of Vdac to 0 - +4V. Vdac from U111-1 goes to the ADC comparator through R120 and to the X1 input of U108 Multiplexer. When X1 is selected, the Vdac output of U108-3 ranges 0 - +4V.

During each interrupt cycle (-INT, not -NMI), Vdac assumes the 48 different CV destination values for the voices. U118/U120 Sample/Hold (S/H) Address and Strobe latches synchronize the 4051s so Vdac strobes the correct S/H at the precise time that it assumes the corresponding value.

For example, to select a specific Vdac destination, U124-7 (on sheet A), -CSOF, goes low, causing U118 (on sheet B) to latch three address bits. These select one of eight outputs of each 4051 (except U108) with the ABC address inputs. Then -CSOE goes low, and U120 latches one of VOICE 1-6 lines low to enable a single demultiplexer. By this combination, Vdac will charge the sample/hold (S/H) capacitor to which it is connected, with the present DAC voltage.

Each S/H consists of a .01 uF low-leakage capacitor in concert with the very high impedance of the 3394 inputs. Since there is no discharge path, the capacitor retains whatever Vdac charge with which it is briefly strobed, until the next strobe. A 1M resistor and .001 capacitor are used on the filter and VCA lines to help filter out "digitization" noise which appears on the envelopes.

Since each CV line to the voices is separate and individual (rather than parallel) the voices can produce inependent sounds. This capacity is in contrast to our Prophet synthesizers in which most voice controls are paralleled.

To obtain a better understanding of the DAC, it will be useful to actually observe Vdac on an oscilloscope while exercising various control options (through serial data input). For example, the dynamics of the filter, amplifier, and modulation envelopes as well as the modulating LFO can be easily observed.

DAC TRIM

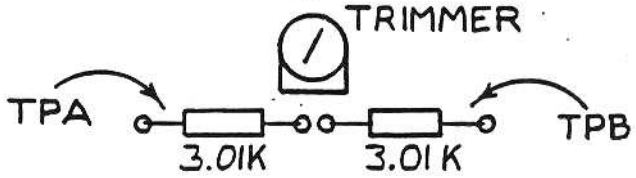
1. Warm-up 610 (with cover closed) for at least five minutes.

2. Hold CONTROL RECORD and press SELECT #7. This sets the DAC output to 0V to allow you to measure the DAC offset. (This also locks-up the computer so that to reset will require switching power off/on.

3. Set DVM to read mV (.000).

4. Measure voltage at TPA. An offset of greater than +/- 0.9 mV is out of spec.

Figure



5. If the offset is positive, add the offset value to 1 mV.
   If the offset is negative, subtract the offset value from 1 mV.

6. Connect DVM to TPB and trim R1205 to the value figured in step 5, +/- 0.1 mV.

7. Seal the trimmer.

ADC

U108 is the ADC multiplexer, which connects the selected input from the wheels, or control knobs to its output, according to the address provided by three bits of U118. If any wheels or knobs are selected, D128 and D129 pull-up the comparator, enabling the output. The voltage on the wiper of the selected wheel or knob is compared to the positive Vdac by successive approximation. The comparator state is monitored by U154 Input Driver (which also polls the footswitch.)

SYNTHESIZER

The CEM3394s are highly-integrated voltage-controlled voices which contain:

- a multi-waveshape oscillator (SHAPE) with variable frequency (OSC) and pulse width (PW),
- a mixer (MIX) to balance the oscillator against an external input,
- a four-pole low-pass filter with adjustable frequency (FIL), and resonance (RES),
- a VCA which applies the oscillator ouput to the filter frequency input CV (FIL MOD),
- and a final VCA (VCA) which shapes the voice dynamics.

CAPS A through D determine the frequencies of each filter pole. The VCO CAP sets the basic oscillator range. The VCA CAP actually ac-couples the filter output to the VCA input. The REF pin sets basic oscillator range.

The external audio input of all voices is driven by Q102 noise source and amplifier Q101. C1222 ac-couples the noise to the 3394s. In Rev A, serial numbers 1 - 900, a 5837 digital noise source is used.

The voice outputs are summed by U145-7, which drives U144 Tune Comparator (see below) and U147 FET switch. The 4049 is connected in an unconventional way to achieve noiseless audio switching. D114/115 protect the switch by clamping the audio level to 0.3 Vpp. The switch is operated by one bit from U148-15. The normal and inverted control pulses, and some slewing capacitors and resistors. To enable audio, section D is turned off at the same time as section C is turned on, allowing current to pass through the switch from R162 to the summing junction of buffer amplifier U145-2.

The feedback path from U145-1 through R164 through switch section D assists in shutoff action. D116 and D117 clamp this level. To disable audio, section C is turned off, inhibiting audio current from R162 at the same time as section D is turned on, drastically reducing the gain of U145 to further squelch any audio signal which may leak through the switch.

TUNE

The Tune system is responsible for the entire performance of the Six-Trak in the sense that without its corrective influence, the six oscillators could not by themselves be expected to constantly stay in tune, due to temperature drift and component aging. Tuning is automatic. Basically, after the 610 detects about 30 seconds of inactivity, it precisely-measures oscillator frequencies over the seven-octave range of one oscillator, and learns the exact CVs required to produce perfectly-tuned octaves. After another 30 seconds, it tunes the next oscillator.

The oscillators are "scaled" to produce an octave change of pitch in response to a CV change of 3/4V. The differences between the theoretical and actual CVs which produce specific intervals are called tuning "biases." When playing, these biases are independently recalculated for each note and each oscillator, so that all six oscillators remain in tune throughout their range. In other words the computer measures the oscillator error at octaves, then during playback averages the error and corrects the note to which that oscillator happens to be assigned.

Frequency is measured in terms of ½-us events. There is a reference number of events (stored in EPROM) which will be produced by counting for one cycle at a specific octave, or for two cycles at an octave above that, or for four cycles at two octaves up, and so on. At each octave, the oscillator CV is adjusted by successive approximation until the total time count equals the reference count. When it does, the oscillator is in tune. It will take slightly more or less than exactly 3/4-volt to tune exactly 1 octave higher. This small but significant voltage difference is the bias which is averaged over the individual semitones.

To tune, the audio output is switched off and the computer selects one voice to drive U144 Tune Comparator. R167 pulls the output high until a positive audio cycle on the inverting input toggles the output low. C1230 discourages oscillations.

The squared-up oscillator or filter pulses drive the period-counting hardware consisting of U148 Tune Control latch, U150 Status Driver, U146 Flip-Flop, and two of three counters in U133.

For example, to tune Oscillator 1 to 261 Hz (middle C), the CPU first programs the Cycle Counter to count one cycle. The MSB of the DAC is set and this CV is applied to OSC 1. OSC 1 begins to generate a pitch in the upper middle of its range.

U148-2 latches out the gate (G) signal which enables the Cycle Counter. Then U148-10 outputs the -FFP pulse which by presetting Q, forces -Q, low. This we call a "fake" clock pulse which is actually required for the Cycle Counter to begin its count accurately (the clock loads a preset value into the 8253 count register in preparation for counting). The FF status is monitored by U150-12.

The FF is then cleared by the -FF CL bit from U148-12, in preparation for the oscillator or filter pulse. In Revs B and C -Q therefore places a high on the D input which gates the flip-flop to toggle -Q as clocked by the comparator. (Rev A uses a a bit from the computer via U148-5.) When the Cycle Counter receives the first low edge (after the fake clock), its output U133-10 goes low. This is also monitored by U150. When the CPU sees this low, it resets the FF in preparation for the next edge. U151-8 inverts this signal, enabling the Total Time counter at U133-14. The counter begins to increment at the 2 MHz rate.

Since the Cycle Counter has been programmed for a terminal count of one, when it receives the next low edge, its output (pin 10) goes high, stopping the Total Time counter. The Total Time register now holds the number of 2-MHz pulses equivalent to one oscillator cycle. The CPU sees that this specific total time count is way above the reference. This is because setting the MSB happens to drive the oscillator about an octave above C-261. So the computer turns off the MSB, sets the next significant digit, and measures the resulting count. It continues in this manner, setting each bit which does not cause the oscillator to overshoot its reference count.

One cycle at 130 Hz equals about 15,288 2-microsecond periods. To be tuned at this octave (C3), the oscillator must generate this number. To tune the next higher octave (C4), the reference is halved to 7644 and CV again set by successive approximation so that one cycle produces that count. For the higher octaves, C5 - C7, the reference count remains the same, while the Cycle Counter is reprogrammed for 2, 4, ...32 cycles. C2 is tuned at 30,576 counts. For the lower octaves, C0 - C1, the biases are actually extrapolated from the curve suggested by the higher-frequency measurements, because counting these slow waves would take an inconvenient amount of time.

TUNE TEST

In the tune test, each voice oscillator is checked against A-440 and its error is displayed as a +/- value in the display. When the value is negative, PROGRAM, PARAMETER, and VALUE all light. Three display digits equals one DAC bit. All voices must read within two DAC bits (six digits) of each other for each key tested. Otherwise may indicate a bad voice.

1. If the 610 is Rev A (serial numbers 1 - 900), a small modification may be required (or may have already been performed:
    a. Cut trace at U146-2.
    b. Jumper U146-2 to U146-6.

2. Hold CONTROL RECORD and press SELECT 9. This enables the tune test.

3. Center the PITCH wheel.

4. Initialize the PITCH wheel by holding CONTROL RECORD and pressing SELECT 3. (The switches respond normally even though the CONTROL LEDs blink.)

5. Select the basic patch (CONTROL RECORD + SELECT 8).

6. Manually tune (CONTROL RECORD + SELECT 6). Like most analog oscillators, the 3394s drift until they are thoroughly warm. Therefore retuning is usually necessary during the procedure. When, during the procedure below, a voice is found to be out of the six-digit range, manually retune and check the voice again. If the voice then tunes fine, accept it but keep your eye on it for unreasonable drifting.

7. While holding C2 (middle C), watch the display, and adjust MASTER TUNE for the closest indication to 00. (The knob will operate in units of three.) After adjusting, do not readjust until the test is finished.

8. While in the tune test, pressing the same note advances the voice assignment so you can test all six voices one after the other by just pressing the key. (Pressing two keys at once will produce a meaningless display.)

9. Check that all voices are within six digits of each other (at C2).

10. Check all voices at each of the white keys in this octave and at C3 and C4 (highest key).

11. Select PARAMETER 00 COARSE FREQUENCY, and adjust its value to maximum (48).

12. Check each voice at each C.

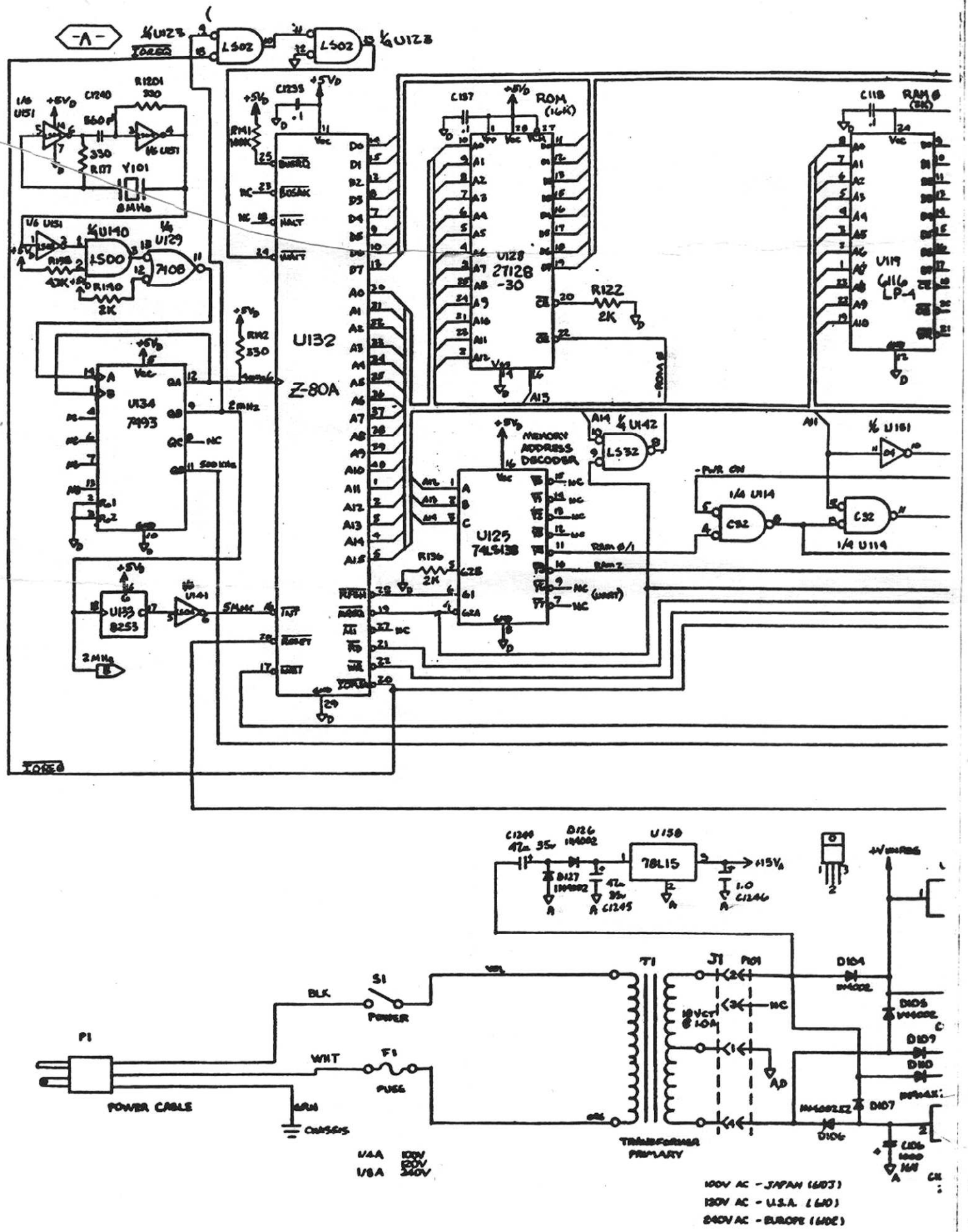
13. Check each note in the top octave.

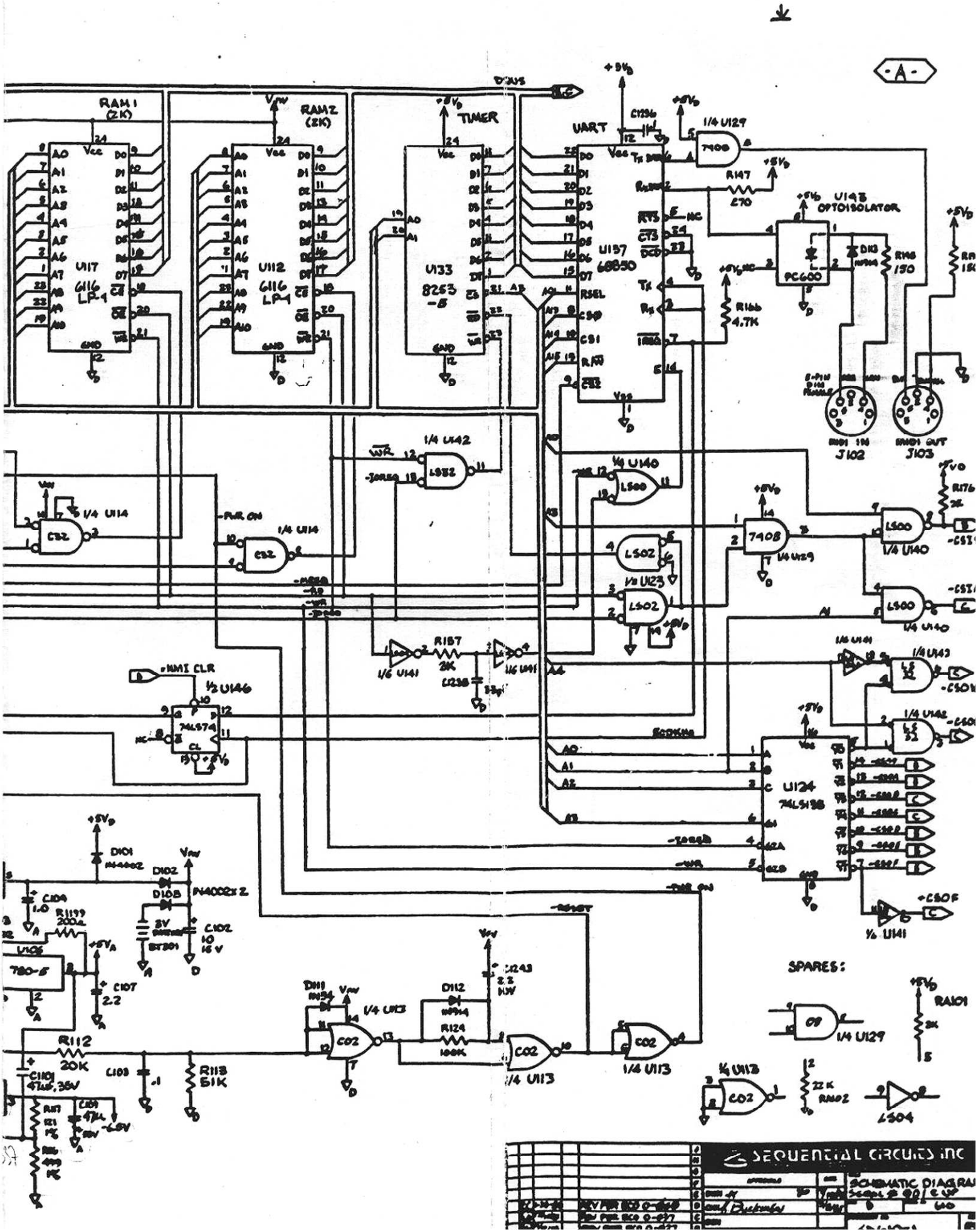
14. If the display read +/- 99, the voice tuning is too far out of range for the computer to measure.

15. To exit test, CONTROL RECORD + SELECT 9, or reset.

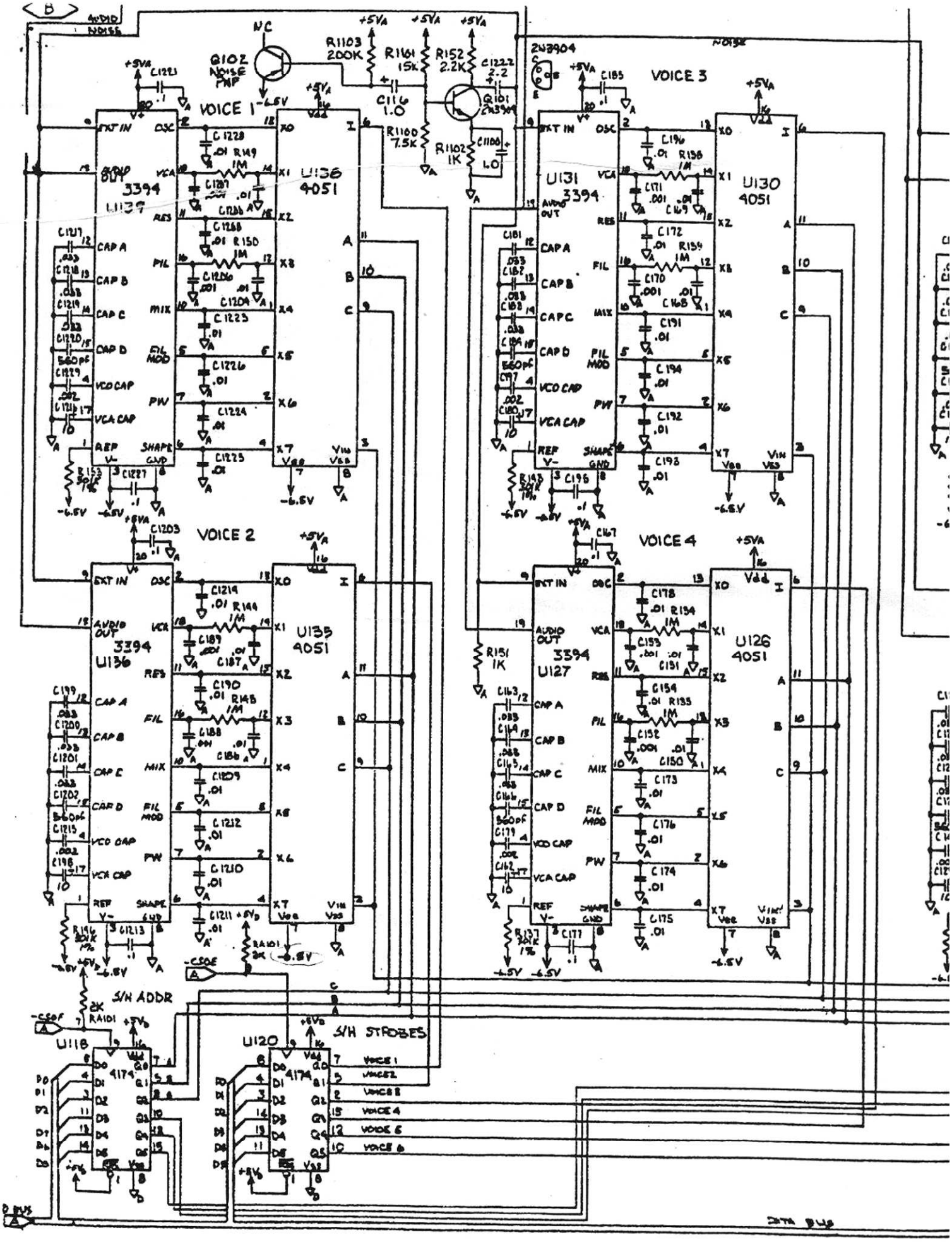
SHEET C

The control panel offers no surprises, except that the LEDs are not matrixed but operated by latches and decoders, to unburden the CPU of LED scanning responsibilities.

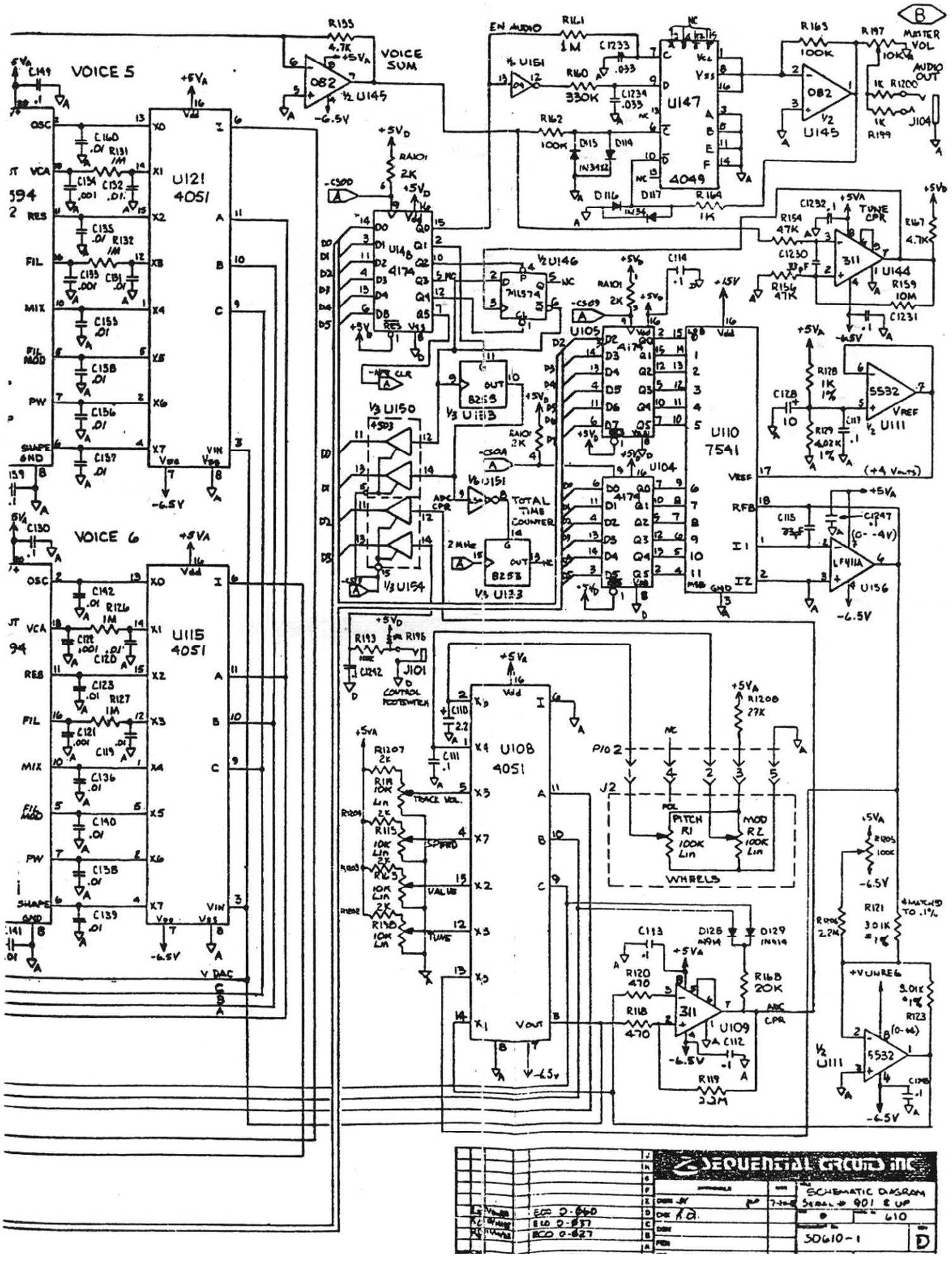

-A-
U132
Z-80A
U128
27128
-30
U119
6116
LP-4
U134
7493
U133
8253
U125
74LS138
MEMORY ADDRESS DECODER
U158
78L15
+15V
P1
POWER CABLE
BLK
WHT
S1
POWER
F1
FUSE
CHASSIS
T1
TRANSFORMER PRIMARY
J1
P101
D104
D105
D106
D107
D109
D110
1/4A 100V
1/8A 120V
240V
100V AC - JAPAN (6103)
120V AC - U.S.A. (610)
240V AC - EUROPE (6102)

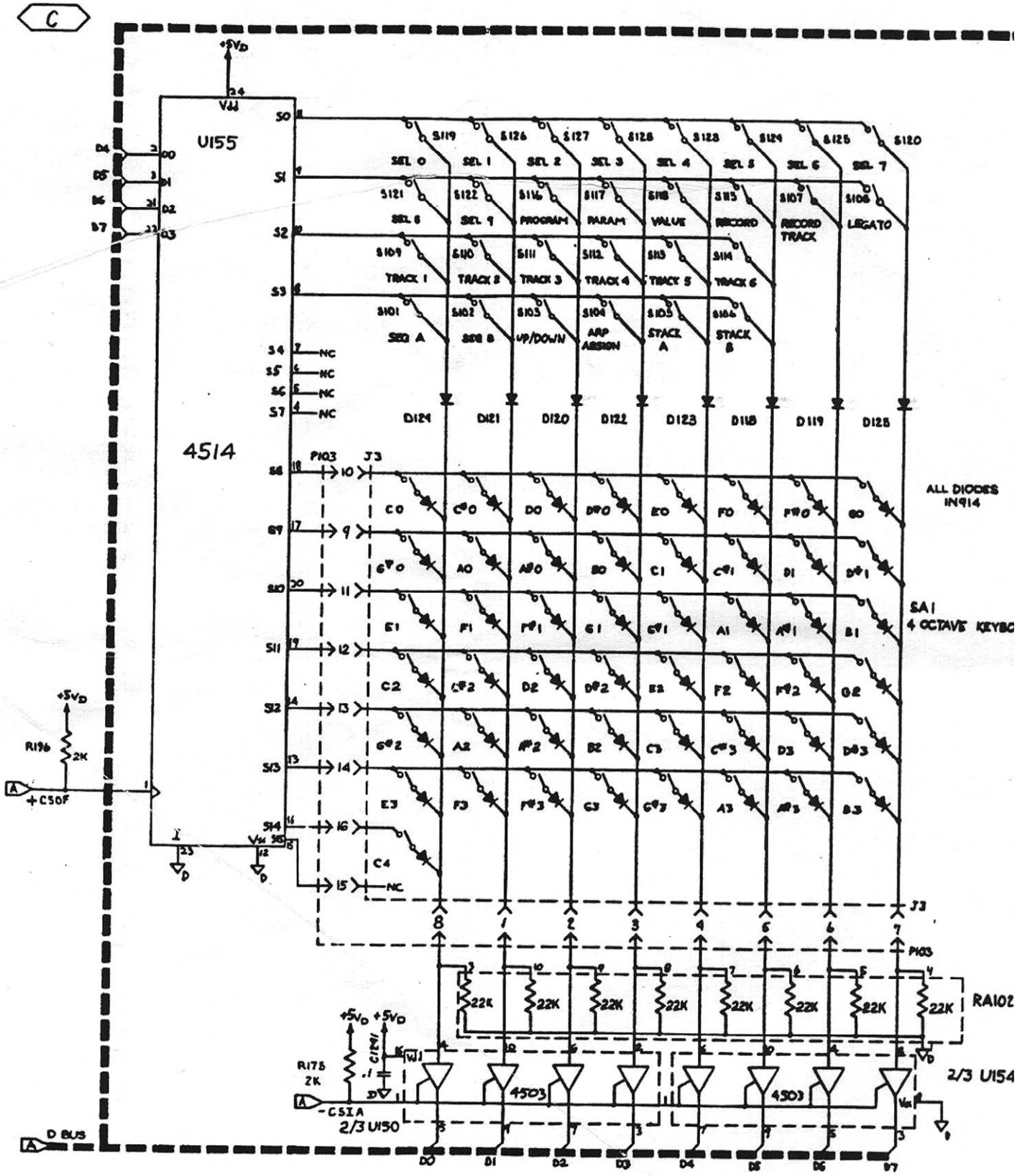


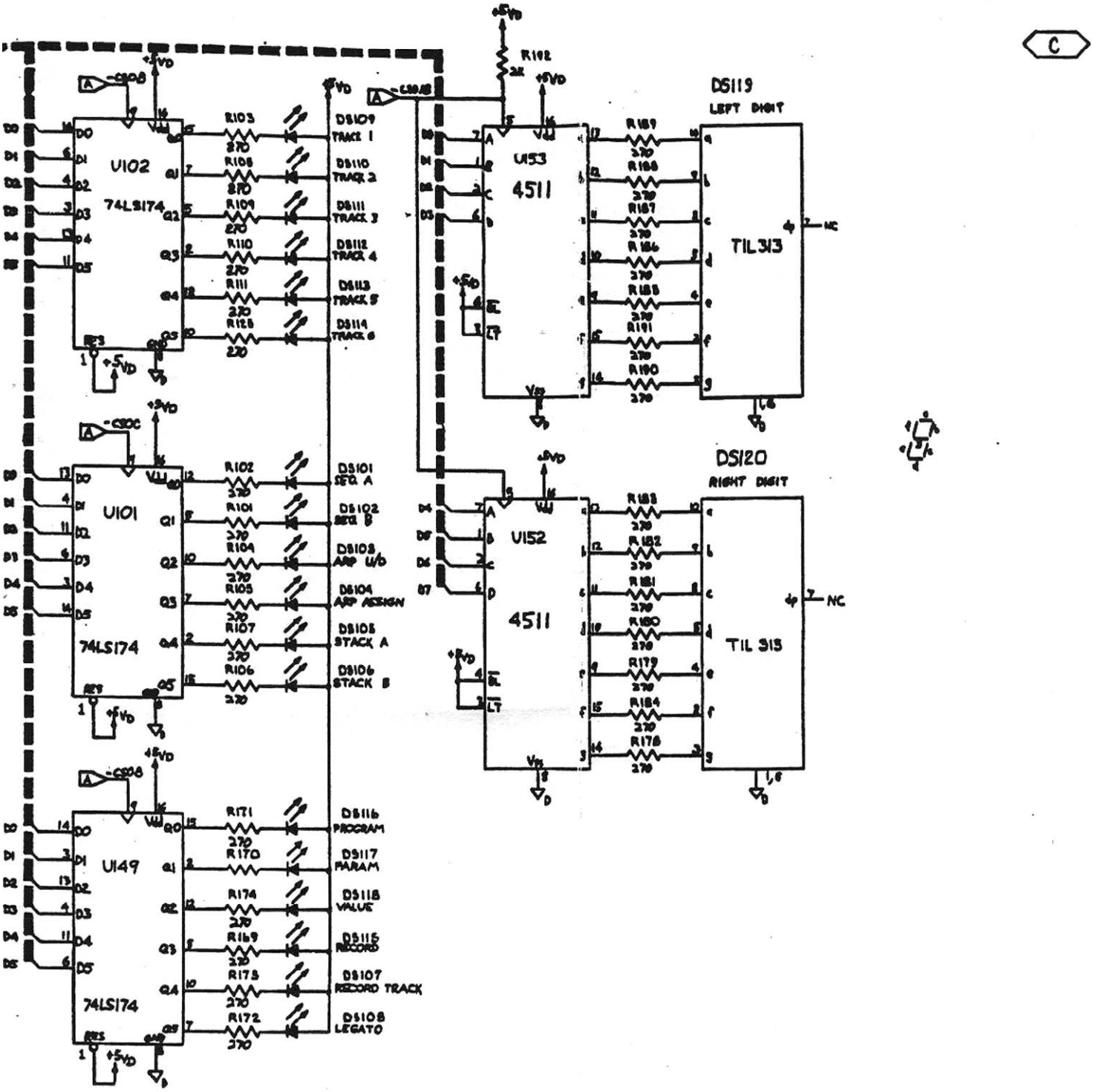
-A-
RAM1 (2K)
RAM2 (2K)
TIMER
UART
U117 6116 LP-1
U112 6116 LP-1
U133 8253 -5
U137 68850
U143 OPTOISOLATOR
PC600
J102
J103
1/4 U129
7408
1/4 U142
LS32
1/4 U140
LS00
LS02
1/4 U123
1/4 U114
C32
R157 2K
1/6 U141
1/2 U146
74LS74
U124 74LS138
D101 1N4002
D102
D103 1N4002x2
C104 1.0
R1199 200Ω
U106 780-5
C107 2.2
C102 10 16V
BT301 3V
R112 20K
C101 47µF, 35V
C103 .1
R113 51K
D111 1N54
1/4 U113
C02
D112 1N914
R124 100K
C1243 2.2 10V
1/4 U113
SPARES:
1/4 U129
RA101 2K
1/4 U113
RA102 22K
LS04
SEQUENTIAL CIRCUITS INC
SCHEMATIC DIAGRAM



VOICE 1
VOICE 2
VOICE 3
VOICE 4
Q102 NOISE PNP
Q101 2N3904
2N3904
U139 3394
U136 4051
U135 4051
U131 3394
U130 4051
U127 3394
U126 4051
U118 4174
U120 4174
S/H ADDR
S/H STROBES
AUDIO NOISE
NOISE
DATA BUS


VOICE 5
VOICE 6
VOICE SUM
TOTAL TIME COUNTER
TUNE CPR
MASTER VOL
AUDIO OUT
CONTROL FOOTSWITCH
WHEELS
PITCH R1 100K Lin
MOD R2 100K Lin
TRACK VOL.
SPEED
VALUE
TUNE
V DAC
SEQUENTIAL CIRCUITS INC
SCHEMATIC DIAGRAM
610
30610-1
D


C
U155
4514
+5VD
Vdd
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
D0
D1
D2
D3
D4
D5
D6
D7
NC
S119
S126
S127
S128
S123
S124
S125
S120
SEL 0
SEL 1
SEL 2
SEL 3
SEL 4
SEL 5
SEL 6
SEL 7
S121
S122
S116
S117
S118
S115
S107
S108
SEL 8
SEL 9
PROGRAM
PARAM
VALUE
RECORD
RECORD TRACK
LEGATO
S109
S110
S111
S112
S113
S114
TRACK 1
TRACK 2
TRACK 3
TRACK 4
TRACK 5
TRACK 6
S101
S102
S103
S104
S105
S106
SEQ A
SEQ B
UP/DOWN
ARP ASSIGN
STACK A
STACK B
D124
D121
D120
D122
D123
D118
D119
D125
P103
J3
C0
C#0
D0
D#0
E0
F0
F#0
G0
G#0
A0
A#0
B0
C1
C#1
D1
D#1
E1
F1
F#1
G1
G#1
A1
A#1
B1
C2
C#2
D2
D#2
E2
F2
F#2
G2
G#2
A2
A#2
B2
C3
C#3
D3
D#3
E3
F3
F#3
G3
G#3
A3
A#3
B3
C4
ALL DIODES IN914
SA1
4 OCTAVE KEYBO
R196
2K
+CSOF
22K
RA102
R175
2K
C1241
.1
-CSIA
2/3 U150
4503
2/3 U154
D BUS



SEQUENTIAL CIRCUITS INC

SCHEMATIC DIAGRAM
SERIALS 901 & UP

"D" 610

SD610-1 D

SCALE — SHEET 3 OF 3

ECO 0-860
ECO 0-897
ECO 0-927
RELEASED