

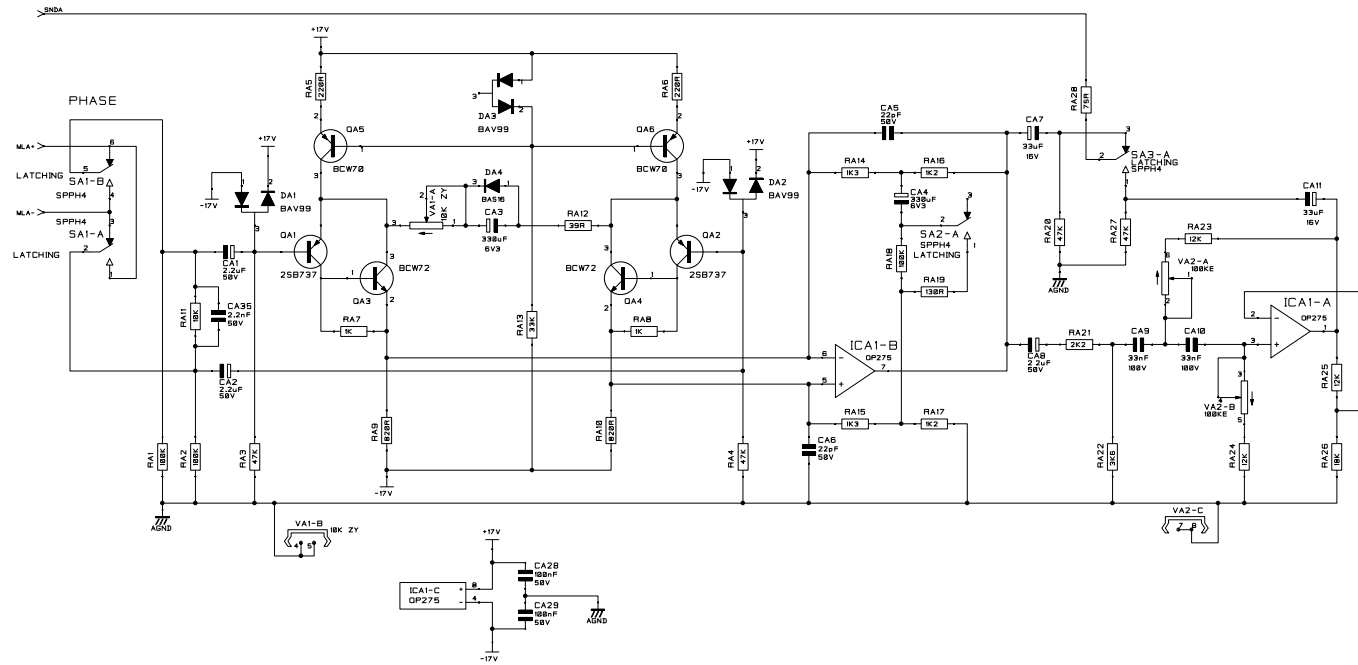
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 (2) CHANNELS C TO H (3 TO 8) ARE SAME AND TO BE REPEATED.  
 (3) TOTAL CHANNELS ARE A TO H (8) ON PCB

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TITLE SERIES TWO MIC AMP  
 DRG NO. ED4019



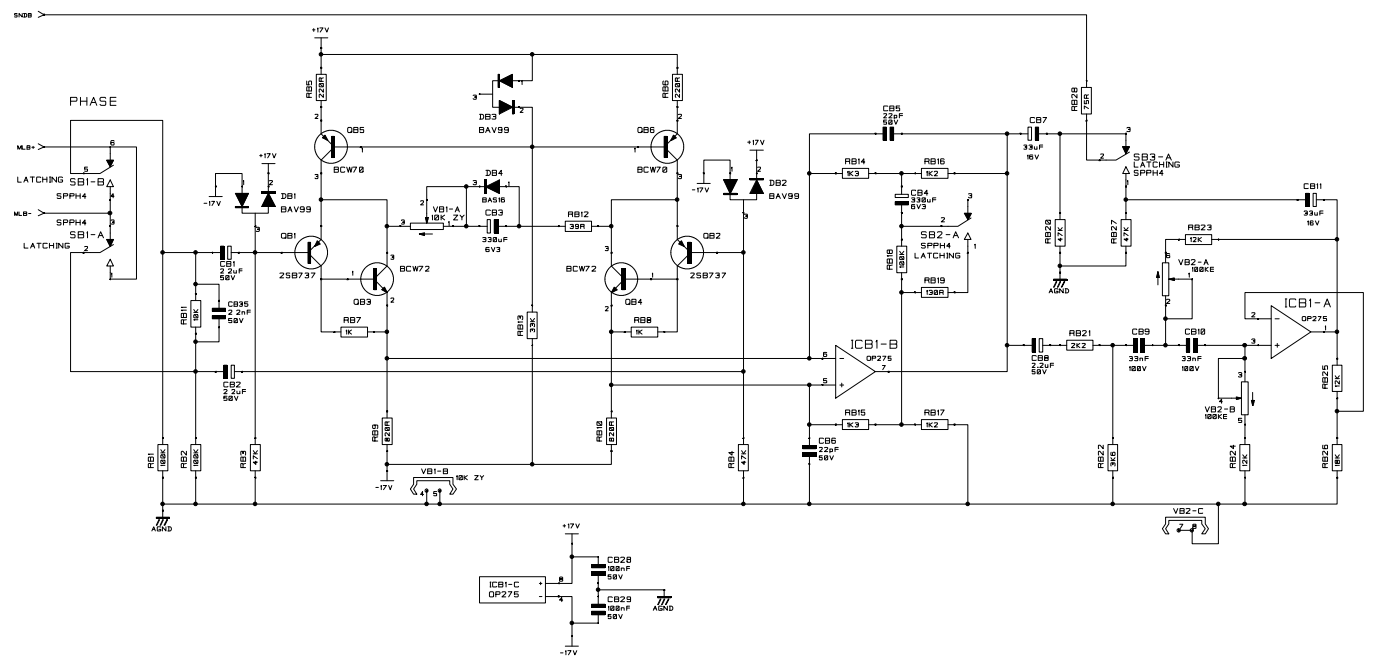
- NOTES
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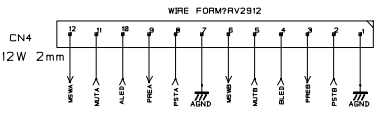
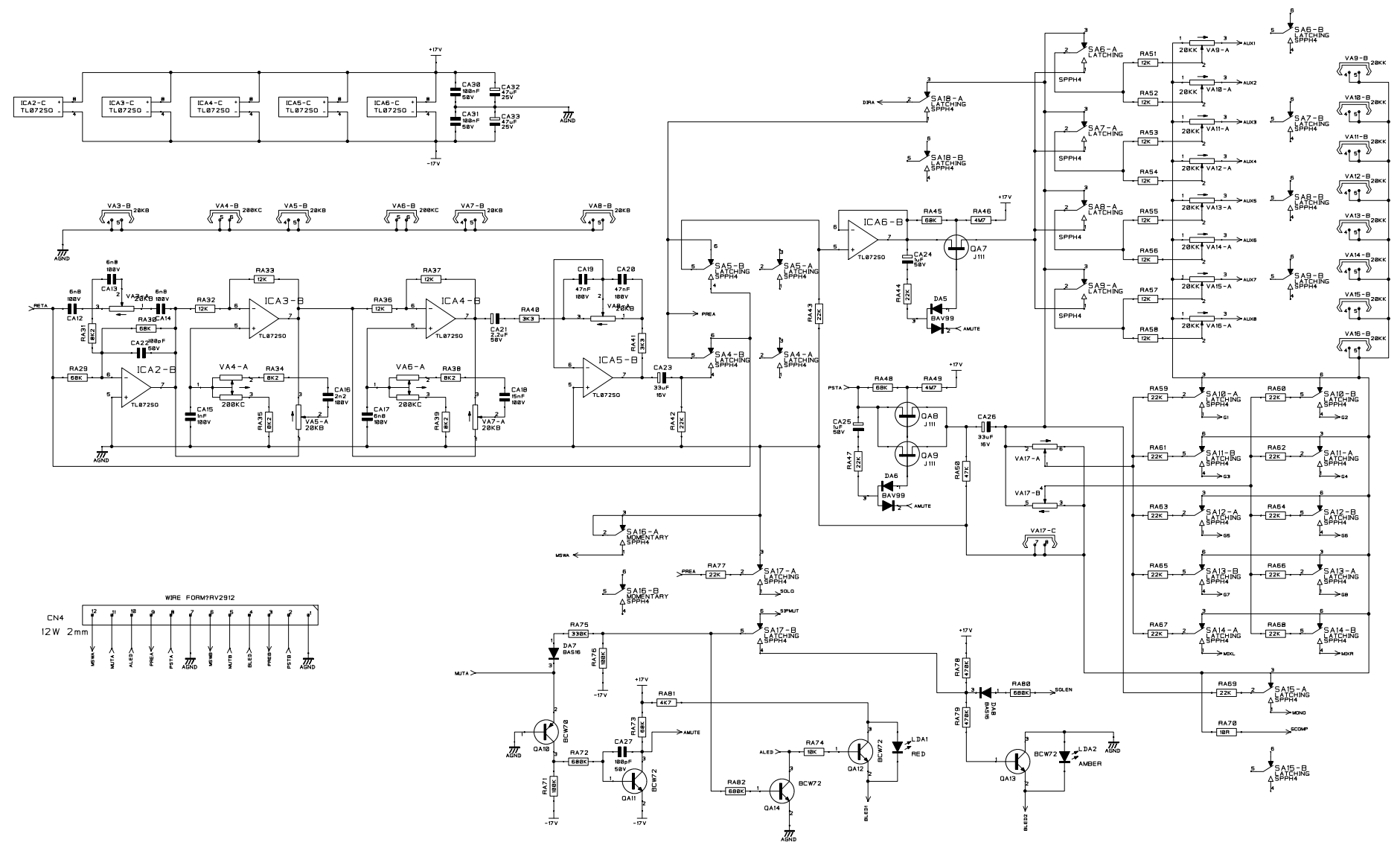
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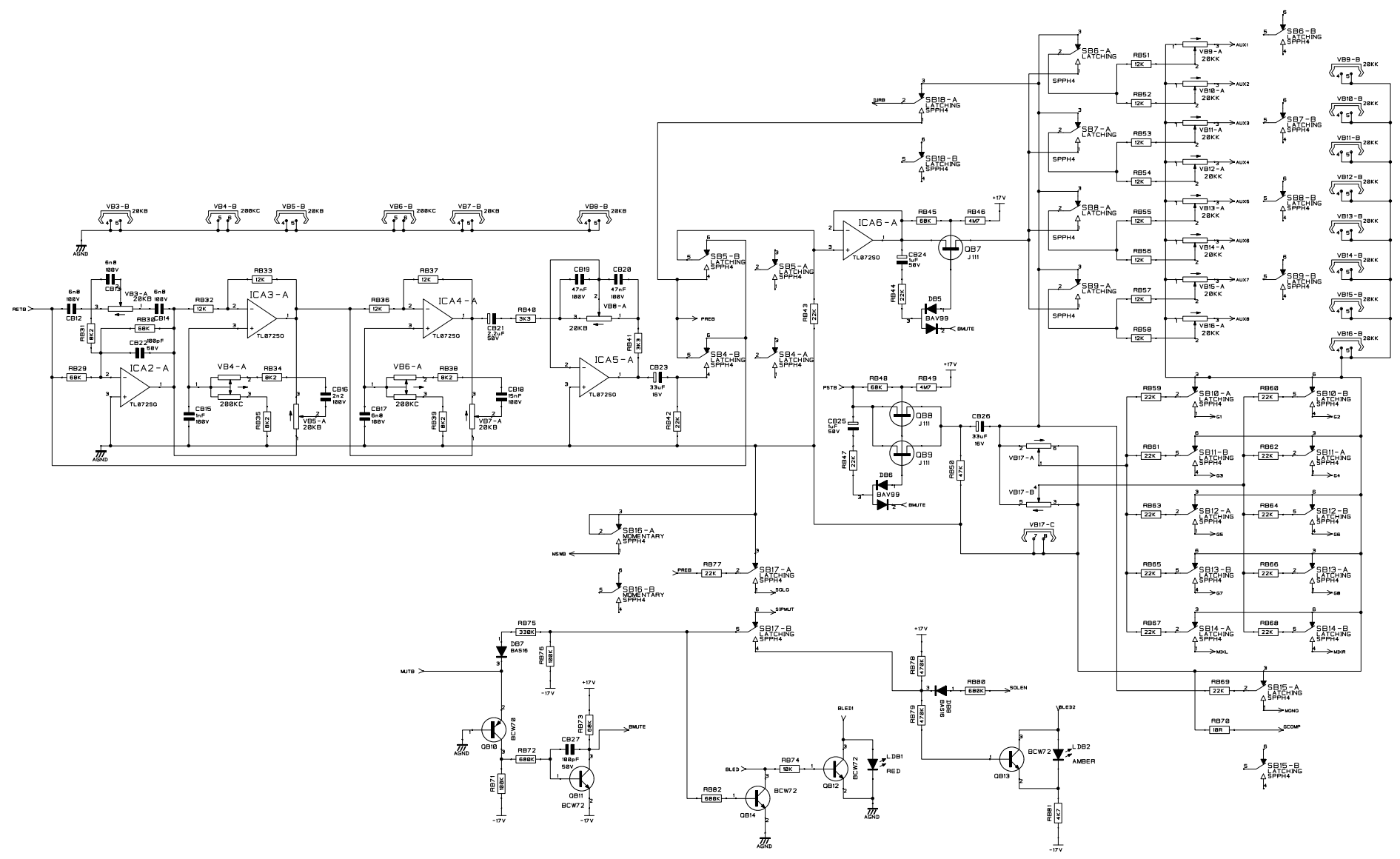
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- NOTES
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DATE			DRG NO.	ED4019

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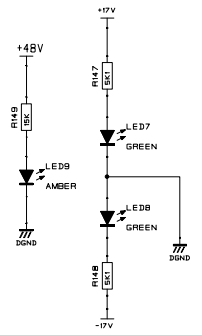
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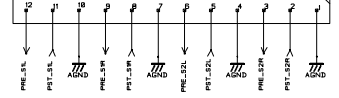
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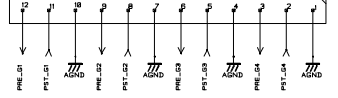
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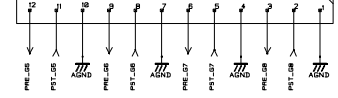
STEREO 1 & 2  
MALE  
DF3A-12P-2DSA



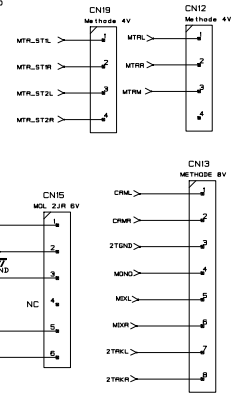
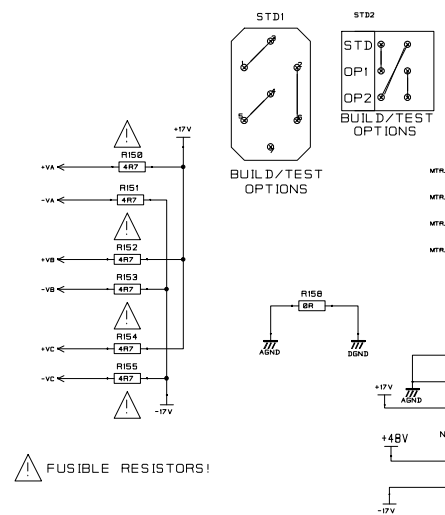
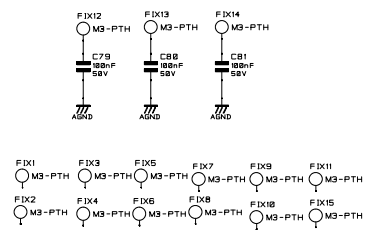
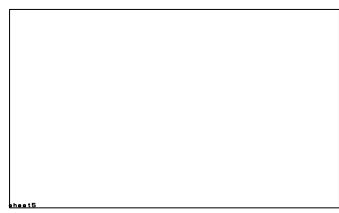
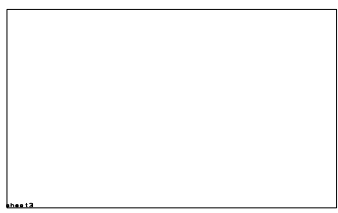
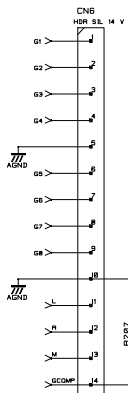
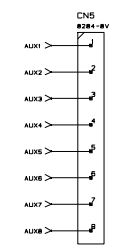
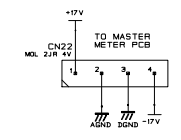
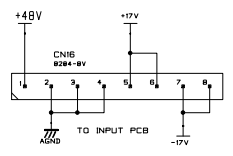
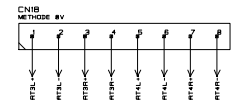
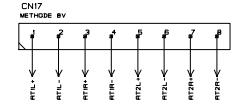
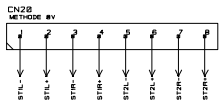
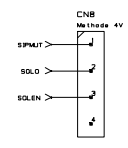
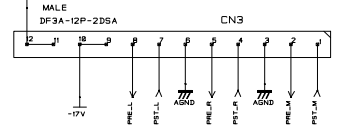
GROUPS 1-4  
MALE  
DF3A-12P-2DSA



GROUPS 5-8  
MALE  
DF3A-12P-2DSA



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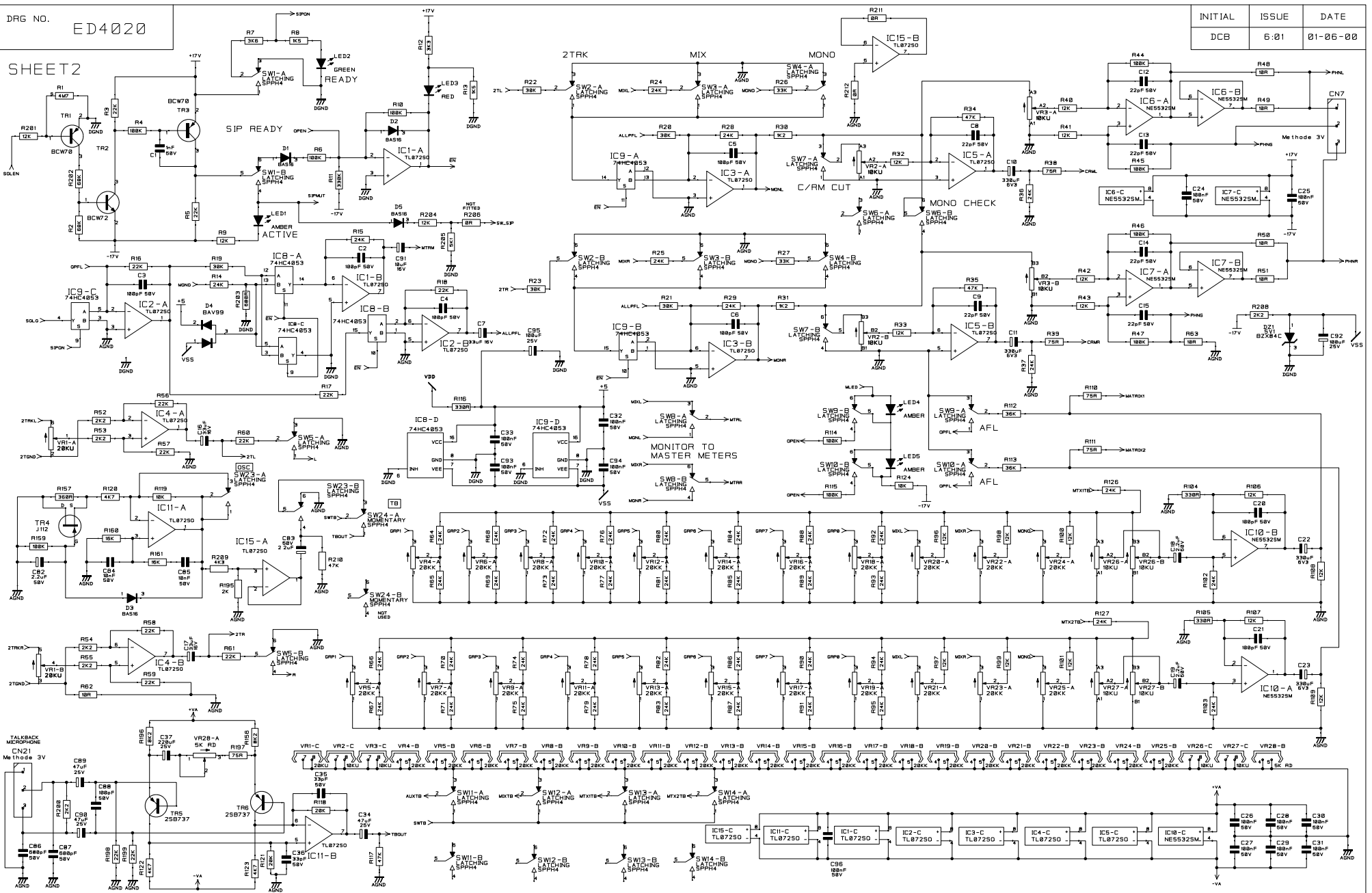
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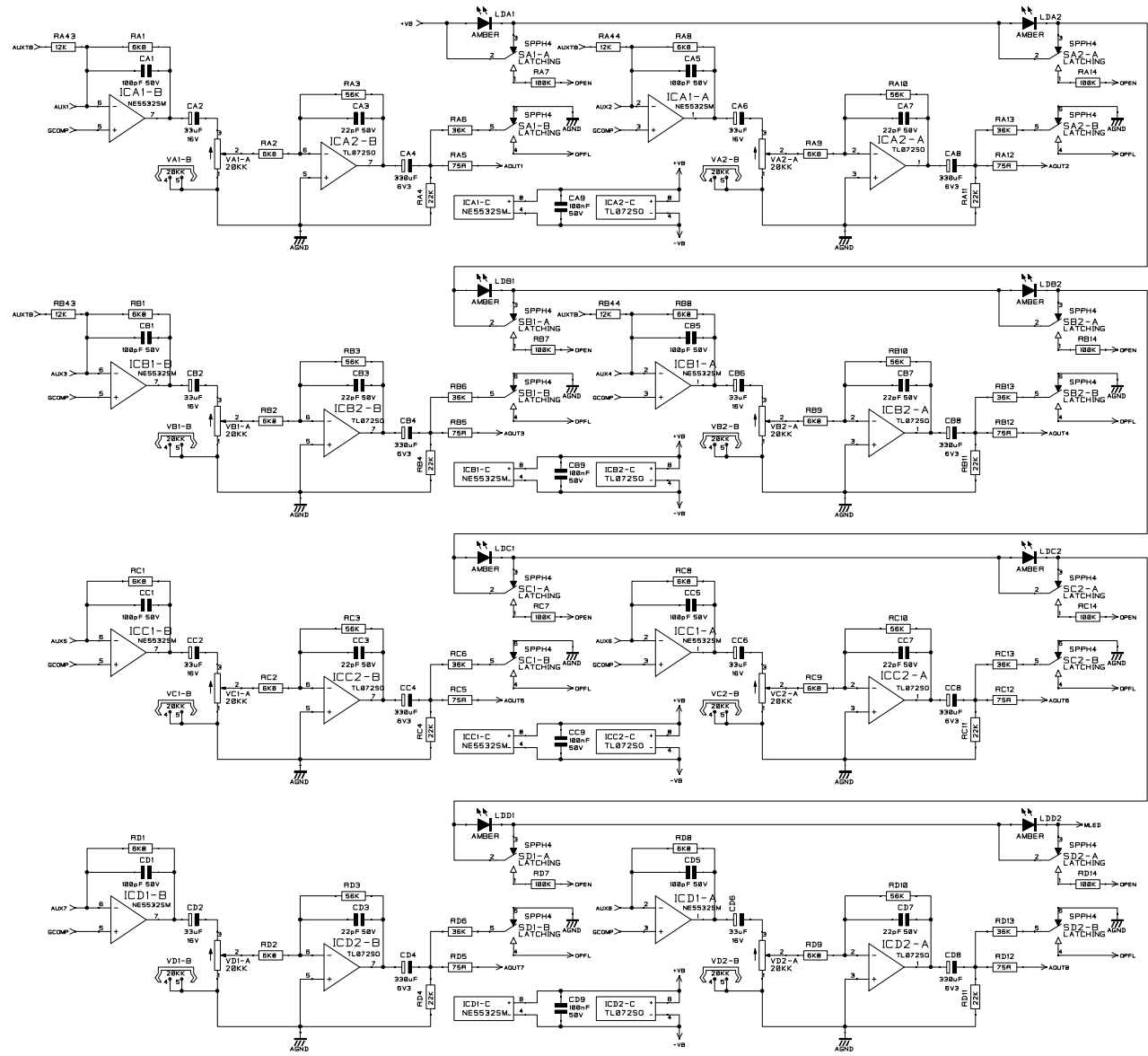
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SHEET 3



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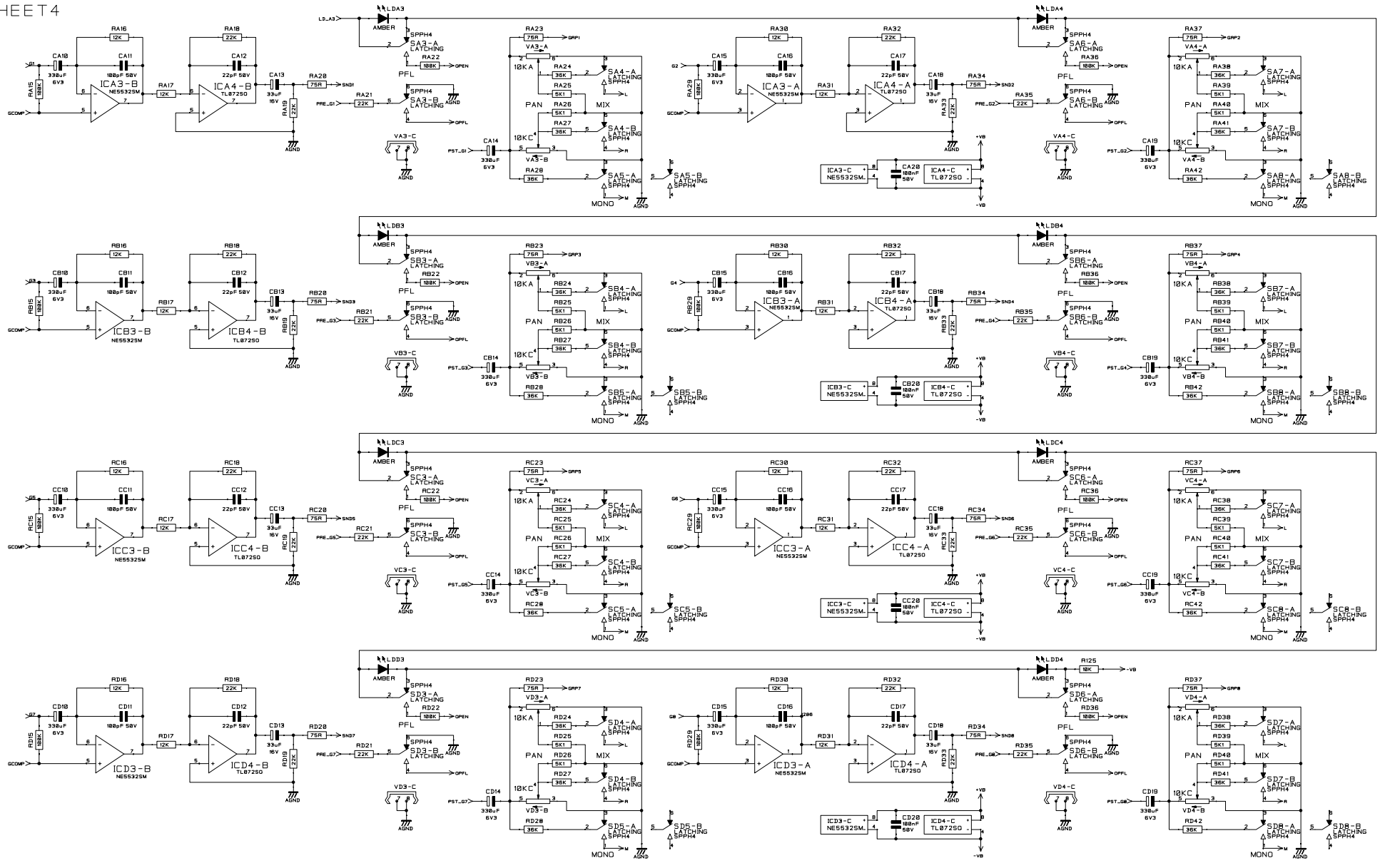
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SHEET 4



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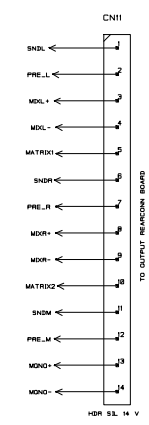
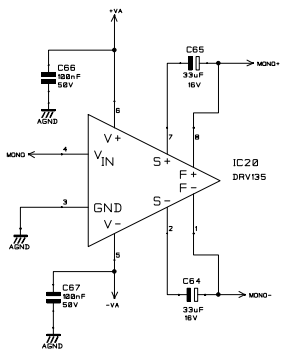
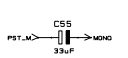
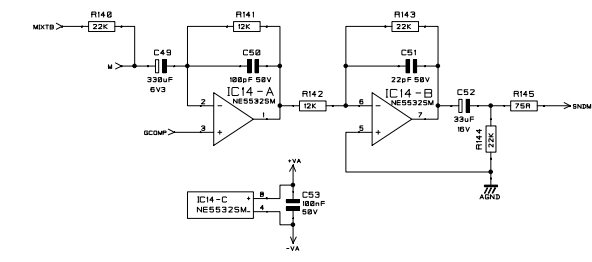
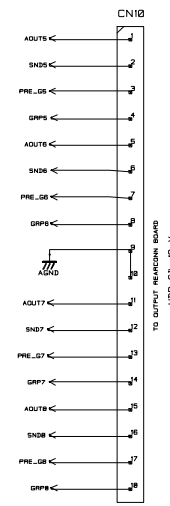
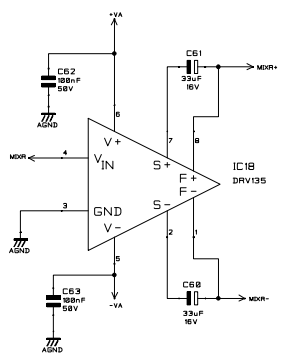
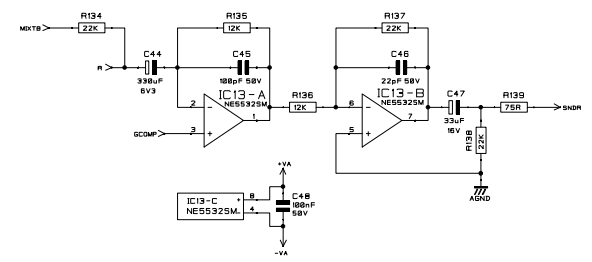
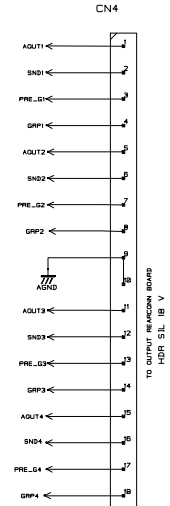
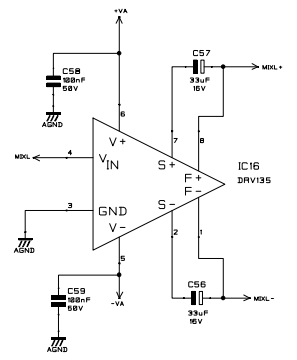
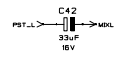
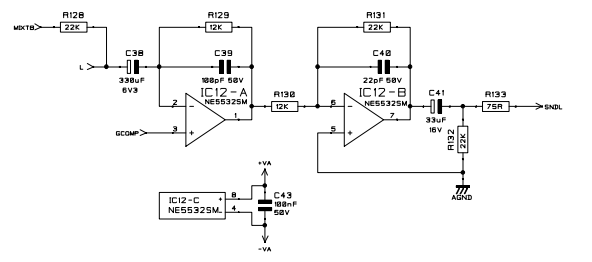
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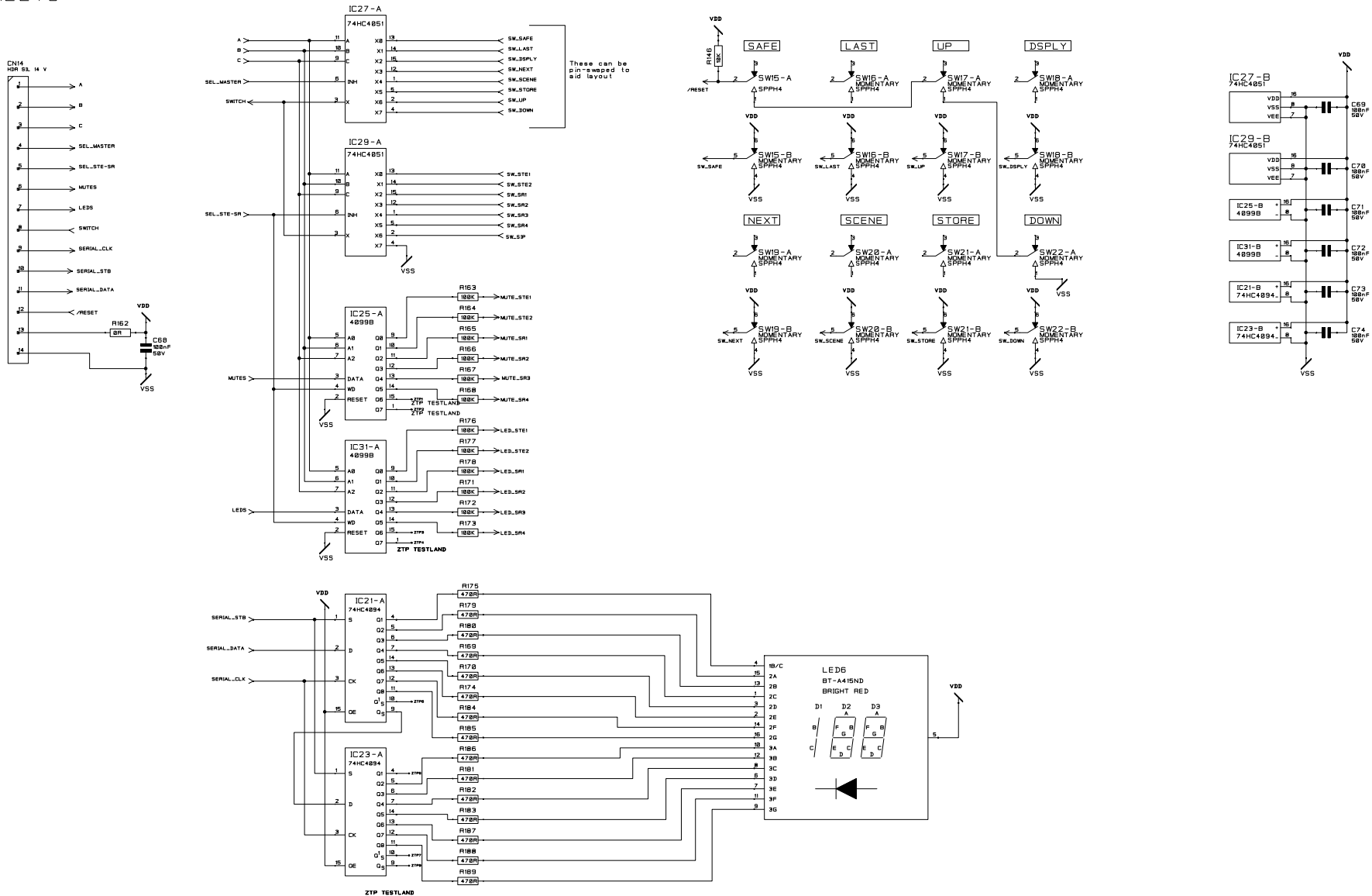
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SHEET 6



These can be pin-swapped to aid layout

NOTES

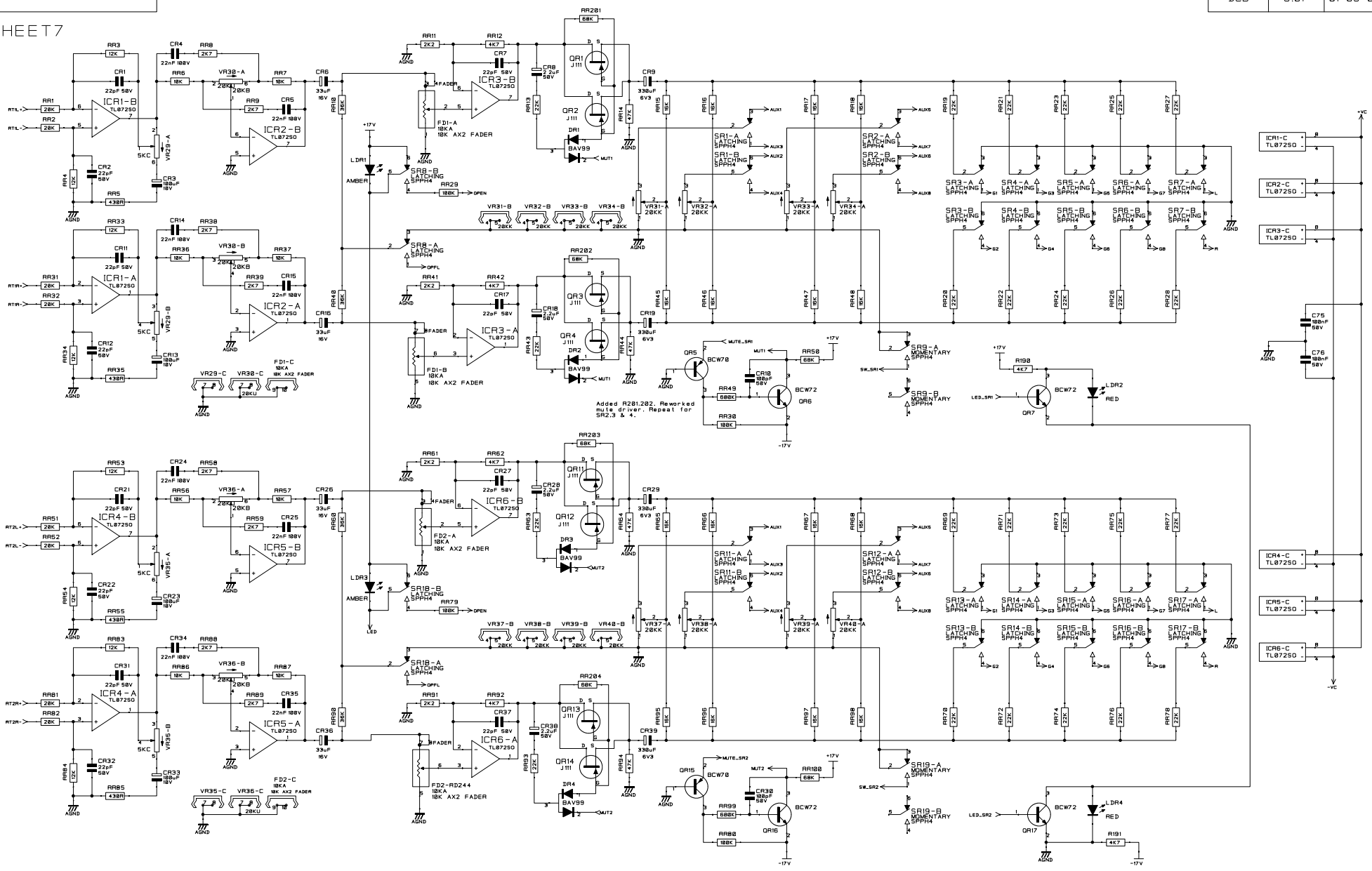
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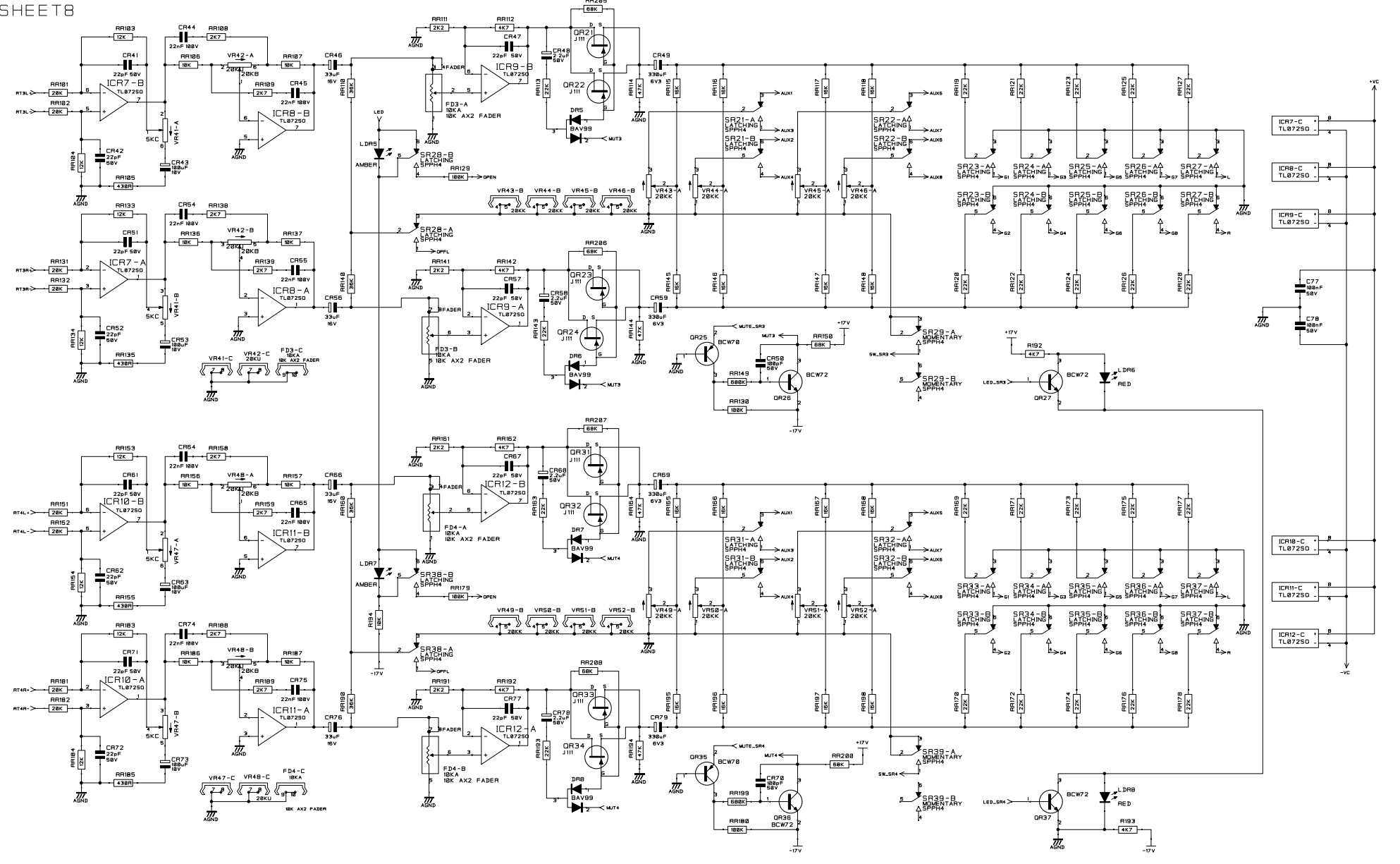
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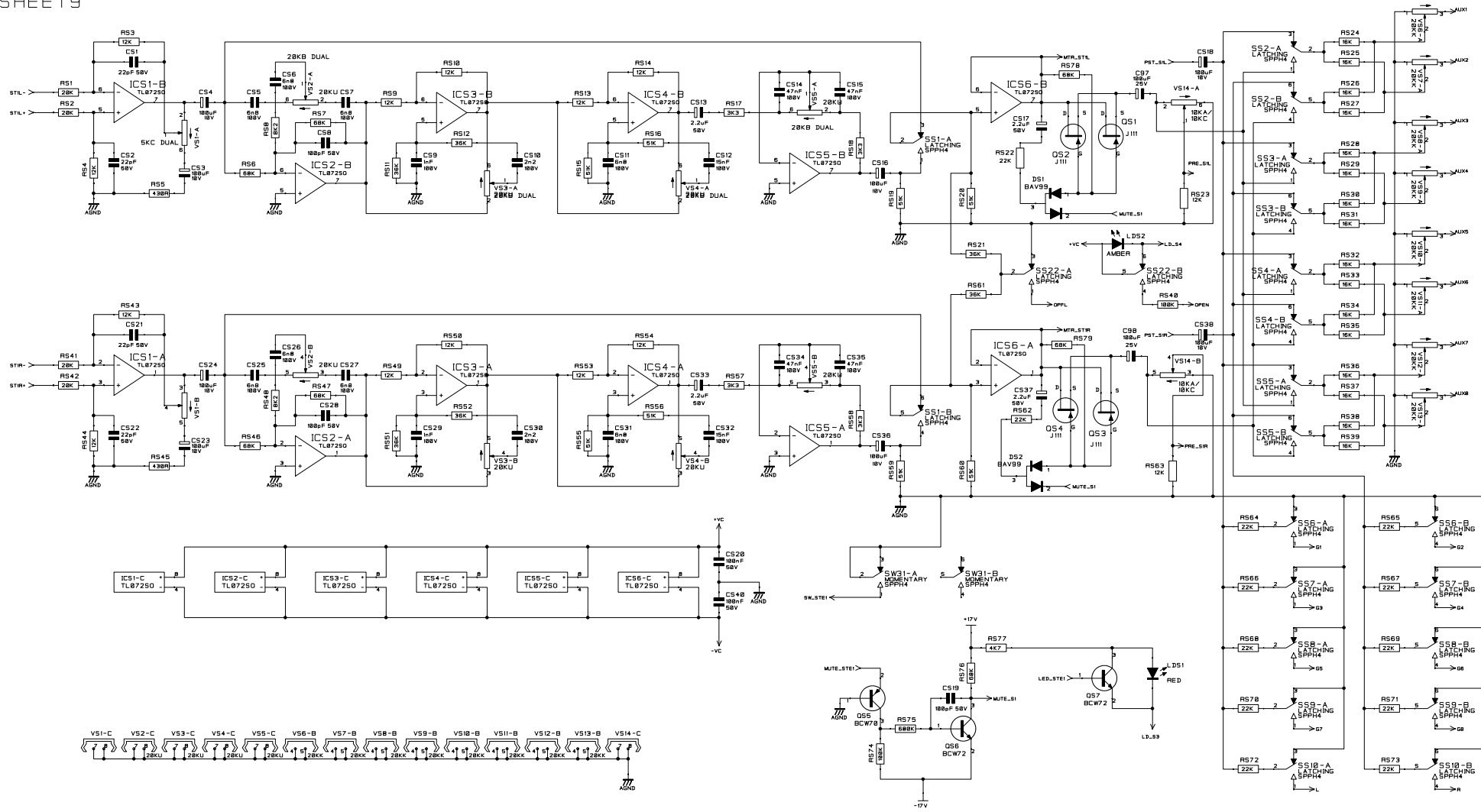
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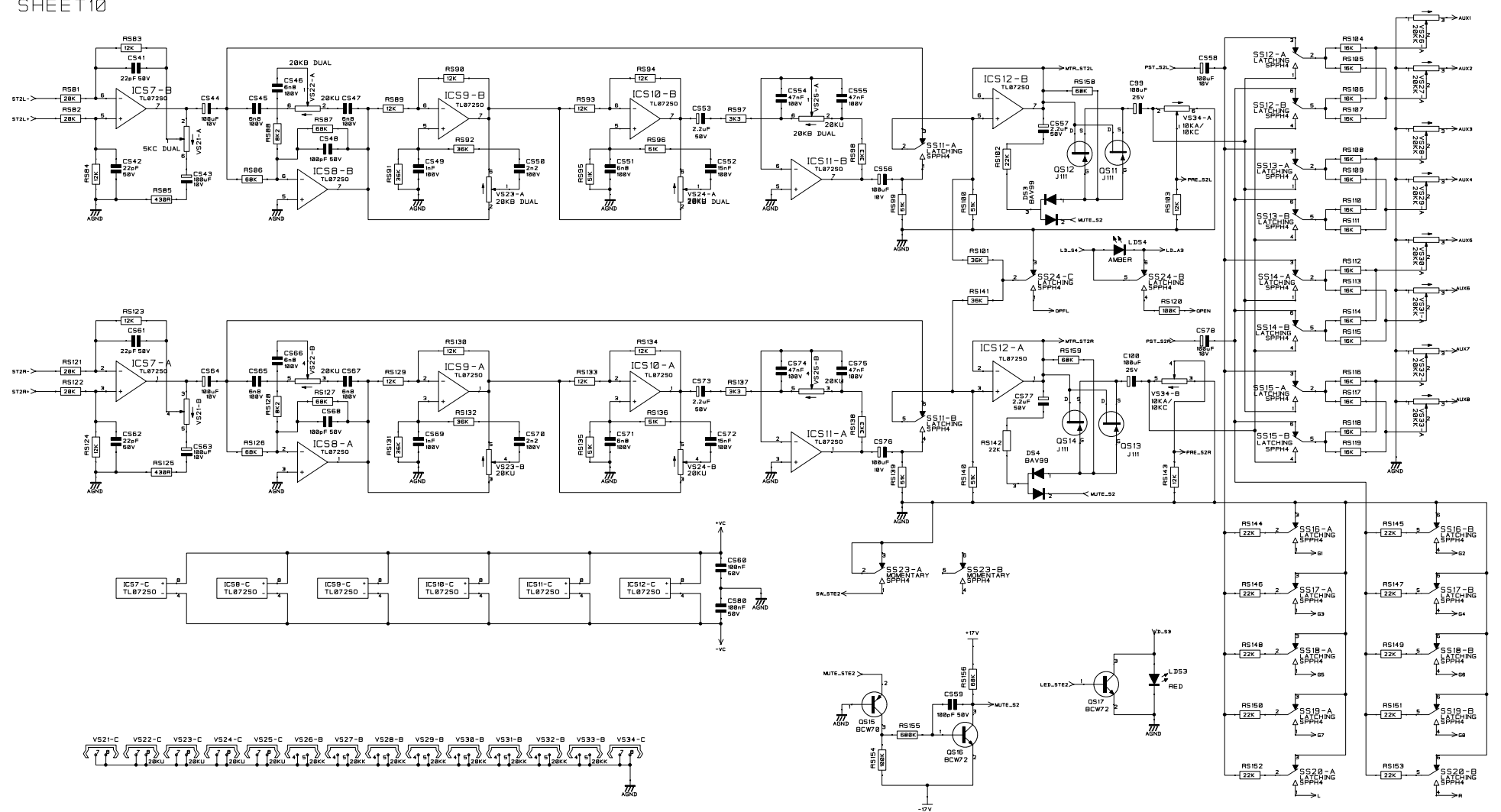
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SHEET 10



NOTES

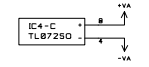
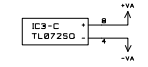
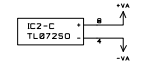
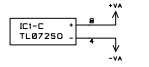
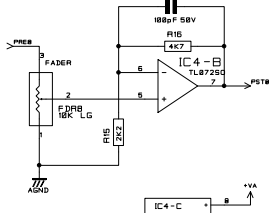
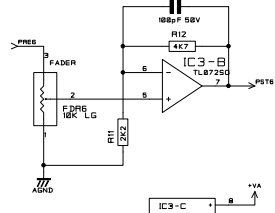
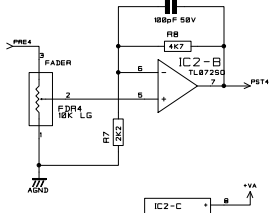
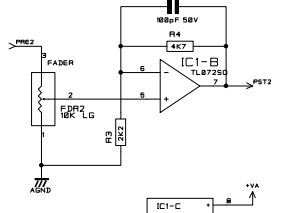
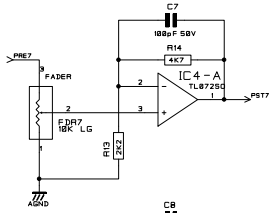
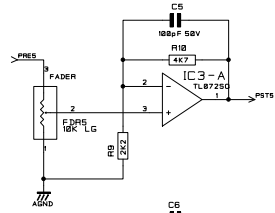
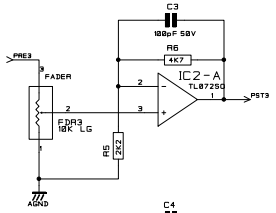
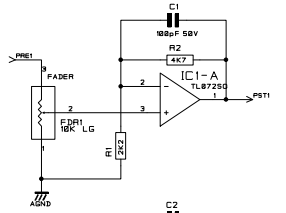
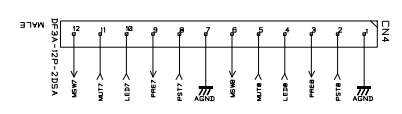
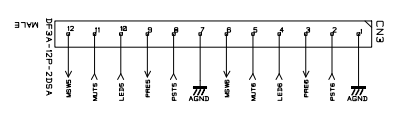
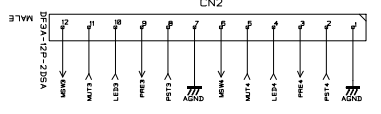
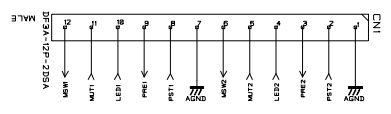
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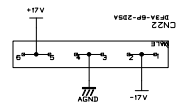
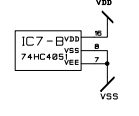
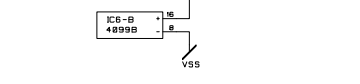
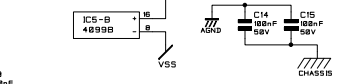
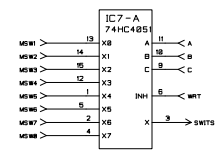
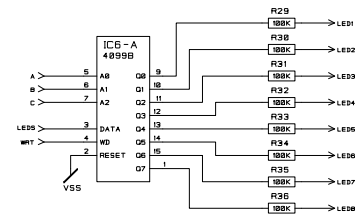
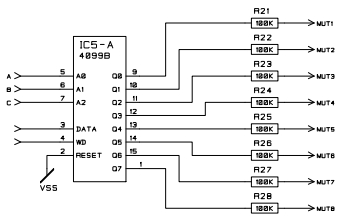
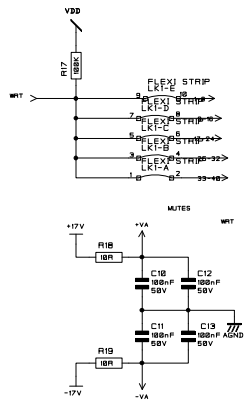
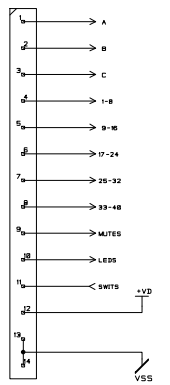
TITLE  
SERIES TWO  
MASTER

DRG NO. ED4020



CN5 HDR SIL 14 V  
PUT CN5 ON BACK OF PCB.

USE OPEN 10W HDR OR 2 ROWS OF 5 PIN SIL TO MAKE INTO JUMPERS.



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NOTES

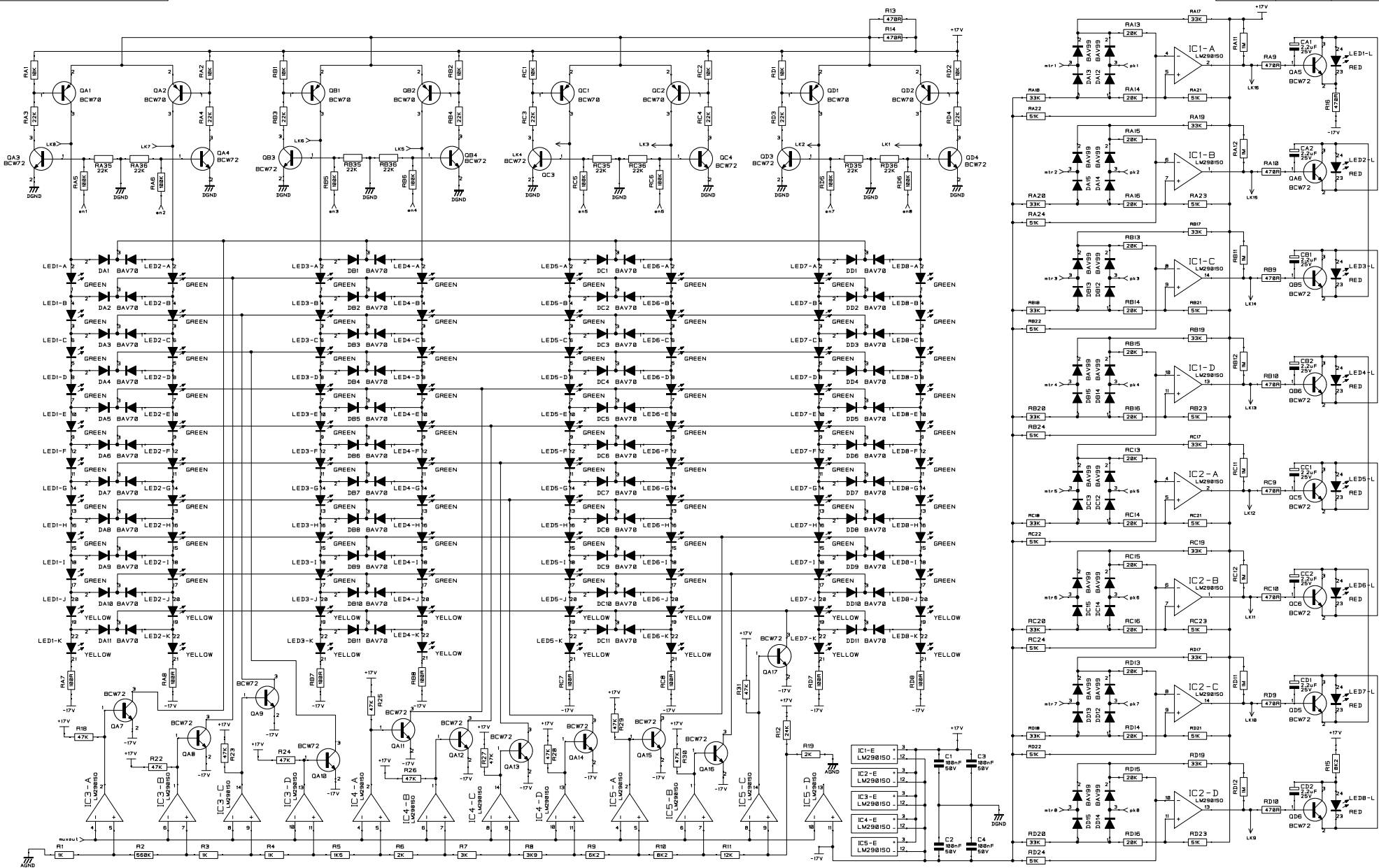
DRN. GHB  
DATE

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TITLE  
BLYTH LIVE  
INPUT FADER  
DRG NO. ED4021



INITIAL	ISSUE	DATE
DCB	6:01	08-03-00



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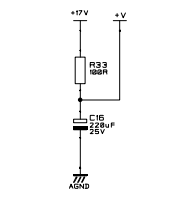
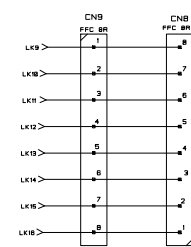
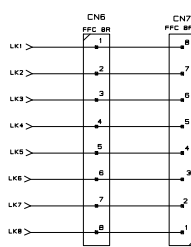
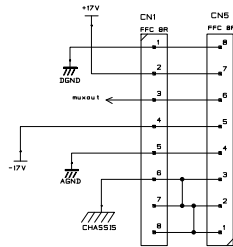
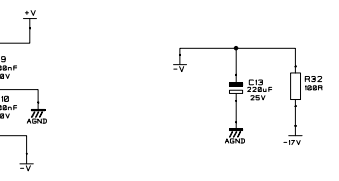
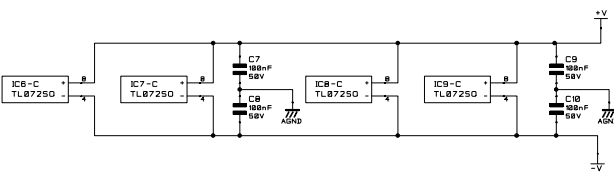
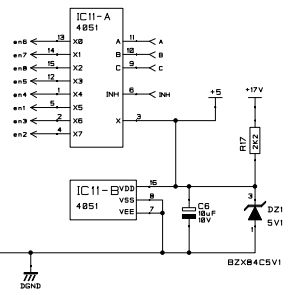
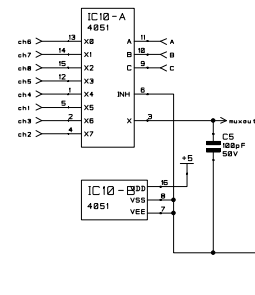
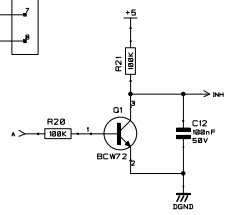
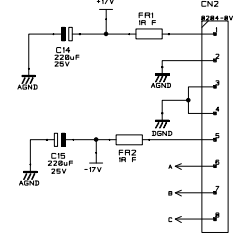
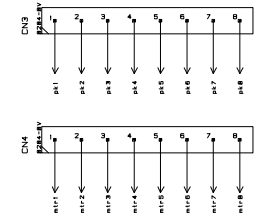
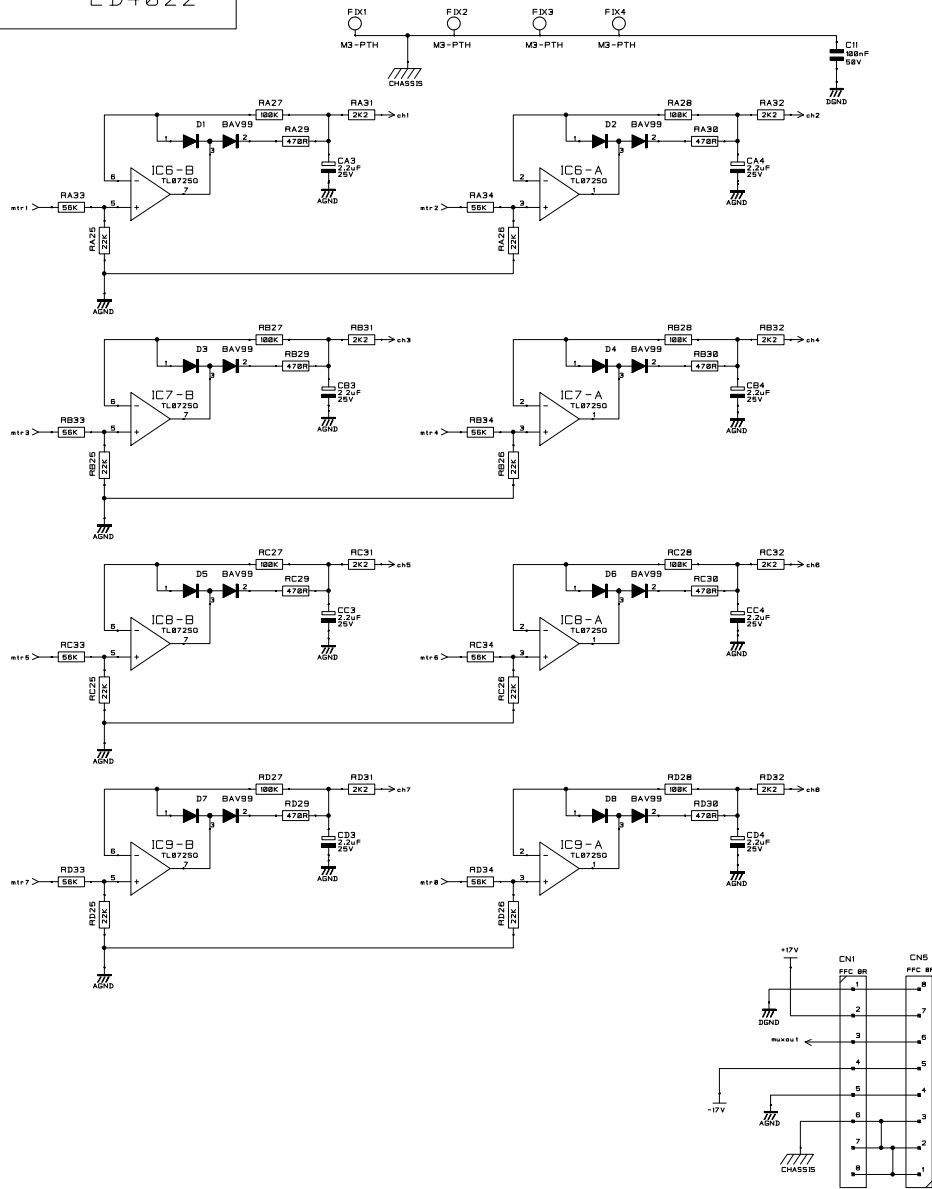
DRN.	GHB
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SERIES TWO  
METER BOARD

DRG NO.	ED4022
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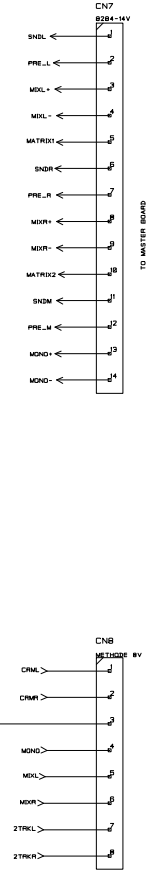
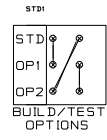
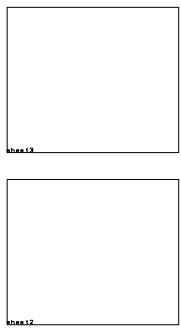
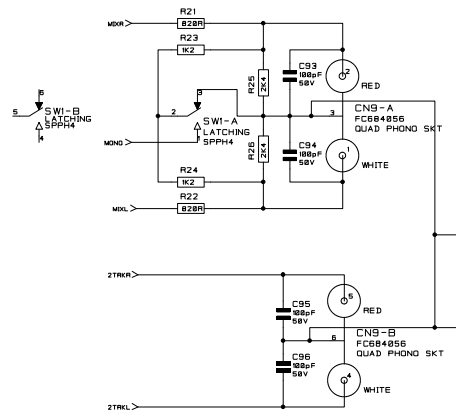
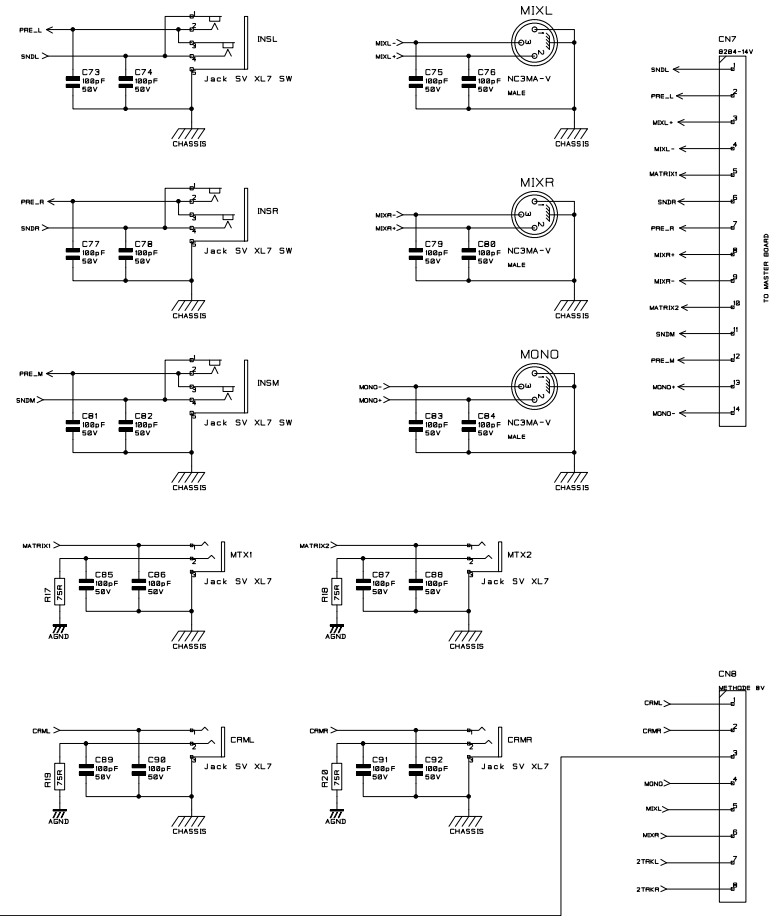
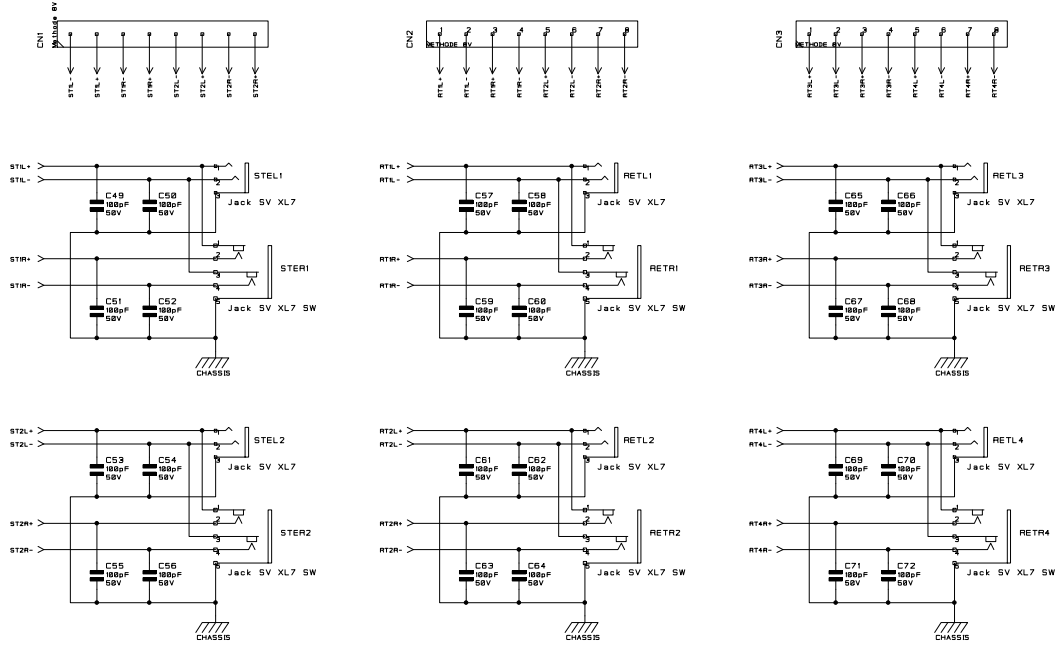
DATE

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METER BOARD

DRG NO. ED4022

INITIAL	ISSUE	DATE
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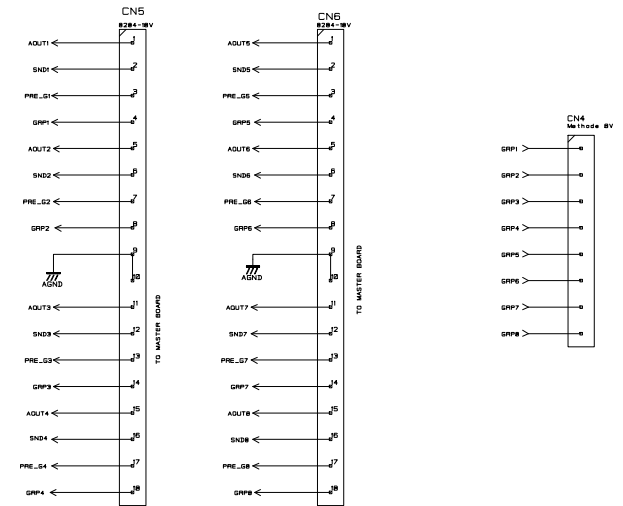
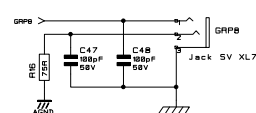
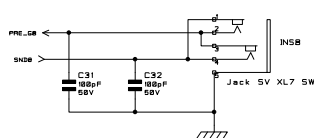
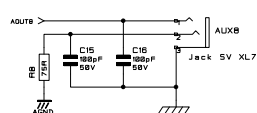
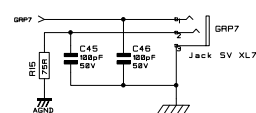
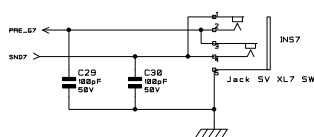
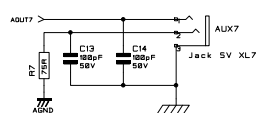
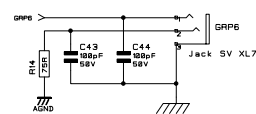
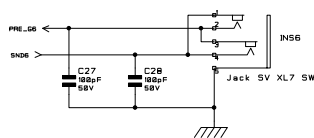
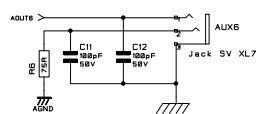
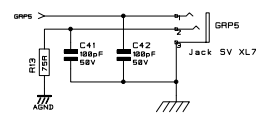
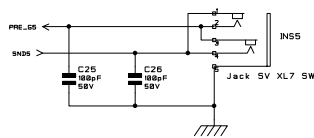
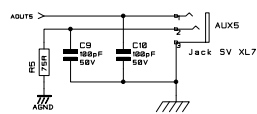
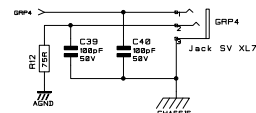
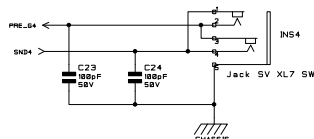
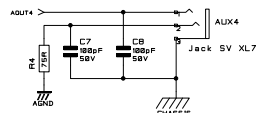
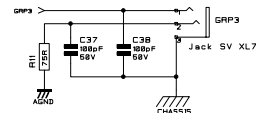
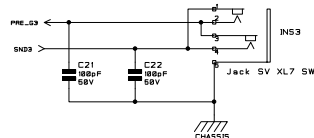
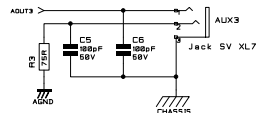
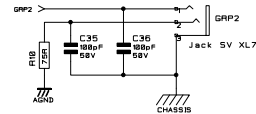
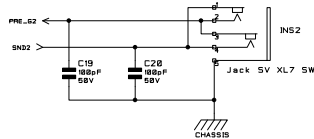
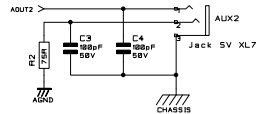
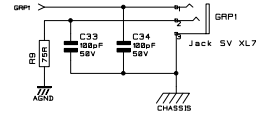
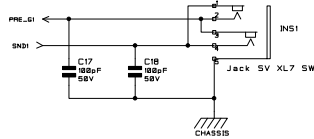
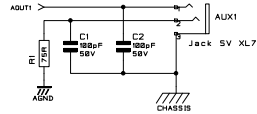
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TITLE  
SERIES TWO  
Rearconn & Midi  
DRG NO. ED4025

INITIAL	ISSUE	DATE
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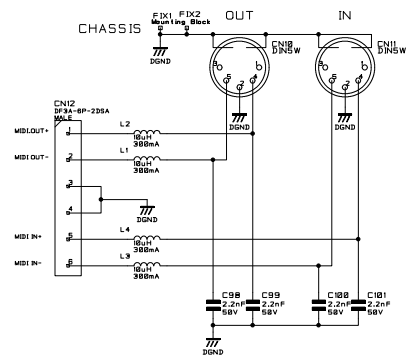
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PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CONNECTORS

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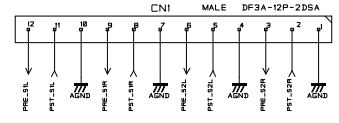
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DATE 00-00-00

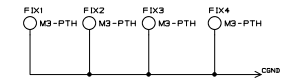
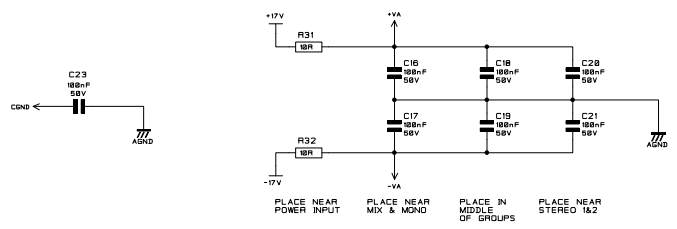
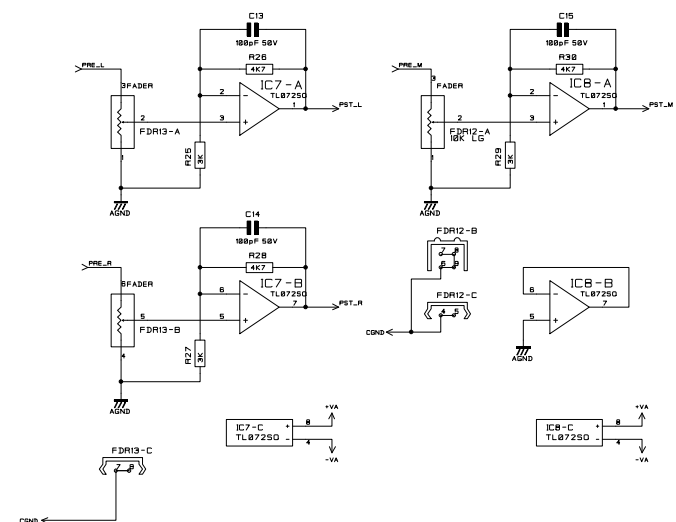
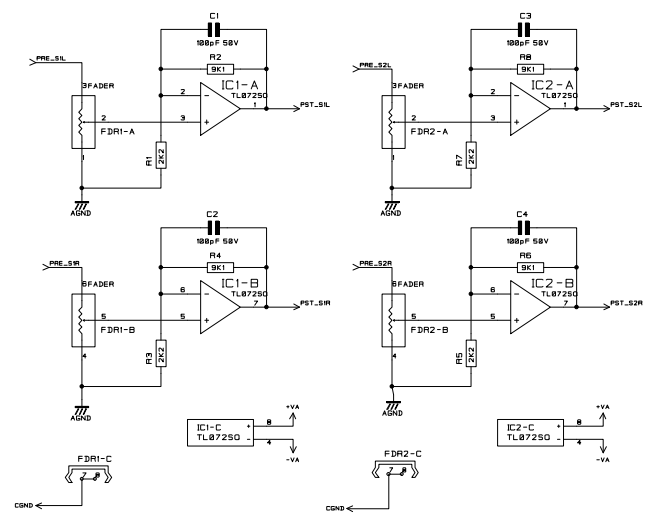
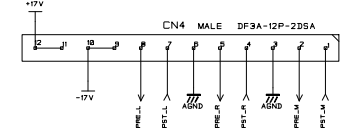
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Rearconn & Midi  
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STEREO 1 & 2



LR MIX & MONO



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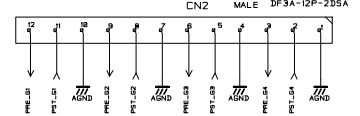
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DRN. YES  
 DATE 11-02-99

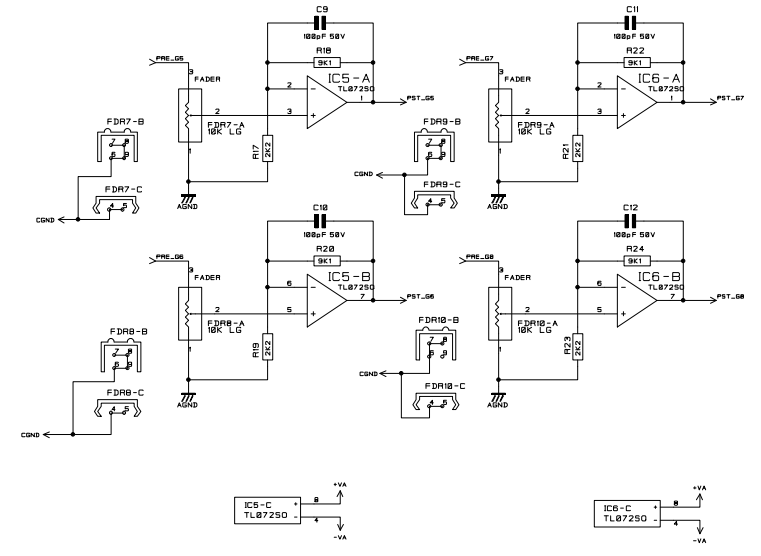
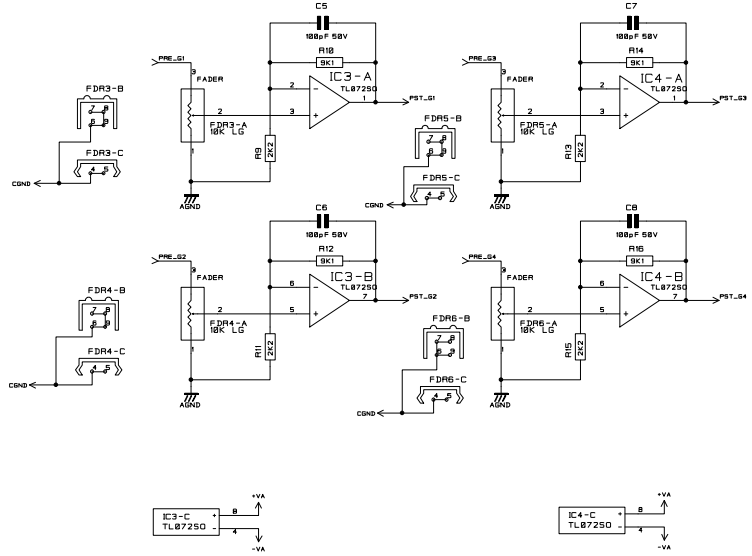
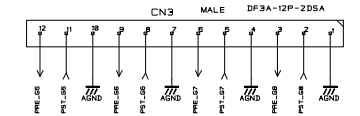
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TITLE  
 SERIES TWO  
 OUTPUT FADER PCB  
 STEREO, LR & MONO FADERS  
 DRG NO. ED4026

GROUPS 1-4



GROUPS 5-8



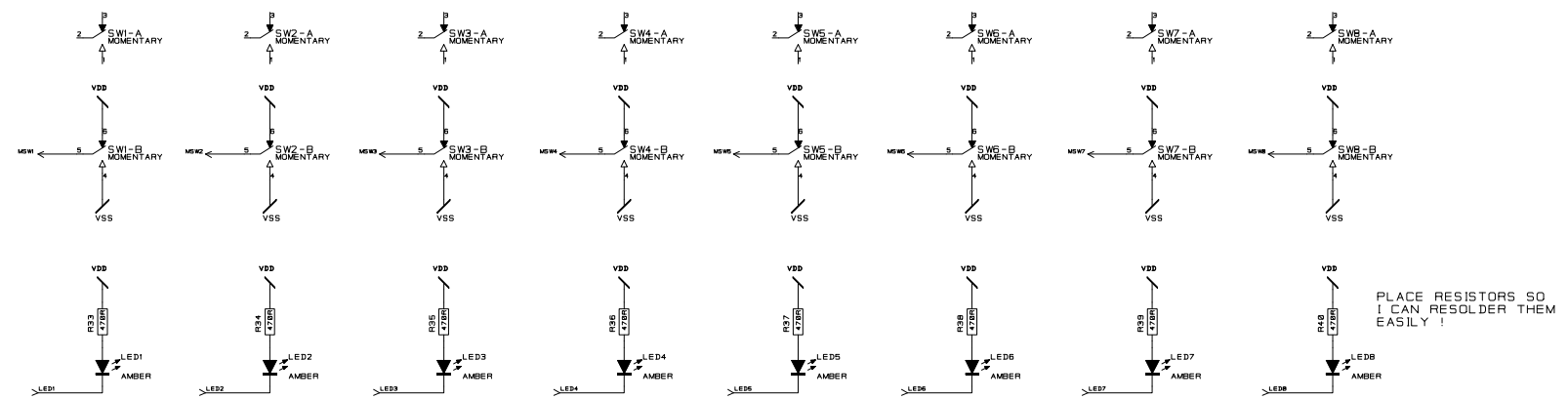
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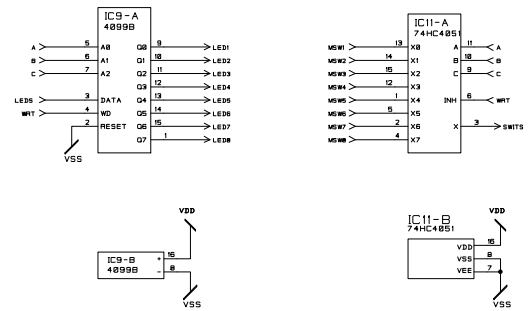
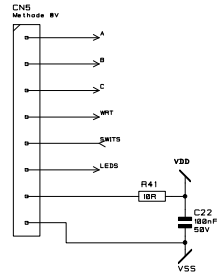
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SERIES TWO  
OUTPUT FADER PCB  
GROUP FADERS  
DRG NO. ED4026

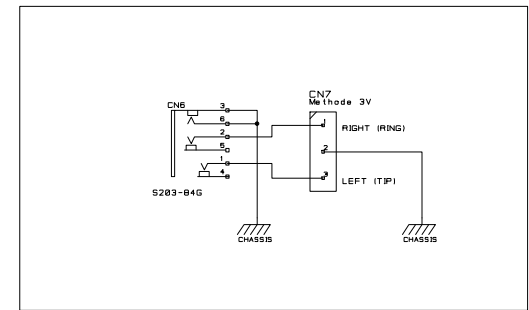


PLACE RESISTORS SO I CAN RESOLDER THEM EASILY !

FLOOD FILL WITH Vss



HEADPHONE SOCKET



FLOOD FILL WITH CHASSIS. KEEP CHASSIS FLOOD AT LEAST 5mm AWAY FROM Vss FLOOD FILL

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NOTES

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DATE 11-02-99

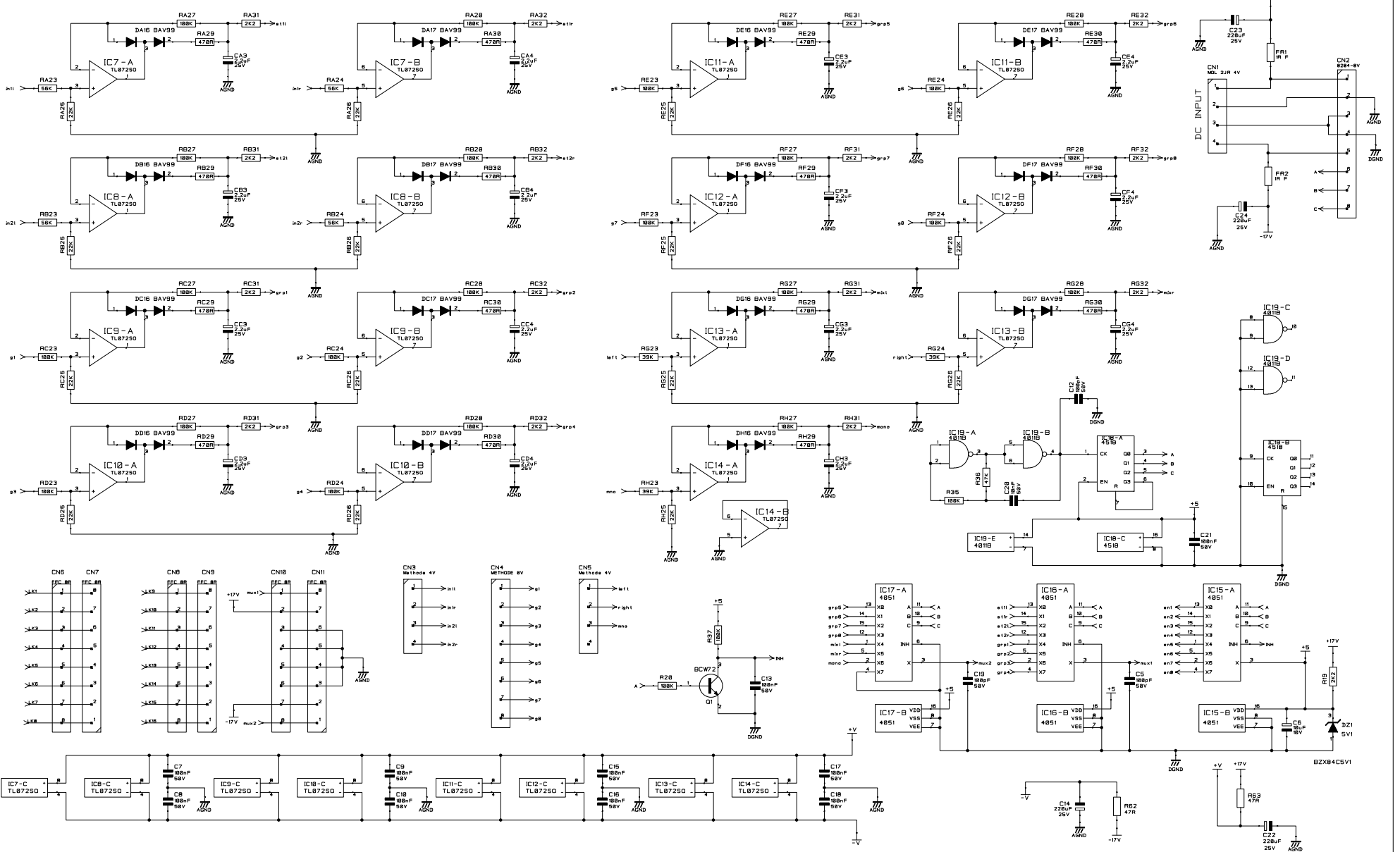
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TITLE  
SERIES TWO  
OUTPUT FADER PCB  
MUTE GROUP PCB  
DRG NO. ED4026



DRG NO. ED4027

INITIAL	ISSUE	DATE
TW	6:02	19-4-00



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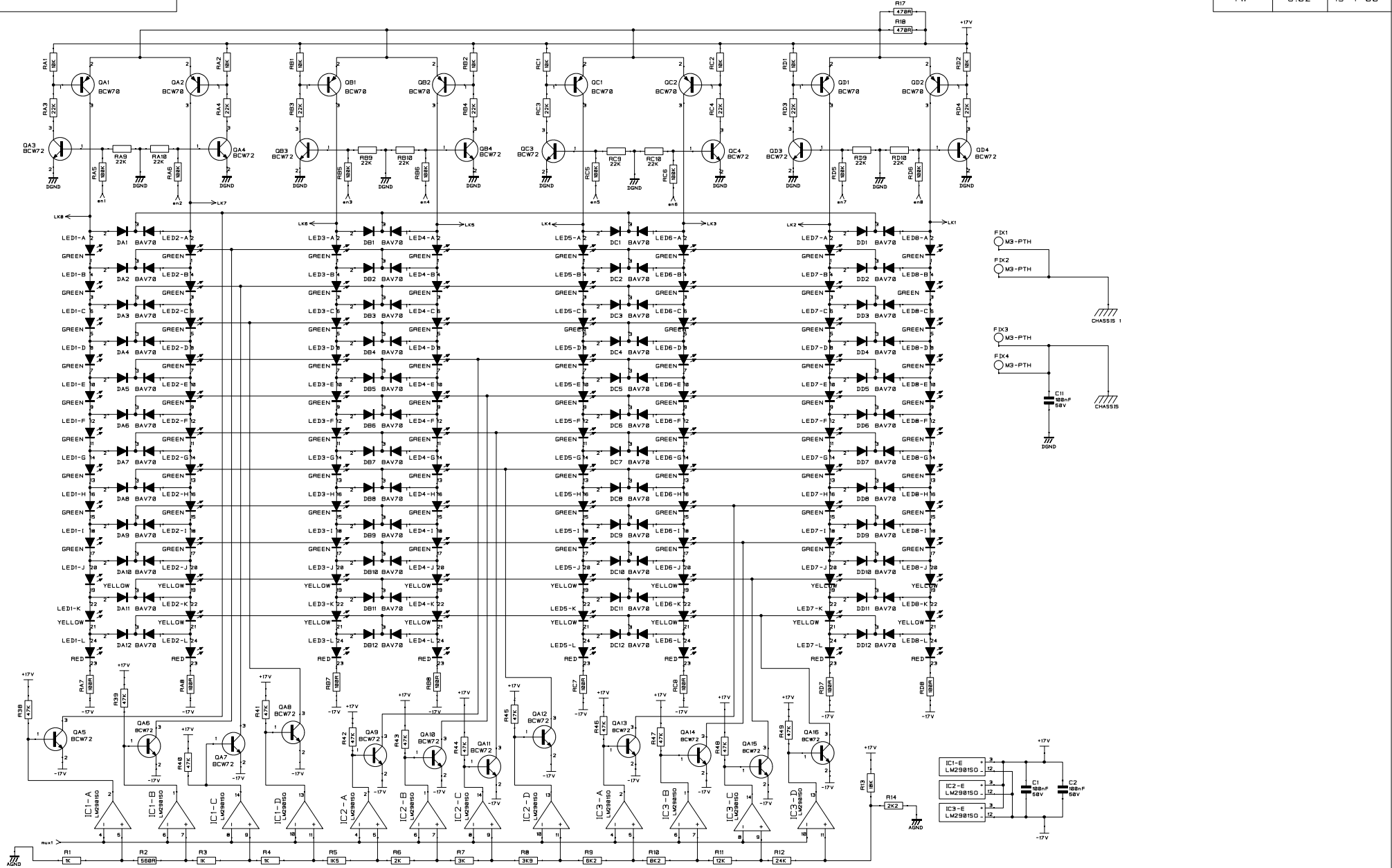
NOTES

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DATE 22-02-99

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TITLE  
SERIES TWO  
O/P METER  
DRG NO. ED4027  
SHT. 1 OF 3

INITIAL	ISSUE	DATE
TW	6:02	19-4-00



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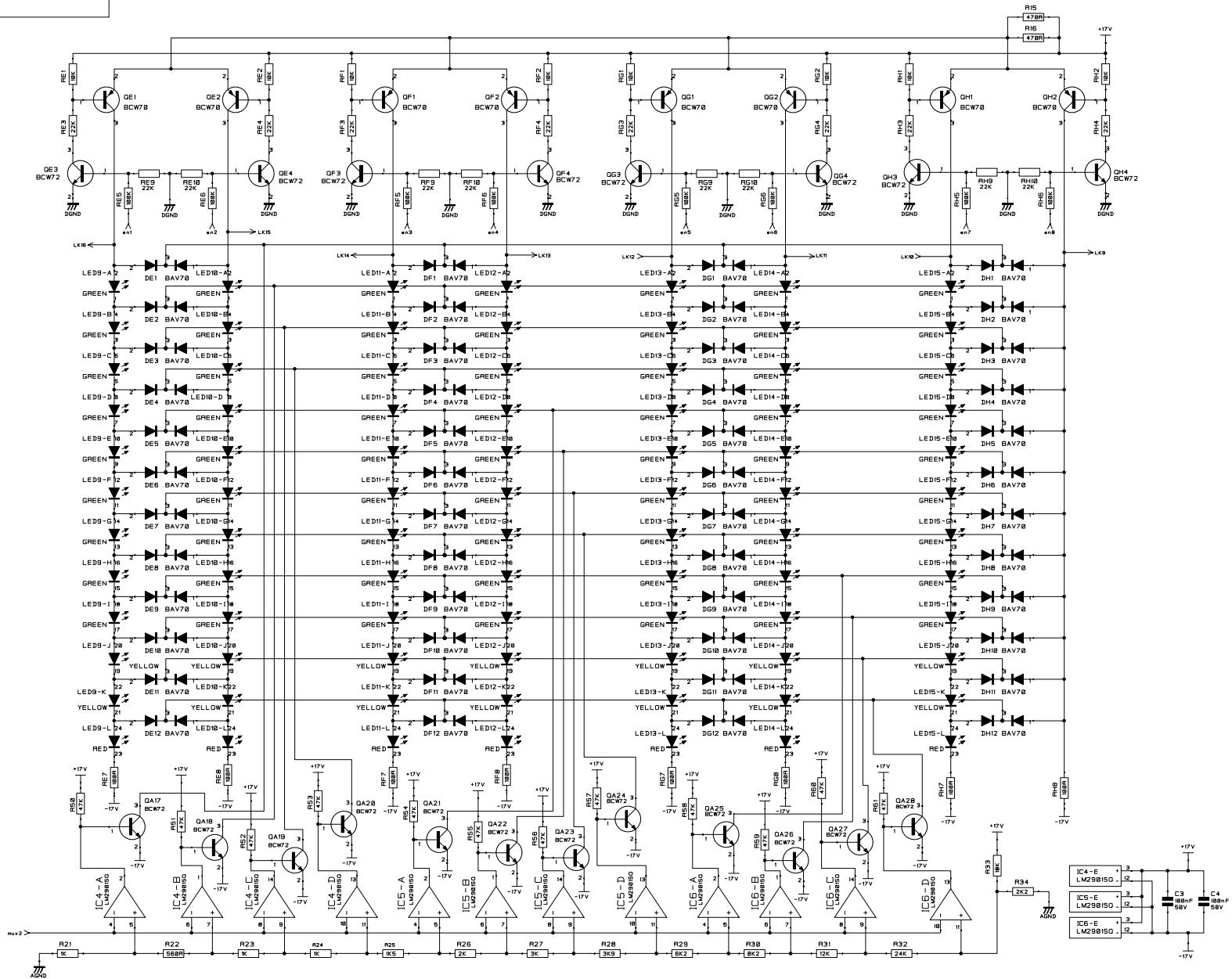
NOTES

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DATE 22-02-99

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FAX: 01707 650482

TITLE  
SERIES TWO  
O/P METER  
DRG NO. ED4027

INITIAL	ISSUE	DATE
TW	6:02	19-4-00



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TITLE  
SERIES TWO  
O/P METER

DRG NO. ED4027

DRG NO. ED4028

INITIAL	ISSUE	DATE
YS	1:00	11-03-99

Microcontroller

Fader Servos 1-4

Fader Servos 5-8

Channel Interface

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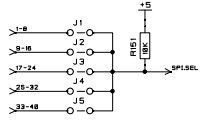
TITLE  
SERIES TWO  
MOVING FADER  
INTERFACE PCB

DRG NO. ED4028

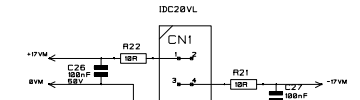
SHT. 1 OF 4

INITIAL	ISSUE	DATE
YS	1:00	11-03-99

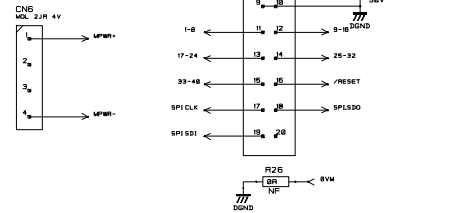
Use Open 10-Way Header or 2 Rows of 5-Pin SIL To Make Into Jumpers



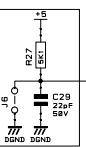
PLACE CONNECTOR CN1 ON BOTTOM SIDE OF PCB



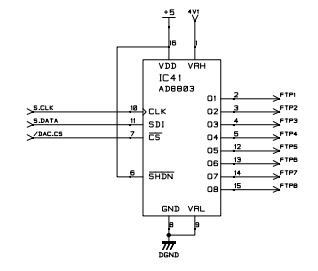
PLACE CONNECTOR CN6 ON BOTTOM SIDE OF PCB



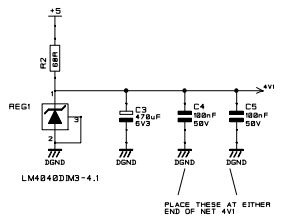
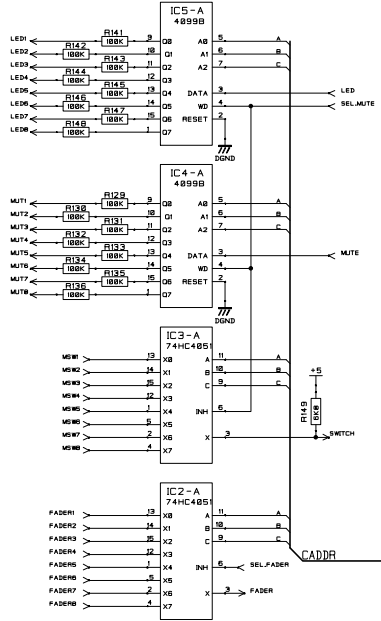
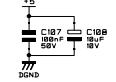
Place 0.5MHz Oscillator (L1) as close as possible to Pin 18 during In-Circuit Programming



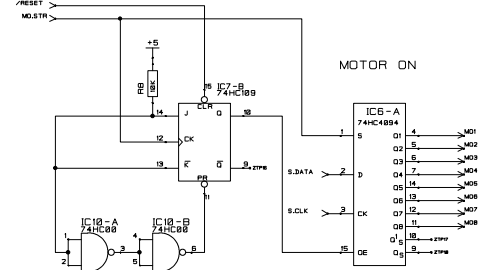
FADER TARGET POSITION



Supply Decoupling for AD8883 Place close to the IC Route separate traces from the input connector if possible

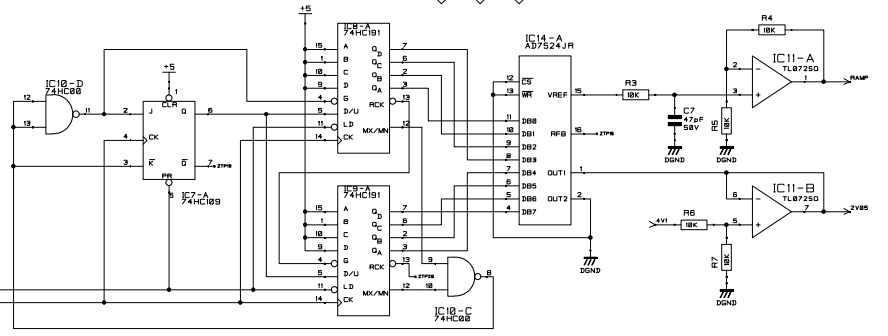


PLACE THESE AT EITHER END OF NET +5V



MOTOR ON

RAMP GENERATOR



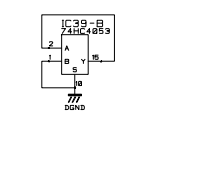
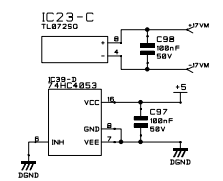
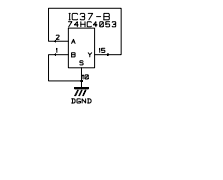
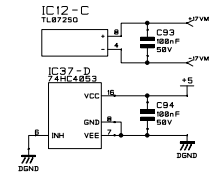
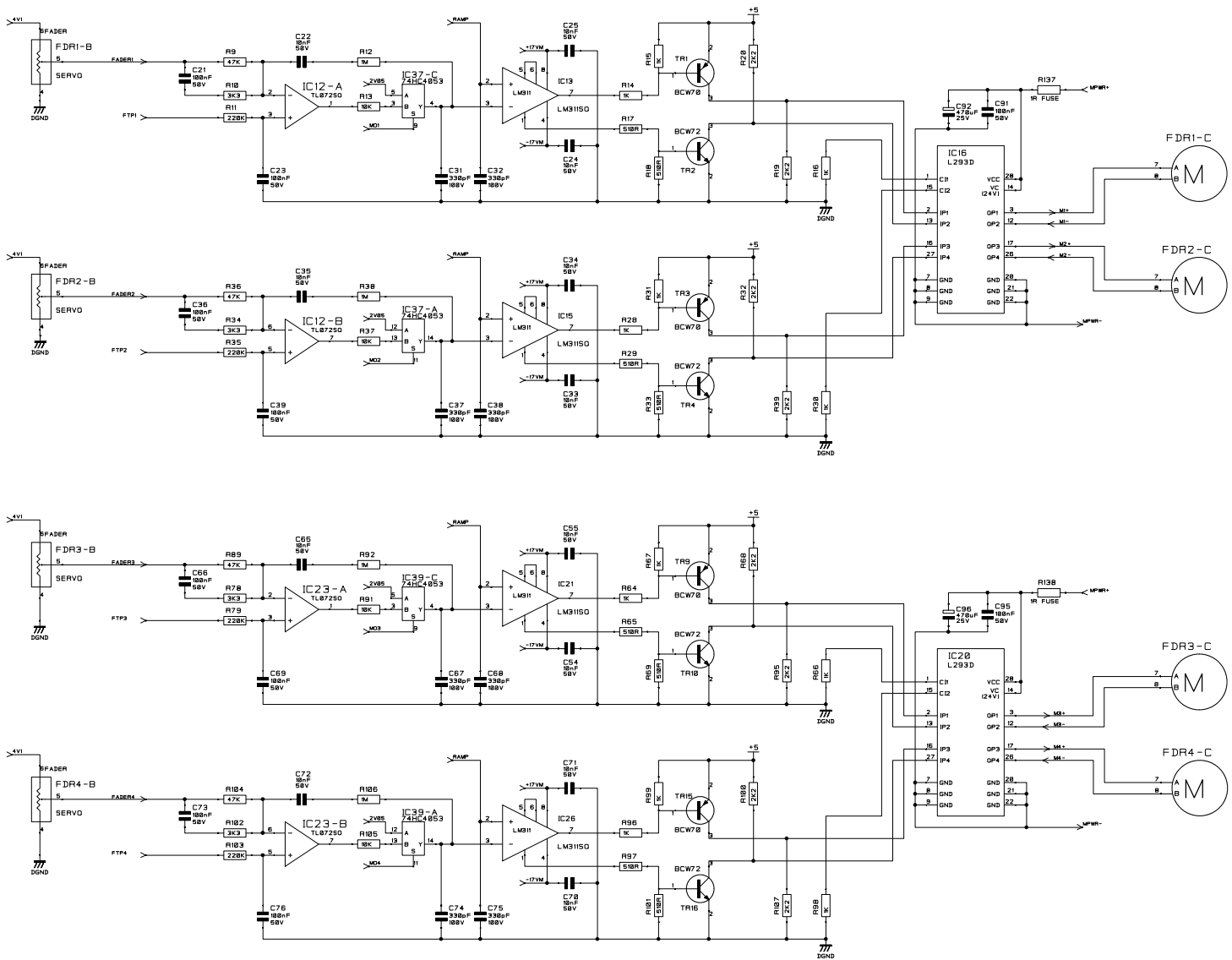
CONTROL LOGIC

**NOTES**  
**IMPORTANT**  
 This PCB is extremely layout critical, particularly:  
 Fader1-Fader8, Fader, 4V1 and 2V05 nets  
 Shield these nets using DGND.  
 Copy the layout used on the latest issue of the Digi-328 IP Control Surface PCB (IED3007) as closely as possible.  
 See Gordon Mills or Yan Speake for guidance

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TITLE  
**SERIES TWO**  
 MOVING FADER  
 INTERFACE PCB  
 DRG NO. ED4028  
 SHEET 1 OF 4

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FADER SERVOS 1-4

NOTES

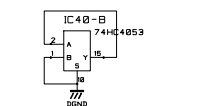
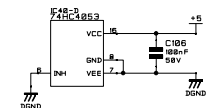
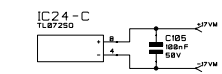
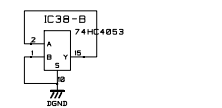
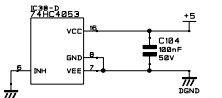
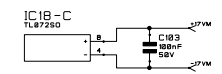
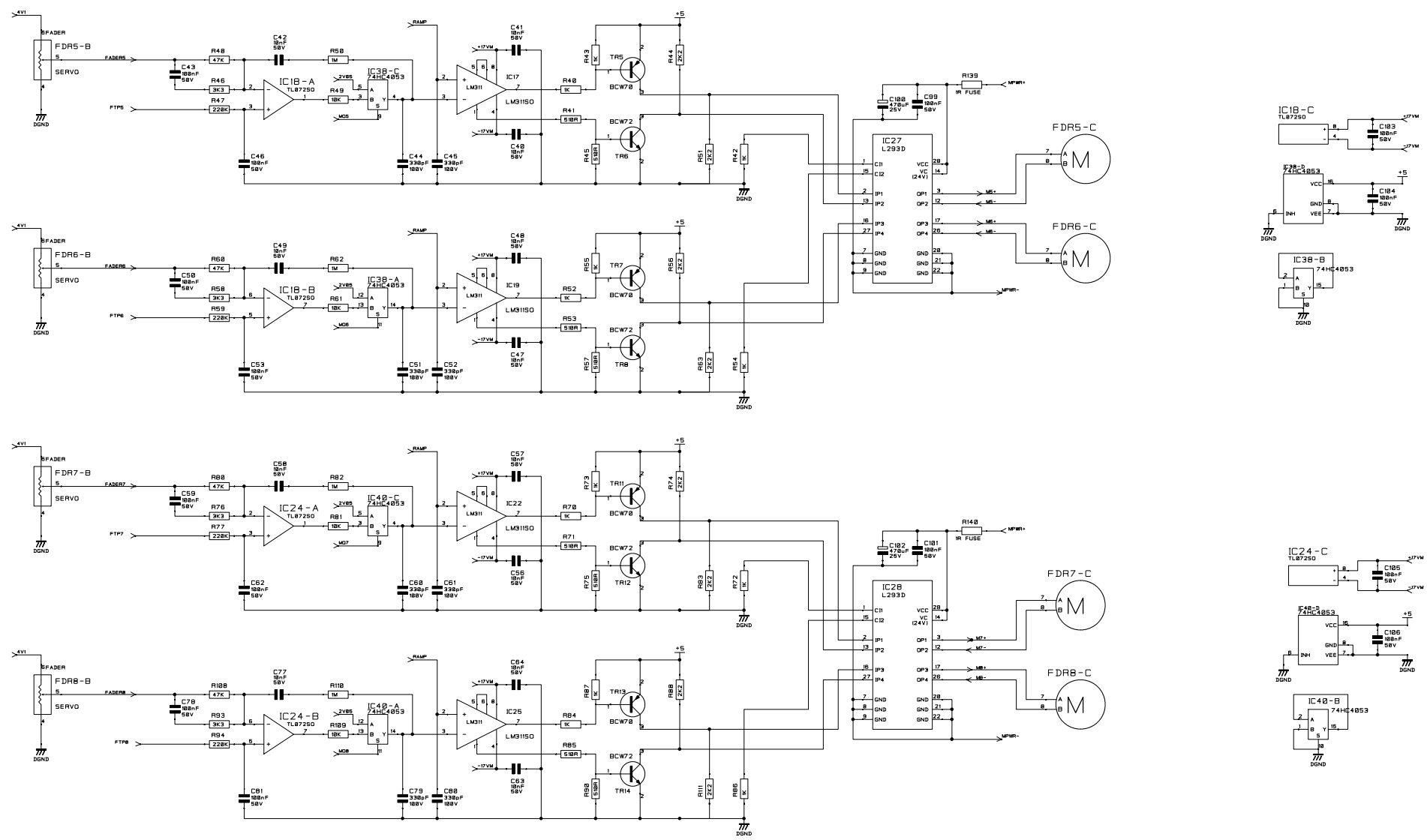
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TITLE  
SERIES TWO  
MOVING FADER  
INTERFACE PCB

DRG NO. ED4028



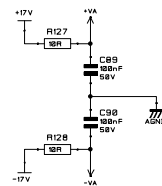
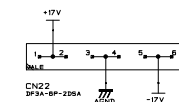
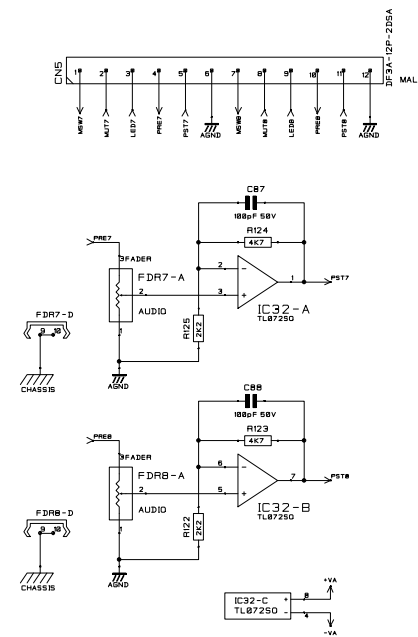
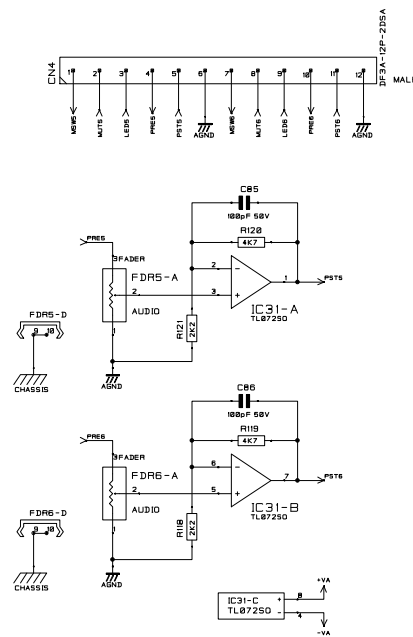
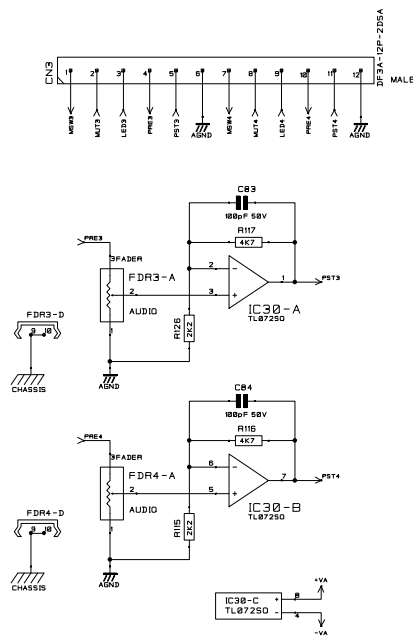
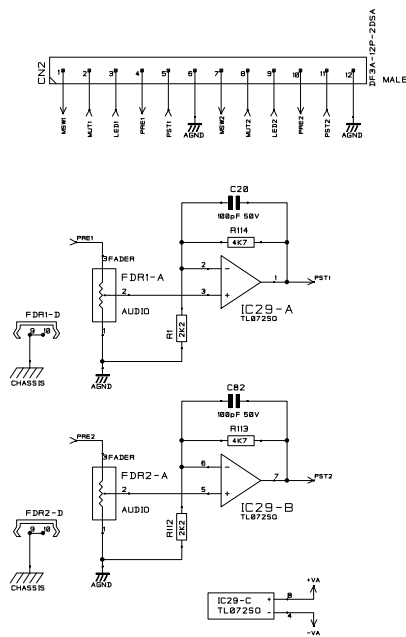
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MOVING FADER  
INTERFACE PCB  
DRG NO. ED4028



CHANNEL INTERFACE

NOTES

CAUTION - AUDIO CIRCUITRY  
KEEP AWAY FROM DIGITAL AND SERVO CIRCUITS  
AND PLACE IN "AGND" GROUND PLANE.  
SEPERATE ANALOGUE AND DIGITAL  
PLANES BY AT LEAST 5mm

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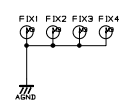
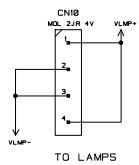
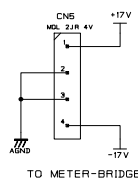
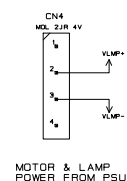
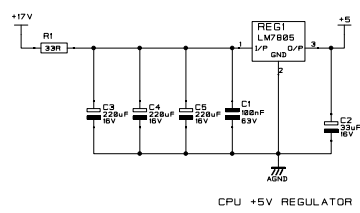
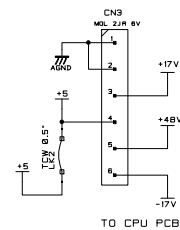
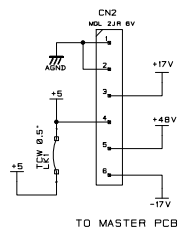
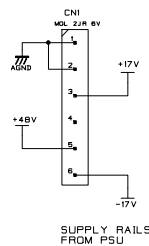
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SERIES TWO  
MOVING FADER  
INTERFACE PCB

DRG NO. ED4028





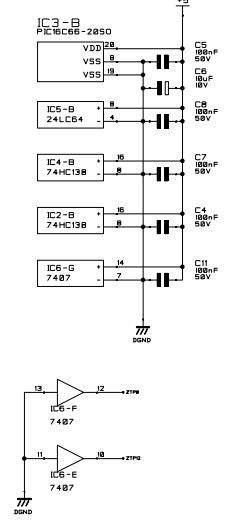
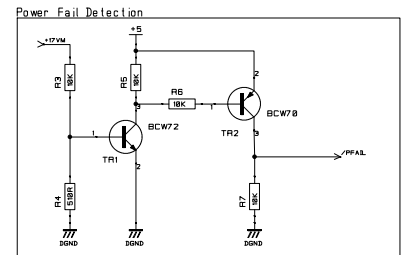
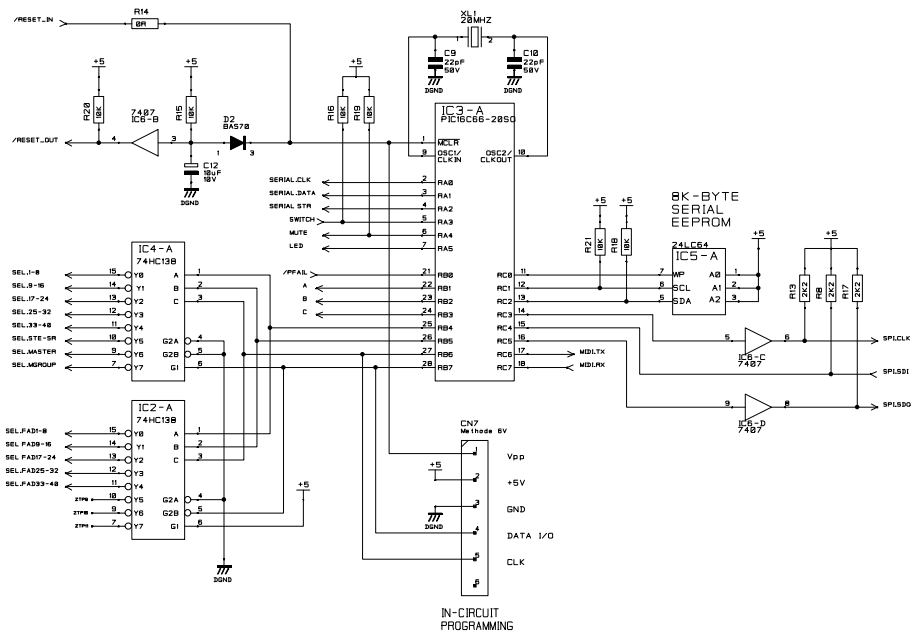
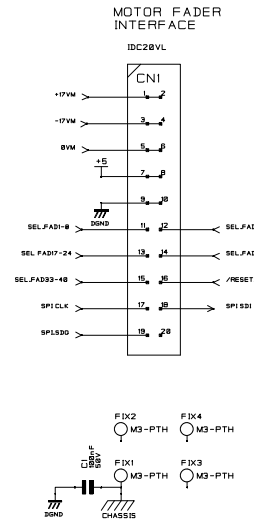
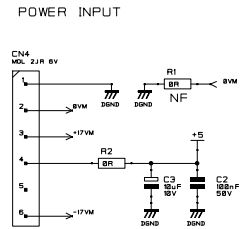
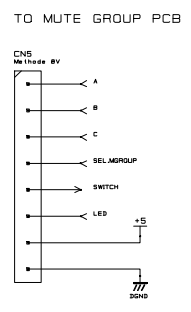
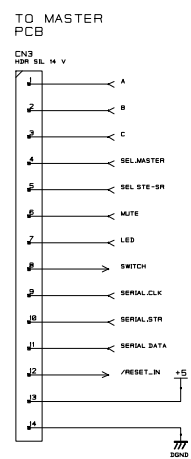
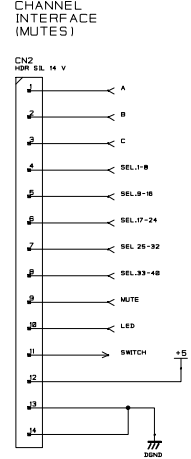
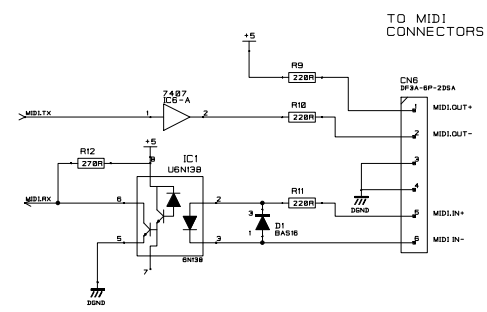
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TITLE  
SERIES TWO  
PSU DISTRIBUTION PCB  
DRG NO. ED4041



**LAYOUT NOTES**

To minimise EM radiation into O/P fader PCB, if possible, route all Clock Signals on top side only. Non-clock signals can be routed either side.

Flood fill bottom side with DGND, particularly beneath microprocessor and, if possible beneath logic ICs.

Flood-fill top side with DGND also.

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NOTES

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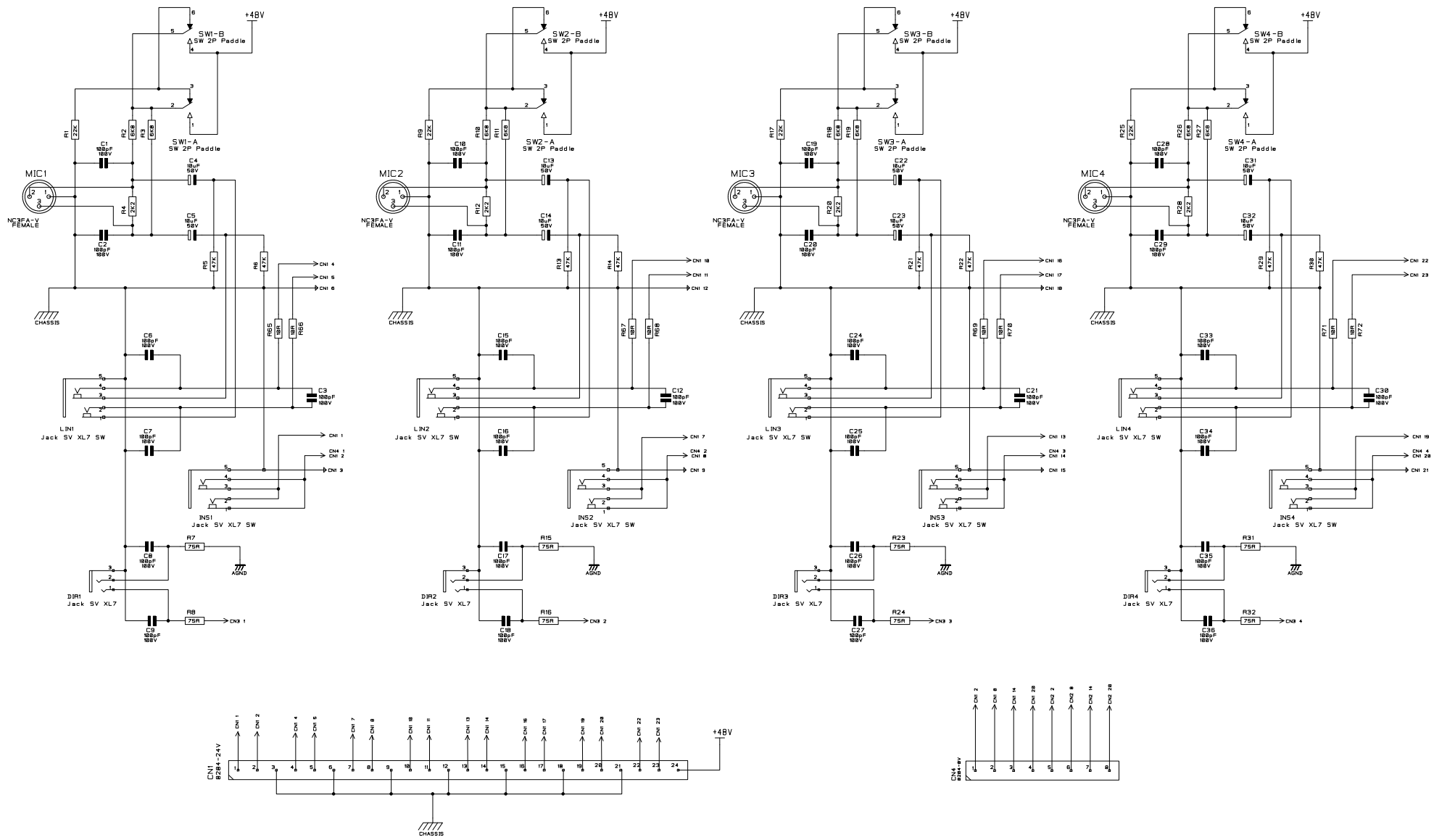
DATE 24-05-99

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TITLE  
**SERIES TWO**  
MUTE AUTOMATION  
CPU PCB

DRG NO. ED4023

SHT. 1 OF 1



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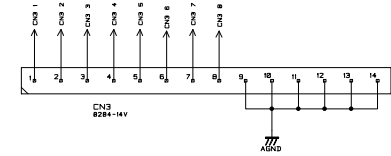
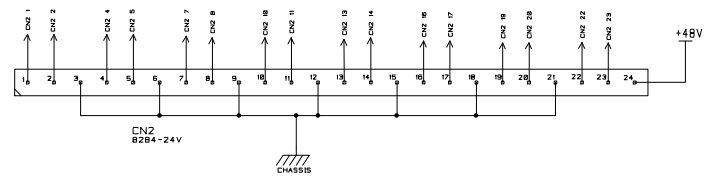
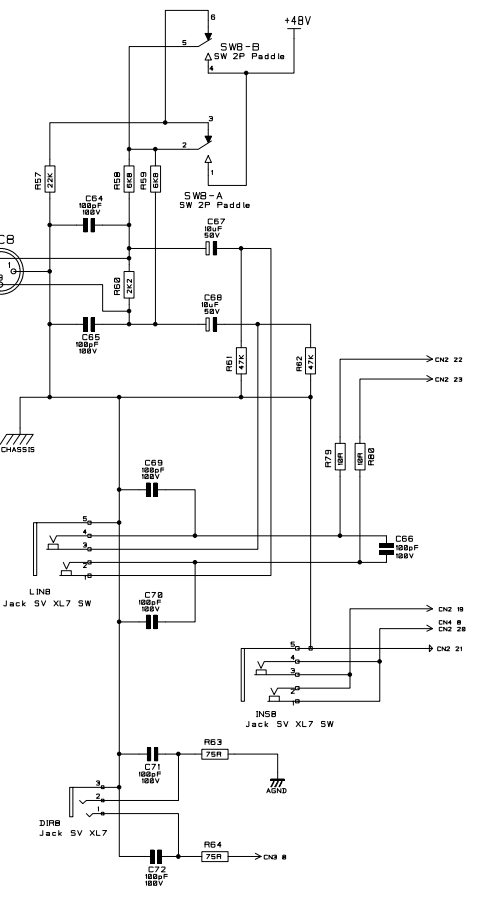
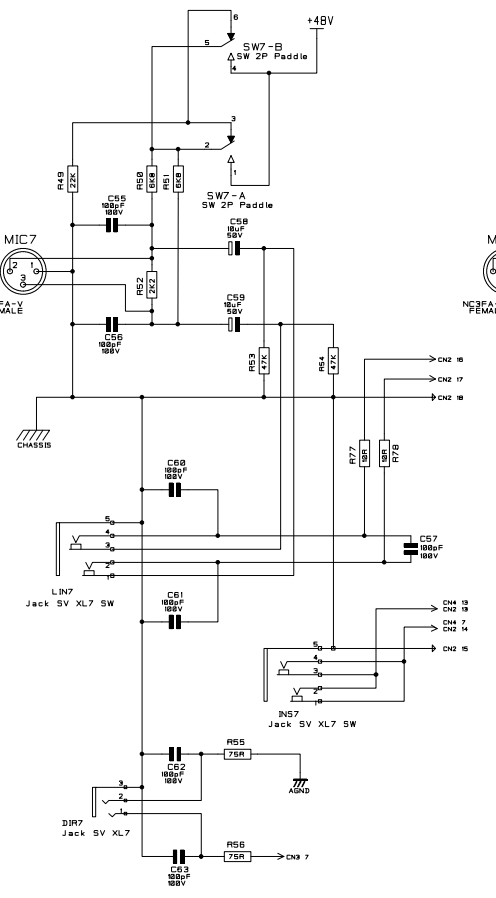
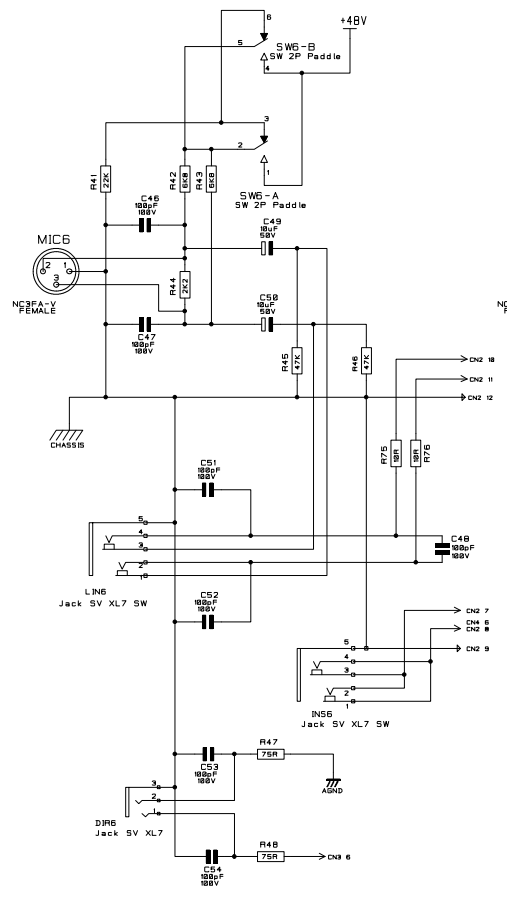
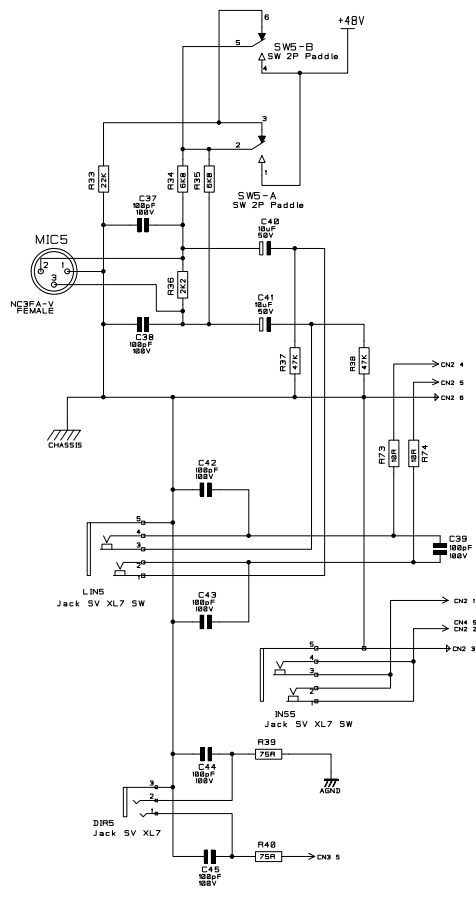
NOTES

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DATE 03-12-98

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TITLE  
SPIRIT PRO  
REARCONN BOARD

DRG NO. ED4024



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