THE URSA MAJOR 323

SERVICE MANUAL

URSA MAJOR StarGate 323
SERVICE MANUAL
MARCH 1984

REV - 0
PART # 0879
PRICE: $25.00

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PROPRIETARY TECHNOLOGY

This service manual is made available only for use by authorized, registered owners of the StarGate 323. Its contents are not to be copied, and use of this information in the manufacture of competing devices will result in prompt legal action. Service manuals are only available from the factory, not from dealers. Refer to the StarGate Owner's Manual for additional invaluable information.

IMPORTANT SAFETY NOTICE

THERE ARE HAZARDOUS VOLTAGES PRESENT IN THE StarGate 323 WHEN IT IS CONNECTED TO THE AC POWER LINE, EVEN WHEN THE POWER SWITCH IS "OFF". DO NOT DO ANY DISASSEMBLING, COMPONENT REMOVAL, OR PROBING INSIDE THE UNIT WHILE IT IS PLUGGED INTO THE AC POWER LINE.

ACKNOWLEDGEMENT

The StarGate 323 and its documentation, like any other product, is the work of more than one person. I would like to thank each of my co-workers for their help in making the 323 a reality. In particular, I would like to thank those who worked on this manual. These are: Cyd Weiner, who spent many laborious hours at an uncooperative word processor (which had a propensity for eating words rather than processing them!), and David Drolette, our Chief Technician, who provided me with numerous opportunities and insights that helped check out the diagnostic procedures contained in this manual. Finally, I would like to thank Chris Moore, who conceived and managed the StarGate project.

Mark Bruckner

TABLE OF CONTENTS

I. GENERAL THEORY OF OPERATION

The StarGate 323 simulates both the reverberation produced in natural acoustic settings such as concert halls, and that produced by other simulators such as plates.

The StarGate 323 is designed around a 16K (16,384) word by 16 bit audio RAM array. This allows the StarGate to store 512 milliseconds (approximately 1/2 second) of digitized audio. The StarGate simulates reverberation by writing the input audio into memory, and then reading it back after various delays. A total of 24 reads are done for every write operation.

The first read is for test purposes. The next 15 reads, called feedback taps, are combined together after reading and fed back to the input to be written back into the memory with the next audio input sample. The last 8 reads, called audition taps, are output to the left and right reverb output channels. By controlling the delays and gains of each reverb and audition tap, the StarGate produces reverberation as the incoming audio is cycled around through memory, subjected to different gains and delays.

All of the above read and write operations are performed by the StarGate 323 every machine frame. The machine frame, which is identical to the timing signal TCB7, occurs every 31.25 microseconds. TCB7 is divided up into 256 bit times of 122 nanoseconds. Figure I shows: the machine frame, TCB7, and the operations that are performed in each machine frame.

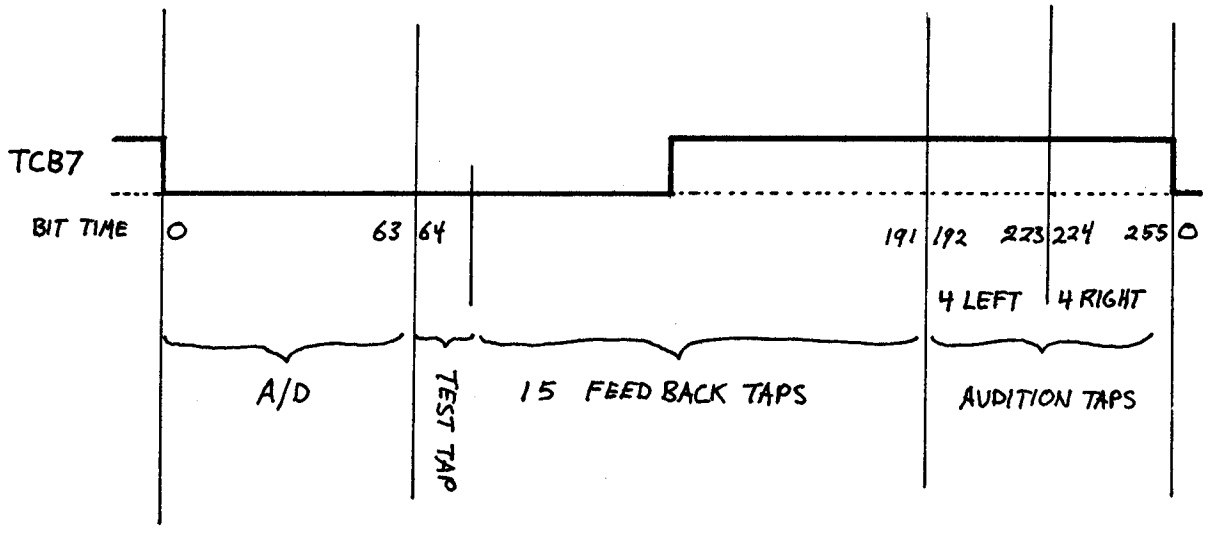

FIGURE I

During the first quarter of the machine frame (bit times 0 through 63) the machine digitizes the next audio input sample and stores it in memory. The next 2 quarters of the machine frame (bit times 64 through 191), are used to read and calculate the 15 feedback taps. As each feedback tap is determined, it is converted to an analog signal and fed back to the input of the machine where it is mixed with the incoming audio signal and written into memory in the next machine cycle.

During the last quarter of the machine cycle, (bit times 192 through 255), the left and right audition taps are determined. These taps, when converted to a left and right analog signal, become the reverb outputs of the StarGate. The left audition taps are read from memory during bit times 192 through 223 and the right audition taps are read from memroy during bit times 224 through 255. A total of 8 taps are read from memory, 4 for the left and 4 for the right.

The user can control all of the characteristics of reverberation with the front panel controls of the StarGate. LED displays allow him to monitor the settings of the machine at any given time. The major characteristics of the reverb are controlled by the 3 red knobs on the StarGate's front panel. These are: ROOM, PRE DELAY, and DECAY TIME.

The ROOM knob controls the type of room the reverberation is occurring in. Rooms 1 and 2 are small tight rooms good for percussion, while Rooms 7 and 8 represent large spaces with many discrete echoes good for synthesizers and "space effects". Rooms in between, such as Rooms 4 and 5, represent various sized halls good for piano and symphonic music.

The PRE DELAY knob controls the delay time that occurs before the first early reflections of the reverberation are heard. The Pre Delay can be set from 0 to 320 milliseconds.

The DECAY TIME knob controls the decay time of the reverb envelope. The Decay Time selected is the time it takes for the input signal to decay 60dB down from its original level. The StarGate controls the Decay Time by changing the gains of the 15 reverb feedback taps. Taps given larger gains linger over a longer period of time.

LF and HF Decay knobs: After the 15 reverb feedback taps are converted to analog they pass through a high and low frequency attenuator. These are controlled by the grey LF and HF Decay knobs on the front panel. By increasing the high frequency attenuation, the high frequencies die out more rapidly and are muffled. The LF Decay control modifies the low frequencies in much the same way. Both the LF and HF decay controls leave the midband portion of the reverberation unaltered. The machine has its full 15K bandwidth with the LF and HF controls both turned to their extreme clockwise position.

DIRECT and REVERB knobs: The StarGate also provides a direct path by which the incoming dry unreverbed sound can be mixed with the reverb output to produce a natural mix of dry and reverberant sound. The exact amount of each can be controlled by the dry DIRECT and REVERB mixing knobs on the StarGate's front panel.

All of the adjustments described in the paragraphs above are made in addition to the built-in delay algorithms of each room. The design enginers of URSA MAJOR have chosen each set of delays to approximate the reverberation range designated by the room number. As we have seen, the user can easily and intuitively change the reverberation characteristics within each room as well as change the nature of the sound by changing the room.

II. CIRCUIT OPERATION

The following is a description of the circuits in the StarGate and an explanation of how they operate. These descriptions refer frequently to the schematics in Appendix C and it would probably be helpful to refer to them as you are reading each section.

II.A. POWER SUPPLY

The power supplies for the StarGate are located in the rear section of MOM3. Schematics for the power supplies are shown on sheet 11 in the schematic section (Appendix C).

The incoming AC voltage is fed through Fuse F1 and both sides of the line are switched by the main power switch, S7, on the front panel. The voltage selector switch S8, located in the front right hand corner of MOM3 near the main power switch, can put the two transformers primary windings in parallel for 115V or in series for 230V operation.

Two different secondary windings are used to develop the three regulated power supplies and one unregulated power supply. One winding is used for the +5V power supply. This supply is regulated by an LM338 TO-3 regulator mounted on the back panel. This supply is also protected by a separate fuse, F1, located just after the recifier circuit. The other winding develops the +15 and -15 supplies which are used for the analog circuits. These regulator circuits function similiarly to the +5 supply.

The remaining unregulated voltage to come from the power supplies on MOM3 is the raw VCC voltage of approximately 10VDC. This supply voltage goes to the front panel board (PAN03) where it is used to light all of the LED's. This supply comes from the +5V supply circuits just before the 5V regulator.

There are no special troubleshooting techniques for the power supplies. If you suspect a problem, test the 3 voltages with a voltmeter. These are straight forward, 3-terminal voltage regulator supplies. AC voltages and critical unregulated DC voltages are indicated on the schematic.

II.B. TIMING GENERATION

The timing generation circuits are shown on schematic sheet 5. A crystal oscillator, U65, generates the 8.192 MHz clock signal. This signal is used to clock the timing counters U52 and U53. These two 4 bit synchronous counters produce eight timing counter bits known as TC0-TC7. These bits form a 256 bit time (BT) machine frame in which one A-D is performed, 15 reverb feedback taps are calculated and D-A'ed, and 8 audition taps are calculated and D-A'ed. This frame is repeated over and over again. The 8 timing counter bits, TC0-TC7, are used as address inputs to the timing PROM's U46 and U47. These PROM's produce 15 timing signals and one SYNC CLEAR pulse. These signals control most of the timing in the rest of the machine. Their outputs are only dependent on the state of the timing counters U52 and U53. The outputs of U47 and U46 are passed through latches U42 and U43 to remove any PROM address decoding glitches before the timing signals are sent to the rest of the machine.

TCB1 is derived from TC1 by U43 and U66 and is a delayed and inverted version of TC1. TCB1 is used as the primary digital clock that clocks the short pipelines in the address and gain sections of the StarGate (schematic sheets 2 and 3). TCB1 also clocks binary counters, U72 and U73, which produce the TCB timing signals TCB2-TCB7. Because these signals are clocked by TCB1, they are guaranteed not to change until TCB1 has occurred. This ensures that the results of calculations based on TCB2-TCB7 change only after TCB1 has stored the results. TCB1, TCB7 and the relationship between them are shown in Scope photo #29. TCB2 and TCB7 are shown in photo #30.

A SYNC CLEAR pulse, generated by timing PROM U47, occurs once every TCB7 and ensures that the TCB timing counters stay in sync with the TC timing counters that control the timing PROMs. This signal is shown in scope photo #28.

The signal TAPOFF, generated by U58 and U59, is used to disable the DACs (U20, U27, and U33) during the feedback taps, or the audition taps (or both). This is used to respectively implement: the REVERB CLEAR; the DRY ONLY; and the REVERB CLEAR and DRY ONLY modes. TAPOFF in these 3 modes (and in its inactive state with no override buttons pushed) is shown in scope photo #6. This photo shows TAPOFF at U58 pin 7. Note that TAPOFF is converted to a 7V high level after U54 pin 10 to ensure that the DACs are disabled.

II.C. ADS

The address and gain calculation section of the StarGate, called ADS, is located on schematic sheets 1, 2 and 3. These circuits determine the delays and gains of the various feedback and audition taps. The address section (located on sheet 3) calculates the write address for the A-D sample to be written into RAM; and for the remaining parts of the machine frame, calculates the delays to be added to the write address for the feedback and audition taps. These delays are obtained from EPROMs U79 and U69. They are then clocked into the delay data register (U62); added to the multiplexed write address by U63 and U70; and then sent to the RAM array in the memory section.

The write address itself is determined by counters U82 and U85 which are clocked by TCB7. The outputs of the write address counter are multiplexed by the row/column mux, (U74 and U80) before being sent to the delay adder.

Gains for the different time slots of the machine cycle (A-D sample, and the feedback and audition taps) are set by circuitry located on schematic sheets 1 and 2. This section of ADS sets the gains from data derived from EPROMs U76, U77 and U78. During the A-D part of the machine cycle the gain is set to 1, and during the feedback taps and the audition taps the gains are varied. The comparator and latched mux (U60, 61, 67 and 68) form a gain ceiling circuit that limits the detemined gains as the decay times knob is turned down resulting in decreased gain and less reverb.

II.D. MEMORY

The memory circuits are shown on sheet 6 of the schematics. The memory circuits are used to store the audio data and to assist in A/D conversion of the audio input. These circuits include: The SAR used to perform A/D operations, 4 octal transparent latches, and the 16K by 16 bit audio memory composed of four 16Kx4 DRAMS.

Just before the end of a machine frame, the A/D conversion for the next frame begins. This occurs when the SAR tests and sets the sign bit SN. At the beginning of the next machine frame, the SAR continues performing the coarse A/D operation. The SAR tests and sets each coarse bit starting with the MSB. During the coarse conversion octal latches U36 and U28 are transparent and U34 is tristated (forcing the inputs to U21 to be all 1's because of a pull of resistor network). At the end of the coarse conversion U36 is latches the contents of the SAR; the SAR is reset, and the fine conversion begins. During the fine conversion, octal latches U34 and U21 are transparent. The SAR then starts with the MSB of the fine bits and tests and sets each bit until the LSB is tested and set. The now fully tested 16 bit audio data word is ready to be written into the audio memory at the write address specified by the address circuitry. The row address, on the multiplexed address bus, is strobed in by the rising edge of RAS in the machine cycle at bit time (BT) 58. This occurs before the fine conversion is complete. The row address is stobed in by the first rising edge of CAS at BT 63. During the entire duration of the fine conversion the write control, W, of the RAMs is high.

When the rising edge of CAS occurs, the now completed audio data word present at the inputs of the RAMs is written into the RAMs. At bit time 64, the write enable W, controlled by LSBE, is taken away from the RAMs and the write operation is complete. After the write operation is complete, the SAR is reset at BT66 and is ready to begin the next A-D operation. For the rest of the machine frame, the RAM is only used to be read from. For each feedback, test, and audition tap one memory read is performed for a total of 24 reads. For each read operation, the row and column addresses are strobed in by RAS and CAS as described above for the write operation. During the read operation, octal latches U36 and U34 are tristated and octal latches U28 and U21 are clocked after each read by DACEN. This latches the tap data word, which was read one tap before it was needed, so that the data can be available to perform a D-A for the entire duration of the tap.

II.E. ADA

The analog to digital and digital to analog conversion circuits, labelled ADA, are located on schematic sheet 7. During the first quarter of the machine frame, the ADA circuits are used to perform analog to digital conversion on the new audio sample. During the next three quarters of the machine cycle, the ADA circuits perform digital to analog conversion on each of the test, feedback, and audition taps.

During A/D, the current audio sample is held by the sample and hold (U17). The hold period of the sample and hold is controlled by the low portion of ISHB signal. This is shown in Scope photo #27. The held audio sample output from the sample and hold then passes through Op Amp buffer U19 whose pot RV9 allows the addition of an offset voltage to the sample. This offset voltage is set to +20mV measured at U19 pin 1 with no audio input (see Scope photo #35). The output of U19 is then sent to pin 2 of the comparator, (U25). Pin 3 of the comparator is connected to analog ground through two 330 ohm resistors in series.

The output of the comparator, CMP, (U25 pin 7) is high or low depending on whether pin 2 or pin 3 is greater. Each time a comparison is made the result (CMP) is clocked into the SAR. As described in Section II.D., the sign bit is tested first, then B14 (MSB), then B13, continuing until B0 (LSB) is tested. When the SAR begins testing, the sign bit is set to zero and all of the remaining bits are set to 1. When the SAR is clocked, CMP is clocked into the SAR and becomes the sign bit and the next bit (B14) is set to zero. This new word is converted by the DACs (U20, U27 and U33) which send the result to the comparator. When the SAR is clocked again, the new result from the comparator becomes bit 14 and bit 13 is set low. This continues until bit 7 is reached where the 8 bit SAR must be reset before the fine conversion can be completed. When the SAR is reset all of the bits are set to 1's except for the MSB which is set to zero. More detail on switching between coarse and fine conversion is contained in Section II.D.

The DACs are current conversion DACs meaning that they sink current in proportion to their digital inputs. Depending on the sign of the audio sample, the Harris switch, U26, steers the DAC output to either draw current away from pin 2 or from pin 3 of the comparator. For positive audio samples, the Harris switch (U26) steers the DAC outputs so that the current flows from pin 2. As the SAR conversion process continues, the voltage of pin 2 converges to 0 as shown in Scope photo #1. When the voltage at pin 2 is 0, the analog value of the digital word being converted by the DACs is equal to that of the audio sample. For a negative audio sample, the switch U26 steers the DAC outputs so that they draw current from pin 3 of the comparator. As the SAR process continues, the analog value at pin 3 of the comparator generated by the DACs converges to be equal to the value of the audio sample of pin 2. This is shown in Scope photo #2.

During the D/A parts of the machine frame the Harris switch at U26 switches the DAC output to U32 instead of to the SAR comparator. The taps are D/A'd in the following order: the test tap, the 15 feedback taps, the 4 left audition taps, and the 4 right audition taps. This is shown in Scope photo #5 taken at the output of Op Amp U32. Again, as in A-D, the Harris switch sends the DAC output to either the inverting or non-inverting input of Op Amp U32 depending on whether the sign (SN) is positive or negative. The output of the Op Amp is then de-multiplexed by a second Harris switch at U31. This switch, which is controlled by ELB, ERB, ETB, and EFB (Scope photos #15-18), separates the serial stream of taps into the left output taps (LO), the right output taps (RO), the test tap (TO), and the feedback taps (FO). The control signals, ELB etc., are designed so that they open the switch during the second half of the tap-- after the analog output of the DACs in U32 have settled. The de-multiplexed outputs of the U31 Harris switch go to four Op Amp integrators, which time integrate the taps that compose each of the outputs. These integrators are built from two dual Op Amps U23 and U24.

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II.F. ANA

The ANA (analog) circuits are located on schematic sheets 8 and 9. These circuits consist of the left and right direct paths, the left and right reverb output paths and the reverb feedback path. The reverb feedback path is shown on Schematic Sheet 9 and the remaining ANA circuits are shown on Sheet 8.

ANA SHEET 8
The left and right audio input channels come into the StarGate through XLR's J1 and J2 and are received by both halves of the dual Op Amp U3. The input signal can be: pin 2 hot, pin 3 hot, or differential. The near unity gain outputs of U3 then go to both halves of the input level pot RV1 on the front panel and then to the Input Mute analog multiplexer at U2. The 4053 analog multiplexer switches the audio output from the Input Level pot on the front panel to ground through two 10K resistors when INMUTE is low. Otherwise it switches the audio signal to the inverting inputs of the dual Op Amps at U8. At this point the stereo outputs from U8 continue along the direct path (LDRY and RDRY) and also branch off (LI, RI) to be summed together to form one signal that is input to the reverb section of the StarGate, (see ANA, Sheet 9). Continuing with the direct path, (in the lower right hand corner of Schematic sheet 8) the left and right channels go to both halves of the direct mixing pot RV4 on the front panel. The left direct channel is then summed with the left reverb output and the right direct channel is summed with the right reverb channel. This is done with the 2 halves of dual Op Amp U16. The left output channel goes to the output driver U15 and then to the XLR output J4. U9 and J3 are respectively used for the right channel output. The output drivers, consisting of 2 Op Amps each, allow the user to receive his signal differentially or with pin 2 or pin 3 hot.

The two channels of the reverb output path, LO and RO, (coming from the Op Amp integrators at U23), each pass through a 15kHz elliptical low pass filter. The filter for the left channel is made from U4 and U10, and the filter for the right channel is constructed from U5 and U11. Both of these filters are identical in design and are located in the lower left hand corner of Schematic sheet 8. The outputs of these filters pass through a de-emphasis circuit (U10 for left and U11 for right) and are then sent to both halves of the reverb mixing pot RV5. From here the signals are summed with the direct path by U16 as described above.

ANA SHEET 9

The signals LI and RI, which branch off from the direct path after U8, are summed together by one Op Amp of U7 to produce a single channel input to the reverb system. Pre-emphasis is added to the signal and then the signal is mixed with the reverb feedback signal. This is done with the remaining Op Amps in U7. The result then goes to the front panel LF and HF attenuation pots RV2 and RV3. These pots form simple analog low and high pass filters which are each buffered by a unity gain Op Amp (U14). The equalized signal then passes through a 15kHz elliptical low pass filter which is identical to those in the reverb output paths. This filter is built from Op Amps U6 and U12. The output of the filter then passes through a non-inverting Op Amp (U12) with a gain of 2. The resulting signal, called AIN, goes to the ADA circuits (Schematic sheet 7) where it undergoes A/D conversion and is stored in memory.

The reverb feedback signal that is mixed with the incoming dry signal, described above, comes from FO. FO is sourced by Op Amp integrator in the ADA circuits and is the time integrated sum of the 15 feedback taps read from memory. (See Section II.E. above). FO passes through several fixed filters before it is mixed with the incoming direct signal. These filters are implemented with various R's and C's and the TL074 quad Op Amp at U13.

At the top of Schematic sheet 9 is located the Rate Level Analog circuits. These circuits and the Rate Level Circuits located on Schematic sheet 1 develop a DC level in proportion to the amplitude of the StarGate's input audio. The Rate Level circuit takes the audio just after LI and RI are summed together and presents them to a 370Hz Low Pass filter. This filter is constructed from one of the Op Amps in the quad TL074 at U30. The output of this filter is then passed through a 106Hz high pass filter constructed from another Op Amp in U30. The remaining 2 Op Amps in U30 are used to construct a full wave precision rectifier. The resulting band passed and rectified signal is called RATLVL and goes to the LM339 comparators on ADS (Schematic sheet 1).

II.G. DISPLAY

The display for the StarGate uses a multiplexed scan technique. Circuitry on MOM3 (Schematic sheet 4), determines the audio peak level (from digital audio level bits) and generates 8 multiplexed display data bits and 4 display mux control bits. PAN3 (Schematic sheet 10) receives the data bits, decodes the 4 display mux control bits, and steers current through the LED's using two current driver IC's.

II.G.1. OPERATION OF MOM3 DISPLAY LOGIC

The display logic on the MOM board is divided into two parts. These are: (1) the audio level peak hold circuit; and (2) the display mux control logic, display multiplexer, and display PROM circuits.

The audio peak hold circuit is centered around an 8 bit Peak Hold Latch (U56) which holds the current peak audio level. Updating of this latch is controlled by the Peak Update Logic (U48, U55, U96-U98), which consists of an 8 bit comparator, a one-shot, and three gates. The Peak Hold Latch is updated whenever the audio level increases or whenever the one shot (U98) times out indicating that the current level has been held for long enough (approximately 100 milliseconds). The COMPARE VALID pulse, (Photo #36), instructs the Peak Update Logic as to when the new audio level data is valid.

The overall operation of the scanned multiplexed display is controlled by the three write counter bits WC4, WC5, and WC6. These bits control which of the eight different areas of the front panel is to be displayed at any given time. The write counter bits cycle through the entire set of eight different display states every 4 milliseconds.

The Display Mux Control logic circuit controls which data is to be displayed during each of the display states. This circuitry consists of logic gates U95 and parts of U96 and U94. The circuit is controlled by UC4, WC5, and WC6 (which tells it the display state) and produces two display mux control bits BIT0 and BIT1. These bits (shown in Photos #37 and 38) form a 2 bit code that determines which data (ie: peak level, reverb decay, override switches, etc.) will be selected by the Display Multiplexer.

The Display Multiplexer is located in the middle of Schematic sheet 4 and consists of U90, U91 and U92. The data selected by the multiplexer goes to the Display PROM (U99) which does the necessary code conversions needed to determine which segments of the particular display group need to be illuminated. The output of the Display PROM becomes the 8 bit Display Data Word that goes to the front panel.

The signal DISPENB (shown in Photo #39) disables the display and the Display PROM during the transitions between each of the eight display states determined by WC4-WC6. This eliminates possible ghosting as the displays change from one illuminated group to the next. DISPENB is generated by U83 which has WC2 and WC3 as its inputs.

II.G.2. OPERATION OF PAN3

The front panel, PAN3, is shown on Sheet 10 of the schematics. The front panel operates from: the three write counter bits WC4-WC6 (which determine the display states), the DISPENB signal, and the eight multiplexed display data bits. The three write counter bits (labelled S0-S2 on the display schematic) along with DISPENB are decoded by U100 to produce eight non-overlapping common anode control signals. These negative true logic signals are then inverted by U101 and sent to U102, a non-inverting current driver, which directly drives the common anodes of the eight display groups. Note that because of the decoder at U100 only one display group is driven at one time. Note also the pooling of DI4 and D9-D11 as one display group.

The 8 bit multiplexed display data is received by U103, an inverting current sink driver, which sinks current coming from any of the eight display groups. Current is limited by resistors R101-R108. Note that resistors R109 and R110 ensure equal current flow through the two segments that are controlled by one display data bit (D7) on display DI4.

III. TROUBLESHOOTING, TESTING, AND CALIBRATION

III.A. Test and Troubleshooting Equipment

You will need, at a minimum, a good dual-trace scope (25MHz or, preferably, better), with an external trigger. Also useful would be a low-distortion audio oscillator, a distortion analyzer, an audio volt meter, and a DVM. Clip leads, and an 8 pin DIP switch would all be helpful.

A second StarGate working normally is, obviously, a valuable tool. The second unit can be used as a reference and as a source for a known working PAN3, which can be very helpful in isolating a display problem to the display board (PAN3) or to the MOM board.

III.B. Disassembling Instructions

DANGER: High voltage is present inside unit. Be sure to unplug and remove the line cord completely before beginning disassembly.

III.B.1. Removing top and bottom covers: The top and bottom covers of the StarGate are each held on by 11 screws. To remove either cover, remove the screws and then gently pry the cover free. After removing both covers, you will have access to both the component and etch sides of MOM3.

III.B.2. Removing soldered components with multiple leads: The circuit boards in the StarGate have plated-through holes. When removing a component, use a vacuum solder remover to completely remove the solder from the hole. Component leads should be free and should wiggle easily before you try to pull them from their holes. Since most of the IC's in the StarGate are socketed, there are very few components with multiple leads that should have to be removed during servicing. If the need arises, however, be very careful that all leads are free before you attempt to remove an entire component. If you are really stuck, try to get a pair of diagonal cutters between the component and the top side of the board, and cut the component free, one lead at a time. Do anything to avoid damaging the board.

III.B.3. Procedure for removing or replacing socketed IC's:
When replacing an IC or removing one from a socket, shut the power off to the StarGate. Failure to do so could damage the IC itself, or another IC associated with it, or even the power supply. IC's, especially the EPROMs, PROMs, and Harris 201 switches are highly susceptible to static electrical problems and should be kept in conductive material like tin foil until used.

When inserting an IC into a socket, be careful that all pins are straight, that they engage the correct hole on the socket, and that each lead seats properly. If undue force is needed to seat the IC in the socket, you are probably bending a lead over and not getting it into its hole. Use a real IC extractor to pull IC's straight out, and thus keep all the pins straight. An inspection or dental mirror will help you sight between the IC and socket to check for bent-over leads.

The following IC's are sorted parts and should only be replaced with URSA MAJOR provided parts: DAC 08's and Harris 201 switches.

III.C. CALIBRATION AND TOTAL HARMONIC DISTORTION

III.C.1. CALIBRATION

There is only one calibration that has to be made in the StarGate. This setting is made at the factory and its adjustment pot is sealed with "no tamper" paint. There should be no need to alter or change this adjustment. If however, there is any need to verify this calibration, the factory calibration procedure is outlined below.

To verify the DAC offset pot setting do the following:

(1) Disconnect any input signal from the 323 input XLR's

(2) Set the StarGate front panel as follows:
Input level: counter clockwise
Room = 1
Decay time = 0
Reverb clear: ON

(3) Place scope probe A on U19 pin 1
Set trace at main cross hair of scope when grounded.
Set scope to 20mV/div (2mV/div for X10 probe)

(4) Place scope probe B on the TCB7 test point
Set scope to 5V/div.
Trigger on channel B
Set scope to display 3.91 usec/div. Do this by setting controls to 2usec/div and going OFF CAL until the scope display looks like Scope Photo #35

(5) Calibration is correct when trace A measures exactly 20mV in the time interval just before the falling edge of TCB7. This is shown in Scope Photo #35

(6) If the calibration is incorrect, adjust pot RV9 (located near U20) until trace A looks exactly like that shown in Scope Photo #35.

III.C.2. TOTAL HARMONIC DISTORTION

The following describes how to measure the total harmonic distortion of the StarGate 323 direct and reverb paths:

Direct Path Total Harmonic Distortion (THD).

(1) Set up test equipment (audio oscillator and THD meter) as shown in figure III.C.2.

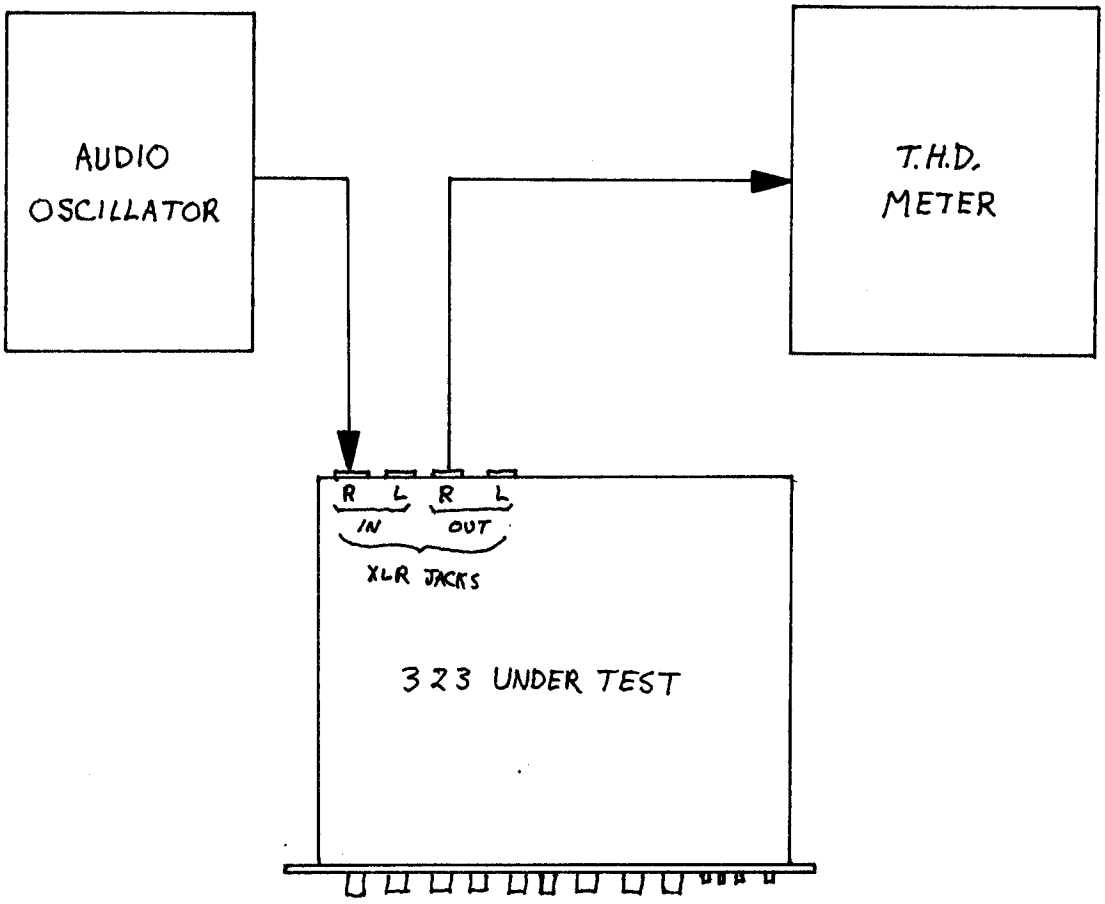
(2) Set up StarGate 323 front panel as follows:
Direct: counterclockwise
Reverb: counterclockwise
Adjust input level so that 0 limit LED is just barely off.

(3) Measure distortion on THD meter. For 400Hz audio, distortion should be less than -80dB.

(4) Repeat (3) except connect test equipment to the left inputs and outputs.

FIGURE III.C.2.

STARGATE 323 TOTAL HARMONIC DISTORTION MEASUREMENT



Reverb Path Total Harmonic Distortion.

(1) Remove the top cover as described in Section III.B.1.

(2) Set up test equipment as shown in Figure III.C.2.

(3) Set up StarGate 323 front panel as follows:
Direct: counterclockwise
Reverb: clockwise
Adjust input level so that O limit LED is just barely off.
Room = 1, Decay Time = 0.0

(4) Disable the reverb feedback path by grounding the junction between R74 and R90.
Switch test modes SW9, position 1, 2 and 4 to "on". If you do not have an 8 pin DIP switch, use jumpers to connect pins 1 to 8, 2 to 7, and 4 to 5 of SW9.

(5) Measure distortion on the THD meter. For 400Hz audio, distortion should be -65dB or better.

(6) Repeat distortion for the left reverb output by connecting the THD to the left output XLR of the StarGate. (You do not need to swap the inputs since they are summed before reverb processing begins).

III.D. TROUBLESHOOTING and TESTING PROCEDURES

III.D.1. Intermittent Problems: The most difficult problems to track down are those that are intermittent, that appear only when the unit is cold, only when the unit is hot, only when it is hit occasionally, or, seemingly, at random. You must be very patient with this kind of machine. If you are quite sure that it has been intermittent, then get it on the bench and try it out. If it seems to work normally, let it cool down, try again, heat it up, try it again, hit it, bang it, etc., until, however you manage to do it, you get the problem to appear and remain. Once the intermittent machine is actually operating in the failed mode, be very gentle with it so that you keep it broken until you find the problem.

If you haven't already, carefully remove the top cover and start probing around with the scope. It is hoped that when the machine is in the failure mode that listening to the machine will tell you something about where the problem is. As you proceed in normal troubleshooting from this point, be very, very careful that you don't disturb the machine into working normally again. Use the probe very gently to look for intermittent connectors, where a signal appears on one side of the connector and not on the other. Look for illegal logic levels, non-normal power supply voltages, etc.

III.D.2. Visual Check: Look in the unit for things like an IC that has come loose or fallen out. Look for something that is charred or burned. Look for a connector, such as a ribbon cable, that has jiggled loose. Look for a piece of wire or a solder blob lying down in the machine. Make sure none of the IC's have bent or broken legs.

III.D.3. General Strategies and Suggestions: When troubleshooting circuits in the StarGate, check the schematics carefully for signals that you can identify as logic control signals. These are the signals created by the circuits shown on sheet 5 of the schematics and the signals present on the corner pins of U26. If you are suspicious of a particular circuit, check the destinations of the signals that control the activity of that circuit and make sure you get traces that match the oscilloscope photographs in Section V. Always look at signals at their destinations, rather than at their sources. A further point in this regard is that finding a valid signal at the solder side

connection is not the same confirmation as finding a valid signal on the proper IC pin in its socket. Be sure that questionable signals have actually found their way down through sockets, along the etch in the PC board, and back up through the sockets to the ICs.

Only when you are confident that a malfunctioning circuit is receiving all the correct timing signals coming from the outside and all the proper power supply voltages should you start to probe more deeply.

III.D.4. Power Supply Check: Power supply circuitry is located at the back of the MOM3 board.

To check voltages with a Digital Multi-Meter:

(1) Attach common lead of DMM to ground.

(2) Test the various power supply voltages using the test points and spec voltages given the table.

Voltage	Measuring Point at rear of MOM3	Spec Voltages
+5	trace labelled +5V near J7	+4.75V to +5.25V
+15	trace labelled +15 near XLR's	+14.25V to +15.75V
-15	trace labelled -15 near XLR's	-14.25V to -15.75V

III.D.5. Test Functions at MOM3 SW9: The StarGate 323 has 4 built-in special test functions that aid in de-bugging and working on circuit problems. These are accessed by inserting jumpers across the pins of the empty SW9 socket located on MOM3 near U79. The most convenient way to use this feature is to insert a mini-DIP 8-pin switch in the socket at SW9. If you can't do that you can activate the switches by inserting a small piece of jumper wire.

Here is a brief description of the function of each of the test positions:

MOD DIS: To activate the Modulation Disable (MOD DIS) mode insert a jumper across pin 1 and 8 of SW9. When this mode is enacted the Modulation Counter on Schematic sheet 2 is cleared and all of the background randomization of the machine stops. This séverely modifies the function of the StarGate 323 and as such it no longer acts as a reverberator. This test mode is most useful when you also have the junction of R74 and R90 shorted to ground with a jumper. Without this jumper the machine will go into oscillation. This test mode will allow the trouble-shooter to look at LO, RO, FO and TO without them being modified by the machine's background randomization process. If LO, RO, etc look okay with modulation disabled but not with the machine operating normally, then the modulation circuits or the circuits controlled by them are suspect.

Z DELAY: The Zero Delay (Z Delay) test mode is enabled by shorting pins 2 and 7 of the SW9 socket. This function clears the Delay Data Register and prevents any tap delays from being added to the write address. This function can be useful for isolating suspected arithmetic read errors. If clicking or gross distortion caused by these errors goes away when this test mode is enabled, then the Delay Circuits on Schematic sheet 2 should be suspected. This test mode does prevent the StarGate 323 from operating normally as a reverberator.

WC DIS: The write counter disable test mode is enabled by shorting pins 3 and 6 of the SW9 socket. This test function clears the write address counter so that every ADC sample is written to highest address (16,383) of the RAM. This test mode also disables the front panel display because the display logic uses the write counter bits to operate from. Enabling this test mode also inhibits the StarGate 323 from operating as a reverberator.

SIGN DIS: The Sign Disable test mode is enabled by jumpering pins 4 and 5 of SW9 test socket. This test mode disables the GSN latch on Schematic sheet 6 (MEM) and prevents the Gain PROM (on Schematic sheet 2) from changing the signs of the feedback and audition taps. This test mode is most useful when used in conjunction with MOD DIS and Z DELAY for measuring the distortion of the reverb paths. This is how it is done at the factory.

III.D.6. TROUBLE-SHOOTING

Steady state audio problems as well as intermittent problems which introduce pops, clicks, or distortion into the output signal can be diagnosed using the following test procedure. To use this procedure set up the StarGate as follows:

(1) Remove the top and bottom covers.

(2) Connect an oscilloscope probe to the TCB7 test point. TCB7 will be used to synchronize the scope.

(3) Mate that probe to the scope's B input (or to the scope's external sync input if you prefer).

(4) Set the scope's B channel to 5V/div. actual and set the time scale to 2usec/div. Adjust the B channel when grounded to be on the first horizontal cross hair above the bottom of the scope display.

(5) Referring to the bottom trace of Scope Photo #1 in Section VI, set the scope to trigger on the falling edge of TCB7 and adjust the scope's X position knob so that this occurs at the very first vertical hairline on the left of the scope display. Now adjust the OFF CAL knob of the scope until the next falling edge of TCB7 is aligned exactly with the 8th centimeter of the scope display. The scope is now calibrated to 3.91 usec/div. The traces you see with probe A should match the photos in this manual.

(6) Connect an audio oscillator to either of the input XLR's of the StarGate 323 and adjust its frequency and level for an input level display on the front panel of greater than -3dB and less than 0dB. The frequency should be down around 40-100Hz.

(7) Connect a stereo monitor to the StarGate 323 output XLR's so that you can listen to the output.

(8) For most diagnostic tests that you will want to perform on the StarGate 323, the following front panel settings will be used:

LF Decay and HF Decay: clockwise
ROOM = 1
PRE DELAY = 0.0
DECAY TIME = 2.0 sec
Override switches: OFF

NOTE: Some of the following tests require the junction of R74 and R90 to be shorted to ground with a clip lead jumper. This is used to prevent the reverb outputs from feeding back to the inputs and disturbing the test results. It is important to remember to remove this jumper after each test.

You are now set up to do most basic tests needed to diagnose the StarGate 323. First, determine whether the problem exists in the direct path, the reverb path, or both. To do this first listen to the StarGate with the direct mixing POT on the front panel turned completely up (clockwise) and the reverb POT turned all the way down. Then listen with the direct turned off and the reverb turned all the way up. The direct path should produce a clean low frequency steady tone from the audio monitor. The reverb path, operating normally, should produce a low frequency wavering "tremolo" sound. You should not hear any clicks, pops, higher pitched tones, or distortion.

If your machine wakes up in different states each time it is turned on, then proceed to Section III.D.6.f. paragraph (a). Otherwise continue.

If an audio problem is only heard when listening to the direct path then continue with this paragraph, otherwise go to the next paragraph. This audio problem is limited to the top half and lower right quarter of the ANA circuits on Schematic sheet 8. These are straight forward audio Op Amp analog circuits and do not require the test set up described earlier in this section. Note that because this circuitry is shared with the reverb path, the problem will most likely be heard in the reverb path also.

If an audio problem is only heard in the reverb path, (Reverb pot clockwise, Direct pot counterclockwise) then the problem cannot exist in the direct path circuits described in the paragraph above. A reverb audio path problem can be caused by a variety of problems in a variety of places. The best way to attack reverb path problems is to minimize the possible areas that can be causing it. This is the approach that the procedures in the following sections use.

III.D.6.a. AIN

An easy area to check first for reverb path problems is AIN. This will allow the trouble-shooter to verify most of the analog circuits on Schematic sheet 9. This allows him to prove that the circuits leading up to AIN (the beginning of the 323 digital circuits) are working. The AIN test point is located at pin 4 of J12 test socket. To be sure AIN is unperturbed by the reverb feedback output (FO), the reverb feedback loop must be disabled. This is done by shorting the junction of R74 and R90 to ground with a clip lead or by pushing in the REVERB CLEAR switch. When looking at AIN use scope probe A and trigger on A. Look for distortion, clipping, or oscillation. If everything looks okay then proceed to the next section. If any of these problems exist, trace back through the circuit until the problem disappears and then look in the area you checked just before the problem disappeared.

III.D.6.b. VGAIN

After checking AIN, the next best place to look is VGAIN. Checking VGAIN will verify all of Schematic sheet 2 and the U40 DAC on sheet 7. The VGAIN test point is located to the left of U40 on the MOM board. It is labelled "TP3 VGAIN". Connect scope probe A to VGAIN and trigger on channel B (TCB7) as described at the beginning of the trouble-shooting section. Look at VGAIN and verify that it looks exactly like VGAIN shown in Scope photo #11. Verify that the first two centimeters of the scope display are identical to the photo; verify that the feedback taps (centimeters 3 through 6) go all the way to zero gain at the top of the photo and that they move up and down completely and uniformly without jumping or skipping; verify that the audition taps (centimeters 7 and 8) look exactly as shown in the photograph. If everything

looks OK, then proceed to the next section. If areas of each feedback tap are missing or they are skipping or jumping check to see if some of the modulation bits (labelled MC on Schematic sheet 2) are missing or shorted together. If VGAIN looks as though it's frozen in some weird state with no feedback tap movement at all, then check the Modulation Counter U87 and U88 on Schematic sheet 2. If VGAIN is missing altogether or looks distorted, look at the DACs on Schematic sheet 7, especially the DAC at U40.

III.D.6.c. ANALOG TO DIGITAL CONVERSION

Proceeding further into the machine, the next thing to verify is the analog to digital conversion process. The best way to verify whether the A-D process is functioning is to look at pins 2 and 3 of the comparator. Trigger on channel B with TCB7 as described at the beginning of the trouble-shooting section. Also, short the junction of R74 and R90 to ground with a jumper. Look at pin 2 of the CMP05 (U25) with probe A. Pin 2 of the CMP05 should look identical to Scope Photo #1. Now look at pin 3 of the comparator, this should look identical to Scope Photo #2. If everything looks ok, then proceed to the next section (III.D.6.d.). If either pin does not show the correct trace then look at the following:

SAMPLE AND HOLD: look at pin 5 of U17, an LF398 sample and hold. Verify that the signal looks like a properly sampled audio waveform--that is a sine wave made up of small flat stairsteps with slewing in between the steps. If pin 5 is not OK then verify the timing signal ISHB, (Scope photo #27). If ISHB is OK then verify the input to U17 at pin 3. This is the same point as AIN. If OK, then replace U17.

SAR BITS: Look at the input bits to the two coarse DAC's, U27 and U33. Starting with B14, look to see that each bit is initially set high at the left of the scope display then tested low (by the SAR), and finally set both high and low. Make sure that the peak LED on the front panel is just barely off. Each bit will be tested and set succeedingly further and further to the right. The input bits for U27 and U33 should be identical.

TIMING SIGNALS: If problems are still encountered, check the timing signals S and SARCK on U41, the SAR. These are shown in Scope Photos #19 and #20. Also check MSBE (Photo #14), LSBE (Photo #13), DAC and DAC (Photo #23), and DACEN (Photo #24). As a final resort check the inputs and outputs of the latches U21, 28, 34 and 36; and on sheet 7 of the schematics for floating or shorted signals, check the timing signals EP, EN, DP, and DN.

III.D.6.d. LO, RO, FO and TO TEST POINTS:
After checking VGAIN and the A-D, look at LO, RO, FO and TO. This will allow the trouble-shooter to check the remaining circuits on Schematic sheet 7 (ADA). This test will also give the trouble-shooter some idea that the address circuits on ADS Schematic sheet 3 are functioning normally. The LO, RO, FO and TO test points are located at the J12 test socket. The exact locations of the test points in the socket are indicated in the J12 diagram in the upper right hand corner of Schematic sheet 7. To look at the test points, trigger the scope on channel B using TCB7 as described at the beginning of the trouble-shooting section. Also jumper the junction of R74 and R90 to ground. Now look at LO (J12 pin 8) and verify that it looks similiar to Scope Photo #7. Do the same for RO, TO and FO. These are shown in Scope Photos #8 through #10. Check for distortion and uneven shading. For FO, verify that all of the taps are moving in response to modulation. If everything is OK then proceed to the next section.

If any one of the four test points does not look right and the others do, then check the U31 Harris switch timing signals. These are ELB, ERB, ETB, and EFB and are shown in Scope Photos #15 through #18. Also check the Op Amps U23 and U24. If these are OK, or your problem is that all of the LO, RO, FO, and TO test points are there but look distorted or unevenly shaded, then check pin 6 of the 5534 at U32. This signal should look like Scope Photo #5. Check to make sure the feedback taps (centimeters 2 through 6) are moving up and down and that the audition taps (centimeters 7 and 8), are identical to the photo. The first two centimeters should be at ground as shown in the photo. Check that the shading is similiar to that shown in the photo and that there are no unshaded holes or skipping in any of the taps. Also check that the positive and negative limits of each tap are uniformly centered in respect to ground.

If U32 pin 6 still does not look right and the circuits you checked in the A-D section appear to be operating correctly, then check the fine DAC. The fine DAC is located at U20. Observe the output at pin 4 and compare it to Scope Photo #3. Verify that the fine half of the SAR process is occurring in the second centimeter of the scope display and that the first centimeter is relatively quiet. For clarity, the feedback taps can be disabled by pushing REVERB CLEAR on the front panel. This is shown in Scope Photo #4.

If all of the above does not help, then continue to the next section where the address logic will be investigated.

III.D.6.e. ADDRESS LOGIC

If the StarGate output appears to be grossly distorted; or LO, RO and FO did not look normal and the problem could not be found in the above sections; then the address logic of the machine should be investigated. If LO and RO look OK but the output is slightly distorted or has frequency response problems then go to section III.D.6.f. (OTHER AREAS) paragraph c. The Address Logic, (ADS), is located on sheet 3 of the schematics. There is no simple test or test point that can be used to verify the functioning of these circuits. The best way to check these circuits is to check the timing signals and then all of the inputs and outputs of all the chips on sheet 3. (That's why the writer of this manual had you check everything else first!). Starting with the timing signals, check: TCB7A, MODB, MOD, TCB1, TCB2, and RAS. These, or their complements, are shown in the scope photos in Section IV. Next check the inputs and outputs of all the chips looking for shorts, illegal logic states, or grounded signals. It can sometimes be helpful to enact the Zero Delay (Z Delay) or the Modulation Disable (MOD DIS) test modes. To use these test modes see Section III.D.5. If the problem seems to go away when either test mode is enabled, then check the section of circuitry that is disabled by the test mode. Before checking that circuitry, turn the test mode back off, so that the circuitry under question can now operate.

III.D.6.f. OTHER AREAS

If you are still having problems then check the following remaining areas:

(a) TIM (Schematic sheet 5). Verify that the SYNC CLEAR pulse (Scope Photo #28) reaches pin 1 of both U72 and U73. Also verify that TCB7 is always delayed from TC7 by approximately 122 nanoseconds.

(b) ADS + MEM (sheets 2 and 5). Verify that the GSN and INVERT SIGN signals assume legal logic levels and are not grounded, or stuck high, or shorted to some other signal.

(c) ANA (sheet 8). Check the low pass filter and de-emphasis circuits at the outputs of LO and RO. To check the left channel look at U10 pin 8 and then at U10 pin 14. To check the right channel look at U11 pin 8 and then U11 pin 14.

(d) ANA (sheet 9). Verify the reverb fixed EQ circuits. Do this by first shorting the junction of R74 and R90 to ground to break the reverb feedback loop. Then look to see whether you can trace FO along through the circuit to R90.

III.D.7. TROUBLE-SHOOTING NON AUDIO PROBLEMS

This section describes how to trouble-shoot problems with the override switches and the display. For some of the following diagnostic tests you will need the test set up described at the beginning of Section III.D.6. (You will however, not need the distortion meter!)

III.D.7.a. OVERRIDE SWTICHES

If the REVERB CLEAR or DRY ONLY override switches fail to work, look at the TAPOFF signal (Scope Photo #6) and see if the waveform takes on all of the states indicated. Also look at the destination of this signal at the DACs and see if TAPOFF reaches a full high level of +7.5 volts. This is essential to turn off the DACs. If INPUT MUTE fails to work check the INMUTE signal at U2, check its power supplies or try swapping the chip if you have a spare.

III.D.7.b. DISPLAY

If you are having problems with the display and the StarGate 323 otherwise functions normally, then proceed to the next paragraph. If the StarGate does not otherwise function normally, then it is best to check the write counters on Schematic sheet 3 first before checking the display circuits themselves. This is especially true if the display is completely blank or appears to be jammed to display only a small part of the display. If the write counters appear to be functioning, especially write counter bits WC2 through WC6, then proceed to the next paragraph.

If the StarGate 323 otherwise functions normally then the problem is located in either: the display board itself (PAN03), the jumper (J10) to the display board, or in the display logic on Schematic sheet 4. First check to see that the display board is getting all of its voltages and grounds. This is especially important to check if the display is completely blank. The voltages to check are: +5V, Raw Vcc (+10VDC), digital ground, and Raw Vcc Ground (DISPGND). If these are ok, and if you have a second working StarGate 323 you may want to swap the display boards and verify whether the problem exists in the display board or in the display logic circuitry on the MOM board. If the problem is in the display logic circuits on MOM, or you don't know, then check the Display Mux and Display Mux Control circuits on Schematic sheet 4. Scope Photos #37, #38 and #39 should help you when checking the Display Mux Control Logic. Note that these scope photos use WC6 as a scope trigger. WC6 can be found at U95 pin 1 on the MOM board.

III.D.7.c. JAMMED PEAK LEVEL DISPLAY

If the reverberator does not otherwise function normally and possibly sounds as if it is oscillating then the problem is most likely located in the MEM, ADA, ANA or ADS sections of the StarGate (see the beginning of this diagnostic section). If the StarGate otherwise functions normally and the audio outputs respond to changes of the input level pot on the front panel, then the trouble-shooter should direct his attention to the Peak Update Logic on sheet 4 of the schematics. When checking the Peak Update Logic circuits first check the COMPARE VALID pulse used to clock the peak hold circuits. This is shown in Scope Photo #36. Then check the one-shot (U98), the comparator outputs (U48 and U55), and the Peak Hold Latch (U56).

III.E. SPARE PARTS

III.E.1. OBTAINING REPLACEMENT PARTS FROM THE FACTORY: Most of the components in the StarGate 323 should be locally obtainable. In addition, some dealers, especially overseas dealers, will have purchased spare parts kits from URSA MAJOR and should have even the hard-to-find parts on hand. If your dealer doesn't have a part, and you wish to buy parts directly from the factory, please be sure to furnish the following information: the serial number of your machine; the module and revision number on which the component appears (MOM3 or PAN3); a complete description (including part number) of the defective part, and, if possible, the proper URSA MAJOR part number from the parts list (Appendix B). It would also be helpful to us if you would describe any peculiar circumstances attendant with the failure. We would like to be able to detect any emerging failure pattern in the field, so that we may respond to it with a change in design or choice of parts in future units.

III.E.2. EMERGENCY SUBSTITUTIONS: Some possibilities for emergency substitutions may be easy for you to obtain locally. Most of the logic IC's are from the 74LS series. They can be replaced with military versions (54LS), with equivalent LS versions from other manufacturers, and, in some cases, with conventional 7400 series IC's. For example, a 74LS163 could probably be temporarily replaced with a 74163. The DAC08s used in the StarGate are sorted parts and replacements can only be obtained from URSA MAJOR. The HI201HS analog switch (U26 and U31) is sole sourced by Harris and can only be replaced by that part. The 64K DRAMs (U22, 29, 35 and 37) can be replaced with any of the TI, INMOS, or Fujitsu parts indicated in NOTE 1 on sheet 6 of the schematics.

III.E.3. PASSIVE COMPONENTS: With regard to the passive components, any of the resistors in the StarGate could be obtained locally. A single in-line resistor network, such as those found on MOM3 can even be replaced with discrete resistors, if care is used in soldering an assembly of 1/4 watt resistors together. Bypass capacitors are completely non-critical; the many 0.02's and 0.1's sprinkled around the machine can be replaced with an equivalent part. This is also true for the 4.7uF and 22uF tantalum capacitors. In most instances, the bypassing is conservative enough so that if the capacitor were to fail, it could simply be removed.

IV. SCOPE PHOTOGRAPHS

Key to Scope Photographs

1. Test conditions required for each Scope Photograph are listed to the right of each photo. Any test condition not required for a particular photo has been deleted. For example, if the input frequency is irrevelant, that heading will not appear in the caption.

2. A "Standard" front panel setting is as follows:

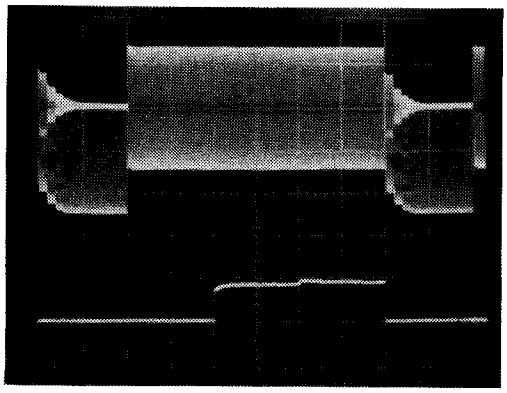
Room = 1
Pre Delay = 0.0
Decay Time = 2.0
Override switches: OFF
LF, HF, Direct and Reverb: clockwise
Input Level: adjust as required to get peak level.

3. LOCATION OF THE SCOPE SYNC SIGNALS.

TCB7: TCB7 can be found at TP1 located between U88 and U89. This signal is used as a scope sync in most of the Scope Photos. This signal is always used with an OFF CAL scope setting. To set the OFF CAL scope setting set the scope to 2usec/div., trigger on the falling edge of TCB7 and adjust the scope's OFF CAL knob until TCB7 looks as is shown in the photos, that is, with the next falling edge of TCB7 falling exactly at division 8 on the scope screen.

MC5: MC5 can be found at J13 located to the right of U77. MC5 is on the left most pin of J13 as indicated by the silkscreen. Remember to set the scope back to ON CAL when using this signal.

WC6: WC6 can be found at U95 pin 1. Remember to set the scope back to ON CAL when using this signal.



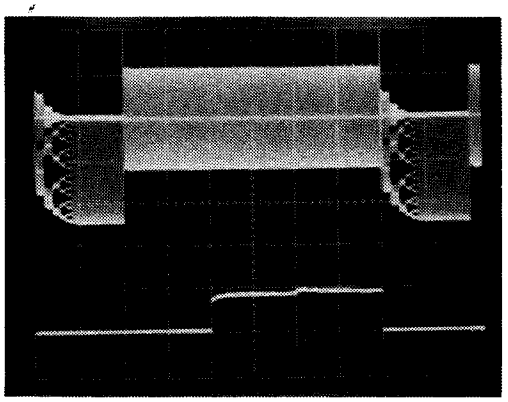
#1 COMPARATOR PIN 2 INPUT

TOP TRACE: Comparator pin 2 (CMP Ø5)
U25 - pin 2
2V/div

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENT: 100Hz audio input with level display just below peak.



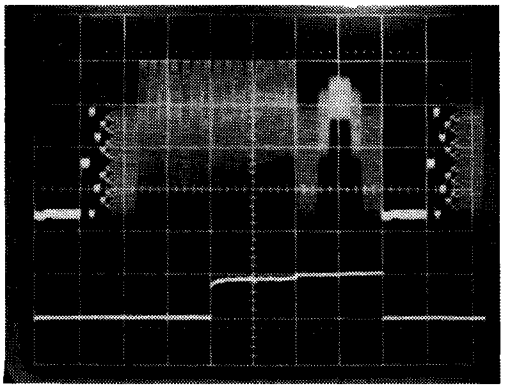
#2 COMPARATOR PIN 3 INPUT

TOP TRACE: Comparator pin 3 (CMP Ø5)
U25 - pin 3
2V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div (OFF CAL)

COMMENT: 100Hz audio input with level display just below peak.



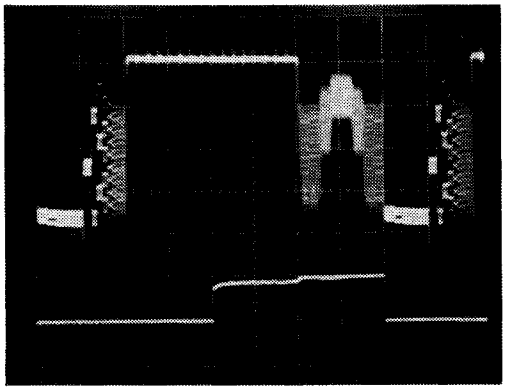
#3 FINE DAC WITH FEEDBACK TAPS

TOP TRACE: Fine DAC
U20 - pin 4
.5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENT: 100Hz audio input with level display just below peak.
ROOM 1, Decay Time = 2.0



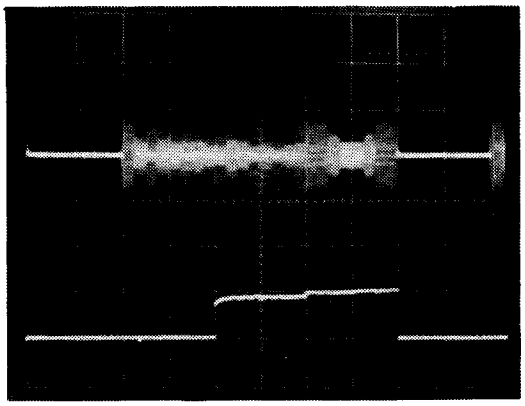
#4 FINE DAC (without feedback taps)

TOP TRACE: Fine DAC
U20 - pin 4
.5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENT: 100Hz audio input with level display just below peak.
REVERB CLEAR: ON
ROOM 1, Decay Time = 2.0



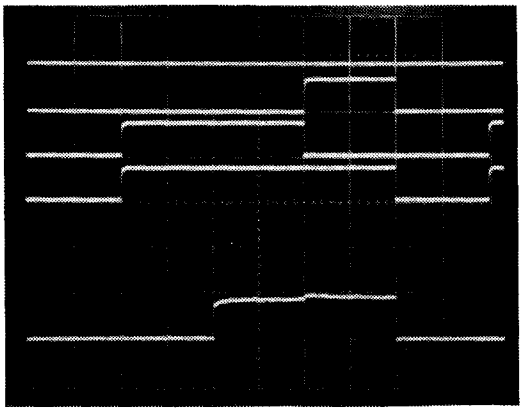
#5 U32 PIN 6

TOP TRACE: U32 pin 6
.5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENTS: 100Hz audio input with level display just below peak.
ROOM 1, Decay Time = 2.0



#6 TAPOFF

TRACE 1: TAPOFF with DRY ONLY and REVERB CLEAR off.

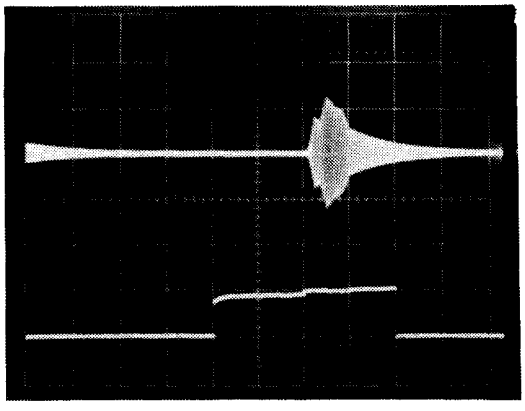
TRACE 2: TAPOFF with DRY ONLY on.

TRACE 3: TAPOFF with REVERB CLEAR on.

TRACE 4: TAPOFF with DRY ONLY and REVERB CLEAR on.

TRIGGER TRACE: TCB7

SCOPE SETTING: 3.91 µsec/div.(OFF CAL)
All traces are 5V/div.



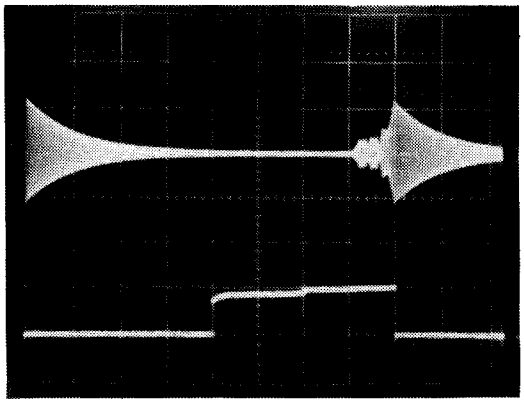
#7 LO LEFT AUDITION TAPS

TOP TRACE: LO, J12 pin 8
2V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENTS: 100Hz audio with level display just below peak.
ROOM 1, Decay Time = 0.0



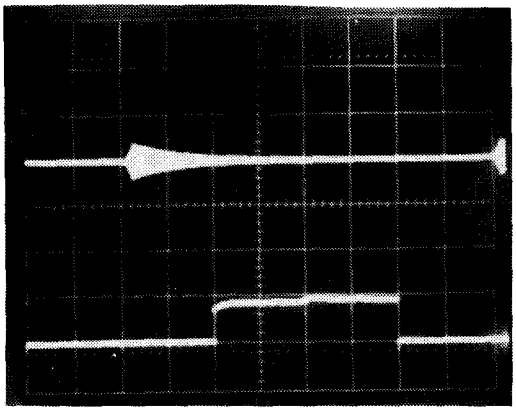
#8 RO RIGHT AUDITION TAPS

TOP TRACE: RO, J12 pin 7
2V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

COMMENTS: 100Hz audio with level display just below peaking
ROOM 1, Decay Time = 0.0



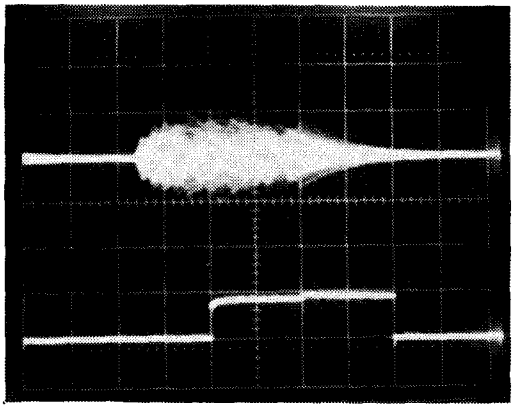
#9 TO TEST TAP

TOP TRACE: TO, J12 pin 6
2V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

COMMENTS: 100Hz audio with level display just below peak.
ROOM 1, Decay Time = 0.0



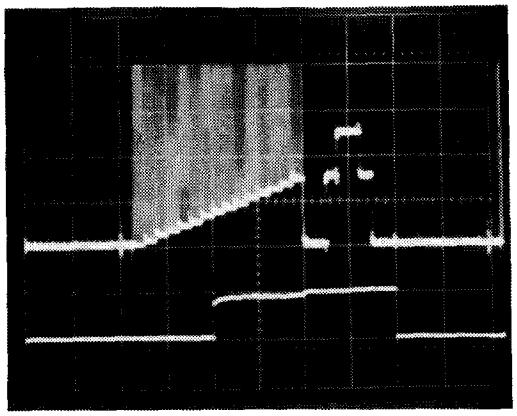
#10 FO FEEDBACK TAPS

TOP TRACE: FO, J12 pin 5
2V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

COMMENTS: 100Hz audio with level display just below peak.
ROOM 1, Decay Time = 2.0



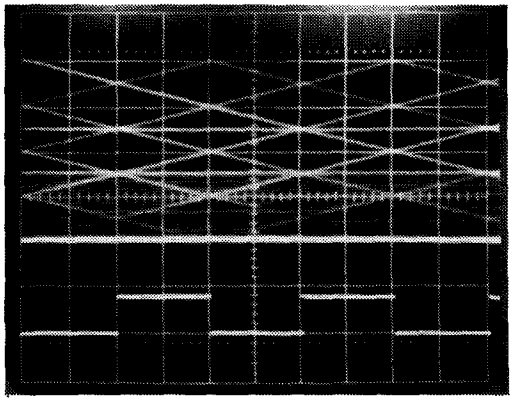
#11 VGAIN

TOP TRACE: VGAIN TP3
200mV/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

COMMENTS: ROOM 1, Decay Time = 2.0



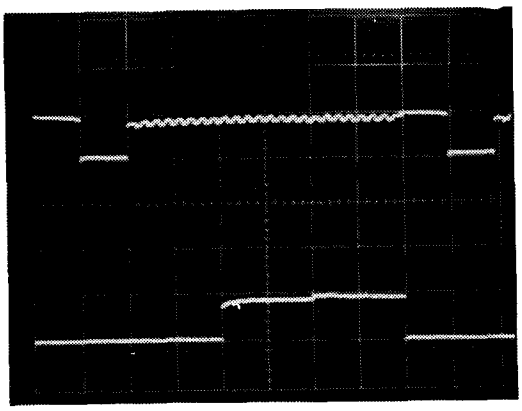
#12 VGAIN WITH MC5 SYNC

TOP TRACE: VGAIN TP3
200mV/div.

TRIGGER TRACE: MC5 5V/div.

SCOPE SETTING: 2ms/div ON CAL

COMMENTS: ROOM 1, Decay Time = 2.0

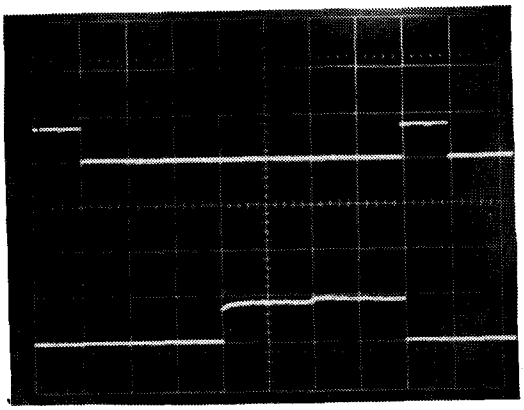


#13 $\overline{\text{LSBE}}$

TOP TRACE: $\overline{\text{LSBE}}$, U34 pin 1
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

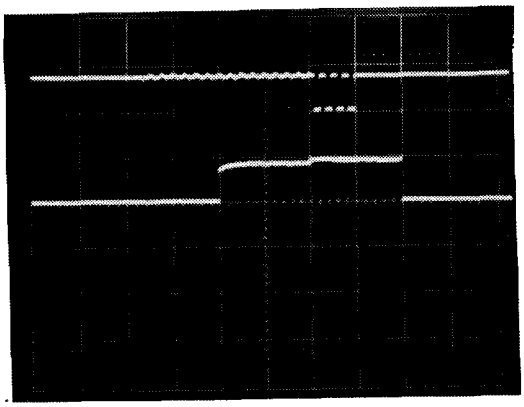


#14 MSBE

TOP TRACE: MSBE, U36 pin 11
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

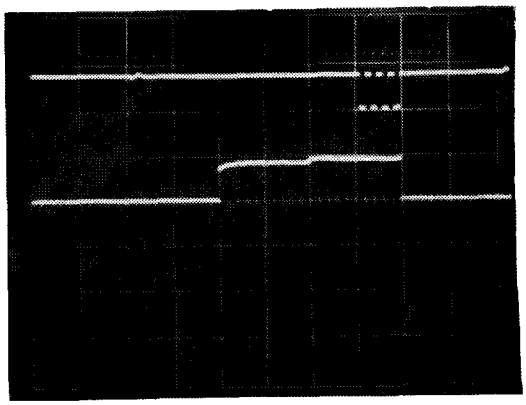


#15 $\overline{\text{ELB}}$

TOP TRACE: $\overline{\text{ELB}}$, U31 pin 1
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 usec/div. (OFF CAL)

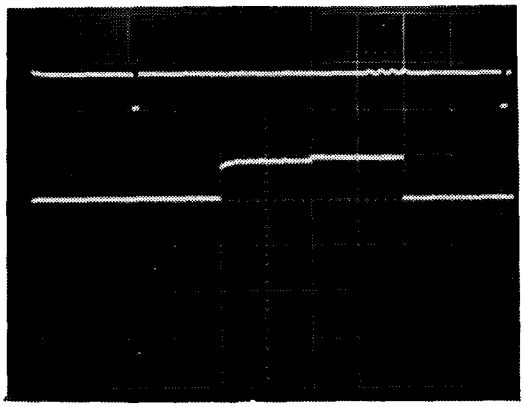


#16 $\overline{\text{ERB}}$

TOP TRACE: ERB, U31 pin 8
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

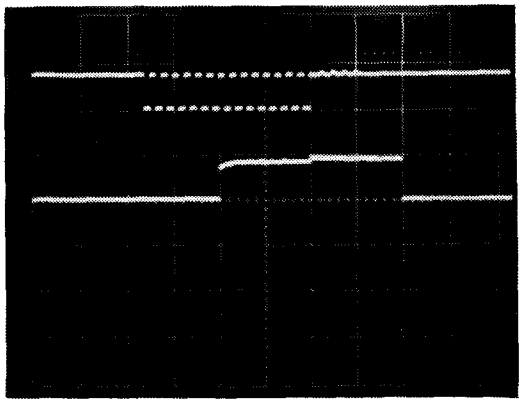


#17 $\overline{ETB}$

TOP TRACE: $\overline{ETB}$, U31 pin 9
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 usec/div. (OFF CAL)

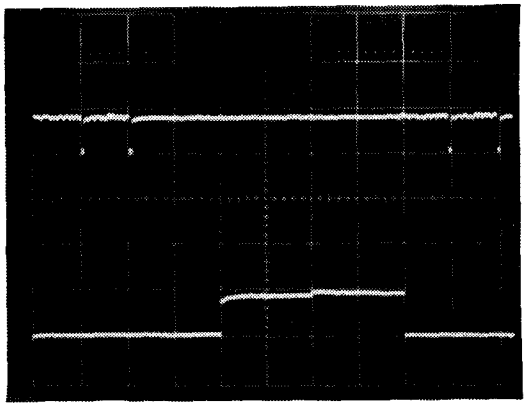


#18 $\overline{EFB}$

TOP TRACE: $\overline{EFB}$, U31 pin 16
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 usec/div. (OFF CAL)

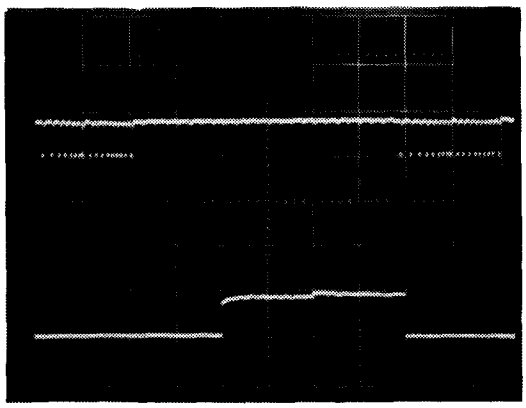


#19 $\overline{S}$

TOP TRACE: $\overline{S}$, U41 pin 10
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

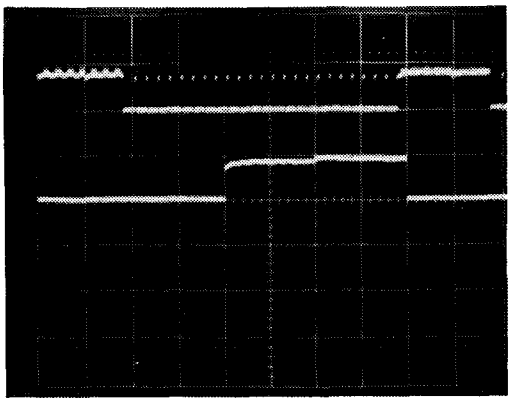


#20 SARCK

TOP TRACE: SARCK, U41 pin 9
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

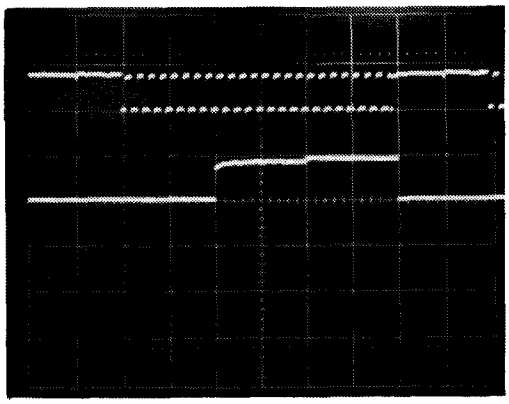


#21 $\overline{RAS}$

TOP TRACE: $\overline{RAS}$, U22 pin 5
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

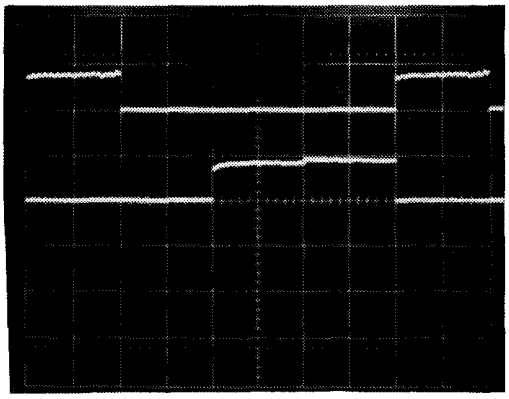


#22 $\overline{CAS}$

TOP TRACE: $\overline{CAS}$, U22 pin 16
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

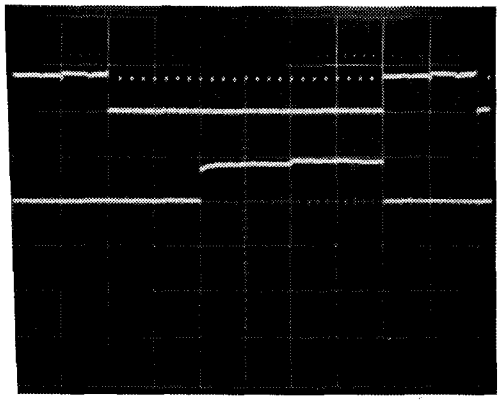


#23 $\overline{DAC}$

TOP TRACE: $\overline{DAC}$, U34 pin 11
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

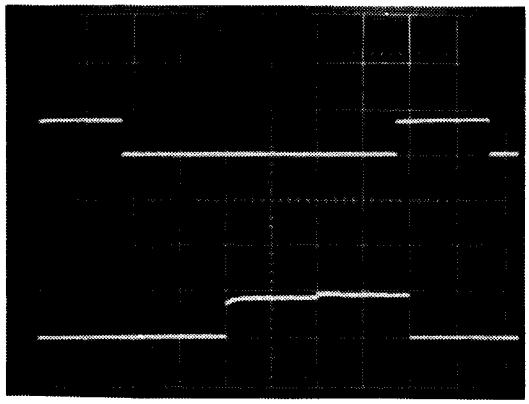


#24 DACEN

TOP TRACE: DACEN, U21 pin 11
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 µsec/div. (OFF CAL)

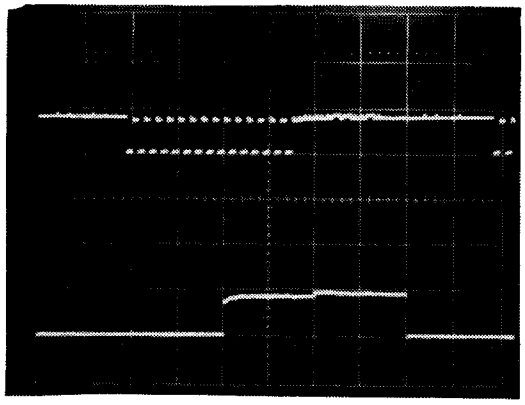


#25 $\overline{\text{DACX}}$

TOP TRACE: $\overline{\text{DACX}}$, U78 pin 20
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

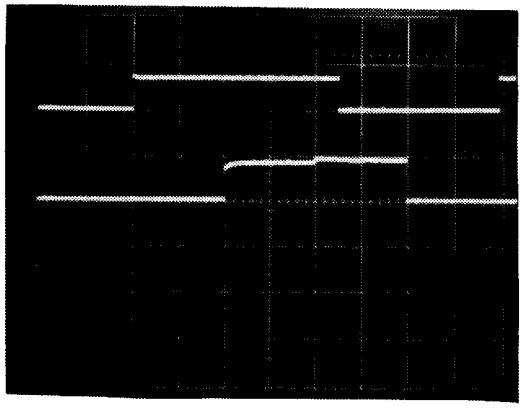


#26 $\overline{\text{MODB}}$

TOP TRACE: $\overline{\text{MODB}}$, U79 pin 20
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

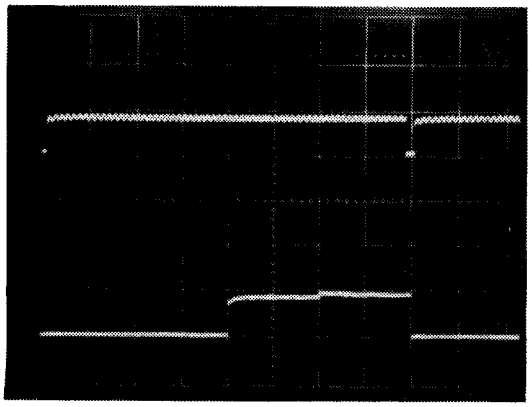


#27 ISHB

TOP TRACE: ISHB, U17 pin 8

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

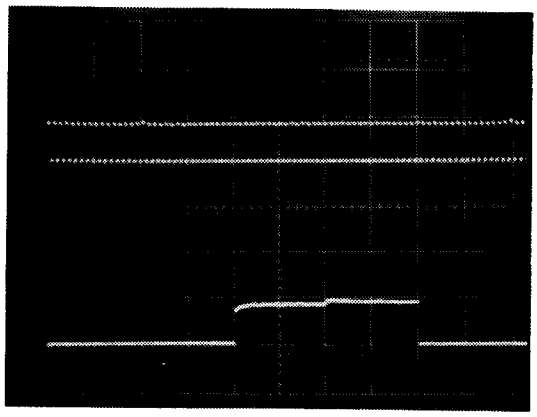


#28 $\overline{\text{SYNC CLEAR}}$

TOP TRACE: $\overline{\text{SYNC CLEAR}}$, U72 pin 1
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

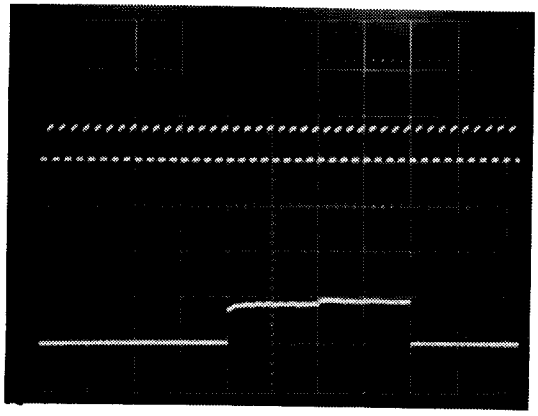


#29 $\overline{\text{TCB1}}$

TOP TRACE: $\overline{\text{TCB1}}$, U51 pin 10
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

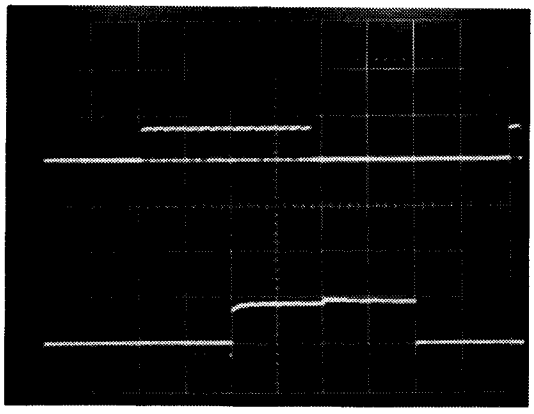


#30 TCB2

TOP TRACE: TCB2, U74 pin 1
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

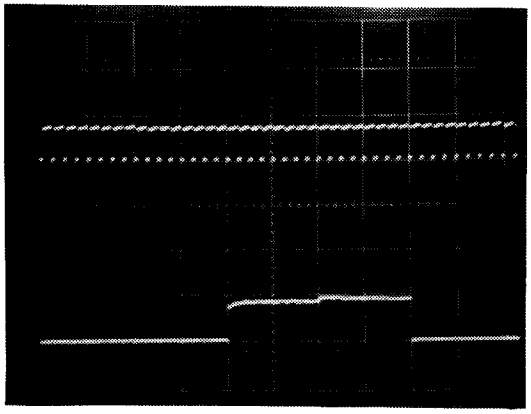


#31 GAIN MOD PROM ENABLE

TOP TRACE: GAIN MOD PROM ENABLE
U97, pin 12
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

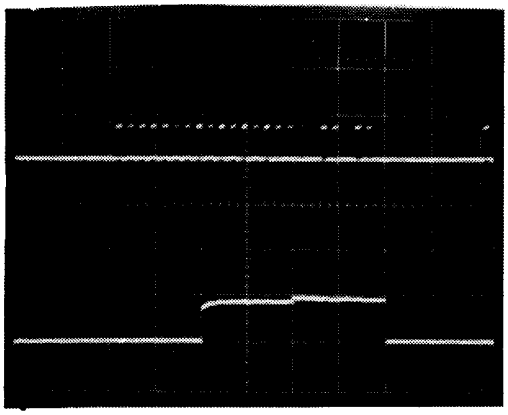


#32 $\overline{\text{GAIN LATCH}}$

TOP TRACE: $\overline{\text{GAIN LATCH}}$, U61 pin 11
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

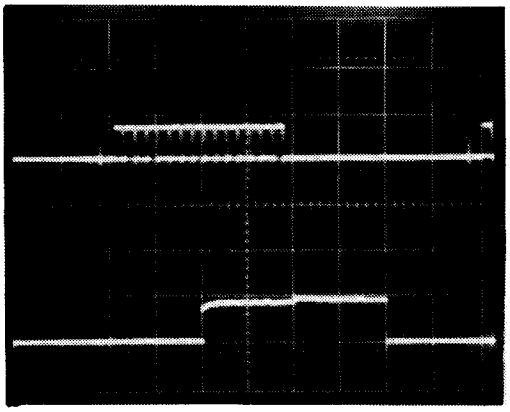


#33 DELAY ADDER CARRY IN

TOP TRACE: DELAY ADDER CARRY IN
U63 pin 7
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

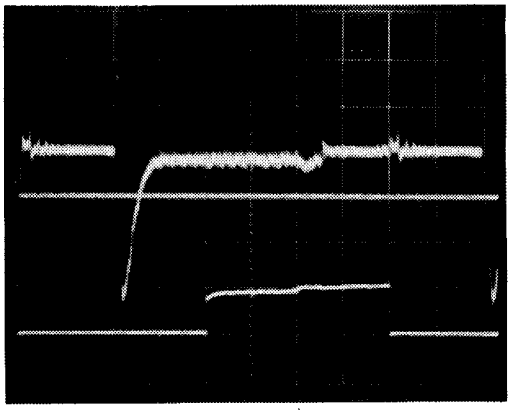


#34 A<B

TOP TRACE: A<B, U97 pin 13
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

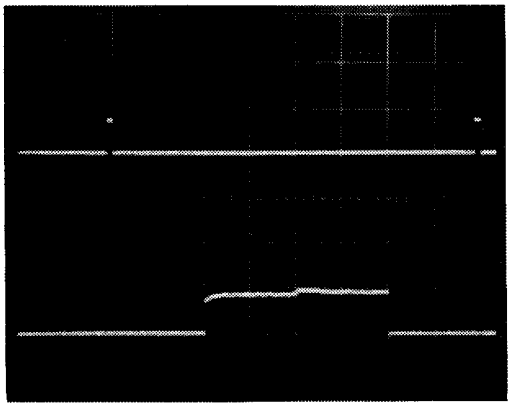


#35 DAC OFFSET

TOP TRACE: DAC OFFSET, U19 pin 1
20mV/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

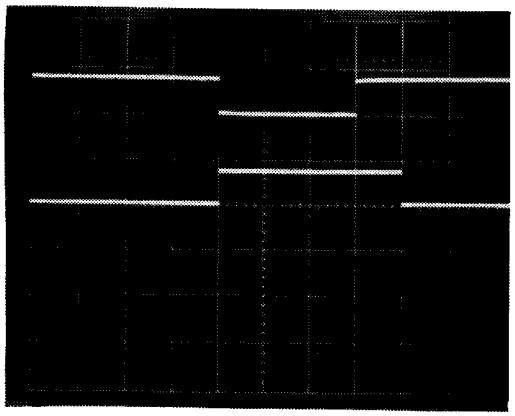


#36 COMPARE VALID

TOP TRACE: COMPARE VALID, U96 pin 10
5V/div.

TRIGGER TRACE: TCB7 5V/div.

SCOPE SETTING: 3.91 μsec/div. (OFF CAL)

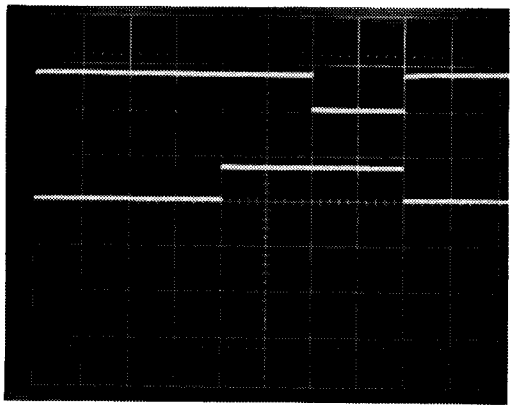


#37 DISPLAY MUX CONTROL BIT Ø

TOP TRACE: DISPLAY MUX CONTROL BIT Ø
U92 pin 14
5V/div.

TRIGGER TRACE: $\overline{WC6}$ 5V/div.

SCOPE SETTING: .5ms/div. ON CAL

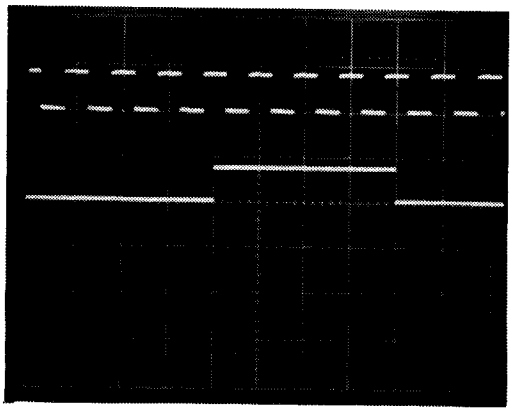


#38 DISPLAY MUX CONTROL BIT 1

TOP TRACE: DISPLAY MUX CONTROL BIT 1
U92 pin 2
5V/div.

TRIGGER TRACE: $\overline{WC6}$ 5V/div.

SCOPE SETTING: .5ms/div. ON CAL



#39 $\overline{DISPENB}$

TOP TRACE: $\overline{DISPENB}$, U99 pin 20
5V/div.

TRIGGER TRACE: $\overline{WC6}$ 5V/div.

SCOPE SETTING: .5ms/div. ON CAL

APPENDIX A.

This appendix contains all of the Factory Field Service Bulletins or ECO's released for the StarGate 323. Each Bulletin describes a remedial procedure for a specific problem or describes a hardware change necessary to implement an improvement in the machine design. There is currently only one Field Service Bulletin released for the StarGate 323.

Bulletin #1 -- Intermittent Clicking Sound

URSA MAJOR, Inc.

Box 18, Belmont, MA 02178 • Telephone (617) 489-0303
Telex: 921405 URSAMAJOR BELM

323 FIELD SERVICE BULLETIN #1 13 March 1984

TITLE: INTERMITTENT CLICKING SOUND

SYMPTOMS: Infrequent, occasional clicking sounds, mostly occurring only with signal present. The clicks may or may not also be reverberated by the 323. Sometimes all the Input Level LED's on the front panel display will flash when a click occurs.

UNITS AFFECTED: Serial Numbers 301-325. All units shipped after 13 March 1984 are OK and do not need attention.

PROBLEM: Occasional glitches on PROM U71 output pin 11 cause errors in ADC or DAC operations at some input signal levels. Our solution to the problem is to eliminate an IC no longer used, and to jumper a signal around it.

REQUIRED MATERIALS:

1. 16 pin DIP plug with pins 6 and 7 tied together, and with no connections to any of the other 14 pins. Such plugs are being provided with this FSB.

HOW TO CORRECT THE PROBLEM:

1. Remove the AC Cord from the 323 and unscrew the 11 4-40 screws that secure the top cover. Remove the top cover.

2. Viewing the PC board, with the front panel facing your stomach, locate IC U86, located at the right rear of the board, near the power transformer.

3. Using an IC extractor, or small screwdriver, remove this IC U86 (an 74LS253) from its socket and discard.

4. Insert the DIP Plug or DIP Header provided with this FSB in the socket, with the dot toward the rear of the unit. Be careful that the dot end is toward the rear, and that you align all 16 pins before pushing the Plug in. Be sure it is fully and firmly seated in place.

5. Put the top cover back in place, and secure it with its 11 screws.

APPENDIX B. PARTS LIST

The following is a parts list for the StarGate 323. It is intended to help you should you ever have to replace a part or order one from the factory.

APPENDIX B
Parts list

STOCK NO.	PART	LOCATION	QTY
RESISTOR 5% 1/4W			
201-0105	100	R5,R6,R7,R8,R9, R10,R18,R38,R91, R113,R114,R115, R116,R159,R160	15
201-0108	220	R94,R96	2
201-0122	47K	R85,R162	2
201-0464	3.9K	R83	1
201-0465	7.5K	R75	1
201-0569	1M	R133	1
201-0572	33K	R77,R89,R93	3
201-0606	330	R154	1
201-0721	3.3K	R76,R86,R111	3
201-0844	1.5k	R98	1
201-0845	1.6k	R105,R106	2
201-0846	2.2k	R156	1
201-0847	6.8k	R107	1
201-0848	13k	R87,R88	2
201-0849	18k	R19,R39,R70	3
201-0850	30k	R27,R47	2
201-0863	75k	R17,R37,R69	3
201-0866	16	R151	1
201-0867	36	R152	1
201-0868	82	R153	1
201-0869	56K	R108	1
201-0872	16k	R92	1
201-0875	91K	R71	1
RESISTOR 1% 1/4W			
202-0083	1.00k	R1,R2,R3,R4,R118 R119,R120,R121, R124,R125,R126, R127,R155	13
202-0087	4.02k	R101,R103	2
202-0093	10.0k	R11,R12,R13,R14, R15,R16,R31,R32, R33,R34,R35,R36, R51,R52,R53,R54, R55,R56,R58,R72, R73,R78,R79,R80, R84,R95,R97,R109, R111,R131	30

STOCK NO.	PART	LOCATION	QTY
202-0096	20.0k	R57,R139,R161	3
202-0470	124	R157	1
202-0473	383	R158	1
202-0474	619	R138	1
202-0483	20.5k	R130,R135	2
202-0612	200	R140,R142,R144,R146	4
202-0613	3.09k	R102,R104	2
202-0615	5.23k	R23,R43,R62	3
202-0851	1.87k	R136,R137	2
202-0852	2.00k	R25,R45,R64,R74, R132,R134,R147,	9
202-0853	6.19k	R30,R50,R68	3
202-0854	8.66k	R21,R41,R60	3
202-0855	9.31k	R20,R40,R59	3
202-0856	11.5k	R28,R48,R66	3
202-0857	11.8k	R22,R42,R61	3
202-0858	12.1k	R26,R29,R46,R49 R65,R67	6
202-0859	12.7k	R24,R44,R63	3
202-0860	16.2k	R117,R122,R123 R128	4
202-0861	38.3k	R81,R82	2
202-0862	221	R129	1
202-0876	2.37k	R90	1

RESISTOR 5% 1/2W

203-0582	100	R101,R102,R103, R104,R105,R106, R107,R108,R109,R110	10

RESISTOR NETWORK (SIP)

214-0500	10PIN 3.3K	RN8,RN9,RN10,RN11, RN12,RN13,RN14	7

RESISTOR NETWORK (DIP)

220-0326	8PIN QUAD .05% 10.0K	RN1,RN2,RN3,RN4, RN14,RN15	6
220-0635	8PIN QUAD .05% 330	RN5,RN6	2

STOCK NO.	PART	LOCATION	QTY
POTS			
240-0747	Dual 50k	RV1,RV2,RV3,RV4, RV5	5
250-0443	100k	RV9	1
CAP, TANT SOLID DIPPED			
301-0128	22uF/16V	C98,C100,C104, C123,C149,C150,	6
301-0258	4.7uF/35V	C53,C55,C74,C75, C99,C151,C152	7
CAP, ALUMINUM ELECTROLYTIC			
310-0136	4.7uF/35V	C9,C10,C18,C31, C56,C59,C60	7
310-0356	2200uF/35V	C80,C81	2
310-0357	15000uF/16V	C196	1
310-0452	22uF/25V	C128,C130,C131,C192	4
CAP, POLYPROPYLENE AXIAL			
331-0140	220pF/2.5%	C50,C63,C82,C83,C87, C88,C91,C103,C105, C212	10
331-0141	1000pF/2.5%	C1-C4,C11-C13,C15, C19-C22,C24,C25,C27, C30,C32-C35,C37,C38, C42-C46,C51,C54,C65,	32
CAP, CERAMIC DISC			
361-0132	.01uF/50V	C118	1
361-0133	.02uF/50V	C7,C8,C14,C16,C17, C23,C26,C28,C29,C36, C39-C41,C47,C48,C52, C57,C61,C62,C64,C67, C68,C72,C76-C79,C106, C119-C122,C132-C146, C148,C153-C185,C187- C191,C193,C198-C203, C210,C211,C213,C214, C215,C303,C304	100
365-0131	.0047uF/1600V	C194,C195	2

STOCK NO.	PART	LOCATION	QTY
CAP, STACKED POLYESTER			
371-0599	.22uF/63V	C49,C69,C70,C71, C73	5
CAP, MONOLYTHIC			
381-0294	.1uF/50V	C5,C6,C84,C86,C89, C90,C92-C97,C101, C102,C110-C117, C124-C127,C305,C306	28
DIODES			
410-0154	1N4148	D17-D20	4
410-0155	1N4004	D1-D8,D11,D14	10
410-0156	1N5404	D12,D13	2
421-0160	1N4783A	D15,D16	2
425-0725	1N6263	D9,D10	2
OSCILLATOR			
431-0746	8.192MHz	U65	1
LED's			
452-0813	T1 3/4, RED	D8,D9,D10,D11	4
452-0814	T1 3/4, YELLOW	D6,D7	2
452-0815	T1 3/4, GREEN	D1-D5	5
LED, SEVEN SEGMENT DISPLAY			
460-0348		DI1-DI7	7
IC's, DIGITAL			
470-0161	74LS00	U51,U95,U97	3
470-0162	74LS04	U44,U66,U89,U94	4
471-0163	7406	U54	1
470-0164	74LS08	U96	1
470-0165	74LS14	U45	1
470-0167	74LS74	U50,U57,U83	3
470-0315	74LS85	U48,U55,U67,U68	4
470-0270	74LS86	U49,U81	2
471-0168	74123	U98	1

STOCK NO.	PART	LOCATION	QTY
470-0332	74LS138	U39,U100	2
470-0819	74LS158	U74,U80	2
470-0169	74LS163	U52,U53,U72,U73,U75	5
470-0787	74LS240	U101	1
470-0215	74LS253	U58,U91,U92	3
470-0171	74LS257	U90	1
470-0797	74LS273	U62	1
470-0216	74LS283	U63,U70	2
470-0820	74LS298	U60,U61	2
470-0316	74LS373	U21,U28,U34,U36,U38	5
470-0317	74LS374	U42,U43,U56,U59	4
470-0492	**74LS393**	**U82,U85,U87,U88**	**4**

PROM's

0803	28L22	U71	1
0810	28L22	U47	1
0811	28L22	U46	1
0804	2732	U76	1
0805	2732	U77	1
0806	2732	U78	1
0807	2732	U79	1
0809	2732	U99	1
0808	2764	U69	1

N.B. These parts are available from Ursa Major only.

DAC's

480-0337	DAC08HQ	U20,U27,U33,U40	4

N.B. This part should be obtained from Ursa Major (it is sorted).

RAM

496-0767	16Kx4 Dynamic RAM TMS-4416-15 OR MB81416-15 OR IMS2620P-15	U22,U29,U35,U37	4

SAR

510-0174	AM2502	U41	1

STOCK NO.	PART	LOCATION	QTY
DISPLAY DRIVERS			
525-0354	ULN-2803A	U103	1
525-0356	UDN-2981A	U102	1
VOLTAGE REGULATORS			
535-0182	LM340T-15 OR MC78M15CT OR UA7815KL	U105	1
535-0183	LM320T-15 OR MC7915CT OR UA7915KC	U104	1
535-0437	LM338K	U106	1
COMPARATORS			
540-0568	CMP-05FZ	U25	1
540-0798	LM339	U64	1
SAMPLE + HOLD 545-0199 ANALOG SWITCH	LF398	U17	1
550-0202	MC14053BCP	U2	1
550-0768	HI-201HS-5	U26,U31	2
OP-AMPS			
555-0198	NE5534	U32	1
555-0203	TL074CN	U4-U7,U10-U13,U30	9
555-0337	NE5532N	U3,U8,U9,U15,U19	5
555-0579	TL072CP	U14,U16,U23,U24	4
SOCKETS, DIP			
560-0148	8pin		14
560-0149	14pin		30
560-0150	16pin		29
560-0152	20pin		13
560-0459	18pin		4
560-0816	28pin		6
SOCKET, CAPTIVE DIP			
561-0151	16pin	J10	1

	STOCK NO.	PART	LOCATION	QTY
	SOCKET, MISC.			
	562-0052	TO-220	J11,J12	2
	562-0192	Fuse Clip	F1,F1,F2,F2	4
	562-0371	TO3	Chassis Mount	1
	FUSES			
	565-0193	3AG .75A 115V	F2	1
	565-0194	8AG 2.5A	F1	1
	TRANSFORMER			
	570-0788	115/230 V		1
or	570-0839	100/200 V		
	CONNECTOR			
	574-0751	Phono Jack	J5,J6,J7	3
	576-0749	"XLR" Male	J3,J4	2
	576-0750	"XLR" Female	J1,J2	2
	578-0257	Power Receptacle	Chassis Mount	1
	583-0784	Wafer, 3 pin	J13	1
	WIRE			
	600-0546	White 20 AWG 15.5 inches	PC1	1
	600-0547	Black 20 AWG 16.0 inches	PC2	1
	600-0551	Red 20 AWG 2.0 inches	#2	1
	600-0552	Black 20 AWG 2.0 inches	#1	1
	600-0553	Green 20 AWG 2.0 inches	#3	1
	600-0556	Green 20 AWG 3.0 inches		1

STOCK NO.	PART	LOCATION	QTY
TEST POINT			
610-0786	Wire Loop Test Point	TP1-TP5	5
WIRE JUMPERS			
610-0812	White .7 inches long	L1-L11	11
POWER CORD			
615-0266	American, 7.5 feet		1
RIBBON JUMPER CABLE			
620-0796	16 pin 9.0 inches both ends up	J9	1
SWITCHES			
630-0753	5 station 4 assmb. switch PCB Mount, with buttons	S4-S7	1
631-0045	Voltage Selector switch, PCB Mount	S8	1
633-0752	16 position digital rotary switch	S1-S3	3
BUTTONS AND KNOBS			
640-0874	Black Switch Button		4
646-0792	Light Grey Knob with Matte Black Sides		2
646-0793	Blue Knob with Matte Black Sides		3
646-0794	Red Knob with Matte Black Sides		3

STOCK NO.	PART	LOCATION	QTY
SPACERS			
657-0800	Nylon, Hex .406 inches 6-32, M/F	SOA,SOB	2
658-0801	Nylon, Hex 2.813 inches 6-32, F/F	SOA,SOB	2
MISC. HARDWARE			
660-0217	Machine Screw, Pan Head 4-40x3/16, Black		22
660-0218	Machine Screw, Pan Head 4-40x5/16, Black		4
660-0219	Machine Screw, Flat 82 degree 4-40x5/16, Black		8
660-0224	Machine Screw, Pan Head 6-32x1/4, Black		16
660-0226	Machine Screw, Pan Head 6-32x1/2, Black		2
660-0446	Machine Screw, Pan Head 4-40x4/16, Black		8
660-0447	Machine Screw, HexCap 6-32x3/8, Black		4
660-0449	Machine Screw, Pan Head 6-32x5/16, Black		4
660-0589	Machine Screw, HexCap		4
665-0790	#4 3/16 sheet metal screw		2
665-0791	#2 3/16 sheet metal screw		4
680-0450	Esna Nut 6-32		8
680-0563	Esna Nut 8-32		4
680-0688	Esna Nut 4-40		2
685-0228	#6 Internal Star Washer		17
686-0686	#6 Split Lock Washer		2
690-0238	Right Angle Bracket		4
696-0300	Power Receptacle Pin Crimp Terminal		3
698-0239	Terminal Ring, Crimp #6, #22 AWG		1
705-0234	#4 Nylon Washer TO220 Case Insulator		2
705-0802	Flat Nylon Washer		3
708-0282	TO-220 Voltage Regulator Insulator		2
708-0423	TO-3 Voltage Regulator Insulator		1

STOCK NO.	PART	LOCATION	QTY
HEAT SINK			
715-0370	TO-3 Chassis Mount Heat Sink		1
FRONT PANEL MASK			
725-0840	323 polycarbonate, Multi-Color		1
FRONT PANEL WINDOW			
730-0748	clear plastic		1
BUMPON (FEET)			
745-0253	square, black		4
SHEET METAL			
750-0763	Chassis		1
750-0764	Front Panel		1
750-0765	Bottom Cover		1
750-0818	Top Cover		1
TO-3 VOLTAGE REGULATOR COVER			
785-0372	TO-3 Cover		1
785-0558	TO-3 Screw Cover		2
POWER SWITCH SHIELD			
786-0789	1/16 clear, plexi, 3.0x1.75 with 90 degree bend		1
MISC.			
0881	Owner's Manual		1
0882	Quick Reference Card		1
770-0864	Shipping carton		1
780-0706	Packing foam		1

APPENDIX C. BLOCK DIAGRAMS AND SCHEMATICS

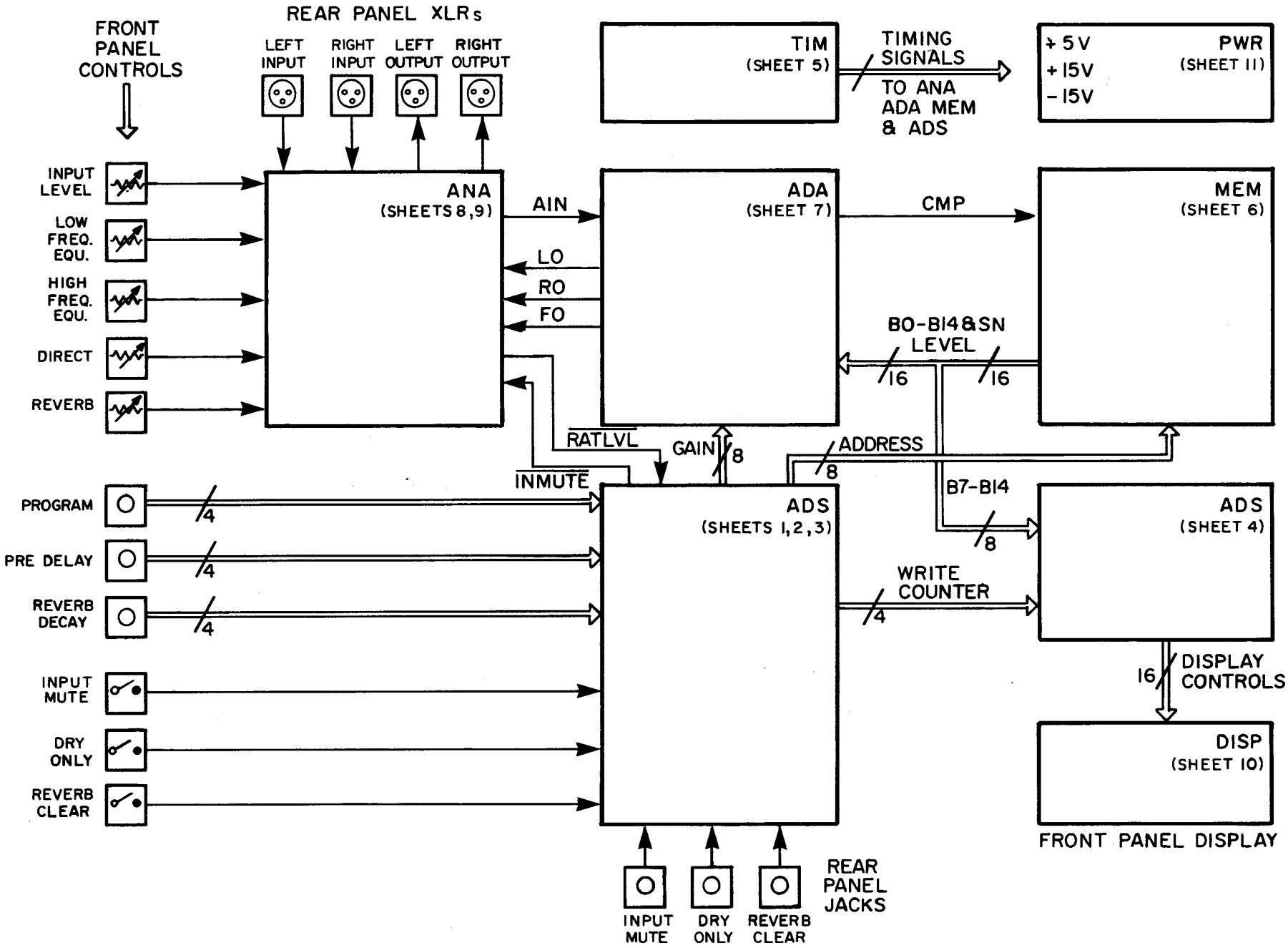
These schematics are, of course, crucial if you are trying to service a StarGate 323. Standard conventions were used in drawing the schematics. Logic flow is from left to right and from top to bottom. All signals enter each sheet from the left and leave each sheet from the right. Whenever a signal enters or leaves a sheet, it is clearly marked with the signal's name and the sheet number of its source or destination. Connectors, ie J13 etc, are shown as narrow vertical rectangles with the pin numbers written inside them. The signal name and its source or destination are listed to the side of the connector. The designation "P/O" stands for "Part Of".

The following are additional notes about the schematics:

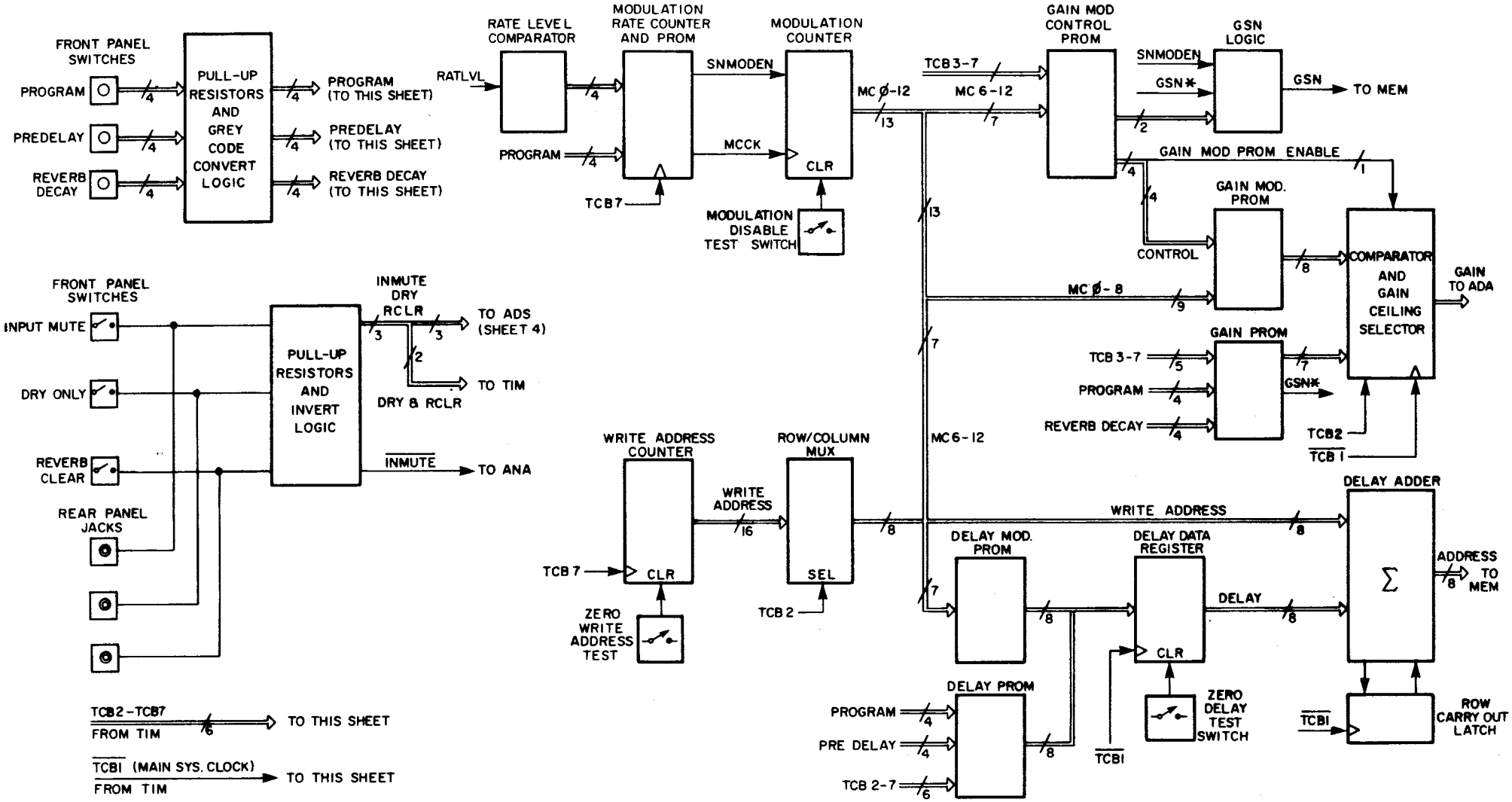
Note 1. The following components (shown on Schematic sheet 7) have been deleted: R141, R143, R145; C107, C108, C109; and RV6, RV7, RV8.

Note 2. The current software revision of PROM 0803-B forces signal SNMODEN to zero. This signal is located at U71 pin 11, (shown on Schematic sheet 7).

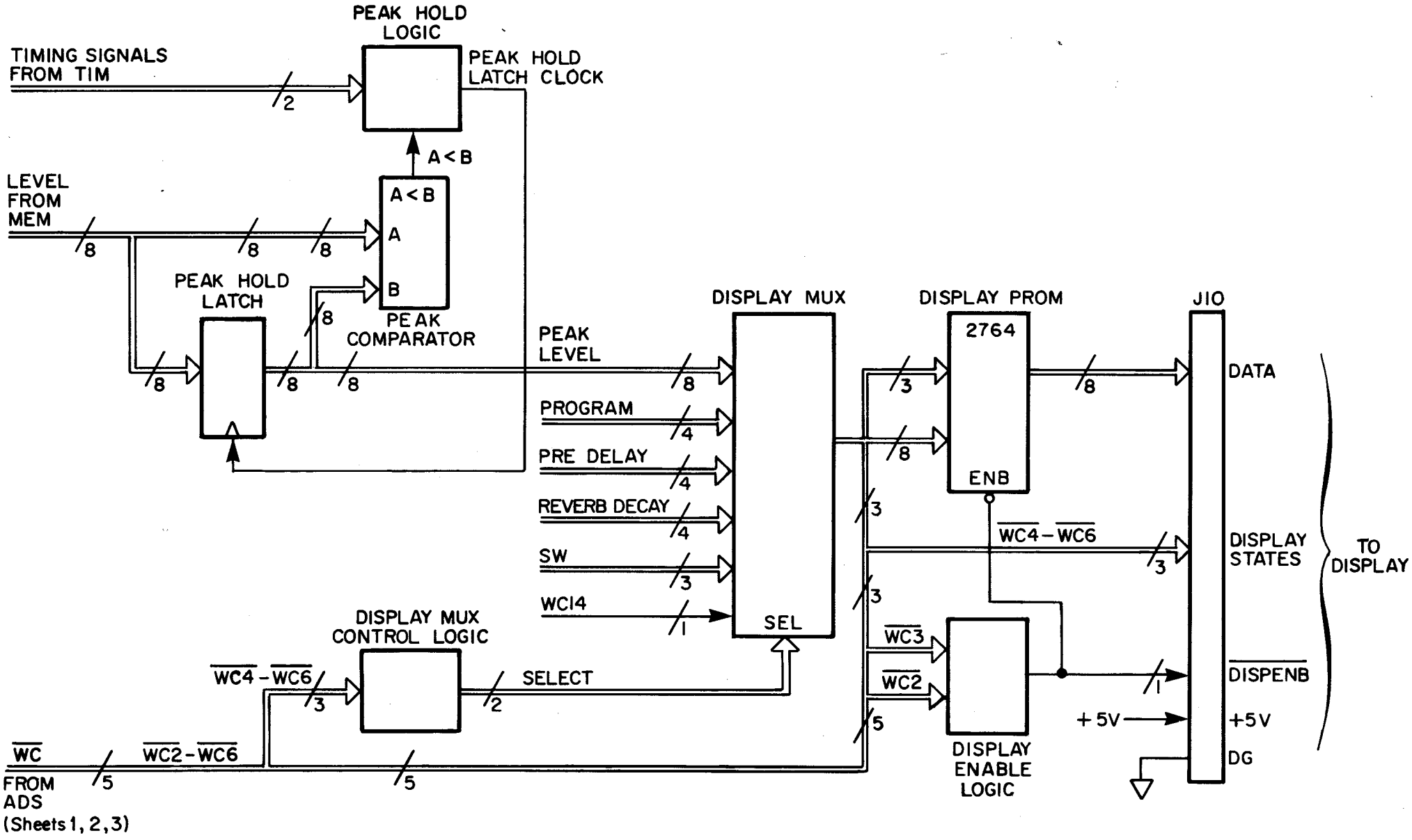
Note 3. U86 has been deleted from the machine. This is indicated in the Schematics (sheet 2). In earlier numbered machines (serial #s 301-325) U86 was replaced with a black DIP header that shorts pins 6 and 7 together. Machines after serial #325 have no jumper located in the socket or have no socket at all. These machines do have pins 6 and 7 shorted together.



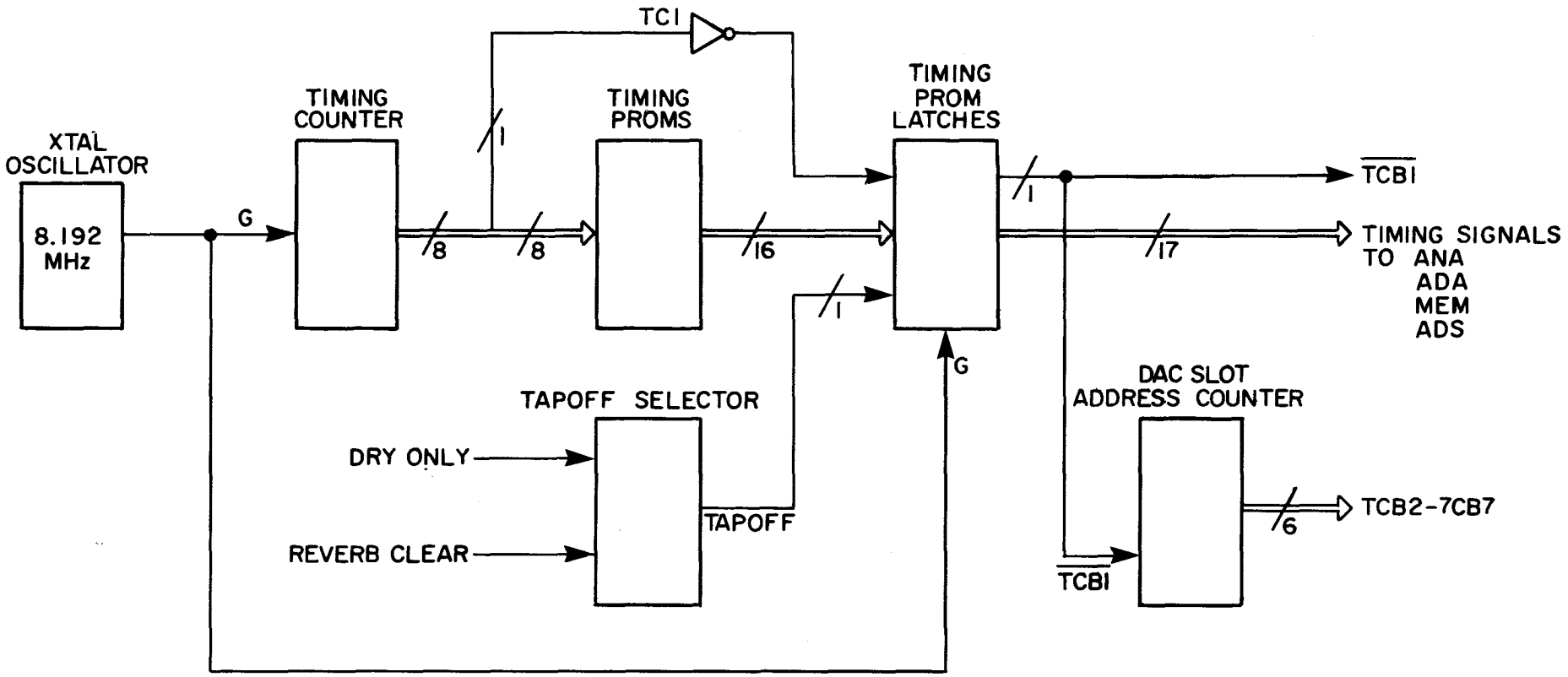
STARGATE 323 DIGITAL REVERBERATOR
SYSTEM BLOCK DIAGRAM



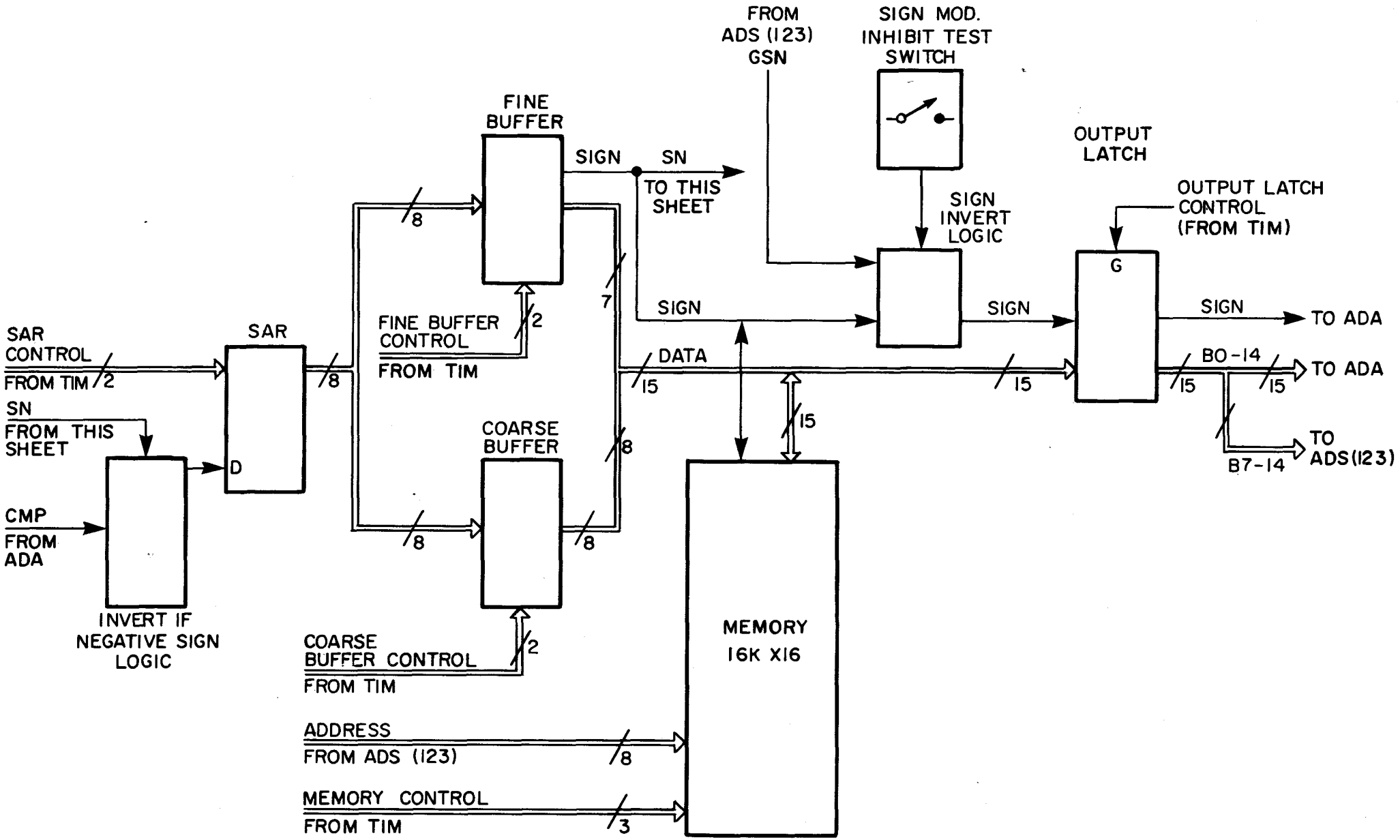
STARGATE 323 DIGITAL REVERBERATOR
ADS-BLOCK DIAGRAM
(Schematic Sheets 1,2,3)



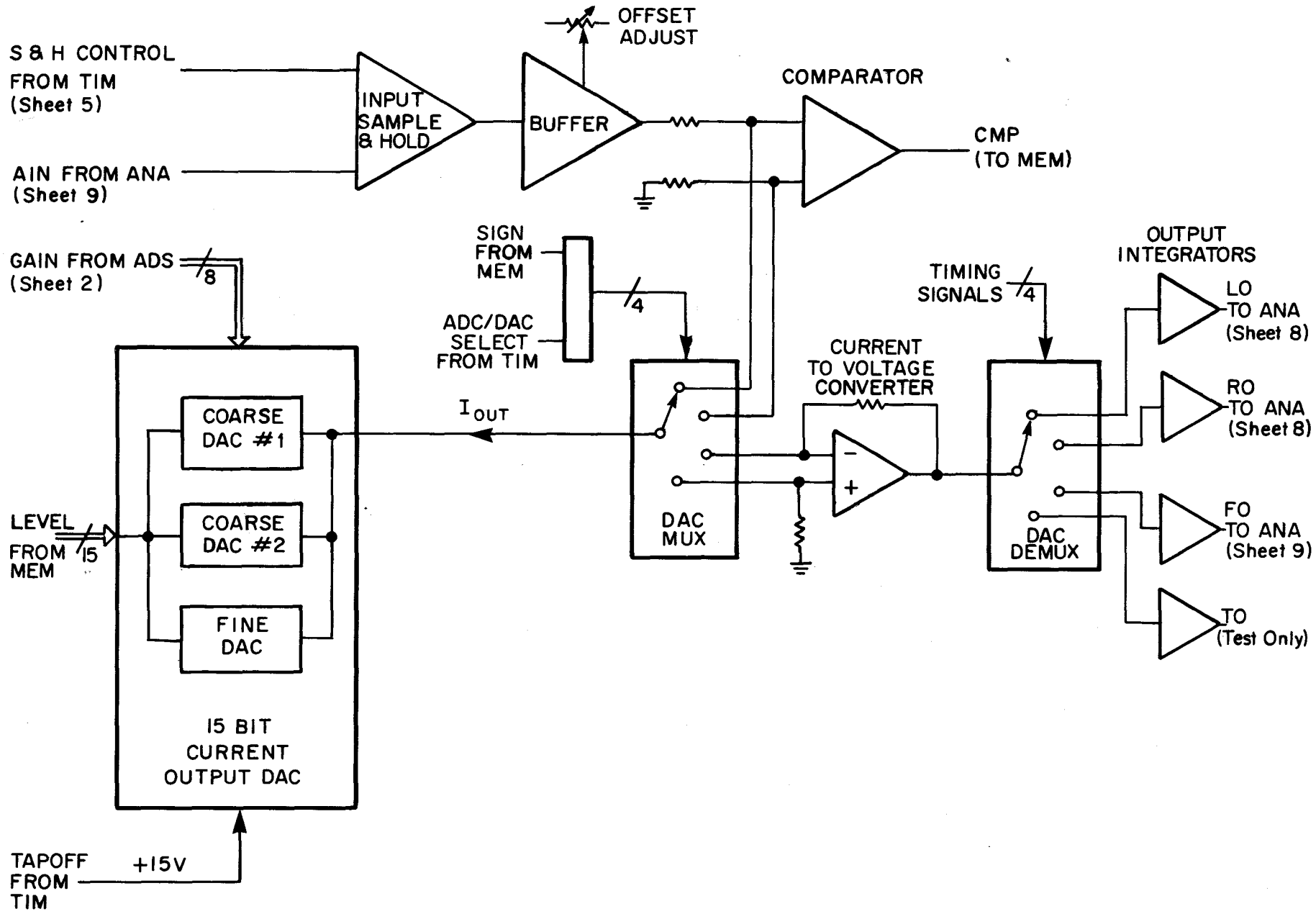
STARGATE 323 DIGITAL REVERBERATOR
ADS–BLOCK DIAGRAM
(Schematic Sheet 4)



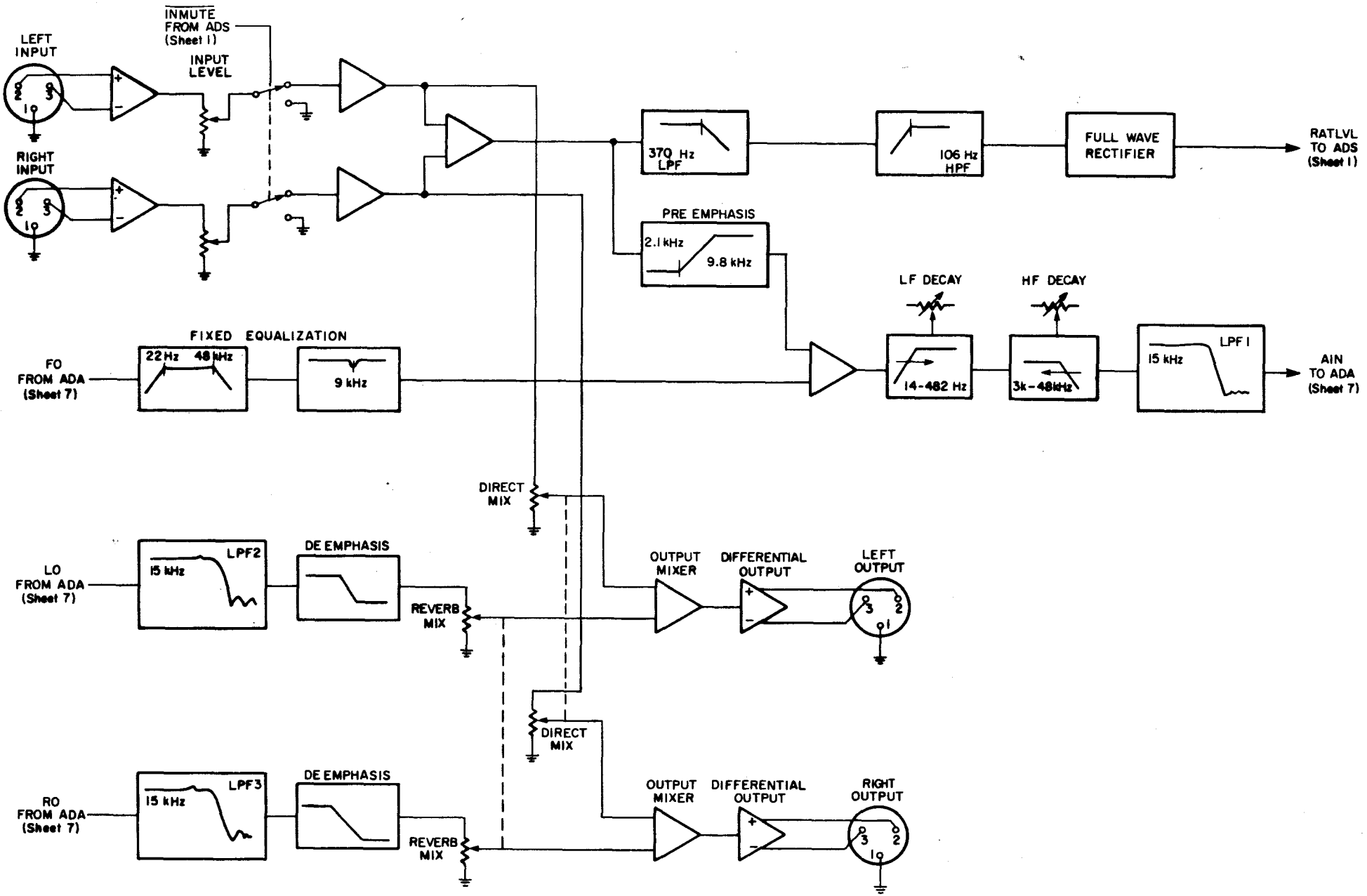
STARGATE 323 DIGITAL REVERBERATOR
TIM-BLOCK DIAGRAM
(Schematic Sheet 5)



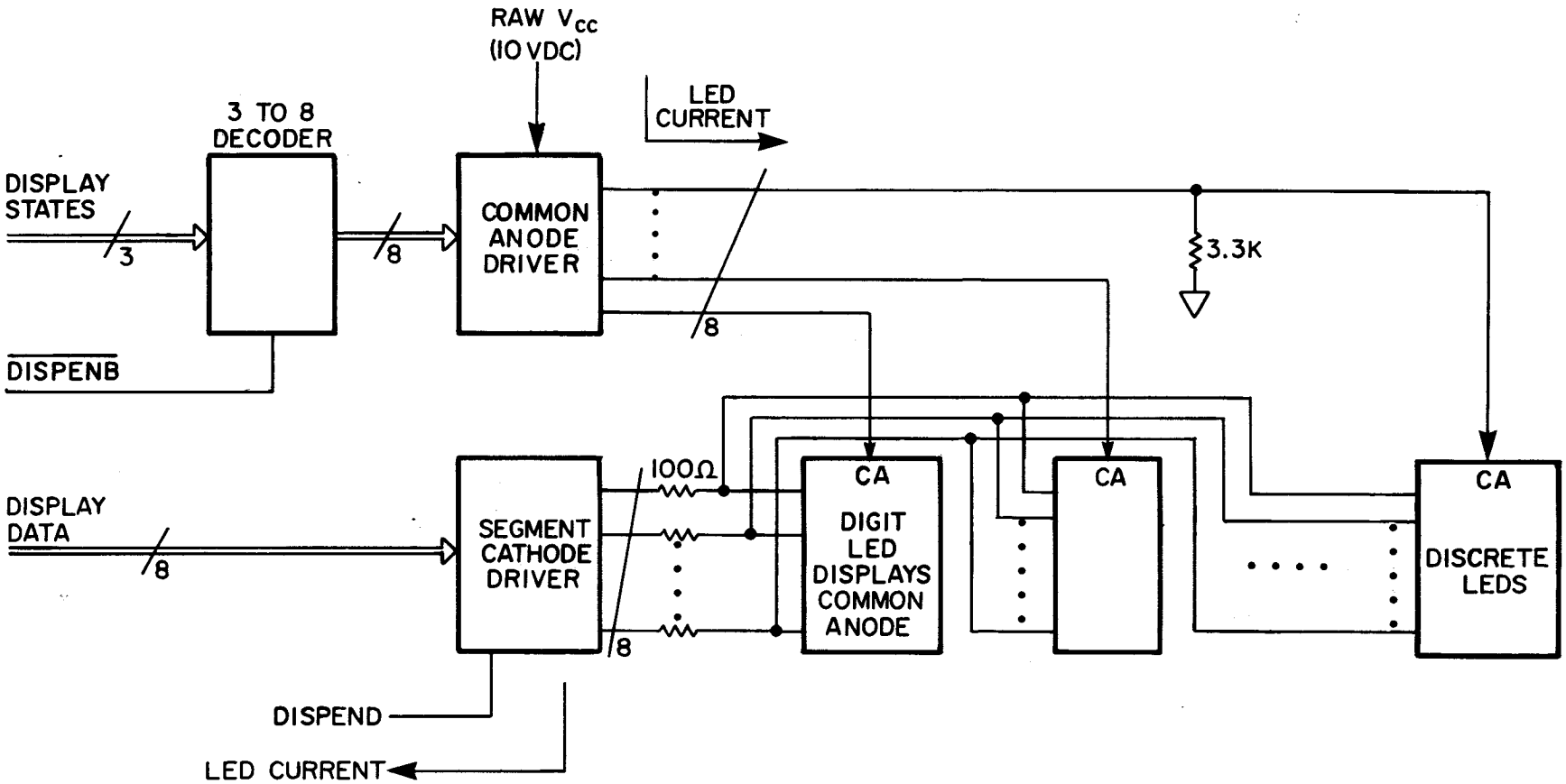
STARGATE 323 DIGITAL REVERBERATOR
MEM - BLOCK DIAGRAM
(Schematic Sheet 6)



STARGATE 323 DIGITAL REVERBERATOR
ADA-BLOCK DIAGRAM
(Schematic Sheet 7)



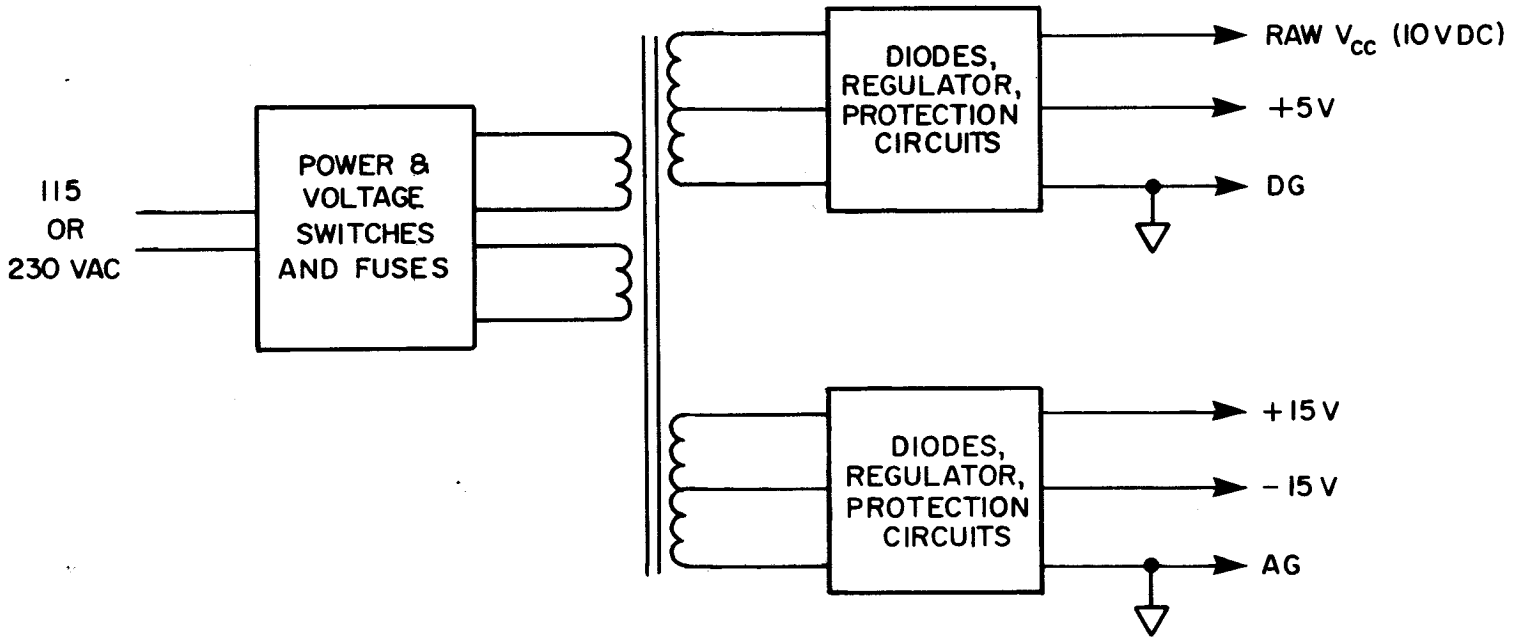
STARGATE 323 DIGITAL REVERBERATOR
ANA-BLOCK DIAGRAM
(Schematic Sheets 8,9)



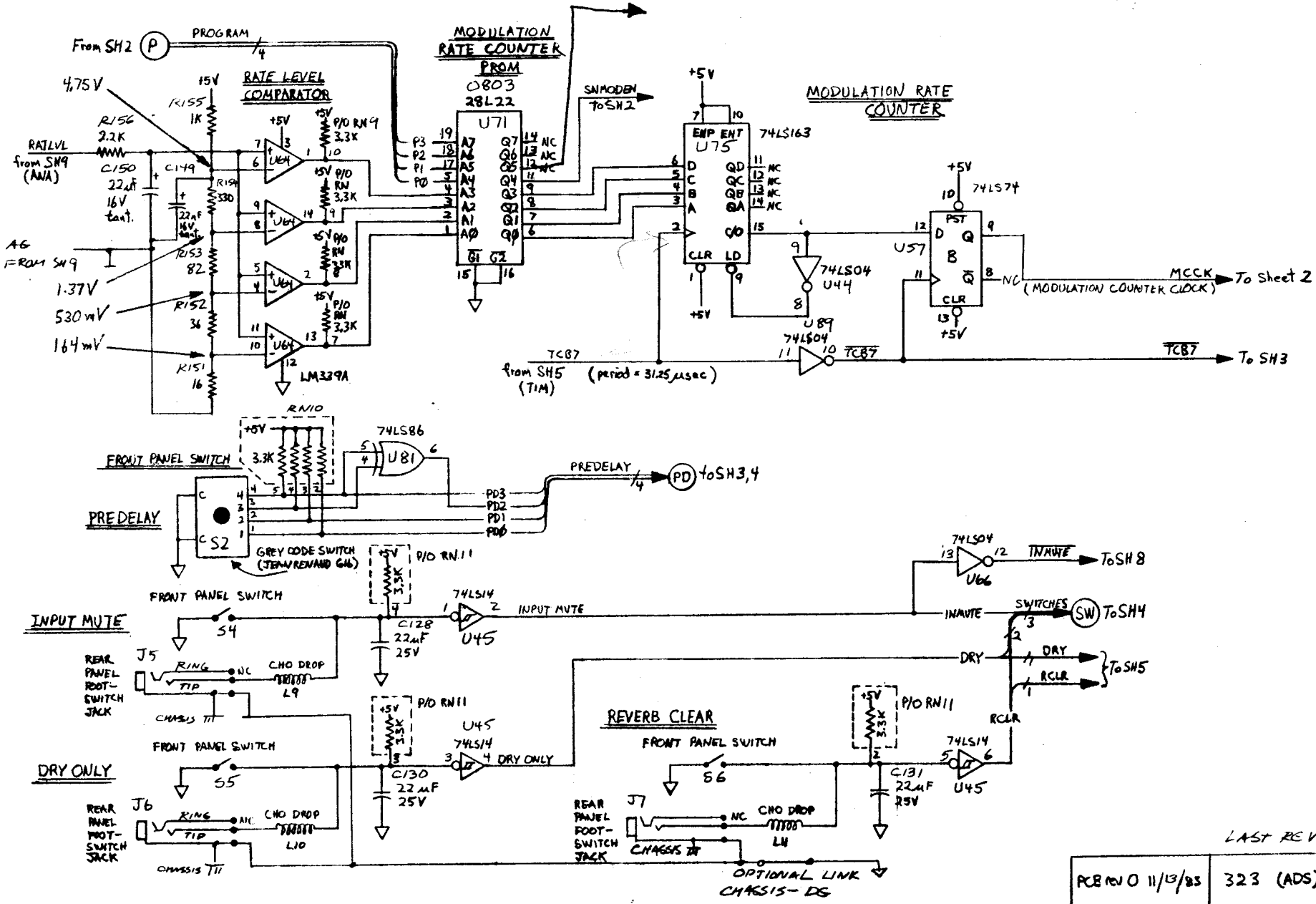
STARGATE 323 DIGITAL REVERBERATOR

DISP-BLOCK DIAGRAM

(Schematic Sheet 10)

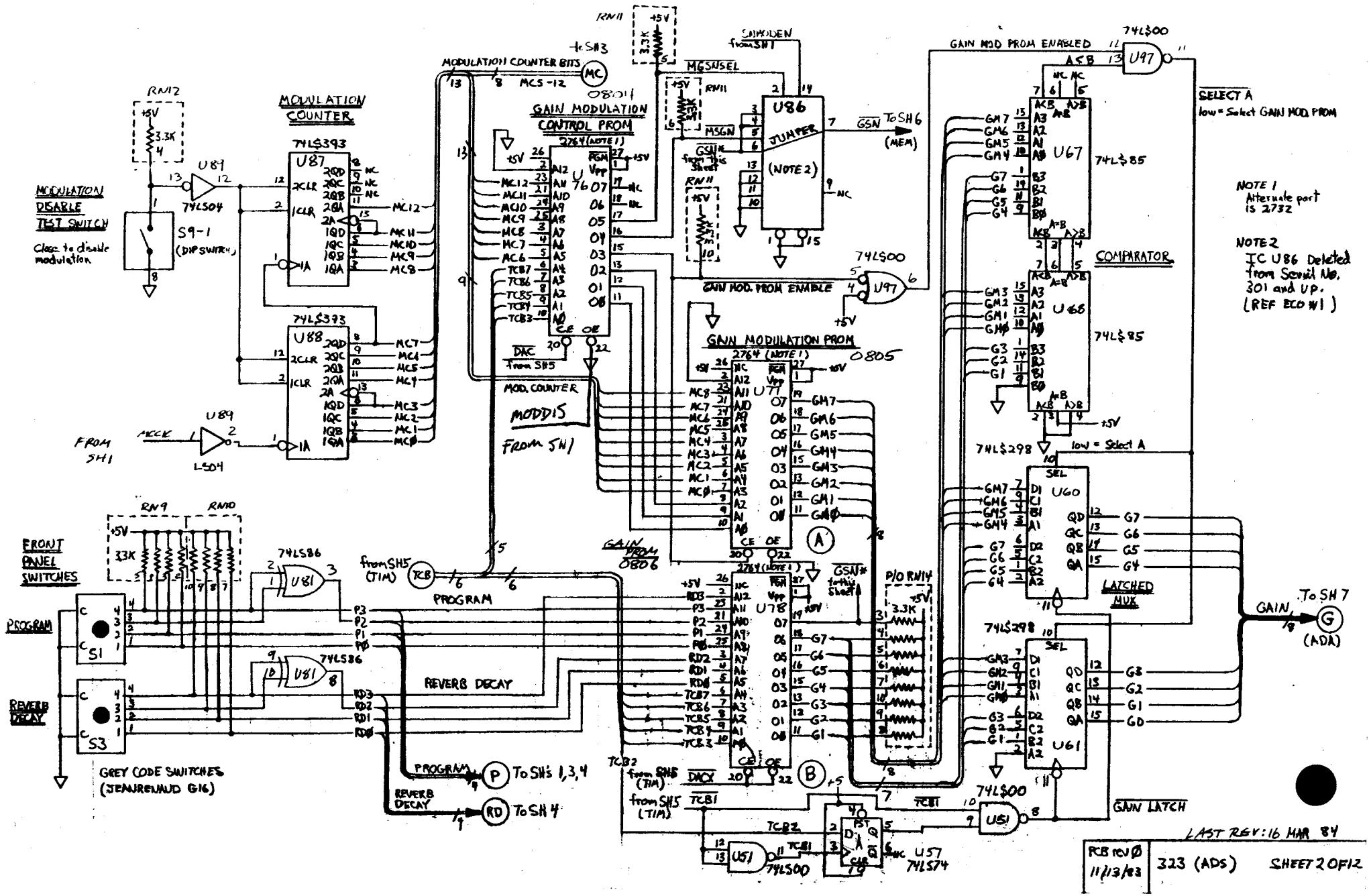


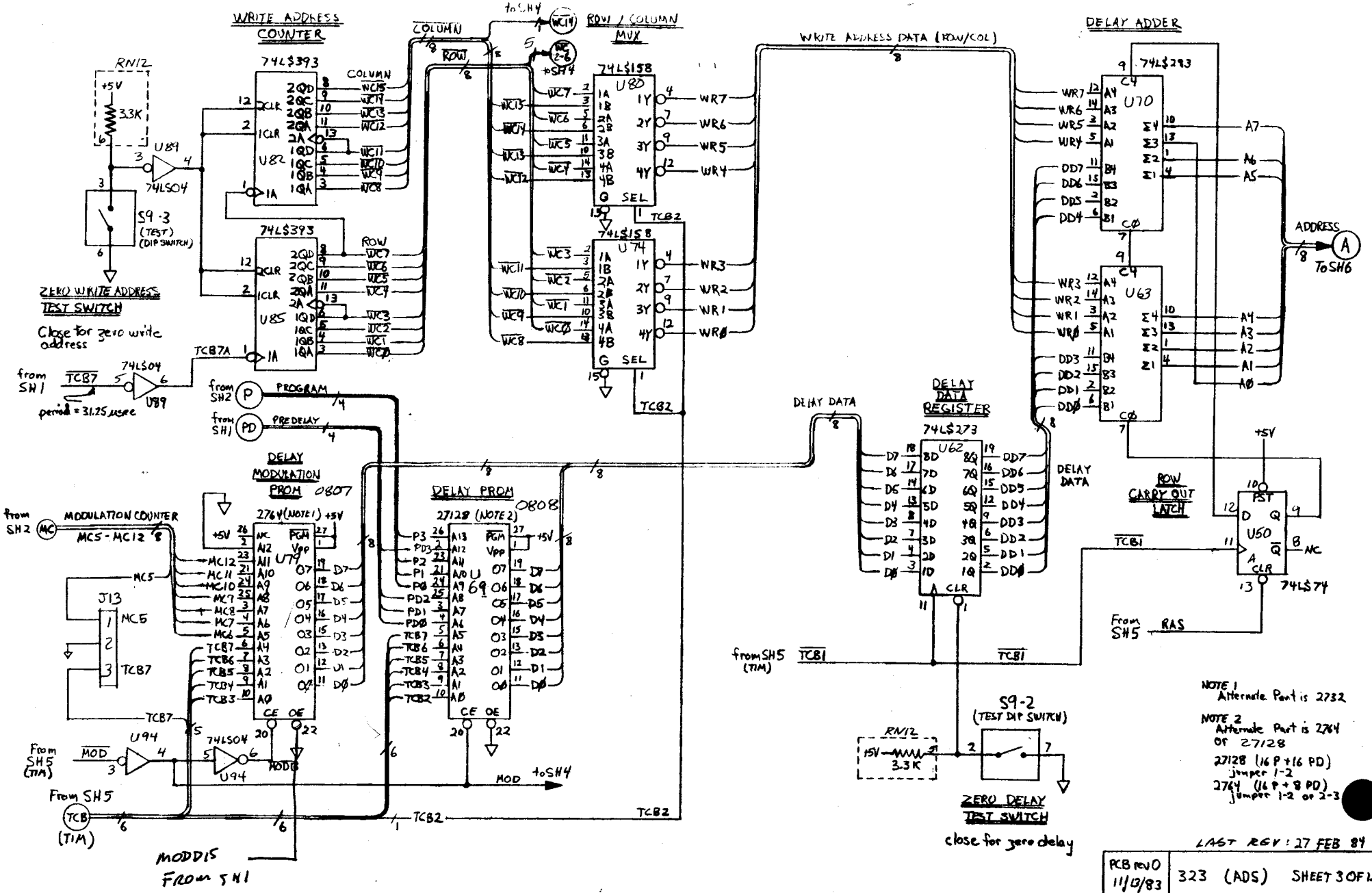
STARGATE 323 DIGITAL REVERBERATOR
PWR-BLOCK DIAGRAM
(Schematic Sheet 11)

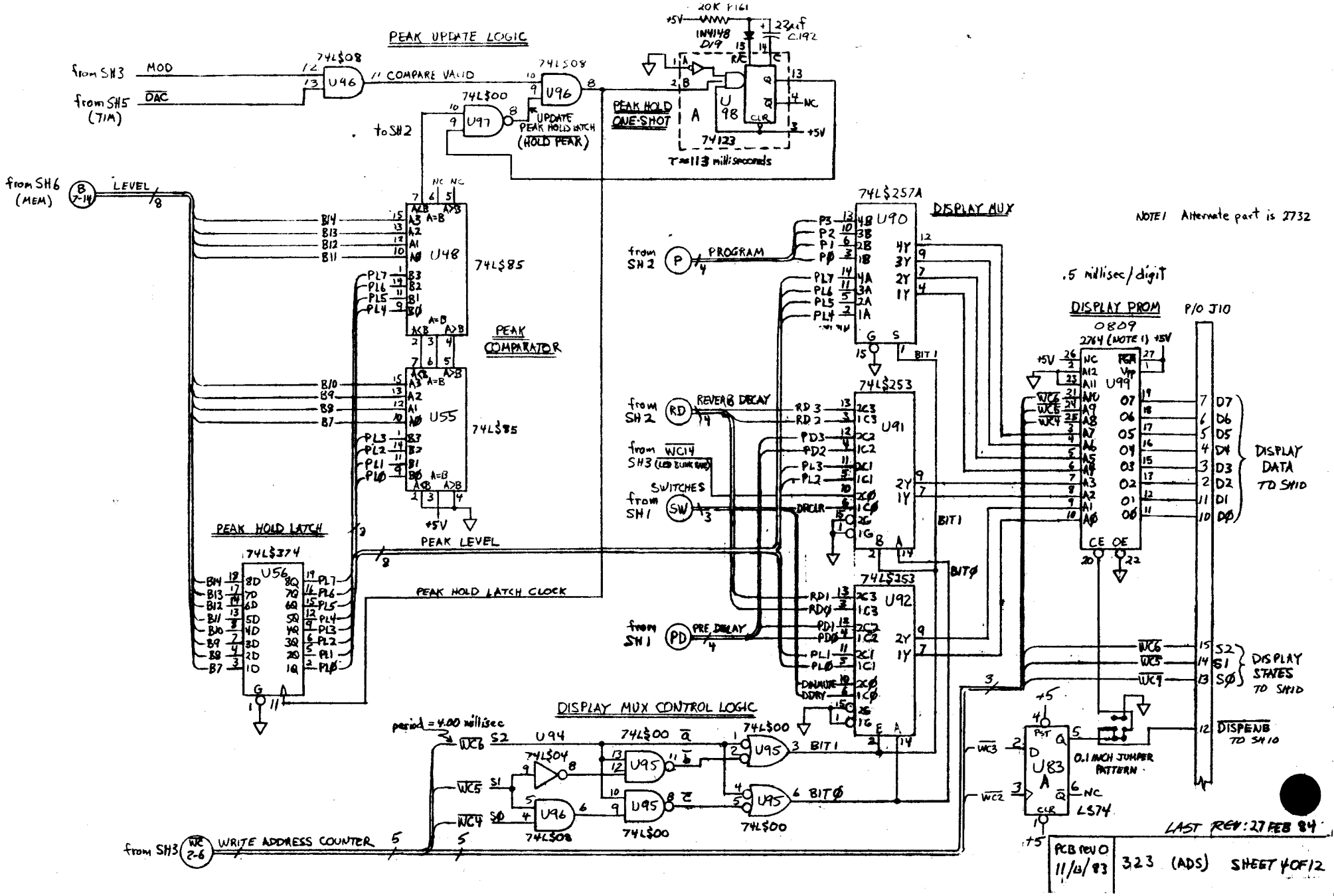


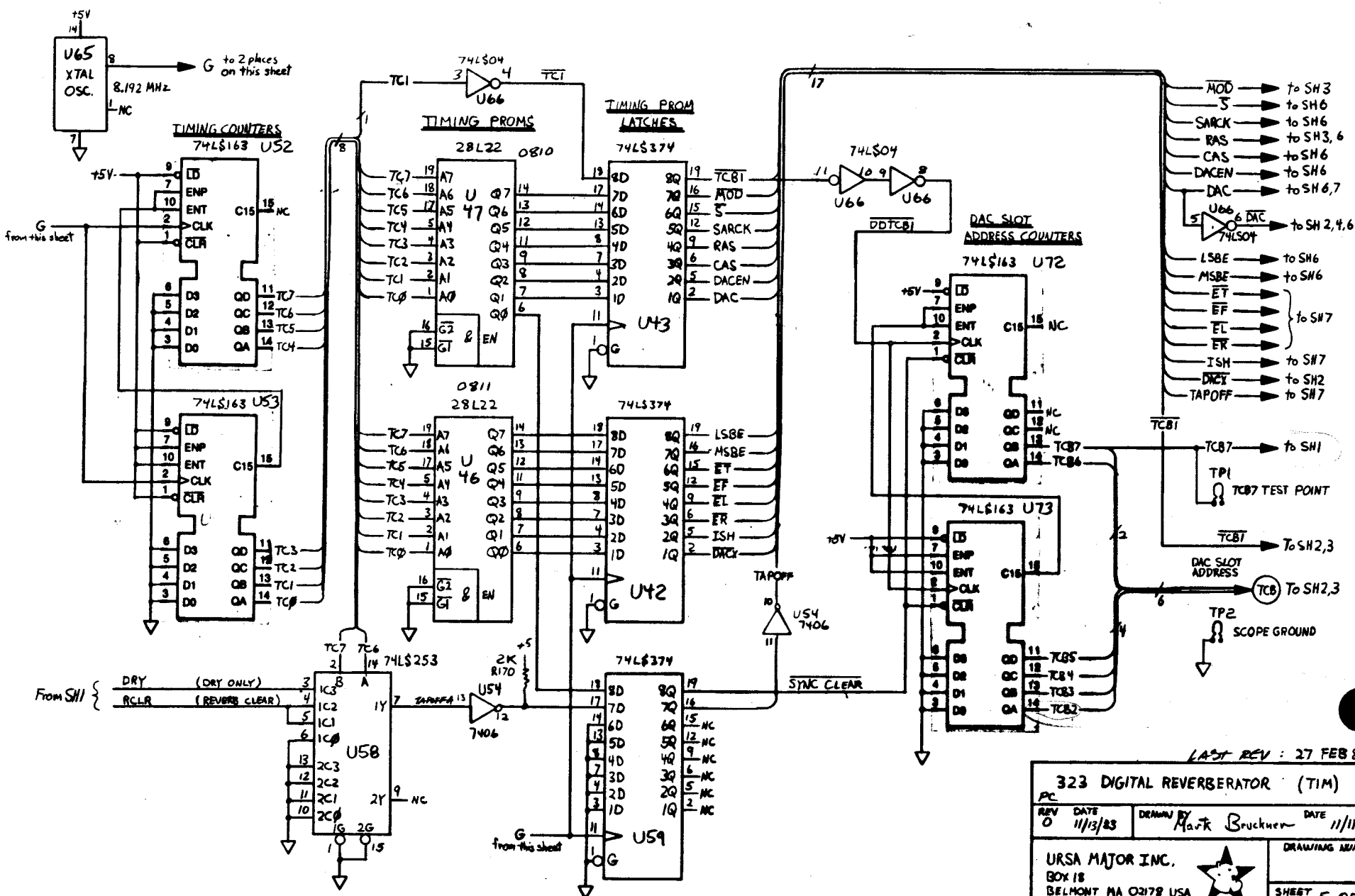
LAST REV: 27 FEB 84

PCB rev 0 11/13/83	323 (ADS)	SHEET 1 OF 12


MODULATION DISABLE TEST SWITCH
Close to disable modulation
S9-1 (DIP SWITCH)
MODULATION COUNTER
74LS393
U87
U88
74LS04
U89
MCCK
FROM SH1
MODULATION COUNTER BITS MC5-12
to SH3
GAIN MODULATION CONTROL PROM
2764 (NOTE 1)
U76
0801
DAC from SH5
MOD. COUNTER
MODDIS
FROM SH1
MGSUSEL
GSMODEN from SH1
U86
JUMPER
(NOTE 2)
GSN To SH6 (MEM)
GAIN MOD. PROM ENABLE
GAIN MOD PROM ENABLED
74LS00
U97
GAIN MODULATION PROM
0805
U77
GAIN FROM 0806
U78
P/O RN14
3.3K
SELECT A
low = Select GAIN MOD PROM
NOTE 1
Alternate part is 2732
NOTE 2
IC U86 Deleted from Serial No. 301 and UP. (REF ECO #1)
COMPARATOR
U67
U68
74LS85
74LS298
U60
U61
LATCHED MUX
low = Select A
GAIN
To SH 7
(ADA)
GAIN LATCH
U57
74LS74
FRONT PANEL SWITCHES
PROGRAM
REVERB DECAY
S1
S3
RN9
RN10
RN12
33K
74LS86
U81
GREY CODE SWITCHES (JEAN RENAUD G16)
PROGRAM
REVERB DECAY
To SH's 1,3,4
To SH 4
from SH5 (TIM)
TCB2
TCB1
DACX
LAST REV: 16 MAR 84
PCB rev Ø 11/13/83
323 (ADS)
SHEET 2 OF 12


WRITE ADDRESS COUNTER
74LS393
U82
U85
COLUMN
ROW
WC15
WC14
WC13
WC12
WC11
WC10
WC9
WC8
WC7
WC6
WC5
WC4
WC3
WC2
WC1
WC0
RN12
+5V
3.3K
U89
74LS04
S9-3
(TEST)
(DIP SWITCH)
ZERO WRITE ADDRESS TEST SWITCH
Close for zero write address
TCB7A
from SH1
TCB7
period = 31.25 usec
from SH2
P
PROGRAM
from SH1
PD
PREDELAY
toSH4
WC14
WC15-8
toSH4
ROW / COLUMN MUX
74LS158
U80
U74
G
SEL
WR7
WR6
WR5
WR4
WR3
WR2
WR1
WR0
TCB2
WRITE ADDRESS DATA (ROW/COL)
DELAY ADDER
74LS283
U70
U63
A7
A6
A5
A4
A3
A2
A1
A0
DD7
DD6
DD5
DD4
DD3
DD2
DD1
DD0
ADDRESS
A
To SH6
DELAY DATA
DELAY DATA REGISTER
74LS273
U62
DELAY DATA
ROW CARRY OUT LATCH
+5V
PST
U50
74LS74
TCB1
From SH5
RAS
DELAY MODULATION PROM
0807
DELAY PROM
0808
27128 (NOTE 2)
U79
U69
from SH2
MC
MODULATION COUNTER
MC5 - MC12
MC5
MC6
MC7
MC8
MC10
MC11
MC12
J13
TCB7
TCB6
TCB5
TCB4
TCB3
TCB2
PD0
PD1
PD2
PD3
MOD
MODD
U94
74LS04
From SH5 (TIM)
From SH5
TCB
(TIM)
MODDIS FROM SH1
from SH5 (TIM)
TCB1
S9-2
(TEST DIP SWITCH)
RN12
+5V
3.3K
ZERO DELAY TEST SWITCH
close for zero delay
NOTE 1
Alternate Part is 2732
NOTE 2
Alternate Part is 2764 or 27128
27128 (16 P + 16 PD) jumper 1-2
2764 (16 P + 8 PD) jumper 1-2 or 2-3
LAST REV: 27 FEB 84
PCB rev 0
11/13/83
323 (ADS)
SHEET 3 OF 12


PEAK UPDATE LOGIC
from SH3 MOD
from SH5 (7IM) DAC
74LS08 U46
// COMPARE VALID
74LS08 U96
74LS00 U97
UPDATE PEAK HOLD LATCH (HOLD PEAK)
to SH2
20K R161
+5V
1N4148 D19
22uf C192
PEAK HOLD ONE-SHOT
74123 U98
T=113 milliseconds
NOTE 1 Alternate part is 2732
from SH6 (MEM) B 7-14 LEVEL 8
74LS85 U48
74LS85 U55
PEAK COMPARATOR
+5V PEAK LEVEL
PEAK HOLD LATCH
74LS374 U56
PEAK HOLD LATCH CLOCK
74LS257A U90
DISPLAY MUX
from SH2 P PROGRAM 4
from SH2 RD REVERB DELAY 4
from SH3 WC14 (LED BLINK ENB)
from SH1 SW SWITCHES 3
from SH1 PD PRE DELAY 4
74LS253 U91
74LS253 U92
BIT 1
BIT Ø
.5 millisec/digit
DISPLAY PROM
0809
2764 (NOTE 1) +5V
P/O J10
U99
DISPLAY DATA TO SH10
DISPLAY STATES TO SH10
DISPENB TO SH10
0.1 INCH JUMPER PATTERN
U83 LS74
DISPLAY MUX CONTROL LOGIC
period = 4.00 millisec
WC6 S2
WC5 S1
WC4 S0
74LS04 U94
74LS00 U95
74LS08 U96
from SH3 WC 2-6 WRITE ADDRESS COUNTER 5
LAST REV: 27 FEB 84
PCB rev 0 11/13/83
323 (ADS)
SHEET 4 OF 12



LAST REV : 27 FEB 84

323 DIGITAL REVERBERATOR (TIM)

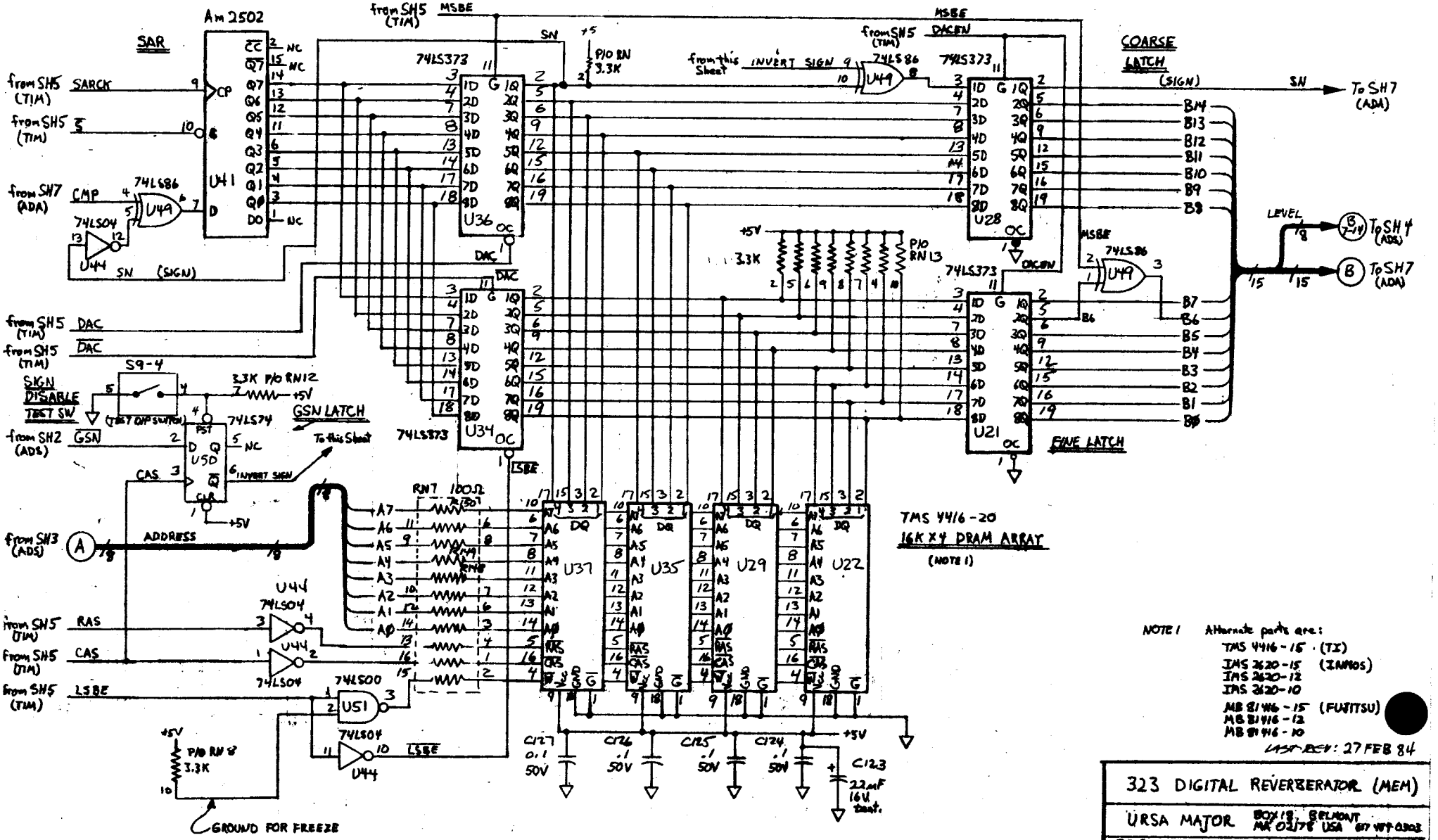
PC

REV	DATE	DRAWN BY	DATE
0	11/13/83	Mark Bruckner	11/11/83

URSA MAJOR INC.
BOX 18
BELMONT MA 02178 USA
(617) 489-0303

DRAWING NUMBER

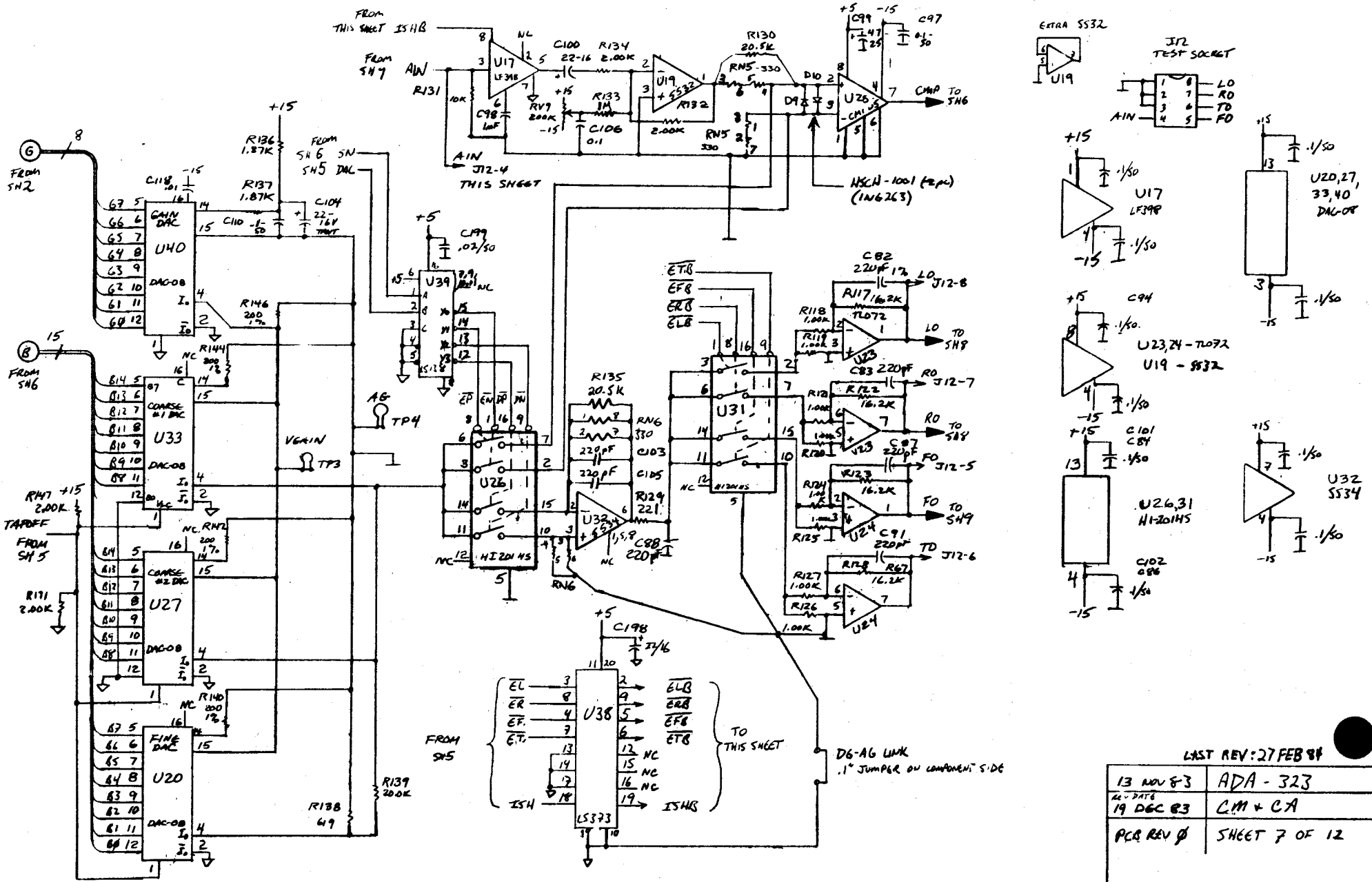
SHEET 5 OF 12



NOTE 1 Alternate parts are:
TMS 4416-15 (TI)
IMS 2620-15 (INMOS)
IMS 2620-12
IMS 2620-10
MB 81416-15 (FUJITSU)
MB 81416-12
MB 81416-10

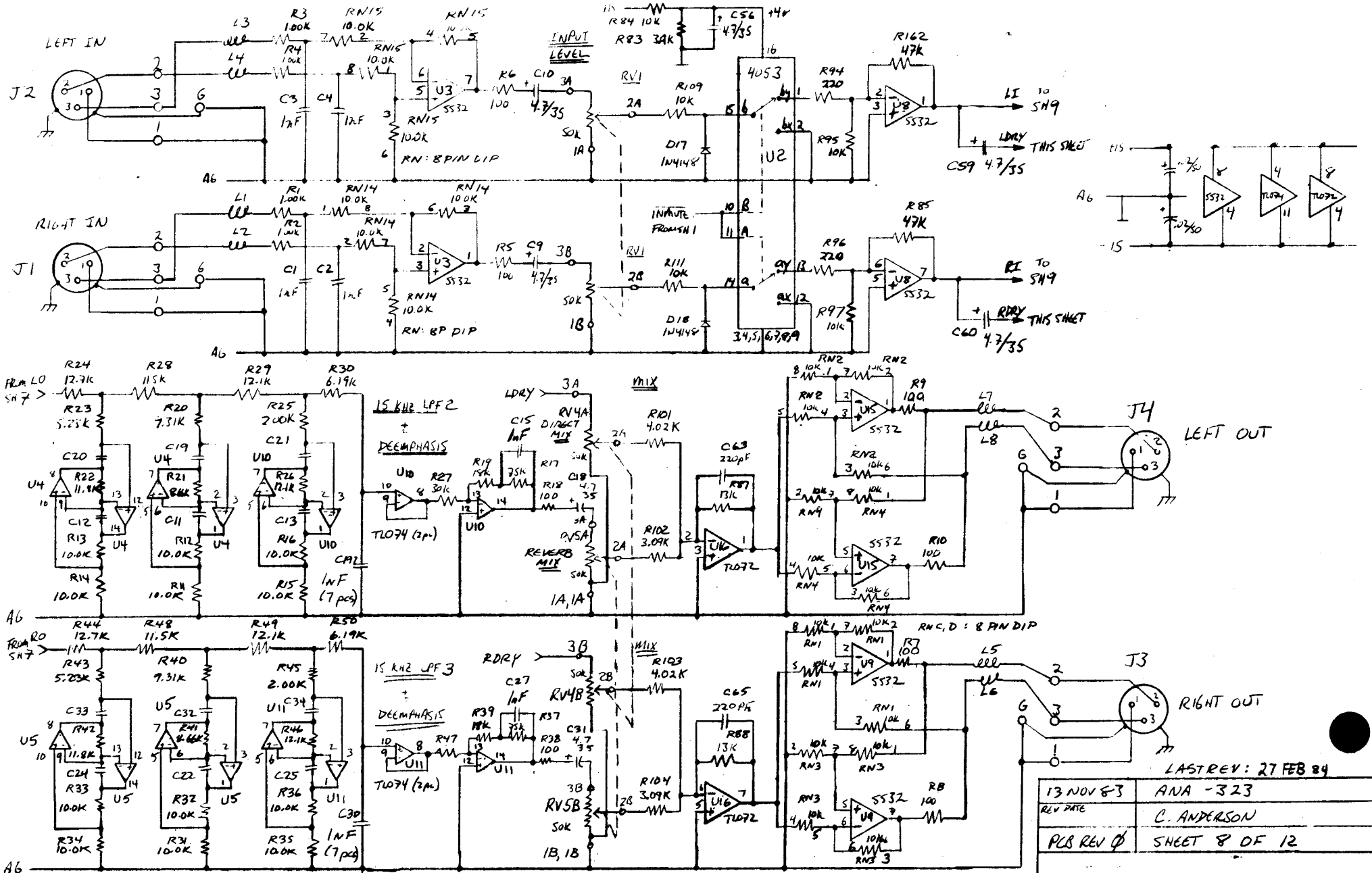
LAST REV: 27 FEB 84

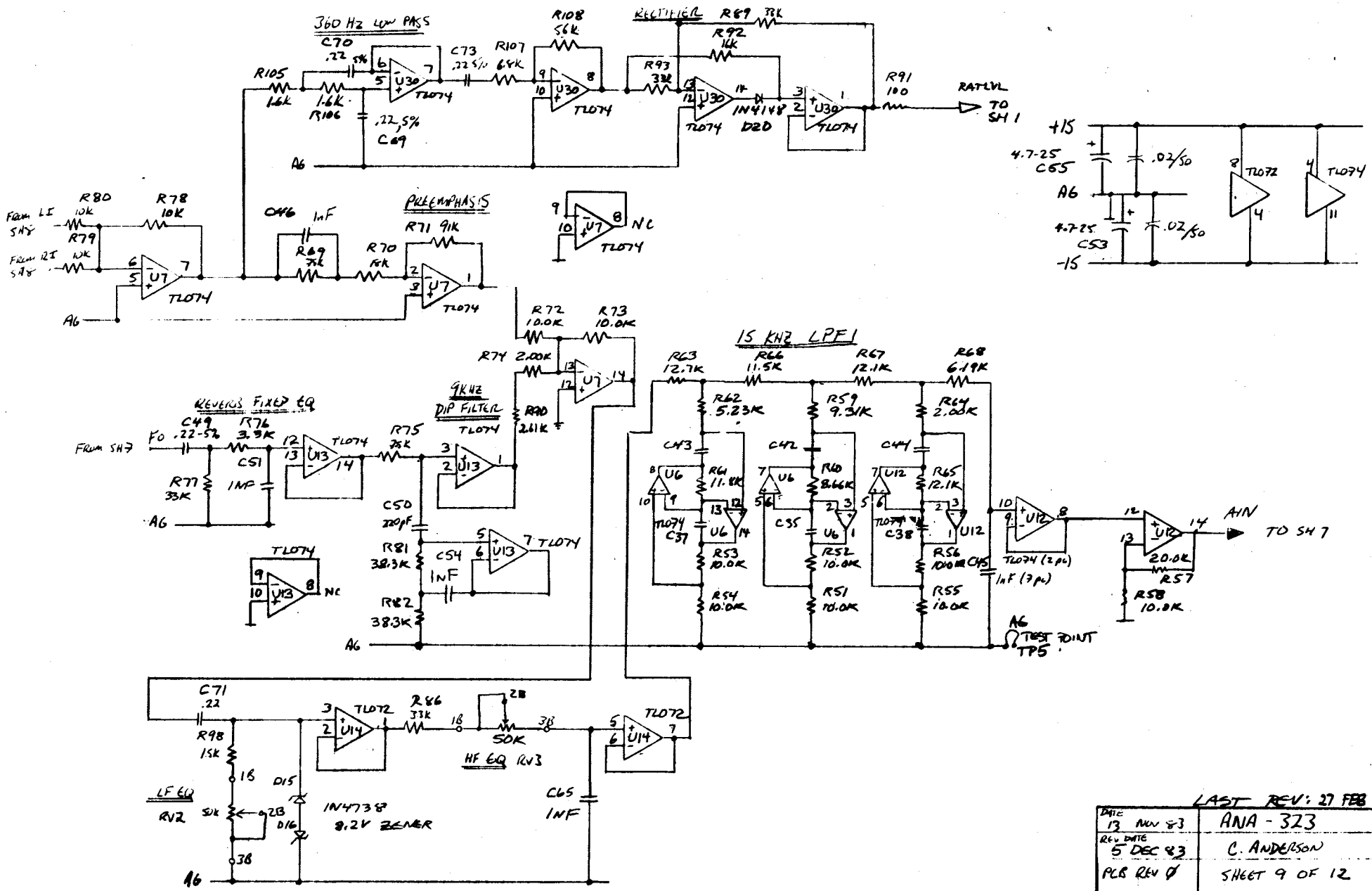
323 DIGITAL REVERBERATOR (MEM)	
URSA MAJOR BOX 18, BELMONT MA 02178 USA 617 489-0303	
ORIG 26 JULY 83 - CM	
PC REV 0 DATE 11/13/83	SHEET 6 OF 12



LAST REV: 27 FEB 84

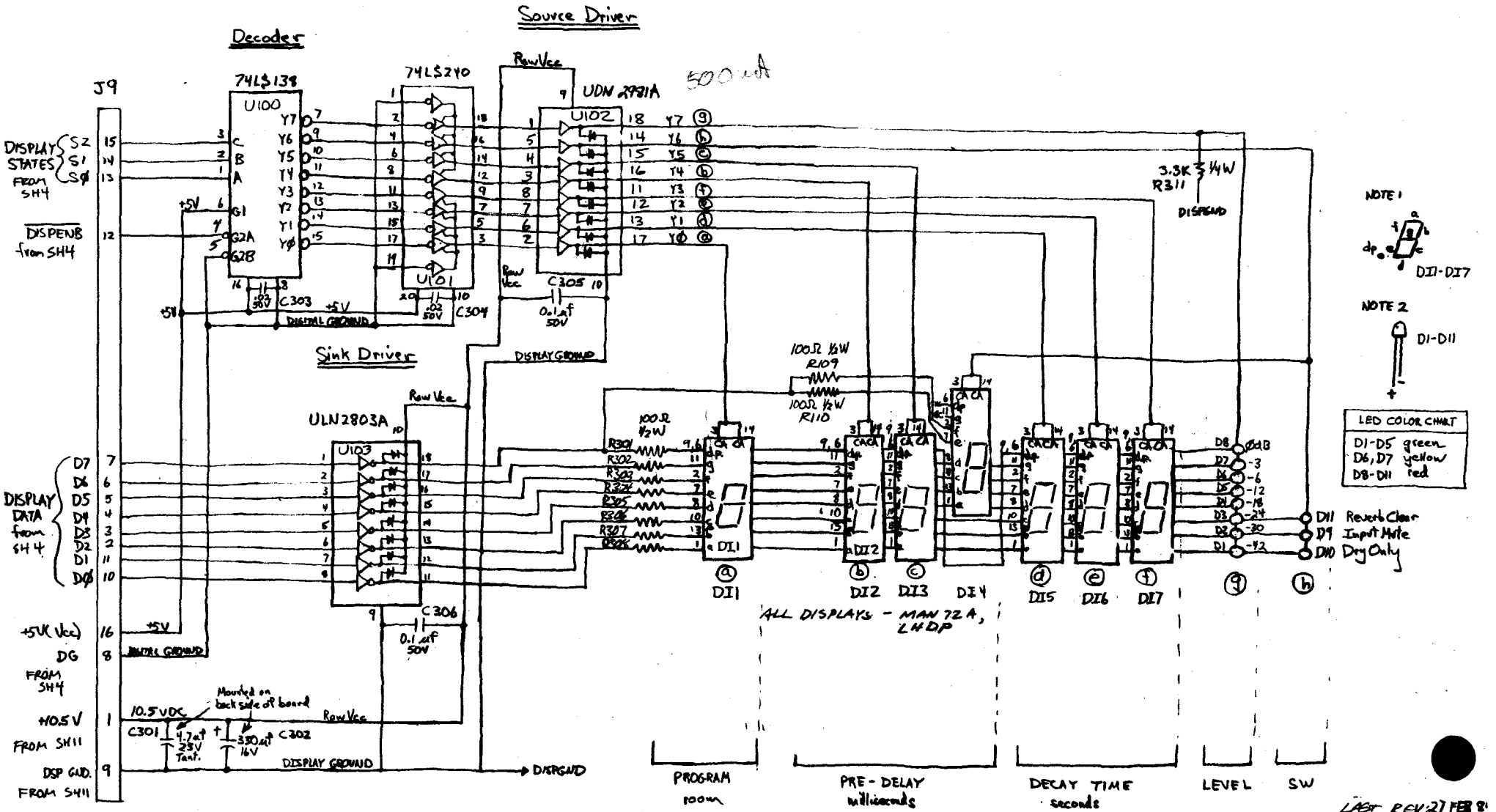
13 NOV 83	ADA - 323
REV DATE 19 DEC 83	C.M + C.A
PCB REV Ø	SHEET 7 OF 12

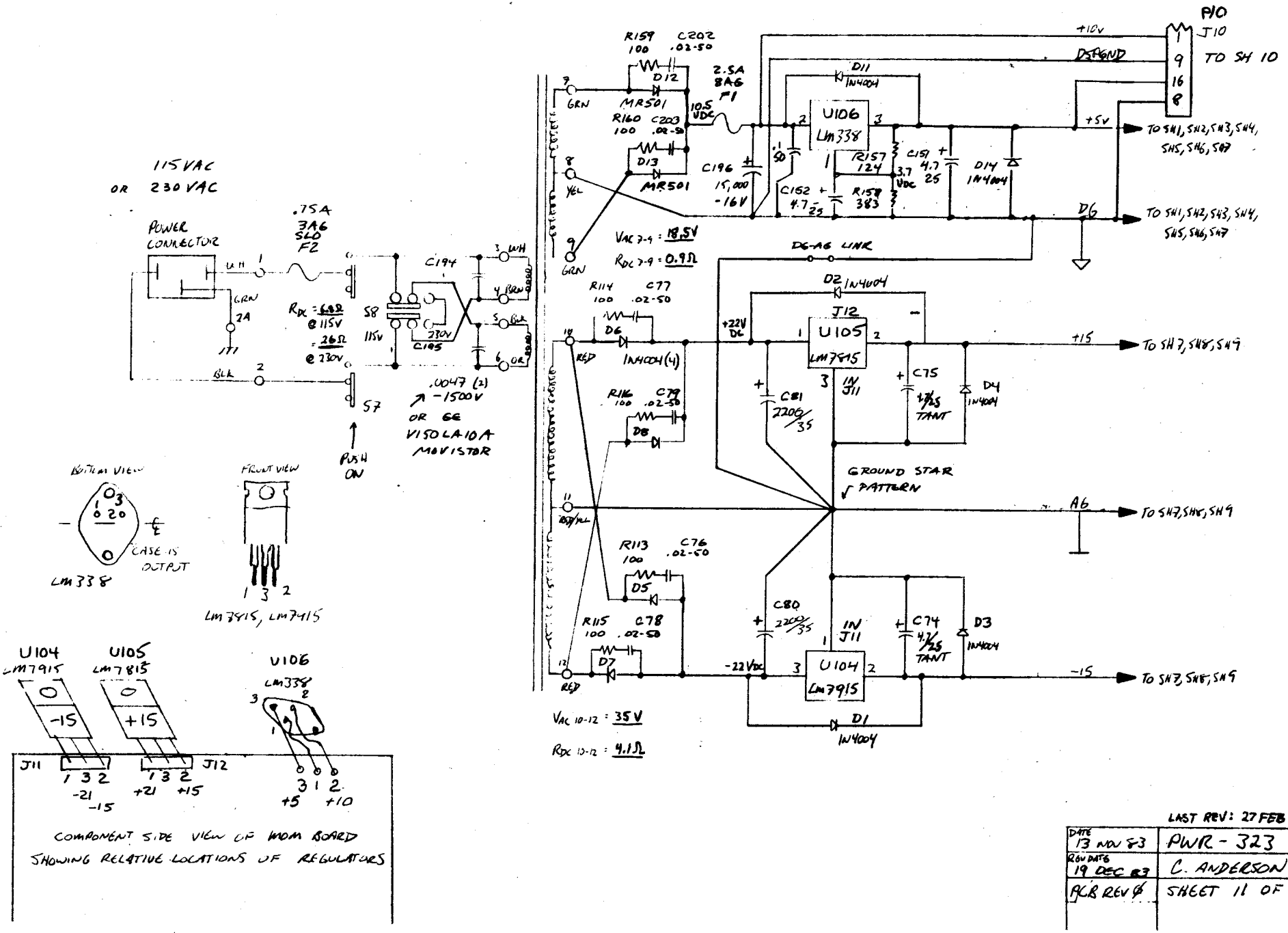

LEFT IN
RIGHT IN
J2
J1
INPUT LEVEL
RV1
4053
U2
TL072
5532
TL074
LDRY
RDRY
THIS SHEET
MIX
DIRECT MIX
REVERB MIX
15 KHZ LPF 2
15 KHZ LPF 3
DEEMPHASIS
TL074 (2pk)
LEFT OUT
RIGHT OUT
J4
J3
RN C, D : 8 PIN DIP
RN: 8PIN DIP
LAST REV: 27 FEB 84
13 NOV 83
ANA -323
C. ANDERSON
PCB REV Ø
SHEET 8 OF 12



LAST REV: 27 FEB 84

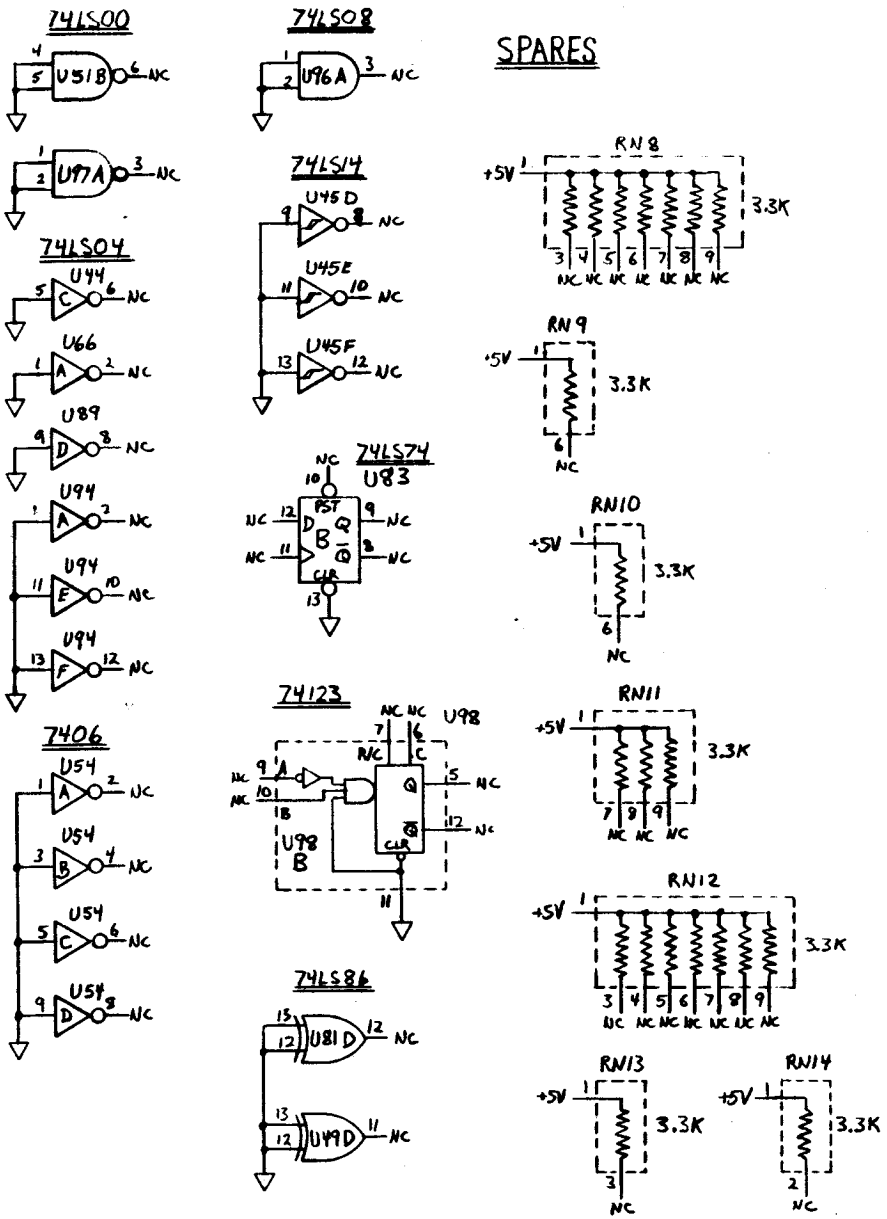
DATE 13 NOV 83	ANA - 323
REV DATE 5 DEC 83	C. ANDERSON
PCB REV Ø	SHEET 9 OF 12


Decoder
Source Driver
Sink Driver
J9
74LS138
U100
74LS240
U101
UDN 2981A
U102
ULN2803A
U103
DISPLAY STATES FROM SH4
S2
S1
S0
DISPENB from SH4
D7
D6
D5
D4
D3
D2
D1
D0
DISPLAY DATA from SH4
+5V (Vcc)
DG
FROM SH4
+10.5V
FROM SH11
DSP GND.
FROM SH11
10.5 VDC
C301 4.7uf 25V Tant.
C302 330uf 16V
Mounted on back side of board
C303 .02 50V
C304 .02 50V
C305 0.1uf 50V
C306 0.1uf 50V
R109 100Ω ½W
R110 100Ω ½W
R301 100Ω ½W
3.3K ¼W R311
DISPGND
DIGITAL GROUND
DISPLAY GROUND
Row Vcc
NOTE 1
DI-DI7
NOTE 2
DI-DI1
LED COLOR CHART
DI-D5 green
D6, D7 yellow
D8-DI1 red
DI1 Reverb Clear
DI0 Input Mute
D9 Dry Only
ALL DISPLAYS - MAN 72A, LHDP
PROGRAM room
PRE-DELAY milliseconds
DECAY TIME seconds
LEVEL
SW
PCB rev Ø 11/13/83
Mark Bowman
DISP - 3 BEAR SHEET 10 OF 12
LAST REV: 27 FEB 84



LAST REV: 27 FEB 84

DATE 13 NOV 83	PWR - 323
REV DATE 19 DEC 83	C. ANDERSON
PCB REV Ø	SHEET 11 OF 12



LAST REV: 27 FEB 84

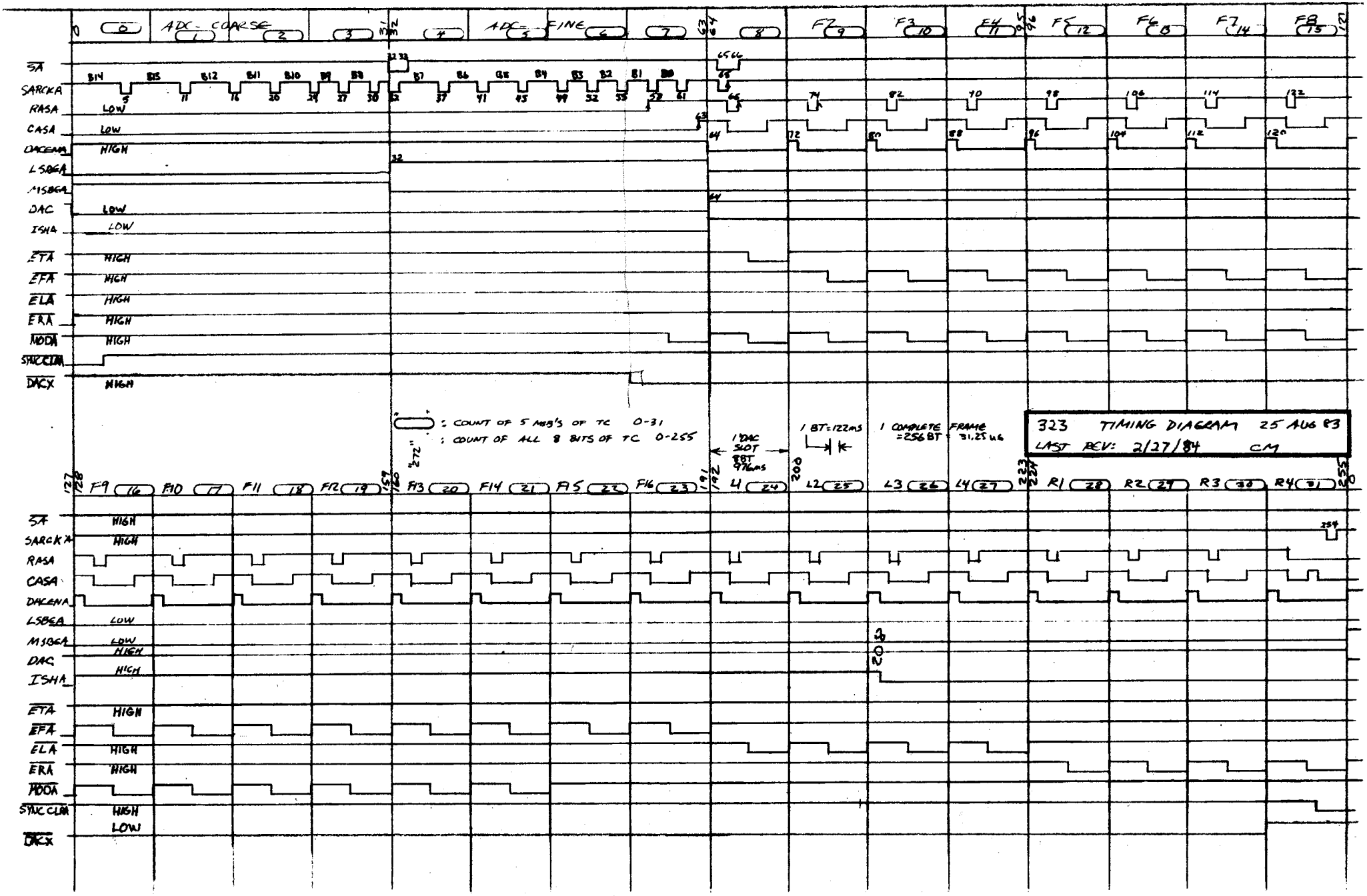
323 DIGITAL REVERBERATOR (SPARES)

PC REV	DATE	DRAWN BY	DATE
Ø	12/19/83	Mark Bruckner	12/19/83

URSA MAJOR INC.
BOX 19
BELMONT MA 02178 USA
(617) 489-0303

DRAWING NUMBER

SHEET 12 OF 12


ADC - COARSE
ADC - FINE
F9
F10
F11
F12
F13
F14
F15
F16
L1
L2
L3
L4
R1
R2
R3
R4
SA
SARCKA
RASA
CASA
DACENA
LSBEA
MSBEA
DAC
ISHA
ETA
EFA
ELA
ERA
MODA
SYNCCLM
DACX
LOW
HIGH
: COUNT OF 5 MSB'S OF TC 0-31
: COUNT OF ALL 8 BITS OF TC 0-255
1 DAC SLOT 8BT 976ns
1 BT=122ns
1 COMPLETE FRAME =256 BT = 31.25 us
323 TIMING DIAGRAM 25 AUG 83
LAST REV: 2/27/84 CM