THE URSA MAJOR 8X32

SERVICE MANUAL

Serial #:

URSA MAJOR 8X32
SERVICE MANUAL
NOVEMBER, 1983

REV - 0
PART #0754
PRICE: $25.00

URSA MAJOR, Inc.

Box 18, Belmont, MA 02178 • Telephone (617) 489-0303
Telex: 921405 URSAMAJOR BELM

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PROPRIETARY TECHNOLOGY

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IMPORTANT SAFETY NOTICE

THERE ARE HAZARDOUS VOLTAGES PRESENT IN THE 8X32 WHEN IT IS CONNECTED TO THE AC POWER LINE, EVEN WHEN THE POWER SWITCH IS "OFF". DO NOT DO ANY DISASSEMBLING, COMPONENT REMOVAL, OR PROBING INSIDE THE UNIT WHILE IT IS PLUGGED INTO THE AC POWER LINE.

8X32 SERVICE MANUAL: OUTLINE OF CONTENTS

APPENDIX A. RUNNING DESIGN CHANGES/FIELD SERVICE BULLETINS

I. GENERAL THEORY OF OPERATION

The 8X32 simulates both the reverberation produced in natural acoustic settings, such as concert halls, and that produced by other simulators, such as plates and chambers. There are many types of circuits in the 8X32, but this general overview will be limited to the actual sound processing circuitry.

The sound processor uses a bank of 16 kilobit random access memories (RAM's). That sizeable block could provide approximately 800mS of digitized audio were it used as one large memory. It is, however, subdivided into eight different smaller memory segments, each of which is isolated from the others. In this way, there can be eight different sounds in the 8X32 memory, each co-existing independently of the others.

The first and largest segment of the memory is the multi-tap portion, called MT. The MT segment has to be written into once every sample. Like every other memory segment, it has one input. MT has, however, twelve taps which are subdivided into various groups, with each group used in a different way in the reverberation process.

The first two taps are called Early Reflections. These taps are connected to an internal stereo mixer which receives the two signals and makes them available to the output as ERL and ERR, where they create the earliest part of the reverberation sound.

The remaining 10 taps on the MT segment are used in two groups. Five odd-numbered taps (M5, M7, M9, M11, M13) go to a mixer and develop a left-channel multi-tap signal IRL. The even-numbered taps (M4, M6, M8, M10, M12) are fed to another mixer and form the right-hand channel multi-tap signal IRR. IRL and IRR are sent to the output and are part of the total sound heard by the user. They are also fed into a third mixer and combined to give the signal IR. IR is, therefore, the sum of ten time delay signals derived from the input, each of them with a different time delay, amplitude, and polarity.

By this point in the process, the 8X32 has synthesized the early parts of the reverberation, Early Reflections and Initial Reverberation. These twelve discrete repetitions of the input sound simulate first reflections from the walls of a room, or the first few occurrences of echoes in a plate reverberator.

The remaining seven segments of memory are used to synthesize the decay portion of the reverberation. The 8X32 can produce up to 20.0 seconds of decay time from its 800mS of total available memory. It achieves this through a technique of putting signals into memory, extracting them after time delay, and recirculating them. In this way they continually loop back and forth and gradually die out. One hundred milliseconds of memory can produce a decay time of 20.0 seconds if the sound is allowed to recirculate 200 times.

IR is fed forward to a segment of the memory called the All Pass (AP). The AP has one input and one tap. Sound from the one tap, after a delay, is fed back into the input of the AP with a specified gain, and is also sent on as the APO (All Pass Output) signal. APO is a mix of a 6mS signal and the input signal, IR.

The AP's function is to increase echo density without changing frequency response. Gains are adjusted to produce flat frequency response. The AP adds no significant time delay as the echo density is increased.

The 8X32's six remaining segments of memory are the comb filters, which are abbreviated as C1-C6. The comb filters are identical circuits except that each of them has a different built-in time delay. Each of the comb filters takes APO, delays it, attenuates it, and feeds it back to the segment's input. The signal will then decay at a rate dependent upon the amount of attenuation.

All six comb filters receive the APO signal but each comb feedback tap (CF1-6) recirculates the emerging signal only to its particular memory segment. This strategy helps create a more complex reverberation pattern.

Besides the CF, each comb segment has two more taps, one left and one right, with which to audition its own reverberation. The left and right stereo mixed signals, CL and CR, are fed to the output of the 8X32 and form the decay, or true reverberation, portion of the sound produced. CL and CR each receive six taps. CL receives all the left audition taps from the comb filters (CL1-6), while CR receives CR1-6.

So, as is indicated by the front panel designations, the reverberation produced by the 8X32 has three components. The first two short taps coming from MT produce the Early Reflections. The other ten taps from MT are combined in groups of five to create left and right signals for Initial Reverberation. The decaying, true reverberation component of the final output sound is produced by the comb filters, with a boost in the echo density provided by the All Pass Filter.

The user modifies the characteristics of the reverberation produced by the 8X32 with the front panel controls. The LED displays allow him to monitor the settings operating in the machine at any given time. Plus (+) and minus (-) nudge buttons control Level and incremental delay (indicated by mS) for both Early Reflections and Initial Reverberation. The Level controls determine the amount of gain given the signals, and, therefore, the proportion of their contribution to the output sound, with a display of 1 representing the least, and 8 the greatest proportion of the mix. Up to 98mS of delay can be added to that built into the Program in use by operating the mS nudge button. This allows the user to control when each component of the reverberation begins.

The decay time (RT60, or time to decay to -60dB) is controlled by another set of nudge buttons. Decay time is adjusted in the 8X32 by changing the gain of signals circulating through comb filters. Signals given large gains linger over a longer period of time.

Reverberation dies out not only as a function of time, but as a function of frequency. Each of the 6 feedback taps has a high and low frequency attenuator. By increasing high frequency attenuation, the high frequencies die out more rapidly and are muffled. The Front Panel provides 4 discrete values that can be adjusted from 8kHz, which is relatively flat, to a great deal of roll-off, as low as 1kHz. This function of the 8X32 acts like a treble control, except that it modifies the reverberation decay time, not just the character of the sound. The LF Decay controls modify low frequencies in much the same way. Both the HF and LF decay controls leave the midband portion of the reverberation unaltered.

All the adjustments described above are made to the built-in delays of the selected Program. The design engineer has chosen each set of delays to approximate the reverberation range designated by the Program name. As we have seen, the user can modify reverberation characteristics within a Program, but there remains a dramatic change going from one Program to another.

II. OPERATION OF THE CIRCUITS

The following descriptions of the circuits in the 8X32 and how they operate refer frequently and specifically to the schematics and diagrams in Appendix C. Please turn to the appropriate drawings and use them as you go through each sub-section devoted to an individual PC board or type of circuitry. All chip numbers refer to the board being described unless the text specifically indicates another

II. A. MOM-2

II. A. 1. Power Supply Circuits (Sheet 4 of MOM-2 schematic): The right-hand section of MOM-2 is devoted to the seven power supplies of the 8X32. The 8X32 features a 6-segment display (U44) soldered into this portion of the Mother board. You can easily see the display through the top cover louvers. Each segment indicates the status of one of the power supplies. The display should read "+1." if all the supplies are working properly. Refer to the silk screen on the PC board for the coding of the power supply voltages to the different segments. The seventh power supply (-5V) is not indicated on the display. See Section III.D.4. for a comprehensive procedure to check each supply, including -5V, for proper voltages.

The incoming AC voltage is fed through two fuses and both sides of the line are switched by the main power switch on the front panel. A voltage selector switch, located on the lower right-hand corner of MOM-2, can put the two transformers' primary windings in parallel for 115V or in series for 230V operation.

Three different secondaries are used to develop the regulated power supply voltages. The +5 power supply is regulated by an LM338 regulator on the back panel, which is capable of putting out about 2½ - 3 ampheres. An SCR is tied across the output of this power supply in a crow-bar circuit. If over-voltage should occur, the SCR will go into conduction and short circuit the +5V supply, keeping it from rising enough to burn out integrated circuits. In such a case, the 5-amp fuse (F3) should blow as an added safeguard.

Another winding develops the +15, -15, and the +12V supplies. You should note that the +12V supply is only used by the RAM's. A third secondary winding produces the +7½ and -7½V supplies. All the regulators function in roughly the same manner, with fixed-value adjustment resistors which cannot be altered by the user.

The -5 substrate bias for the RAM's is derived from -7½V with a Zener diode and a resistor. This -5V supply is connected to the gate of Q1, a transistor connected to the 12V regulator. This circuit is intended to shut down the 12V to the RAM array should the -5V supply drop to zero (0). This will preserve the RAM's in the event of power failure.

There are actually two other voltages coming from the power supply area of MOM-2. One is called raw VCC (raw +5), or approximately 9.3V DC, depending upon the schematic. Among other places, this

voltage goes to the front panel board (PAN-1), where it is used to light all the LED's. In units still using REV-1 CPU-1, +9V is used to develop a 5½V power supply for memory operation.

The REV-1 CPU board also made use of approximately 8V AC taken from the secondary of the 7½V power supply winding. The REV-2 CPU-1 does not observe this 8V supply, which was used as check against power failure.

There are no special troubleshooting techniques for the power supplies. If you suspect a problem, check the 6-segment display and then test the various voltages as described in III. D. 4. These are straightforward, 3-terminal voltage regulator supplies. AC voltages and critical unregulated DC voltages are indicated on the schematic.

II. A. 2. Timing Circuits (Sheet 1 of MOM-2 schematic): The timing circuits on MOM-2 deliver the control signals to the rest of the 8X32. Timing for the machine is based on a high-frequency crystal oscillator, operating at 10MHz and divided by a series of counters. The finest timing subdivision used is 100 nanoseconds. A complete frame, or sampling time, is composed of 512 of these bits. Thus, the sampling frequency is approximately 20kHz.

The timing chain outputs TC0-TC8 are fed to three different PROM's (U26, U27, U15), which are used as look-up tables to deliver the timing and control signals. All the timing signals are latched by flip-flops (U5, U6, U25, U28) controlled by the crystal oscillator so that they are in synchronization. A few variations and special signals, such as $\overline{\text{ILCK}}$ and CPC, are derived with gates based on the timing counter inputs and some of the PROM outputs. Crucial timing signals are shown in Section IV. #1-5.

A possible source of trouble in this portion of the machine is a faulty crystal oscillator. An unstable crystal oscillator will not maintain a steady frequency and the 8X32's output will exhibit anomalies of pitch shift, wow and flutter, or, possibly, distortion. To check the crystal oscillator, connect a scope probe and observe a signal such as G (MOM-2/U3/6) on an oscilloscope. Triggering from the signal itself, put about ten or fifteen of the sqaure wave periods on the oscilloscope face and watch the scope display for a while. Concentrate especially on the later square waves, the ones on the right-hand edge of the scope. Because the scope is triggering on the left, those square waves will always be sharp. Crystal jitter can, however, show up as fuzziness on the right portion of the screen.

Other troubleshooting of the timing circuits is relatively easy, since virtually all of them are independent of the rest of the machine. Exceptions to this, however, are some of the signals coming from U27 and U28, which are dependent upon the value of a signal called RNG. RNG is determined by the first A-D conversion test done for each of the eight memory segments. If RNG's value is zero (0), it will select one set of clock signals from U27. If its value is one (1), it will select a different stream of signals. This affects

the signals SAR1CK and SAR2CK and involves TESTB5, TESTB6, and TESTB7. With no signal input into the machine, RNG should always be set to zero (0). When the signal rises to the point that the -36dB LED comes on, some of the A-D conversions will be done with RNG equal to one (1). The use of RNG permits a slower, more accurate A-D conversion for small signals.

II. A. 3. Address Circuits (Sheet 3 of MOM-2 schematic):

II. A. 3. a. Address generation for RAM's - The circuits in the upper left of the MOM-2 ADS schematic sheet generate the read and write addresses for the RAM's. In each 51.2uS sampling period these circuits will generate the eight write addresses needed to store the results of the eight A-D conversions, and they will generate the thirty-two read addresses used to read data back from the memory segments. Furthermore, these circuits compute a row and a column address for each read or write address. (All the circuits used for the address computation and storage operate on bytes of data 7 bits wide, one byte of data for the row address, one byte for the column address. The values are computed in sequence.) Thus, in each time frame, the machine is actually doing eighty address computations.

The sampling period is divided into eight major subdivisions, during each of which an A-D conversion is completed and the results are stored in memory. Within each of those eight subdivisions, four different addresses for reading taps from RAM are computed, one-at-a-time, and the sequence is completed by the computation of a write address used to store the results of the simultaneously performed A-D conversion. Binary information determining which memory segment is to be written into is derived from TCB8, TCB7, and TCB6 coming into U9. These bits assume the values 0 - 7 throughout the frame. Signals PN2, PN1, and PN0 coming into U9 tell the address logic which memory segment to use for a read operation.

The address generation circuits operate in a feedback loop that can be difficult to trouble-shoot. A description of the loop should help. Starting at the end of the chain, U12 and U71 are scratch-pad RAM's (LS189's) that store the last write addresses computed. The results of the last write address are fetched from these two memories and, as the schematic shows, are brought into the adders, U21 and U46. (These signals are called CP6-CP0. CP stands for Current Point, or current point in memory, where write is to take place.) U21 and U46 create the new address by subtracting 1 from the old address. This is accomplished by setting the other adder inputs to one (1). The decremented write address is then passed through U34 and U48. From there it is fed into comparators U33 and U47, which compare the newly-computed write address to the minimum bottom value allowed for that memory segment. That minimum is retrieved from the PROM U20. As long as the new write address is not below the minimum value, it is used directly, passed on through U35 and U49, and latched into the registers U36 and U50. If, however, the newly-computed write address is below the bottom of the memory segment, the PROM U22 is activated to provide a data word, LP0-LP6, which will be added to the

erroneous write address in U35 and U49 to pop that address to the top of the segment. In this way we have implemented a down counter which decrements from the top of the memory segment to the bottom, and then wraps up to the top again.

The outputs of U36 and U50 go to 2 different places. The complement outputs are fed into the scratch pad RAM's (U12 and U71) and stored there to replace the previous current point value. The non-complemented values are fed directly to the 16K RAM's (MOM-2/U51-U64, see sheet 2, MEM, of MOM-2 schematics) and used as the row and column addresses. Between the row and column address operations, any carry-out that might have occurred from U21/10 is stored temporarily in a flip-flop (U1) and used as a carry input when the column address, the more significant byte, is computed next. In this way a 14-bit wide counter is implemented in two passes through a 7-bit wide data path.

The operations for the read address are similiar. First, the last value used as a write address for the memory segment is fetched from the RAM's U12 and U71 and applied to the adders U21 and U46. Now, however, the delay PROM U10 is activated by pulling its pin 15 to ground, and the correct time delay value, in binary form, is retrieved from this PROM, added to the last write address to form a read address, and passed through U34 and U48. U48 is used to add a time delay value if this is an early reflection (ER) tap or an initial reverberation (IR) tap. If the user has selected a non-zero delay time for those functions, the value appears at the other inputs of U48, on signals ERID0-ERID3, at the appropriate time for the taps that need it. The output of the adders, U34 and U48, is again checked by comparators, U33 and U47. This time the check ensures that the read address just computed is not greater than the top of the memory segment, it will be corrected by retrieving the negative of the length of the segment from U22 and adding that value, so that it pops back down to the bottom. Finally, the read address is latched in U36 and U50 and is available for use in the RAM. Again, a row address is computed, carried out, and used in the succeeding computation of the column address.

For further assistance on troubleshooting the address logic see the discussion of the test feature ADST (Section III.D.5.b.).

II. A. 3. b. Gain generation for the DAC's on ANA-2 - MOM-2/U85 and MOM-2/U86 are used to produce the gain values needed by the multiplying DAC. U85 is a PROM whose various inputs change in response to Program and Decay Time settings on the front panel to provide the gains needed for each of the 32 taps. U86 is a simple latch used to hold the results.

II. A. 3. c. Storage of Reverberation Parameters - A series of latches (LS374's) and an LS670, all shown on the right hand portion of the MOM-2 ADS sheet, are used to hold values provided by CPU-1. These values are the reverberation parameters and cause the machine to alter reverberation according to the user's settings.

An 8-bit data bus called CPUB, signals CPUB0-CPUB7, comes from the CPU board and feeds the input of these various latches. To load the values into these latches, the CPU sends a signal (PLE, PLE2, or PLE4, etc.). These signals are all very brief, difficult-to-observe pulses that occur infrequently and cause the new data to be latched into the appropriate register. From U74 and U75 values go off to ANA-2 that are used for the High and Low Frequency Decay setting, and, also, the level settings for Early Reflections and Initial Reverberation. Program and Decay Time bits are also latched by these circuits and are used in the ADS circuitry.

II. A. 4. Memory Circuits (Sheet 2 of the MOM-2 schematic)

II. A. 4. a. A-D Conversion Circuits - U41 and U42 are 8-bit successive approximation registers (SAR's), used in conjunction with some gates to control the successive approximation A-D process. During an A-D conversion, the signals from U41 and U42 are steered through transparent latches, LS373's to the appropriate DAC. During the eight major subdivisions of the sampling time, the two DAC's alternate function as A-D and then D-A converters. U91 and U89 are transparent latches that steer the SAR data to A-D converter #2. U81 and U79 are transparent latches that steer the SAR data to A-D converter #1. This steering is controlled by timing signals present at these registers (for example TC6, TC6, and TCB6).

The gates at the output of U41 and U42 are used to modify the test states that the SAR's would otherwise put out on their own. The most major modification is an initial test at 1/64 of full scale to determine the range bit RNG. If the signal is found to be below this range threshhold, i.e., a very small signal, conversion of the first five bits on U41 is skipped and the conversion jumps to the eight finer bits controlled by U42. A large signal will result in a signal range of one (RNG=1), and all thirteen bits will be tested and converted. By the end of the A-D period, the bits sitting at the inputs of the RAM's (MOM-2/U51-U64) represent the A-D converted value for the audio input signal. They are written into the RAM after the RAM has been given the correct write address, and after the signal RAMWT, which controls write operations into the RAM, has been set low. (See Section IV #11).

II. A. 4. b. Audio Data Storage Circuits in the RAM's - The output of the RAM's, that is, the pin 14 signals, are fed to the input of LS374 registers (U80, U78 or U81, U79). There are two sets of these registers, one for each converter, and they hold the data read from the RAM during the entire D-A period. The data from the RAM is available at the inputs to both registers. The timing signals, such as DACK1 and DACK2 and 2TCB6, are used to determine which of the LS374's will receive and respond to the data from the RAM's.

II. A. 4. c. Information Circuits to the CPU - The more significant audio bits are decoded by an LS30 (U39) and a small PROM (U38), and then latched by U82 and U84. The outputs of U82 and U84 are available to CPU-1 on the CPIR bus, CPIR7-0 (CPU Input Registers).

CPIR7-4 contains the level information of the MT segment, representing the audio input to the reverberator. The lower order bits, CPIR0-CPIR3, represent the highest signal level of the other seven memory segments. The registers U82 and U84 are updated every time a new signal level is higher than the one currently stored in the register, and they are initialized again each time the CPU reads the register CPIR. When the CPU reads CPIR, it sends out a pulse, PLE5, to clear the registers and reset them. In this way the hardware gives CPU-1 an assist in capturing the peak signal level, no matter how short it may be, and the CPU receives the data and interprets it to light the front panel signal level displays.

II. A. 4. d. Troubleshooting RAM Noise Problem - The only common field failure connected to the memory circuits manifests itself in the Decay LED's flickering on and off with no input signal coming into MOM-2. This indicates a noise problem whose source is probably in the RAM array (U51-U64). The lowest numbered chip will produce the largest noise error. If the chips in your unit are made by National Semiconductor, check pin 14 of each IC for float with an oscilloscope. Float will be indicated by a straight line (no signal activity) between 2 and 3V. A normally operating 8X32 will show activity down to 0.0V and up to 5V.

II. B. ANA-2

II. B. 1. I/O Circuitry (Sheet 1 of ANA-2 schematics): The I/O sheet covers the circuits between the audio input and the first A-D converter input as well as those between the results of all the A-D's and the reverberation computation and the output. The sheet also shows the logic buffers.

II. B. 1. a. Input Circuitry - The audio input path begins with the XLR correction (J19) and runs through active differential input stages and a summer to combine them into one signal. That signal is subjected to the rear panel sensitivity adjustment and then goes through a sharp cut-off low-pass filter, implemented with U73 and U74. Aperture connection is provided by U74 while, at the output of that IC, a voltage divider knocks the signal level down to insure that the CMOS circuits at the A-D input will not be overloaded. On later versions of ANA-2 a trim pot adjusts the DC offset presented to the input of the MT segment of memory (MTIN).

II. B. 1. b. Output Circuitry - Two identical output signal paths are shown on the I/O sheet, one for the left and one for the right. Each begins with another 7kHz sharp cut-off, low-pass filter identical to the one on the input path and then proceeds through buffer stages into an active-balanced differential output. If they are fed to an unbalanced input, a short connection should be used to ground pin 2 to pin 1 at the XLR connector plugged into the back of the 8X32. This active output stage senses the status of its two different outputs and puts out the same voltage whether it is used differentially or single-endedly.

The signals ERL and ERR (Early Reflections Left and Early Reflections Right) appear at the top left-hand edge of the ADA sheet. The signal M1 is now set to 0 and not used. Therefore, ERL is simply the signal M2 and ERR is M3, both from the first main segment of memory. (M1 was used in the first version of the software for the 8X32). The next summers develop the Initial Reverberation left and right signals by combining 10 more M taps into two groups (See Section V. #22). Both groups are then fed to the output and into another summer down at the bottom of this column of circuits to develop the signal IR, or Initial Reverberation. The circuits represented directly below the Initial Reverberation on the ADA sheet develop the signals CL and CR by combining 6 left taps and 6 right taps, respectively, from the C segments of memory. These are the true reverberation signals fed into the output (See Section IV. #21).

The ADA sheet also details various connectors. J12 appears near the left center of the schematic and indicates the connector which carries the eight A-D inputs. J13 in the upper right corner details the connector through which the various feedback signals are passed on their way to the circuits on the FBC sheet. J17 also shows signals that are being passed through a connector, in this case a resistor network, on into circuits also shown on the FBC sheet, but with signals destined for the output.

II. B. 3. FBC (Sheet 3 of ANA-2 schematic): The feedback circuits appear on the left side of this sheet. Seven of the memory segments involve a time delay in which the output of the section is recirculated to the input. One of the segments is the All Pass, and the others are C1 through C6, the Comb Filters.

The op amp U69 is used to develop signals for the All Pass circuit. One of these signals is fed across the top of the schematic sheet through a programmable attenuator to a five-pole filter, and then buffered by U78 to provide the signals APO1 and APO2. These are the signals that feed into the reverberator, having come ultimately from the ten M segment taps. They represent a version of the input signal with greatly increased echo density. Field Service Bulletin 10 (See Appendix A), a noise reduction precedure for the 8X32, details some changes that have been made to the circuits on the FBC sheet, specifically a small amount of pre-emphasis that has been added between U69 and U70.

Down the left edge of the FBC sheet are six identical circuits feeding between, for example, C1F and C1IN. These are feedback paths that alter the signal that will be recirculated to create reverberation. C1F coming in from the left is the feedback tap on the segment C1. The gain of C1F has already been set by the multiplying D-A function and is always less than unity. The first circuit, consisting of the .22uF capacitor (C129), U58, and U55, constitutes a programmable low-frequency decay circuit which acts as a 6dB/octave low-frequency cut-off. C149 and U61 form a programmable high-frequency decay circuit which introduces high-frequency roll-off. The last op amp (U64) is used to combine the feedback signal with both the feed-forward signal APO2 and a small adjustable DC offset coming from a trim pot. The output C1IN ultimately goes back to the ADA circuit and into the A-D converter.

In the right hand center of the FBC sheet there are four identical circuits followed by some op amp summers further to the right. The four circuits, typified by U2 and U3, are used to control the levels of Early Reflections and Initial Reverberation for left and right outputs. These are programmable attenuators operating with eight steps of level attenuation and controlled by signals from CPU-1. The outputs of these level control circuits and CL and CR are combined into left and right signals called LDRIVE and RDRIVE. These are fed to the I/O sheet and through low pass filters to the output.

II. C. CPU-1

II. C. 1. Operation of CPU-1: CPU-1 is a small daughter board which sits on top of MOM-2 and provides microprocessor control of user memory, reads the front panel button settings, and lights the front panel displays. It sends user-set parameters off to the rest of the reverberator to determine the reverberation characteristics. It receives power and peak signal level information from MOM-2.

Two versions of CPU-1 have been shipped. The later board (REV 2) has a more sophisticated method of protecting user memory. REV 2 is also adaptable for use with the remote control, and, potentially is adaptable to an automated mix-down computer interface. To easily determine which version of CPU-1 is operating in your machine, remove the top cover and check CPU-1/U19. The first version will have an empty 40-pin socket at that position. In the second version, a WD2123 will be inserted in the socket. Since most of the circuits are identical, one discussion will cover both boards.

The clocking signals for the CPU* come from MOM-2. This fact makes the operations of CPU-1, at least to the extent of the fundamental clock rates, synchronous with the rest of the machine. There is no local crystal oscillator, except for the UART. This CPU* is an 8085 single chip microcomputer, located at U3 on CPU-1.

CPU-1 is organized as a dual-bus system. Referring to the CPU-1 Block Diagram you will see an address bus and a data bus. The data bus interacts with program storage in two E-PROM's (U7 and U8) and with a CMOS RAM (U5, U6), used for both the user register memory and for scratch pad memory requirements of the 8085 beyond its internal scratch pad. On a REV 2 board, the data bus also sends and receives information to and from the dual UART (U19), which interacts with a remote if one is connected. The data bus sends and receives data from the 8279 (U20), which is the keyboard and display controller chip. The 8279 is the CPU-1 interface with the PAN-1 board. A buffer (U11) brings data in from the CPIR bus for input level and reverberation level use. A latch (U14) sends data to MOM-2 to control reverberation parameters.

*NOTE: CPU-1 is the printed circuit board. The CPU is the single chip at U3.

Because the user memory in the CMOS RAM's must be preserved at all cost, precautions were taken in both revisions of the board to ensure that data would never be corrupted or lost during power failure or switching power on or off. The REV 1 board accomplishes this with a one-shot which checks the 8-volt AC signal. When it determines that a certain number of cycles of the AC line are missing, as, for example, when the power dies or the AC switch is shut off, it removes the signal PWROK and inhibits the operation of the user RAM.

In the later version, the power supply observation is more sophisticated. REV 2 units first monitor the raw +5V supply and determine if it has gone to less than 7-1/2V. If this is the case, the 8085 has time to finish any pending operations using the CMOS RAM, and waits to see what happens next. If the detector on the 5V supply indicates that +5 has also begun to drop and has reached 4.75V, then the 8085 is completely disabled and waits until the voltage rises again. In any event, it has protected the CMOS RAM by opening switches that send the Chip Select and Write Enable signals (CS and WR) into the CMOS RAM's.

On the REV 2 version of the board, there is a Western Digital 2123 UART (U19) that works with RS232 send-and-receive buffers (U22, U23). U23 is used to interact with the remote control, while U22 is a spare to be used in the future to interact with an automated mix-down system.

A large 24-pin connector (J5) receives signals from the panel board (PAN-1). This is almost completely a connection of 8279 pins from U20 to PAN-1.

II. C. 2. CPU-1 Troubleshooting Suggestions: A machine that loses its memory at power-up or forgets at any time may have a CPU problem. Other indications of a failure somewhere on the board are no front panel display at all, or nothing happening when the front panel buttons are pressed, or, perhaps only some of the displays and controls on the front panel working.

Each version of the CPU board has a different way of indicating that the unit has a memory problem. REV 1 boards show "00" in the Register display window and show "E"s across the Early Reflection, Initial Reverberation, and Decay Time display windows. REV 2 boards show ".bd." in the Register window. If your unit has a memory problem test the lithium battery and make sure it is producting 3V. If you have a REV. 1 CPU-1 and the cause of the memory failure is not the battery, or if you have another problem that you have isolated to the CPU-1, you should contact the factory and trade the REV.1 board for a REV. 2. URSA MAJOR policy is to replace a REV 1 CPU-1, subject to availability, without charge. You will need a REV 2 board should you ever wish to use the 8X32 with a remote control.

If your unit is ignoring the front panel controls or the front panel shows nothing at all there is a series of checks you should make to isolate and locate the problem:

i. Make sure that CPU-1 is receiving the +5V power supply.

ii. To isolate the problem to the CPU, check the following probe points for activity to ensure that the indicated signals are reaching CPU-1 from MOM-2 - TICK at U3/7, TCB1 at U3/1, CPC at U9/9 and RAMWC at U25/13.

iii. If those signals are coming into CPU-1 properly, the next step in factory procedure is to pull the 8085 CPU chip at U3 and swap it for one that works. If that option is not available to you, scan the address lines coming out of U3. Tri-state these address signals (from U3/12-19, U3/21-28) and you should see activity at all three levels. Also check to make sure that you are getting a high signal from U3/36.

iv. The WD2123 UART at U19 should be swapped out if the machine will not power up. The WD2123 can be removed after the 8X32 has reached full power without changing the operation of the machine much at all. If, however, the chip is missing or defective, power-up will be halted.

v. The 8279 at U20 is the interface with PAN-1. Make sure that the clock signal CLK is coming into U20/3. Also check to see that the signal 79INT emerges from U20/4 and reaches its destination at U3/8. 79INT goes high when a front panel button is pressed and is then reset by the CPU chip. If 79INT is not reset, the machine freezes.

If the machine powers up and responds to some of the front panel controls but some segments are out or some of the buttons do not work, try swapping out the chips at U20 or U79.

Memory problems that are present when the battery is functioning properly might be caused by the EPROM's at U7 and U8. There is some history of field failure for these IC's, though the 2716's used in early machines were far less reliable than the 2732's used now.

Remember that CPU-1 problems will not manifest themselves in subtle effects on the algorithm - no noise, no pops, no unwanted variations in the reverberation produced by the 8X32. A failure on the CPU means that you will not be able to use the machine properly in quite obvious ways.

II. D. PAN-1

II. D. 1. Multiplex Display and Drivers: The display drive is done in a multiplex scan mode. The 8279 on CPU-1 sends down the segment drive information to U1. U1 buffers the information and steers current from the raw +5-volt supply to the appropriate segments, through series-limiting resistors. One set of resistors (R9,R10,R13,R12,R15,R14,R11, R1) determines the current levels through all the discrete LED's on the display, and another set (R8,R7,R5,R6,R4,R3,R2) determines current through the 7-segment digit displays. The cathodes of all these LED's and digit displays are brought down, and are, in fact, 15 different signals which go to cathode drivers U4 and U5 (these are buffers which sink current down from the cathodes, into the ground). The cathode drivers are selected one-at-a-time via the 4-bit, 1-of-16 decoder, U3. The information to appropriately drive U3 also comes from the 8279 on CPU-1. The sequence of operations is to first set the correct segment drive information into U1, and then to turn on the appropriate cathode driver at U4 or U5 so that the correct display is activated. (See Section IV. #25, #26.)

II. D. 2. Keyboard Matrix: All the push-buttons on the front panel are arranged as part of a keyboard matrix. Scan lines KR7-KR0 go low when the user closes a button connecting it to one of the signals KS0-KS4. The signals KS0-KS4 are set low one-at-a-time via a decoder (U2), under commands from the 8279 on CPU-1. This is a time sequence scanning method whereby the common line of the switches in one column is set low and the CPU determines if any of the scan lines goes low. PAN-1 receives raw +5 volts from MOM-2 and +5 volts itself from CPU-1 via the ribbon cable.

II. E. The Remote Control

II. E. 1. Power and Signal Transmission From and To the Mainframe: The 8X32 hand-held remote control is connected to the mainframe via a D connector at each end, and a 4-wire cable shielded in two groups. The heavier wire pair sends raw +5, that is, about 9 volts DC, and digital ground to the remote. The smaller pair of wires provides data transmission to the remote and from the remote back to the CPU. In the remote, the +9 volts sent from the mainframe is treated by voltage regulators, one of which drops the 8 or 9 volts received down to +5 for use as the power supply for most of the IC's. A pair of voltage regulators (ICL7660's) take the +9 volts and turn it into an inverted, regulated voltage at about -8 or -9 volts. The bipolar +9 and -9 volts are used by the RS232 transmitter that sends data from the remote back to the mainframe.

II. E. 2. REM-1: The remote contains two printed circuit boards. REM-1 is visible after you have removed the back cover of the remote. All of the active circuitry in the remote is arrayed on REM-1. REM-1 has a UART type 6402 which receives data from the CPU

and controls the transmission of data back up to the CPU. The other large circuit on REM-1 is an 8279 like the one on CPU-1. The 8279 on REM-1 scans the keyboard on PAN-2, reads it for activity, and steers segment and cathode drive currents to the 7-segment and discrete LED displays. A 4712 provides a local baud rate generator to control the UART. Various random logic circuits and gates manage and arbitrate the communications with the main unit.

The other PC board in the remote control is PAN-2, which holds only resistors, displays, and push-buttons.

III. TROUBLESHOOTING, TESTING, AND CALIBRATION

III. A. Test and Troubleshooting Equipment

You will need, at minimum, a good dual-trace scope (25MHz or, preferably, better), with an external trigger. Also useful would be a low-distortion audio oscillator, a distortion analyser, an audio volt meter, and a DVM. Clip leads, DIP clips, a 16-pin resistor network, and DIP switches (both 4 and 8 PST) would all be helpful.

A second 8X32 working normally is, obviously, a valuable tool. The second unit can be used as a reference and as a source of modules for swapping into the defective machine. If the the MOM-2 circuits seem to be functioning properly in the problem 8X32, then it is often helpful to swap an ANA-2, CPU-1, PAN-1, PAN-2, or REM-1 module temporarily with the good unit. One hopes that this will help isolate the problem to one module. In that case, you can compare signals in the two units to isolate the problem further.

III. B. Disassembling Instructions

III. B. 1. Removing top and bottom covers: Both the top and bottom covers of the 8X32 are held on by 11 screws. To remove either cover, remove the screws and then gently pry the cover free. After removing both, you will have access to the component sides of MOM-2 and ANA-2.

III. B. 2. Hinge on ANA-2: To gain access to the solder side of both MOM-2 and ANA-2, remove the following from ANA-2: the input cable at J19; the output cable at J20; the gain pot cable at J23; the five (5) 6/32" x 1/4" screws at H12, H13, H15, H16, and H17; and the three (3) stand-offs from SOA, SOB, and SOC. After all these parts have been removed ANA-2 will hinge forward, exposing the solder sides of both boards.

III. B. 3. Removing components with multiple leads: All the modules in the 8X32 have plated-through holes. When removing a component, use a vacuum solder remover to completely remove the solder from the hole. Component leads should be free and should wiggle easily before you try to pull them from their holes. Since all the IC's in the 8X32 are socketed, there are very few components with multiple leads that should have to be removed during servicing. If the need arises, however, be very careful that all leads are free before you attempt to remove an entire component. If you are really stuck, try to get a pair of diagonal cutters between the component and the top side of the board, and cut the component free, one lead at a time. Do anything to avoid damaging the board.

III. B. 4. Procedure for removing or replacing IC's: When replacing an IC or removing one from a socket, shut the power off to the 8X32. Failure to do so could damage the IC itself, or another IC associated with it, or even the power supply. IC's, especially the CMOS circuits which comprise some of the chips on ANA-2 and CPU-1 and are used

variously throughout the machine, are highly susceptible to static electrical problems and should be kept in conductive material like tin foil until use.

When inserting an IC into a socket, be careful that all pins are straight, that they engage the correct hole on the socket, and that each lead seats properly. If undue force is needed to seat the IC in the socket, you are probably bending a lead over and not getting it into its hole. Use a real IC extractor to pull IC's straight out, and thus keep all the pins straight. An inspection or dental mirror will help you sight between the IC and socket to check for bent-over leads.

III. C. Calibration

III. C. 1. ANA-2 - ADC offset adjustments: Set the 8X32 to "0.0" seconds Decay Time in the PLATE I Program. Set your oscilloscope at 10mV/div., 5uS/div. Place the scope probe on a monitor point indicated in the table below and then adjust the corresponding potentiometers until the scope trace forms a continuous horizontal line at -20mV DC. (See Section IV #27, #28.)

In early units (before REV 2), RV10 and RV11 do not appear and these adjustments cannot be made for AP and MT. In this case, adjust RV4 for C5 and RV3 for C2 in the manner above, but you will see a second signal trace, probably a broken line, on your scope screen.

Monitor Point	ADC Name	Potentiometer
RN14/3	C6	RV2
	C4	RV6
RN14/5	C5	RV4
	AP	RV10
RN15/11	C2	RV3
	MT	RV11
RN15/13	C1	RV1
	C3	RV5

III. C. 2. To verify Total Harmonic Distortion (THD) levels of the 8 memory segments use the following procedure (See Figure III.C.2., THD Verification and Calibration-Connector Diagram):

a. Remove the ribbon cable from ANA-2/J11 and ANA-2/J12, and set aside.

b. Remove DIP shunt from ANA-2/J13 and set aside.

c. Remove DIP resistor network from ANA-2/J17 and set aside.

d. Connect XLR output, left channel, to THD and noise meter in this fashion - pin 3 to hot input of meter,
pin 2 to ground at female XLR,
pin 1 to ground at ground of meter.

e. Set front panel to 20.0 seconds Decay Time in SPACE. Both Early Reflections and Initial Reverberation should be set at 0mS and Level 1. LF Decay should be 20Hz, and HF Decay should be set at 8kHz.

f. For all 8 memory segments measure at Limit** and at -40dB, connecting as is shown in the following table.

Memory Segment	Inject Scope Signal Here	Pick-up ADA Output Here	ADA Output Limit	ADA Output -40dB
MT	J12/16	U16/1	R6*	R5*
AP	J12/15	J13/2	R6	R5
C1	J12/14	J13/3	R6	R5
C2	J12/13	J13/4	R6	R5
C3	J12/12	J13/5	R6	R5
C4	J12/11	J13/6	R6	R5
C5	J12/10	J13/7	R6	R5
C6	J12/9	J13/8	R6	R5

*Connect to the end of R5 or R6 nearest the back of the machine. If R5 (510 ohms) is missing, tack solder a resistor of 430-680 ohms temporarily in place.

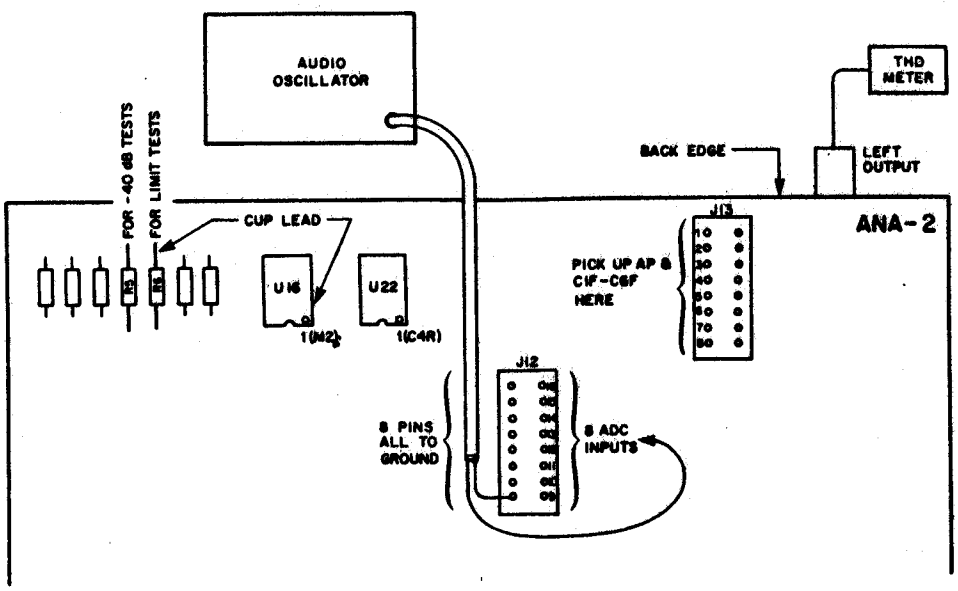
g. For limit level, oscillator level is about +8dBV (±3.9V peak to peak). Use 41Hz signal frequency. For -40dB test, drop oscillator level to -32dBV (±39mV peak to peak). Again use 41Hz signal frequency.

h. For -40dB test, connect ADA output clip lead to R5 to get extra voltage gain. Always pass signal through 8X32 output circuits to get low pass filter action to keep 20kHz sampling rate from output.

i. If THD meter has low pass filter, switch it on.

j. THD limits are: LIM level, -66dB or .05%.
-40dB level, -38dB or 1.3%.

** "Limit" is a signal level adjusted so the "0" (red) Input and/or overflow LED on the front panel is just out.



THD VERIFICATION & CALIBRATION
Connector Diagram

FIGURE III. C. 2

III. C. 3. Total Harmonic Distortion:

a. Set up to measure Limit THD of C1. Set Decay time in SPACE program to 1.0 seconds. Adjust RV7 for min THD (should be -66dB or better).

b. Repeat (a), for C4, adjusting RV8.

c. Set up to measure Limit THD of C4R (clip lead from U22-1 to R6). Adjust RV9 for min THD -66dB.

III. C. 4. CPU-1 Adjustment procedure for voltage detection thresholds is as follows:

a. Connect a variable power supply to be used as Vcc (4.5V - 6.0V range min).
   i. Remove red wire from CPU-1/J6/3.
   ii. Connect positive (+) voltage to CPU-1/J6/3.
   iii. Rest of J6 must remain connected.

b. Plug in CPU-1 board to be adjusted.

c. Place scope probe on CPU-1/U28/4. Adjust scope for 2V/division, 5mS/div.

d. Connect DVM from CPU ground (CPU-1/J6/5) to CPU-1/J6/3 to monitor variable power supply.

e. Adjustment loop for RAM disable threshold:
   i. Start with Vcc at 5.25vdc.
   ii. Reduce Vcc.
   iii. Note at what point the scope trace goes high.
   iv. Turn pot CPU-1/RV1.
   v. Repeat loop until the descending voltage drives the scope trace high at 4.75 vdc (acceptable limits are 4.80V to 4.75V).
   vi. NOTE: After each trial adjustment of RV1, you must repeat loop, starting again at Vcc = 5.25V.

f. Restore red wire to J6/3 and remove variable power supply (+) lead from J6/3.

g. Connect variable power supply to be used as Vcc (9.5 - 7.0 V range min.)
   i. Remove purple wire from CPU-1 /J6/1
   ii. Connect variable power supply (+)lead to J6/1.
   iii. Connect DVM from CPU-1 ground (J6/5) to J6/1 to monitor variable power supply.

h. Place scope probe at CPU-1/U2/4. Scope set as at (c) above.

i. Adjustment loop for "no store" threshold.
   i. Start with raw Vcc at 8vdc.
   ii. Reduce raw Vcc.
   iii. Note at what point that the scope trace goes high.
   iv. Turn pot CPU-1/RV2.
   v. Repeat loop until the descending voltage drives the trace high at 7.50vdc (acceptable 7.4V - 7.6V).
   vi. After each trial adjustment of RV2, you must repeat loop starting again at Vcc = 8V.

j. Restore J6 wires as they were and remove leads from variable power supply.

k. Paint the pots with "no tamper" paint.

III. D. Troubleshooting and Testing Procedures

III. D. 1. Intermittent Problems: The most difficult problems to track down are those that are intermittent, that appear only when the unit is cold, only when the unit is hot, only when it is hit occasionally, or, seemingly, at random. You must be very patient with this kind of machine. If you are quite sure that it has been intermittent, then get it on the bench and try it out. If it seems to work normally, let it cool down, try again, heat it up, try it again, hit it, bang it, etc., until, however you manage to do it, you get the problem to appear and remain. Once the intermittent machine is actually operating in the failed mode, be very gentle with it so that you keep it broken until you find the problem.

If you haven't already, carefully remove the top cover and start probing around with the scope. It is hoped that the failure mode that you can hear by listening to the machine will tell you something about where the problem is. As you proceed in normal troubleshooting from this point, be very, very careful that you don't disturb the machine into working normally again. Use the probe very gently to look for intermittent connectors, where a signal appears on one side of the connector and not on the other. Look for illegal logic levels, non-normal power supply voltages, etc.

III. D. 2. Visual Check: Look in the unit for things like an IC that has come loose or fallen out. Look for something that is charred or burned. Look for a connector, such as a ribbon cable, that has jiggled loose. Look for a piece of wire or a solder blob lying down in the machine. Make sure none of the IC's have bent or broken legs.

III. D. 3. General Strategies and Suggestions: When troubleshooting circuits in the 8X32, check the schematics carefully for signals that you can identify as logic control signals. Examples of such signals are data sent from the CPU, timing signals, outputs of counters, etc. If you are suspicious of a particular circuit, check the destinations of the signals that control the activity of that circuit and make sure you get traces that match the oscilloscope photographs in Section V. Always look at signals at their destinations, rather than at their sources. A further point in this regard is that finding a valid signal at the solder side connection is not the same confirmation as finding a valid signal on the proper IC pin in its socket. Be sure that questionable signals have actually found their way down through sockets, along the etch in the PC board, and back up through the sockets.

Only when you are confident that a malfunctioning circuit is receiving all the correct timing signals coming from the outside and all the proper power supply voltages should you start to probe more deeply.

III. D. 4. Power Supply Check: Power supply circuitry is generally located at the back right corner of the MOM-2 board.

A quick look at the 7-segment display (MOM-2/U44) will tell you which of the power supplies are on. If all are operating, the display should read +.1 (decimal to the right of 1 should not be lit). The silk screen on the PC board indicates the voltage/segment correlation. You should note that the presence of -5V power is not shown by the display. Test for -5V power is not shown by the display. Test for -5V at MOM-2/FB2 as indicated below.

To check voltages with a Digital Multi-Meter:

Attach common lead of DMM to ground.

Test the various power supply voltages using the test points and spec voltages given in the table.

Voltage	Measuring Point on MOM-2	Spec Voltages
+5	R20 - either end	+4.75V to +5.25V
-5	FB2 - either end	-4.9V to -5.1V
+12	FB3 - either end	+11.4V to +12.6V
+7.5	R18 - end indicated on silk screen	+7.13V to +7.88V
-7.5	R19 - end indicated on silk screen	-7.13V to -7.88V
+15	R21 - end indicated on silk screen	+14.25V to +15.75V
-15	R22 - end indicated on silk screen	-14.25V to -15.75V

To test battery: Set meter to DC Volts in the 20V range. Voltage from battery should measure a nominal 3V (min 2.9V to max 3.2V).

III. D. 5. Test Functions at MOM-2/U70: The 8X32 has 4 built-in special test functions that aid in de-bugging and working on circuit problems. They are accessed by inserting jumpers across the pins of an empty socket labelled U70 located on MOM-2 (under the CPU board near the front of the machine). The most convenient way to use this feature is to insert a mini-DIP 8-pin switch in the socket at U70. If you can't do that you can activate the switches by inserting a small piece of jumper wire.

Here follows a brief description of the function of each of the test positions.

III. D. 5. a. CPUDIS: Insert a jumper across pins 1 and 8. This is labelled SW1 on the timing schematic (TIM, sheet 1 of MOM-2 schematic). CPUDIS is useful when you need to work on portions of the circuitry underneath CPU-1 or if you suspect the CPU itself is introducing problems into the rest of the machine. When CPUDIS is enabled, all the data latches that receive information for the front panel settings are forced into a known state. That is, the CPU is no longer necessary in order to operate the rest of the 8X32. You may, in fact, completely remove CPU-1 from the rest of the machine while you work on other problems.

Referring to the ADS schematic (sheet 3 of MOM-2 schematics), you can see that CPUDIS forces the program SPACE, with a Decay Time of 4 or 5 seconds, ER and IR levels to maximum with a delay time of 0. CPUDIS also sets LF Decay to 20Hz and HF Decay to 8kHz and disables the "Input Mute" and "Reverb Clear" functions.

III. D. 5. b. ADST: Insert a jumper from pin 2 to pin 7. ADST stands for Address Test. This is the most complex of the test modes in the machine, though its function is to simplify the operation of the address logic so that it's easier to analyze.

The address logic is a feedback circuit in which the results of the previous computation reappear at the input to the circuit and are used as the basis for the next computation. This kind of circuitry is sometimes difficult to trouble-shoot because a fault anywhere in the loop, either the feed forward or the feedback path, can cause the circuit to fail and stop dead.

The address logic has to compute 40 addresses, the 32 read addresses for the D-A taps that have to be read from memory, and also the 8 write addresses for the eight memory segments. In addition, each of the 40 addresses consists of a row and a column portion for the dynamic RAM. This is a total of 80 addresses that are computed within a 51uS time frame.

When the test function is operating the machine only computes a write address for one segment, and only a column address at that. It therefore, drops down from preparing 80 addresses in each time frame to preparing one. This obviously makes it much easier to observe and analyze the address circuits.

When you invoke the ADST function you should see square waves at the output of U50 and U36. Starting at MOM-2/U50/11 and working up, the square waves should increase in period binarily.

III. D. 5. c. ADAT: Insert a jumper between pins 3 and 6. ADAT stands for Analog to Digital to Analog Test. This is a test function which disconnects the A to D and the D to A converters from the 16K memories in the machine. It does this by modifying the signals that go to the tri-state steering logic connected to the DAC inputs. These are chips on MOM-2, (MEM, sheet 2, MOM-2) that steer data to the converters either from the successive approximation register (SAR) or the RAM outputs. When this test function is selected, the DAC's always receive data that come from the SAR via the LS373 transparent latches. This works as follows: Recall that the 8X32 does 8 A-D conversions. Each converter in the test mode does an A-D conversion and then the transparent latch is disabled so that the results of the A-D conversion are held in the latch. The latch remains connected to the DAC, so that after the DAC has been used for the A-D conversion, the data is present and held constant at the DAC inputs, and is reconstructed by the current voltage converter into an output, actually into the four D-A slots that follow that A-D conversion.

We actually rarely use this feature at the factory but it could be helpful in isolating sources of noise and distortion to either the memory or the converter section. If the noise and distortion goes away when ADAT is invoked then you can suspect the memory.

Unfortunately the test mode severely modifies the entire function of the machine. The 8X32 no longer functions as a reverberator when the test mode is selected, so it can only be useful if you are injecting signals into the connector ANA-2/J12 and measuring distortion via the techniques discussed in Section III.C.2.

III. D. 5. d. GONE: Jumper from pin 4 to pin 5. GONE stands for Gain 1. This is a fairly simple test function that forces a gain of 1 into the multiplying D-A so that all the taps are reconstructed with the same gain. This mode is useful if you question that the gain setting circuitry or the gain DAC are working properly. You can set this switch closed if you simply want to make all the taps look identical, not varying in gain, for test purposes.

III. D. 6. Trouble-shooting Audio Problems Using ANA-2/TP1: Intermittent problems encountered in the 8X32 which introduce pops, clicks, or distortion into the output signal can often be diagnosed using the master test point on ANA-2. To use ANA-2/TP1 to observe activity throughout the machine, connect the 8X32 as follows:

Remove the top and bottom covers.

Connect an oscilloscope probe to MOM-2/U28/15 for signal MTLB, which you will use to synchronize the scope.

Mate that probe to input B, or to an external sync input on the scope if you prefer.

Referring to Scope Photo #31 in Section IV, adjust MTLB to occur as a positive going pulse in the 8th centimeter of the scope display. Your sweep speed will be approximately 6.4uS/div. The scope is now calibrated so that the traces you see should match the photos in this manual.

Connect input A of your oscilloscope to TP1, which can be found at the junction of R63, R64, and R65 on ANA-2 (central portion of ANA-2, slightly above and to the right of dead center).

Connect an audio oscillator to either of the input XLR's of the 8X32 and adjust its frequency and level for an input level display on the front panel of greater than -6dB and less than 0dB. The frequency should be down around 40-100Hz. Tune the frequency slightly to extinguish the red, overflow LED, should it be on.

Connect a stereo monitor to the 8X32 output XLR so that you can listen to the output.

The front panel settings for the 8X32 should be:

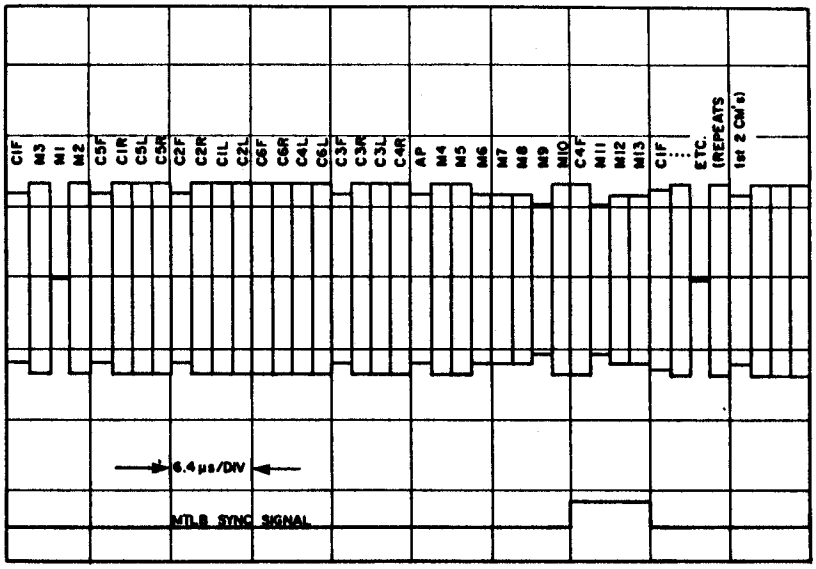
Program - PLATE 1
Early Reflections at 0mS and Level 8.
Initial Reverberation at 0mS and Level 8.
6.0 Decay Time
LF Decay at 20Hz, HF Decay at 8kHz.

In a normally operating 8X32, you should now hear a clean, low-frequency tone from the audio monitor.

Adjust the scope sensitivity for input A, which you have connected to TP1, to look at the signal activity.

The first eight centimeters of the oscilloscope display shows each of the 32 D-A operations that the 8X32 performs. (See Figure III.D.6). The exact height of these thirty-two D-A activity level regions will vary depending upon your choice of frequency in the audio oscillator. However, each of the thirty-two regions should be uniformly shaded green (if your scope has a green phosphor), without any areas of darker or lighter shading, or any other anomalies. (See Section IV, #29).

In reality, of course, you are probably performing this test because you have an audio problem and will in fact see anomalies in some of the regions. Figure III.D.6 shows the tap assignments in those first eight centimeters. By referring to the figure you should now be able to identify the signals which are not normal. For example, if you find that, in the third centimeter, the first, second, and fourth signal regions look distorted or are missing while the third region looks fine, then you know you have a problem with memory segment C2. Or, a problem with the All Pass segment would show up as an anomaly only in the first portion of the 6th centimeter.



DA TAP ASSIGNMENTS SEEN AT ANA TPI

FIGURE III. D. 6

After you have found a problem region on the scope face, you will have a better idea of where to look in the circuits of the 8X32. The table below should help you diagnose some specific problems you might encounter. By going through the table you should also become familiar with the overall diagnostic strategy for using TP1.

ANA-2/TP1 DIAGNOSTIC TABLE

Region(s) Affected	General Diagnosis or Diagnostic Technique	Likely Sources of Problem
All D-A taps	Problem in circuits affecting both converters	Power supply circuits, logic buffer circuits on ANA-2, SAR's on MOM-2, memory
Those from 4 memory segments, either AP, C4, C5, and C6 (converter #1) OR MT, C1, C2 and C3 (converter #2)	These groupings indicate the problem is related to one of the two A-D converters. See Section VI, Sheet 2 (ADA) of ANA-2 schematic.	Any circuit common to all A-D operations done by a particular converter.
8 regions all coming from one of the 4 de-multiplexers (ANA-2/U20,U26,U17, U23). Check sheet 2 (ADA) of ANA-2 schematic.	One of the DMUX circuits is not working	The DMUX chip involved (ANA-2/U20,U26,U17,U23) or a bad logic signal that drives the DMUX (such as DMS2H which drives U26)

Region(s) Affected	General Diagnosis or Diagnostic Technique	Likely Source of Problem
16 regions, all coming either from U20 and U26 via their sample-and-holds OR from U17 and U23 via their sample-and-holds. (Check Sheet 2 (ADA) of ANA-2 schematic).	Probably a D-A rather than an A-D problem, in one of the converters	In converter #1, D-A problems would be confined to circuits using U39 and U30. In converter #2, D-A problems would be confined to circuits using U44 and U38. Another source of D-A problems might be the registers on MOM-2.
Regions coming from 2 memory segments, one of the following pairs: C6 and C4, C5 and AP, C1 and C3, C2 and MT.	ADC problems in signals that share sample-and-hold, a buffer and a comparator	The particular signal path indicated by the memory segments involved. For example if the problem resides in the C6 and C4 pair, check the sample-and-hold at ANA-2/U32 and the comparator at ANA-2/U40.
Those coming from one memory segment (such as C1L, C1R and C1F coming from C1)	A problem with the input signal path for the particular memory segment; Check Sheet 3 (FBC) of ANA-2 schematic.	Either active or passive components in that input signal path. For C1 related problems, for example, check ANA-2/U58, U55, U61, and U64 as well as associated passive components
AP tap, all eighteen of the C taps, with the 12 MT slots O.K.	Problems with the All Pass Circuits	Refer to Sheet 2 (FBC) of the ANA-2 schematic. The All Pass circuits are shown across the top of the sheet. Problem could be U69 or any of the circuitry in the low-pass filter or attenuator stage which lie on the signal path which takes AP and IR and yields AP01 and AP02.
Any tap not occupying both positive and negative levels.	Problem with a DMUX which steers current for positive and negative A-D and positive and negative D-A	Depending on taps involved (check sheet 2 (ADA) of ANA-2 schematic) either the DMUX at ANA-2/U39 or ANA-2/U44.

Problems with address logic are probably the most difficult to track down in the 8X32. They can result in clicking, distorted sounds, and feedback that won't die out and sounds like a motor running. The procedure you have just been using can be modified to produce clues about possible address problems:

A ribbon cable runs into the A-D converter section on ANA-2 and is plugged into J11 and J12. Remove the cable and set it aside.

The right-hand pins of the jack J12 are the inputs to the eight memory segments. Starting at the top (pin 16) of J12, they run MTIN, APIN, C1IN, C2IN, C3IN, C4IN, C5IN, and C6IN.

To facilitate making connections into the eight memory segment A-D inputs, insert a 16-pin DIP resistor network of any handy value. This resistor network should contain 8 resistors running left to right down the length of the DIP.

Put a 16-pin test clip on that resistor network and connect an audio oscillator via some test leads. The audio oscillator should be set at about 3½V output at approximately 40Hz. Connect its ground to a convenient ground on ANA-2 and its hot lead, to begin with, to pin 16 of the DIP clip on the resistor network in J12.

The scope should now show output in slots M2-M13. All the other slots should show no signal activity. Now move the test lead to J12/15 and you should see activity only at the AP slot on your oscilloscope (the first slot in the 6th centimeter). See Section IV. #32 for a scope photo of how MT and AP should look. You can move the test lead down through the other 6 inputs to see C1-C6, and match your traces with those shown in #31.

In a normally functioning 8X32 you will only see activity in the slots related to the memory segment you are testing. Any signal activity in the other slots indicates a problem, most likely with the memory, but possibly with the ADA circuitry. Signals in unwanted slots make four DMUX's on ANA-2 (U17, U20, U23, U26) suspect, along with their associated DMS control signals, and their associated address signals coming off pins 9, 10, and 11.

You can see some obscure things here too. For example, if, when you are applying the signal to C1, you also see activity on the three slots associated with C3, you should be suspicious of the MUX U34. (See Section IV, #33, #34 for other examples).

NOTE: Remember that when you are using the test point you are looking at the multi-plexed D-A activity at the output of U30 and U38. The test point shows relatively raw and unprocessed activity in the 32 taps. The test point is a very valuable diagnostic tool, but problems related to the DMUX's and Sample-and-Holds will not be revealed while using it. You may have to probe further to make sure signals are O.K. at the output of the Sample-and-Holds.

III. E. Spare Parts

III. E. 1. Obtaining replacement parts from the factory: Most of the components in the 8X32 should be locally obtainable. In addition, some dealers, especially overseas dealers, will have purchased spare parts kits from URSA MAJOR and should have even the hard-to-find parts on hand. If your dealer doesn't have a part, and you wish to buy parts directly from the factory, please be sure to furnish the following information: the serial number of your machine; the module and revision number on which the component appears (MOM-2, ANA-2, CPU-1, PAN-1, REM-1, or PAN-2); a complete description (including part number) of the defective part, and, if possible, the proper URSA MAJOR part number from the lists (Appendix B) in this manual. It would also be helpful to us if you would describe any peculiar circumstances attendant with the failure. We would like to be able to detect any emerging failure pattern, so that we may respond to it with a change in design or choice of parts in future units.

III. E. 2. Emergency substitutions: Some possibilities for emergency substitution parts may be easy for you to obtain locally. Most of the logic IC's are from the 74LS series. They can be replaced with military versions (54LS), with equivalent LS versions from other manufacturers, and, in some cases, with conventional 7400 series IC's. For example, a 74LS163 could probably be temporarily replaced with a 74163. The 4051 multiplexers on ANA-2 should be replaced only with Motorola 4051B types. Also on ANA-2, the 4741 quad op amps should be replaced only with Motorola chips or National LM 348N's.

III. E. 3. Passive components: With regard to the passive components, any of the resistors in the 8X32 could be obtained locally. A single in-line resistor network, such as those found on MOM-2 and ANA-2, can even be replaced with discrete resistors, if care is used in soldering an assembly of 1/4 watt resistors together. Bypass capacitors are completely non-critical; the many 0.02's and 0.1's sprinkled around the machine can be replaced with an equivalent part. This is also true for the 4.7uF and 22uF tantalum capacitors. In most instances, the bypassing is conservative enough so that if the capacitor were to fail, it could simply be removed.

III. E. 4. Spare modules for troubleshooting: A few dealers may have spares of the easily removeable modules, ANA-2, CPU-1, and PAN-1. These can be helpful during troubleshooting, or as a source of parts. In troubleshooting, the obvious advantage is that you can simply swap out an entire section of circuitry to see where the problem lies. If you have access to a second machine, and module swapping narrows the problem so that you recognize which module is not working properly but you are unable to fix the unit, please contact URSA MAJOR by telephone, telex, or letter, and we'll arrange for swapping a replacement module.

IV. SCOPE PHOTOGRAPHS

Key to Scope Photographs

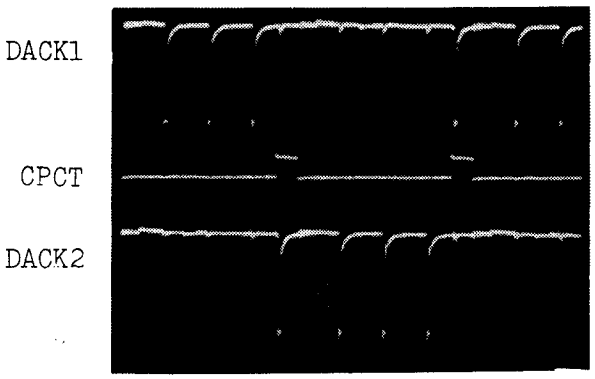
1. Any sub-heading in the scope photo captions which does not apply to a particular photo has been deleted. For example, if the Input Frequency is irrelevant, that heading will not appear in the caption.

2. A "Standard" Front Panel Setting (FP Setting) is as follows:
   Program - SPACE
   Decay Time - 20.0 Seconds
   Early Reflections - 0mS, Level 8
   Initial Reverb - 0ms, Level 8
   LF Decay - 20Hz
   HF Decay - 8kHz
   Input Mute - off
   Reverb Clear - off

3. ANA-2/TP1 can be found at the junction of R63, R64, and R65 (central portion of ANA-2, slightly above and to the right of dead center). Refer to Section III.D.6 for a discussion of Troubleshooting with ANA-2/TP1.

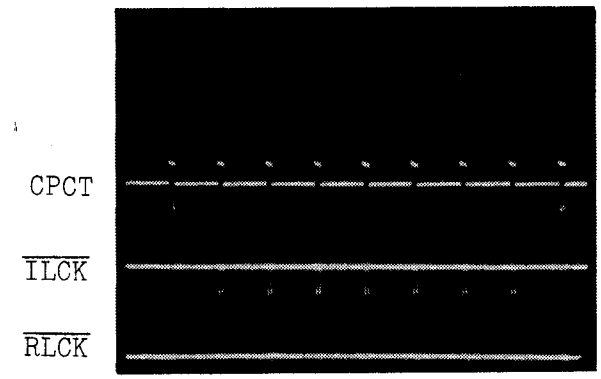
4. MTLB can be found at MOM-2/U28/15.

5. CPCT can be found at MOM-2/U24/5.



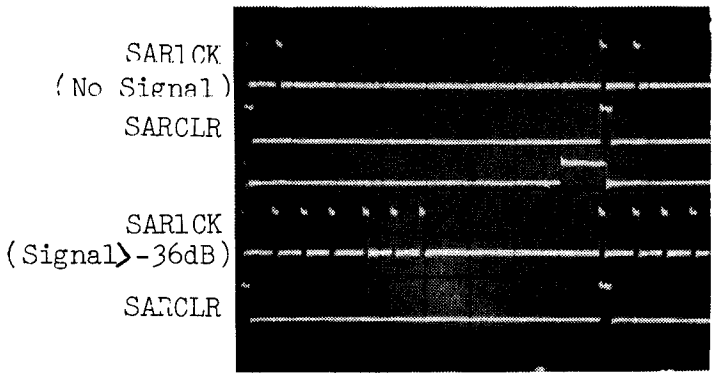
#1 DAC CLOCKS

Probe Point: DACK1-MOM-2/U81/11
DACK2-MOM-2/U80/11
Trigger Signal: CPCT
FP Setting: Standard
Scope Setting: 1V/div.,2uS/div.
Comment: CPCT at 5V/div.



#2 SIGNAL LEVEL CLOCK PULSES

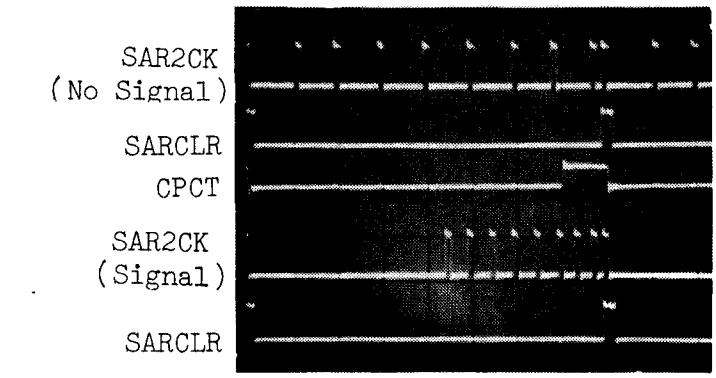
Probe Points: $\overline{\text{ILCK}}$ - MOM-2/U87/4
$\overline{\text{RLCK}}$ - MOM-2/U87/10
Trigger Signal: CPCT
Scope setting: 2V/div., 5uS/div.
Comments: CPCT at 10V/div.



#3 SAR CLOCK SIGNALS

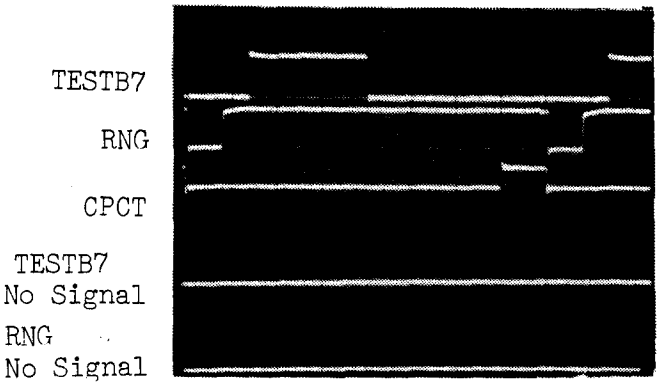
Probe Points: SAR1CK - MOM-2/U28/9
SARCLR - MOM-2/U28/12

Trigger Signal: CPCT
Scope Setting: 5V/div., 5mS/div.



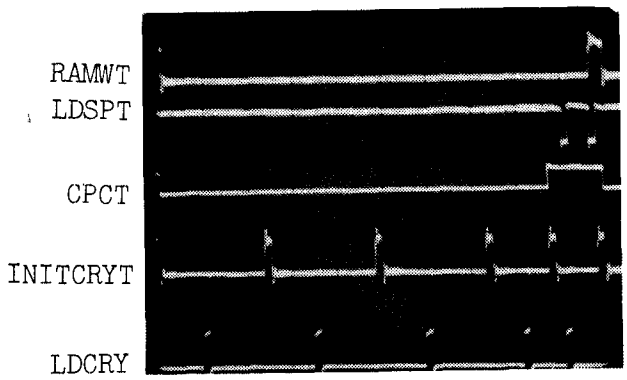
#4 SAR2CK

Probe Point: SAR2CK:MOM-2/U29/5
SARCLR:MOM-2/U29/9
Trigger Signal: CPCT
Scope Settings: 5V/div., 1uS/div.



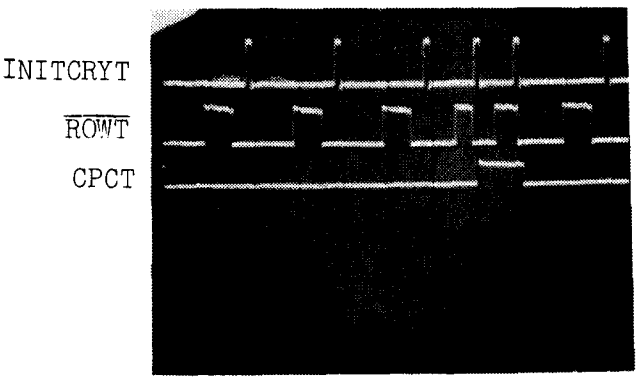
#5 TESTB7

Probe Points: TESTB7 -MOM-2/U31/3
RNG -MOM-2/U41/14
Trigger Signal: CPCT
Scope Setting: 5V/div., 1uS/div.



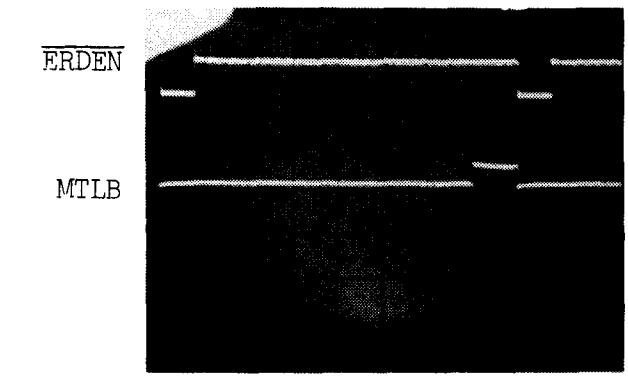
#6 RAMWT, LDSPT, INITCRYT, LDCARY

Probe Points: RAMWT - MOM-2/U37/3
LDSPT - MOM-2/U12/3
INITCRYT - MOM-2/U11/13
LDCRY - MOM-2/U1/3
Trigger Signal: CPCT
Scope Settine: 5V/div., .64uS/div.



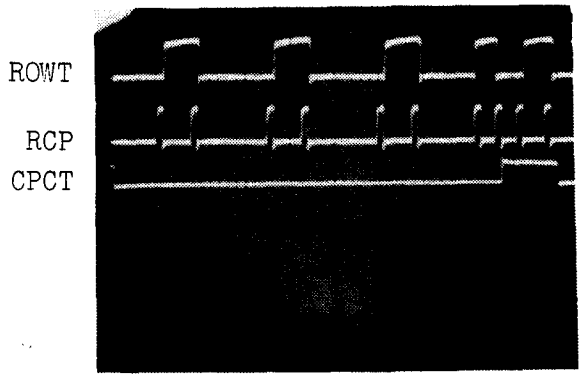
#7 INITCRYT COMPARED TO $\overline{\text{ROWT}}$

Probe Point: INITCRYT-MOM-2/U11/13
$\overline{\text{ROWT}}$-MOM-2/U19/10
Trigger Signal: CPCT
Scope Setting: 5V/div., luS/div.



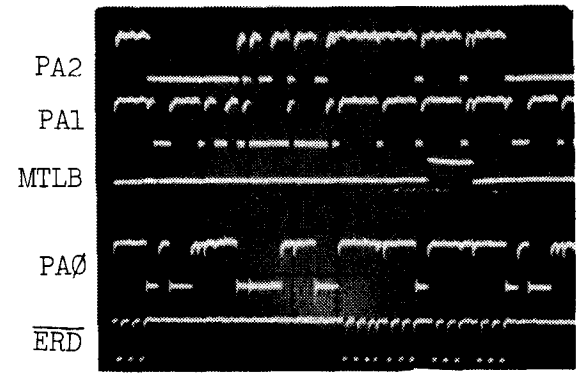
#8 $\overline{\text{ERDEN}}$

Probe Point: MOM-2/U72/4
Trigger Signal: MTLB
Scope Settings: 5V/div., 6.4uS/div.



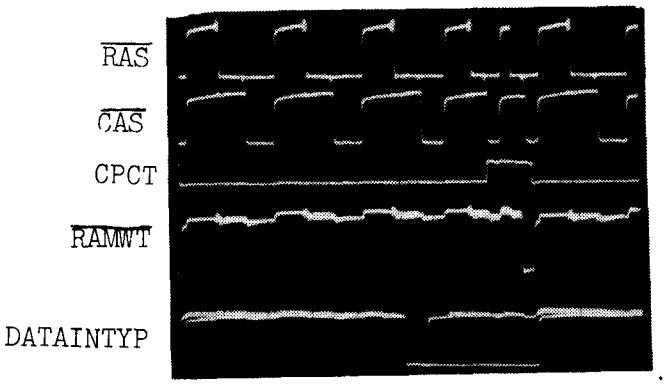
#9 ROWT, RCP

Probe Point: ROWT-MOM-2/U19/11
RCP-MOM-2/U50/9
Trigger Signal: CPCT
FP Setting: Standard
Scope Setting: 5V/div., .64uS/div.



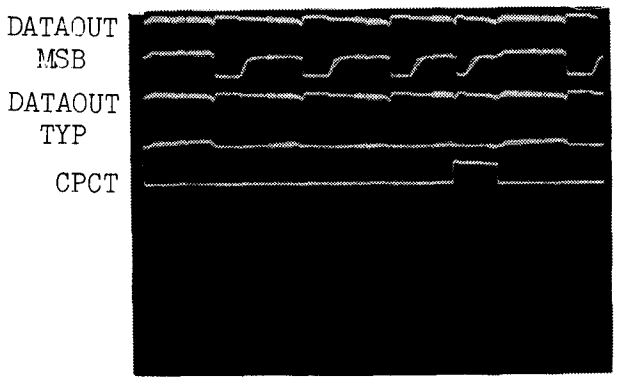
#10 PARTITION ADDRESSES

Probe Point: PA2-MOM-2/U9/7
PA1-MOM-2/U9/9
PA0-MOM-2/U9/12
$\overline{ERD}$-MOM-2/U72/5
Trigger Signal: MTLB
Scope Setting: 5V/div., 6.4uS/div.



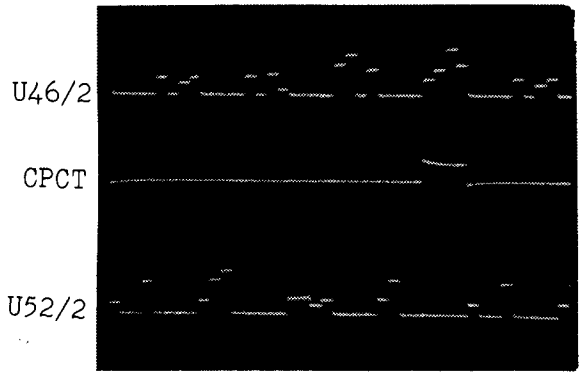
#11 SIGNALS $\overline{RAS}$, $\overline{CAS}$, DATAINTYP, $\overline{RAMWT}$

Probe Points: $\overline{RAS}$-MOM-2/U51/4
DATINTYP-MOM-2/U51/2
$\overline{CAS}$-MOM-2/U51/15
$\overline{RAMWT}$-MOM-2/U51/3
Trigger Signal: CPCT
Input Frequency: 41 Hz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 2V/div., 8uS/div.
Comments: CPCT is at 5V/div.



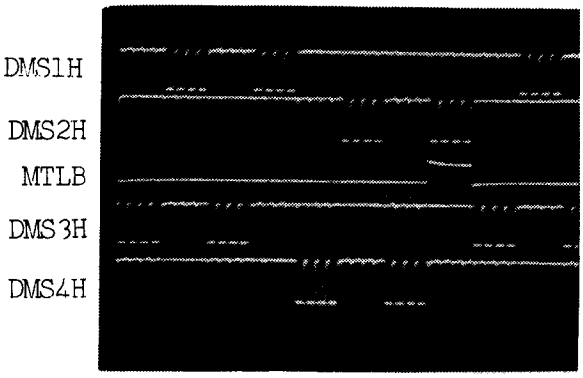
#12 DATAOUT MSB COMPARED TO DATAOUT TYP

Probe Points: DATAOUT MSB-MOM-2/U54/14
DATAOUT TYP-MOM-2/U56/14
Trigger Signal: CPCT
Input Frequency: 41 Hz
Input Level Display: Limit Level
FP Setting: Standard
Scope Setting: 2V/div/, 6.4uS/div.



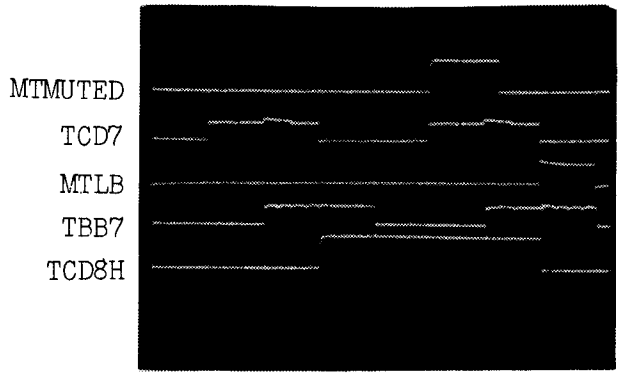
#13 GAIN DAC OUTPUTS

Probe Points: ANA-02/U46/2
ANA-02/U52/2
Trigger Signal: CPCT
Scope Setting: .5V/div., 6.4uS/div
Comments: Shows the variable reference for the DAC's as a function of gain. Bottom horizontal of signals is at -1.2V.
NB: This is E4-0 software, not current E4-1 software.



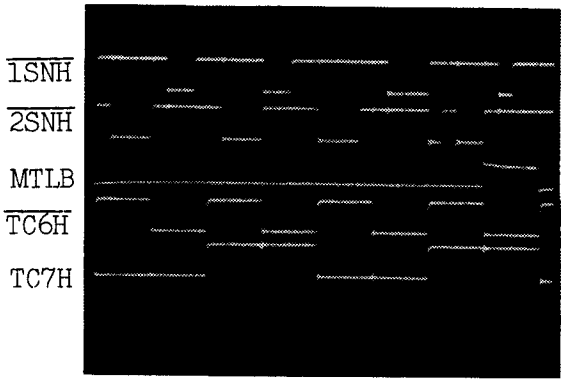
#14 DAC DMUX STROBES

Probe Points: DMS1H - ANA-2/U14/8
DMS2H - ANA-2/U14/6
DMS3H - ANA-2/U14/4
DMS4H - ANA-2/U14/12
Trigger Signal: MTLB
Scope Setting: 5V/div., 6.4uS/div.



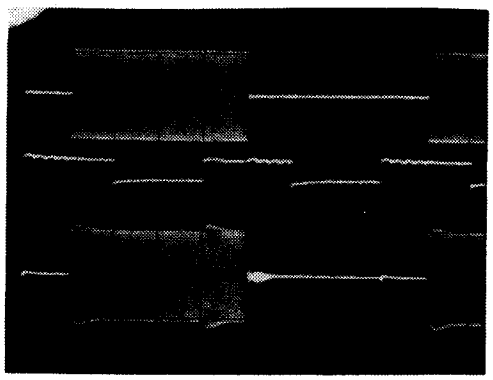
#15 ANA-2 LOGIC SIGNALS

Probe Points: MTMUTED-ANA-2/U66/6
TCD7 -ANA-2/J1/11
TBB7 -ANA-2/U35/8
TCD8H -ANA-2/U34/9
Trigger Signal: MTLB
Scope Setting: 10V/div., 5.1uS/div.



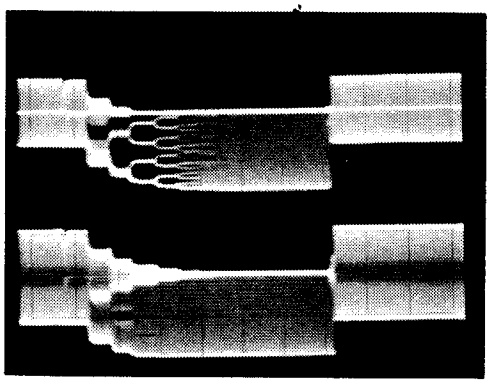
#16 $\overline{1SNH}$, $\overline{2SNH}$, $\overline{TC6H}$, TC7H

Probe Points: $\overline{1SNH}$ - ANA-2/U39/11
$\overline{2SNH}$ - ANA-2/U44/11
$\overline{TC6H}$ - ANA-2/U44/9
TC7H - ANA-2/U44/10
Trigger Signal: MTLB
Scope Setting: 10V/div., 5.1uS/div.



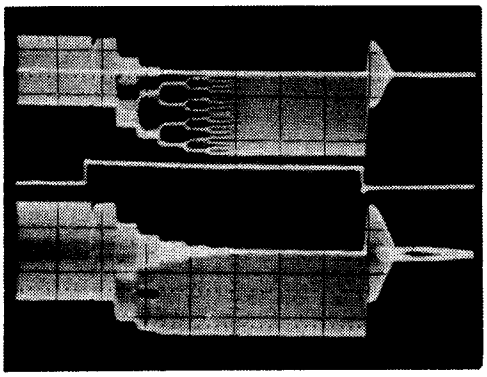
#17 ADA INPUT MUX and SAMPLE-and-HOLD

Probe Points: MUX Output -ANA-2/U34/3
TBB7 -ANA-2/U35/8
S&H Output -ANA-2/U36/1
Trigger Signal: TBB7
Input Frequency: 41 Hz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 4V/div.(for top and bottom signals), .9uS/div
Comments: Sample-and-Hold is in a hold mode when TBB7 is low.



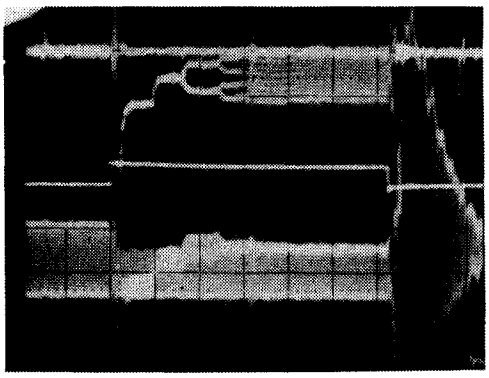
#18 AD CONVERTER - COMPARATOR INPUTS
POSITIVE and NEGATIVE SIGNALS

Probe Points: Pos.Sig-ANA-2/U42/3
Neg.Sig-ANA-2/U42/2
Trigger Signal: MOM-2/T20/16
Input Frequency: 41 Hz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 2V/div., 1uS/div.
Comments: Delayed Time Base Magnification.
Signal in Test point MOM-2/T20/16 at ±3.95V AC.



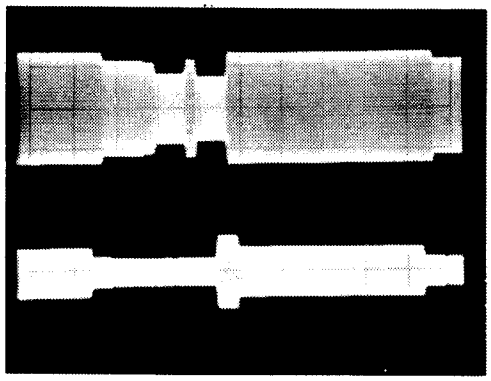
#19 COMPARATOR INPUTS - HIGH SIGNALS

Probe Points: Pos.Sig.: ANA-2/U43/3
Neg.Sig.: ANA-2/U43/2
Trigger Signal: MTLB
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 2V/div., 1uS/div.
Comments: MTLB is at 10V/div. scope amplitude.



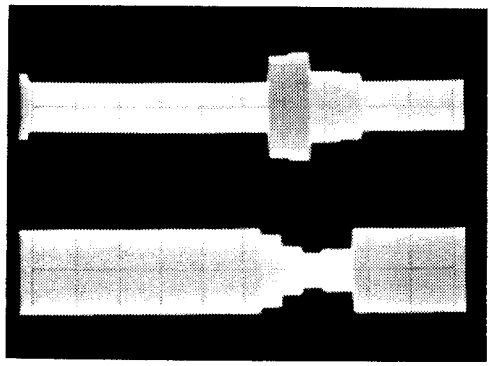
#20 COMPARATOR INPUTS - LOW SIGNALS

Probe Points: Pos.Sig.: ANA-2/U43/3
Neg.Sig.: ANA-2/U43/2
Trigger Signal: MTLB
Input Frequency: 41 Hz
Input Level Display: No LED's on
FP Setting: Standard
Scope Setting: 20mV/div., 30uS/div.
Comments: MTLB sensitivity at 10V/div. Shows the wiffle tree while being driven at -40dB from limit.



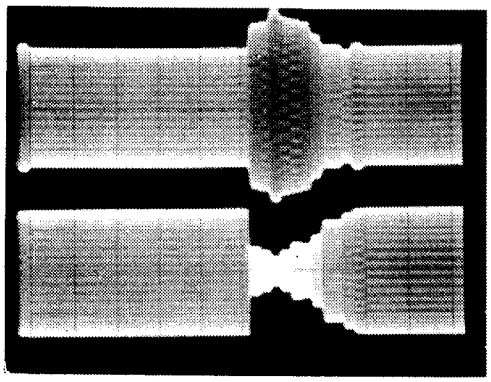
#21 CL and CR SUMMERS

Probe Points: CL-ANA-2/28/7
CR-ANA-2/28/1
Trigger Signal: MTLB
Input Frequency: 4.2 kHz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 2V/div., 6.4uS/div
Comments: Shows each is sum of 6 signals



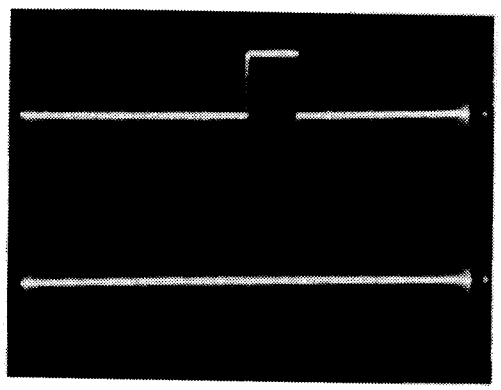
#22 IRL and IRR SUMMERS

Probe Points: IRL-ANA-02/75/1
IRR-ANA-02/75/7
Trigger Signal: MTLB
Input Frequency: 4.2 kHz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Setting: 2V/div., 6.4uS/div.
Comments: Shows each is sum of 5 signals



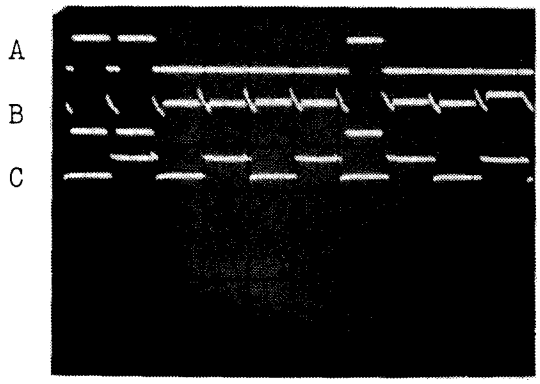
#23 AP SUMMER

Probe Points: APIN-ANA-02/69/1
APO-ANA-02/69/7
Trigger Signal: MTLB
Input Frequency: 4.203 kHz
Input Level Display: Just Below Limit
FP Setting: Standard
Scope Settin: 2V/div., 6.4uS/div
Comments: Shows sums of 11 signals each trace.
MT only driven.



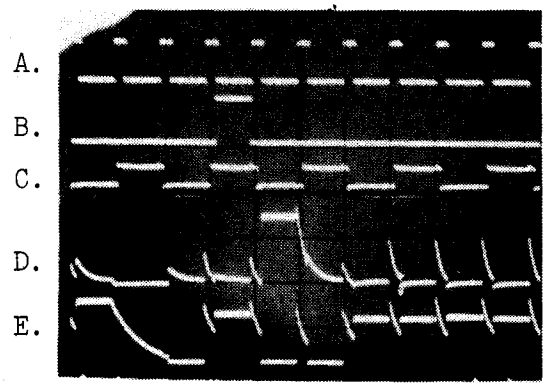
#24 EFFECT OF INPUT MUTE

Probe Point: ANA-2/U33/10
Trigger Signal: MTLB
FP Setting: Standard, Decay Time not applicable.
Scope Setting: 5V/div., 6.4uS/div.
Comments: Bottom trace is 0.0V trace.



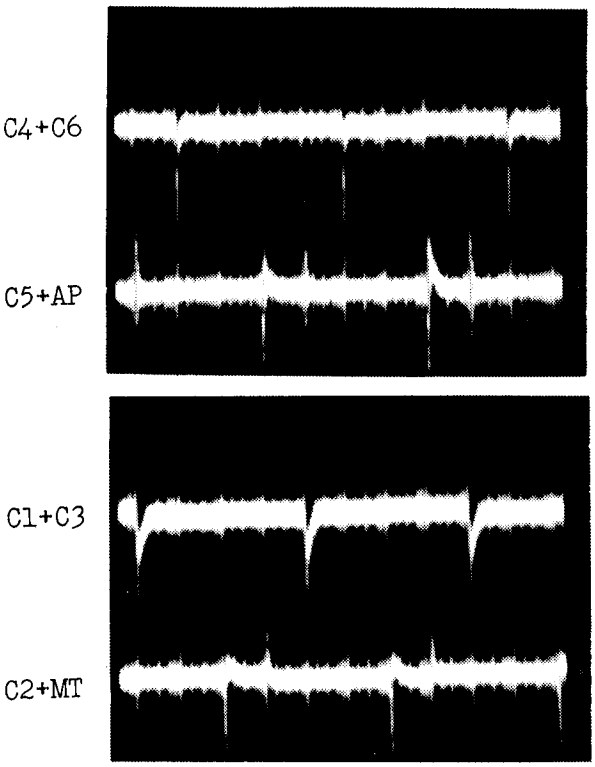
#25 PAN-1 BOARD SIGNALS

Probe Point: A-PAN-1/U1/2
B-PAN-1/U1/17
C-PAN-1/U3/2
Trigger Signal: C(PAN-1/U3/2)
Scope Settings: 5V/div., 5mS/div.



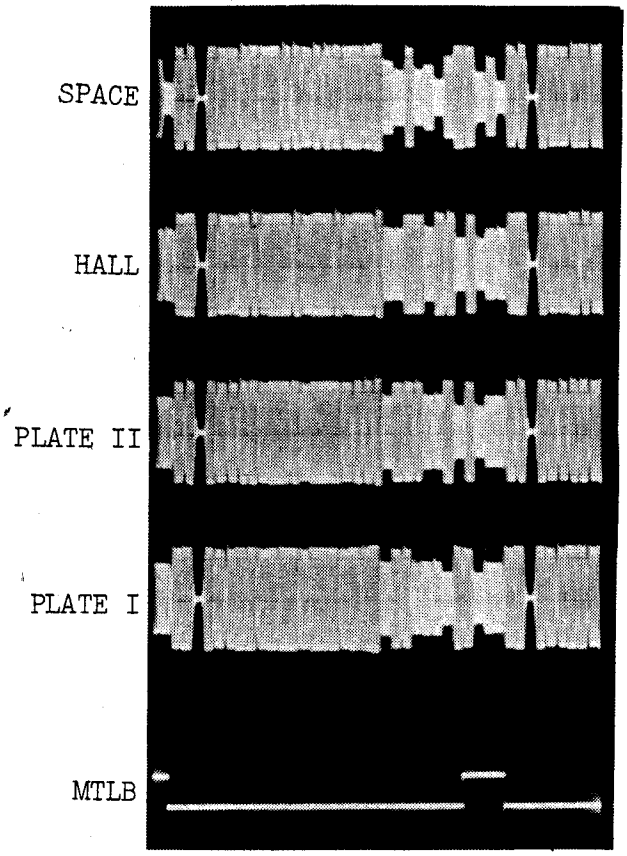
#26 RELATIONSHIP OF SIGNALS ON PAN-1

Probe Point: A(INH)-PAN-1/U3/23
B(Typical Signal on Output of Demux, Shows Phasing) -PAN-1/U3/10
C(Trigger)-PAN-1/U3/2
D(Typical Signal After Going Through Current Driver (U4), On To A Display. Note That Input Is Signal From U3/10)-PAN-1/U4/14
E(Typical Signal From Current Sink U1) - PAN-1/U1/17
Trigger Signal: PAN-1/U3/2
Scope Setting: 5V/div., .5nS/div.



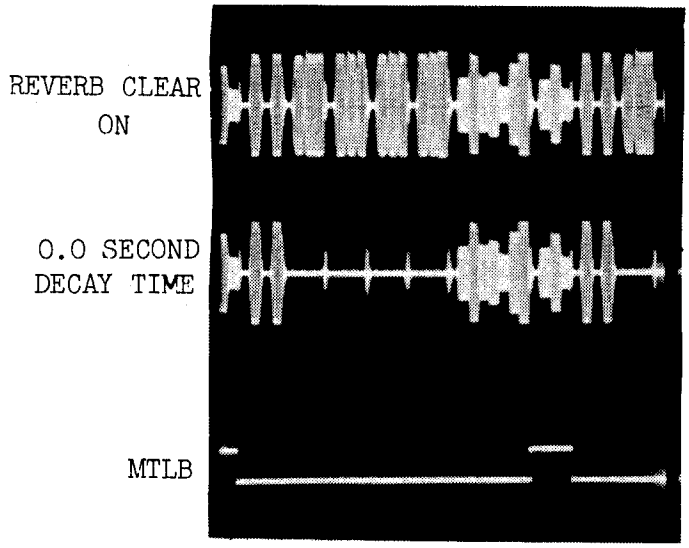
#27 ADC OFFSETS
#28

Probe Points: C4+C6 - ANA-2/RN14/3
C5+AP - ANA-2/RN14/5
C1+C3 - ANA-2/RN15/13
C2+MT - ANA-2/RN15/11
Trigger Signal: MTLB (not shown)
Comments: See Section III. C. 1 for an explanation of how to make the offset adjustments.



#29 ALL D-A TAPS - 4 PROGRAMS

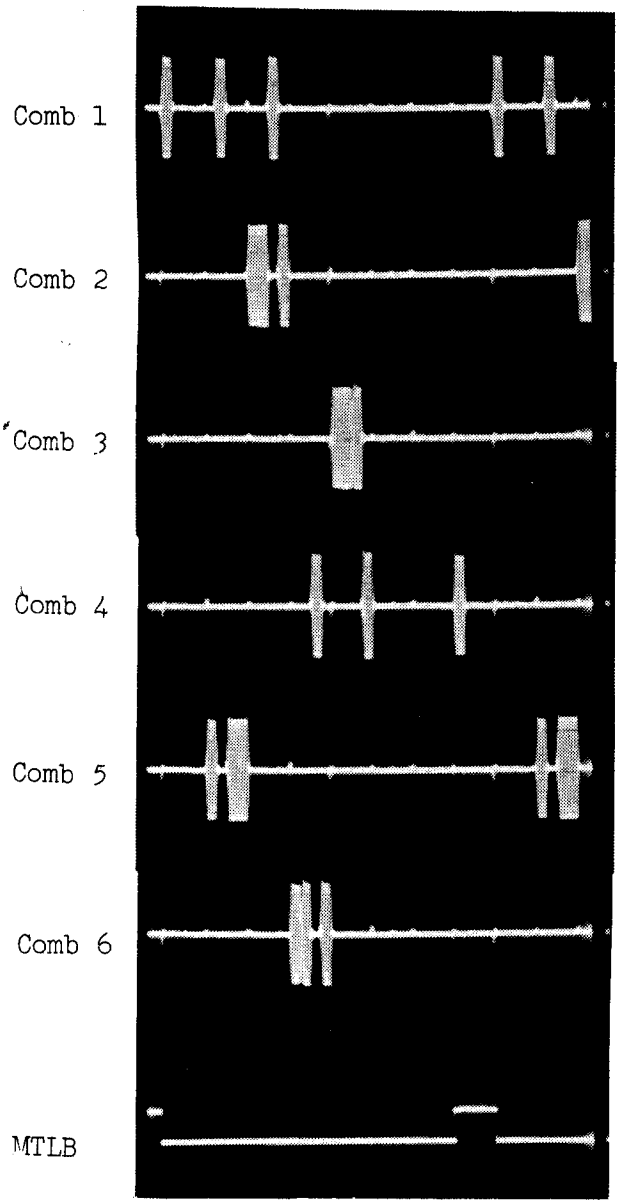
Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III. D. 6 for an explanation of how to use ANA-2/TP1.
All 8 inputs at ANA-2/J12 driven to ±3.95V.



#30 REVERB CLEAR (0.2 SECOND DECAY TIME OVERRIDES FRONT PANEL SETTING) COMPARED TO 0.0 SECOND DECAY TIME

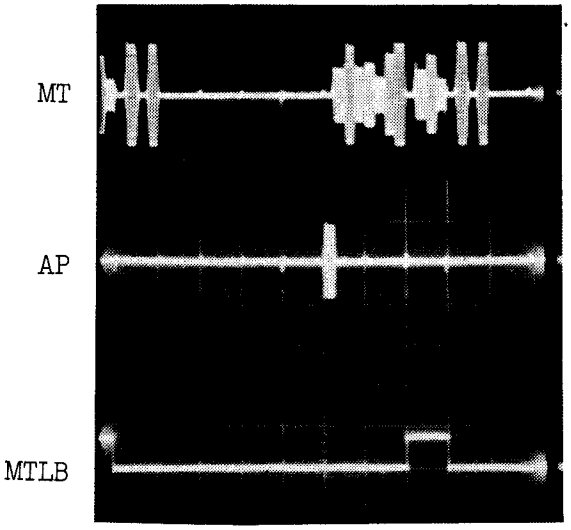
Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III. D. 6 for an explanation of how to use ANA-2/TP1.

All 8 inputs at ANA-2/J12 driven to ±3.95V.



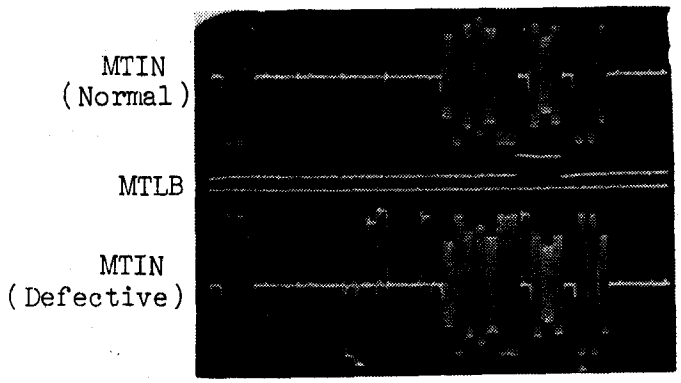
#31 COMBS 1-6

Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III. D. 6 for explanation of how to use ANA-2/TP1.
Each trace is the designated comb only driven at ±3.95V through ANA-2/J12 at the following pins:
C1 - pin 14
C2 - pin 13
C3 - pin 12
C4 - pin 11
C5 - pin 10
C6 - pin 9



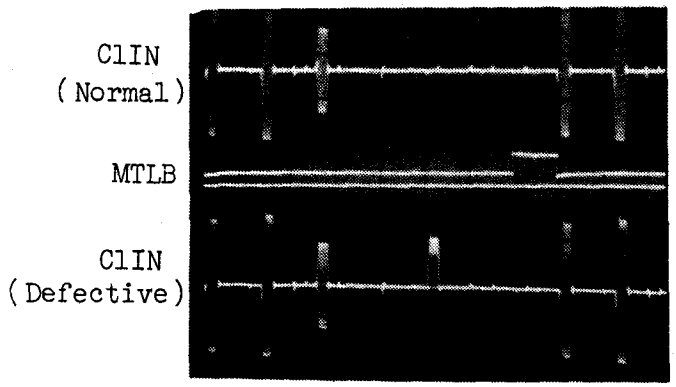
#32 MT and AP (MTIN and APIN only driven)

Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III. D. 6 for explanation of how to use ANA-2/TP1.
Each trace is designated signal only driven at ±3.95V through ANA-2/J12, MT at pin 16 and AP at pin 15.



#33 NORMAL COMPARED TO DEFECTIVE SIGNAL USING ANA-2/TP1 (Signal MTIN)

Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III. D. 6 for an explanation of how to use ANA-2/TP1.
Only M segment driven on both traces. Note the stray, distorted pulses appearing in the 4th and 5th centimeters, indicating A-D or memory problems.



#34 CONVERSION PROBLEMS IN C1 SEGMENT SHOWN BY USING ANA-2/TP1 Signal C1IN)

Probe Point: ANA-2/TP1
Trigger Signal: MTLB
Comments: See Section III.D. 6 for an explanation of how to use ANA-2/TP1.
Note the ghost in bottom trace indicating conversion problem.