PA

DIGITAL MULTI EFFECTOR

REX50

SERVICE MANUAL

3.12.03.04.08. 026

■ CONTENTS（目次）

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SINCE 1887 YAMAHA
NIPPON GAKKI CO., LTD. HAMAMATSU, JAPAN
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IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and parts replacement. Recheck all work before you apply power to the unit.

This product uses a lithium battery for memory back-up.

WARNING: Lithium batteries are dangerous because they can be exploded by improper handling. Observe the following precautions when handling or replacing lithium batteries.

- Leave lithium battery replacement to qualified service personnel.
- Always replace with batteries of the same type.
- When installing on the PC board, solder using the connection terminals provided on the battery cells. Never solder directly to the cells. Perform the soldering as quickly as possible.
- Never reverse the battery polarities when installing.
- Do not short the batteries.
- Do not attempt to recharge these batteries.
- Do not disassemble the batteries.
- Never heat batteries or throw them into fire.

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.

Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanualen.

■ SPECIFICATIONS

ELECTRICAL CHARACTERISTICS	
Effect Freq. Response	20 Hz–12 kHz
Dynamic Range	Effect: 74 dB Direct: 80 dB
Distortion	0.1% max. @ 1 kHz
INPUT	
Number of Channels	Unbalanced × 2 (Phone Jack)
Nominal Level	–10 dBm
Impedance	<500 k-ohms
Level Control	Rotary, continuous
Level Monitor	3-segment LED
A/D, D/A CONVERSION	
Number of Channels	1
Sampling Freq.	31.25 kHz
Quantization	16 bits
OUTPUT	
Number of Channels	Unbalanced × 2 (Phone Jack)
Nominal Level	–10 dBm
Impedance	>10 k-ohms
Mixing	Effect only, effect + direct signal
MEMORY	
Presets (ROM)	1–30
User Memory (RAM)	31–90 (Battery Backup)
MIDI CONTROL	Memory selection (1–90) by MIDI program change number. MIDI triggering of programs 14 and 16. MIDI base key selection for program 17.
FRONT PANEL	
Keys	MEMORY, PARAM, INCREMENT, DECREMENT, STORE, RECALL, UTILITY, BYPASS
Display	16 char. × 2 line LCD 2-digit 7-segment LED
REAR PANEL	
Control	LEVEL
Footswitch Jacks	BYPASS, MEMORY
INPUT/OUTPUT Jacks	1/4'' monaural phone jacks
MIDI Terminals	IN
STEREO MIX Switch	ON/OFF
GENERAL	
Power Supply	U.S. & Canada: 120 VAC, 15W General Model: 220–240 VAC, 15W
Dimensions (W × H × D)	274 × 44 × 196.2 mm (10-3/4'' × 1-3/4'' × 7-3/4'')
Weight	1.7 kg (3 lbs. 12 ozs.)

*0 dB = 0.775 Vr.m.s.

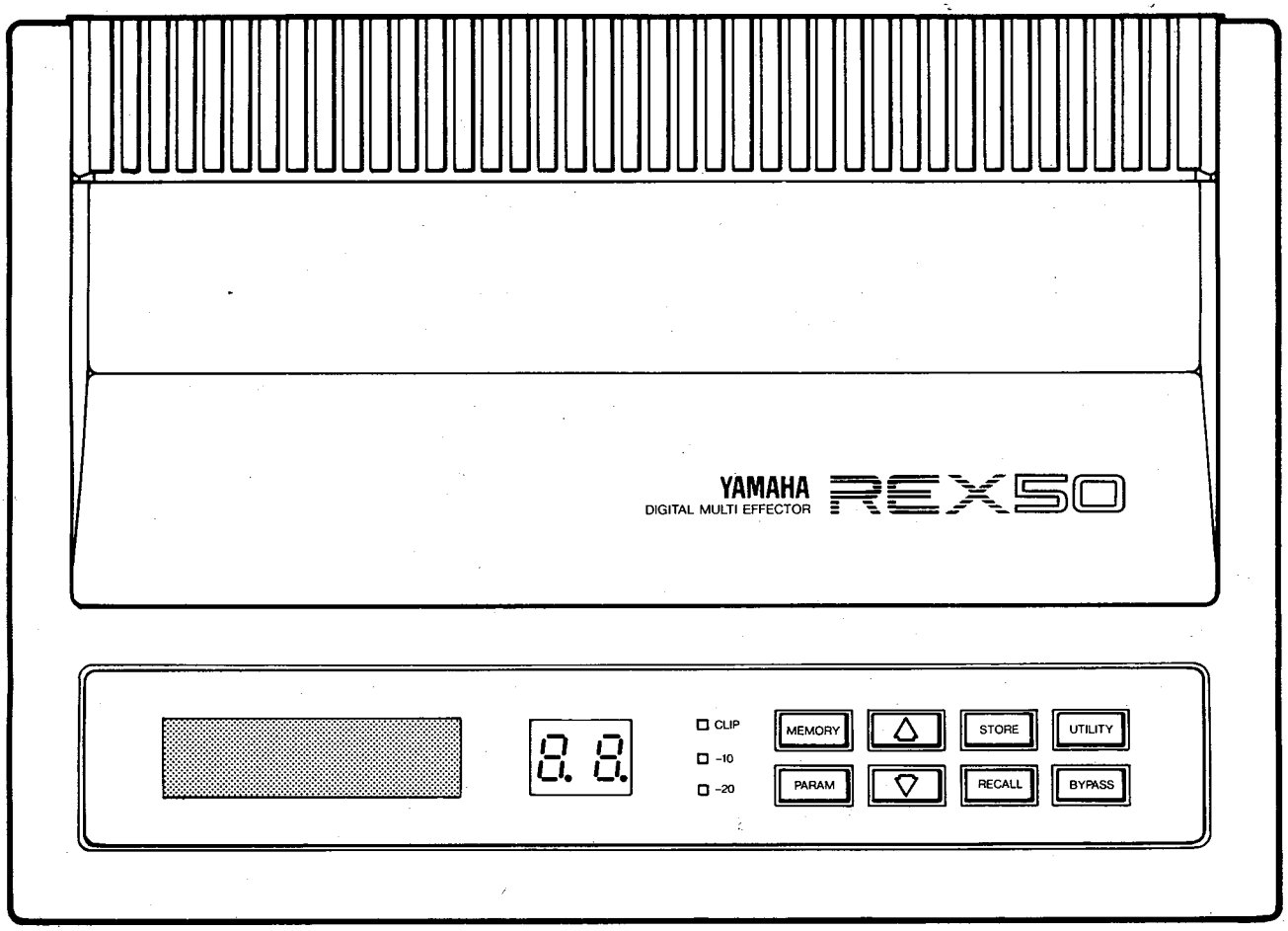
■ 総合仕様

アナログ部	
周波数特性	20Hz～12kHz
ダイナミックレンジ	
ディレイ	80dB
リバーブ、その他	74dB
高調波歪率(ディレイ時)	0.1%(@ 1 kHz, MAXIMUM LEVEL)
INPUT	
チャンネル数	2
方式	アンバランス入力
規定入力レベル	−10dB
適合インピーダンス	500kΩ以下
コネクタ	ホーンジャック
OUTPUT	
チャンネル数	2
方式	アンバランス出力
規定入力レベル	−10dB
適合インピーダンス	10kΩ以上
コネクタ	ホーンジャック
デジタル部	
A/D, D/Aコンバータ	16ビット
サンプリング周波数	31.25kHz
メモリー	
プリセットプログラム	No. 1～30
ユーザーズプログラム	No. 31～90
コントロールパネル	
KEYスイッチ	MEMORY, PARAM, UP, DOWN, STORE, RECALL, UTILITY, BYPASS
ディスプレイ	
メモリーNo.	7セグメント2桁LED
プログラム名称、パラメーター	16文字2段LCD
入力レベル	3素子LED(CLIP,−10.−20)
リアパネル	
可変ボリューム	INPUT LEVEL
フットスイッチジャック	MEMORY, BYPASS,
コネクター	INPUT L(MONO), INPUT R, OUTPUT L, OUTPUT R, MIDI IN
スイッチ	POWER ON/OFF STEREO MIX ON/OFF
電源	AC100V, 50/60Hz
消費電力	10W
寸法(W×H×D)	274mm×44mm×196.2mm
重量	1.7kg

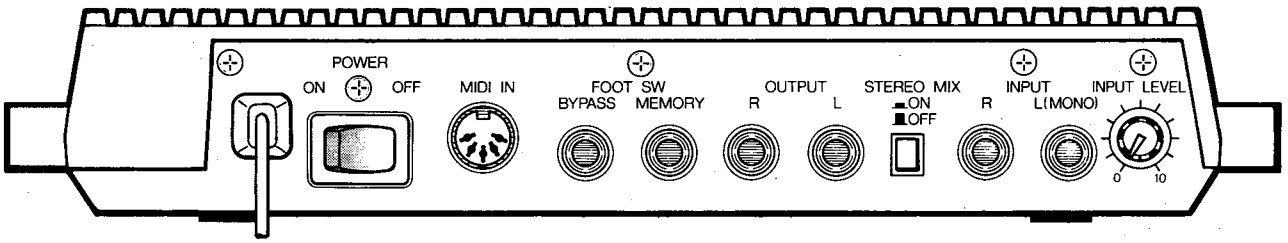
※ 0 dB=0.775Vr.m.s.

■ PANEL LAYOUT（パネルレイアウト）

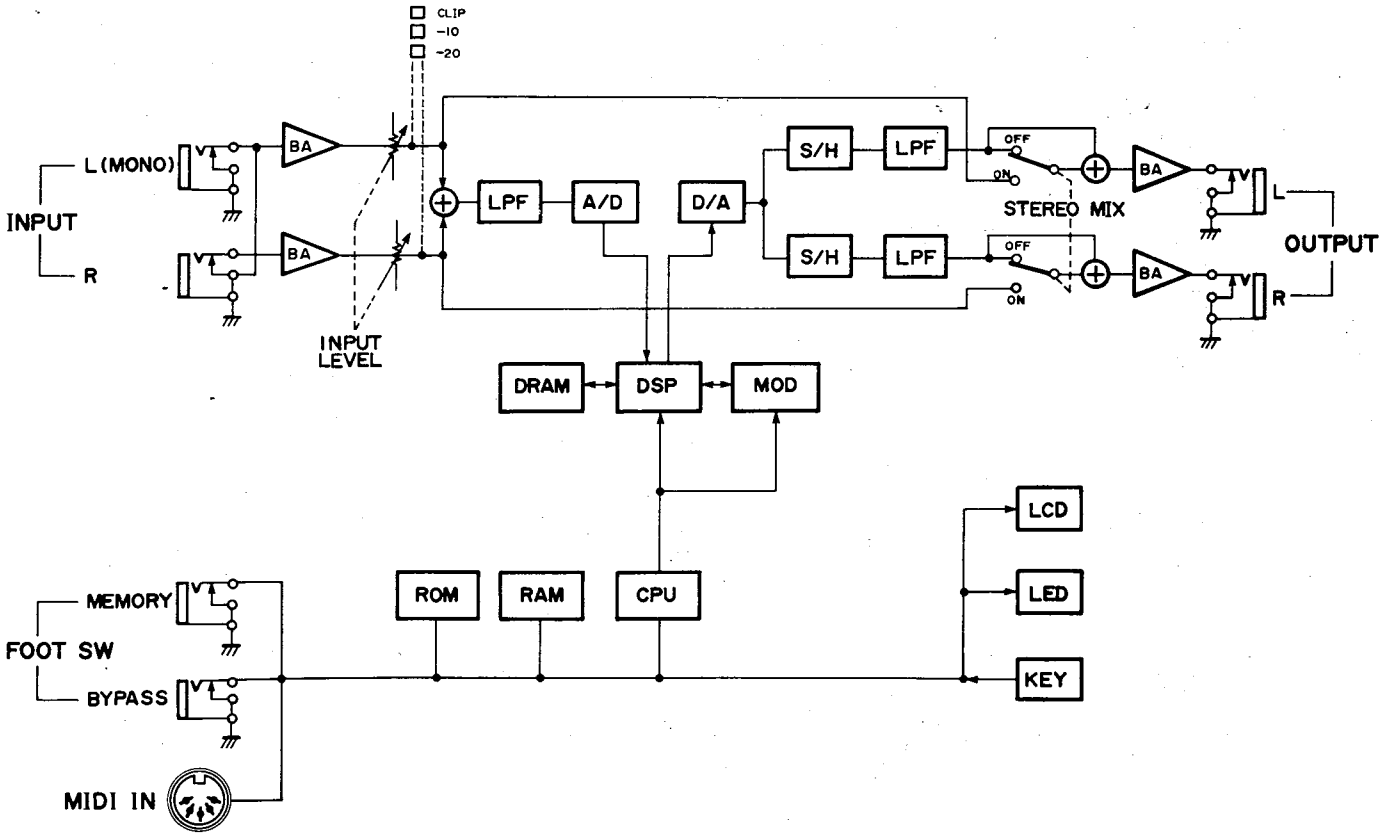
●Front Panel（フロントパネル）



●Rear Panel（リアパネル）



■ BLOCK DIAGRAM (ブロックダイアグラム)



■ LSI DATA TABLE (LSI端子機能表)

● HD63B50P (iG147300) Asynchronous Communications Interface Adapter

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		DC supply 0V	13	R/W	I	Read/Write
2	Rx Data	I	Receive data	14	E	I	Enable
3	Rx CLK	I	Receive clock	15	D7	I/O	Data bus
4	Tx CLS	O	Transmit clock	16	D6	I/O	
5	$\overline{RTS}$	I/O	Request to send	17	D5	I/O	
6	Tx Data	O	Transmit data	18	D4	I/O	
7	$\overline{IRQ}$	I	Interrupt request	19	D3	I/O	
8	CS0	I	Chip select	20	D2	I/O	
9	CS1	I		21	D1	I/O	
10	$\overline{CS2}$	I		22	D0	I/O	
11	RS	I	Resist select	23	$\overline{DCD}$	I	Data carrier detect
12	Vcc		DC supply (+5.0V)	24	$\overline{CTS}$	I	Clear to send

● PCM54HP (XA566001) Digital to Analog Converter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	Vpot		Not used	15	DA4		Bit 13
2	DA16		Bit 1 (MSB)	16	DA3		Bit 14
3	DA15		Bit 2	17	DA2		Bit 15
4	NC		Not used	18	LSB		Bit 16
5	DA14		Bit 3	19	V_O		Voltage Output
6	DA13		Bit 4	20	FBR		Not used
7	DA12		Bit 5	21	INV		Summing Junction
8	DA11		Bit 6	22	GND		Common
9	DA10		Bit 7	23	I_O		Current Output
10	DA9		Bit 8	24	NC		Not Used
11	DA8		Bit 9	25	OFF·S		Not Used
12	DA7		Bit 10	26	+Vcc		+15V
13	DA6		Bit 11	27	ADJ		Not used
14	DA5		Bit 12	28	−Vcc		−15V

● HD6303RF (XC715001) CPU

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		Ground	28	A15	O	Address bus
2	XTAL	I	Clock	29	A14	O	
3	EXTAL	I		30	A13	O	
4	$\overline{NMI}$	I	Non-maskable interrupt	31	A12	O	
5	$\overline{IRQ1}$	I	Interrupt request	32	A11	O	
6	NC			33	NC		
7	NC			34	NC		
8	$\overline{RES}$	I	Reset	35	A10	O	Address bus
9	$\overline{STBY}$	I	Stand-by mode signal	36	A9	O	
10	NC			37	A8	O	
11	P20	I/O	Port 2	38	NC		
12	P21	I/O		39	NC		
13	P22	I/O		40	D7/A7	I/O	Data/Address bus
14	P23	I/O		41	D6/A6	I/O	
15	P24	I/O		42	D5/A5	I/O	
16	NC			43	D4/A4	I/O	
17	NC			44	D3/A3	I/O	
18	A0/P10	I/O	Address bus (/Port 1)	45	D2/A2	I/O	
19	A1/P11	I/O		46	NC		
20	A2/P12	I/O		47	NC		
21	NC			48	NC		
22	A3/P13	I/O	Address bus (/Port 1)	49	NC		
23	A4/P14	I/O		50	D1/A1	I/O	Data/Address bus
24	A5/P15	I/O		51	D0/A0	I/O	
25	A6/P16	I/O		52	R/W	O	Read/Write control
26	A7/P17	I/O		53	AS	O	Address strobe
27	Vcc		Supply power	54	E		Enable

● HD63B21FP (XC716001) Peripheral Interface Adapter

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		Ground	28	R/$\overline{W}$	I	Read/Write control
2	PA0	I/O	Data bus, A	29	$\overline{CS0}$	I	Chip select
3	PA1	I/O		30	$\overline{CS2}$	I	
4	PA2	I/O		31	CS1	I	
5	PA3	I/O		32	E	I	Enable
6	NC			33	NC		
7	NC			34	NC		
8	NC			35	NC		
9	PA4	I/O	Data bus, A	36	D7	I/O	Data bus
10	PA5	I/O		37	D6	I/O	
11	PA6	I/O		38	D5	I/O	
12	PA7	I/O		39	D4	I/O	
13	PB0	I/O	Data bus, B	40	D3	I/O	
14	PB1	I/O		41	D2	I/O	
15	PB2	I/O		42	D1	I/O	
16	PB3	I/O		43	$\underline{D0}$	I/O	
17	PB4	I/O		44	$\overline{RES}$	I	Reset
18	PB5	I/O		45	RS1	I	Register select
19	NC			46	NC		
20	NC			47	NC		
21	NC			48	NC		
22	NC			49	NC		
23	PB6	I/O	Data bus, B	50	$\underline{RS0}$	I	Registor select
24	PB7	I/O		51	$\overline{IRQB}$	O	Interrupt request, B
25	CB1	I/O	Control, B	52	$\overline{IRQA}$	O	Interrupt request, A
26	CB2	I/O		53	CA2	I/O	Control, A
27	Vcc		DC supply	54	CA1	I	

● YM3804 (iT380400) Digital Signal Processor

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	D15	I.O	Data bus	64	VSS		Ground
2	D14	I.O		63	D16	I.O	Data bus
3	D13	I.O		62	D17	I.O	
4	D12	I.O		61	D18	I.O	
5	D11	I.O		60	D19	I.O	
6	D10	I.O		59	D20	I.O	
7	D9	I.O		58	D21	I.O	
8	D8	I.O		57	D22	I.O	
9	D7	I.O		56	D23	I.O	
10	D6	I.O		55	MOD0	I	MOD data input terminal
11	D5	I.O		54	MOD1	I	
12	D4	I.O		53	MOD2	I	
13	D3	I.O		52	MOD3	I	
14	D2	I.O		51	MOD4	I	
15	D1	I.O		50	MOD5	I	
16	D0	I.O		49	MOD6	I	
17	ST1	I	Serial data input terminal	48	MOD7	I	
18	ST0	I		47	$\overline{IC}$	I	Initial clear
19	SO1	O	Serial data output terminal	46	CE	I	Chip enable
20	SO0	O		45	CLK	I	Master clock input terminal
21	XMD	I	Select internal ACIA synchronization mode	44	SYW	I	Input for generating SYNC signals internally
22	XCLK	I	Time-out output terminal	43	$\overline{TSTI}$	I	Terminal for internal test. To enter test mode, connect to GND. When in use, VDD.
23	$\overline{TO}$	O	Time-out output terminal	42	$\overline{TSTR}$	I	
24	$\overline{CRS}$	I	CD counter reset	41	A0	O	Address bus
25	CDO	O	CD data output terminal	40	A1	O	
26	CDI	I	CD data input terminal	39	A2	O	
27	TIMI	O	Unconditionally outputs the 15th bit of the Address Shift Register	38	A3	O	
28	$\overline{REF}$	O	Three-state. Memory which needs refreshing.	37	A4	O	
29	OE	O	Three-state. Connect to memory OE.	36	A5	O	
30	R/W	O	Three-state. Memory read/write signal.	35	A6	O	
31	CAS	O	Three-state. DRAM control signal	34	A7	O	
32	RAS	O	Three-state.	33	VDD		Power supply 5V

● YM3807 (iT380700) Modulation Data Generator

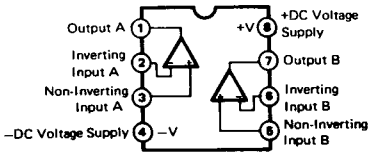
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	NC			24	VSS		Power supply ground
2	MDSI0	I	Inputs data to add to the wave-form data inside MOD	23	CDO	O	CD interface serial data output
3	MDSI1	I		22	CDI	I	CD interface serial data intput
4	MDSO0	O	Outputs MOD internal wave-form data with the same data format as MDSIO.	21	NC		
5	MDSO1	O		20	XCLK	I	CD interface transmission clock input
6	MD0	O	Outputs waveform data for all channels inside MOD.	19	XMD	I	Selects 1/16 mode (asynchronous) or 1/1 mode (synchronous) for the CD interface
7	MD1	O		18	$\overline{CRS}$	I	CD counter reset
8	MD2	O		17	CLK	I	3.2MHz
9	MD3	O		16	$\overline{IC}$	I	Initial clear
10	MD4			15	SYW	I	Sync signal input. One 64th of the master clock.
11	MD5	O		14	MD7	O	Outputs waveform data for all channels inside MOD.
12	VDD		Power supply +5V	13	MD6	O	

● YM3901 (XC282001) ADA

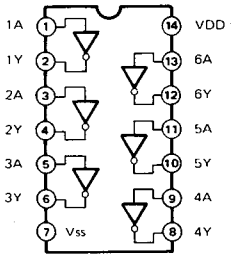
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MCLK	I	System clock	33	DA1	O	Outputs Parallel data 1 to DAC
2	SYIN	I	Input of system synch. signal	34	DA2	O	Outputs Parallel data 2 to DAC
3	SYO	O	Output of system synch. signal	35	DA3	O	Outputs Parallel data 3 to DAC
4	REST	I	System reset signal, except Ran. gen.	36	DA4	O	Outputs Parallel data 4 to DAC
				37	DA5	O	Outputs Parallel data 5 to DAC
5	DRST	I	Reset signal for Randam generator	38	DA6	O	Outputs Parallel data 6 to DAC
				39	DA7	O	Outputs Parallel data 7 to DAC
6	MD0	I	Selecting system mode	40	DA8	O	Outputs Parallel data 8 to DAC
7	MD1	I		41	GND	I	Ground (Earth) Terminal
8	MD3	I		42	DA9	O	Outputs Parallel data 9 to DAC
9	DIC0	I	Mode selection for Diser	43	DA10	O	Outputs Parallel data 10 to DAC
10	GND	I	Ground (Earth) Terminal	44	DA11	O	Outputs Parallel data 11 to DAC
11	DIC1	I	Mode selection for Diser	45	DA12	O	Outputs Parallel data 12 to DAC
12	DN	I	Selection of ser. data format ($\overline{DSP}$/Normal)	46	DA13	O	Outputs Parallel data 13 to DAC
				47	DA14	O	Outputs Parallel data 14 to DAC
13	TD	I	For test, external synch. control	48	DA15	O	Outputs Parallel data 15 (MSB) to DAC
14	TNC	I	Selection of ser. Input data mode at MODE 0 or 3 (Time sharing/NOT)	49	CPIN	I	Inputs the output signal of comparator, at successive approximation
15	DLY0	I	Selection of Phase lag value for DIN 1, 2				
16	DLY1	I		50	ADCK	O	Inner successive comparating register CLOCK
17	DIN1	I	Inputs serial data for DAC				
18	DIN2	I		51	SH1	O	Sample/hold signal 1, Outputs SW sel. signal at MODE 1.
19	DOUT	O	Outputs serial data after AD converting	52	SH2	O	Sample/hold signal 2 (Mode 2 : Switch sel. signal) (Mode 4 : De-glitch signal 3)
20	DDO1	O	Outputs serial data of phase delay for DIN 1, 2				
21	DDO2	O					
22	DAOVC /PRIN	I	Over flow control terminal for DA. GND : OFF, 5V : ON or PRCN : 5V; Initialization of randam number	53	ASW1	O	Outputs switch select signal
				54	SDEN	O	Latch enable signal for data input from DIN 1, 2
				55	SDOUT	O	Converted data input DIN 1, 2 to serial data (out)
23	PRCN	I	For test, at 5V initialization of randam number	56	MPX1	O	For test, select data out
				57	REG1	O	For test, enable signal of register out
24	TM1	O	Outputs timming signal				
25	D32	O	More delayed 32 bit in DIN 2 are output	58	VDD	I	+5V DC voltage
				59	MPX3	O	For test, select signal out
26	VDD	I	+5V DC voltage	60	DEGL11	O	De-glitch signal 11
27	OVFL	O	Outputs over flow signal after AD converting (Active L)	61	DEGL12	O	De-glitch signal 12
				62	REG3	O	For test, enable signal for register 3
28	PRDL	O	Outputs the timming of input for output serial ran. data from PRDO	63	ADCX	O	For test, outputs control signal of clock for successive approximation
29	PRDO	O	Outputs ser. randam data (Two comp. data) for YM3015, 3020				
30	DEG1	O	Outputs De-glitch signal	64	ADST	O	For test, outputs start signal for successive approximation
31	DEG2	O					
32	DAO	O	Outputs Parallel data 0 (LSB) to DAC				

■ IC BLOCK DIAGRAM (ICブロック図)

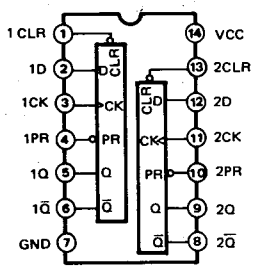
● **NJM4558MT-1** (iG103520)
● **M5238FP** (XB496001)
Dual Operational Amplifier



● **SN74HCU04NSR** (XC723001)
Hex Inverter

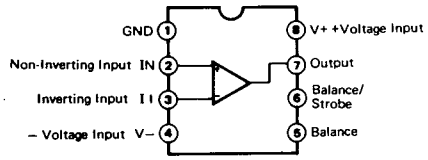


● **SN74HC74NSR** (XC726001)
Dual D-Type Flip-Flop

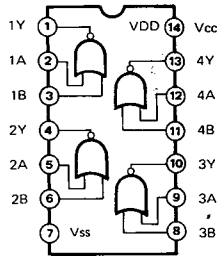


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

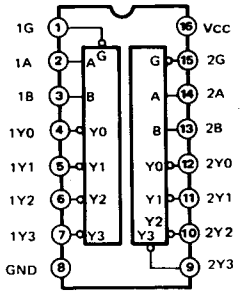
● **NJM311MT-1** (XC714001)
Comparator



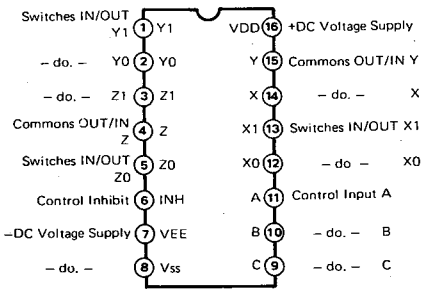
● **SN74HC02NSR** (XC724001)
Quad 2 Input NOR



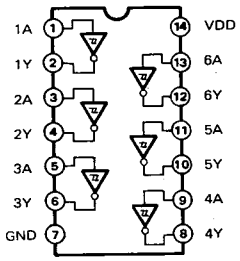
● **SN74HC139NSR** (XC727001)
Dual 2 to 4 Demultiplexer



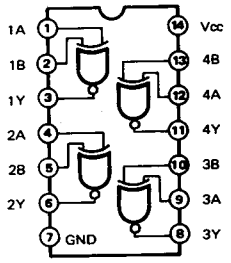
● **TC4053BF-T1** (XB738001)
Triple 2-Ch.
Multiplexer/Demultiplexer



● **SN74HC14NSR** (XC725001)
Hex Inverter



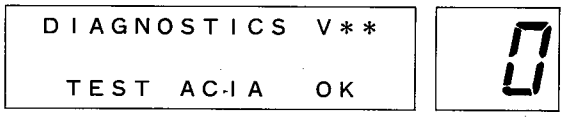
● **SN74LS266NSR** (XC728001)
Quad 2 Input O.C. Ex-NOR



■ TEST PROGRAM

● Test Program Entry

While pressing the BYPASS and MEMORY switches, turn the POWER switch on. If the Test Program is activated, the ACIA test will be performed, the LCD display will then indicate the message as shown below.



● Selection of each routine of the test program

(1) Press the MEMORY switch.

(2) After selecting the disired routine with the ↑ and ↓ switches, press the RECALL switch to initiate the Test Program.

*The 7-segments LEDs will display the Test Program number.

1. TEST1 : LCD check

If this test is initiated, the entire LCD will be turned "ON and OFF" repeatedly. When proper lighting of LCDs has been verified, advance the Test Program to next routine.

2. TEST 2 : LED check

If this test is initiated, the 7-segments LEDs will illuminate in the sequence of 00, 11, 22 to 99. Afterwards all segments of the LED display will light simultaneously for about three seconds. When proper lighting of LEDs has been verified, advance the Test Program to the next routine.

3. TEST 3 : Switch check

If this test is initiated, switch number 00 will appear in the LCD display, as shown below.

Press the switch that is indicated by the LCD display.

Pressing the correct switch will advance the switch test.

Switch number	Switch name
00	MEMORY
01	PARAM
02	↑
03	↓
04	STORE
05	RECALL
06	UTILITY
07	BYPASS

Upon completion of these tests, the LCD display indicates the message as shown below, and then advance the Test Program to the next routine.

If an incorrect switch is pressed, the LCD will display an error message as shown below.

If the RECALL switch is pressed, the switch test will be initiated again.

4. TEST 4 : A/D check

Before entering this test,connect the L and R OUTPUT to a power amplifier so that sound can be heard from speakers. If an offset voltage is present, a clicking sound will be produced. Adjust VR103 on the RV circuit board, so that the clicking sound is minimized.

5. TEST 5 : Setting user memories

If this test is initiated, the LCD display will indicate the message as shown below.

```
DIAGNOSTICS V**
RESET USER PRG?
```

(1) If you select another Test Program, this test will not be performed.

(2) If the STORE switch is pressed, the contents of MEMORY 1—30 will be copied to MEMORY 31—90 and the LCD display will then indicate the message as shown below.

```
DIAGNOSTICS V**
SET USER PRG.
```

6. TEST 10—17 : DRAM check

If these tests are initiated, the LCD display will indicate the code which corresponds to the appropriate test as shown in Table below.

```
DIAGNOSTICS V**
TEST DRAM □□□
```

Test No.	MSB			LSB	□□□
10	IC125	IC126	IC127	IC128	THR
11	IC126	IC127	IC128	IC129	04B
12	IC127	IC128	IC129	IC130	08B
13	IC128	IC129	IC130	0000	12B
14	IC129	IC130	0000	0000	16B
15	IC130	0000	0000	0000	20B
16	1000	0000	0000	0000	−MX
17	0111	1111	1111	1111	+MX

7. TEST 6

After completion of Test 1—5, if the Test Program 6 is initiated, the test routine will reset the system to the normal operating mode.

If the Test 1—5 are not performed and the Test 6 is initiated, the LCD display will indicate an CHECK NOT END message as shown below.

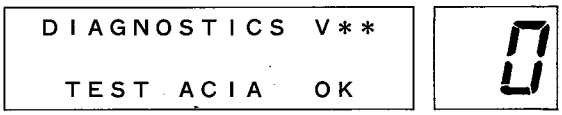
```
DIAGNOSTICE V1.0
CHECK NOT END
```

If the Test Program 90 is selected and the RECALL switch is pressed, the routine will reset the system to the normal operating mode.

■ テストプログラム

●テストプログラムの起動方法

BYPASSキーとMEMORYキーを押しながら、POWER SWをONします。
テストプログラムが起動した場合、下記の様に表示されます。



●テストプログラムの選択方法

MEMORYキーを押し、↑及び↓キーにて所定のテストプログラムナンバーを選択した後、RECALLキーを押します。

テストプログラムナンバーは、7セグメントLEDに表示されます。

1．TEST1：LCD表示器の動作チェック

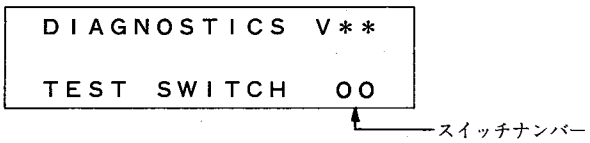
テストプログラムナンバー〝1〟を選択し、RECALLキーを押します。
LCDの全表示ドットが5回点滅します。全てのドットが点灯するか目視により確認します。

2．TEST2：LED点灯チェック

テストプログラムナンバー〝2〟を選択し、RECALLキーを押します。
〝00.11.22～99〟を表示した後、全セグメントを約3秒間表示します。全てのＬＥＤが点灯するか目視により確認します。

3．TEST3：スイッチの動作チェック

テストプログラムナンバー〝3〟を選択し、RECALLキーを押します。
下記の様に表示され、スイッチナンバーが点滅します。



LCDに表示されたスイッチを押します。

(1) 00 が点滅したら　MEMORYキーを押します。
(2) 01　〃　PARAM キー　〃
(3) 02　〃　↑ キー　〃
(4) 03　〃　↓ キー　〃
(5) 04　〃　STORE キー　〃
(6) 05　〃　RECALL キー　〃
(7) 06　〃　UTILITY キー　〃
(8) 07　〃　BYPASS キー　〃

スイッチを押しても、LCDに表示されているスイッチナンバーが進まない場合は、スイッチの不良と考えられます。
(1)～(8)が順番通りに押されなかった場合、ＮＧが表示されます。この場合は、RECALLキーを押して、TEST3を最初から行なって下さい。

4．TEST4：A/Dオフセットチェック

OUT PUT 〝L〟又は〝R〟端子をパワーアンプに接続し、スピーカーにて音が聞ける様にします。
次に、テストプログラムナンバー〝4〟を選択し、RECALLキーを押すと､オフセット電圧があった場合、スピーカーからクリック音が出ます。
このクリック音を聞きながら、ＲＶシート上の調整用半固定ボリュームVR103(OFF SET)を動かして、クリック音が最小になる様に調整します。

5．TEST5：USER MEMORYのセッティング（コピー機能）

テストプログラムナンバー〝5〞を選択し、RECALLキーを押すと、下記の様に表示されます。

```
DIAGNOSTICS V**
RESET USER PRG?
```

STOREキーを押すと、メモリーNo.1～30の内容が、No.31～90にコピーされます。

```
DIAGNOSTICS V**
SET USER PRG.
```

《コピー完了表示》

コピーしない場合…他のテストプログラムナンバーを選択します。

6．TEST10～17：DRAMチェック

テストプログラムナンバー〝10～17〞を選択し、RECALLキーを押すと下表のようにDRAMチェックが行なわれ、LCDには、次の様に表示されます。

```
DIAGNOSTICS V**
TEST DRAM □□□
```

テストプログラムナンバー	MSB側			LSB側	□□□
10	IC125	IC126	IC127	IC128	THR
11	IC126	IC127	IC128	IC129	04B
12	IC127	IC128	IC129	IC130	08B
13	IC128	IC129	IC130	0000	12B
14	IC129	IC130	0000	0000	16B
15	IC130	0000	0000	0000	20B
16	1000	0000	0000	0000	−MX
17	0111	1111	1111	1111	+MX

●テストプログラムから通常動作への復帰

TEST1～5を全て終了してから、テストプログラムナンバー〝6〞を選択し、RECALLキーを押せば、通常動作に戻ります。

TEST1～5を全て終了させずに、テストプログラムナンバー〝6〞を選択し、RECALLキーを押すと、下記の様に表示されます。

```
DIAGNOSTICE V1.0
CHECK NOT END
```

この場合は、テストプログラムナンバー〝90〞を選択し、RECALLキーを押すと、通常動作に戻ることが出来ます。

＊ROM、S-RAMのチェックサム、リード、ライトテスト及びDSP、MODの制御回路のチェックは、通常動作時に、POWER SWをONすると、自動的に行なわれます。

■ ADJUSTMENTS

1-1. Preparation Instructions

- Unless otherwise specified, the volume and switch on the rear panel are to be set as follows.

  INPUT LEVEL ..... maximum
  STEREO MIX ..... off

- Leave the slide switches SW102 and SW103 on the circuit board set to the Test position.
- The load of the L and R OUTPUT connectors are to each be serially connected to a load resistor (10KΩ).

2. Inspection

2-1. Apply an input signal of −5.5dBm at 1kHz to the INPUT L connector and adjust VR102 so that the output signal is clipping slightly at the L OUTPUT connector. Adjust VR103 so that the clipping signal is vertically symmetrical (Obserb the distortion waveforms by utilizing the monitor output of the distortion meter or connect the oscilloscope to the output load).

2-2. Afterwards, adjust VR102 until the distortion waveforms of the L OUTPUT connector for minimum distortion.

2-3. With the same input conditions as stated in section 2-1, adjust VR104 so that the output signal of the L OUTPUT connector becomes +4.5 ± 0.5dBm.

3. Gain

Apply an input signal of −6dBm at 1kHz to the L and R INPUT connectors, output signals of the level listed in the table below are obtained at the L and R OUTPUT connectors.

INPUT	OUTPUT
L ch	+4 ± 1 dBm
R ch	−2 ± 1 dBm
L and R ch	+4 ± 1 dBm

4. Frequency Characteristics

When an input signal of approximately −20dBm is applied to the L INPUT connector, the frequency characteristics of the L and R OUTPUT connectors are within the range listed in the table below. The reference frequency used is 1kHz.

20 Hz − 11 kHz	0 ± 2 dB
12 kHz −	$-1\ ^{+2}_{-3}$ dB

5. Output Distortion Factor

Apply an input signal of 1kHz to the L INPUT connector according to the conditions of section 3, the distortion factor should be less than 0.08%.

6. Maximum Output

When a 1kHz input signal is applied to the L INPUT connector according to the conditions of section 1, the maximum level of the output signal at the L and R OUTPUT connectors should be +4dBm with a distortion factor of less than 0.1%.

7. Meter Sensitivity

When 1kHz input signals are applied to the L and R INPUT connectors according to the conditions of section 1, and the input signals have been adjusted so that the output signals of the table below can be obtained at the L OUTPUT connector. At that point, the LED indicators of the level meter are illuminated as shown in the table below.

OUTPUT	Level meter		
	CLIP	−10	−20
+5.0 dBm	ON	ON	ON
−5.0 dBm	OFF	ON	ON
−14.0 dBm	OFF	OFF	ON
Input is opened	OFF	OFF	OFF

If the LED indicators are not working in conditions as shown in the table, adjust the input signals so that the output signals are within ±4dB and verify proper lighting of the LED indicators.

8. Muting Circuit

After the POWER switch is turned ON, muting is effective for two to four seconds, and no output signals are generated. After this time delay output signals can be obtained at each OUTPUT connector.

9. Noise Level Adjustment

After performing spections 2 through 8, set the slide switches SW101 and SW102 on the circuit board to the Normal position and press the BYPASS switch. When the INPUT is opened, the noise levels of the L and R OUTPUT connectors should be less than −76dBm. If noise levels are not within rated levels, adjust VR103 on the circuit board so that the noise levels are within rated values.

■調整

1-1. 準備

○リアパネルの〝INPUT〟VOL(VR101)
…… MAX
○リアパネルの〝STEREO MIX〟SW(SW103)
…… OFF
○シート内のSW(SW101、102)…… 〝T〟側
○L、R各〝OUTPUT〟端子負荷 …… 10kΩ

1-2. 測定器

(1) 歪率測定時は80kHz −6dB/OCTのフィルターを使用のこと。
(2) ノイズレベル測定時は12.7kHz −6dB/OCTのフィルターを使用のこと。
(3) 発振器の出力インピーダンスは600Ω以下のこと。
(4) 測定器の入力インピーダンスは1MΩ以上のこと。

2. 調整

2-1. 1の項の状態でINPUT L端子に−5.5dBm/1kHzの入力を加え、〝OUTPUT〟L(又はR)端子の出力信号が少し歪み始める位にVR102を調整し、信号が上、下対称に歪み始める様にVR103を調整します。(この時、歪み波形は歪率計のモニター出力で見ます。)

2-2. 2-1の後に、〝OUTPUT〟L(又はR)端子の出力信号において、歪波形が出なくなる様にVR102を再調整します。(歪波形が出る直前の位置に調整します。)

2-3. 2-2の状態で〝OUTPUT〟L(又はR)端子の出力信号が+4.5 ± 0.5dBmになる様にVR104を調整します。

3. 利得

〝INPUT〟各端子に−6dBm/1kHzの入力信号を加えた時、〝OUTPUT〟L及びR端子に下記の出力信号が、得られること。

INPUT端子	OUTPUT端子
L-Chのみ	+4 ± 1 dBm
R-Chのみ	−2 ± 1 dBm
L、R-CH	+4 ± 1 dBm

4. 周波数特性

〝INPUT〟L端子に約−20dBmの入力信号を加えた時、L、Rの各〝OUTPUT〟端子での周波数特性は1kHzを基準として、下記の範囲内のこと。

20Hz ～ 11kHz	0 ± 2 dB
12kHz ～	$-1\ ^{+2}_{-3}$ dB

5. 歪率

3の項でL-Chのみ−6dBmを入力した時、各〝OUTPUT〟端子での歪率は0.08%以下のこと。

6. 最大出力

1の項の状態で〝INPUT〟L端子に1kHzの入力信号を加えた時、L、Rの各〝OUTPUT〟端子に+4dBmの出力信号が歪率0.1%以下で得られること。

7．メーター感度

1の項の状態で〝INPUT〟L、Rの各端子に1kHzの入力信号を加えて〝OUTPUT〟L端子に +5.0 dBm、−5.0dBm、−14.0dBmの各出力信号が得られるよう、入力信号を調整した時、レベルメーターの表示が下表のようになること。

LED / 出力	CLIP (アカ)	−10 (キ)	−20 (キ)
+5.0 dBm	点　灯	点　灯	点　灯
−5.0 dBm	消　灯	点　灯	点　灯
−14.0 dBm	消　灯	消　灯	点　灯
無信号	消　灯	消　灯	消　灯

尚、上記の出力レベルで点灯、消灯しない場合は出力レベルを±4dB以内で変化させて動作すればOKとします。

8．ミューティング回路

パワースイッチ（SW112）をONした後、2～4秒間〝OUTPUT〟端子に出力信号が出力されず、その後各〝OUTPUT〟端子に出力信号が得られること。

9．ノイズレベル

2～8まで検査した後、シート内スライドSW（SW101、102）を〝N〟（NORMAL）側にセットし、〝BYPASS〟SWをONします。この状態で無信号入力時の〝OUTPUT〟L、R各端子のノイズレベルは−76dBm以下のこと。

この時規格に入らない場合は、VR103を最小限動かして、ノイズレベルが規格以下になる位置に調整する。

REX50 [Digital Multi Effector] Date : 5/7, 1987

Model REX50 MIDI Implementation Chart Version : 1.0

Function ...		Recognized		Remarks
Basic	Default	1 - 16		memorized
Channel	Changed	1 - 16		
Mode	Default	OMNI OFF/OMNI ON		memorized
	Messages	x		
	Altered	x		
Note Number		o 0 - 127	*1	
	True voice	x		
Velocity	Note ON	x		
	Note OFF	x		
After Touch	Key's	x		
	Ch's	x		
Pitch Bender		x		
Control Change		x		
Prog Change	True #	o 0 - 127	*2	
System Exclusive		o		
System Common	Song Pos	x		
	Song Sel	x		
	Tune	x		
System Real Time	Clock	x		
	Commands	x		
Aux Mes- sages	Local ON/OFF	x		
	All Notes OFF	x		
	Active Sense	x		
	Reset	x		
Notes		*1 Note ON/OFF is recognized only for pitch change.		
		*2 For program 1 - 128, memory #1 - #90 is selected.		

Mode 1 : OMNI ON, POLY Mode 2 : OMNI ON, MONO o : Yes
Mode 3 : OMNI OFF, POLY Mode 4 : OMNI OFF, MONO x : No

1. Circuit Board: XC633C0
2. IC
   - IC 101~103, 110, 111: NJM4558MT-1(IG103520)OP AMP.
   - 104, 109: M5238FP(XB496001)OP AMP.
   - 105: NJM311MT-1(XC714001)COMPARATOR
   - 106, 137: TC4053BF-T1(XB738001)MPX
   - 107: PCM54HP(XA566001)DAC
   - 108: YM3901(XC282001)ADA
   - 113, 114, 140: SN74HC74NSR(XC726001)DFF
   - 115: SN74HCU04NSR(XC723001)INV
   - 116: SN74HC14NSR(XC725001)INV
   - 117: SN74HC02NSR(XC724001)NOR
   - 118: SN74LS266NSR(XC728001)EX-NO
   - 119: HD6303RF(XC715001)8 bit CPU
   - 120: (XD015002)EPROM
   - 121: TC5565AFL-15(XC717001)SRAM
   - 122: SN74HC139NSR(XC727001)DECO
   - 123: HD63B50P(IG147300)ACIA
   - 124: HD63B21FP(XC716001)8 bit PIA
   - 125~130: M5M4416P-12(IG122320)64K DR
   - 131: YM3804(IT380400)DSP
   - 132: YM3807(IT380700)MOD
   - 133: PST518A-2(XC722001)RESET
   - 134: NJM7812FA(XC720001)12V Regulator
   - 135: NJM7912FA(XC721001)—12V Regulator
   - 136: NJM7805FA(XC719001)5V Regulator
3. Photo Coupller
   - IC 112: PC-900
4. Transistor
   - Q 101: 2SC3064-6B F, G
   - 102, 103, 106, 108, 111, 112, 115: 2SA1037K Q, R, S
   - 104, 105, 107, 113, 116, 119~127: 2SC2412 Q, R, S
   - 109, 110, 114: 2SC3326 B
   - 117, 118: 2SC2411K P, Q, R
5. Diode
   - D 107~112: RLS-73
   - 113~123: 10E-1
6. Zener Diode
   - ZD 101: RLZ5.6B
7. LED
   - LED101: SLP-153B RE
   - 102, 103: SLP-453B YE
   - 104: SL-1284-20
8. Resistor Array
   - MR101~103: EXB-F9E472J5 4.7K x 8
   - 104~106: EXB-F9E103J5 10K x 8
9. Diode Array
   - D 101~106: 1SS226 TE85R
10. Potentiometer
    - VR 101: A10K x 2 EVJRBA01
    - 102, 103: B50K 3P EVN
    - 104: B10K 3P EVN
11. Ceramic Cap.
    - C 167, 168: 2200P 400V
    - 169: 0.1μ
    - 171, 172: 4700P 400V H, D, A
12. Coil
    - L 101: PLA3021A
    - 102~106: 20μ FL5R200QNT
13. LC Filter
    - LPF101~103: TFB-3B
14. Ceramic Resonator
    - X 101: 4MHz KBR-4MSTR
15. Switch
    - SW101, 102: SSS212
    - 103: SUJ
    - 104~111: KHH10908
    - 112: 1801.5423
16. Lithium Battery
    - E 101: CR2032T15