

# AN2533/AN2553

UNIVERSAL, BIPOLAR

±3 1/2-DIGIT (±1999-COUNT)

## DIGITAL PANEL INSTRUMENT

The AN2533/AN2553 breakthrough instrument design reflects Analogic's world leadership in digital panel instrumentation . . . and the experience gained in producing more than 250,000 instruments.

Never before has the OEM user been offered so many and varied opportunities to incorporate "value-added" features into a digital panel instrument - - - increasing the profitability of his product, and exploiting fully his own design expertise. In fact, by standardizing on either of the two configurations, most OEM users can satisfy all of their 3 1/2 digit DPI requirements.

The AN2553 is the more versatile configuration. Its design includes an internal power and signal interface connector which accepts a general purpose plug-in card on which the user can install proprietary analog-interface circuitry. . . . or Analogic can add the special purpose circuitry during manufacture, whichever is more economical. (Typical analog-interface functions that may be provided are: ac and dc current measurement, extended range ac and dc voltage measurement, active multipole filtering, information reinforcement filtering, thermocouple or RTD temperature transducer conditioning, LVDT excitation and demodulation, frequency-to-voltage conversion, current sourcing, auto-ranging, and ultra high impedance buffering.)

The AN2553 and AN2533 both provide power and space for an optional digital circuit card for such add-in features as isolated parallel BCD output, digital linearization, and set-point control. Here again, the add-ons may be provided by the user, or, for quantity requirements, engineered and built in by Analogic.

The AN2533 provides the same advanced performance features and inherent versatility of the AN2553, except that the analog-interface connector is omitted. The basic design common to both is so flexible and adaptable that this lower cost version provides far more value-added application freedom than any conventional design.

In either configuration, exceptional confidence in high quality and reliability is warranted by: (1) Application of worst-case error analysis to ensure specification integrity throughout rated life; (2) Minimizing the component count without "corner-cutting;" (3) Exclusive use of premium, field-proven components; (4) 100% burn-in of all IC's; (5) Use of CMOS digital circuitry resulting in extremely low internal temperature rise (less than 10°C); (6) Generous derating margins; (7) 100% testing of subassemblies; (8) 4-day burn-in of all completed instruments before final test; and (9) Comprehensive, detailed quality-assurance procedures.

Design features that contribute to the wide-range versatility of this design include: a true symmetrical front end; dual-slope, long-period signal integration; choice of bright, luminous, 0.55" (14mm) gas plasma or 0.43" (11mm) LED display; common-mode rejection ratios up to 160dB; normal mode rejection ratios up to 100dB; and a universal 100/117/220/240 Vac power supply.

Compare 3 1/2-Digit Instruments - Study all available specifications. Consider this instrument's potential to maximize the value added to your product. We believe you will agree that we have made available the best general purpose DPI to fulfill present and foreseeable measurement needs.

### FEATURES

- **ACCURACY AND STABILITY**  
Resolution: ± 1999 counts  
Error: Less than ±0.05% Rdg ± 1 count  
Noise: Deadband less than 0.1 count  
Temperature Coefficient: <35ppm/°C typical
- **DISPLAY OPTIONS**  
0.55" (14mm) gas plasma or 0.43" (11mm) LED, self-illuminating  
Automatic polarity  
Pin-selectable decimal points  
Dummy Zeros
- **UTMOST RELIABILITY**  
Low parts count; yet incorporating those needed for safe performance margins  
Cool operation:  
only 2 watts power consumption  
low-power CMOS circuitry  
Standard, proven, volume-production IC chips
- **USE-ORIENTED INPUT CONDITIONING**  
True-differential, balanced symmetrical inputs†  
Low bias current  
High input impedance  
Built-in signal offsetting capability
- **VERSATILE CONTROLS**  
External run/hold  
Remote display control  
User-selectable full scale range
- **UNIVERSAL POWERING**  
Universal transformer; pin connectable  
100, 117, 220 or 240Vac, 49 to 500Hz  
Highly regulated internal supply voltages;  
+5V, +12V, -12V with excess capability
- **PROVEN INTERFERENCE REJECTION**  
High CMRR & NMRR capabilities  
Built-in "reflective" line filter
- **ADAPTABLE MECHANICAL PROVISIONS**  
International DIN/NEMA standard case  
UL 94V-0 Rated  
Front-panel removeable, † easily serviced
- **WIDE ENVIRONMENTAL RANGE**  
Operating temperature range: -10°C to +60°C  
High rejection of electric fields  
Operational in harsh shock & vibration stresses

- **OEM INSTRUMENT-TO-PRODUCT TRANSFORMATIONS**  
By plug-in PC-board assemblies for thermocouple and RTD temperature indicators; pH meters; load cell, bridge, and LVDT weight, force, and pressure instrumentation; etc.
- **SYSTEM-COUPLING OF ANALOG INPUTS AND DIGITAL OUTPUTS**  
Low input bias currents: to fractions of picoamperes!  
Very high impedance input circuits: to 10<sup>12</sup> ohms!  
Isolated and buffered parallel BCD outputs  
Power-sharing and coupling capabilities

†U.S. Patent numbers 3718923, 3751717, 3751791 and others pending

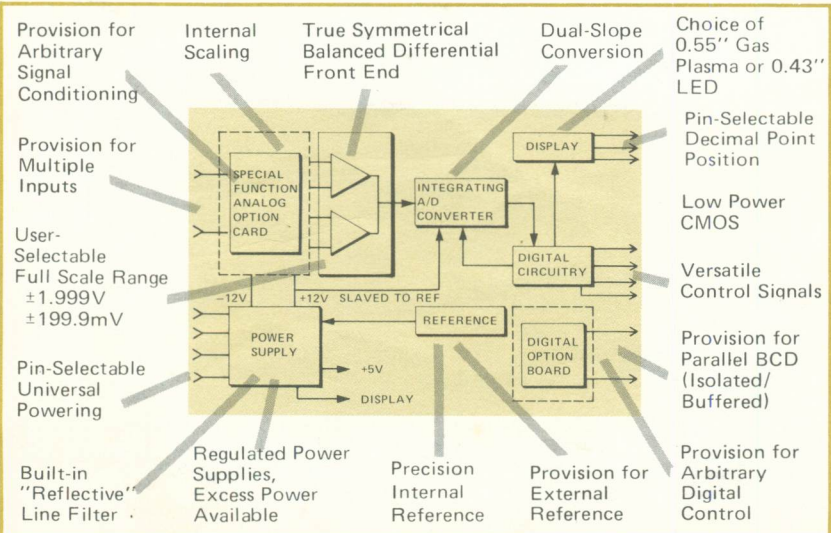


Figure 1. Simplified Block Diagram



## AN2533 & AN2553 SPECIFICATIONS

|  |   |                      |   |                                      |   |
|--|---|----------------------|---|--------------------------------------|---|
| <b>ANALOG INPUT</b>                          |   | <b>Configuration</b> | Bipolar balanced symmetrical differential inputs  | <b>AN2553 EXPANSION CAPABILITIES</b> | Any arbitrary input transducer signal conditioning, plus filtering, amplifying, impedance-matching, and analog linearizing, etc. Any arbitrary input signal scaling |
|  | <b>Full-Scale Range</b>                     |                      | ±1.999Vdc or ±199.9mVdc, user-selectable (special scaling available in OEM-quantity)  |                                      |   |
|  | <b>Bias Current</b>                         |                      | 10nA nominal, 30nA maximum  |                                      | As low as 10 <sup>-13</sup> amperes   |
|  | <b>Offset Current</b>                       |                      | 5nA nominal, 10nA maximum   |                                      | As low as 10 <sup>-13</sup> amperes   |
|  | <b>Dynamic Input Impedance</b>              |                      | 1000 megohms nominal  |                                      | As high as 10 <sup>12</sup> ohms  |
|  | <b>Normal Mode Rejection</b>                |                      | >30dB @ 60Hz with std. hi-freq. filter; up to 100dB with optional lo-freq. filter   |                                      | Up to 100dB   |
| <b>Common Mode Rejection</b>                 |   |                      |   |                                      |   |
|  | <b>Isolated Digital I/O: CMV Range:</b>     |                      | ±500Vdc or peak ac  |                                      |   |
|  | <b>CMRR:</b>                                |                      | >80dB intrinsic (See Application Data)  |                                      | Up to 160dB   |
|  | <b>Non-Isolated Digital I/O: CMV Range:</b> |                      | ±2.5Vdc or peak ac-input V  |                                      |   |
|  | <b>CMRR:</b>                                |                      | >80dB intrinsic   |                                      |   |
|  | <b>Zero-Offsetting</b>                      |                      | ±30 counts nominal at 1-volt full scale   |                                      | Any arbitrary value consistent with maximum input voltage specifications  |
|  | <b>Maximum Differential Input Voltage</b>   |                      | ±20V without damage   |                                      | Up to ±1000V without damage   |
| <b>ACCURACY/STABILITY</b>                    |   |                      |   |                                      |   |
|  | <b>Accuracy</b>                             |                      | ±0.05% of reading ±1 count  |                                      |   |
|  | <b>Resolution</b>                           |                      | ±1999 counts  |                                      |   |
|  | <b>Monotonicity</b>                         |                      | Guaranteed  |                                      |   |
|  | <b>Range Tempco</b>                         |                      | 35ppm of reading/°C typical, 70ppm of reading/°C maximum  |                                      |   |
|  | <b>Offset Tempco</b>                        |                      | 20μV/°C typical   |                                      |   |
|  | <b>Recommended Recalibration Interval</b>   |                      | 12 months   |                                      |   |
| <b>CONVERSION</b>                            |   |                      |   |                                      |   |
|  | <b>Technique</b>                            |                      | Dual-slope integration, each measurement independent of the previous measurement  |                                      |   |
|  | <b>Control</b>                              |                      | Displayed conversion controlled by internal (clock) or external (arbitrary system-developed control logic) command (low level applied to Pin 6 of Connector J1) |                                      | Built-in, arbitrary system-developed control logic (See Application Data, page 4)   |
|  | <b>Rate</b>                                 |                      | ~2 readings/second (internal) or any lower rate controlled by external command  |                                      | Any arbitrary rate less than 2 readings/second, controlled by built-in logic command (See Application Data, page 4)   |
|  | <b>Input Integration Period</b>             |                      | 100 milliseconds nominal  |                                      |   |
| <b>DISPLAY</b>                               |   |                      |   |                                      |   |
|  | <b>Type</b>                                 |                      | 7-segment gas plasma 0.55" (14mm) or LED 0.43" (11mm), planar   |                                      |   |
|  | <b>Number of Digits</b>                     |                      | 3 full-decade digits, and "1" in most significant digit position (See Ordering Guide, page 3 and Fig. 11, for dummy zero options.)                              |                                      |   |
|  | <b>Decimal Point</b>                        |                      | Externally programmable in three positions (See Application Data, page 4)   |                                      |   |
|  | <b>Polarity</b>                             |                      | Automatic, plus or minus sign displayed   |                                      |   |
|  | <b>Overload (More than 1999 Counts)</b>     |                      | All digits blanked; polarity and decimal point remain lighted   |                                      |   |
| <b>DIGITAL SIGNALS</b>                       |   |                      |   |                                      |   |
| (See Timing Diagram, Figure 3.)              |   |                      |   |                                      |   |
| <b>Logic Levels (All Inputs and Outputs)</b> |   |                      | DTL/TTL/CMOS compatible. Sinks 1.6mA at low level (0 to 0.5V) and sources 40μA at high level (+3.5 ±1V)   |                                      |   |
|  | <b>External Blanking</b>                    |                      | Low level input (on Pin 7) blanks three least significant digits  |                                      |   |
|  | <b>Hold</b>                                 |                      | Low level input (on Pin 6) retains last reading in display (See Figure 7.)  |                                      |   |
|  | <b>Overload</b>                             |                      | Low level output (on Pin 7) indicates a measurement greater than 1999 counts  |                                      |   |
|  | <b>Clock</b>                                |                      | Continuous (100kHz nominal)   |                                      |   |
|  | <b>Latch</b>                                |                      | High level output (on Pin J) indicates that counter contents are being transferred into latches   |                                      |   |
|  | <b>Carry</b>                                |                      | Rising edge (on Pin F) indicates counter carry (See Application Data)   |                                      |   |
|  | <b>EOC</b>                                  |                      | Rising edge (on Pin K) signals end of conversion (EOC)  |                                      |   |
|  | <b>Polarity</b>                             |                      | High logic level (on Pin 8) indicates measurement is negative   |                                      |   |
| <b>BCD OPTION CARDS</b>                      |   |                      | Isolated and/or buffered parallel BCD outputs (See Application Data).   |                                      |   |
| <b>MTBF</b>                                  |   |                      | 43,000 hours calculated   |                                      |   |
| <b>POWER</b>                                 |   |                      |   |                                      |   |
|  | <b>Input Voltage</b>                        |                      | 100, 117, 220, or 240Vac rms<br>±10%, 49 to 500Hz   |                                      |   |
|  | <b>Available Output Voltage</b>             |                      | +4.75Vdc ±5% at 30mA<br>+12Vdc ±8% at 10mA; -12Vdc ±8% at 10mA  |                                      |   |
|  | <b>Consumption</b>                          |                      | 2 watts nominal*  |                                      |   |
| <b>ENVIRONMENTAL &amp; PHYSICAL</b>          |   |                      |   |                                      |   |
|  | <b>Operating Temperature</b>                |                      | -10°C to +60°C (+14°F to +140°F)  |                                      |   |
|  | <b>Storage Temperature</b>                  |                      | -25°C to +85°C (-13°F to +185°F)  |                                      |   |
|  | <b>Relative Humidity</b>                    |                      | 0 to 95%, noncondensing   |                                      |   |
|  | <b>Weight</b>                               |                      | 12 ounces nominal (340 grams)   |                                      |   |
|  | <b>Case</b>                                 |                      | High-impact molded plastic case UL 94V-0 Rated standard; metal case available as an option  |                                      |   |
|  | <b>Dimensions</b>                           |                      | DIN-Standard: 96mm (3.78 inches) bezel width x 48mm (1.89 inches) bezel height x 104.9mm (4.13 inches) max. depth (see Figure 8)                                |                                      |   |

\*Slightly higher with LED displays

**NET SIGNAL ENHANCEMENT & INTERFERENCE REJECTION**

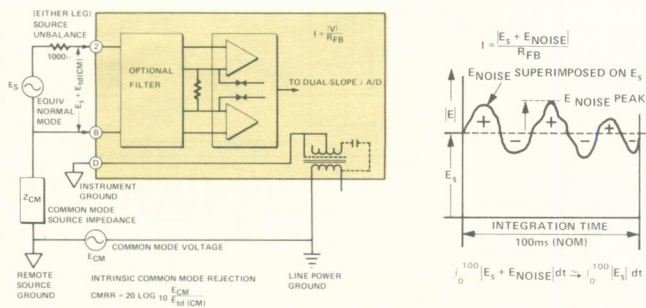
The AN2533/AN2553 exceptional overall signal interference rejection is a combination of:

- (1) The intrinsic front end (input terminal related) CMR
- (2) The normal mode input filter rejection, and
- (3) The long-time integration in the dual slope A/D converter.

As a result, the user has a remarkable flexibility in obtaining accurate normal mode (series) noise rejection.

**TRUE, BALANCED, DIFFERENTIAL INPUT & CMR**

The very high impedance, true balanced symmetrical differential front end (not to be confused with some pseudo-differential types) provides the user with the versatility for making direct additive or subtractive measurements of local or remote noisy inputs from one or more sources, referenced to arbitrary system power or instrument ground. The digitized output represents the true difference of input potentials, and, therefore, it is insensitive (see specifications) to voltage variations and fluctuations common to both terminals. Thus, the input differential circuitry itself can contribute to the rejection of common mode potentials referred to instrument ground. In addition, because of the high degree of isolation of the power transformer, excellent rejection ratios are achieved for common mode voltages up to ±350V with respect to power line ground.



**Figure 4. Transformation of Common Mode Signals,  $E_{CM}$ , to Normal Mode Signals,  $E_{Td(CM)}$ , NMR, and Rejection by Integration**

**NORMAL MODE REJECTION**

Normal mode interference signals, resulting either from conversion of common mode voltage to differential voltage or from additive (series) interferences, may be filtered out by a combination of passive or active input filtering and conversion integration. The standard DPI is supplied with a nominal 20Hz low pass single-pole filter which, in combination with the integration effect, yields approximately 30dB rejection at 50/60Hz. There is ample provision within the AN2533/53 to incorporate either lower frequency and multipole passive filters and/or active filters which utilize the input differential amplifiers as their active elements (see Example A, page 5), so as to obtain normal mode rejections up to 100dB or greater at 50/60Hz.

**INTERFERENCE REJECTION BY INTEGRATION**

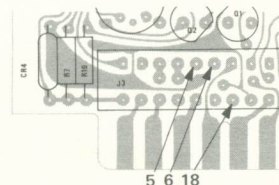
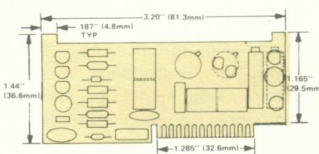
Remaining interference components (after front-end terminal related and input filter rejection) are still further reduced by the 100ms integration. For net signal level-to-peak noise ratios higher than one, the bipolar integration is complete so that, even for non-synchronous 50 or 60Hz interference, rejection greater than 20dB will be achieved.

Overall common mode rejection ratios of greater than 100dB (for example, 80dB intrinsic CMRR, +60dB NMRR, +20dB integration rejection) at 50 or 60Hz with 1000 ohm unbalance in either input line can readily be obtained!

**ANALOG FUNCTION CARD**

Using either the Analogic AN450 General Purpose Analog Function Card with Filter (see Fig. 11), which is typically capable of handling 30 arbitrary components, including potentiometers, dual in-line ICs, and discrete 2-and 3-lead components, or by designing his own such card, the user may build in proprietary circuitry for any arbitrary signal conditioning, excitation, or linearizing function, utilizing the available excess regulated power, stable reference, and additional input terminals for optimum system compatibility.

The General Purpose Analog Function (kluge) Card, with a pre-engineered layout for optimum component space utilization, is held securely in the DPI by connector J3 and the case without the need for any additional mounting hardware.



**Figure 5. Typical Kluge Card Layout**

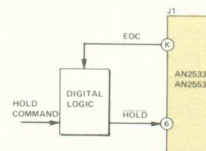
**Figure 6. PC-Board Scaling Connections**

**ARBITRARY SCALING**

With a 10,000Ω feedback resistor ( $R_{FB}$ ) connected as shown in Figure 2, the DPI is normally calibrated at the factory for a full-scale range of 1 volt/1,000 counts. A thermally tracking internal resistor, 1.1 kilohms, may be connected in parallel with the 10,000 ohm resistor by a jumper between positions 5 and 6 on the main assembly PC board (AN2533) or by connections on the analog option board (AN2553). The parallel resistance of 1,000 ohms provides the user-selectable sensitivity of 100mV/1,000 counts (100μV/count). Any other sensitivity may be obtained by a net resistance between positions 6 and 18 according to the formula  $R = \frac{\text{Voltage}/1,000 \text{ Counts}}{0.1 \text{ mA}}$ .

**HOLD**

To hold a displayed reading, gate a HOLD command (the comparator output shown in Figure 2) with the rising edge of EOC (available at pin K), and then generate a DTL low level signal (HOLD). When applied to Pin 6 of the DPI connector, the HOLD signal will keep the last conversion displayed, while the DPI continues to update the measurement internally. When HOLD is removed, the next valid measurement is transferred to the display latches.



**Figure 7. Generating a Hold Command**

**ANALOG LIBRARY OF SPECIAL FUNCTION CARDS**

**DIGITAL CIRCUIT OPTIONS**

- AN404 Function PC Card DIN Standard
- AN406 Latched, Buffered Parallel BCD Output Card
- AN408 Isolated, Buffered Parallel BCD Output Card

**ANALOG CIRCUIT OPTIONS**

- AN450 Analog Function PC Card with Input Filter
- AN451 Analog Function PC Card without Input Filter
- AN452 Thermocouple Cold-Junction Compensation Card

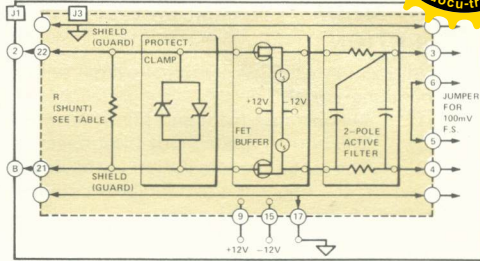
- AN453 RTD Temperature Card
- AN454 Input Filter Card
- AN455 Industrial Current Receiver Card
- AN456 Industrial Voltage Receiver Card
- AN461 True RMS AC Voltmeter Card
- AN462 Power Line Voltage Monitor Card
- AN463 Microvolt Receiver Card
- AN466 Linearized Thermocouple Card



### Assemble A Precision Current Meter

To measure current from amperes to picoamperes, simply select the standard 100mV/1,000 count DPI sensitivity and install the appropriate shunt resistance. Depending on the signal amplitudes and interferences, design protective clamps, low leakage FET buffers, and multipole filters. Appropriately guard for higher sensitivity operation by eliminating leakage current paths. Digitize the output in any arbitrary engineering units by modifying the shunt resistance between Pins 6 and 18 of J3. By connecting either end of the shunt to analog ground, or by other means, assure circuit conformance to common mode limits.

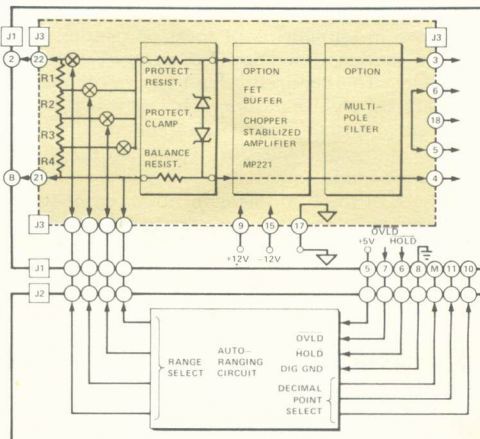
| F.S. RANGE | UNIT COUNT | SHUNT, R |
|------------|------------|----------|
| 2,000 Amp  | 1mA        | 0.100Ω   |
| 200.0mA    | 100μA      | 1.000Ω   |
| 20.00mA    | 10μA       | 10.00Ω   |
| 2.000mA    | 1μA        | 100.0Ω   |
| 200.0μA    | 100nA      | 1.000KΩ  |
| 20.00μA    | 10nA       | 10.00KΩ  |
| 2.000μA    | 1nA        | 100.0KΩ  |
| 200.0nA    | 100pA      | 1.000MΩ  |
| 20.00nA    | 10pA       | 10.00MΩ  |
| 2.000nA    | 1pA        | 100.0MΩ  |



### Build An Extended Range Voltmeter

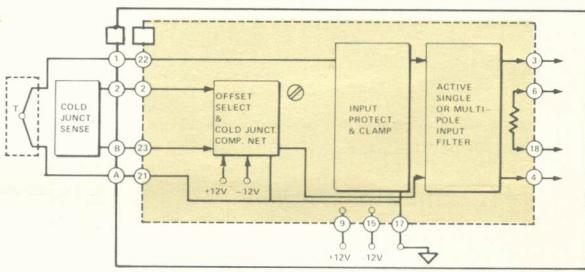
To measure any voltage from kilovolts to microvolts, use either of the selectable standard DPI sensitivities and the appropriate voltage divider network. Depending upon whether a single-range or multiple-range voltmeter is desired, design suitable switching circuits to be activated either by externally programmed range select signals, or optionally, by range control signals developed on the digital function card. Protect the input circuitry with resistive and clamping components, and introduce an optional FET buffer, chopper stabilized amplifier, or standard amplifier module such as the Analogic MP221 if needed in very low level signal applications. Incorporate an optimal filter to obtain the necessary signal enhancement. Measured voltages may be scaled in arbitrary engineering units by suitable modifications to the input divider network alone, or coupled with appropriate scaling resistors,  $R_{FB}$ .

|    | SINGLE-RANGE |      |      | MULTIPLE-RANGE |      |
|----|--------------|------|------|----------------|------|
|    | 1000V        | 100V | 10V  | EITHER         |      |
| R1 | 999K         | 990K | 900K | 9M             | 900K |
| R2 | 1K           | 10K  | 100K | 900K           | 90K  |
| R3 | 0            | 0    | 0    | 90K            | 9K   |
| R4 | 0            | 0    | 0    | 10K            | 1K   |



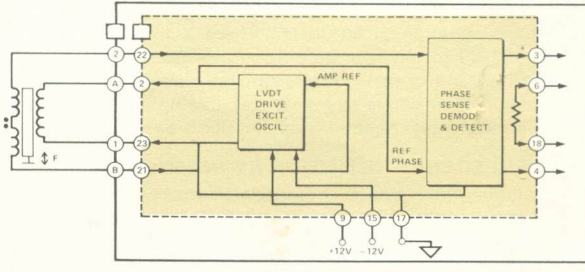
### Construct A Thermocouple Temperature Indicator

Cold-junction-compensated temperature indicators, utilizing any type of thermocouple, with excellent common mode (greater than 160dB!) and normal mode (greater than 100dB!) rejection can easily be constructed with just a few components. A semiconductor or resistive cold junction sensing element, stably powered by the DPI +12V power reference, can generate an offset and cold-junction-compensation variable voltage which can be directly subtracted (or added) from the thermocouple-developed voltage via the true differential balanced input circuitry. Input resistor and zener clamps may provide protection, and filter components as shown in "A" above may form an active two-pole filter. The appropriate resistor across Pins 6 and 18 of J3 scales the output directly in temperature-related engineering units.



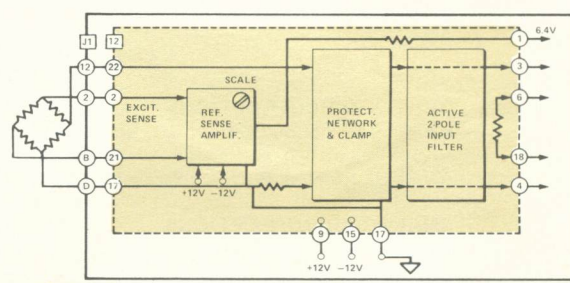
### Develop An LVDT Position Or Force Indicator

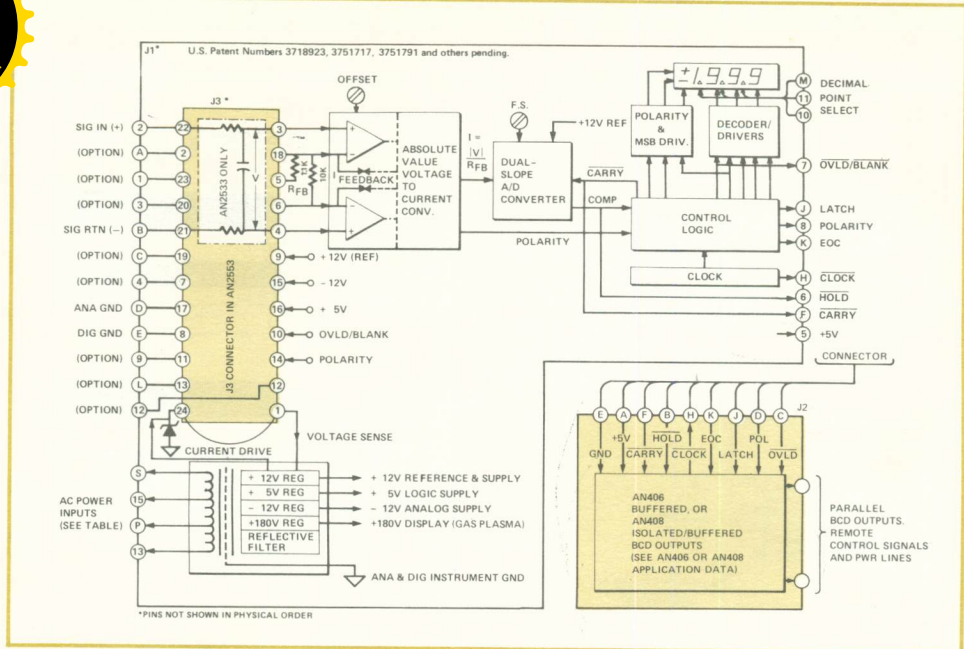
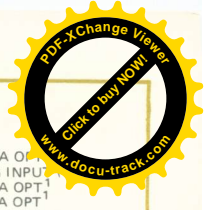
The excitation winding of an LVDT may be driven over a wide range of frequencies by an excitation oscillator powered by the ±12V regulated supplies and amplitude regulated by the precision +12V supply. The combined differential winding output of the LVDT can then be phase-sensitive demodulated in a simple switching circuit whose phase reference is derived from the excitation oscillator. The filter output of the phase sensitive demodulator can then be applied directly to the differential inputs of the DPI. Again, the output may be scaled in any desired force or linear units by choosing the appropriate resistor across Pins 6 and 18 of J3.



### Engineer A Ratiometric Load Cell Meter

The ratiometric capability of the AN2533/2553 may be exploited to perform ratiometric measurements of bridge transducer outputs with an accuracy independent of the external excitation supply variations. Available input pins may be utilized to sense the voltage across the bridge via a reference sense amplifier whose output may be applied via Analog Function Card Connector J1, Pin 1, to control the DPI reference. The differential output of the bridge may be scaled, offset, or amplified, or may be applied directly to the differential inputs. As described above, the scaling resistor between Pins 6 and 18 of J3 converts the output to arbitrary engineering units.





Pin Designations

J1 (bottom)

|                          |   |    |                      |
|--------------------------|---|----|----------------------|
| ANA OPT <sup>1</sup>     | A | 1  | ANA OPT <sup>1</sup> |
| SIG RTN (-) <sup>2</sup> | B | 2  | SIG INPUT            |
| ANA OPT <sup>1</sup>     | C | 3  | ANA OPT <sup>1</sup> |
| ANA GND                  | D | 4  | ANA OPT <sup>1</sup> |
| DIG GND                  | E | 5  | +5V OUT              |
| CARRY                    | F | 6  | HOLD                 |
| CLOCK                    | H | 7  | BLANK IN/OVLD OUT    |
| LATCH                    | J | 8  | POLARITY             |
| EOC                      | K | 9  | DIG OPT <sup>1</sup> |
| DIG OPT <sup>1</sup>     | L | 10 | DEC PT 1             |
| DEC PT 3                 | M | 11 | DEC PT 2             |
| DIG OPT <sup>1</sup>     | N | 12 | DIG OPT <sup>1</sup> |
| AC LINE <sup>3</sup>     | P | 13 | AC LINE <sup>3</sup> |
| DIG OPT <sup>1</sup>     | R | 14 | DIG OPT <sup>1</sup> |
| AC LINE <sup>3</sup>     | S | 15 | AC LINE <sup>3</sup> |

<sup>1</sup> In AN2553, available for user selection with Special-Function card.  
<sup>2</sup> AN2533 connection as shown. In AN2553, available for user selection with Special-Function card.  
<sup>3</sup> See Table below for powering selection.

| LINE VOLTAGE* | P | 13 | S | 15 |
|---------------|---|----|---|----|
| 100V          | ● |    |   | ●  |
| 117V (120)    | ● |    | ● |    |
| 220V          |   | ●  |   | ●  |
| 237V (240)    |   | ●  | ● |    |

\*49 to 500Hz.

Figure 2. Functional Block Diagram

Operating Features & Principles of Operation

As shown in Figure 2, the AN2533 contains a balanced signal enhancement input filter; a floating true differential front end; an absolute-voltage-to-current converter; a dual-slope ratiometric, current-to-count integrating analog-to-digital converter; clock-driven logic control circuitry, decoders, drivers and displays; and regulated power supplies derived from the secondary windings of a universal transformer.

Signal input to connector J1 is conditioned by the built-in filter (AN2533) or by arbitrary signal conditioning on the analog option card inserted in internal connector J3 (AN2553), resulting in a potential difference (V) at J3, pins 3 and 4, connected to the non-inverting inputs of the differential input amplifiers. The conditioned signal input (V) develops a unidirectional signal current (I), whose magnitude depends on the value of the selected feedback resistance (R<sub>FB</sub>), according to the simple Ohm's Law formula shown in Figure 2. The signal current linearly charges a high quality, low leakage, integrating capacitor during the signal integration phase of the dual slope conversion. The current generation circuitry also includes the polarity sensing for display.

Under control of the 100kHz clock-driven logic, the signal integration phase lasts 10,000 counts, thus adding to the overall signal enhancement by providing very high rejection of normal mode interfering noise. At the end of the 10,000 counts, the CARRY control signal causes the integrator to switch into the reference integration phase, during which the integrating capacitor is discharged at a constant rate determined by a current derived from the precision +12V reference until the comparator changes state. The precision resistor network determining the integrating reference current is mounted on the same substrate as the built-in selectable feedback resistance (R<sub>FB</sub>). Thus maximum thermal tracking of ratio-determining dual-slope performance components is obtained. This contributes to the exceptional overall thermal stability of the conversion. Moreover, because the signal integration phase is at least 5 times as long as the reference integration phase (10,000 counts to a maximum of 2,000 counts), noise disturbances are reduced significantly in the output.

The count accumulated during the reference integration phase is latched into the storage register, decoded, and, in addition to the polarity sensed in the current generator, used to update the display about twice a second for optimal flicker-free readings. When the count exceeds 1999, the Control Logic generates an overload (OVLD) signal which blanks the decimal digits while leaving the polarity sign and the selected decimal point lighted.

In addition to decimal point programming, the user may blank the least three significant digits or may choose to hold a displayed conversion by applying DTL-compatible signals at the designated terminals of J1. It is of interest to note that the instrument continues to update its digitized measurement, making available a valid display after the HOLD signal is released.

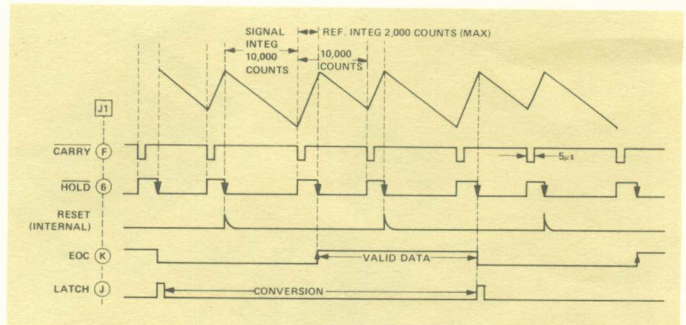


Figure 3. Timing Diagram

DTL/TTL-compatible digital output signals of LATCH, CARRY, EOC, HOLD, and CLOCK, as well as the OVLD and POLARITY signals, are available at connector J1, and are related to the charge-discharge cycle of the integrating capacitor as shown in the timing diagram of Figure 3.

Analog Function Card

Connector J3, when utilized, brings to the analog function card a number of input signal connections, as shown, and all power sources and their ground return references for use in such signal conditioning circuits as described in the Application Data.

Digital Function Card

There is an excess of +5V to power the snap-in digital option card on which isolated and/or buffered BCD outputs are generated. Connections are made via the standard panel instrument connectors. (See Application Data, page 6.)

ORDERING GUIDE

Simply Specify

|   |        |   |   |      |
|---|--------|---|---|------|
| Universal Digital Panel Instrument                                | AN2533 |   |   |      |
| Expanded Digital Panel Instrument                                 | AN2553 |   |   |      |
| Gas Plasma Display  |        | S |   |      |
| LED Display   |        | L |   |      |
| UL 94V-0 Rated Plastic DIN/NEMA Case (Order PL10-5563 Connector)* |        |   | P |      |
| Extruded Aluminum DIN/NEMA Case (Order PL10-5563 Connector)*      |        |   | M |      |
| One Dummy Zero (LED Only)   |        |   |   | 1DZL |
| Two Dummy Zeros (LED Only)  |        |   |   | 2DZL |

\*Optional Screw-Terminal Connector (Analogic PL10-5535) available for solderless wiring for plastic or metal case (See Figure 9)

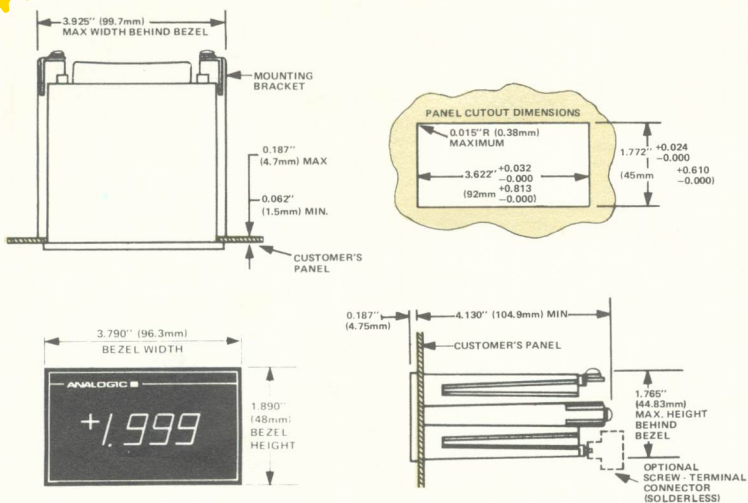


Figure 8. Panel Mounting and Outline Dimensions

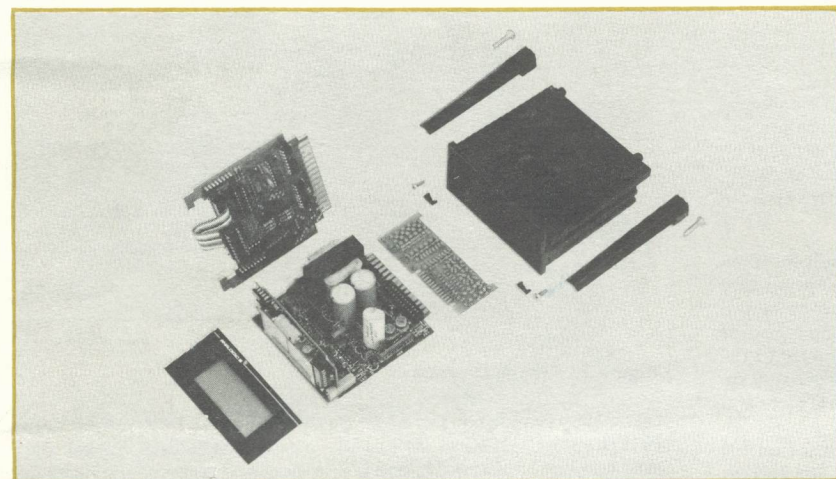
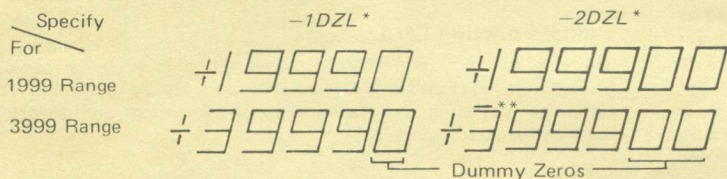


Figure 10. Complete DPI and Additional Function Cards

For LED displays only, either one (1DZL) or two (2DZL) "dummy" zeros may be added to the right end of the digital readout. These zero digits are "fixed"; that is, they always display "0" (1DZL) or "00" (2DZL) for all input signals within the specified range.



\* Add to end of Order Code. Factory installation only.  
 \*\* For positive inputs, negative sign does not light. For overload inputs, decimal point and middle horizontal segments of dummy zeros are lit; negative sign lights for negative overload only.

Figure 11. "Dummy" Zero Display

Rear View –  
 Bezel Not Shown for Clarity

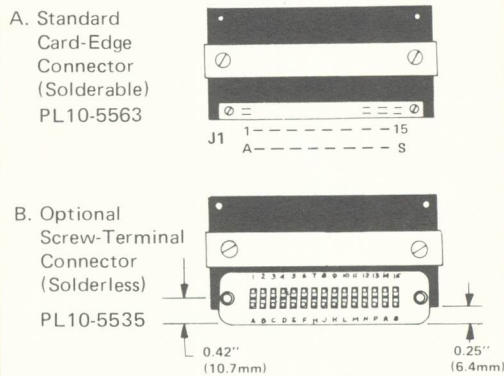
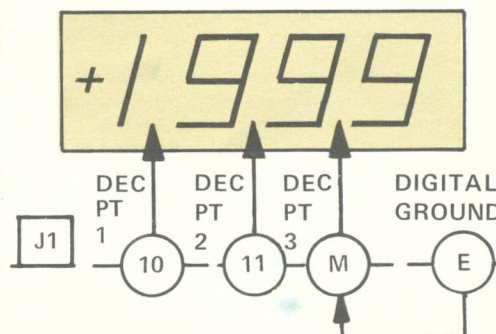


Figure 9. Rear Panel Connectors (metal case option shown)

DECIMAL POINT SELECTION



To display the desired decimal point, simply connect the appropriate pin as shown to Digital Ground (Pin E, J1) using a jumper lead.

Figure 12. Decimal Point Position Terminals

NEED APPLICATIONS HELP?

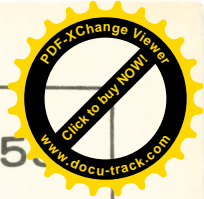
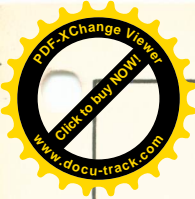
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AVAILABLE FROM:

**KONING EN HARTMAN**  
 elektrotechniek bv  
 postbus 43220  
 2504 AE den haag  
 telefoon 070-210101 telex 31528



# APPLICATION DATA

## AN2553 Setup Instructions

**KONING EN HARTMAN**  
 elektrotechniek bv  
 postbus 43220  
 2504 AE den haag  
 telefoon 070-210101 telex 31528



### GENERAL

1. To operate your AN2553 Digital Panel Instrument, a "KLUGE" card must be inserted in the internal J3 socket on the main PC-board assembly and connections made on that card to the input differential amplifiers. (See the AN2533/AN2553 Data Sheet.)
2. The KLUGE card may be either:
  - a) A custom-designed card manufactured by Analogic; or
  - b) Analogic card AN450, containing a standard input filter; or
  - c) Analogic General Purpose Card AN451, or
  - d) A card designed and produced by the user to interface with the AN2553, mating with connector J3 on the main PC-assembly of AN2553.

### INSTRUCTIONS

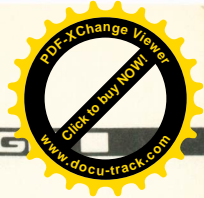
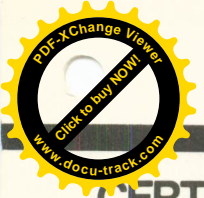
- A. If the KLUGE card incorporates an input-connecting circuit such as in category a), b), or d) above, then:
  - (1) Plug the card into connector J3.
  - (2) Attach signal inputs to the appropriate external J1 terminals as determined by the card-mounted circuitry.

- (3) Attach the source power to the appropriate power input terminals as shown in the table of Powering Connections on the Data Sheet.
- B. If the KLUGE card is a general-purpose Analogic AN451, then:
  - (1) Identify the instrument connector (J1) terminals to which the signal inputs, SIG IN (+) and SIG RTN (-), are to be connected.
  - (2) Refer to the J1-J3 interconnection table below, and determine the J3 terminals at which the signal inputs will be present after they have been connected as required by step (1) above.
  - (3) Install any desired signal-conditioning circuitry between the P3 edge-connector terminals on the general purpose card.
  - (4) Plug the card into mating J3 connector.
  - (5) Attach signal inputs to the selected J1 terminals; attach power to appropriate J1 terminals according to the instructions shown in the AN2533/AN2553 Data Sheet.
- C. The AN2553 is now ready for operation. See Data Sheet for Scaling Instructions.

J1 - J3 CONNECTIONS FOR AN2553

| INTERNAL AN2553 CIRCUIT | EXTERNAL OR J1 CONNECTION | J3    | EXTERNAL J1 CONNECTION | INTERNAL OR AN2553 CIRCUIT |
|-------------------------|---------------------------|-------|------------------------|----------------------------|
| REF SENSE               | _____                     | 1 24  | _____                  | REF DRIVE                  |
| _____                   | J1 - A                    | 2 23  | J1 - 1                 | _____                      |
| *SIG IN (+)             | _____                     | 3 22  | J1 - 2                 | _____                      |
| *SIG RTN (-)            | _____                     | 4 21  | J1 - B                 | _____                      |
| FEEDBACK                | _____                     | 5 20  | J1 - 3                 | _____                      |
| FEEDBACK                | _____                     | 6 19  | J1 - C                 | _____                      |
| _____                   | J1 - 4                    | 7 18  | _____                  | FEEDBACK                   |
| DIG GND                 | J1 - E                    | 8 17  | J1 - D                 | _____                      |
| +12V REF                | _____                     | 9 16  | J1 - 5                 | +5V                        |
| OVLD/BLNK               | _____                     | 10 15 | _____                  | -12V                       |
| _____                   | J1 - 9                    | 11 14 | J1 - 8                 | POLARITY                   |
| _____                   | J1 - 12                   | 12 13 | J1 - L                 | _____                      |

\*Inputs to Differential Amplifiers after signal conditioning.



# CERTIFICATE OF CALIBRATION

For Digital Panel Instrument AN2530/53 -S-P \_\_\_\_\_ Serial No. 1222540

ANALOGIC CERTIFIES that this Digital Panel Instrument has been duly inspected and tested prior to shipment, and that it meets or exceeds all of the requirements specified in its published mechanical, electrical and operational performance characteristics. All tests were performed using methods that preserve NBS traceability for the instrument.

NOTE: The following tests were performed after

- a) 96 hours minimum burn-in at a nominal 50°C and at nominal line voltage unless otherwise specified.
- b) Vibration at 5G's for 30 seconds at 60Hz in a horizontal plane.

## I. CALIBRATION

Zero Span + \_\_\_\_\_ • 7 mV for +001 Reading  
 - \_\_\_\_\_ • 7 mV for -001 Reading

| Positive Inputs (mV) | Reading |                                     |
|----------------------|---------|-------------------------------------|
| 000                  | 000     | <input checked="" type="checkbox"/> |
| + 400                | + 399   | <input type="checkbox"/>            |
|                      | + 400   | <input checked="" type="checkbox"/> |
|                      | + 401   | <input type="checkbox"/>            |
| + 800                | + 799   | <input type="checkbox"/>            |
|                      | + 800   | <input checked="" type="checkbox"/> |
|                      | + 801   | <input type="checkbox"/>            |
| + 1800               | + 1798  | <input type="checkbox"/>            |
|                      | + 1799  | <input type="checkbox"/>            |
|                      | + 1800  | <input checked="" type="checkbox"/> |
|                      | + 1801  | <input type="checkbox"/>            |
|                      | + 1802  | <input type="checkbox"/>            |

| Negative Inputs (mV) | Reading |                                     |
|----------------------|---------|-------------------------------------|
| 000                  | 000     | <input checked="" type="checkbox"/> |
| - 400                | - 399   | <input type="checkbox"/>            |
|                      | - 400   | <input checked="" type="checkbox"/> |
|                      | - 401   | <input type="checkbox"/>            |
| - 800                | - 799   | <input type="checkbox"/>            |
|                      | - 800   | <input checked="" type="checkbox"/> |
|                      | - 801   | <input type="checkbox"/>            |
| - 1800               | - 1798  | <input type="checkbox"/>            |
|                      | - 1799  | <input type="checkbox"/>            |
|                      | - 1800  | <input checked="" type="checkbox"/> |
|                      | - 1801  | <input type="checkbox"/>            |
|                      | - 1802  | <input type="checkbox"/>            |

## II. DISPLAY TEST

All numerals are decoded and displayed

## III. OVERRANGE

Three LED's blank with both ± 2.010 volts applied

## IV. SUPPLY VOLTAGE COMPLIANCE

| Supply Voltage | Input  | Difference in Reading (a - b) |                                     |
|----------------|--------|-------------------------------|-------------------------------------|
| 105 Vac        | 1.000V | + 1                           | <input checked="" type="checkbox"/> |
| 130 Vac        | 1.000V | 0                             | <input checked="" type="checkbox"/> |
|                |        | - 1                           | <input type="checkbox"/>            |

## V. COMMON MODE

Conditions: Apply ± 1800mV to input  
 Apply ± 700mV between Analog Ground and Signal Return

Change in Reading \_\_\_\_\_ 000   
 \_\_\_\_\_ 001

## VI. MISCELLANEOUS

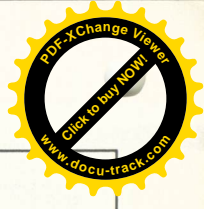
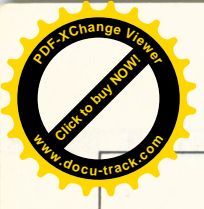
- a) All three Decimal Points externally programmable
- b) External Display Blanking

FORM 16-500004 REV. 2

Tested By: GP Date 5-25-82

Accepted By: \_\_\_\_\_ Date \_\_\_\_\_  
 QA 11 Q.A. Inspector  
 MAY 27 1982





**The minimum connections required for use as a conventional measurement instrument are:**

**1. Signal Input**

Single Ended: Connect (+) side of signal input to J1-2; connect (-) side of signal input to J1-B and J1-D.

Differential Input:\* Connect (+) side of signal input to J1-2; connect (-) side of signal input to J1-B; connect analog ground to Pin J1-D.

**2. AC Input**

For 100Vac: connect ac line between J1-P and J1-15

For 117Vac: connect ac line between J1-P and J1-S

For 220Vac: connect ac line between J1-13 and J1-15

For 240Vac: connect ac line between J1-13 and J1-S.

**3. Decimal Point**

DP1 — connect J1-E to J1-10 to light the decimal between the MSD and hundreds digit [1.888]

DP2 — connect J1-E to J1-11 to light the decimal between the hundreds and tens digit [18.88]

DP3 — connect J1-E to J1-M to light the decimal between the tens and ones digit [188.8]

**4. For the AN2553, a kluge card must be installed in J3, (on motherboard). See product data sheet.**

See Product Data Sheet for maximum common mode voltages.

J1 A0  
300 0 1000