5.3.2 CIRCUIT VOLTAGES

The following voltages may be used as a general guide during faultfinding. All voltages are measured with respect to ground (chassis) with a high input impedence instrument with the supply line voltage at the nominal value set on the SUPPLY VOLTAGE switch. The readings are taken with the front panel controls set as follows unless otherwise indicated:-

INTENSITY, X SHIFT and both Y SHIFT CONTROLS at mid position.
CH1 and CH2 input coupling switches in GND position.
DISPLAY MODE in NORMAL position.
Y MODE in CH1 position.
TIME/CM. at 1ms/cm.
X EXPAND in X1 position (fully anti-clockwise).
TRIGGER LEVEL mid position.
BRIGHT LINE OFF.
TRIGGER SOURCE in EXT. position.

Y Pre-Amplifier

D301 Anode	– 7.2V
D302 Cathode	+ 7.2V
TR301 Drain	+ 10V
TR301 Source	+ 1.5V
TR303 Collector	0V
TR303 Base	– 9.2V
TR302 Drain	– 9.8V
TR302 Source	– 18.5V
TR305 emitter	– 0.7V
TR306 emitter	– 0.7V
TR307, TR308 collectors	+ 5.8V
TR309 collector	0V
TR310 collector	+ 4.2V

Y Output Amplifier

TR408, TR409 bases	+ 0.7V
TR408 collector	+ 5.1V
TR409 collector	+ 4.5V
TR406, TR407 bases	+ 16V
TR406, TR407 collectors	+ 17.5V
TR404, TR405 bases	+ 19.8V
TR404, TR405 collectors (Y plate mean potential)	+ 109V

Beamswitch and Signal Switch

TR319 collector	+ 1.9V CH1 selected + 0.1V CH2 selected
TR321 base	0V
D317, D318 Anodes	+ 1.4V (– 0.6V in REFRESHED mode)
D319, D320 Anode	–0.6V (+ 1.4V in REFRESHED mode)
D323 Anode	– 6.4V

ADC: Scaling Amplifier

TR201 base	0V
TR202 collector	+ 6.5V
TR203 collector	+ 2.8V
TR204 base	0V
D204 Anode	– 6.5V
TR206 base	+ 2V
TR206 collector	+ 5.1V

ADC: Sample and Hold

D208 Anode	– 12.2V
TR213 Gate	+ 1.4V
TR213 Source	+ 2.9V
TR214 Drain	+ 1.4V
TR214 Source	– 4.5V

ADC: Summing Amplifier

IC102 pin 2	+ 2V
IC102 pin 1	+ 10.6V
IC102 pin 12	– 1.7V

ADC: Current Sources

IC101 pin 3		+ 3.7V
IC101 pin 4		+ 7V
IC101 pin 1		+ 5.3V
TR134 base		+ 3.9V (D1 high)
	or	+ 0.1V (D1 low)
TR134 collector		+ 4.7V (D1 high)
	or	+ 6.1V (D1 low)
TR135 collector		+ 6.0V (D1 high)
	or	+ 5.4V (D1 low)
TR232 emitter		+ 10.7V

Timebase

TR914 base	0V
TR915, TR916 collectors	+ 5.5V
TR901, TR902 collectors	+ 14V
TR903 collector	+ 18V
TR904 base	+ 13.7V
TR904 collector	+ 15.6V
TR905 collector	– 19.4V (– 20.6 when triggered)
TR909 base	– 1.8V (+ 0.8 when triggered)
TR912 base	+ 0.8V (– 3.4V when triggered)
TR912 collector	+ 0.2V (+18V when triggered)
TR913 collector	+ 13.2V (+ 0.2V when triggered)
TR924 base	+ 0.6V (plus 11.4V positive going ramp during sweep)
TR924 collector	– 4.4V (plus 6V negative going ramp during sweep)
Junction R998/R983	– 12.2V
TR927 emitter	+ 6.4V
TR925, TR926 collectors (X plate mean potential)	+ 85V

Logic Levels

Inputs: Logic '0' (max.)	+ 0.8V
Logic '1' (min.)	+ 2V
Outputs: Logic '0' (max.)	+ 0.4V
Logic '1' (min.)	+ 2.4V
Typical Levels: Logic '0'	+ 0.2V
Logic '1'	+ 4V

5.3.3 DATA FAULTS

When tracing faults which cause gross distortions (steps, discontinuities, etc.) of the display in the REFRESHED and ROLL modes, it is helpful to distinguish between three cases:

1. Addressing errors. These will occur at particular positions across the screen in the X direction regardless of the setting of the vertical shift controls.
2. Data errors. These will occur at specific positions up the screen in the Y direction regardless of the Y shift control.
3. Timing errors. These will usually be spikes or notches occurring in a fairly random fashion, but often affected by the timebase range switch and the store controls, interaction between the traces may also occur.
   Address lines may be verified by checking for a true binary sequence, that is, by ensuring each bit is changing at twice the frequency of the next most significant bit. This may be done at the address inputs of the stores by switching to the ROLL mode with the timebase range switch at 50μs/cm. In this condition the stores are continuously addressed by the write address counter only. Pressing the LOCK FULL STORE push-button selects the read address counter only.

The eight data lines may be checked from the output of the analogue to digital convertor at SK.F, through the 'data in' latches, IC618 and IC619, the eight store packages, 'data out' latches IC650 and IC659, to the digital inputs of the digital to analogue convertor, IC745. Note that the sense of the data is inverted after the input latches. If a triangle or sawtooth (as obtained from an oscilloscope ramp output for example) waveform is used as an input signal, the data will approximate to a binary sequence as with the address counters, and may be easily verified. With the instrument in the ROLL and the timebase set fo 100μs/cm., the read and write address counters will be running at the same rate, so that the data output rate from the store will be the same as the data input rate, thus simplifying checking. Note that even in this condition, however, the output data cannot be compared directly with the input data since the relative timing between the two (due to the time that the data is held in the store before being read out) will be arbitrary.

Timing errors must be found by checking the various clockpulses and control signals around the store and A.D.C. against the timing diagrams given in this section and also the circuit description section. When inspecting fast pulses, a fast rise-time oscilloscope must be used (say better than 10ns) together with an appropriate low capacitance probe and earth lead. The logic devices used are from the well known 'T.T.L.' (Transistor-Transistor Logic) family and typical propagation delays for each type of device may be obtained from manufacturer data sheets.

5.3.4 CHECKING DATA PATH

1. Apply a sine wave or triangle input signal of 8 cms. amplitude.
2. Set trigger controls to give a stable display.
3. Switch DISPLAY MODE to REFRESHED

Are all data outputs from A.D.C. at SKF pins 6, 7, 11 - 16 changing?

NO →
1. Check clock signals at SKF pins 1, 2, 5, 10.
2. Check input signal to comparators at emitters of TR215, TR221 and TR223.
3. Check input scaling amplifier.
4. Check decoding logic.

YES

Is data changing at input to each store (pin 11)?

NO → Check clock pulse to data in latches at IC603 pin 6.

YES

Is data changing at D.A.C. inputs IC745 pins 5 - 12?

NO →
1. Check for correct operation of R/$\overline{W}$ control at each store (pin 3)
2. Check clock pulse to data out latch at IC625 pin3.

YES

Is display changing?

NO →
1. Check sample-and-hold pulse in dot joiner circuit.
2. Check dot joiner circuit
3. Check D.A.C.IC

YES

Do steps or discontinuities in display remain in fixed x position as display is shifted vertically?

YES →
1. This indicates a fault in either the writing or reading address sequence. Selecting ROLL at 50μs/cm. range (not STORED) drives the address lines from the write address counter only. Check each store package has the correct drive from the address counter. Pressing LOCK FULL STORE button drives the address lines from the read counter only and these may be checked also.
2. Check for faulty stores by changing each store with MSB store (IC641).

NO

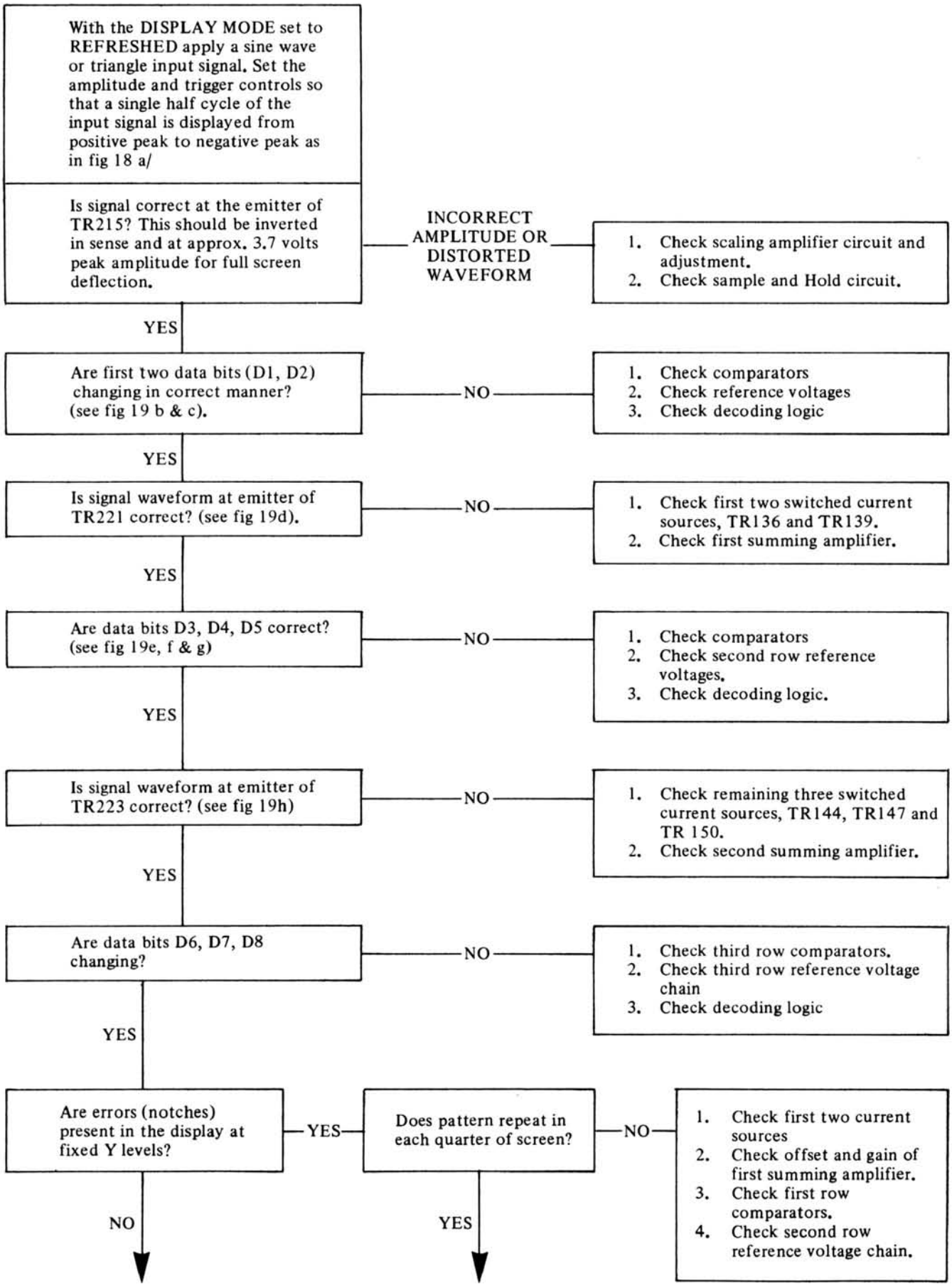
Are steps or discontinuities fixed in Y direction?

NO →
Indicates timing fault or intermittent error. Check:
1. Clock signals to A.D.C.
2. Timing of clock pulses to data in and out latches.
3. Timing of all store control signals and address selector control line.

YES

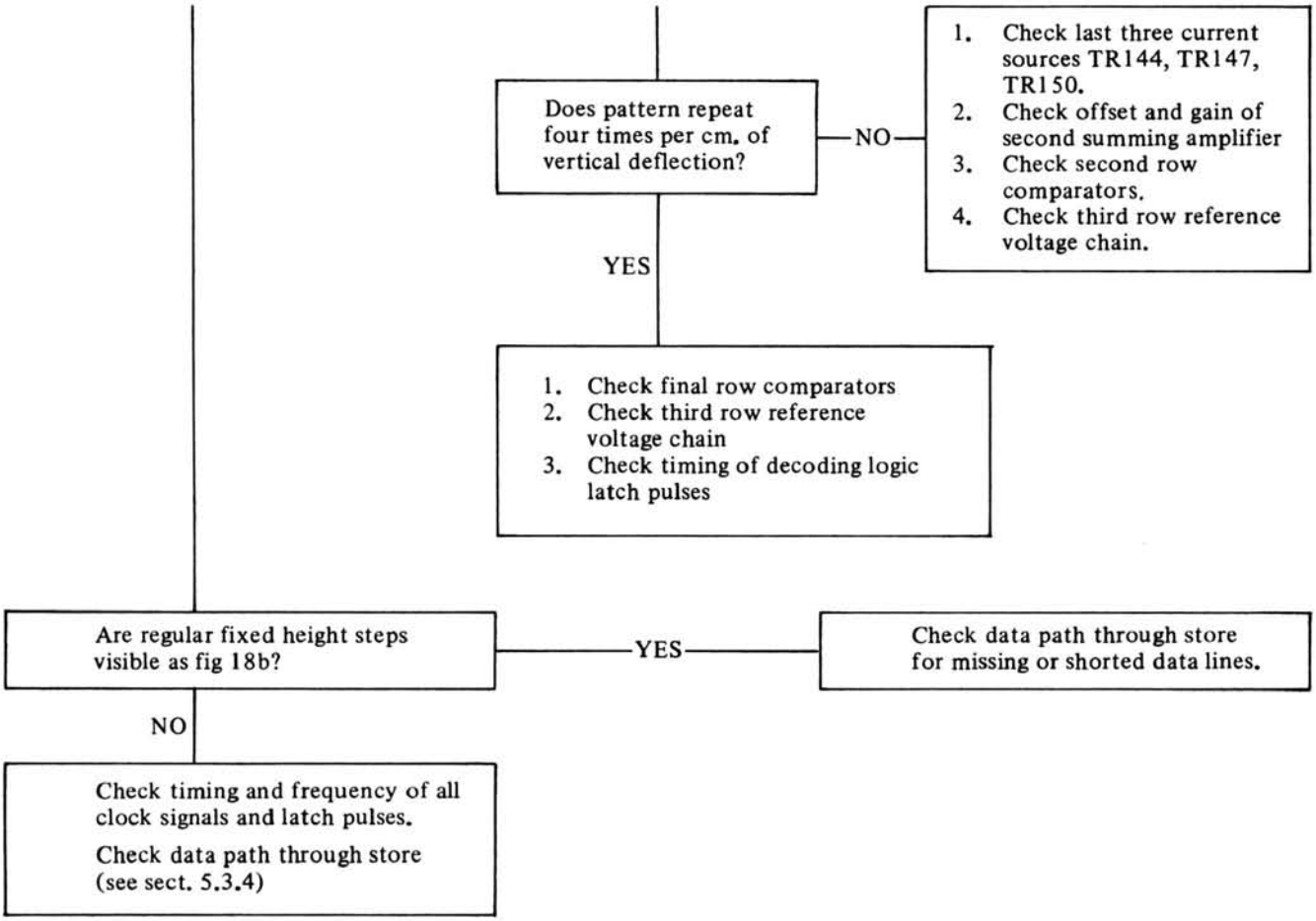
1. Check for data lines shorted (Identical data on two lines).
2. Check A.D.C. (Sect. 5.3.5.)

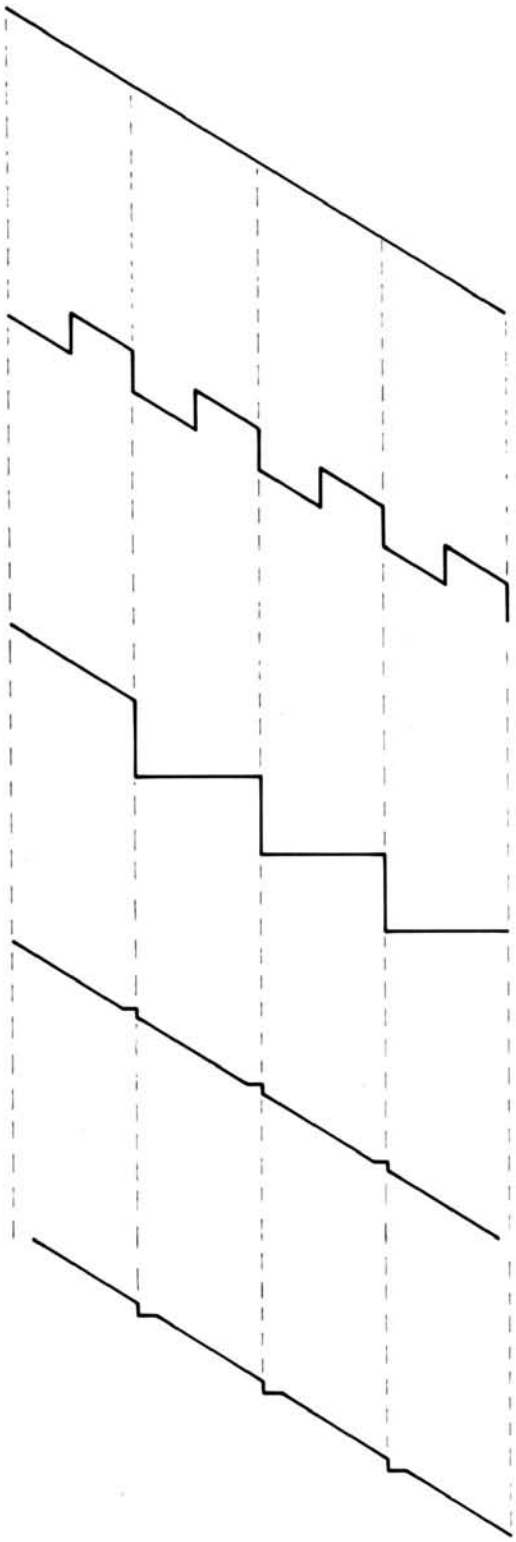
5.3.5 ANALOGUE TO DIGITAL CONVERTOR FAULTS



continued overleaf

5.3.5 (Contd.)


Does pattern repeat four times per cm. of vertical deflection?
NO
1. Check last three current sources TR144, TR147, TR150.
2. Check offset and gain of second summing amplifier
3. Check second row comparators.
4. Check third row reference voltage chain.
YES
1. Check final row comparators
2. Check third row reference voltage chain
3. Check timing of decoding logic latch pulses
Are regular fixed height steps visible as fig 18b?
YES
Check data path through store for missing or shorted data lines.
NO
Check timing and frequency of all clock signals and latch pulses.
Check data path through store (see sect. 5.3.4)



A/ INPUT SIGNAL

B/ DATA BIT MISSING

STEP HEIGHT	DATA LINE
4 cms	D1
2 cms	D2
1 cm	D3
5 mm	D4
2.5 mm	D5
1.2 mm	D6
.6 mm	D7
.3 mm	D8

C/ FIRST TWO SWITCHED CURRENT SOURCES IN ADC NOT WORKING (TR136 AND TR139)
OR
FIRST SUMMING AMPLIFIER FAULTY.

D/ Similar faults for remaining three current sources and second summing amplifier but step height 4 times smaller and pattern repeats over each quarter of the screen.

E/ CONVERSION ERRORS DUE TO

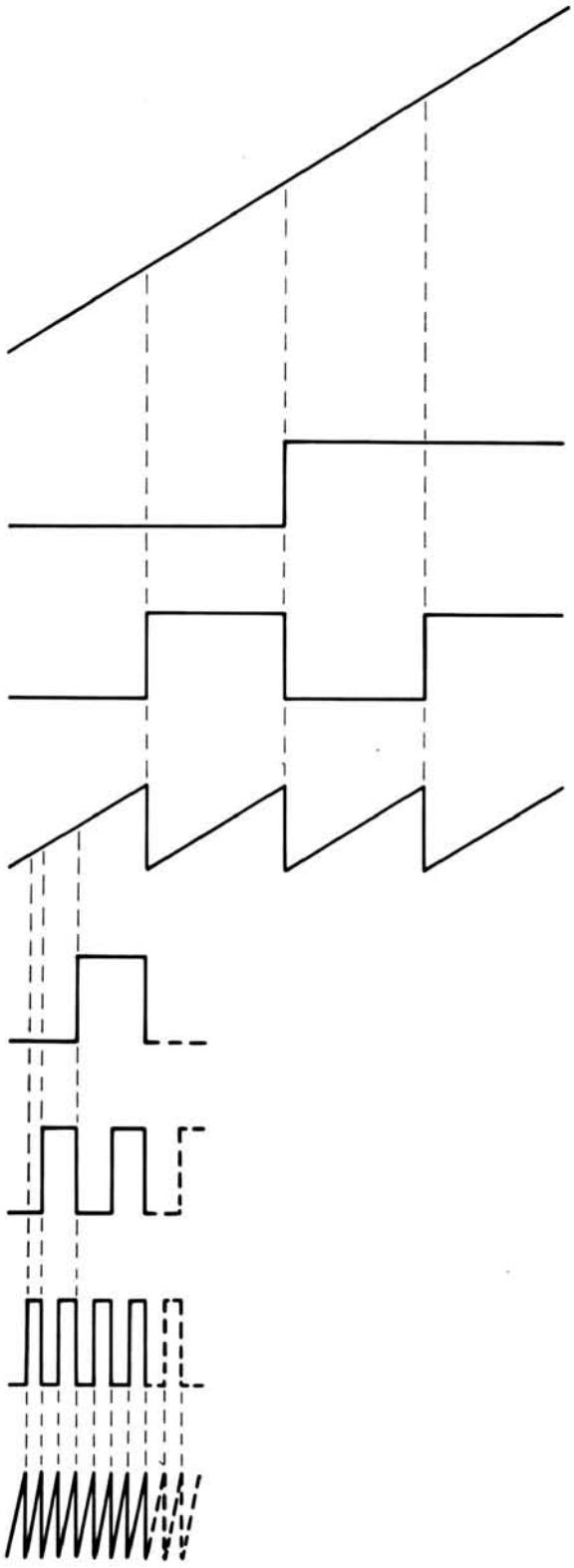
1/ Maladjustment of current sources (R122, R114)

2/ Offsets in first summing amplifiers.

3/ Offsets in first row of comparators.

4/ Timing errors (check clock signal timing)

Fig. 18 Data Faults



A/ INPUT SIGNAL AT EMITTER OF TR215

B/ D1 OUTPUT (SK.F PIN. 16)

C/ D2 OUTPUT (SK.F PIN. 15)

D/ WAVEFORM AT EMITTER OF TR221 OUTPUT OF FIRST SUMMING AMPLIFIER

E/ D3 OUTPUT (SK.F PIN 14)

F/ D4 OUTPUT (SK.F PIN 13)

G/ D5 OUTPUT (SK.F PIN 12)

H/ WAVEFORM AT EMITTER OF TR223 OUTPUT OF SECOND SUMMING AMPLIFIER

Fig. 19 ADC Waveforms