4.1 SYSTEM DESCRIPTION

With the MODE switch in the NORMAL position the instrument operates in a conventional manner. Referring to fig.2., input signals are applied to two identical pre-amplifiers which incorporate the sensitivity controls, both variable and switched, and also the Y shift and input coupling controls. The outputs of these pre-amplifiers are applied to the beamswitch and also to the trigger selector switch. The beamswitch selects one or other of the two channels and on dual trace, is operated either in a chopped or alternate sweep mode, dependent on the setting of the timebase range switch. The output of the beamswitch is applied via the signal switch to the Y output amplifier which drives the vertical deflection plates of the c.r.t. A trigger signal is selected by the trigger selector switch and shaped into fast pulses by the trigger amplifier which contains the trigger level, slope and coupling controls. These trigger pulses are supplied via the control logic to the timebase and initiate a linear ramp, the duration of which is determined by resistors and capacitors switched by the timebase range switch in the usual manner. This ramp is applied via the X amplifier to the horizontal deflection plates of the c.r.t. A bright line facility is available such that when no trigger signal is being received, the timebase is made to free run, producing a visible base line.

When the MODE switch is in the REFRESHED position, the signal switch is changed over so that the output from the Dot Joiner is routed to the Y output amplifier.

Analogue signals from the beamswitch are applied to the Analogue to Digital Converter (ADC) which produces an 8 bit binary code (word) representing the instantaneous signal level at 550 nanosecond intervals.

The data produced by the ADC can be loaded into a store under the control of the timing logic. The store can hold 1024 such 8 bit words and the data is entered at a rate such that the information contained in the whole store represents one complete sweep. This data is then continuously read out (non-destructively) at a fixed rate and reconstituted as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output amplifier to give a continuous display of the store contents. Since the output from the DAC is in the form of discrete levels, a dot joiner is included to join up these levels and provide a continuous display.

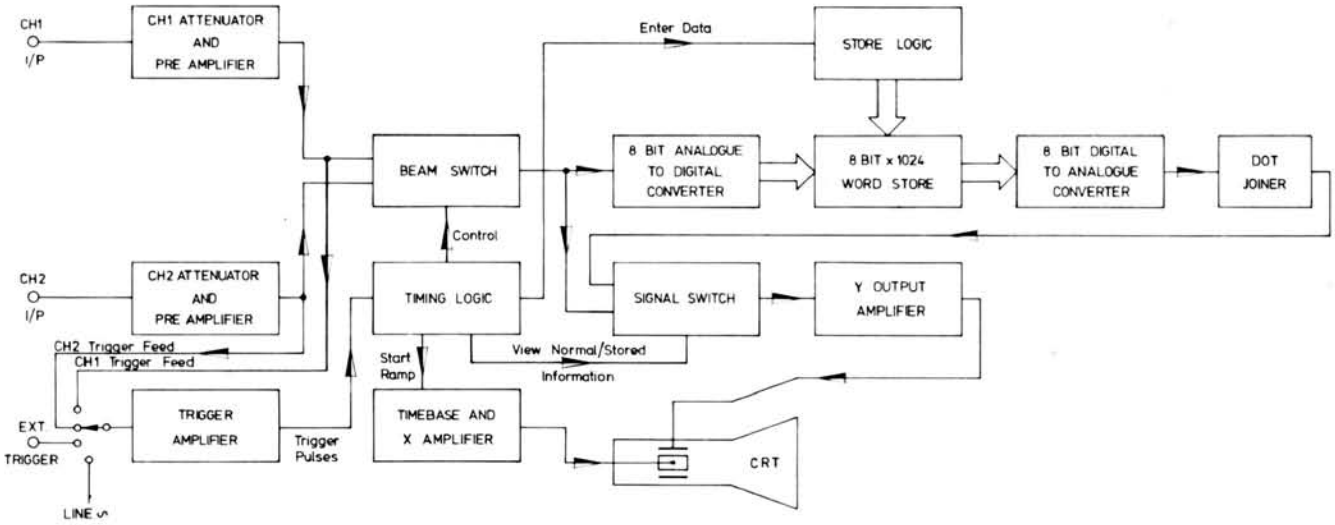

Fig.2 Block Diagram of Instrument

The timebase section provides continuous sweeps at a fixed rate of 100μs/cm irrespective of the setting of the timebase switch, and synchronised to the store read out cycle.

Note that the trigger amplifier is now entirely dissociated from the timebase since the latter is running continuously. The function of the trigger amplifier is to initiate a read-in cycle, when a screen full of new information will be entered into the store. The rate at which new data is entered determines the effective timebase rate of the viewed signal; the 1024 available store locations represent approximately 11.3 cms. of trace length, thus there are 91 samples per cm. A data entry rate of 0.91 MHz would correspond to 100μs/cm. and 91 Hz to 1s/cm. and so on. The data entry rate is determined by a programmable digital divider controlled by the timebase range switch. This divider operates on the basic clock frequency of 1.82MHz which corresponds to 50μs/cm, the fastest sweep rate available in the digital mode.

Dual trace operation in the REFRESH mode is catered for by operating the beamswitch in the chop mode at half the data entry rate, thereby storing samples of each trace in alternate store locations. Since the store is being read out at a relatively fast rate, however, the alternate sweep technique is used during read out, with store

locations relevant to one trace being read out on one sweep, and the remaining location on the next sweep. The STORE control provides a conventional single shot facility to enter one triggered sweep of data into the store, while the LOCK STORE controls inhibit immediately the entry of any new data.
The ROLL mode of operation is similar to the REFRESHED mode except in the way in which new data is entered into the store. Instead of waiting for a trigger pulse to initiate a new data input cycle, data is continuously entered into the store. Thus, if data entry is made to stop on receipt of a trigger pulse, the contents of the store will be information stored before the trigger pulse, rather than after it as in a conventional trigger sequence. To expand this facility, which operates only in conjunction with the single shot store controls, a switched delay is incorporated marked STORED TRIGGER POINT which allows the input of new data to continue after a trigger is received, for a time corresponding to ¼, ½ or ¾ of the store length. This allows the amount of pre-trigger and post trigger information retained in the store to be varied to suit the application.

Circuit References
Each component in the instrument is specified by a circuit reference consisting of a letter prefix and a number. The number also indicates which printed circuit board assembly the component is mounted on as shown below:-

Circuit Reference No.	
0 – 99	Main Frame Components
100 – 399	Analogue to Digital Converter Assembly
400 – 499	E.H.T. Board
500 – 599	Power Supply Board
600 – 699	Store Logic Board
700 – 799	Timing Logic Board
800 – 899	Output Unit 4001 – Fitted as an option. See separate handbook for details.
900 – 1099	Timebase Board.

The location of the various assemblies is shown in Figs.14, 15 and 16.

4.2 POWER SUPPLIES

4.2.1 GENERAL
Referring to Fig.20 all the power supplies for the instrument are derived from the transformer, T51. Two tapped primary windings are switched by S52 to allow for three supply voltage ranges and fuse FS51 provides fault protection. The supply indicator neon, NE 51, is supplied via limiting resistor R58 from the 115 volt tap on the transformer.

4.2.2 LOW VOLTAGE SUPPLIES
Five separate secondary windings supply bridge rectifiers, BR51–BR55, mounted on the transformer and provide unregulated supplies of +170V, +26V, –26V, +18V, –10V and +8V across the reservoir capacitors, C509A, C510, C511, C512, C502 and C51, respectively. Note that the –10V and +8V supplies are floating with respect to ground due to the action of the regulators. The +170V supply is further smoothed by R540 and C509B and protected by fuse, FS501. The + 26V, –26V, + 18V and –10V supplies are fed to high performance integrated circuit regulators, IC503, IC504, IC501 and IC502 respectively to provide stabilised lines of +20V, –20V, +12V and –6V. These devices contain all the circuitry necessary for a conventional series regulator, together with current limiting and thermal shutdown facilities to protect the device against overloads arising from short circuits, etc. Note that the two 20V lines are in fact provided by 15V regulators in conjunction with zener diodes, D503 and D504.
The +8V supply feeds a discrete series regulator comprising transistors, TR505–TR510, and associated components, to provide a stabilised +5V line. The long tailed pair, TR505 and TR506, compares the output voltage with the voltage across the zener diode, D505, and provides an error signal which is passed via the emitter follower, TR509, to the series pass transistor, TR510. A second long tailed pair, TR507 and TR508, senses the voltage drop across the current sensing resistor, R522, and if the supply current rises above 3 amps will shut down the regulator by reducing the reference voltage at the base of TR505. The resistor network, R518, R517 and R520, determines the limiting current and also provides a 'foldback' limiting characteristic by reducing the permissible output current of the regulator as the output voltage falls. This prevents excess dissipation in the series pass transistor under short circuit conditions. The zener diode, D506, prevents the output voltage of the regulator rising excessively high under fault conditions and thus protects from damage the integrated circuits supplied from this line.

4.2.3 E.H.T. SUPPLIES
The two remaining secondary windings are associated with the cathode ray tube (c.r.t.) supplies. The 6.3V winding feeds the c.r.t. heater and the 850 volt winding provides the –1kV and the +3kV supplies. Stabilisation of both lines against supply voltage variations is achieved as follows. One end of the 850V winding feeds the rectifier diodes in the normal manner, the other end passes to ground via a bridge rectifier, BR401. The alternating current in the winding passes through R406 and TR402 as direct current developing a steady voltage across C402. This voltage, controlled by the conduction of TR402, is effectively subtracted from the peak voltage available at the 'hot' end of the winding and thus by varying the base-emitter voltage of TR402, the rectified high voltage supplies can be controlled. The average value of the base-emitter voltage of TR402 is established by the voltage at TR403 emitter. This in turn is controlled by the voltage at TR403 base set by the feedback resistor, R411, from the –1kV supply line and the combination of R409 and R410, thus establishing a closed feedback loop. A small current also flows from the base of TR403 via R407

to the unregulated −26V supply. Since this voltage changes with the line voltage, this trims out any remaining fluctuations in the E.H.T. supplies due to supply variations. The −1kV supply is derived by the diodes, D404, D405 and D406, feeding the reservoir capacitors, C404, C407 and C406. The voltage is smoothed by R413, R414 and C405, C408 and C409 and applied to the grid of the c.r.t. The cathode potential of the tube is held positive w.r.t. the grid as determined by the brilliance control, R419, and the second anode potential is set by R416 to optimise the focus. Small positive voltages set by R417 and R408 are applied to the third anode and interplate shield to minimise raster distortion.

4.2.4 GRATICULE ILLUMINATION

The graticule is illuminated by two lamps, ILP1 and ILP2. The supply for these lamps is derived from the emitter follower, TR401, and controlled by the potentiometer, R402. This circuit is supplied from the 8 volt winding of the transformer via diodes, D53 and D54.

4.2.5 THE TRACE ROTATION COIL

A coil, L51, fitted round the neck of the c.r.t. inside the magnetic shield, is used to align the trace with the horizontal graticule lines. The current for this coil is taken from the pre-set potentiometer, R529, through R530 on the power supply board. The direction of rotation can be reversed by interchanging the coil connections at the power supply board.

4.3 THE Y AMPLIFIER

4.3.1 THE Y PRE-AMPLIFIER

The attenuator and pre-amplifier in Channel 1 are identical to those in Channel 2. Accordingly only Channel 1 will be described. Referring to Fig.21 the input signal is applied to the front panel socket, SKV, and then to the 3 position lever switch, S1, via R22. This switch selects AC or DC input coupling by including or by-passing C20 in the signal path. On the middle position of the switch, the input socket is disconnected and the input to the amplifier is connected to ground. Input sensitivity selection is performed in two stages; the six lowest ranges, 5−200mV/cm, are obtained by switching the gain of the amplifier as described later. The 0.5−20V/cm ranges are provided by switching in a ÷100 attenuator section before the amplifier and repeating the gain switching. This attenuator is formed by R24 and R351 with C305 to set the h.f. response. C303 is adjusted to maintain the total input capacitance of the highest ranges equal to the lower ranges. Diodes, D301 and D302, limit the peak signal voltage at the amplifier input to approximately 8 volts and in conjunction with R26, protect the instrument against damage from inputs of up to 400 volts peak.

The input stage consists of the field effect transistor, TR301, connected as a source follower driving the emitter follower, TR305, via R303. The operating current of TR301 is defined by TR302 which is an identical transistor mounted in a common package with TR301 to ensure close matching and good thermal tracking. TR302 is self biased such that the operating current will develop a voltage across R308 equal to the gate-source potential. Since this same current flows in TR301 and R303 is identical to R308, the voltage at the base of TR305 is equal to the gate voltage of TR301. The drain-source voltage of TR301 is maintained constant by 'boots-rapping' with TR304 and D303. The drain-source voltage of TR302 is also maintained constant by the cascode transistor, TR303. Diode, D304, prevents the base-emitter junction of TR305 becoming reverse biased under overdrive conditions. The voltage at the gate of TR302 can be varied by R373 to balance out small variations in matching characteristics.

The signal at the emitter of TR305 is applied via the switched resistor network, R28/34, and the common base stage, TR306, to the shunt feedback amplifier formed by TR307, R312 and R311. This can be regarded as a 'virtual earth' amplifier with R311 as the feedback resistor and the R28/R34 network as the input resistor. Thus, the overall gain of the stage is selected by S3B to provide the six basic input sensitivities of the instrument. The common base transistor, TR306, is interposed to balance the d.c. offset voltage introduced into the signal path by TR305. Diode D305 is fitted to protect TR306 from reverse base-emitter voltages. The output from the collector of TR307 is taken via R315 to the base of TR309, which, together with TR310, forms a long-tailed pair. Transistors, TR315 and TR308, are connected in a similar fashion to TR306 and TR307 and provide a balancing d.c. voltage at the base of TR310. The mutual conductance of the long-tailed pair is determined by series combination of R319, R320 and R3. Resistor, R3, is the variable sensitivity control and is shorted by S13 when in the 'CAL' position. The preset potentiometer, R319, sets the overall gain of the pre-amplifier and C309 provides h.f. compensation. Movement of the displayed trace will occur when the variable sensitivity control, R3, is operated unless the voltages at the emitters of TR309 and TR310 are equal (except for the input signal) and this balance is set up using potentiometer, R369. The collector current of TR309 feeds into a load resistor on the timebase board to provide an internal trigger signal.

4.3.2 BEAM SWITCH

The collector current from TR310 is passed through a cascode transistor, TR317, to the emitter of the beam switch transistor, TR319. A d.c. current determined by the shift control potentiometer, R1, and the series resistor, R387, is injected at the emitter of TR317 to provide a shift range of ±12 cms. If the base of TR319 is held high (approx. 3.3 volts) the signal current will pass through the forward biased diodes, D313, D315 and D316, to the load resistor, R389. If the base voltage of TR319 is low (approx. 0.4 volts) the signal current will flow through TR319 to ground and D313 will become reverse biased isolating Channel 1 from the common load resistor, R389. An identical beam switch circuit controls the output of

the Channel 2 pre-amplifier but the drive to transistor, TR320, is the complement of that to TR319.
For dual trace operation the beam switching technique employed depends upon the main operating mode switch. In the NORMAL mode the channels are switched on alternate sweeps when the timebase range switch is set to 2 msec./cm. or faster. On the lower timebase ranges the beam is chopped at a 225kHz rate. In the REFRESHED and ROLL modes the channels are always chopped at a rate dependent on the setting of the time-base range switch. On the 50μsec./cm ranges and above, the chopping rate is 0.9MHz; below this the chopping rate decreases pro rata i.e. at 5msec./cm, it is 9kHz and at 5 seconds/cm. it is 9Hz.

4.3.3 SIGNAL SWITCH

The combined input from both channels appears across R389 at a level of approximately 37mV/cm. This signal is taken via R201 to the Analogue to Digital convertor (section 4.4) and also via emitter follower, TR321, to the signal switch formed by diodes, D317 to D320. This determines whether the signal passed to the Y output stage is the direct signal from the pre-amplifiers (NORMAL mode) or the stored signal from the Digital to Analogue convertor (REFRESHED and ROLL modes). In the NORMAL mode, transistor TR324 is turned off and its collector is at a high level thus turning TR325 fully on. The voltage at the junction of diodes D319 and D320 will be low and both diodes will be reverse biased. The two diodes, D317 and D318, will be forward biased and conducting however, and a signal at the emitter of TR321 will be transferred to the junction of D318 and D319, and via R379 to the Y output stage. When a high level is applied via R362 to the base of TR324, this transistor is turned on, TR325 becomes cut off and the situation is reversed with D317 and D318 reverse biased and the signal from TR322 emitter transferred to the output stage. The stored signal from the Digital to Analogue convertor is applied via R355 to the base of TR322. To compensate for the dc level shift introduced into the signal path by the emitter followers, TR321–TR322, a bias supply is provided for the output stage by transistor, TR323, which is operating under quiscent conditions identical to transistors, TR321 and TR322. The collectors of all these three transistors are supplied via R391 and clamped by D321 to approximately −0.7V in order to reduce dissipation in the devices.

4.3.4 Y OUTPUT AMPLIFIER

The Y output amplifier shown in Fig.20 is a conventional two stage differential amplifier. Input signals from the signal switch are applied via SK.U to the base of TR409 and a bias signal at the same d.c. level (approx. +0.6 volt) is fed to the base of TR408. These two transistors form a long-tailed pair with the gain determined by the resistor combination, R437 and R438, in conjunction with the collector load resistors, R441 and R442. The two resistor-capacitor combinations, R443, C424, C426 and R448, C430 provide pulse response correction. The zener diodes in the collectors, D411 and D412, set the collector-emitter voltage across each transistor so that variations in power dissipation (and hence junction temperature) of the transistor with signal amplitude, are minimised. The output signal from this stage is applied to the bases of a second long-tailed pair, TR406 and TR407, which are connected in cascode configuration with TR404 and TR405, respectively.
The c.r.t. deflection plates are driven from the collectors of TR404 and TR405 with inductors, L401 and L402, providing shunt compensation. The networks, C419, C420, R425 and C421, R427 across the gain setting resistors, R426 and R435, provide h.f. compensation to ensure good pulse response.

4.3.5 BLANKING AMPLIFIERS

There are two separate blanking amplifiers producing intensity modulation of the c.r.t. display and these operate with three separate input signals viz:

i) The Sweep Blanking signal. This cuts off the beam except when a timebase sweep is in progress.
ii) Chop Blanking. This is a short duration blanking pulse applied in the NORMAL mode only when the beamswitch is being switched from one channel to the other at the fast chopping rate.
iii) Trigger Point Bright-Up. This is a short duration bright-up pulse applied once per sweep when a trace has been stored in the ROLL mode of operation.

The Sweep Blanking signal is amplified by a d.c. coupled amplifier comprising TR513 and associated components. The sweep blanking signal is derived from a TTL. logic gate (IC902a) in the timebase via R971 (see Fig.24). When no sweep is in progress the sweep blanking signal is at a low level (<0.4 volt) and transistor TR513 is cut off. The collector voltage in this condition is determined by the resistor chain, R526, R527 and R528, at approx. 90 volts. This voltage is applied to the second grid electrode (blanking electrode) of the c.r.t. and the beam is cut off.
When a sweep is initiated the sweep blanking input from the timebase rises to a high logic level (approx. 4 volts) turning on transistor TR513. The base drive to this transistor is limited by D507 becoming forward biased to avoid saturating the transistor and the collector voltage falls to 4 volts, thus unblanking the c.r.t. beam.
The remaining two input signals are amplified by the circuit comprising TR514, TR515 and TR516. Both the Chop Blanking (CB) and Trigger Bright-Up (TBU) signals are produced by TTL logic devices situated on the Timing Logic board and the Store Logic board respectively (see Fig.23). For detailed information on the timing of these signals see section 4.5
The Trigger Bright-Up signal is inverted by the common emitter stage, TR514, and applied to the base of TR515 via R508. The Chop Blanking signals are applied directly to the base of TR515 via R507 and the speed-up capacitor, C505. The signal at the collector of TR515 is fed to the base of TR516 via the d.c. level-shifting network, D508 and C519. The pulses occurring at the collector of

TR516 are a.c. coupled to the grid of the c.r.t. by C506. The resistor, R533, serves to isolate the c.r.t. grid from the relatively low output impedance of the power supply and the clamping diode, D509, prevents the grid from being driven positive w.r.t. the supply, and thus possibly positive w.r.t. the cathode.

4.4 ANALOGUE TO DIGITAL CONVERTOR

4.4.1 BLOCK DIAGRAM DESCRIPTION

The function of the Analogue to Digital Convertor (ADC) is to quantise the instantaneous signal magnitude into one of 256 levels. These levels are represented by an 8 digit binary code (8 bit word) and the conversion is performed once every 550 nanosec.

Referring to the block diagram Fig.3 the input is applied, via a scaling amplifier, to a sample-and-hold circuit. This samples the signal level every 550nSec. and presents this level to the first row of comparators. These compare the signal against 3 fixed voltage levels corresponding to ¼, ½ and ¾ full scale input voltage. The output states of these three comparators are then decoded to give the first two most significant bits of the output data, D1 and D2. A 'remainder' signal is produced by subtracting from the original signal the voltage represented by the two bits already decoded. This operation is performed by a summing amplifier, A1, and a 2 bit Digital to Analogue Convertor (DAC). The reference voltages for the comparators are generated by the precision resistors, R, and the current source, I1. These voltages correspond exactly to the voltages subtracted from the input signal in the summing amplifiers. Typical waveforms are shown in Fig.4.

This process is then repeated using a row of 7 comparators to decode the next 3 bits of data and a further DAC and summing amplifier to drive the final row of 7 comparators.

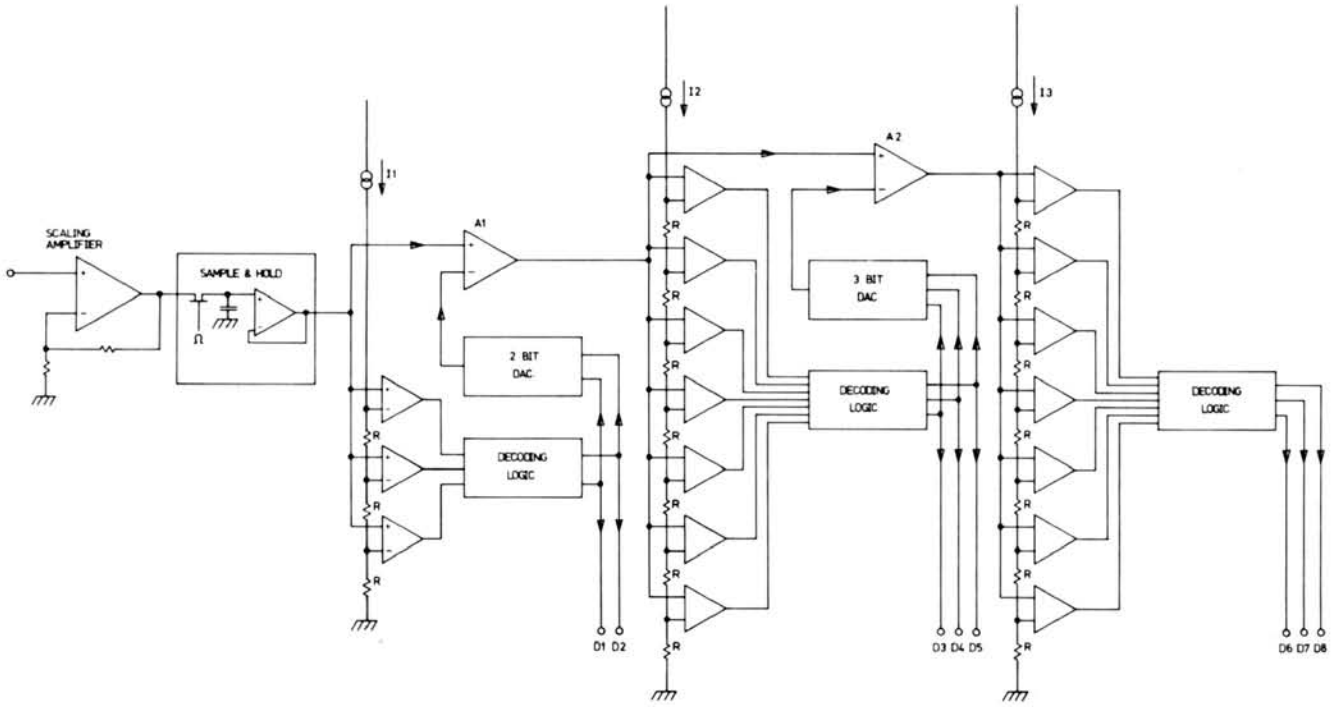

Fig.3 Block Diagram of ADC

4.4.2 SCALING AMPLIFIER

Referring to the circuit diagram Fig.22 the analogue input signal from the beamswitch is applied via R201 to the base of TR201. TR201 and TR202 are a Darlington connected pair which, together with TR203 and TR204, form a conventional long-tailed pair amplifier. The output signal is taken from the collector of TR203 via the emitter-follower, TR205, and fed to the base of the sample-and-hold input transistor, TR206. The gain of the scaling amplifier (approximately x12) is determined by applying negative feedback via the potential divider network, R211, R207 and R208. Potentiometer, R217, and resistor, R209, introduce a d.c. offset into the amplifier output by drawing current through the feedback network. The diodes, D215 and D216, are normally reverse biased and clamp the output signal of the amplifier to within the working range of the ADC.

4.4.3 SAMPLE-AND-HOLD

The signal from the scaling amplifier is presented via the emitter follower, TR206, to the sampling transistor, TR208. This is a junction f.e.t. and it's gate is controlled by the monostable circuit formed by TR209, TR207, TR210 and TR212.