by inverter, IC727a, turning off the ARMED l.e.d. and returning the trigger enable line to the low state. The TRIGGERED l.e.d. is illuminated as previously described until a STOP signal from the store sets the refreshed B/S–Q low. This causes the TRIGGERED l.e.d. to be extinguished and the STORE l.e.d. to be lit. IC733c now has one low input, driving its output high, and the 'enter data' gate, IC733b, has two high inputs making its output (the ENTER DATA line) low. Loading of the store is therefore prevented, until either the RELEASE button or the STORE button is pressed. If the RELEASE button is pressed, IC708a is cleared driving one input of gate, IC732b, low and so turning off the STORE l.e.d. Gate, IC733c, now again has two high inputs, and its output acting on IC733b drives high the ENTER DATA line.
If the STORE button is pressed, IC726a–$\overline{Q}$ is set low driving low an input to IC732b, extinguishing the STORE l.e.d. and causing the ENTER DATA line to go high.

Roll Hold-Off

When the sequence ARMED, TRIGGERED, STORED, has occurred the $\overline{\text{STORE LED}}$ line acting on the 'clear' input of bistable, IC742a, sets its Q low, applying a 'clear' to bistable, IC726b, setting its Q output low. This, acting through inverters, IC731b and IC713b, ensures that the TRIG. ENABLE line is held low when the STORE button is again pressed. Data will be loaded but the refresh B/S will not respond to trigger signals. The bistables, IC726b and 742a, provides hold-off such that when a trigger is eventually accepted and the store generates a STOP signal, the final display consists entirely of information loaded after the last pressing of the STORE button. Without this hold-off, a trigger signal could be accepted immediately and if the stored trigger point switch was set to its top position (100% pre-trigger), the display would consist almost completely of old (previously stored) information. When the STORE button is pressed, the write address counter is clocked and the least significant write address bit (B1) is used to clock IC742a, setting Q high, and this applies a high to the J input of IC726b, and also removes the low on its 'clear' input. This bistable can now respond to the store STOP output acting on its clock input. This will be generated by the next equality to occur between the number generated by the write address counter and the number held in the trigger print store. (This is not modified by the two bit adder circuit since the number set up on the stored trigger point switch, S602, is made 00 by the gates, IC606c, d, turning on when the refreshed $\overline{Q}$ line is high.) The clocking of IC742a by B1 ensures that IC726b is not cleared immediately by an existing equality between the write address counter and the trigger point store (S602 previous set to END TRACE position). When the STOP signal occurs, Q–IC726b, is set high enabling gate, IC731b, and allowing the TRIGGER ENABLE line to go high.

4.6.4 NORMAL MODE BEAM SWITCHING AND CHOP BLANKING

When S601 is set to normal, the read and write counters and the store continue to operate but their precise functioning in this mode is not important. Normal oscilloscope operation will be maintained as long as the timebase switch is set to range 18 or faster. Selecting a range below this will automatically bring in the refreshed mode.
In the normal mode the logic must provide several functions:-
1. Beam switching pulses ('Chop' and 'alternate' depending on timebase range).
2. Chop blanking pulses.
3. Trigger enable.
4. Connect the composite signal from Y input to Y output stage.

The inputs of the quad open collector NAND gate, IC710, are driven from the range switch and the mode switch to provide in normal operation, two lines which are used to obtain the required function.
a) A high on ranges 12/23 + normal line (BOT. 12 NORM).
b) Its inverse (O/P IC710d).
A "low on norm" line is obtained from S601. The timebase range switch connects 8L to ground on ranges 17/1 and hence S601 will ground cathode of l.e.d., D607, the anode of which is fed via the saturated transistor, TR701, from the +5V supply. D601 is therefore lit, indicating normal operation.

Beam Switching

CH1, CH2, or dual trace operation is selected by S603 acting on gates, IC736c and d. When input 10 of IC736c is set low, its output is set high, selecting CH2. When input 12 of IC736d is set low, output IC736c is set low, selecting CH1. If neither 10, or 12 of IC736 is set low, control of channel selection is passed to 13 of IC736d, which is connected to the output of the signal switch, IC709a, b, c, and d. In the normal mode, the "$\overline{\text{NORM}}$" line acting on 9, 10 and 4 of IC709, prevents the signal from the write address counter (12 of IC655) from passing through, and enables the signal from Q of IC708b to control the beam selection. This bistable is switched in two ways depending on the range setting, low sweep speeds select CHOP, high sweep speeds select ALTERNATE.
On ranges 12/17, the $\overline{\text{BOT. 12. NORM}}$ line acting on the 'clear' input of IC708b drives Q low, $\overline{Q}$ high. However the 'preset' input is driven from the gate, IC729a. As 2 of IC729a is high (BOT. 12. NORM line), the signal on the output of IC729a which is obtained from the second stage of the read counter, will control the state of the 'preset' input of IC708b. When the 'clear' is low and 'preset' high, Q is low, $\overline{Q}$ high. When 'clear' is low and 'preset' is low, $\overline{Q}$ is high and $\overline{Q}$ is high. Therefore, although the bistable does not change from one stable state to the other, the output at Q changes under the control of the second stage of the read counter. On the ranges 12/18 therefore the beam switch is operated at a frequency of 227kHz (chop mode). On ranges 11/1 the $\overline{\text{BOT. 12. NORM}}$ line drives the 'clear' high, and its inverse, acting through gate, IC729a drives high the 'preset' of bistable, IC708b. Therefore this bistable is

able to respond to pulses on its clock input, and with J & K high will change state for every –ve transition on its clock input, which is driven via 11/M, N by the display ramp Bistable Q output. Therefore at the end of every sweep, the beam switch will change over.

Chop Blanking

This signal obatined at the common output of three two-input open collector NAND gates IC713a and d and IC716a, with R703 as the common load. Chop blanking is only required in normal mode on the ranges, 12 to 18, when displaying two channels. The $\overline{\text{BOT 12}}$ line acting through IC713d will disable the chop blanking on the top ranges. The CH1, CH2 selection lines are applied to both inputs of gate, IC716d. Therefore if only one channel is selected, the output of this gate will be high, and IC716a acting as an inverter, will disable the chop blanking. As the beam switch in the 'chop' mode is driven from the 2nd stage of the read address counter, the blanking waveform must have a frequency of twice this. Therefore the output of the first stage of the read address counter is taken through an inverter, IC727f, to one input of IC713a, the other input being driven from the clock input to the read counter. Output of IC713a will be a waveform which is low for one system clock period (550ns) and high for three periods.

NOTE: When IC713d and 716a pull the blanking output permanently low, the display is not blanked because the blanking amplifier is a.c. coupled.

4.7 TRIGGER AND TIMEBASE

A clock diagram of the timebase and its control is shown in Fig.13 and the full circuit in Fig.24.

4.7.1 TRIGGER ENABLE

The logic system controls the state of the trigger enable line, 10M/N, to the timebase, which must be high to enable trigger.

In the normal mode, the $\overline{\text{NORM}}$ line acting through S702b (the release switch) on the clear input of IC708a, makes IC708a $\overline{Q}$ high. This is connected to one input of IC731c, a two input NAND gate, the other input of which (driven from the display mode switch) goes low only in ROLL. Consequently its output is low in the normal mode. This output drives one input of open collector NAND gate, IC713b, the output of which is common with IC713c, with R760 as a common load. The inputs of IC713c are driven from $\overline{Q}$–bistable, IC723a, which is disabled in the normal mode (preset low) with its $\overline{Q}$ low. As both IC713b and c outputs are therefore 'off' the trigger enable line is always high in the normal mode.

The state of the Input/Output lines on connector M/N, which connects the logic system to the timebase, is shown below for normal operation.

M/N			
	1	9	
	2	10	Hi
	3 Low during fly back.	11	Hi during sweep
	4	12	Lo
	5 Hi ranges 7/23, Lo 1/6	13	Hi during sweep
	6 Lo	14	
	7	15	Lo
	8	16	

4.7.2 TRIGGER CIRCUIT

The Line, CH1, CH2, and Ext. trigger signals appear on R912, 913, 914 and 915 respectively. R59, mounted on

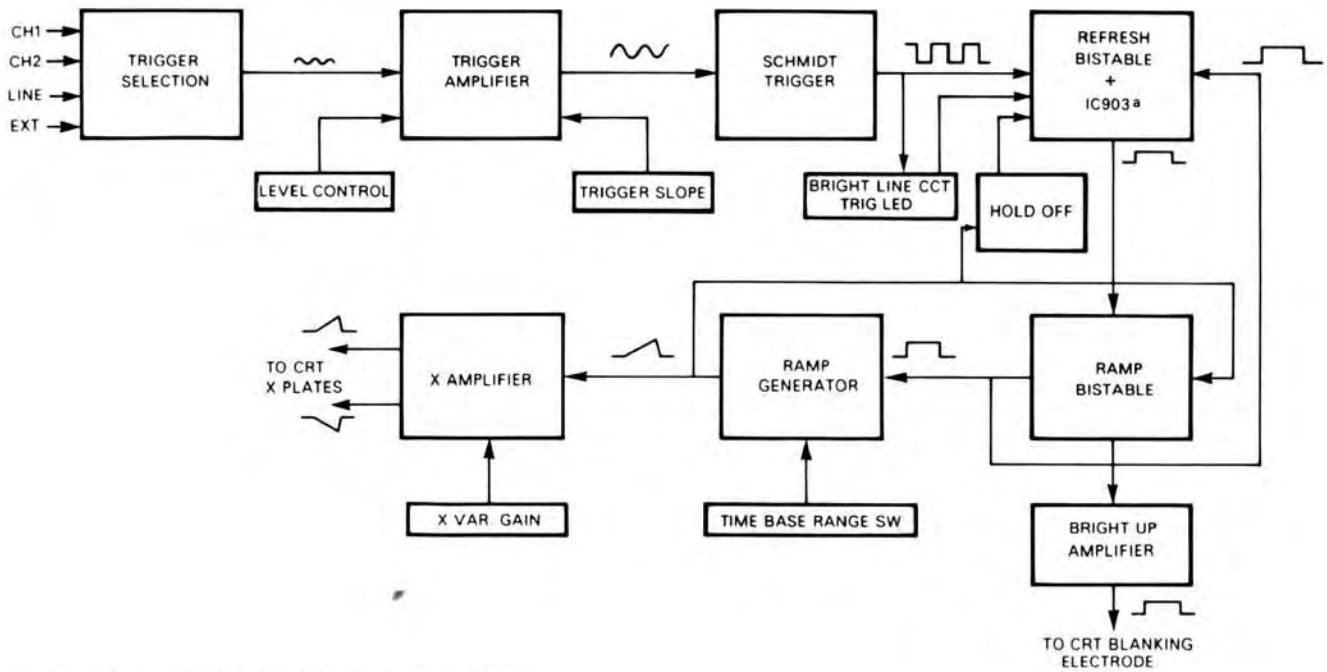

Fig.13 Timebase Block Diagram: Normal Mode

the transformer and connected to the low voltage winding, forms one arm of a potential divider with R912, resulting in a ± 50mV line frequency waveform appearing on R912, R913 and R914 are the collector loads of each TR309, in CH1 and CH2 preamplifiers. One centimeter of Y deflection results in a signal of approximately 25mV on these loads. R90 and R915 form an approximately 200:1 attenuator to external trigger signals. R1010, R1011, and R1008, R1009 are adjusted to take the collector currents which flow in the CH1, CH2 trigger leads, thus maintaining the voltage across R913 and R914 near zero in the absence of Y signals. One of these signals, selected by S900aR, the trigger source and slope switch, is passed to S901, the trigger coupling switch, and from there to the base of TR914. There are four possible signal paths, A.C. coupled via C907, H.F. rej. via C907 and R916 with C909 bypassing h.f. signals to ground. (fco ≙ 15kHz), LF. rej. via C908 with R917 bypassing l.f. signals to ground (fco ≙ 15kHz) or D.C. coupling.

TR914, acting as an emitter follower, passes the trigger signal to the amplifier pair, TR915 and TR916, the potential derived from the level control R7 being passed via emitter follower, TR917, to the base of TR916. Thus the amplified trigger signal appearing between the collectors of TR915 and TR916 contains a d.c. component determined by the setting of R7. The gain of this amplifier is determined by R919, 925, 920 and is approximately 4X. The signal is passed via S900bR to the input of amplifier, TR901/TR902. If CH1, CH2 or EXT are selected the collectors of TR915 and 916 are connected to the bases of TR901/902 for positive slope, and TR902/901 for negative slope. If line trigger is selected, the slope switching is reversed since the line trigger signal is in antiphase to the a.c. supply. TR901/902 form a differential amplifier whose output on the collector of TR902, drives the Schmitt trigger circuit TR903/TR904. The gain of amplifier TR901/902 is approximately 20 and the output d.c. voltage is adjusted with the common emitter resistor, R1012.

The function of the trigger circuit, TR903/904 is to generate a fast negative edge at the collector of TR904, independent of the rate of change of the applied signal. The signal appearing on the collector load of TR903/R932, is coupled via the network, R933, C902 and R935 to the base of TR904, whose emitter is connected to the emitter of TR908 and to the emitter resistor, R934. The emitter coupling introduces positive feedback which results in a latching action as follows:-

When the base of TR903 is at a low voltage, TR908 is off, its collector potential is high, therefore the base potential of TR904 is high turning on TR904. The emitter potential of TR904 is now higher than the base potential of TR903. When the base of TR903 goes more positive than the emitter of TR904, TR903 starts to take some of the emitter current of TR904, causing a reduction in its collector voltage which is communicated to the base of TR904 thus causing a further reduction in the current flowing. This effect is regenerative finally leaving TR903 on and TR904 off. The base potential of TR904 is now below that of TR903. As R932 is small, the change in base potential of TR904 is small (≙ 600mV between these two conditions) so that an a.c. signal of greater amplitude than this applied to the base of TR903 (if its d.c. level is adjusted) will cause the circuit to alternate in state. Thus the output of the circuit for any input above a minimum will consist of a series of equal amplitude pulses. C903 is a speed-up capacitor used to reduce the fall times of the output waveform.

4.7.3 BRIGHT-LINE AND TRIGGER INDICATOR

The waveform appearing at the output of the Schmitt circuit is coupled via R937/C904 to the detector circuit, D901, TR905 and C906. Positive going transitions on the Schmitt output result in C904 charging up via D901. Negative transitions result in the base of TR905 being driven negative, and C906 is charged negative by the emitter current of TR905. If no more negative inputs are applied, C906 charges slowly positive through R939, until the base-emitter junction of TR906 is forward biased. TR906 is then turned on and pulls the base of TR909 negative via R948, turning off TR909, and switching off the l.e.d., D916. If a trigger signal amplitude or level is altered such that the Schmitt trigger generates pulses again, C906 will be charged negative, TR906 is turned off and TR909 is turned on causing D916 to be lit. TR906 also controls the emitter current of TR911 via D903. The base biasing network, R950/R949, of TR911 is controlled by the $\overline{\text{NORM}}$ line via TR910. When $\overline{\text{NORM}}$ is low, TR910 is on, and the base voltage of TR911 is approximately 4V positive with respect to the emitter of TR906, hence when TR906 turns on and saturates, current will flow in TR911 and its load R970, such that TR911 will saturate. Its base voltage under these conditions is approx. 1.5V w.r.t. the emitter of TR906. When $\overline{\text{NORM}}$ is high, TR910 is off and the base voltage of TR911 is equal to the emitter voltage of TR906, therefore no current will flow in TR911 when TR906 is turned on. TR910 can be held off by S7 ("Pull for bright line off" on front panel). The current drawn by TR911 through R970 acts as a d.c. trigger on the timebase bistable in the absence of Schmitt trigger pulses and is only allowed in the normal mode when S7 is open.

4.7.4 TIMEBASE BISTABLES (REFRESH AND RAMP BISTABLES)

The refresh bistable consists of TR912 and TR913, cross coupled via R951 and R955 with C915 and C916 as speed-up capacitors and R953 and R954 as collector loads. The collector of TR913 drives the inverter, TR908, via network, R952. C914, R947 and D900, with the load resistor of TR908, R944, connected to the + 5V logic supply line. Thus the output at the collector of TR908 is in phase with the collector of TR912 and is a T.T.L. compatible signal designated "REFRESH Q" in the logic diagram. A T.T.L. signal on R946 will control the state of TR907 via network, R946/R945. The collector load of TR907 is connected to the base of TR912, hence a low on R946 will cause TR907 to turn on and therefore the

timebase bistable TR912 and TR113 will be reset into the condition of TR912 on, TR913 off. The driven end of R946 is designated as the 'clear' input of the refresh bistable on the logic diagram. This bistable can be set (Q output high) by the occurrence of a negative edge at the output of the Schmitt trigger (collector TR904) via C905, and D904 allows the negative pulse to pass if the junction of R938/R963 is near ground potential. If the junction of these resistors is at approximately + 5.5V, D904 is reverse biased sufficiently to prevent (hold-off) the trigger pulses from reaching the bistable input. (See section 4.7.5 on Hold-Off.) The bistable can also be set (Q output high) by the d.c. trigger current from the bright line circuit via R970. (See section 4.7.3 on Bright line.) This current is also blocked by the hold-off voltage while junction R938/R963 is high.

Assume that the bright line circuit is off, (no current in R970), the hold-off voltage is low, TR912 is on, TR913 is off and the Q output of IC903b (Ramp B/S) is low. A single negative transition at the output of the Schmitt trigger will cause TR912 to go off, TR913 to go on, and the Refresh Q output to go high. This output acts on three gate inputs, IC904c, IC906c and IC902d. For normal operation the table in section 4.7.1 shows that IC902d and IC906c have one input low (12N) therefore their outputs are permanently high and Refresh Q has no effect. Only IC904c is enabled (IC904d + IC904c form a 2 line to one line selector controlled by the $\overline{\text{NORM}}$ line) consequently when 10 of IC904 goes high, the common output (load R968) is pulled low causing a negative edge on the clock input of bistable, IC903b (Ramp B/S). Preset of 903b is always high, 'clear' is controlled by TR919 and is high until the end of sweep, J and K inputs are both high (low on 12N drives the output of IC906 high). These are the conditions required to cause outputs Q, $\overline{\text{Q}}$ of IC903b to reverse on a negative going clock edge. Q output therefore goes from low to high, and driving through inverter, IC905a, turns off TR920 (voltage across base resistor, R961, falls to zero). The timing capacitor selected by the timebase range switch is now free to charge positively (see section 4.7.5 for Ramp Generator). The Q of the ramp B/S (IC903b) also acts on two other gates, IC902c and IC902b, both two input NAND gates. (Operation of IC902b is described in the HOLD-OFF section.) Because 12N is low, the output of IC902d will be high, so one input of IC902c is high. When Q–IC903b goes high the output of IC902c goes low, driving IC902a output high. This supplies current to the bright-up amplifier (mounted on the Power Supply p.c.b.) via R971 and a coaxial lead, causing the c.r.t. beam to be unblanked at the start of sweep.

The ramp generator output (emitter of TR923) goes positive at a rate determined by the time base range switch, reducing the negative base voltage on TR919 via the potential divider R973/R974, and eventually when the emitter of TR923 reaches + 11V, TR919 is turned on, pulling the 'clear' input of IC903b low, causing Q to go low and $\overline{\text{Q}}$ high. ('clear' input of IC903b is connected to N3 into the logic system but no pull-down input occurs on this line in the normal mode.) When Q goes low, TR920 is turned on via IC905a, discharging the timing capacitor. The $\overline{\text{NORM}}$ line (6N) connected to IC905b causes its output to be high (high on NORMal), enabling three gates, IC902b, IC904b and IC904c. This output also turns on the hold-off circuit via TR918.

The output of IC904b (load resistor, R909) goes low when the Ramp B/S is reset, clocking IC903a. Conditions on IC903a are 'clear' high, 'preset' high (see note) J high, K low and $\overline{\text{Q}}$ high. The negative transition of the clock input will cause $\overline{\text{Q}}$ to go low, turning on p.n.p. transistor, TR907, via R946, and so pulling the base of TR912 positive, turning TR912 on, TR913 off, and Refreshed Q output low. This is connected via 13N to the logic system, and controls the 'clear' inputs of bistables, IC734a and b. When Q Refreshed goes low, IC734a and b are cleared and the Q output of IC734a drives the 'clear' input of IC903a low via interconnection 14N, returning it to the quiescent state.

NOTE: On all ranges below 50μs/cm to the slowest available range on normal (200ms/cm), a reset pulse will occur on 15M prior to the end of sweep. This positive-going pulse acting via inverter, IC904a, causes IC903a $\overline{\text{Q}}$ output to go low, thus resetting the Refresh B/S. which in turn clears bistables, IC734a and b, driving Q–IC734a low and via interconnection 14N, clearing IC903a. The clear input is still preset when the ramp B/S IC903b is reset by TR919 and therefore the clock pulse generated by IC903b cannot set IC903a again.

4.7.5 HOLD-OFF CIRCUIT

The $\overline{\text{NORM}}$ line is inverted by IC905b (output high on normal), turning on TR918, connecting one side of the hold-off capacitor (selected by S6dB) to ground, and making an input (5) of the NAND gate, IC902b, high. The other input of this gate is driven high by the Ramp B/S Q output when the ramp is running. Therefore the output of the IC902b goes low during the sweep and the output of IC901a will be driven high, cutting off D912 and diverting the current passing through R962 into D902. This current will charge the hold-off capacitor selected by S6dB, moving the junction of R963, D902 and R938 positively so that D912 and D911 are turned on when the capacitor voltage reaches + 5V plus two diodes forward bias potentials. (+ 6.2V approx.) This voltage acting through R938 drives the junction of C905 and D904 positively so preventing trigger pulses from the Schmitt trigger reaching the refresh bistable. At the end of sweep the Q output of the ramp bistable goes low, and drives the output of IC901a low. D902 is cut off and the hold-off capacitor is discharged slowly from + 6.2V until at approximately 0 volts, D902 again conducts. Therefore trigger pulses are prevented from starting another sweep for a time sufficient to enable the timing capacitor to discharge completely.

4.7.6 RAMP GENERATOR

This can use two timing networks, R1007 and C923 or the resistor and capacitor selected by the time base range switch, S6. The selection is controlled by the TOP 6 and

$\overline{\text{NORM}}$ lines acting on IC905c. In normal mode operation, $\overline{\text{NORM}}$ is low and IC905c output is high. The state of $\overline{\text{TOP 6}}$ has no effect. TR931 is turned on and TR930 is turned off by the differential signal applied from IC905c/905d via level shifting networks, R1002/R1003 and R1006/R1005. TR931 pulls the gate of f.e.t., TR929. low (−10V approx.) turning it off, and gate of f.e.t., TR928, is held by D909 and R1000 at a potential near its source voltage, so that this f.e.t. is turned on. This connects the R and C selected by the timebase range switch, S6, to the input of the ramp generator. Timing network, R1007 and C923, is selected in 'refreshed' and 'roll' operation on ranges, 7/23, by $\overline{\text{NORM}}$ and $\overline{\text{TOP 6}}$ being high. However $\overline{\text{TOP 6}}$ goes low on ranges, 1/6, so that the timebase range switch R and C is always used on these ranges. The ramp generator is a bootstrap circuit consisting of TR921, TR922, TR923 and D905. The timing resistor is connected from the junction of D905 and R978 to the timing capacitor, the other end of which is earthed. The junction of the resistor-capacitor timing network is connected to the base of TR921 via TR928 or TR929.

The voltage difference between the base of TR921 and the ramp O/P, TR923, is about + 0.6 volts, and D905 is a 10V zener diode whose bias current is supplied by R977. Consequently there is a voltage difference across the timing resistor of approximately 10V. The current flowing in this resistor will flow into either TR920 (if it is turned on) or the timing capacitor. If TR920 is on (Q ramp B/S is low) the timing capacitor cannot charge and the ramp output (emitter TR923) remains at approx. + 0.6V above earth. When TR920 turns off at the start of sweep, current flowing in the timing resistor starts to charge the capacitor positively. As the voltage gain between the base of TR921 and the emitter of TR923 is very nearly 1, the voltage across the timing resistor will remain essentially constant, thus maintaining a constant charging current into the capacitor and therefore a linear increase of voltage against time at the output of the circuit. At the end of sweep when the ramp O/P voltage is approx. + 11V the Q of the ramp B/S goes low. TR920 is turned on and rapidly discharges the timing capacitor, bringing the ramp output voltage back to + 0.6V.

4.7.7 X OUTPUT AMPLIFIER

TR924 and TR927 form a p.n.p. differential amplifier whose gain is controlled by the network, R987, R988, R6, R990 and R991. The base of TR924 is driven by the ramp generator and the base potential of TR927 is controlled by the X shift potentiometers, R8A and R8B. Preset controls, R988 and R990, are set so that as R6 is varied from maximum resistance to minimum, the gain is changed by 10 times. As the dynamic range of this amplifier is then only approx. 1.5V under these conditions, D913 and D914 are required to protect TR924 and TR927. The mixed sweep plus shift signal produced by this stage at its output loads, R983 and R998, drives the differential high voltage amplifier, TR925/TR926, whose collectors are connected via R985/R992 to the X plates of the c.r.t.

4.7.8 OPERATION IN THE REFRESHED MODE

Conditions at Logic/timebase interface M/N are:

1		9	
2		10	Hi after release Lo after 'Store' and trigger
3	Low during display ramp fly back	11	Hi during display ramp
4		12	TOP6. REF. $\overline{\text{LOCK 100\%}}$
5	$\overline{\text{TOP6}}$	13	Hi after trigger Lo after 'Stop'
6	Hi	14	
7		15	Stop (Storefull) signal
8		16	Ramp start signal

In this mode the display ramp B/S, IC903b, is controlled from the store, but the refreshed bistable, TR912/3, is under control of the incoming trigger signals as in the normal mode.

Assume that no trigger signals are occurring. The ramp start signal from the store on M/N 16, passes through gate, IC904, to the clock input of the display ramp B/S, setting Q high and via IC905a, drives off the ramp gate transistor, TR920, and starts the sweep.

The $\overline{\text{NORM}}$ line being high selects timing component's R1007, C923 via IC905c, d and $\overline{\text{TR928}}$ to 931. This is a sweep of 100μs/cm. A RAMP $\overline{\text{RESET}}$ signal from the store will occur on M/N3 before the analogue ramp reset transistor, TR919, is turned on by the increasing ramp voltage. This reset pulse acting on the 'clear' input of IC903b drives Q−IC903b low, thus turning on TR920 and discharging the timing capacitor, C923. On timebase ranges 1μs/cm to 50μs/cm, the $\overline{\text{TOP6}}$ line (M/N5) acting via IC905c, d, and TR928 to TR931, selects the normal timing R's and C's, and therefore the sweep speed is that set by the timebase range switch. The analogue ramp reset transistor, TR919, may now be turned on by the increasing ramp voltage before the store generates a ramp reset signal. Thus only a portion of the store contents may be displayed on the c.r.t. on these ranges.

If a trigger signal occurs, the refresh bistable, TR912/3, is triggered as in the normal mode, by a negative step on the output of the Schmitt trigger driving off TR912 and, setting the refresh bistable Q (collector TR908) high. This removes the 'clear' inputs to the dual D type bistable, IC734a and b, making IC734b sensitive to the next $\overline{\text{P4}}$ pulse on its clock input. This drives Q−IC734b high, the $\overline{\text{Q}}$ of IC734a going low drives the output of gate, IC734b, high. This is the ENTER DATA line. Pulses from the range divider can now pass through gate, IC732, to clock the write address counter and also generate store write cycles. Q−IC734a going high removes the 'clear' input from IC903a making this bistable sensitive to the STOP signal generated by the store after 1024 new data words have been loaded. This signal acting via IC904a on the preset input of IC903a, sets $\overline{\text{Q}}$ low, turning on TR907

which in turn, pulls the base of TR912 positive thus resetting the refresh bistable, TR912/3. The refreshed bistable Q output (collector TR908) going low clears bistables, IC734a and b, driving $\overline{Q}$–IC734a high, and this acting via gate, IC733b, drives the ENTER DATA line low, inhibiting the entry of new information into the store. This cycle will repeat for every trigger signal until the STORE button is pressed and starts a single shot sequence. This is described in section 4.7.1.

In the refreshed mode the hold-off time delay is not required. TR918 is turned off by the NORM line (output of IC905b) going low, and this effectively disconnects from ground C90, 91 and 92, the hold-off capacitors.

Read/Write interrupt on ranges 50μs/cm to 1μs/cm. The changing of the display ramp generator timing components on these ranges has already been described. Another special condition applying to these ranges is that the read cycles must be interrupted to enable information to be written into the store. On slower timebase ranges (100μs/cm and below) read cycles taking 550ns occur every 1100ns and write cycles taking 550ns can occur no more frequently. Therefore read and write cycles can be interlaced. On the 50μs/cm to 1μs/cm ranges the write cycles occur every 550ns, leaving no time for read cycles. The system adopted is to read the store at a higher speed (550ns/address) until a trigger signal requires the store to accept new information.

The store then writes 1024 new data words at 550ns/address, and immediately after this two complete reading sweeps occur before another trigger signal is allowed to initiate a new writing sequence (see section 4.6.3).

On the ranges 50μs/cm to 1μs/cm in the refreshed mode with LOCK FULL STORE button out, the TOP6 REF. LOCK 100% line M/N12 will be high. If the Q output of the refreshed bistable, TR912/3, is low (no write cycles occurring) the output of gates, IC902d and 906c, will be high as on the slower timebase ranges. Therefore as IC906c drives high and J and K inputs of the display ramp bistable, this bistable will continue to respond to ramp start pulses from the store. However when a trigger signal switches the refresh bistable Q high during a display sweep, the output of gate IC902d is immediately driven low, causing the removal of the display ramp bright-up via IC902a and c. This is required since the write address counter will now have control of the store so that store data out will not be relevant to this displaying sweep. Also on completion of the display sweep, all three inputs to gate, IC906c, will be high, driving its output low and inhibiting any further displaying sweeps until the Q output of the refresh bistable goes low on the completion of the write sequence.

4.7.9 OPERATION IN THE ROLL MODE

Conditions at timebase/logic interface M/N are as for the refreshed mode. (See 4.7.8.)

The display ramp bistable, IC903b, is under the control of the store previously described for the refreshed mode. The hold-off circuit, C90, 91 and 92 is disabled as in the refreshed mode and the timing R and C are R1007 and C923. Until the STORE button is pushed, the trigger enable line is held low preventing operation of the refreshed bistable, TR912/3, (data is written into the store because input 5 on IC733b is low, driving the ENTER DATA line high). After the STORE button is pressed, the first trigger signal will drive the Q output of the refreshed bistable, TR912/3, high, removing the 'clear' input to bistable, IC734a and b. The first P4 clock pulse after this drives the Q outputs of IC734a and b, high, and the next P4 pulse drives Q output of IC734b, low. Further P4 pulses have no effect. The one clock period wide pulse from Q–IC734b acts on IC605d to allow through one P5 pulse from IC605c which acts as a clock to the trigger point store, IC613, IC621 and IC629, causing the state of the write address counter at the instant of trigger to be held in this store.

When a stop signal is generated by the store, this resets the refreshed bistable as previously described for the refreshed mode. (See 4.7.8.)

Ranges 100μs/cm to 1μs/cm

The TOP6 line acting through IC905c and d, and TR928 to 931, selects the normal timing components for these ranges. The display ramp bistable is reset by the analogue ramp reset transistor, TR919, and set by the ramp start signal from the store. Operation of the refreshed bistable is not effected. The sweep time is insufficient (except on the 50μs/cm range) to display the total contents of the store, and the stored trigger point marker may not be displayed.

On timebase range 7 (100μs/cm) after the RELEASE button has been pressed, the read and write counters are both clocked at 0.909MHz rate, so that the read and write addresses are never coincident. This is also true on timebase ranges 50μs/cm to 1μs/cm where the read and write counters are clocked at 1.818MHz. To generate a display on these ranges, the display ramp start is generated from the read address counter most significant bit until the STORE condition is reached. The write address counter then stops counting so that coincidence pulses are again generated and can be used to start the display ramp.

4.8 D/A CONVERTER AND DOT JOINER

Referring to the circuit diagram, Fig.25, the D/A converter is provided in a single integrated circuit, IC745. The latched eight bit binary outputs from the store, D1 to D8, are applied to the inputs, pins 5 to 12, and determine the output current from pin 4 as a proportion of the input reference current to pin 14. The reference input is fed through R729 from the zener diode, D701. R730 provides fine adjustment of this current to set the full amplitude of the analogue output.

The output from the D/A convertor is in the form of a step waveform which follows each successive change of digital input. The purpose of the subsequent dot joiner circuit is to convert this into a series of straight lines joining these successive levels.

As the D/A output level settles to a new value, amplifier IC744 detects its difference from the dot joiner output, and sets a voltage via sampling switch, TR707, on a storage capacitor, C707. This voltage is sufficient to drive

the integrating amplifier, IC743, to correct the error by the time the next sample is taken.
In more detail, the gain of IC744 and of the complete system is defined by the input resistor, R799, the shunt feedback resistor, R736 and the voltage divider, R751, and R734. The preset potentiometer, R774 with R733, provides a zero setting control to centre the displayed waveform. The output of IC744 is buffered by emitter follower, TR704, to drive the 'hold' capacitor C707 through the sample switch, TR707.
The data from the store is latched by P5 pulses, and the D/A converter and IC744 are allowed to settle before TR707 is switched on during a P4 pulse. These pulses are a.c. coupled by C709 into the base of the saturated switch, TR705. This transistor is normally conducting so that D702 holds the gate of TR707 near to −10V. TR707 is thus non conducting. During the P4 period the drive to C709 goes negative, TR705 is turned off and its collector rises toward + 5V. The emitter follower, TR706, takes the gate of TR707 rapidly toward + 5V until its collector-base junction clamps at 0V. In this condition TR707 conducts. At the end of the P4 period, TR705 is turned on and D702 returns the gate potential rapidly to −10V. TR709 and TR708 generate a similar but inverted drive waveform which is applied via C712 to C707 to compensate for the inherent gate to source capacitance of TR707 which injects an unwanted portion of the gate switching signal into the storage capacitor. The −10V line is defined by the zener diode, D703.
The integrator formed by TR743 can be considered to operate in its simplest form when f.e.t. switch, TR712, is open. In this condition the rate of change of output voltage for a given input voltage is determined by the input resistor, R750, with R785 and the feedback capacitor, C714. The input voltage from C707 is buffered by the emitter follower, TR710. R785 is used to adjust the output slope so that the detected error is reduced to zero at the next P4 sample period. If R785 is mis-set, the output will overshoot or undershoot in response to a step change of input but when set correctly the system will balance in one sample period.
The above condition with TR714 on and TR712 off, holds for the display of single trace information on the top 6 timebase ranges. In this mode, readout is taken on every clock pulse, P4 pulses are applied directly to C709 and the slope defined by C714 and R750 corresponds to 1 clock period.
For dual trace operation on the top 6 ranges or single trace operation on the slower ranges, the readout is taken from alternate clock pulses. The P4 input via C709 is gated accordingly and TR712 made to conduct. This introduces C715 into the integrator to slow the output slope by a factor of two and C713 provides slope adjustment for this mode.
For dual trace operation on the slower timebase ranges, readout is taken on one clock pulse in four, the P4 input to C709 is gated accordingly and TR714 is switched off. R752 and R768 are introduced into the circuit to halve the rate of change of integrator output voltage again, R774 providing balance adjustment.
Switches, TR712 and TR714, are controlled by TR713 and TR711 respectively. When on single trace operation and on the top 6 ranges, both inputs to the base of TR713 are high and TR713 is biased off and R759 holds the gate of TR712 at −10V. When either input goes low, TR713 conducts and its collector voltage is + 5V. D707 clamps the gate of TR712 at 0V for conduction.
TR717 operates similarly to turn off TR714 in all but the top 6 ranges and dual trace operation, but hold it on, either in single trace operation or on the top six ranges. Single trace operation with LOCK. ALT. SAMPLES is equivalent to dual trace.

4.9 CALIBRATOR

This consists of the adjustable current source, TR934, and current steering pair, TR933 and TR932. The most significant bit from the read address counter (11 on IC640b) is applied to the base of TR932 via 4N. The read address counter is clocked continuously at 1.82MHz on range 1/6 and 0.909MHz on ranges 7/23. The 10 bit counter divides these rates by 1024 giving frequences of 1.78kHz and 8.89kHz at TR932 base and also at the output. The drive to TR932 causes the current from TR934 to be switched between TR932 and TR933, where it flows into R1019 and R1020. R1017 is adjusted to give 1V across R1019 and R1020 in series, (1kΩ) and therefore 100mV across R1020 (100Ω). The current required to do this is 1mA so that shorting the 1V and 100mV cal. out pins together will cause 1mA to flow in the link.