Gould 400
Digital Storage Oscilloscope
Service Manual

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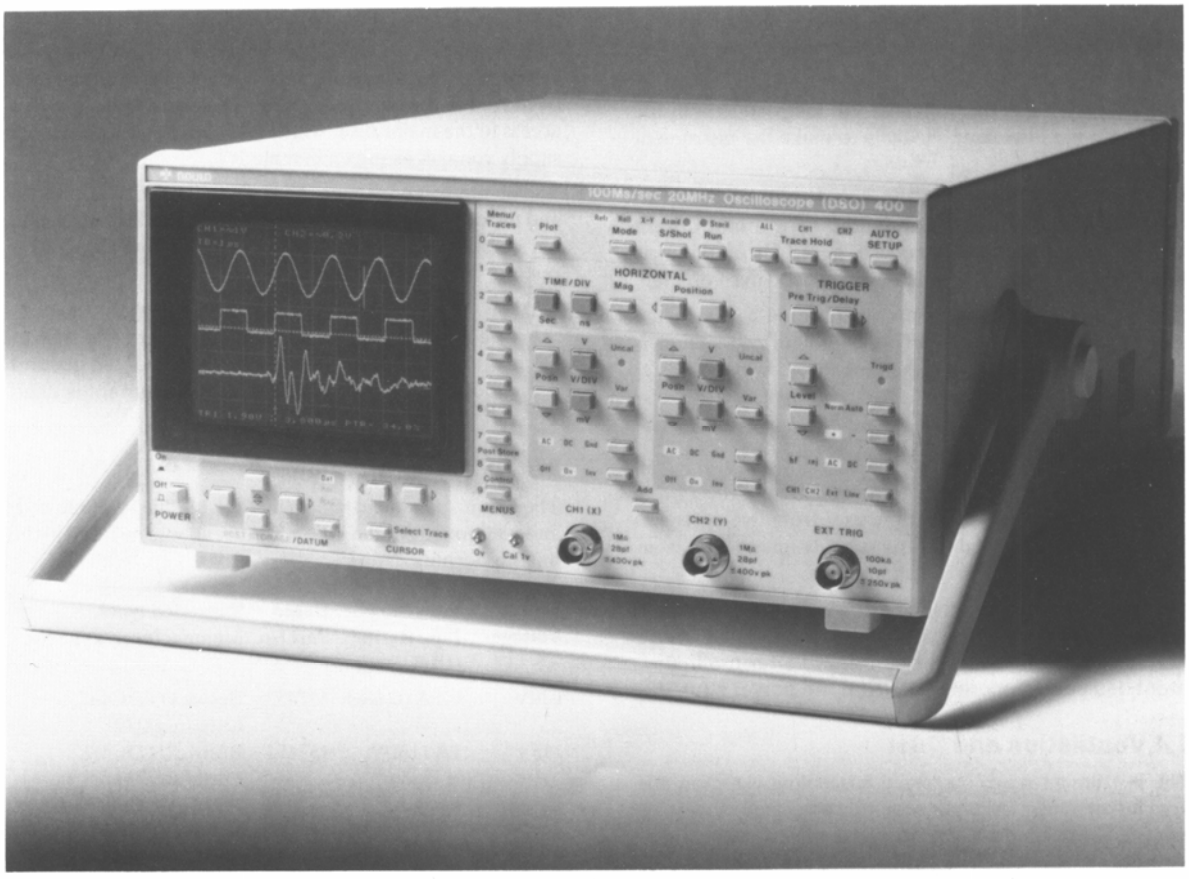
Introduction

This service manual is written primarily for the service engineer who is performing a standard recalibration or who is undertaking repairs when the instrument has developed a fault. The system overview will help the engineer to understand the inner workings of the 400 Digital storage oscilloscope (DSO).

The fault finding procedure given in this manual takes a systematic approach. Starting with the symptoms, the engineer is led to the area or areas at fault by a series of questions in the form of several flowcharts. These require no knowledge of the system, although a basic knowledge of electronics is essential. Throughout this manual a reasonable level of understanding is assumed. A list of abbreviations and mnemonics used is shown in section 9.

Many of the complex operational features of the 400 DSO are performed at chip level. The system includes one large semi-custom gate array which generates the ten phase system and related timings and handles the acquisition of data. On the analogue side there are three semi-custom analogue I.C.'s, two of which are channel preamplifiers providing virtually all the input signal processing, the third is the trigger signal processing circuit. When fault finding, they can be treated as 'Black Boxes' so alleviating some of the more difficult servicing tasks.

Should a problem arise whilst servicing the instrument expert help and advice is available from Gould (see section 10 for details).



1.0 SAFETY AND POWER REQUIREMENTS

1.1 International Safety Warning

(as required for I.E.C. 348 Cat I)

This manual contains information and warnings which must be observed to keep the instrument in a safe condition. The instrument should not be switched on if it is damaged and it should not be used under wet conditions.

1.2 Grounding

AC The instrument must be operated with a protective ground connected via the yellow/green conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply plug is inserted into the socket on the back of the instrument. If the final connection to the supply is made elsewhere, ensure that the ground connection is made before line and neutral.

DC If the instrument is powered from an isolated dc source and not connected to the mains, the unit will not be grounded. Independent provision must be made to maintain the case at a safe potential, preferably by grounding the negative side of the DC supply, or the ground terminal on the rear panel.

Any interruption of the protective ground conductor inside or outside the instrument is likely to make the instrument dangerous.

CAUTION: The negative DC terminal is the ground connection and as such is connected to the instrument case. Care should be taken to avoid ground loops when, for example, the instrument is used in a vehicle.

Signal connections to the instrument should be connected after and disconnected before the ground connection is made, i.e. the supply lead must be connected whenever signal leads are connected.

1.3 Live Parts

The instrument should not be operated with covers removed. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance and repair purposes.

WARNING: Removing the covers may expose voltages in excess of 8000V at the side of the display tube; these may be present for up to one minute after the instrument has been disconnected from the power source.

1.4 Ventilation and Dust

The instrument relies on forced air cooling via a fan and ventilation slots. Adequate ventilation can usually be achieved by leaving a 3" gap around the instrument.

The instrument should not be operated in dusty environments.

If the screen filter requires cleaning it can easily be removed by pressing in its right hand edge as shown by the moulded arrow.

1.5 Operating Temperatures

The instrument is designed to be operated in an environment having an ambient temperature of between 0 and 50 deg. C, and to operate with full accuracy between 15 and 35 deg. C.

Note: *Direct sunlight, radiators and other heat sources should be taken into account when assessing the ambient temperature.*

1.6 Power and Frequency Requirements

The instrument uses less than 85VA and operates from line voltages of 90V to 130V, and 190V to 265V, at 45Hz to 70Hz and 400Hz see section 2. Under the extreme conditions of 90V and 45Hz, the instrument will still operate correctly even if there is a half cycle dropout in the mains supply. The instrument may be powered from a direct current supply in the range 12V to 33V. The unit cannot be damaged by applying power to both inputs simultaneously.

Before connecting the instrument to the supply, ensure that the rear panel mains voltage selector is set to the appropriate voltage. Access to the voltage selector can only be made if the mains connector is removed, and is by lifting the top edge of the connector panel. The selector itself can then be moved to the required setting. This same panel provides access to the mains fuse, which must be changed to suit the supply voltage, as shown in table 1.7

The ac power connection is via a standard IEC connector and the dc power input is via the supplied 0.25" spade terminal connector (Gould part No. 457839). See fig 7.2 for polarity details.

CAUTION: The negative DC terminal is the ground connection and as such is connected to the instrument case. Care should be taken to avoid ground loops when, for example, the instrument is used in a vehicle.

1.7 Fuse Requirements

The fuse arrangement shown in table 1.7 must be followed, and additionally in the UK, a 3A fuse should be fitted in the line supply plug.

Supply Voltage	Slow Blow Fuse Rating (UL/CSA)	Gould Part No.	Suggested types. Manufacturer/Type No.
230V	0.5A (0.6A)	457452	Beswick/TDC488, Littlefuse/239
115V	1A (1.2A)	457454	Beswick/TDC488, Littlefuse/239
12V dc	5A (6A)	457979	HRC type Beswick/S505

Table 1.7 Fuse ratings.

Note: *The DC fuse should be an HRC type with a 1500A break capacity. For different DC voltages, the DC fuse rating multiplied by the voltage used should equal 60W. e.g. at 30V a 2A fuse should be used.*

2.0 SPECIFICATION

DISPLAY

CRT: 5 inch diagonal screen
Raster scan, vertically scanned

Graticule: Electronically generated 8 × 10 divisions with 0.2 sub divisions

Intensity: Separate controls for Traces, Graticule and Alphanumerics

VERTICAL SYSTEM

Two identical channels, CH1 and CH2. Inputs via BNC connectors

Sensitivity: 2mV/div to 5V/div in 1-2-5 sequence

Accuracy: ± 2.5% of reading ± 1 digitising level (1/30 of a division)

Variable Sensitivity: >2.5:1 range allowing continuous adjustment of sensitivity between ranges

Input Impedance: 1MΩ/28pF

Input Coupling: AC-DC-GND

Bandwidth: DC: 0 - 20MHz (-3dB)
AC: 4Hz - 20MHz (-3dB)

Input protection: 400V DC or peak AC at 10KHz or less

Expansion: Post storage × 0.062 to × 4.00

HORIZONTAL SYSTEM

Sweep rate: 27 ranges in 1-2-5 sequence

Transient capture: 500ns/div to 50s/div.

Repetitive sampling: 200 and 100ns/div

Sample rate accuracy: ± 0.01%

Expansion: × 10 with linear dot interpolation

TRIGGER DELAY

Trigger delay range: 20ns to 5000s

Trigger delay accuracy: ± 0.01%, ± 1ns

Pre-trigger: 0 to 100% of sweep in 0.4% steps

Resolution: 2% of time/div, 20ns min.

TRIGGER SYSTEM

Variable level control with Auto/Normal facility, resolution of less than 0.1 div. Auto/Normal

Mode: In Auto the timebase free runs when insufficient signal (20Hz - 20MHz) is present or when the selected level is outside the range of the input signal.

Source: CH1, CH2, External or Line

Coupling: DC, AC or high frequency reject filter

Slope: +ve or −ve

Sensitivity:

Internal DC Coupled	<0.3 div DC to 2MHz
	<1.5 div DC to 20MHz
AC Coupled	<0.3 div 10Hz to 2 MHz
	<1.5 div 4Hz to 20MHz
External DC Coupled	<150mV DC to 2MHz
	<600mV DC to 20MHz
AC Coupled	<150mV 10Hz to 2MHz
	<600mV 4HZ to 20MHz

Range:
Internal ± 10 divisions
External ± 3V

External input impedance: 100KΩ/10pF

External input protection: 250V DC or peak AC

Trigger Jitter: 50s/div to 0.5μs/div, ± 2% of time/div (unexpanded), ± 2ns
0.2μs/div and 0.1μs/div, ± 2ns

DISPLAY MODES

Refreshed: Stored data and display updated by triggered sweep

Roll: Stored data and display updated continuously for timebases 50ms/div to 50sec/div. Trigger stops the updating process

Refresh and roll operate as repetitive single shot for timebase ranges faster than 50ms/div

Dot Join: Dots are joined by vertical raster lines. Linear dot interpolation is provided when the trace is X-expanded

X-Y: X-Y display is 8 × 8 divisions. Stored data and display are updated by triggered sweep. There is no dot joining, × 10 expansion or cursor in this mode. CH1 is used as the × (8 bit resolution 25 steps/div) and CH2 as the Y (7 bit resolution 15 levels/div) deflection

Single trace: CH1 or CH2

Dual trace: CH1 and CH2

Add: CH1 and CH2 can be added to give the algebraic sum of the two channels. Addition is post storage

Invert: Both channels may be independently inverted

Single Shot: Freezes store at the end of a single triggered sweep

Display trace hold:(all) Freezes the display immediately

Channel 1 Trace hold: Freezes channel 1 display immediately

Channel 2 Trace hold: Freezes channel 2 display immediately

Reference trace: One reference trace can be displayed in addition to the two input channels. This can display a waveform memory of a trace copied from CH1 or CH2

ACQUISITION SYSTEM

Maximum sample rate: 100 megasamples/sec simultaneously on each channel

Vertical resolution: 8 Bits (1 in 256) 30 levels per division

Record length: 501 points per channel

ACQUISITION MODES

Normal mode: Transient and repetitive signal capture. (Repetitive capture is only on timebase ranges 100 or 200ns/div, which gives an equivalent sample rate of 2ns/sample on the 100ns/div range.)

X-Y mode: Bandwidth 20MHz (-3dB). Acquisition rate dependent on the timebase range.

Averaging: Averages can be set from 2 to 256 in binary sequence, selected from the menu system. Averaging operates continuously or, using single shot for the set number of acquisitions (weighted average).

Peak detection: Minimum pulse width 2μs for 100% probability of capture. Operates on timebase range 100μs/div or slower

MEMORY

Waveform memory: 3 reference memories are selectable for waveform data storage. These memories are Non-volatile

Setup: The control set up is retained in memory during power down

Retention time: The memory support is trickle charged and will retain information for one month after power down

ON SCREEN MEASUREMENTS and ALPHANUMERIC DISPLAY

Datum Lines: Horizontal and vertical full screen amplitude time and voltage datums

Cursor: The measurement cursor can be assigned to a trace and measurements made in time and voltage with respect to the datums

Cursor measurement display: △Voltage and △Time displayed on screen

Accuracy: Voltage ± 2.5% of reading, ± 1 digitising level (1/30 division)

Time ± 0.01% of reading ± 1 digit

Resolution: Voltage 0.4% of F.S.D.
Time 0.2% of F.S.D.

Trigger Indication: Trigger level indication on screen. On trace trigger point indication

Alphanumerics: Display on screen to indicate vertical sensitivity and input coupling for each channel, timebase speed and pre trigger or trigger delay. Arrow for off screen indication of trigger point and traces

MENU SELECTION

Control master menu: Selects menus for prime functions:- Status, display and trigger facilities, display intensity, reference trace control, RS423 interface, and special functions

Menu/traces: Alternately switches between trace display and the last menu selection

Post storage master menu: Selects menus for fast access to save/recall trace and plot output parameters

AUTO SET UP

Automatically sets the front panel controls to display any applied repetitive input signal for frequencies greater than 20Hz. Trigger and timebase priority is CH1, CH2 and line

RS423 INTERFACE

Serial interface port for bi-directional waveform data and associated range parameter transfer

Baud rate: 75, 150, 300, 600, 1200, 2400, 4800, 9600

Data bits: 8

Parity: None

Start-stop: Fixed one start bit, one stop bit

DIGITAL PLOTTER OUTPUT

The instrument can directly output to suitable HPGL format plotters via the RS423 interface port

Plot mode: Manual or auto selection to output a stored trace

Annotation: Range and scaling annotation, graticule, cursors and cursor readout can all be included in the plot output

Colors: Color pens automatically selected when available

ENVIRONMENTAL

Temperature: Operating 0 °C to +50° C
Full specification +15° C to +35° C
Storage −40° C to +70° C

Humidity: Operating IEC 68-2-Ca at 45° C with 95% RH
Non operating IEC 68-2-D6 cycling, 25° C to 45° C with 95% RH, 6 cycles (144 hours)

Vibration: MIL spec 810D. Random frequency vibrations of 5-500Hz at 1g rms for 15 minutes.
IEC 68-2-6 Test Fc. 15 cycles of 1 minute duration 10 to 55Hz at 0.6mm peak to peak displacement in each of the three major axis (4g at 55Hz)

Safety: Designed for IEC 348 Cat 1 standard

EMC: EMI to BS 6527, VDE 0871 Class A
ESD 10KV to IEC 801-2, BS 6667-2

MISCELLANEOUS

Calibrator: 1V peak to peak ± 1% Frequency approx 1KHz calibration signal on front panel

Ground: Front panel ground reference

POWER REQUIREMENTS

AC Voltage: 90 to 130V or 190 to 265V

Frequency: 45 to 70 Hz. 400Hz operation is available as an option.

DC Voltage: 12 to 33V

Power: 85VA/70W approx

WEIGHT

5.5Kg (12 lb) approx

DIMENSIONS

135mm height × 277mm width × 389mm depth
(5 ½ × 11 × 15 inches) excluding handle

ACCESSORIES SUPPLIED

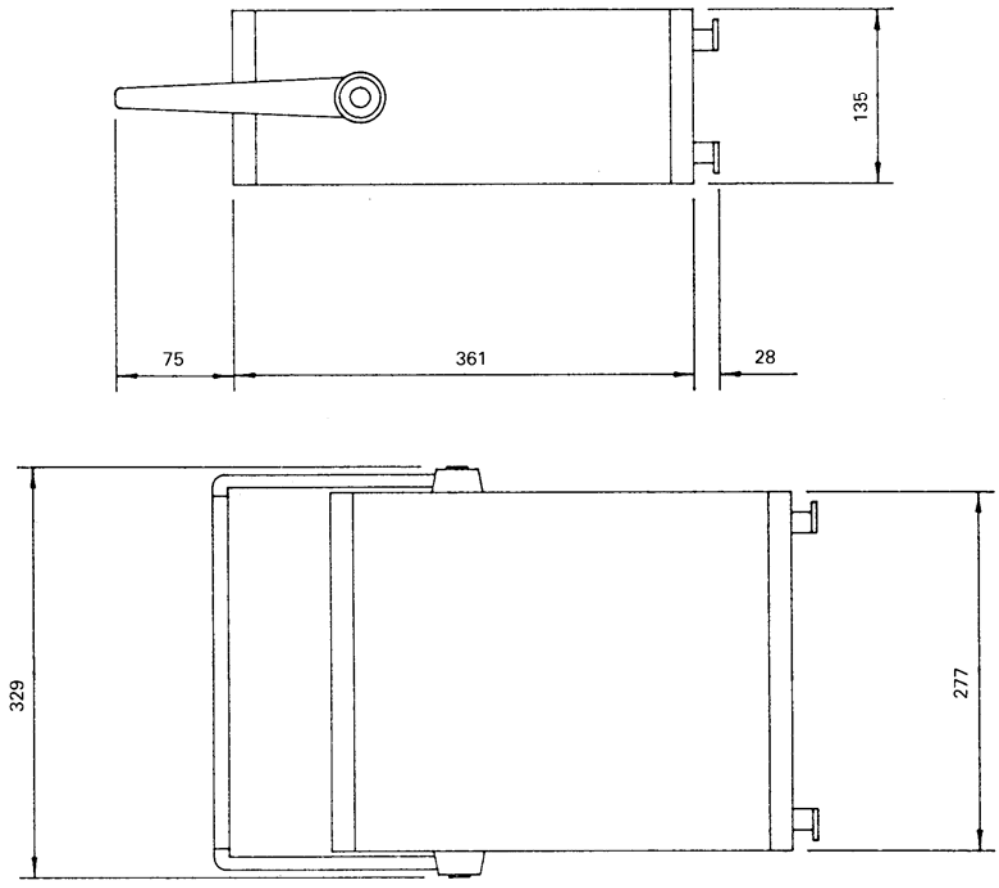
Operating manual	PN 457400
Line cord UK	PN 457826
Line cord USA/Canada/Japan	PN 456980
Line cord Europe	PN 456979
DC power connector	PN 458055

OPTIONS

Option 106: 400Hz operation. This option must be ordered with the 400

OPTIONAL ACCESSORIES

Rack mounting kit	PN 04090490
Carrying case (soft padded)	PN 04101221
Carrying case (hard, foam lined)	PN 04101222
Front facia cover	PN 04101220
Accessory Pouch	PN 04101223
Probe DC to 100MHz switched x1 and x10	PB12
Probe DC to 250MHz 1200V x100	PB17
Probe DC to 7MHz 15KV x1000	PB27
Service Manual	PN 04101224



3.0 SYSTEM OVERVIEW

The first step in understanding the operation of the 400 Digital Storage Oscilloscope is to gain an appreciation of the how a signal is transferred from the input BNC to a trace on the display. Section 3.1 below describes the signal's path through the 400's major circuit blocks. Following this section, microprocessor control, triggering, timebase generation and the CCD are described. For further details see the block diagrams at the end of this section, and for detailed descriptions of each circuit area see section 5.4.

3.1 From the BNC to the Screen

Signals connected to the front panel BNC sockets first encounter the AC/DC coupling circuit followed by the first attenuation stage which either applies a 1:1 or a 50:1 attenuation to the signal, which can have a wide dynamic range from 2mV/div to 5V/div. The degree of attenuation is dependent on the vertical range selected by the operator or the AUTO SETUP function.

The signal now passes into the semi-custom preamplifier chip which performs the rest of the signal scaling including variable gain, invert and vertical shift. The shift level and variable gain control are generated by the microprocessor in the VGEN circuit, the invert control also comes from the microprocessor but via a serial bus line. The preamplifier provides both a signal output and a trigger drive signal.

Next the signal is clocked into the CCD which is under the control of the gate array and the ECL timebase circuitry. The CCD processes the signal in two different ways depending on the timebase range selected.

Timebase ranges 100μs/div and slower:
On these ranges the CCD is clocked at 1MHz and simply acts as an analog delay line.

Timebase ranges 50μs/div and faster:
On these ranges, the signal is entirely captured in the CCD before being replayed for digitisation. The clock rate for the data capture depends on the timebase selected and varies from 2.5MHz to 100MHz. The signal is then read out at a 1MHz rate irrespective of the rate of the capture.

After coming out of the CCD the signal now consists of both CH1 and CH2 data multiplexed together, this common signal is buffered and amplified and has CCD corrections added to it before being digitised onto the YBUS.

Once on the YBUS the data is processed by the gate array and the max-min function is performed if required. Without max-min the signal is unaffected but with it, glitches and aliases can be detected. After the max-min circuit the signal is passed to a store and further processed by the gate array to generate the separate video waveforms for each trace together with the graticule and the alphanumeric display.

These video drive signals are summed together in the video circuit which allows additive signals to produce a brighter image. The individual intensities of the traces, graticule and alphanumerics are selected by the user from a menu and controlled by the microprocessor on the serial bus by switching various resistors into and out of transistor current paths.

The output of the video circuit drives the CRT directly to produce the visible display.

3.2 Microprocessor Control

Most functions within the 400 are directly controlled by the microprocessor in one of three ways:-

Parallel Bus

Most of the data transfer is performed on one of the 8 or 16 bit parallel buses. These functions include the ROM and RAM address and data lines, the vertical signal data, CCD correction and scanning the front panel switches.

Serial Bus

The serial buses consist of a one bit data stream with a clock and an enable line. The data is extracted from the stream by a serial to parallel converter, i.e. a long shift register. Each device on the serial bus uses three connections rather than the ten or more that are required on a parallel bus. Therefore fewer tracks are needed to transfer the data and more output pins can be available on the receiving device.

The serial buses control the input preamp and relay selection, trigger selection, front panel led drives, display intensity and the self calibration attenuator.

Control voltages

The remaining operations in the system are voltage controlled, the voltages being generated by the VGEN circuitry connected to the five VGEN lines from the MPU. The eight voltages generated are used to provide the variable and position levels to the two input channel preamplifiers, a self calibration offset voltage also to the preamplifiers, the trigger level control and a VGEN feedback reference.

3.3 Triggering

Most of the trigger signal generation is performed in the semi-custom trigger amplifier chip. Signals from the two channel preamplifiers, the EXT socket and from the mains transformer (line trigger) are fed to the trigger chip where one of them is selected as the trigger source by the action of the serial bus. A high frequency reject filter can be switched in on the channel or external trigger signals, and a positive or negative going trigger edge can be selected, again controlled by the serial bus. Trigger level control is by an analog voltage into the trigger chip from the VGEN circuit. The trigger amplifier finally produces an ECL level trigger signal.

3.4 Timebase Generation

The trigger signal initiates the acquisition cycle in one of three acquisition modes according to the timebase selected: For the slow timebase ranges, 50s to 50μs, the signal is clocked into and out of the CCD at 1MHz, digitised and 1 in n of the samples are fed to a store at a rate appropriate to the timebase where the complete trace is built up before passing on to the video circuit. For timebase ranges from 20μs to 500ns the signal is clocked into the CCD by the fast timebase clock and again clocked out at 1MHz. Finally for the two fastest ranges 200 and 100ns, the ETS circuitry is used to determine the sampling points. By measuring the ETS ramp level, the software determines when the next samples should be taken and successively samples the entire signal to obtain all the required 501 trace points.

The ECL output from the trigger chip is latched in the ECL circuit and starts the ETS ramp. The next timebase clock after the trigger stops the ETS ramp. The ramp is only used on the two fastest timebase ranges. The trigger signal is then synchronised with the timebase although it has been delayed by two timebase clock periods.

The fast timebase clocks are derived from a master 100MHz oscillator and the 1MHz clock is produced in the gate array. Most of the pre and post trigger counting and timing is performed by the gate array as is the acquisition and data replay timing.

3.5 CCD

The CCD chip forms the heart of the 400 acquisition system. It is basically an analog delay line which has separate clock lines for input and output. This allows analogue signals to be captured at high speeds, i.e. as quickly as one sample every 10ns, the acquired data is then read out at a slower rate (1MHz).

The CCD is constructed internally from eight separate charge coupled lines each 128 elements long. Two analogue inputs are provided which allow the lines to be split into two groups of four. These two sets are driven in parallel by the CCD clock drivers. At the end of the lines within the CCD there are two multiplexers working together: a 1 of 4 multiplexer which is phase related and a 1 of 2 which is channel related. The final output from the CCD is switched by these multiplexers to produce the following sequence: channel 1 FA, channel 2 FA, channel 1 FB, channel 2 FB, channel 1 FC etc. where F means phase.

CCD Correction

Each line within the CCD exhibits a different gain and DC offset which has to be corrected. The gain only varies from line to line, but the offset depends on the particular position along each different line. The offset corrections are held in RAM for each of the 1024 line elements. The signal corrections are applied to the output of the CCD, before the signal is presented to the analogue to digital converter (ADC), by three digital to analogue converters (DAC's) driven from an 8-bit parallel bus.

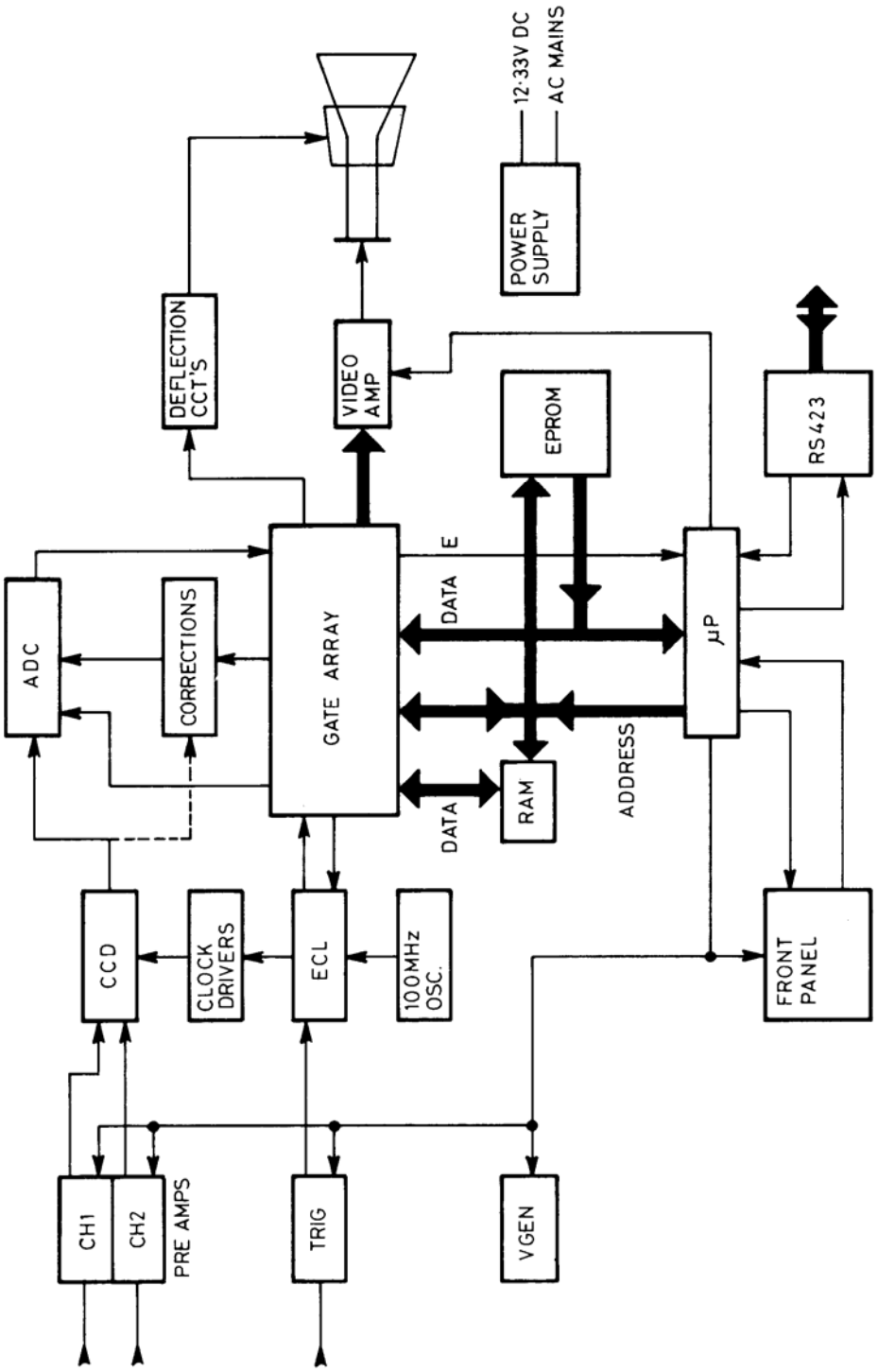


Fig. 3.1 Main System Block Diagram

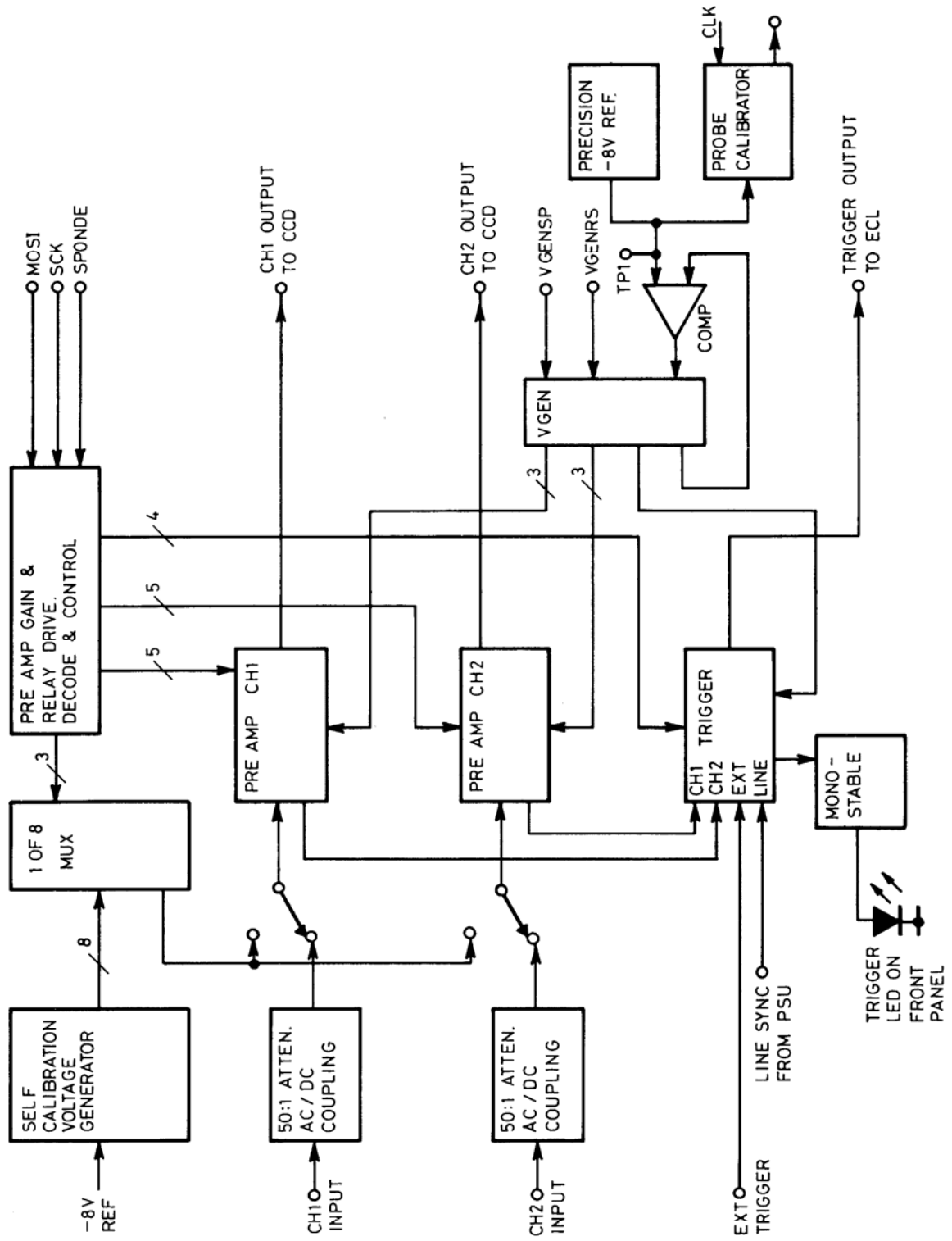


Fig. 3.2 Input Stage Block Diagram

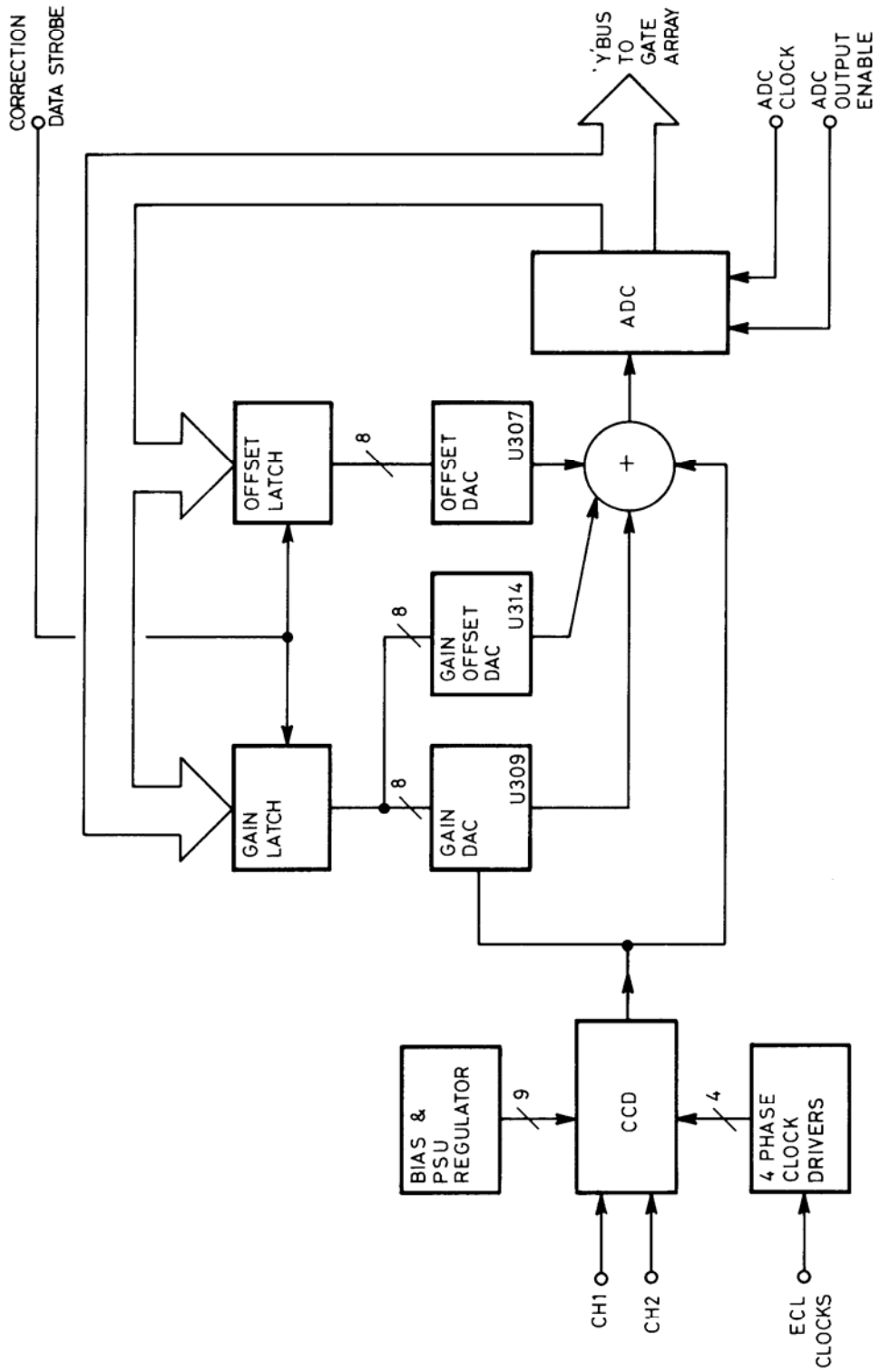


Fig. 3.3 CCD Correction Block Diagram

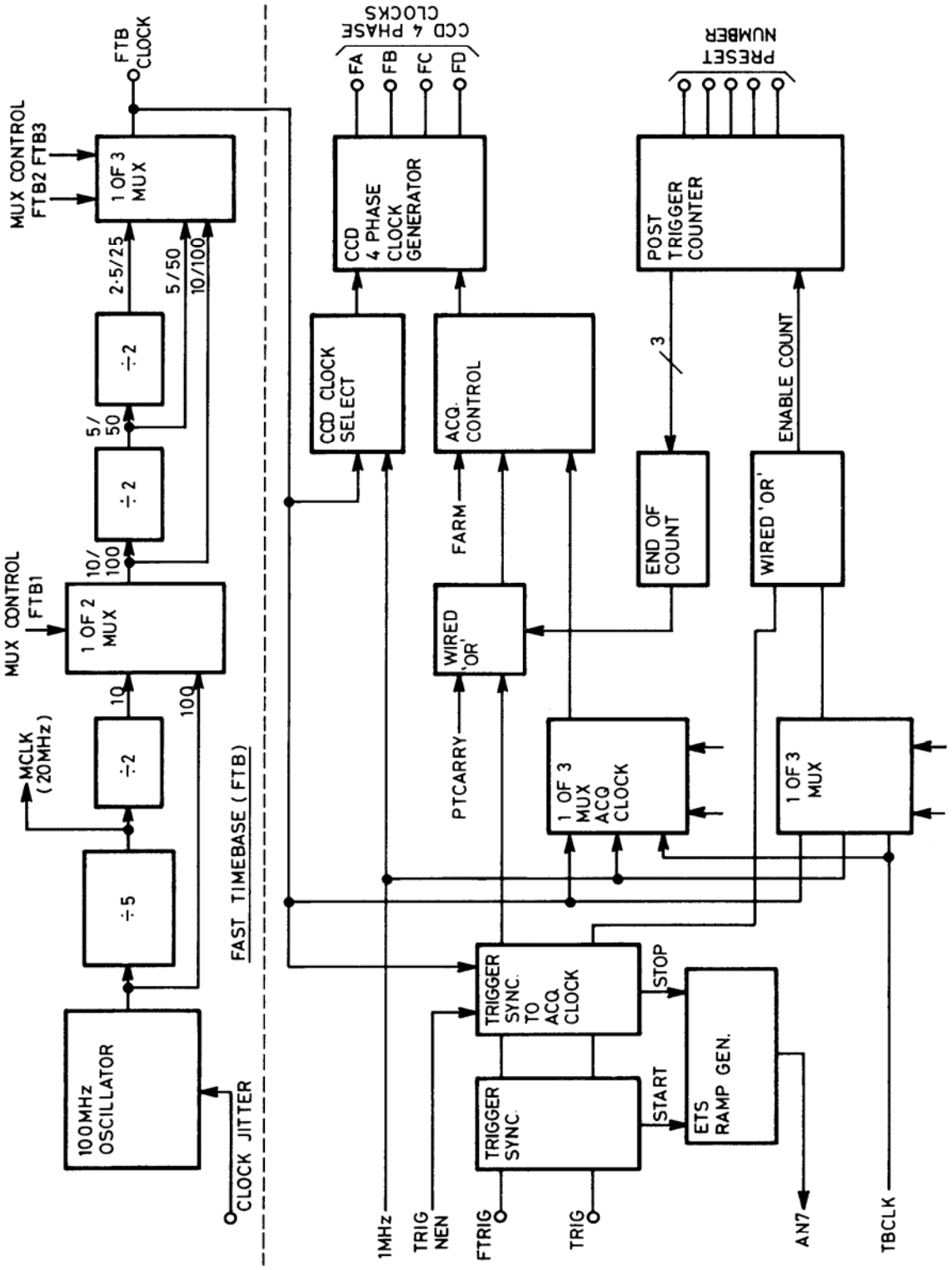


Fig. 3.4 ECL Block Digram

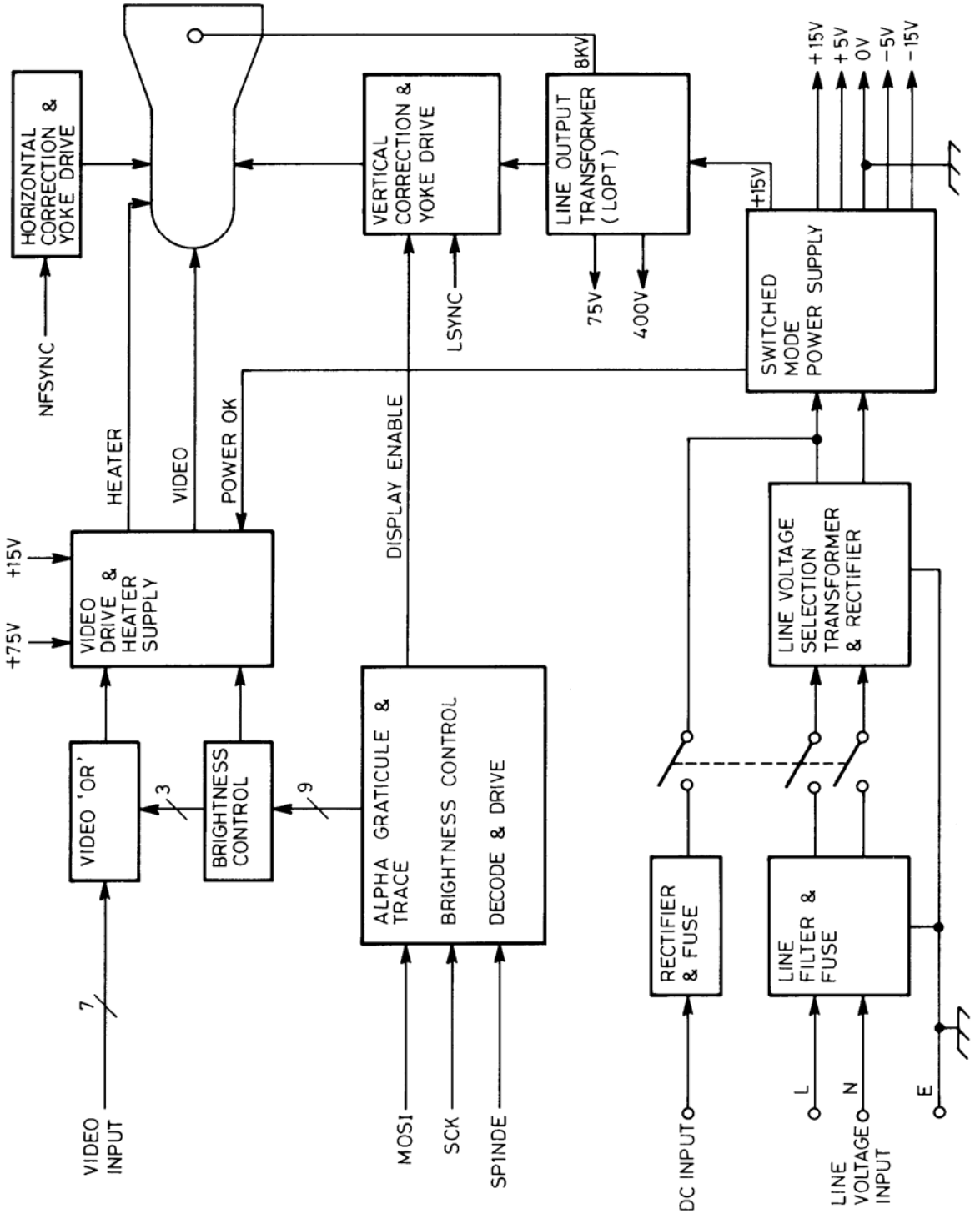


Fig. 3.5 Video & Power Supply Block Diagram

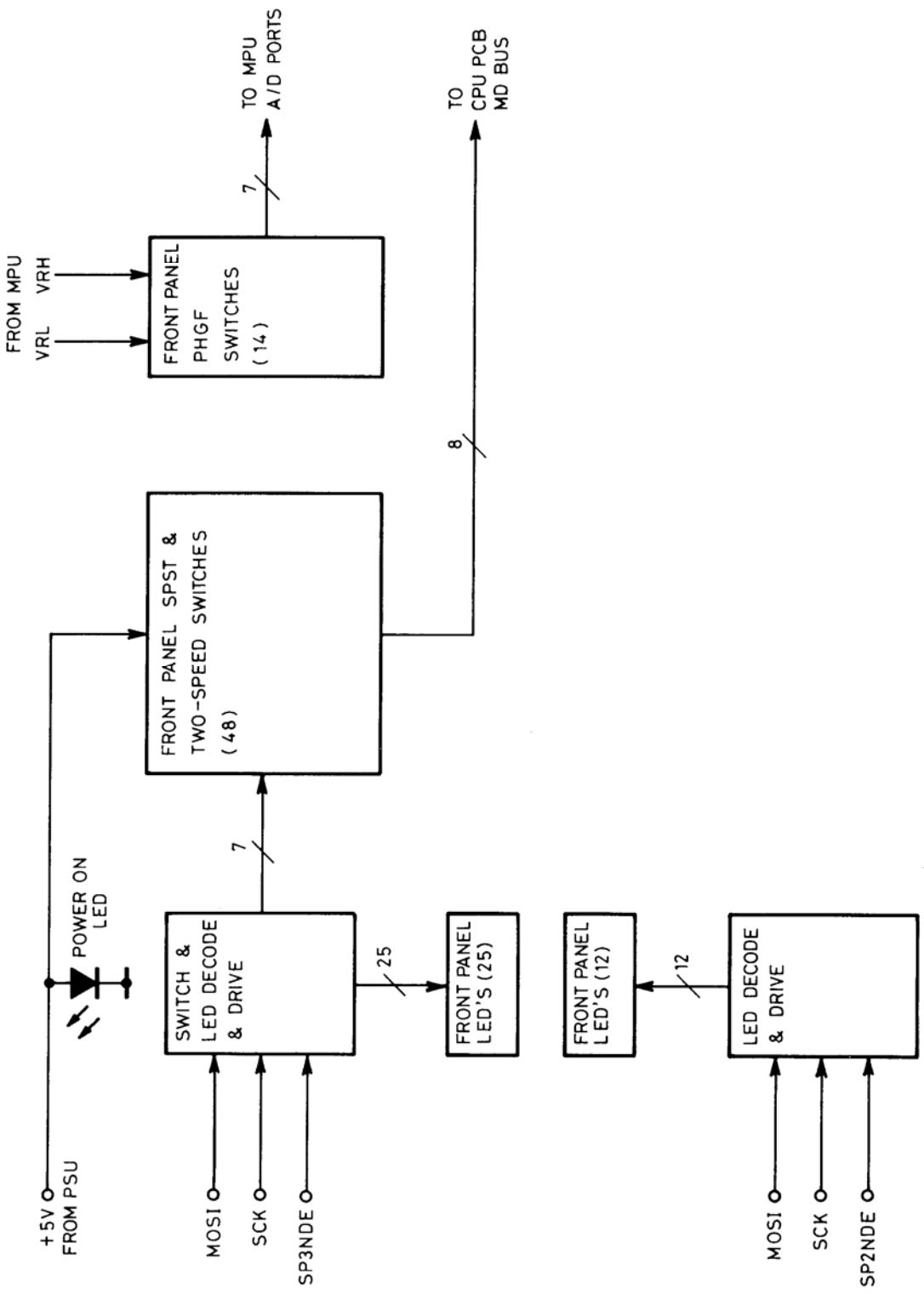


Fig. 3.6 Front Panel Block Diagram

4.0 CALIBRATION and TEST

Many of the features of the 400 are internally maintained in calibration by the microprocessor. However, as with any other oscilloscope, it should have a regular annual calibration. The schedule given below uses a minimum of test equipment, all of which should be readily available in any test department.

The instrument should arrive fully calibrated. This will ensure that the unit will operate within specification for at least a year under normal operating conditions (see section 1). A few of the adjustments in the calibration procedure are interactive, i.e. the setting of one will affect the others. In the schedule below it has been assumed that these controls will be set to approximately the correct positions and will only require a minor adjustment.

All the controls are discussed individually although it is recommended that the entire schedule is completed in order. Calibration cannot be assured if this is not done.

To gain access to the inside of the instrument, remove the four screws in the rear moulding feet, and simply slide the whole cover assembly backwards off the unit. If any dust has accumulated inside the oscilloscope particularly around the fan it should be carefully removed using a vacuum cleaner. All the controls can now be reached, some from the underside of the main board. See figure 7.3 for their location.

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WARNING: Removing the covers may expose voltages in excess of 8000V at the side of the display tube; these may be present for up to one minute after the instrument has been disconnected from the power source.

Numbers in brackets refer to numeric button sequences required to obtain a particular effect, using the menu system. e.g. (9-777) means press button 9 then button 7 three times.

Equipment required

1. Four Digit Digital voltmeter
2. General Purpose Oscilloscope
3. Oscilloscope Calibrator
4. Fast Edge Generator, Tektronix PG506 or similar
5. Function Generator
6. High Frequency Signal Generator, Tektronix SG503 or similar
7. Capacitance Standardiser (28pf), Waugh Instruments or similar
8. 50 Ohm input termination

4.1 400 Calibration Schedule

The correct fuses should be fitted to the unit as shown in table 1.7

1. Power supply
   Check +15V supply on PLG pin 4 to within ±0.2V (R621).
2. Heater voltage
   Check for +12V on CRT brown lead to within ±0.2V (R718).

Display Set up

Note: *The centering magnets on the rear of the yoke are NOT for centering but to make the center of the display as linear as possible.*

3. Initial display
   Set R735 (Intensity) midway. Adjust R734 (Black Level) for a visible background raster.
   Remove all the geometry correction magnets from the pegs on the yoke assembly. Set R746 mid way. Adjust R706 and R709 so that the raster sweep width is approximately 80mm and ensure that the ramp appearing on the horizontal scan coils is approximately centered about 0V, by monitoring the top of R717.
4. Center linearity
   Twist the yoke assembly by adjusting the yoke clamp so that the graticule lines are as near horizontal and vertical as possible. Only look at the central part of the display as any corner distortion will be confusing.
   The ring magnets should now be adjusted to make the center lines of the graticule as straight as possible.
5. Vertical position and height
   Adjust R746 (raster vertical adjust) and L702 (height) to get a vertical raster approximately 62mm centrally positioned on the tube face.
6. Video alignment
   Adjust R741 (video delay) so that the graticule is set 2mm from the top of the raster.
7. Black level
   Set graticule to lowest intensity above off (menu 3). Adjust R734 for a just blank background and just visible graticule lines.
8. Horizontal position and width
   Adjust R706 (horizontal position) to align the left hand edge of the graticule 5mm from the left hand edge of the display. Adjust R709 (horizontal width) for a graticule width of 80mm.
9. Picture Geometry Magnets
   The uncorrected display tends to have pin cushion rather than barrel distortion. If necessary, this can be corrected with the geometry magnets, part number 458026, as follows:

   WARNING: High voltages exist on the CRT. Exercise extreme caution while fitting magnets to the yoke.

   a) Ensure that the major axes of the display are straight and perpendicular.

   b) Push a ½" square rubber magnet onto each of the four "diagonal" pegs on the yoke. Adjust each of these four magnets to push in their corners of the display.

c) Add a magnet to the top and bottom pegs. These magnets affect the top and bottom edges of the picture and also affect whether the two ends of the top or bottom edge are the same height. Adjust them until the top and bottom edges of the display are as straight as possible.

d) Add a magnet to each side peg. Adjust them for the straightest edge to the display

A second magnet may be required on a peg and in these cases, it must be aligned with the first so that their fields reinforce, not cancel, each other.

10. Intensity
Set alpha intensity to max (3-3). Reduce R735 from maximum to obtain reasonable alpha numeric focus in corners. Keep R735 within ¼ of a turn from max.

11. Focus
Adjust R745 for best overall focus, particularly at the corners of the graticule.

13. CCD Supply voltage
Set R364 for +14.50V at TP4.

14. VGEN. reference
Adjust R61 for -8.00V at TP1.

15. Default calibration
Select initialse cal. stores (9-777-6). Disable autocal (9-6-1).

Avoid using Y shift controls until next full software calibration.

Set R9, R22 & R390 midway and both channel inputs to GND.

16. Invert Balance
Select 10mV/div on both channels, adjust R373 for central traces. Adjust R82 for no channel 1 invert movement. Change to 100mV/div and adjust R9 for no channel 1 invert movement.
Repeat as necessary until there is no movement on either vertical range.
Repeat the whole process for channel 2 using R83 for the 10mV/div range and R22 for 100mV/div.

17. Step balance
Select 0.1V/div on both channels. Adjust R373 for central traces. Check CH1 & 2 step balance, 0.1V to 10mV/div for less than ± 3 divs.

18. Y Calibration
Apply a 600mV 1KHz calibration signal to both channels switched to AC coupling with a timebase of 0.2ms/div. Adjust gain (R390) for best gain compromise between CH1 & CH2. Adjust R373 for best centring of both traces.

19. Autocal.
Select Full Calibration (9-6-4). When complete, check CH1 & CH2 calibration status (9-777-2), (see section 4.4). Any excessive deviations are highlighted. If the instrument fails calibration (indicated on status pages), try a calibration hardware test (9-777-4), this checks the DACs. If no failure message is displayed but the gain deviation required is greater than ±2% then proceed as follows.

a) Note the deviation required, select trace mode and set CH1 to 0.1V.

b) Apply a 600mV 1kHz calibration signal to CH1 with the deviation of the calibrator set to the value noted in a).

c) Adjust R390 to make the peaks of the square wave exactly 6 screen divisions apart.

d) Repeat the Full Calibration (9-6-4) and check for a deviation of less than ±2%.

20. Attenuator compensation
Set both channels to 0.2V/div, and set the timebase to 50μs/div. Connect high amplitude pulse output from PG506/106 set for approximately 6 divs amplitude at 10KHz to channel 1. Adjust C2 for a square corner. Repeat for channel 2 adjusting C17.

21. Input capacitance
a) Change the timebase to 5μs/div and switch channel 1 to 0.1V/div. Apply a 0.1V × 10div 1KHz calibrator input to CH1 only via a 28pF standardiser. Check that the over/undershoot on squarewave corner is less than 6%. Switch calibrator and volts/div to 0.2V and adjust C3 to match previous shape.

b) Transfer calibrator signal to CH2 input and repeat test adjusting C16.

22. Internal calibrator
Adjust R56 for 1 Volt amplitude signal at the front panel calibration output within ± 1% by comparison with amplitude calibrator (Bradley). The frequency should be approximately 1KHz (±15%).

23. ETS Ramp correction (see section 4.6)
Select ETS Setup (9-777-4). Apply a 1MHz sinewave to CH1. Set R514 fully clockwise.
To set the ETS ramp slope, press button 6 and after approximately 10 seconds note the number shown. Adjust R514 slowly anticlockwise until the number is in the range 4 to 6. After each slight movement of the potentiometer, pause for a few seconds to monitor the ramp minimum number. If it falls below 5, turn R514 slightly clockwise and then press button 6 to restart the test. Repeat this until the number shown is consistently 4,5 or 6. Wait about 15 seconds after each change of reading.

24. CCD Phase correction
10MHz sinewave 0.1μs/div. Adjust R385, R387, C370, C371, for optimum waveform on CH1 & CH2 when S/Shot is pressed repeatedly.

25. LED Intensity
Select Roll mode and ensure that Horizontal Mag is off, no holds are on, no red LEDs are on, no HF reject is selected, and that neither the armed or stored LED is on, so that there are a total of 11 LEDs illuminated including the power on LED. Six of these are connected to U1 and 4 to U2.

Measure the voltage across R15 on the front panel PCB and adjust R12 for 150mV i.e. 25mA per LED. Measure the voltage across R14 and adjust R13 for 100mV i.e. 25mA per LED.

26. Back-up battery current

CAUTION Performing this test will cause all stored trace and calibration data to be lost.

Remove LK1 from the CPU board and measure the trickle charge to the battery. On a nearly fully charged cell the current should be approximately 3mA. Remove the mains and/or DC supply to the unit and measure the discharge current from the battery which should be a maximum of 100μA.

For further performance checks, see section 4 of the operators manual.

4.2 Test Menus

To aid the test and calibration process, there are a series of test menus which either activate a function or provide information on the current state of parts of the system functions. The front panel controls remain live while the test menus are displayed allowing, for example, the calibration status to be checked for different timebases.

The Test menus are obtained by pressing numeric button 7 three times when the control master menu is displayed. If the instrument is turned off while a test menu is being displayed, the instrument status menu will be shown when the unit is next powered up.

4

4.3 Noise Debug

Repeatedly pressing button 1 selects the noise debug function for CH1, CH2 or Off. When it is on, the selected trace is magnified by a factor of 4 in the Y direction and displayed as the reference trace. This mode is not required for calibration purposes.

4.4 CH1 Calibration Status

Selecting this option using key 2 provides a numeric display of the status of the various calibration coefficients for CH1. Pressing key 6 changes the display to the calibration status for CH2. Pressing key 6 again returns to CH1 calibration status.

To exit from either display, use the Menu/Traces key.

Any value that is marginal, i.e. close to, but not failing calibration, will be shown in inverse video. If an inverse video 'S' is shown, this indicates that the shift calibration for that range is marginal. If an inverse video 'V' is shown, this indicates that the variable gain offset for that range is marginal. If an inverse video 'TL' is shown, this indicates that the trigger level gain calibration is marginal.

The limits for indicating marginal status are selectable for the factory Test or QA departments by key 6. The limits are detailed in table 4.4 below.

	Highlight Limits Lower	Upper	Fail above
Gain	±6.5%	±18%	±21.4%
Offset	±37mV	±41mV	±50mV
CCD offset	±94	±104	±128
Shift	±2.6 div	±3 div	
Variable gain offset	±6 div	±7 div	

Table 4.4 Calibration Limits

Pressing key 1 on a calibration status page will select the information for the next CCD phase in the sequence 0, 1, 2, 3, 0... The gain % values should be similar between phases. The offset values will be the same on every phase, and the CCD offset values whilst being closely grouped within a range, may have very different average values from one range to another. The offset and CCD offset values will change if the channel under examination is switched to invert.

If any calibration coefficient is marginal, then the message "WARNING: MARGINAL CALIBRATION" will appear even if the marginal coefficient is not on the currently displayed page. If any calibration sequence has failed, then an appropriate message will appear instead. The status "CAL COMPLETE" indicates that an attempt has been made to calibrate all coefficients, even if some have failed calibration or are marginal. "CAL INCOMPLETE" in inverse video indicates that at least one calibration coefficient has not been computed due to aborting a full calibration or initialising the calibration stores (see section 4.8).

The gain deviation shown gives assistance in setting up the gain pot R390. See section 4.1.19 for details.

4.5 Test Cal Hardware

Selecting this function causes the response of the CCD gain and offset correction DACs to be shown graphically on the screen. The gain DAC response should be an almost horizontal line which may slope either up or down from the 00 end. The offset DAC line should be sloping down roughly 45 degrees from the 00 end.
Button 7 returns the display to the test menu.

4.6 ETS Setup

When this function is selected, the instrument is set to the fastest timebase range in a repetitive capture mode. Any held traces will be lost. This test is used to set the slope of the ETS ramp, see item 28 in calibration schedule.
Press button 7 to exit from this test.

4.7 ETS Debug Mode

This mode is used to check the ETS function, and draws a histogram 5 divisions wide at the bottom of the screen, which should be set so that its amplitude is as even as possible across its width. Set R385 & R387 to mid-travel, C370 & C371 to minimum (vanes open). Select copy trace 1 to reference trace (9-4-2) & ETS debug mode (9-777-5). Connect 1MHz sinewave of suitable amplitude to CH1 input and adjust R514 for as even an accumulation of points as possible along the 5 division trace at bottom of screen (histogram). In order to restart accumulation the timebase will need to altered by one range, keeping within the ETS ranges.

4.8 Initialise Cal Stores

Selecting this option sets the RAM data for all the calibrations to their mid values. When a full calibration is performed, reseting the RAM data is the first thing to happen.

4.9 RS423 Test Interface

The two options possible from this function are HPGL and TEST; selected by successive presses of button 7. The normal mode is HPGL where the RS423 interface is used to output trace data as described in the operators manual. In the test mode, control of the unit is given to the test ROM fitted as U2. If the test ROM is not fitted the message 'CANNOT FIND TEST ROM' is displayed.

If this function is test rather than HPGL the message 'INSTRUMENT UNDER REMOTE CONTROL' is added to the RS423 interface menu and trying to change the Baud rate or the handshake from the RS423 interface menu has no effect.

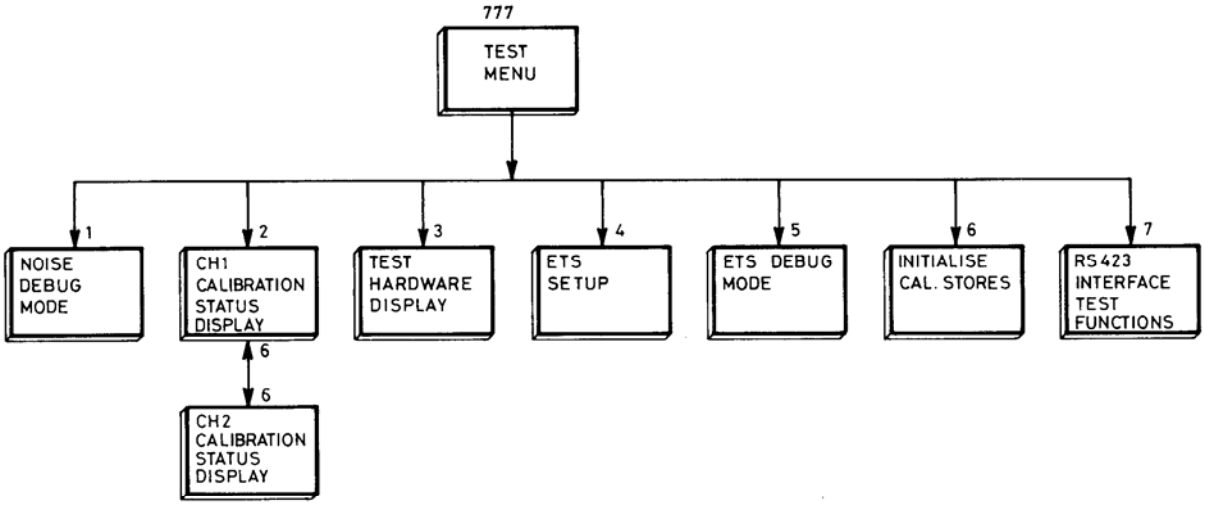


Figure 4.2.1 The test menu structure

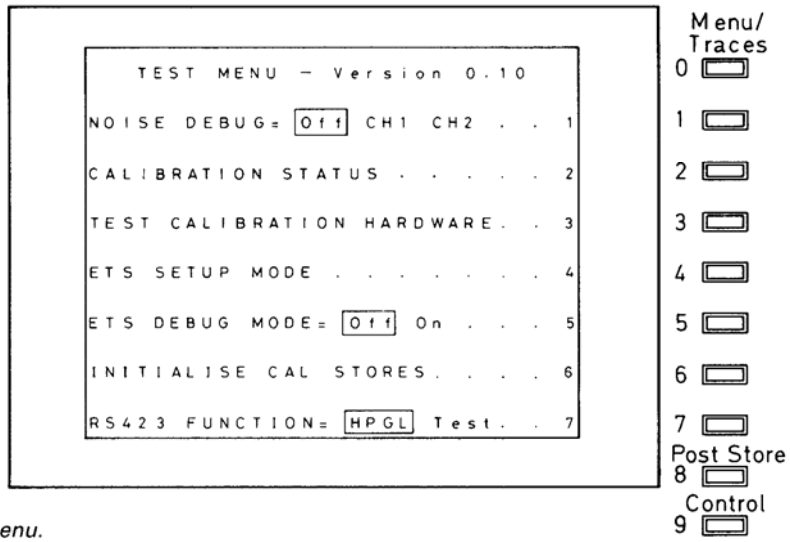


Figure 4.2.2 Test Menu.

5.0 SERVICING

This section takes a systematic approach to servicing a faulty instrument. Starting with a list of symptoms, symptom tables are consulted. These indicate a section of text or a flow chart which will aid in locating the faulty area(s). At the end of this section are the circuit descriptions. These describe the circuits block by block indicating what the circuit does rather than how it does it. It is left to the engineer to interpret them and to make the final diagnosis of the fault within the circuit areas. Unless stated otherwise all component references refer to components located on the main printed circuit board.

WARNING *Many of the circuits within the 400 contain high voltages, in some cases in excess of 8000V. Suitable precautions should be taken whilst working on a 'Live' instrument. The circuits associated with the tube can retain charges for about one minute after power down.*

5.1 How to Use this Section

This section covers the detailed information required to service a faulty 400. It is divided into three parts: symptom tables, fault finding flowcharts and circuit descriptions.

When approaching an instrument for servicing it is necessary to discover all the symptoms of a fault. In some cases this can be easy; for example if the microprocessor fails then the instrument will be unable to do anything. But many very different faults have fairly similar, if not identical symptoms.

With the list of symptoms consult the symptom tables. These are rather like the index of a book, the symptoms referring to a flowchart or a piece of text in section 5.3.

The flowchart will lead to the faulty area(s) by giving instructions for a series of measurements to be taken on the circuit boards. These are fairly detailed but no knowledge of the instrument is required to follow them. There are two types of box on these flowcharts: decision boxes and command boxes. Decision boxes have sloping sides and two exits, one marked 'Y' for Yes and one marked 'N' for No. The command boxes have straight sides and contain instructions about actions that need to be performed.

Having ascertained the area at fault, or in some cases the component, the final decision as to the required cure is left to the engineer. Considering the high reliability of the components used in the 400 it may be advisable to establish the cause of the failure.

To find a circuit area on the main PCB refer to the block location diagram figure 6.1.1. To find the position of a component, locate it in the parts list preceeding the circuit on which it appears and note its grid number. This grid refers to a position on the PCB as shown in the layout drawings figures 6.2 to 6.5.

Section 5.4 provides descriptions of all the circuit blocks. These are of varying sizes depending on the function(s) provided. Typical in-circuit measurements are given, particularly in the analogue areas, to aid the engineer.

The 400 contains many features controlled and calibrated directly by the microprocessor. When a circuit fails within one of these control loops the results are not predictable. This uncertainty is caused by the software/hardware interaction. The fault finding flowcharts presented take this into account.

The flowcharts are based mainly on the failures of semiconductor devices. These are the most likely faults on new models. However, as the instrument ages interconnections and wiring will tend to fail more frequently. This type of fault may be deduced from the circuit areas that apparently fail.

5.2 Symptom Tables

The tables given below cover the most likely symptoms to be expected. They are used in conjunction with Section 5.3 to locate the faulty circuit areas.

Before using the symptom tables ensure that all the internal plugs and sockets are securely connected, that there are no broken wires and that the CPU board is pressed fully home into its connector.

How to Use the Tables

1. Make a list of the fault's symptoms.
2. Check through the index of symptoms, Sections 5.2.1 to 5.2.7, and make a note of the likely faults.
3. Refer to each of the indicated tables for a more detailed description of the fault and its symptoms.
4. If one of the tables matches the fault closely then follow the procedure given in the text. If not, re-check the problem and its symptoms looking for additional clues.
5. Where a function appears not to work, it may be that the front panel switching is not performing correctly. If the front panel LEDs do not show the correct operation of the selector switches then see fault 5.3.5 before looking too deeply into individual circuit blocks.

5.2.1 General System faults

Table No.	Symptom
5.3.1	Total System Failure
5.3.2	Total Failure of trigger system
5.3.3	No CRT display
5.3.4	Some or all the front panel LEDs not working

5.3.5	No response to some or all front panel switches
5.3.9	No alphanumerics
5.3.10	Memories lost on power down
5.3.11	Alphanumerics unreadable or incomprehensible
5.3.12	No dot join
5.3.13	No trace display in X-Y mode
5.3.14	Power supply unit not working
5.3.15	Variable shift and level do not work (VGEN Faulty)

5.2.2 Display Faults

Table No.	Symptom
5.3.3	No CRT display
5.3.9	No alphanumerics
5.3.11	Alphanumerics unreadable or incomprehensible
5.3.12	No dot join
5.3.13	No trace display in X-Y mode
5.3.16	No horizontal deflection
5.3.17	No frame blanking
5.3.18	Poor focusing
5.3.19	One or more traces not displayed
5.3.20	Cramping of horizontal lines
5.3.21	Cramping of vertical lines

5.2.4 Triggering Faults

Table No.	Symptom
5.3.2	Instrument fails to trigger
5.3.6	Trigger source and coupling not selectable
5.3.7	No external; or No line; or No channel trigger
5.3.22	Cannot trigger from the EXT source
5.3.23	High frequency reject filter not selectable or always selected
5.3.24	No control of the trigger level

5.2.5 Acquisition Faults

Table No.	Symptom
5.3.25	Trace off the top or bottom of the screen
5.3.26	Trace 'stepped'

5.2.6 Y Preamplifier Faults

Table No.	Symptom
5.3.8	Trace distorted
5.3.27	No Y shift or variable gain
5.3.28	Invert not functioning
5.3.29	One or more attenuator range or input coupling selection not available
5.3.30	Input coupling not selectable

5.2.7 I/O Faults

Table No.	Symptom
5.3.31	No calibrator signal
5.3.32	No Response over RS423

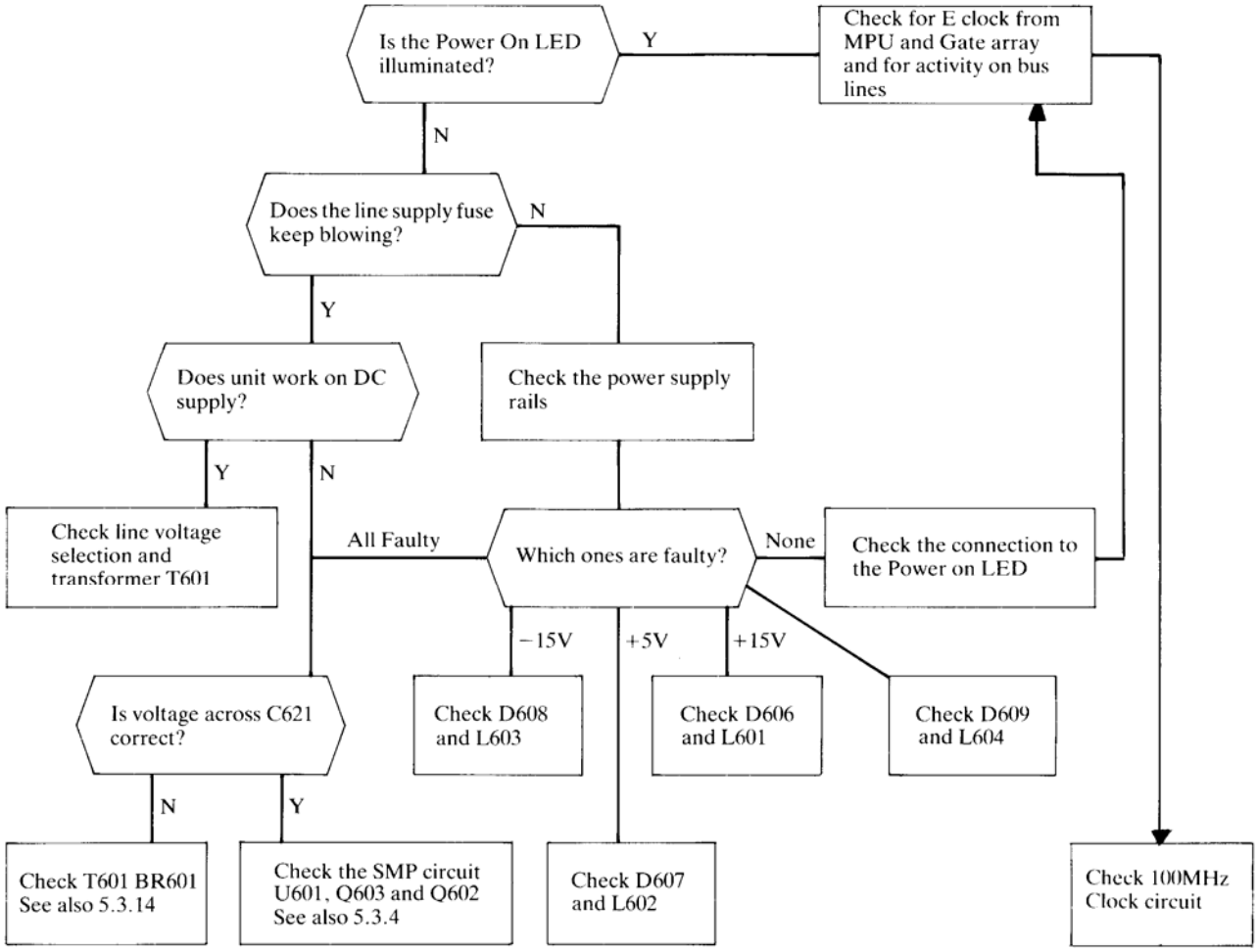
5.2.8 Front Panel LEDs Flashing

Table No.	Symptom
5.3.33	Hold All LED flashes
5.3.34	Roll LED flashes
5.3.35	X-Y LED flashes
5.3.36	Refr LED flashes

5.3 Fault Finding

5.3.1. Total System Failure

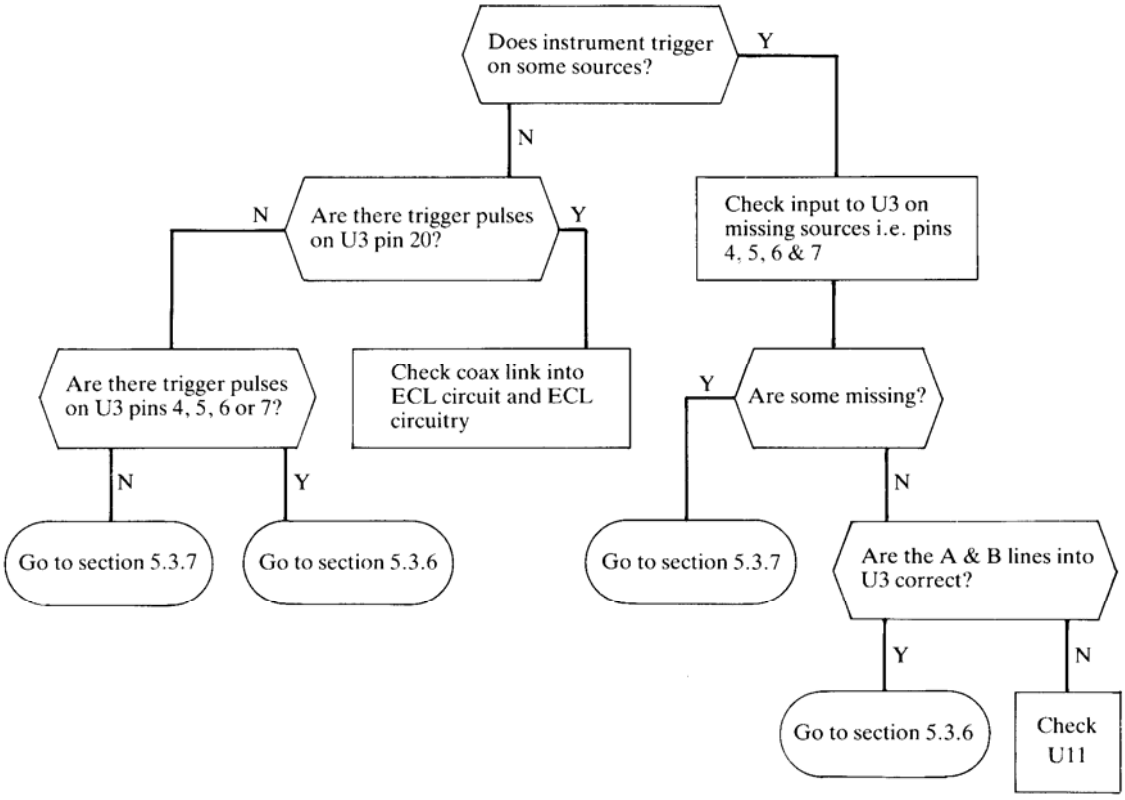
symptoms: There is no display and no front panel controls function.



5

5.3.2 Instrument Fails to Trigger

symptoms: With a suitable signal input, it is not possible to obtain a stable triggered trace.

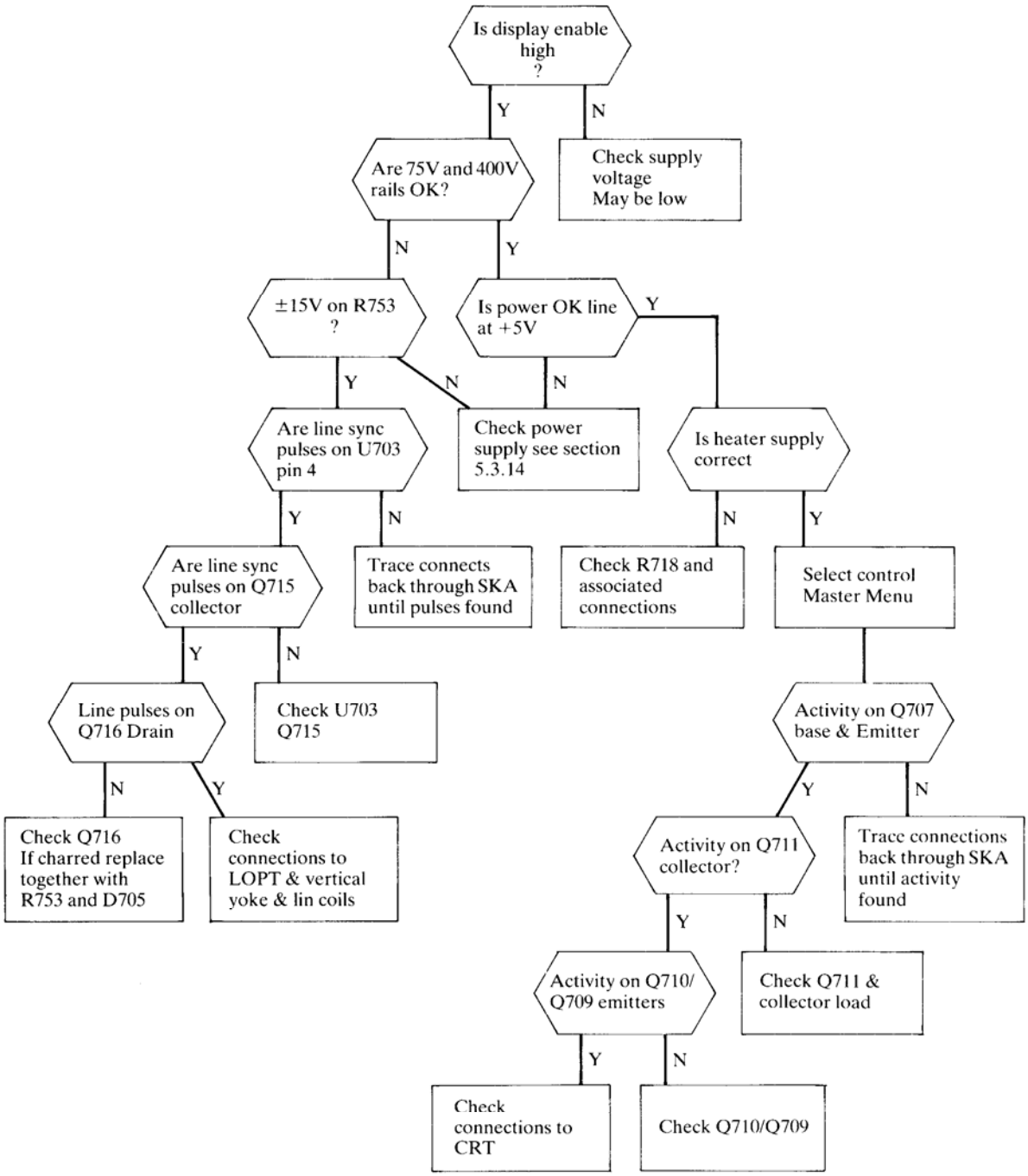


* NB line trigger is only present when the instrument is connected to AC Power

5

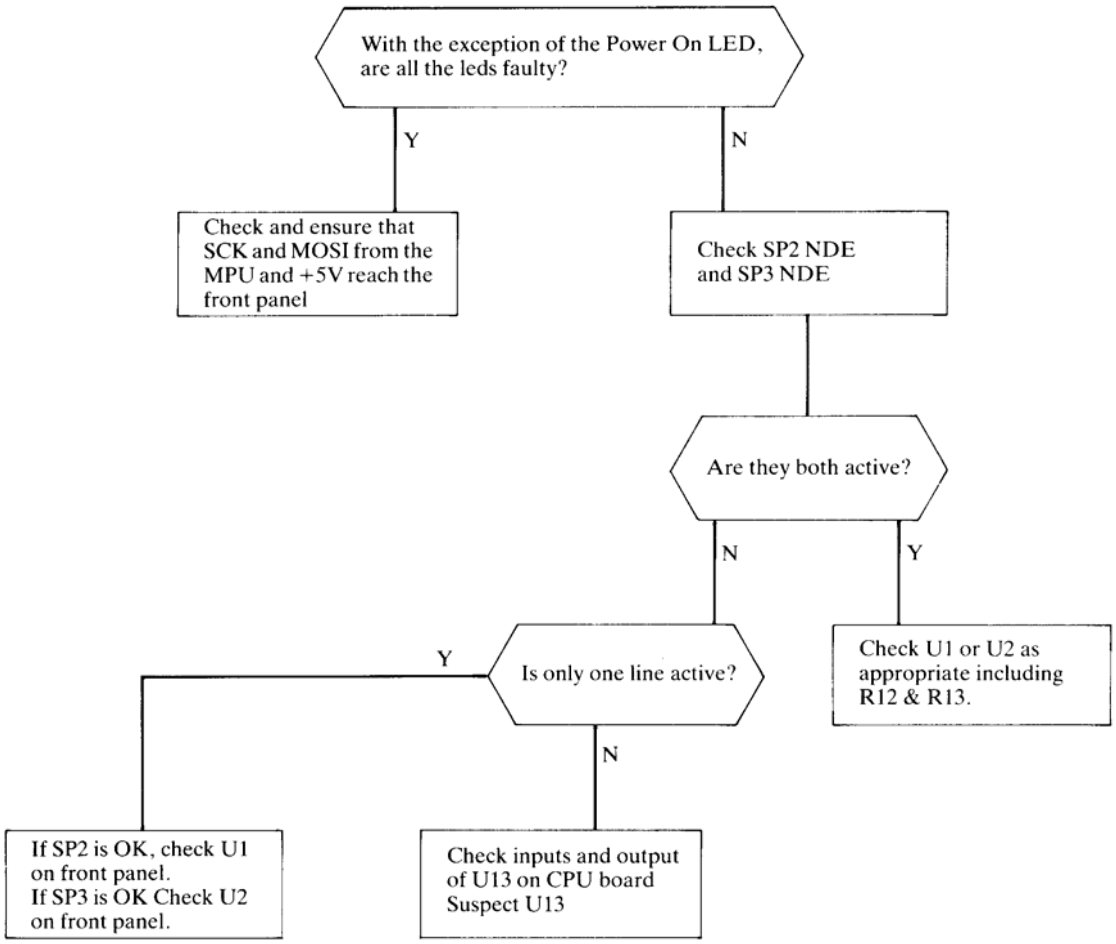
5.3.3 No CRT Display

symptoms: There is no trace, graticule or alphanumeric display on the screen. The front panel LEDs illuminate as normal.
If either R753, D705 or Q716 appear to be burnt or charred, replace all three components



5.3.4 Some or all the front panel LED's not working

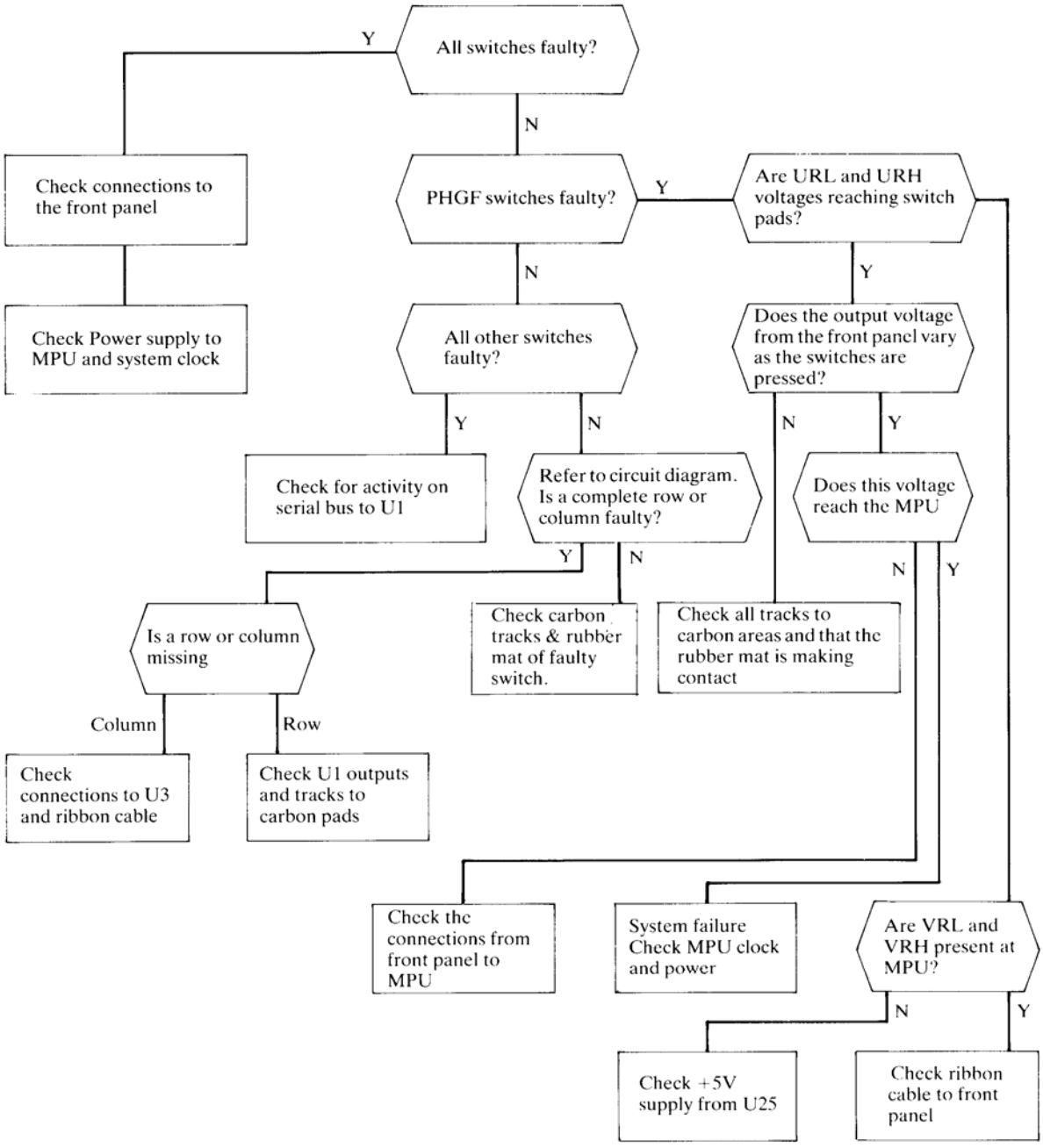
symptoms: When various functions are selected, the expected display is obtained but the front panel indications are wrong.



5

5.3.5 No Response to some or all front panel switches

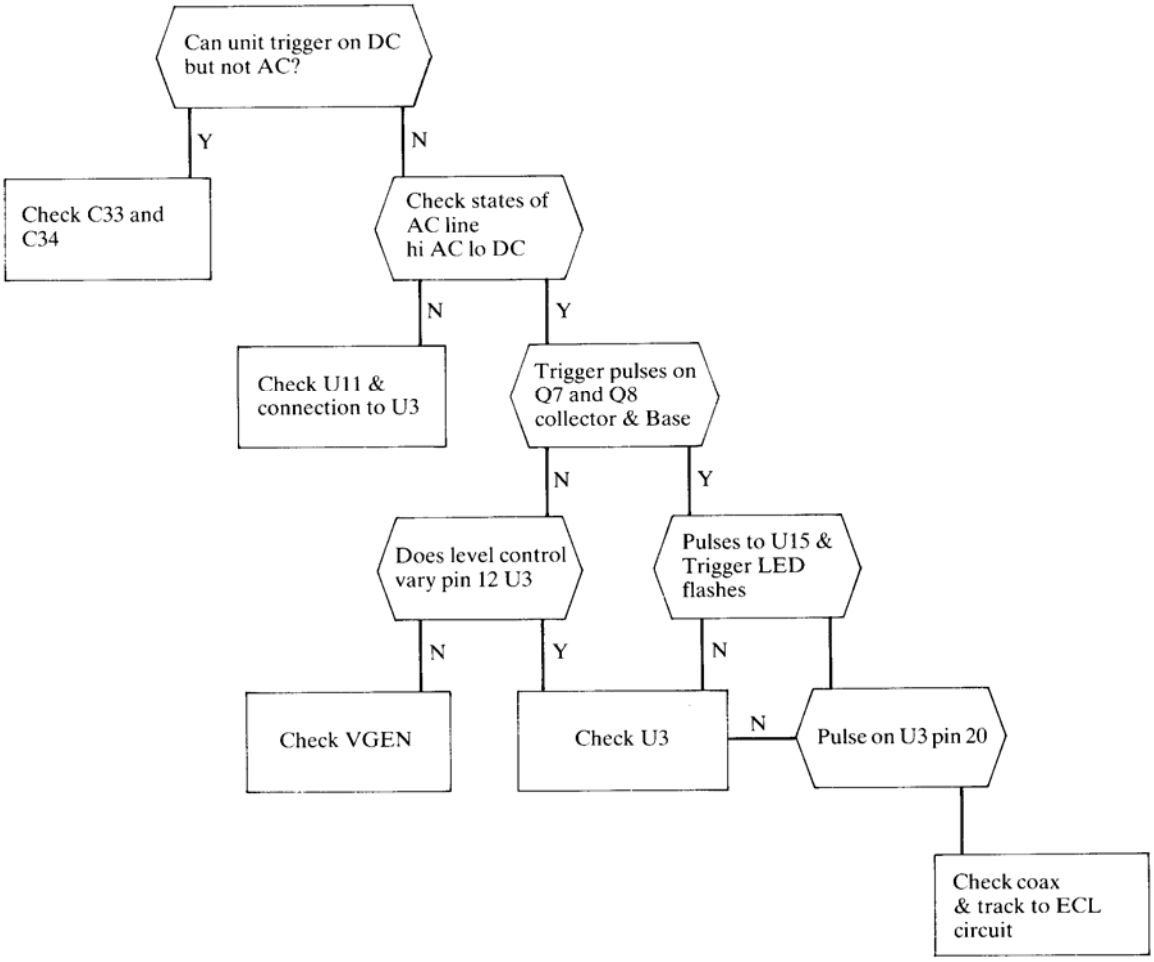
symptoms: Some or all of the front panel switches do not function as expected.



5

5.3.6 Trigger source & coupling not selectable

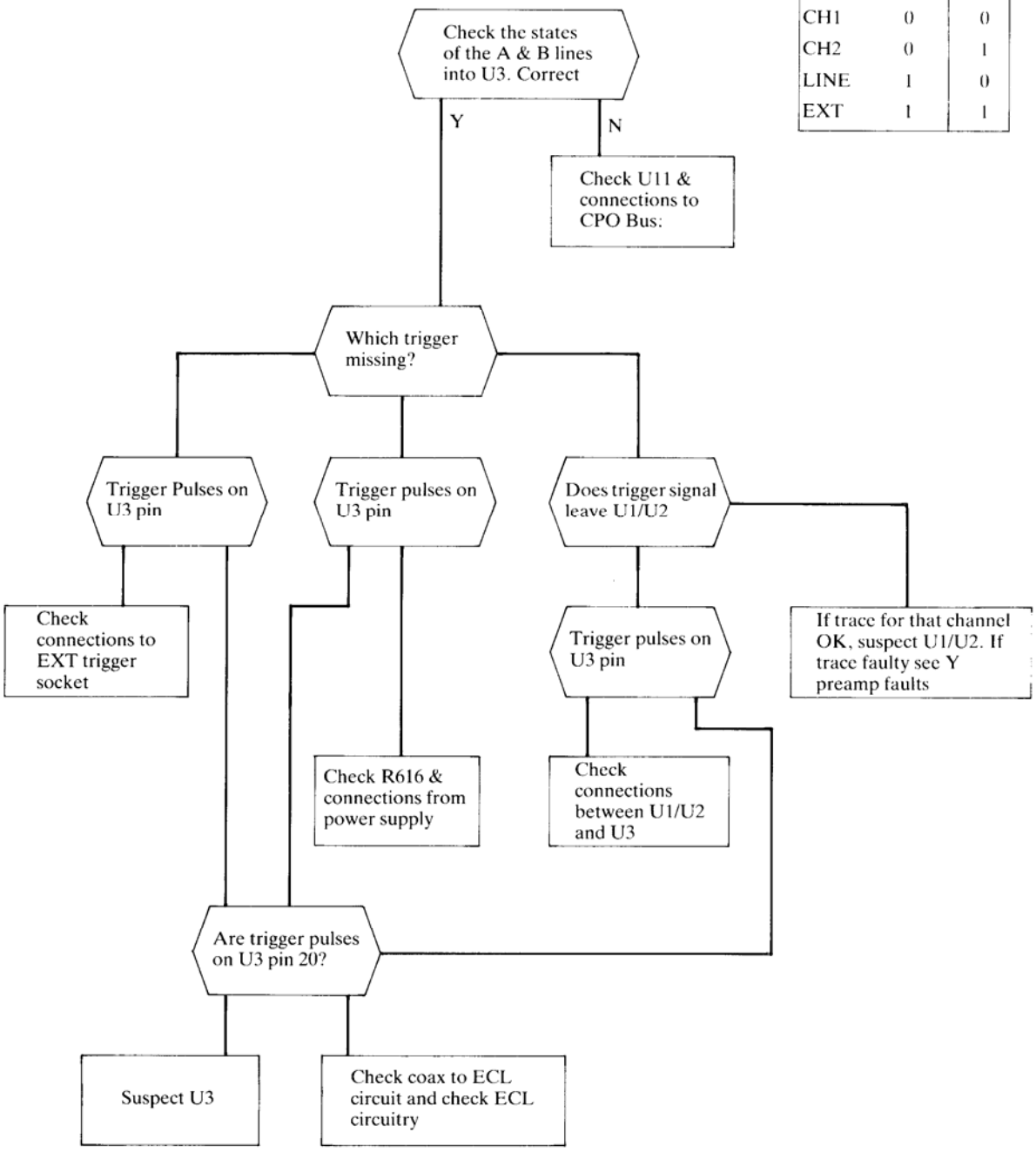
symptoms: It is not possible to select certain trigger sources or couplings



5.3.7 No External, or No Line Trigger or No channel trigger

symptoms: with a suitable trigger source connected it is not possible to obtain a stable, triggered trace from one of the trigger sources. The unit performs correctly from another trigger source

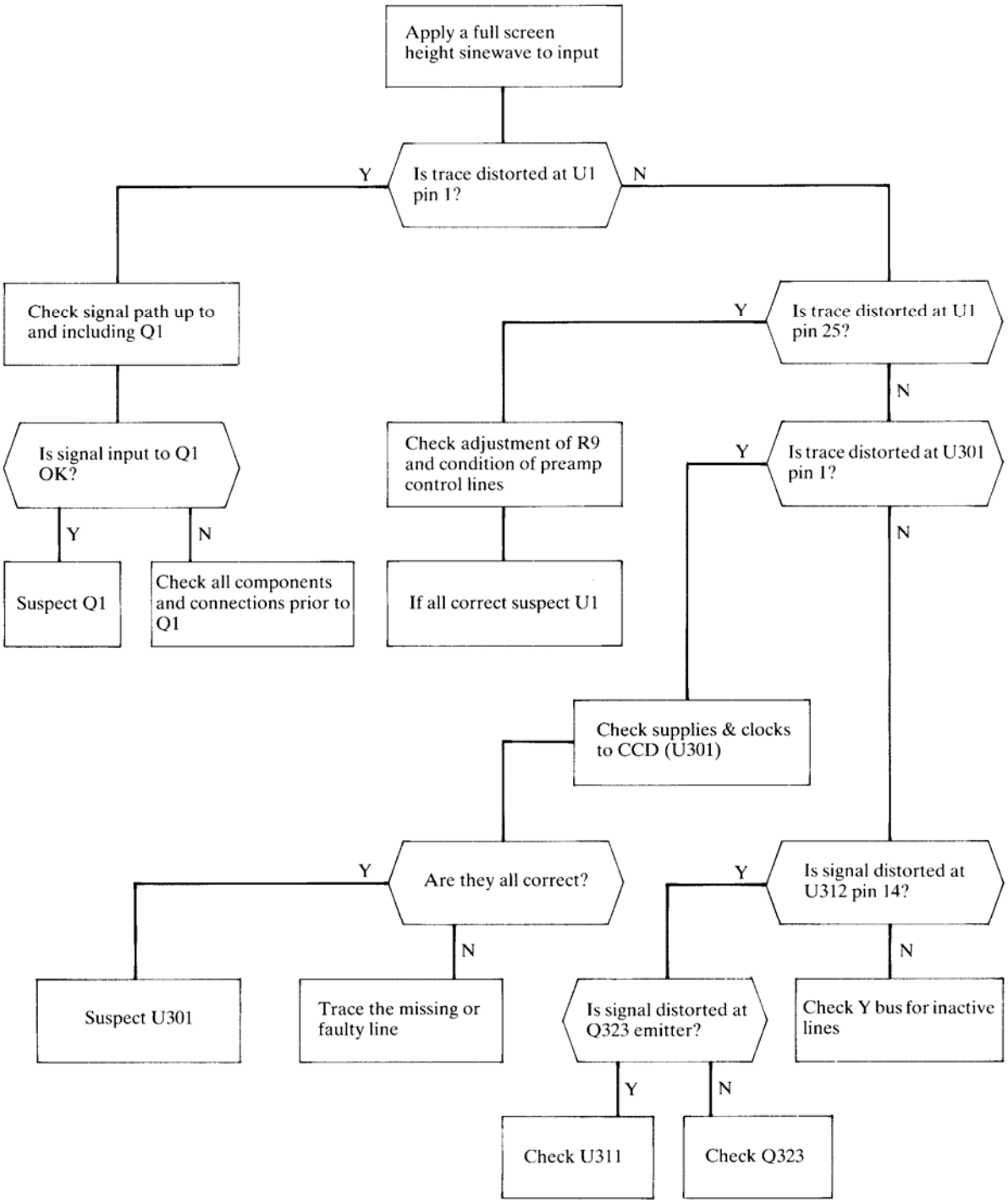
Trigger source	A	B
CH1	0	0
CH2	0	1
LINE	1	0
EXT	1	1



* NB line trigger is only present when instrument is connected to AC power.

5.3.8 Trace distorted

symptoms: The trace is not a true representation of the input signal and it does not appear any noisier than expected



5.3.9 No alphanumerics

symptoms: All traces and the graticule are displayed correctly but no alphanumerics can be seen.

If there are no alphanumerics, check first that the intensity setting from the display and intensity menu is not set to minimum, then check that the alphanumeric data signal is reaching the base of Q707 from the gate array U24. If the signal does reach Q707 check its emitter connections and D710. If the data does not leave the gate array then suspect a fault within the gate array itself, which should be replaced after ensuring that all the supplies to it are correct.

5.3.10 Memories lost on power down

symptoms: The trace memories cannot be recalled once the instrument has been switched off. Also the instrument performs a complete recalibration on power up.

The circuit is described in 5.4.26, battery backup. If data is not being held in the RAM U8 during power down, check that LK16 is still in place maintaining B1 in circuit. Check that the charging circuit, Q2 and associated discrete components, is recharging the battery. If the battery is in circuit and being charged then it is not retaining its charge and should be replaced.

5.3.11 Alphanumerics unreadable or incomprehensible

symptoms: The alphanumerics may be clear but the words unreadable or the actual characters may be unrecognisable.

This problem is caused by either the RAM or the gate array. Part of the RAM area may be faulty which may show up as fault 5.3.33, or there may be a fault within the gate array, which should be replaced after ensuring that all the supplies to it are correct.

5

5.3.12 No dot join

symptoms: When dot join is selected On from the display and trigger menu, the individual un-joined dots are still displayed.

This problem may be caused by one of the microprocessor address lines held at a fixed level preventing a control port from being written to, or it may be due to a fault within the gate array, which should be replaced after ensuring that all the supplies to it are correct.

5.3.13 No trace display in X-Y mode

symptoms: When an X-Y display is selected no trace information is displayed even though the instrument is receiving valid triggers and is armed. The graticule and alphanumerics are correct.

The X-Y signal is output by the gate array to R755 and D715 where it is summed to the rest of the display data. Check that the X-Y data is present along its path and that the data reaches both the base of Q705 and R703. If the data does not leave the gate array then suspect a fault within the gate array itself, which should be replaced after ensuring that all the supplies to it are correct.

5.3.14 The power supply unit is not functioning correctly

symptom: some or all of the internal supply voltages are missing.

This could be because the power supply has failed or because part of the rest of the unit has developed a fault and is drawing excess current thus pulling down the power supply. Carefully examine the unit for evidence of burnt or charred components and tracks.

In order to facilitate testing and fault finding of the power supply, a set of four 'solder blob pads' on the underside of the main PCB and a six way connector (PLG) have been provided. These facilities permit two modes of operation:

1. With the solder pads bridged the instrument operates normally from a mains or dc supply connected via the rear panel. The internal supply voltages may be monitored at PLG, see table 5.3.14.

2. With the solder blob switches open and power applied through the rear panel, the power supply outputs are isolated from the rest of the instrument. Their voltages can be measured on PLG. It is recommended that fixed resistors are connected to PLG to draw at least 100mA from each supply rail, however as the output voltage is slightly load dependent, the measured voltages will not necessarily be exactly as indicated on the circuit.

PLG Pin No.	Voltage
1	−15V
2	−5V
3	+5V
4	+15V
5	No Connection

Table 5.3.14 PLG Connections

If it is suspected that part of the instrument is drawing excessive current from one of the supply rails, a resistor can be soldered across the solder pads and the current deduced from the voltage across this resistor.

5.3.15 VGEN faulty

symptom: One or more of the following functions do not work, Y shift, variable gain, and trigger level, or the instrument may fail offset calibration.

Any of these symptoms could occur if one or more outputs from the VGEN sample and hold buffer amplifiers U6 and U7 are missing. These sample and holds control the functions shown in table 5.3.15

U6a	Y shift	Channel 1
U6d	Variable gain	Channel 1
U7c	Offset cal	Channel 1
U6c	Y shift	Channel 2
U7b	Variable gain	Channel 2
U6a	Offset cal	Channel 2
U7d	Trigger level	
U7a	VGEN ramp control	

Table 5.3.15 VGEN sample and hold Functions

Check that the voltage on pin 3 of U5 is a sawtooth ramp with a period of approx 4.2ms and that the count inputs on pins 9, 10 and 11 are 33ms, 16.5ms and 8.2ms square waves respectively. If the ramp is missing, check that Q15 is being switched on and is discharging C50 by the VGENRS pulse via Q14 and Q16 every 4.2ms. If all the outputs from U5 are missing, check that the outputs from U5 are being enabled by an approximately 10μs negative going pulse every 12ms.

5.3.16 No horizontal deflection

symptoms: The only trace visible is a vertical line at the left hand edge of the screen or the screen is blank.

The circuit is described in section 5.4.19, Horizontal deflection and line correction. Check for negative going 20ms sync pulses on the base of Q701 to reset the frame ramp, check that the ramp drive is present by examining the voltage across R717, ensure that all the connections to the horizontal yoke are intact and being driven by U701a.

5.3.17 No frame blanking

symptoms: The left hand edge of the screen picture is extra bright where the continuous vertical scan waits for the next frame ramp to commence.

Check that the NFSYNC pulses from the gate array are reaching D713 and thus turnging off Q711 during the flyback period. Ensure that the pulses also turn off U702 via D719 again during the flyback period.

5.3.18 Poor focusing

symptoms: The screen picture has a poor overall focus particularly in the corners of the display.

Check the 400VDC rail from D703 and C719 to R745. Check the connections from R745 to the tube base circuit board, connection A3.

5.3.19 One or more traces not displayed

symptoms: The instrument operates correctly apart from one or more traces, the cursors, alphanumerics or graticule is missing from the display.

Check first that the black level control R734 is correctly set and no selections on the display intensity menu are set to minimum. Follow the missing trace signal from the gate array, U24 on the CPU board to the diode and resistor summing network D701, D715-718, R730 and R755-758. If the data does not leave the gate array then suspect a fault within the gate array itself, which should be replaced after ensuring that all the supplies to it are correct.

5.3.20 Cramping of horizontal lines

symptoms: Some cramping of the horizontal lines occurs at the top and/or the bottom of the screen.

This fault is most likely to be caused by one of the three problems described below.

a) Cramping near the top of the screen may be due to too high a resistance in the vertical deflection current path, Q716, L701, L702, L704 etc. or not enough linearity correction from L701 which may indicate that one of its permanent magnets is damaged.

b) Cramping at the bottom of the screen may be due to too low a resistance in the vertical deflection path, Q716, L701, L702, L704 etc. or too much linearity correction from L701.

c) If the cramping is only at the extreme top and bottom of the screen, this is most likely to be due to too much S correction because C721 is faulty and has too small a value.

The above three faults can all be caused if too much geometry correction has been attempted using external magnets on the yoke assembly. See section 4.1 item 9.

5.3.21 Cramping of vertical lines

symptoms: Some cramping of the vertical lines occurs at the left and/or the right hand edges of the screen display.

This is due to the horizontal linearity correction not functioning correctly. Check the linearity circuit consisting of U701b, D711, D709, and associated discrete components. The horizontal ramp together with any S correction can be seen by examining the voltage across R717.

5.3.22 Cannot trigger from the EXT source

symptoms: The instrument triggers normally on all selections except EXT.

Check the integrity of the connections from the front panel socket to U3 pin 4. If the signal is reaching the trigger chip (U3), and all the voltages and control lines to it are correct then suspect U3.

5.3.23 HF reject not selectable or always selected

symptoms: It is not possible to trigger on high frequency signals (HF reject permantely on) or it is not possible to reject the high frequency components on the input signal to trigger on the low frequency parts (HF reject not selectable).

Check that U11 pin 31 changes state as the filter is selected. If there is no change suspect U11. If the ouput changes state, check that Q20, Q21 and Q22 are functioning correctly.

5.3.24 No control of the trigger level

symptoms: The trigger level cannot be adjusted and/or the trigger level indicator bars do not move on the display.

The VGEN circuit controls the trigger level and the microprocessor controls the indicator bars, the appropriate part of the instrument should be investigated. If other VGEN functions, vertical shift and variable gain etc. are working then suspect U7d. If none of the VGEN voltage controlled functions appear to work then see the VGEN fault guide, section 5.3.15. If the microprocessor appears to be faulty, check all its data and address lines and the supplies to it.

5.3.25 Trace off the top or bottom of the screen

symptoms: The trace is off the screen as indicated by the arrows and cannot be brought into view using the Y shift control.

Ensure that the signal has not got a large DC component. Switch the input coupling to AC to remove any DC offset from the input and ensure that C1 is actually being switched into the signal path. Check that the Y shift VGEN output is working, see fault 5.3.15. Also check that the emitter voltage of Q322 is approximately 3.5V. If not check D305, R373 and Q322.

5.3.26 Trace 'stepped'

Symptoms: A smooth continuous trace such as a sinewave appears to be mixed up and has large gaps in it. Alternatively the trace may be made of large clearly visible steps.

Note: *The traces are made up of 256 discrete Y levels and on close examination of the screen the levels can be seen. This is normal for digital storage oscilloscopes and should not be confused with the above problem.*

Apply a full screen height sinewave to an input and check that all the data lines are active on the following buses:
a) the Y bus to U312, and the gate array U24
b) the data outputs from U306, U308, and U314
c) the memory data bus to U8 and the gate array U24

5.3.27 No Y shift or variable gain

symptoms: Vertical shift and or variable gain does not function on one or both of the input channels.

This is due to a fault in the VGEN circuit. If other VGEN functions, trigger level or vertical shift and variable gain for the other input channel are working then suspect the appropriate buffer amplifier: U6b and U6d for CH1 or U6c and U7b for CH2. If none of the VGEN voltage controlled functions appear to work then see the VGEN fault guide, section 5.3.15

5.3.28 Invert not functioning

symptoms: The invert trace function is not working for either CH1 and or CH2, or if it is working there is a DC shift on the inverted trace even if the input is grounded.

If invert is not functioning at all, then examine the control line output from U11: pin 16 for CH1 and pin 13 for CH2, and check that it goes low when invert is selected. If the control line is activating correctly and reaches pin 1 of the appropriate preamplifier, suspect the preamplifier chip.

If an extra DC offset is present on CH1 or CH2 when invert is selected, check R9 or R22 and their related components as appropriate.

5.3.29 One or more of the attenuator ranges or the input coupling selections is not available.

symptoms: One or more of the attenuator ranges cannot be selected. It is possible to obtain abnormal ranges and possibly the input will be permanently AC, DC or Ground coupled.

If the attenuator read-out on the CRT does not change as the front panel controls are adjusted see fault 5.3.5

The input coupling is selected using relays - for AC RL1 is open and for DC RL1 is closed (see table 5.3.29a) - and the attenuator is controlled in two ways. Firstly through a 50:1 relay switched attenuator and secondly by three control lines into the channel preamp chip. Check first that the correct control signals for the selected range are reaching the preamp chip (see table 5.3.29b), and secondly that the attenuator relay is actuating properly - U11 outputs go low to energise the relays. If both of these are correct, the channel preamp U1/U2 maybe faulty. If the above signals are incorrect, check U11 and the associated pull up resistors N5 or N6 and the diode array N4. Check that the serial bus data and clock into U11 is present and not corrupted.

Coupling	RL1	RL2	RL3	RL4
AC	0	X	X	X
DC	1	X	X	X
GND	X	1	0	0

Table 5.3.29a Input coupling settings

1 = Energised, 0 = Not energised, X = Don't care

Range/cm	**x0.1**	**x1.25**	**x2**	**x4**	**RL4**	**RL2**	**RL3**
GND	X	X	X	X	0	1	0
2mV	0	0	1	0	0	0	1
5mV	0	1	0	1	0	0	1
10mV	0	1	1	1	0	0	1
20mV	1	0	1	0	0	0	1
50mV	1	1	0	1	0	0	1
100mV	1	1	1	1	0	0	1
200mV	0	0	0	1	1	1	0
500mV	0	1	1	1	1	1	0
1V	1	0	1	0	1	1	0
2V	1	0	0	1	1	1	0
5V	1	1	1	1	1	1	0

Table 5.3.29b Attenuator settings

X= Don't care, 1=High/Energised, 0=Low/Not energised

5.3.30 Input coupling not selectable

symptom: AC, DC or GND coupling is fixed and cannot be changed. The LEDs change as the AC/DC/GND switch is pressed. If the LEDs do not change see fault 5.3.5.

This could be caused by either C1 or R2 being faulty or because RL1 is not switching or not being switched. (C15, R15 and RL6 for CH2). Check the components for short or open circuit and ensure that the relay is being energised correctly from the output of U11.

5.3.31 No calibrator signal

symptoms: There is no 1KHz signal present on the front panel output points.

Check that the base of Q18 is receiving clock pulses from the gate array, if necessary trace the signal back. Check also the connections to the front panel sockets and that Q18, Q19 and Q17 are actually working and producing a signal.

5.3.32 No Response over RS423

Symptoms: No data or commands can be sent or received via the RS423 interface connection.

Many faults involving the RS423 interface can be traced to incorrect signal connections. Check the setting of SW1 and the interface cable. If there is no obvious error check that SW1 is mechanically sound. If the rest of the unit functions correctly then suspect U22 and U23 and their associated discrete components.

5.3.33 Symptom: Hold All LED flashes on power up

This happens due to a RAM check failure. Check that the RAM U8 is correctly plugged in and that all the data and address lines are connecting with its pins. Check that the buffers U11 and U12 are not corrupting the microprocessor address lines. If everything appears to be correct, change the RAM.

5.3.34 Symptom: Roll LED flashes on power up

This occurs when the Paged ROM is not found. Check that U4 and U3 are in firmly in their correct sockets and that the address and data lines are reaching the pins of the devices.

5.3.35 Symptom: X-Y LED flashes on power up

This is because of a Root ROM check sum failure. This may occur if one of the ROMs has been plugged into the wrong socket ie U3 into U2 socket or if there is a fault on the address or data bus to one of the ROMs

5.3.36 Symptom: Refr LED flashes on power up

This indication occurs if the paged ROM version/data does not match the root ROM. Check that ROMs have not been inadvertently swapped with different issues from another set.

5.4 CIRCUIT DESCRIPTIONS

The following sections of text describe the operation of the individual circuit blocks of the 400. The section numbers used in section 5.3, cross reference the circuits under discussion in the flowcharts with the descriptions here. To find the components on the boards see figures 6.1 - 6.4.

Index of circuit blocks

5.4.1 Input attenuator

The input attenuators N1 and N2 are identical custom resistor networks that provide a 50:1 attenuation for CH1 and CH2 respectively. This attenuation is switched on and off by relays 2, 3 and 4 for CH1, and relays 7, 8, and 9 for CH2.

Measurements

U11 pin 38	0V	range 200mV to 5V/div
U11 pin 38	+5V	range 2mV to 100mV/div
U11 pin 38	+5V	input switched to ground
U11 pin 39	+5V	range 200mV to 5V/div
U11 pin 39	0V	range 2mV to 100mV/div
U11 pin 39	+5V	input switched to ground
U11 pin 40	0V	range 200mV to 5V/div
U11 pin 40	+5V	range 2mV to 100mV
U11 pin 40	+5V	input switched to ground

5.4.2 Attenuator Relay Control

The five relays per channel are switched by the outputs from U11 the serial data decoder/driver. Each relay coil is connected to a separate output and can be individually controlled by the data on the serial bus.

Measurements

U11 pins	0V	R1 energized and contacts closed

5.4.3 Custom Preamp/Attenuator

Incoming signals to either channel 1 or channel 2 are handled identically so only channel 1 will be described here. The signal coupling is selected to be either ac or dc by the action of RL1. With RL1 open, C1 the ac coupling capacitor is in circuit and with RL1 closed C1 is by-passed. For further details on the input switching arrangements see table 5.3.29a.

Most of the signal processing is performed by U1 a semi-custom chip. The variable dc control levels for U1 come from the VGEN circuit whilst the switched control lines are driven by U11. For details of the state of the switched lines for different gains see table 5.3.29b. Q2 and Q3 are simply the pnp transistors in the gain switching stage of the preamp chip. U1 provides two outputs, one is the signal output to the CCD circuit and the other is a trigger signal which is passed to the trigger circuit (U3). The internal arrangement of U1 can be seen in Fig 6.6.2.

Measurements

VN3	−8V
VN1	−8V
VN2	−8V
VP1	+12V
VP2	+12V
VP3	+12V
VP4	+5V

5.4.4 Voltage Generator (VGEN)

The VGEN circuit produces eight voltages: 2 offset correction, 2 shift and 2 variable gain voltages for the channel preamplifiers, a trigger level control voltage and a reference control voltage.

All 8 voltages are generated from a linear ramp by sampling the ramp through a 1 of 8 multiplexer, U5, with individual sample and holds, U6, U7 and C40 - C47, at times determined by an internal timer/counter in the microprocessor U1 (CPU Board).

The ramp itself is generated by U9c and C50 and reset by Q15 which is driven by Q14 and Q16 from a high going pulse on the VGENRS line. The reference control voltage is compared with the unit's fixed -8V reference by U9d and fed back to the linear ramp generator U9c, thus fixing the calibration of all the VGEN outputs. The appropriate output is selected by the control lines VGEN0,1 and 2, when the multiplex inhibit line is taken low by VGENSP.

Measurements

U5 pin 11	squarewave 8ms 5V pk-pk	
U5 pin 10	squarewave 16ms 5V pk-pk	
U5 pin 9	squarewave 32ms 5V pk-pk	
U6b pin 8	0V	trace off top of screen
U6b pin 8	−4V	trace mid screen
U6b pin 8	−8V	trace off bottom of screen
U6d pin 14	0V	variable gain X1
U6d pin 14	−7V	variable gain X0.4
U7c pin 7	−4V	typically
U7d pin 8	0V	trigger level maximum below trace
U7d pin 8	−4V	trigger level mid trace
U7d pin 8	−8V	trigger level maximum above trace
U7a pin 1	−8V	

5.4.5 -8V Reference Voltage Generator

The -8V reference voltage is generated by U9b,D13 and D14, and is set by R61. This voltage can be measured on TP1.

Measurements

U9b pin 5	−6.2V	typically
U9b pin 6	−6.2V	typically
U9b pin 7	−8V	

5.4.6 Probe Calibrator

The 1V 1kHz probe calibration signal is created by U9a, Q17, Q18 and Q19. The output level is set by R56 from the -8V reference voltage and the frequency is controlled by the CAL output from the gate array U24 (CPU Board).

Measurements

U9a pin 2	0V	
Q18 base	squarewave	1 kHz 3V pk-pk on 2V pedestal
U9a pin 1	+4V	

5.4.7 CCD and Supplies

The CCD, U301 obtains its 14.5V power supply and 2.2V bias from a local power supply derived from the +15V rail by U304, Q324 and the associated discrete components. The 14.5V is set by R364 and can be monitored on TP4, and the bias voltage is simply divided from this rail by R366 and R367. All the other supplies to the CCD are decoupled locally

Measurements

U301 pin 4, 12 and 34	−5.6V	typically
U301 pin 24	+0.5V	typically
U301 pin 21	+0.5V	typically
U301 pin 25	+1.8V	typically
U301 pins 2, 3 and 20	+14.5V	

5.4.8 CCD Drivers

The four phase clocks to the CCD are driven by two, two phase clock drivers. Their operation is identical so only one is described here. The clocks from the preceding ECL circuit are differentially terminated by U305b. The resistor, capacitor and inductor network at the front end allows adjustment of the differential delay and termination of FA and FB. The ECL output from U305b drives the differential pair Q301 and Q302, the current source for which is Q303. U302 in conjunction with R310, R309, R308 and R322 compares the average level of the output waveform with half the value of the required output clock pulse amplitude. Feedback to the current source Q303 corrects the output swing, thus removing any drift from this circuit block.

The complimentary followers Q304, Q327 and Q308, Q328 buffer the collector outputs of Q301 and Q302 respectively and directly drive the CCD sample clocks ØAS, ØBS, ØES and ØFS. Resistors R316 and R328 introduce a small delay to the sample clocks before feeding them, as the transport clocks, to ØAT, ØBT, ØET and ØFT.

Measurements

U305b pin 2	pulses 1V pk-pk on −1V pedestal. Period dependent on timebase
U305b pin 3	pulses 1V pk-pk on −1V pedestal. Period dependent on timebase
Q315 emitter	pulses 12V pk-pk period dependent on timebase

5.4.9 CCD Correction

DAC's U307, U309,and U314 are used for offset, gain, and gain offset correction respectively. Data words from RAM are latched from the YBUS on the leading and trailing edges of the COFFSET pulses by U308 and U306. Current from U307 is summed with the CCD output related current at the junction of R376, R396, and R391, thus providing offset correction.

For the gain correction, the CCD output signal varies the VREF input to U309. U309 multiplies the latched digital word, from U308, by its VREF input producing an output which is dependent on the CCD output, which when summed with the CCD output by U311, acts as a gain correction.

The gain correction process produces an offset which needs to be removed and this is achieved by U314 which functions in the same way as U307.

The output of U311 (pin 6) feeds the ADC input (U312 pin 14).

Measurements

U311 pin 3	3V
Q323 base	Multiplexed signal of trace 1 and 2 DC level typically 3V with traces at centre of screen
U311 pin 6	multiplexed signal of trace 1 and 2 0V equivalent to centre of screen

5.4.10 Vertical ADC

The ADC (U312) is a full flash converter driven by the ADCCLK line and enabled onto the YBUS by ADCOE. Voltage regulators U310 and U313 provide U312 with the ADC reference voltages.

Measurements

U310 pin 2	+1.2V
U313 pin 2	−1.2V
U312 pin 18	Clock pulses 5V pk-pk

5.4.11 100MHz Oscillator

The basic timing reference within the 400 is a 100MHz oscillator built around U501c and XL501. U501b buffers the clock signal to the fast timebase generator circuit. The MPU can 'Kick' the oscillator and introduce a phase offset via C525 which is in turn kicked from the serial bus via U11 on the preamp and trigger circuit. This prevents absolute phase locking between sampling edges and an external signal on ETS ranges.

Measurements

U501b pin 3	100MHz Clock

5.4.12 Fast Timebase Generator

The fast timebase can be any of six frequencies and is derived from the 100MHz clock as follows: D Type flip flops U502b, U502a and U503b form a divide by 5 counter, which is followed by U503a, a divide by two stage, the output of which is therefore 10MHz. Either this signal or the basic 100MHz then passes through a 1 of 2 Multiplexer - formed by U504c and U504d and controlled by FTB1 through a TTL to ECL level translator U509c. U505a and U505b are further divide by two stages whose outputs together with the earlier 1 of 2 multiplexer's 10/100MHz output, are selected by a 1 of 3 multiplexer consisting of U507c, U504a and U504b. FTB2 and FTB3 via U509a and U509b control the selection in this final stage. The resulting fast timebase clock may be monitored on TP2. The control signals required for various clock frequencies are shown in table 5.4.12.

Timebase	FTB3	FTB2	FTB1	FTB CLK
500ns	1	0	0	100MHz
1μs	0	0	0	50MHz
2μs	0	1	0	25MHz
5μs	1	0	1	10MHz
10μs	0	0	1	5MHz
20μs	0	1	1	2.5MHz

Table 5.4.12 FTB control settings

Measurements

U501b pin 3	100MHz
U503b pin 15	20MHz
U503a pin 2	10MHz
U504c pin 14 and U504d pin 15	10 or 100MHz selected by FTB1
U505a pin 3	5 or 50MHz selected by FTB1
U505b pin 14	2.5 or 25MHz selected by FTB1
TP2	2.5, 5, 10, 25, 50 or 100MHz selected by FTB1, FTB2 and FTB3. See table 5.4.12.

5.4.13 Trigger Sync

The asynchronous trigger signal from the trigger circuit U3, passes through three D-Type flip flops. First it is latched in U517a, then it is synchronised to the timebase by U517b. Finally, U510a produces a trigger signal synchronised to the timebase, delayed by two timebase periods.

Measurements

U517a pin 3	+ve edge on trigger
U517b pin 15	+ve edge on timebase clock
U510a pin 3	+ve edge sync'd to timebase clock

5.4.14 ETS

The ETS circuit produces a ramp whose final level is a measure of the time difference between a trigger and the next timebase clock. Q501, Q502 and C526 form a fast ramp generator which starts, stops and resets under the control of U514a and U516c. The ramp is started by the latched trigger signal from U517a and stopped by the synchronised trigger output from U517b on the next timebase clock.

Measurements

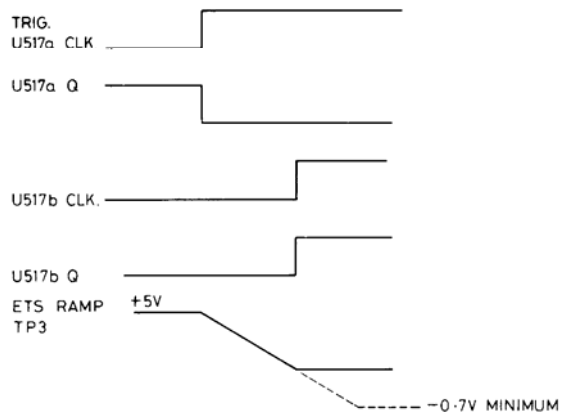


Fig. 5.4.14 ETS ramp generation

5.4.15 Acquisition Control and CCD Clock Select

The CCD clock frequency is either 1Mhz or the fast timebase depending on the output from a 1 of 2 multiplexer U507a and U507b which is switched by U509d from the CA line. The rate is dependent on the time per division selected; slower than 50μs/div uses a CCD clock of 1MHz.

Measurements

U507b pin 7	logic 0	Timebase 50s to 50μs/div
U507b pin 7	logic 1	Timebase 20μs to 0.1μs/div
U519d pin 15	1MHz clock	Timebase 50s to 50μs/div
U519d pin 15	see FTB	Timebase 20μs to 0.1μs/div
U519d pin 12	logic 1	Timebase 50s to 50μs/div

5.4.16 Post Trigger Counter and Selection

The post trigger counter stages U511 and U512a are really only the 3 least significant bits of a 16 bit descending counter whose other 13 bits are contained within the gate array. U511b is enabled by the wired OR consisting of U515a, U515c, U515d, and U510a preventing it from counting unless acquisition has been triggered, the appropriate clock is present and the higher bits of the counter have reached zero. U516b detects an all zero condition from the counter and enables U510b thus turning on the 4 phase generator as long as a valid trigger is latched on the output of U517b and the post trigger carry line from the gate array is low.

Measurements

U516b pin 7	negative going pulse 5μs wide 20ms period Timebase 0.2ms/div

5.4.17 4 Phase Clock Generator

The four phase clocks for the CCD are generated by a Johnson counter U506a and U506b from the CCD clock.

Measurements

U506b pin 15	250KHz clock phase A	Timebase 50s to 50μs/div
U506b pin 14	250KHz clock phase B	Timebase 50s to 50μs/div
U506a pin 2	250KHz clock phase C	Timebase 50s to 50μs/div
U506a pin 3	250KHz clock phase D	Timebase 50s to 50μs/div

5.4.18 Power Supply

Mains power applied to the instrument is filtered by the input connector's built in filter. The mains voltage series/parallel switching also occurs at the input connector. Transformer T601 transforms the mains input to 24Vac, then BR601 and C621 rectify and smooth this to about 26V dc. C621 removes most of the ripple from the DC side of BR601. Prior to BR601 the ac voltage is fed to the trigger chip U3, as the line trigger input, and also to the CPU board as SPSYNC. The regulation of the power supply is performed by U601 a switched mode controller whose sense line monitors the output current via the voltage across the source resistor from Q602. If the sense line rises above 1V, the controller shuts off the output. The soft start circuit raises the sense line above 1V, thus forcing the output to turn off, and then gradually lowers the sense voltage to slowly increase the output.

Measurements

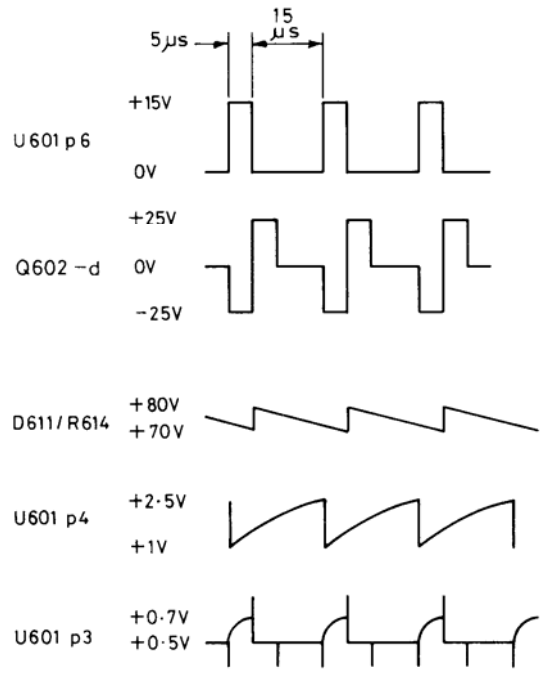


Fig. 5.4.18 Typical Power Supply Waveforms

5.4.19 Video Horizontal Deflection and Line Correction

U701b and C706 form part of a ramp generator. R708 and R709 determine the charging current through C706, however not all the current through the above resistors comes from C706, some is supplied via R701 and R702.

When the right hand end of C706 (PLD5) is positive, U701b pin 3 sinks current through D711, and R702 has 0V at both its ends. Together with R701 and C706 this results in a curved RC ramp being generated instead of the more usual linear ramp from a simple integrator.

When the right hand end of C706 is negative, U701b switches diodes D709 and D711 off and acts as an inverting amplifier with a gain of -2. The gain is set by R712 and R713. Twice the current flows through R702 as can flow in R701. Half the current flows through R701, the other half causes an RC bend to be given to the ramp, but in the opposite direction to the bend caused by R701 when C706 was positive.

The overall result of this circuit is that the current through the horizontal yoke L704a has a slightly 'S' shaped waveform which can be seen by monitoring the voltage across R717. The ramp is reset by Q712 which in turn is switched by Q701 driven from NFSYNC. Capacitor C706 is not reset to 0V, but the maximum negative ramp voltage. When Q712 is on, the voltage on C706 must be negative in order to force the voltage at the junction of R707 and R710 to be 0V. The amplitude and starting level of the ramp are set by R709 and R706 respectively. The horizontal yoke L704a is driven by the power Op-amp U701a, pin 8 of which is a virtual earth, as is U701b pin 5.

Measurements

C702	negative going pulse 4ms wide 5V pk-pk every 20ms
U701a pin8	positive going pulse 0.2ms wide 0.5V pk-pk every 20ms
U701a pin 1	positive going 20ms linear ramp 6V pk-pk centered about 0V First 4ms flat with 15V negative pulse at start
R717	positive going 20ms linear ramp 2V pk-pk centered about 0V first 4ms flat
U701b pin 3	negative going 20ms linear ramp 3V pk-pk and last 7ms flat

5.4.20 Video Vertical Deflection

The vertical defection circuit used in the 400 is a standard television tuned flyback system. T701 the line output transformer (LOPT) is really a tapped inductor which stores and then later releases energy. C722 filters a boost voltage generated during the forward conduction of D705. Two simple halfwave rectifier circuits driven from the flyback pulse generate the required 75V and 400V; D704 and C720 produce 75V whilst D703 and C719 produce 400V. The 8kV EHT voltage comes from a voltage doubler fed from an overwind on the LOPT. Line sync pulses LSYNC from the gate array are delayed by U703 to fix the position of the video relative to the raster, then so long as the display enable line from U702 pin 14 into U703b pin 13 is high, the sync pulses turn on Q715 which then turns on FET Q716 sinking current from +15V through part of T701's primary winding to ground.

When Q716 turns off, its drain voltage rapidly rises to about 350V. C718 and the vertical coils L701, L702 and L704b tune the pulse at this point so that it becomes relatively flat topped and 5µS wide for efficient rectification. The body diode of Q716 catches the pulse as it swings negative and clamps the drain to just below 0V.

The flyback pulse causes the scan current in L701, L702 and L704b to reverse thereby forcing the sweep to retrace from the top to the bottom of the CRT. C721 is the S correction capacitor which supplies a sinusoidal current phased such that the resultant sweep current waveform is slightly S shaped to compensate for the geometric distortion caused by the flat CRT screen.

When the instrument is first switched on, the soft start circuit Q702, R763 and C714, controlled by NRS pulses reduces the width of the output from U703b which reduces the time that Q716 is on and thus the current drawn, so that when the instrument is powered by a DC power supply, the peak start-up current is substantially reduced.

Measurements

Q702 base	+5V rises from 0V at switch on
R670	positive going pulse 5V pk-pk 6μs wide every 32μs
U703b pin 10	positive going pulse 5V pk-pk 6μs wide every 32μs
Q715 collector	positive going exponential ramp 12V pk-pk
Q716 drain	positive going pulse 325V pk-pk 20μs wide every 32μs
PLD1	positive going pulse 230V pk-pk 20μs wide every 32μs

5.4.21 Video and Brightness Control

The video signals on the 400 are strings of pulses which cause dots to be illuminated on the CRT. Alphanumerics (NALPHA), the Graticule (NSCALE), X-Y (NXY), Traces 1, 2 and 3 (NTRACE1,2 and 3) and the cursor (NCURSOR) are all individual negative logic digital video signals. All the traces, X-Y and the cursor are digitally OR'd through diodes D701 and D715-D718 to drive the base of Q705. NALPHA and NSCALE directly drive the bases of Q707 and Q706 respectively. These three transistors are all emitter followers whose emitter current is set by the parallel combination of their emitter resistors (e.g. R720-R722 for Q705); the lower the total resistance the greater the current. The emitter resistors are switched in and out of circuit by U702 which is driven from the CPU board.

The emitters are OR'd by D702, D708 and D710 and then via R703 are resistively OR'd with the video signals from R730 and R755-R758 to the emitter of Q711. As more signals become low, more current is diverted from Q711 emitter. The more current drawn from Q711 the brighter the display becomes.

The minimum brightness of the display is set by adjusting the most positive voltage possible with R734 (Black Level). The amplitude of the video signal from that point is set by R735 (Brightness). From the collector of Q711, Q709 and Q710 form a complimentary emitter follower providing a low impedance video drive to the CRT.

The display is blanked by either the NFSYNC pulse through D713 during the field flyback period, or by the POWER OK line being low. Both events cause Q711 to turn off.

Measurements

U702 pins 2, 3 and 4	0V or +5V dependent on brightness setting of graticule
U702 pins 6, 7 and 8	0V or +5V dependent on brightness setting of alphanumerics
U702 pin 18, 19 and 20	0V or +5V dependent on brightness setting of traces and cursor
D713/D719	negative going pulses 5V pk-pk 4ms wide every 20ms
Q705 base	negative going blanked trace and cursor signal 5V pk-pk
Q706 base	negative going blanked graticule 5V pk-pk
Q707 base	negative going blanked alphanumeric signal 5V pk-pk
PLC pin 5	negative going video signal 20V pk-pk on +40V pedestal

5.4.22 Front Panel Switches

All the front panel switches with the exception of the power on/off switch, are made up from a rubber mat with carbon inserts and the front panel PCB with carbon areas screened onto it. There are three kinds of these composite switches: simple single action switches and two kinds of 'push harder go faster' (PHGF) switches.

The single action switches consist of interleaving fingers of carbon on the PCB that are bridged by carbon pads on the rubber mat.

One PHGF switch type has two positions whilst the other is continuously variable. Both PHGF switch types have a carbon dome on the rubber mat that distorts and makes contact over a greater area on the PCB as it is pushed harder.

The PCB carbon area for the two position type consists of two pairs of fingers, the first of which are bridged as soon as the switch is operated and the second pair are bridged when the switch is pressed harder. For the continuously variable PHGF switch, the PCB carbon area is a square whose resistance is paralleled with the carbon dome; the harder the dome is pressed and flattened on to the carbon square, the lower the total resistance.

The variable PHGF switches are used in pairs to produce a voltage at their mid point that varies as either of the pair is pressed, in proportion to the hardness of the press. The voltage output is read by the microprocessor U1 on the CPU board.

The other switches are at the intersections of a grid whose columns are latched onto the memory data bus by U18 on the CPU board. This data is examined every 4ms and when a change is detected, the rows are pulsed from U1 on the front panel to determine the active intersection i.e. the switch that is being pressed.

Measurements

Key Row	positive going 5V pulse 0.5ms wide when a key is pressed	
Analog signals	+2V	no PHGF switch pressed
Analog signals	+3V	appropriate 'up' PHGF switch pressed
Analog signals	+1V	appropriate 'down' PHGP switch pressed

5.4.23 Front Panel LEDs

The front panel LEDs are driven by the two drivers, U1 and U2 which are controlled by the microprocessor. The serial data input is latched and held by the drivers. See table 5.4.23. The brightness of the LEDs connected to U1 may be varied by adjusting R12, similarly R13 varies U2's LEDs.

LED No.	Function	Device -Pin No.	LED No.	Function	Device -Pin No.
D1	Pos	U1-11	D21	CH2 Uncal	U1-26
D2	Mag	U1-25	D22	CH2 AC	U2-18
D3	Datum	U1-18	D23	CH2 DC	U2-19
D4	-------	--	D24	CH2 Gnd	U2-20
D5	Power On	+5V	D25	CH2 Off	U2-3
D6	Refresh	U1-37	D26	CH2 On	U2-2
D7	Roll	U1-36	D27	CH2 Inv	U2-1
D8	X-Y	U1-35	D28	Triggered	Q9
D9	Armed	U1-34	D29	Trigger Normal	U1-13
D10	Stored	U1-33	D30	Trigger Auto	U1-30
D11	Hold All	U1-38	D31	Trigger Slope +	U1-28
D12	Hold CH1	U1-39	D32	Trigger Slope −	U1-31
D13	Hold CH2	U1-40	D33	Trigger Reject	U1-27
D14	CH1 Uncal	U1-16	D34	Trigger AC	U1-29
D15	CH1 AC	U2-14	D35	Trigger DC	U1-2
D16	CH1 DC	U2-16	D36	Trigger CH1	U1-15
D17	CH1 Gnd	U2-17	D37	Trigger CH2	U1-14
D18	CH1 Off	U2-8	D38	Trigger Ext	U1-12
D19	CH1 On	U2-7	D39	Trigger Line	U1-3
D20	CH1 Inv	U2-6	D40	Trigger HF	U1-24

Table 5.4.23 LED Functions

Measurements

U1 LED Drives	+3V	Typically with LED Off
U1 LED Drives	+1.5V	Typically with LED On
U1 pin 19	+4V	Typically

5.4.24 MPU

The MPU U1 is an 8 bit microcomputer with on-chip peripherals consisting of an 8 channel 8 bit ADC, an asynchronous serial interface, a synchronous 3 wire interface, a free running 16 bit timer system offering input capture and output compare lines, real time interrupt, an 8 bit pulse accumulator to count external events or measure time periods, and a monitoring system to protect against software failures, loss of system clock and illegal op codes. The MPU runs the system software, monitors the PHGF switches and the value of the ETS ramp via its ADC, and controls the RS423 interface.

Measurements

U1 pin 52 4.1V typically
Data, address and control lines to U1 are all 0 to 5V signals

5.4.25 MPU Clock and Phase Lock Loop

The MPU acts as slave to the gate array and as such it has to track the gate array timing. The phase lock circuitry, U17 and associated discrete components, phase locks the E clock from the MPU to the E clock generated by the gate array, by using any difference in timing to correct the MPU's 8MHz clock. Resistors R39-44 limit the clock level to below the supply voltage.

Measurements

U17 pin 4	8MHz squarewave
U17 pin 14	2MHz clock
U17 pin 3	2MHz squarewave

5.4.26 Battery Back Up

Power to the internal RAM U8 is supplied in one of two ways. During normal operation of the instrument, +5V is applied via Q2. During power down, B1 takes on the task of maintaining the supply to the RAM via D5. The battery is trickle charged from the +5V rail through Q2 and R34. Any interruption to the power supply is detected on the PWROK line which forces an NMI to the MPU which in turn sends out a pulse to Q1 which disables the RAM putting it in its standby mode thus preventing corrupted data to be written to it, and also turns on Q3, discharging C31. Once the supply has fallen below the battery voltage, B1 begins to supply current to the RAM.

When power is restored, the reset line to the gate array is held low by U21a and U21d until the voltage on C31 crosses the threshold of the input to U21a.

Measurements

Q2 emitter	+4.6V	Power on
Q2 emitter	+4.0V	Power off
Q3 collector	0V	Power off
Q3 collector	+4V	rises from 0V in approximately 2 secs when instrument switched on
Q1 collector	+4V	Power off
Q1 collector	0V	falls from +4V approximately 1 sec after switch on

PS3	PS2	PS1	PS0	U2/CS	U3/CS	U4/CS	ROMA14	ROMA15	Page
0	0	0	0	0	1	1	1	1	B
0	0	0	1	0	1	1	0	1	A
0	0	1	0	0	1	1	1	0	9
0	0	1	1	0	1	1	0	0	8
0	1	0	0	1	0	1	1	1	3
0	1	0	1	1	0	1	0	1	2
0	1	1	0	1	0	1	1	0	1
0	1	1	1	1	0	1	0	0	7
1	0	0	0	1	1	0	1	1	Root
1	0	0	1	1	1	0	0	1	6
1	0	1	0	1	1	0	1	0	5
1	0	1	1	1	1	0	0	0	4
X	X	X	X	1	1	0	1	1	Root

Table 5.4.27 Memory Page Selection

5.4.27 Memory (ROM and RAM)

The CPU board contains the instruments memory which consists of 128k bytes of ROM and 32k bytes of RAM. U2, U3, and U4, are ROMs containing the system software and U8 is a RAM which holds all variable data, i.e. the three trace memories, the control set up and the internal calibration data. The MPU only has access to the RAM during phases 0 and 5 of the 10 phase system when the gate array turns on the MPU's tri-state address buffers whilst disabling its own address buffers. All data to and from the RAM goes via the gate array.

The ROMs reside in the upper 32k of the microprocessor address space. The Root ROM occupies the address range C000-FFFF hex (16k), while the Paged ROM occupies the address range 8000-BFFF (16k) with the page port determining which page is selected. See table 5.4.27

5.4.28 Gate Array

U24 is a CMOS gate array containing 10496 gates of which 90% are used. It contains three main areas that handle acquisition timing, memory management and display functions. It operates on a 10 phase system, where each phase controls a certain task, e.g. all microprocessor communications to the RAM and external ports are handled by the gate array during phases 0 and 5. See figure 5.4.28a.

The acquisition controller contains a timebase generator, facilities to provide pre and post trigger, digital add, max-min, an interrupt controller, and a 1kHz generator for the front panel calibration signal. For further details of the acquisition timing see figures 5.4.28b and 5.4.28c.

The memory controller contains an address generator, co-ordinates the RAM read and write cycles, controls the direct memory access and has control of the operation of the various blocks within the gate array.

The display controller contains the XY, alphanumeric, graticule, cursor, and trace generators.

5.4.29 RS423 Serial Interface

The RS423 output is controlled by the MPU U1 and will also work as an RS232 interface using a limited number of handshake lines. It can be configured as either Data Terminal Equipment (DTE) or Data Communication Equipment (DCE) according to the settings of SW1, see table 5.4.29 below and the operators manual for further details.

Measurements

U22 pin 22	±4V data	Instrument plotting No load connected
U22 pin 7	+5V	Instrument plotting No load connected

Pin No.	SW1 No.	Signal	DTE Direction	Switch Setting	Signal	DCE Direction	Switch Setting
2	A	RX	Input	1 to 2 (up)	TX	Output	2 to 3 (down)
3	B	TX	Output	4 to 5 (up)	RX	Input	5 to 6 (down)
4	C	RTS	Output	11 to 12 (down)	CTS	Input	10 to 11 (up)
5	D	CTS	Input	8 to 9 (down)	RTS	Output	7 to 8 (up)

Table 5.4.29 RS423 Connections

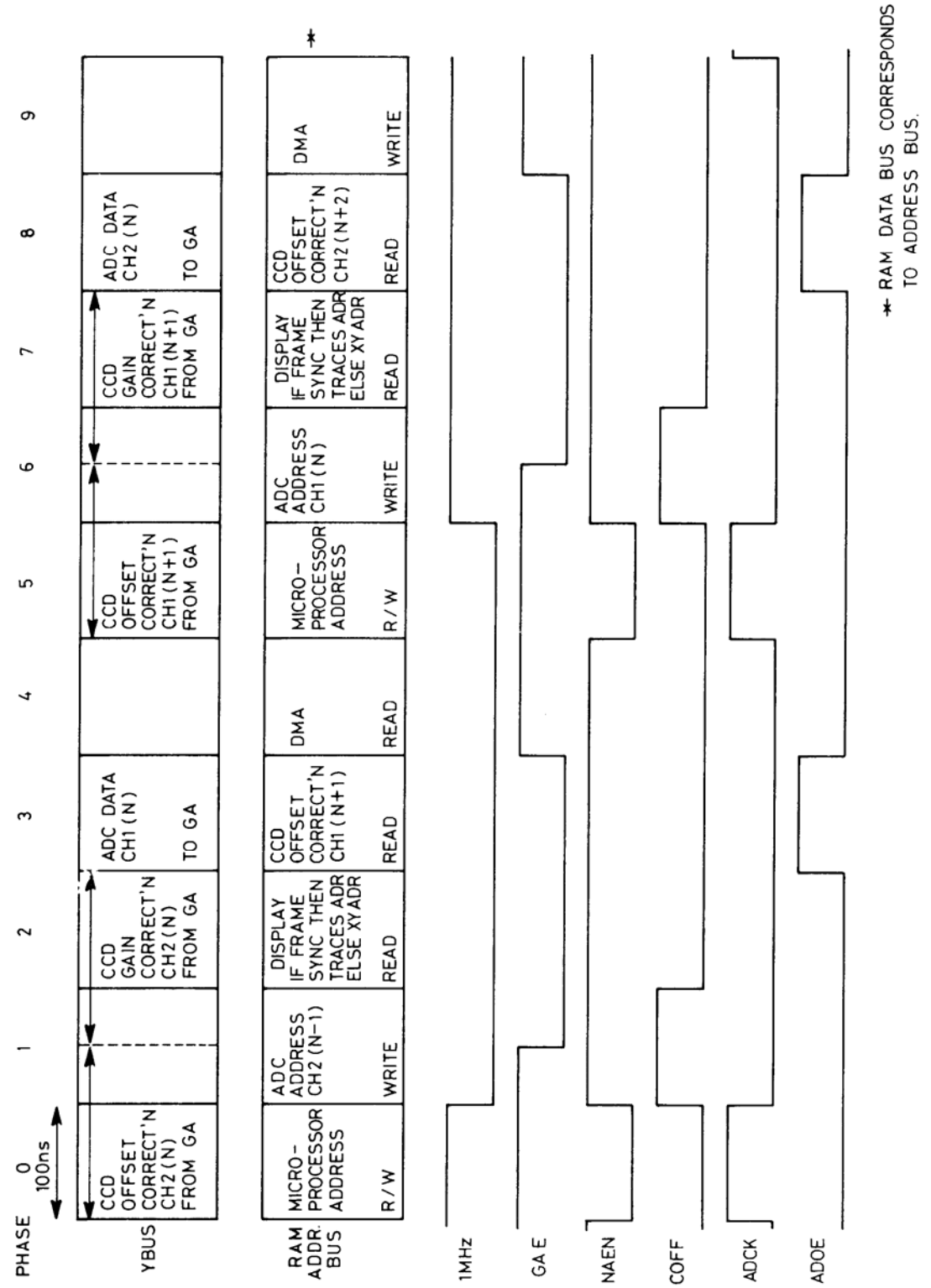


Fig. 5.4.28a Gate Array 10 Phase Timing

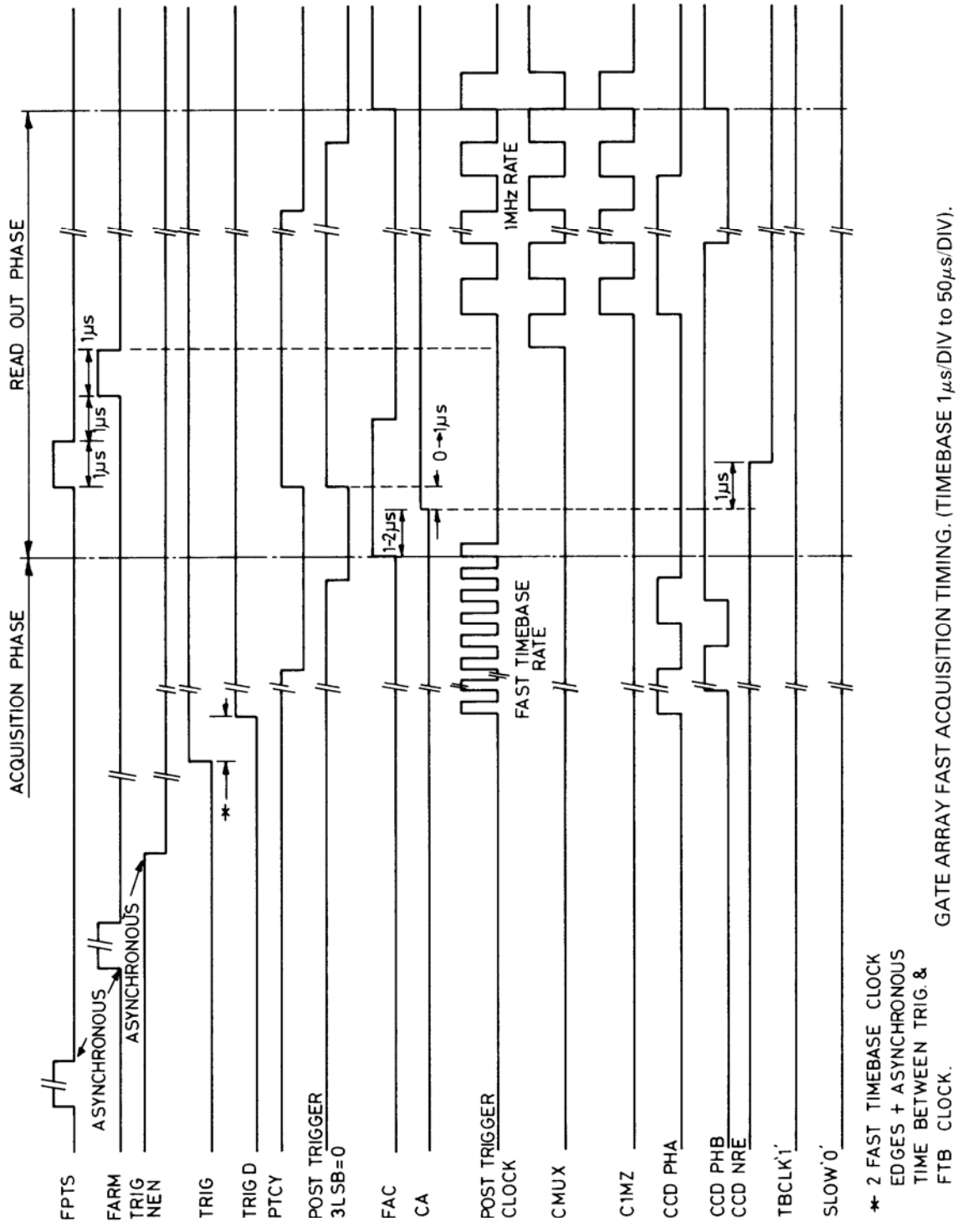


Fig. 5.4.28b Acquisition timing (fast)

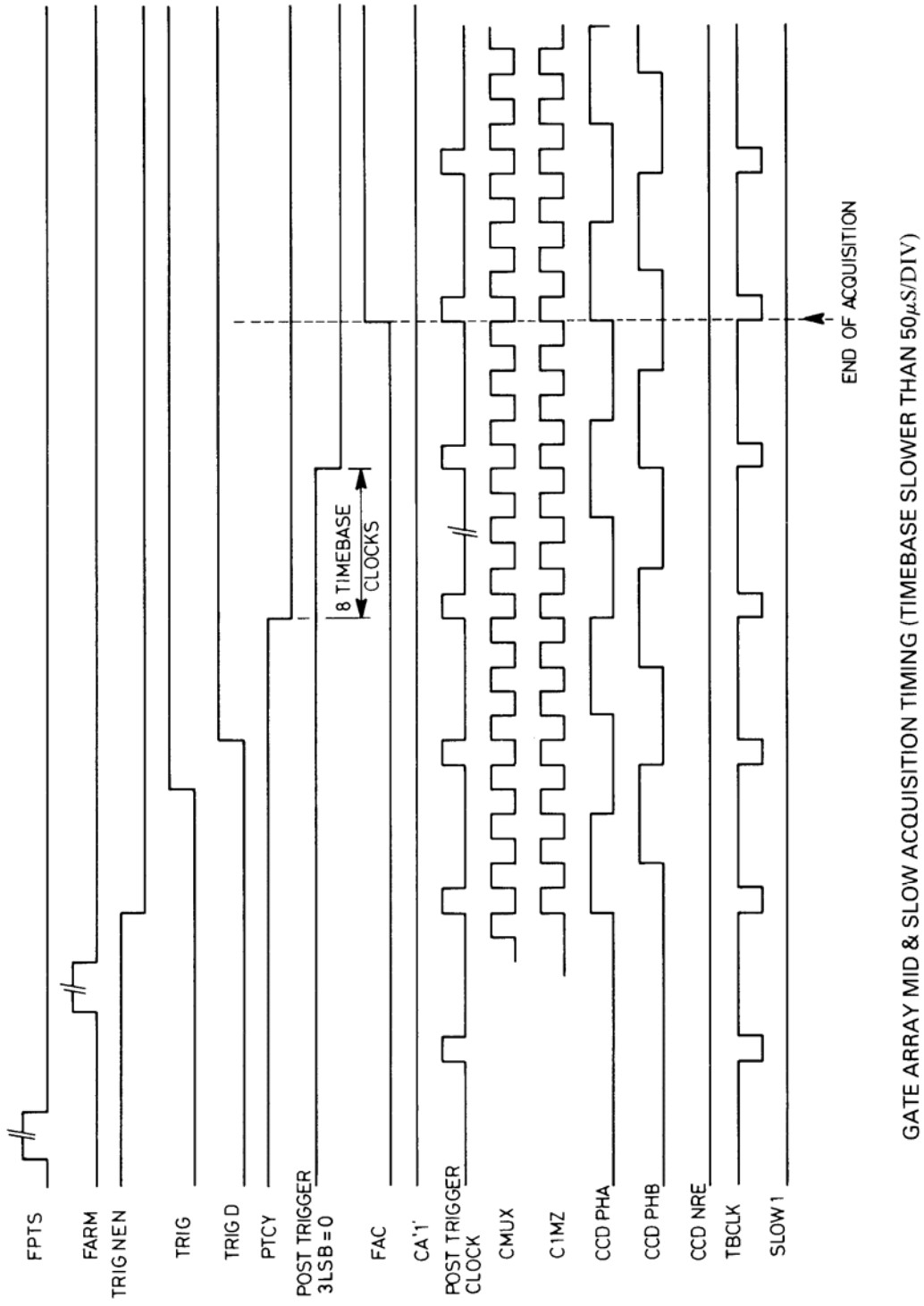


Fig. 5.4.28c Acquisition timing (slow)

5.4.30 Self Calibration Attenuator

As part of the power up automatic set-up procedure both input channels are self calibrated using the voltages produced by N3 a precision attenuator network. N3 divides the -8V reference voltage from the reference voltage generator and presents six stable voltages to U10. U10 is a 1 of 8 multiplexer driven from U11 which is in turn driven by the microprocessor.

5.4.31 Tube Base Board

This board sits on the base plug of the CRT.

WARNING *When the instrument is on, there are voltages up to 400V present on this board. These can be retained for about a minute after power down.*

This board brings all the tube control voltages to the CRT base. Measurements can be taken on this board but care should be taken to avoid touching any pins or tracks.

5.4.32 Tube Scan Coil Board

This board is located on the side of the scan coil assembly and brings all the scan signals to the CRT. R820 and R821 from the deflection circuit are mounted on this board.

6.0 CIRCUIT DIAGRAMS AND COMPONENT LISTS

This section contains all the circuit diagrams of the 400 DSO, together with component layouts and mechanical drawings. For ease of component location, each major functional block on the main PCB can be treated as a separate unit. Each of the main circuit blocks shown in figure 6.1 has its component identification numbers commencing with a different group of hundreds as shown below.

up to	200 Preamp and trigger	(figure 6.6)
	300+ Acquisition (CCD)	(figure 6.7)
	500+ ECL	(figure 6.8)
	600+ Power supply	(figure 6.9)
	700+ Video and deflection	(figure 6.10)

The relevant parts are shown on the component list preceding the appropriate circuit diagram.

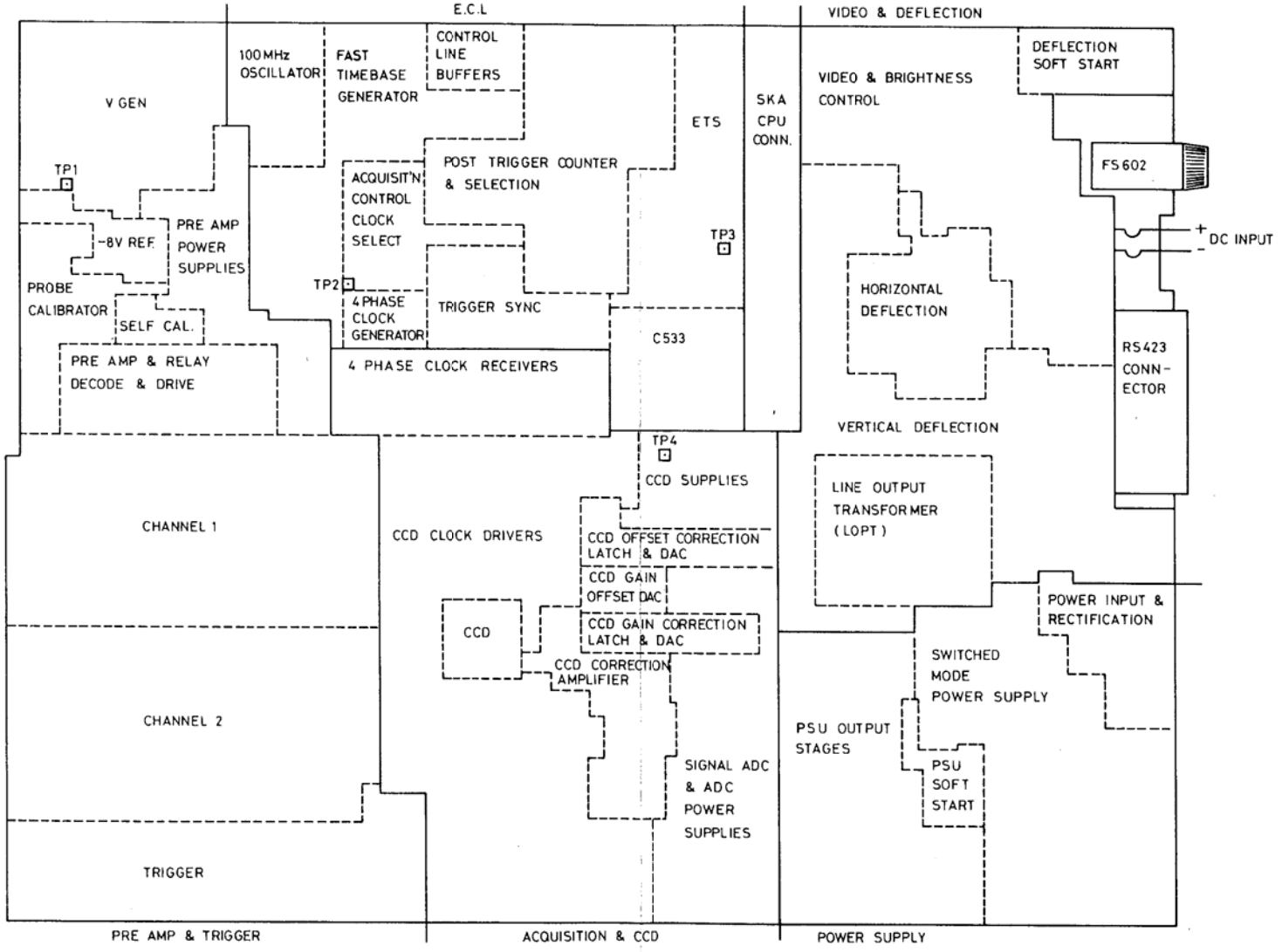


Fig. 6.1.1 Main PCB Circuit Block Location

400 MAIN PCB: PIN OUT OF SKA

Pin	*Signal Name*	*Level*	*Direction*
SKA1A	YBUS0	CMOS	bi-directional
SKA1B	YBUS1	CMOS	bi-directional
SKA1C	YBUS2	CMOS	bi-directional
SKA2A	YBUS3	CMOS	bi-directional
SKA2B	YBUS4	CMOS	bi-directional
SKA2C	YBUS5	CMOS	bi-directional
SKA3A	YBUS6	CMOS	bi-directional
SKA3B	YBUS7	CMOS	bi-directional
SKA3C	CCDMUX	CMOS	from CPU board
SKA4A	CCDNRE	CMOS	from CPU board
SKA4B	CGAIN	CMOS	from CPU board
SKA4C	CAL	CMOS	from CPU board
SKA5A	+5V power	+5V	to CPU board
SKA5B	+5V power	+5V	to CPU board
SKA5C	+5V power	+5V	to CPU board
SKA6A	0V power	0V	to CPU board
SKA6B	0V power	0V	to CPU board
SKA6C	0V power	0V	to CPU board
SKA7A	0V power	0V	to CPU board
SKA7B	0V power	0V	to CPU board
SKA7C	0V power	0V	to CPU board
SKA8A	0V power	0V	to CPU board
SKA8B	0V power	0V	to CPU board
SKA8C	0V power	0V	to CPU board
SKA9A	0V power	0V	to CPU board
SKA9B	0V power	0V	to CPU board
SKA9C	0V power	0V	to CPU board
SKA10A	NCURSOR	CMOS	from CPU board
SKA10B	n/c.....		
SKA10C	TXD		from CPU board
SKA11A	0V power	0V	to CPU board
SKA11B	0V power	0V	to CPU board
SKA11C	0V power	0V	to CPU board
SKA12A	RAM EN	CMOS	to CPU board
SKA12B	RXD		to CPU board
SKA12C	RTS		from CPU board
SKA13A	n/c.....	.....	
SKA13B	n/c.....	.....	
SKA13C	Trigger LED		front panel via CPU board
SKA14A	n/c.....	.....	
SKA14B	VGENRS	CMOS	from CPU board
SKA14C	VGENSP	CMOS	from CPU board

Pin	*Signal Name*	*Level*	*Direction*
SKA15A	NSCALE	CMOS	from CPU board
SKA15B	VGEN2	CMOS	from CPU board
SKA15C	VGEN1	CMOS	from CPU board
SKA16A	NALPHA	CMOS	from CPU board
SKA16B	NX-Y	CMOS	from CPU board
SKA16C	VGEN0	CMOS	from CPU board
SKA17A	NTRACE3	CMOS	from CPU board
SKA17B	SP1NDE	CMOS	from CPU board
SKA17C	MOSI	CMOS	from CPU board
SKA18A	NTRACE2	CMOS	from CPU board
SAK18B	VRL	CMOS	from CPU board
SKA18C	SCK	CMOS	from CPU board
SKA19A	NTRACE1	CMOS	from CPU board
SKA19B	SP0NDE	CMOS	from CPU board
SKA19C	VRH	CMOS	from CPU board
SKA20A	NFSYNC	CMOS	from CPU board
SKA20B	CTS		to CPU board
SKA20C	GND	0V	to CPU board
SKA21A	LSYNC	CMOS	from CPU board
SKA21B	FTRIG	CMOS	from CPU board
SKA21C	SPSYNC	CMOS	to CPU board
SKA22A	+15V power	+15V	to CPU board
SKA22B	+15V power	+15V	to CPU board
SKA22C	+15V power	+15V	to CPU board
SKA23A	−5V power	+5V	to CPU board
SKA23B	−5V power	+5V	to CPU board
SKA23C	−5V power	+5V	to CPU board
SKA24A	FTB2	CMOS	from CPU board
SKA24B	FTB1	CMOS	from CPU board
SKA24C	n/c.....	.....	
SKA25A	AN7	CMOS	from CPU board
SKA25B	TRIGNEN	CMOS	from CPU board
SKA25C	FTB3	CMOS	from CPU board
SKA26A	FARM	CMOS	from CPU board
SKA26B	CCDPHB	CMOS	to CPU board
SKA26C	n/c.....	.....	
SKA27A	FPTS	CMOS	from CPU board
SKA27B	TRIGD	CMOS	to CPU board
SKA27C	FACOMP	CMOS	to CPU board
SKA28A	PT0	CMOS	from CPU board
SKA28B	PT1	CMOS	from CPU board
SKA28C	PT2	CMOS	from CPU board

400 MAIN PCB: PIN OUT OF SKA (Cont)

Pin	*Signal Name*	*Level*	*Direction*
SKA29A	COFFSET	CMOS	from CPU board
SKA29B	ADCCLK	CMOS	from CPU board
SKA29C	ADCOE	CMOS	from CPU board
SKA30A	PTCARY	CMOS	from CPU board
SKA30B	n/c.....	.....	
SKA30C	MCLK	CMOS	to CPU board
SKA31A	SLOW	CMOS	from CPU board
SKA31B	TBCLK	CMOS	from CPU board
SKA31C	PTCLK	CMOS	to CPU board
SKA32A	CCD1MHz	CMOS	from CPU board
SKA32B	CA	CMOS	from CPU board
SKA32C	CCDPHA	CMOS	to CPU board

Fig 6.1.2 400 Main PCB: Pin out of SKA

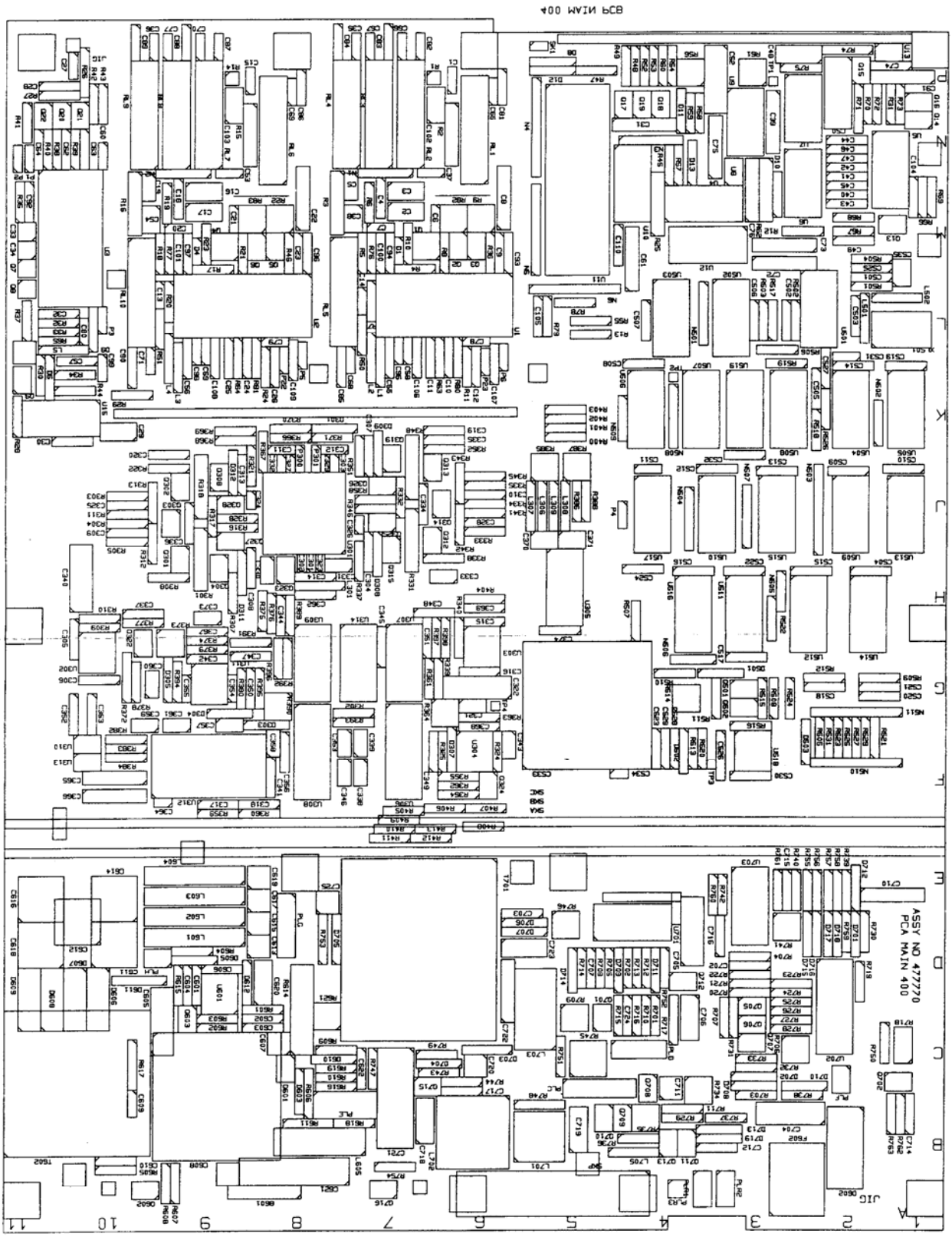


Fig. 6.2 Component layout main PCB

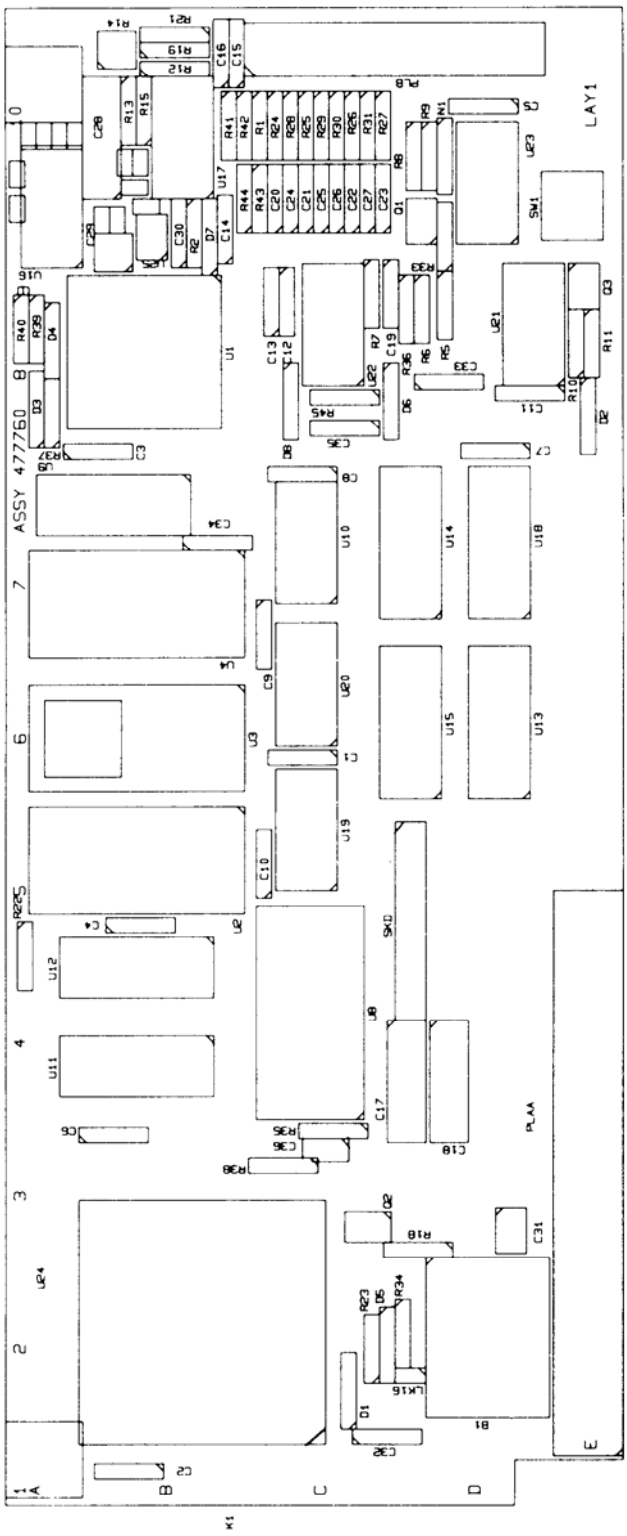


Fig. 6.3 Component layout CPU board

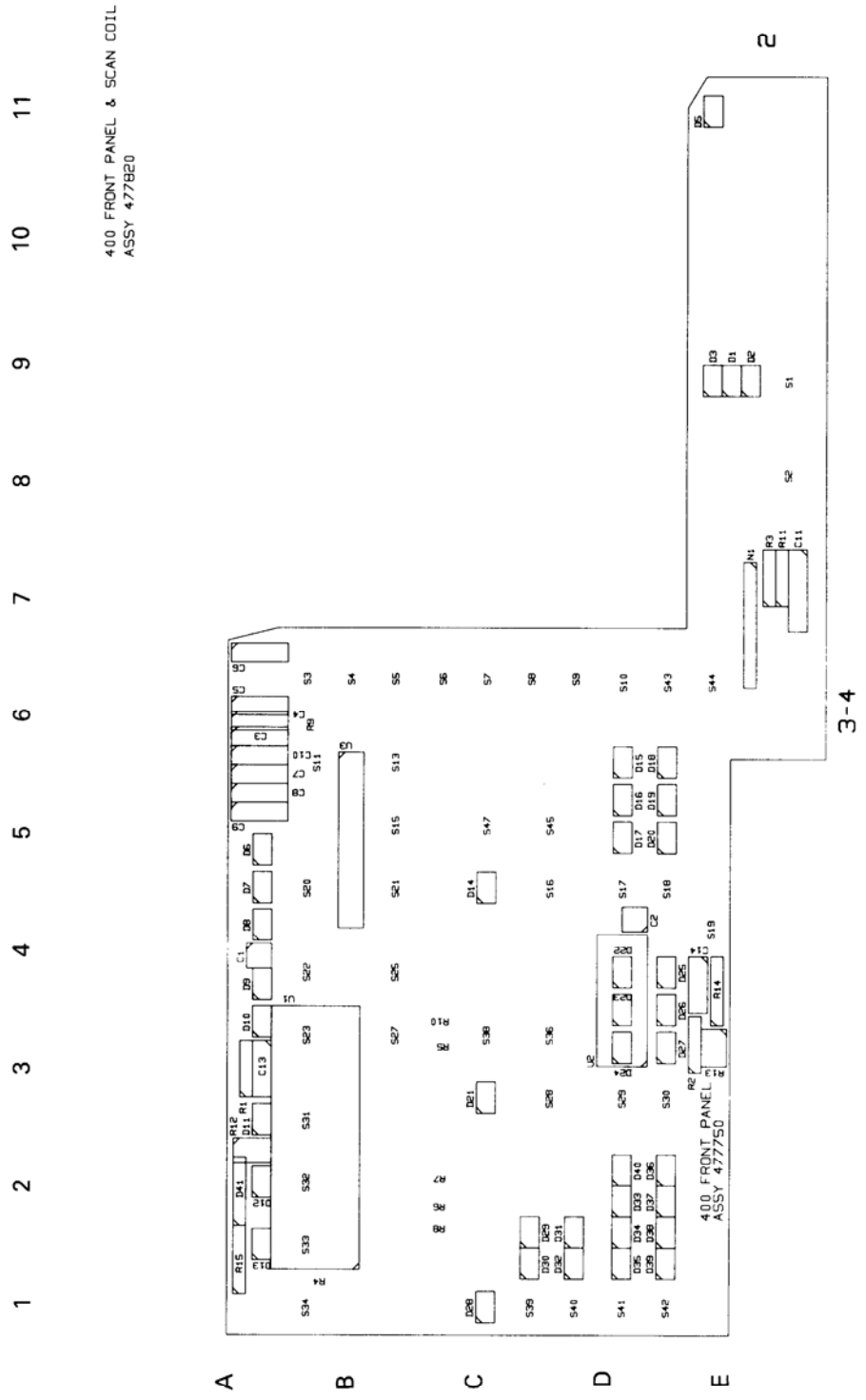


Fig. 6.4 Component layout front panel

PREAMP AND TRIGGER - PART OF 400 MAIN BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R1	47R	5	⅛W	N7	43146
R2	3K9	5	½W	N7	18557
R3	390K	5	½W	M8	18581
R4	47R	5	⅛W	L7	43146
R5	51K	1	¼W	M7	455469
R6	220R	1	¼W	M7	455412
R7	18K	5	⅛W	L7	44237
R8	10K	5	⅛W	M7	44235
R9	10K Pot	20	⅓W	M6	455938
R10	33R	5	⅛W	M7	43144
R11	68R	5	⅛W	K6	43148
R12	2R2	5	¼W	M3	455961
R13	100R	5	⅛W	L5	43150
R14	47R	5	⅛W	N9	43146
R15	3K9	5	½W	N9	18557
R16	390K	5	½W	M10	18581
R17	47R	5	⅛W	L9	43146
R18	51K	1	¼W	M10	455469
R19	220R	1	¼W	M10	455412
R20	18K	5	⅛W	L10	44237
R21	10K	5	⅛W	M9	44235
R22	10K Pot	20	⅓W	M9	455938
R23	33R	5	⅛W	M9	43144
R24	68R	5	⅛W	K8	43148
R25	12R	5	½W	M4	18527
R26	91K	2	¼W	P10	38641
R27	9K1	1	¼W	N11	455451
R28	100R	5	⅛W	K11	43150
R29	1K2	5	⅛W	K10	44227
R30	680R	5	⅛W	K11	44224
R31	15R	5	⅛W	N2	43140
R32	820R	5	⅛W	L11	44225
R33	22K	5	⅛W	L11	44238
R34	5K6	5	⅛W	K11	44233
R35	100K	5	⅛W	M11	44246
R36	7K5	1	¼W	M6	455449
R37	100K	5	⅛W	L11	44246
R38	100R	5	⅛W	N11	43150
R39	220R	1	¼W	N11	455412
R40	220R	1	¼W	N11	455412
R41	1K	5	⅛W	N11	44226
R42	1K	5	⅛W	N10	44226
R43	1K	5	⅛W	N10	44226
R44	1M	5	⅛W	K10	44258
R45	22K	5	⅛W	N4	44238
R46	7K5	1	¼W	M8	455449
R47	1K8	5	⅛W	P5	44229
R48	10K	5	⅛W	P4	44235
R49	10K	5	⅛W	P5	44235
R50	100R	5	⅛W	L7	43150
R51	100R	5	⅛W	L10	43150
R52	1K	1	¼W	P4	455428
R53	1K	1	¼W	P4	455428
R54	7K5	1	¼W	P4	455449
R55	100R	5	⅛W	L5	43150
R56	1K Pot	20	⅓W	P4	455935
R57	1K	1	¼W	N4	455428
R58	2K7	1	¼W	N4	455438
R59	10K	1	¼W	N4	455452
R60	22K	5	⅛W	P4	44238
R61	10K Pot	20	⅓W	P3	455938
R62	56R	5	½W	M3	18535
R63	10K	5	⅛W	K7	44235
R64	10K	5	⅛W	K9	44235
R65	3K3	5	⅛W	L11	43358
R66	10K	5	⅛W	M1	44235
R67	2K7	5	⅛W	M2	44230
R68	2K7	5	⅛W	M2	44230
R69	4K7	5	⅛W	M1	44232
R70	220R	1	¼W	N2	455412
R71	240K	2	¼W	N2	38651
R72	33K	5	⅛W	N2	44240
R73	2K2	5	⅛W	N2	43357
R74	1M8	5	¼W	P2	29594
R75	220K	5	⅛W	P3	44250
R76	180R	5	⅛W	M7	43715
R77	180R	5	⅛W	M10	43715
R78	100R	5	⅛W	L5	43150
R79	100R	5	⅛W	L5	43150
R80	220R	1	¼W	K6	455412
R81	220R	1	¼W	K9	455412
R82	10K Pot	20	⅓W	M7	455938
R83	10K Pot	20	⅓W	M9	455938
RESISTOR NETWORKS					
N1	50:1 Attenuator			M7	456226
N2	50:1 Attenuator			M10	456226
N3	Self Cal Network			N4	456339
N5	47K × 8 SIL	5	⅛W	M6	450602
N6	47K × 8 SIL	5	⅛W	L5	450602
CAPACITORS					
C1	56nF	20	400V	P6	455618
C2	0.6-3.5pF trimmer			M7	452015
C3	0.6-3.5pF trimmer			M7	452015
C4	150pF	10	50V	M7	452157
C5	2.2nF	20	500V	M8	22389
C6	10uF Tant	20	16V	M7	457212
C7	10uf Tant	20	16V	M7	457212
C8	10uF E	+50/-10	25V	M6	32180
C9	100nF	+80/-20	50V	M6	43498
C10	2.2pF	+/-0.5pF	50V	K6	452135
C11	220pF	10	50V	K7	452159
C12	10nF	10	50V	K6	452179
C13	10uF Tant	20	16V	L10	457212
C14	10uF Tant	20	16V	L7	457212
C15	56nF	20	400V	N9	455618
C16	0.6-3.5pF trimmer			M9	452015
C17	0.6-3.5pF trimmer			M9	452015
C18	150pF	10	50V	M9	452157
C19	2.2nF	20	500V	M10	22389
C20	10uF Tant	20	16V	M9	457212

PREAMP AND TRIGGER - PART OF 400 MAIN BOARD (Cont)

Cir ref	Description	Tol%±	Rating	Grid	Part No.
CAPACITORS (Cont)					
C21	10uF Tant	20	16V	M9	457212
C22	10uF E	+50/-10	25V	M8	32180
C23	100nF	+80/-20	50V	M8	43498
C24	2.2pF	+/-0.5pF	50V	K9	452135
C25	220pF	10	50V	K9	452159
C26	10nF	10	50V	K8	452179
C27	6.8pF	+/-1pF	500V	P11	22362
C28	68pF	10	50V	N11	452153
C29	0.22uF	10	100V	K10	44370
C30	100nF	+80/-20	50V	K11	43498
C31	10uF E	+50-10	25V	N4	32180
C32	100nF	+80/-20	50V	L11	43498
C33	10uF E	+50/-10	35V	M11	450587
C34	10uF E	+50/-10	35V	M11	450587
C35	2.2uF Tant	20	35V	P8	35930
C36	2.2uF Tant	20	35V	P10	35930
C37	4.7pF	+/-1pF	500V	M7	29649
C38	1uF Non Polarized	10	50V	M8	455698
C39	10uF E	+50/-10	25V	N3	32180
C40	10nF	10	50V	M2	452179
C41	10nF	10	50V	M2	452179
C42	10nF	10	50V	M2	452179
C43	10nF	10	50V	M2	452179
C44	10nF	10	50V	N2	452179
C45	10nF	10	50V	M2	452179
C46	10nF	10	50V	N2	452179
C47	10nF	10	50V	N2	452179
C48	470nF	10	63V	P3	39181
C49	2.2nF	10	50V	M2	452171
C50	10nF	2½	63V	N2	35924
C52	47uF E	+50/-10	16V	P3	453376
C53	4.7pF	+/-1pF	500V	M9	29649
C54	1uF Non Polarized	10	50V	M10	455698
C55	100nF	+80/-20	50V	K7	43498
C56	100nF	+80/-20	50V	K9	43498
C57	100nF	+80/-20	50V	K11	43498
C58	10uF Tant	20	16V	K7	457212
C59	10uF Tant	20	16V	K9	457212
C60	10uF Tant	20	16V	N10	457212
C61	10uF E	+50/-10	25V	M4	32180
C62	1.8nF	10	50V	N11	452170
C63	47nF	10	50V	N10	457786
C64	47nF	10	50V	N11	457786
C65	2.2uF Tant	20	35V	N6	35930
C66	2.2uF Tant	20	35V	P7	35930
C67	2.2uF Tant	20	35V	P7	35930
C68	2.2uF Tant	20	35V	K8	35930
C69	2.2uF Tant	20	35V	N8	35930
C70	2.2uF Tant	20	35V	P9	35930
C71	2.2uF Tant	20	35V	K10	35930
C72	10uF E	+50/-10	25V	L3	32180
C73	10uF E	+50/-10	25V	M3	32180
C74	100nF	+80/-20	50V	P2	43498
C75	10uF E	+50/-10	25V	N4	32180
C76	10uF E	+50/-10	25V	M3	32180
C77	2.2uF Tant	20	35V	P10	35930
C78	10uF Tant	20	16V	L6	457212
C79	10uF Tant	20	16V	L8	457212
C80	10uF Tant	20	16V	L10	457212
C81	100nF	+80/-20	50V	N6	43498
C82	10uF Tant	20	16V	P7	457212
C83	100nF	+80/-20	50V	P7	43498
C84	100nF	+80/-20	50V	P8	43498
C85	100nF	+80/-20	50V	K8	43498
C86	100nF	+80/-20	50V	N8	43498
C87	10uF Tant	20	16V	P9	457212
C88	100nF	+80/-20	50V	P9	43498
C89	100nF	+80/-20	50V	P10	43498
C90	100nF	+80/-20	50V	K10	43498
C91	10uF E	+50/-10	25V	P2	32180
C92	10nF	10	50V	M11	452179
C93	100nF	+80/-20	50V	M6	43498
C94	100nF	+80/-20	50V	M7	43498
C95	2.2uF Tant	20	35V	K7	35930
C96	100nF	+80/-20	50V	M8	43498
C97	100nF	+80/-20	50V	M9	43498
C98	2.2uF Tant	20	35V	K9	35930
C99	2.2uF Tant	20	35V	K10	35930
C100	100nF	+80/-20	50V	M7	43498
C101	100nF	+80/-20	50V	M9	43498
C102	Not fitted				N7
C103	Not fitted				N9
C104	100nF	+80/-20	50V	M1	43498
C105	100nF	+80/-20	50V	K11	43498
C106	100nF	+80/-20	50V	K7	43498
C107	100nF	+80/-20	50V	K6	43498
C108	100nF	+80/-20	50V	K9	43498
C109	100nF	+80/-20	50V	K8	43498
C110	220pF	10	50V	M5	452159
DIODES					
D1	JPAD50			M7	41814
D4	JPAD50			M9	41814
D5	Zener	5	6V8 400mW	K11	33931
D6	Zener	5	6V8 400mW	M7	33931
D7	Zener	5	6V8 400mW	M9	33931
D8	Zener	5	5V1 400mW	K11	33928
D9	1N4148		75V 150mA	L10	23802
D10	Zener	5	2V7 400mW	M3	33921
D11	1N4148		75V 150mA	N4	23802
D12	1N4148		75V 150mA	P5	23802
D13	Ref Diode	+/-0V3	6V2	M4	40045
N4	Diode array SIL			N6	456614

PREAMP AND TRIGGER - PART OF 400 MAIN BOARD (Cont)

Cir ref	Description	Tol%±	Rating	Grid	Part No.
TRANSISTORS					
Q1	2N5566			M7	457866
Q2	BC557B			M6	44950
Q3	BC557B			M6	44950
Q4	2N5566			M9	457866
Q5	BC557B			M8	44950
Q6	BC557B			M9	44950
Q7	MPSH81			L11	457002
Q8	MPSH81			L11	457002
Q9	BC547B			K11	44951
Q13	BC457B			M2	44951
Q14	2N3906			N1	21533
Q15	U1898			P2	456615
Q16	BC457B			N1	44951
Q17	2N3906			N5	21533
Q18	2N3906			N4	21533
Q19	2N3906			N4	21533
Q20	BC547B			N11	44951
Q21	BC547B			N11	44951
Q22	BC547B			N11	44951
INTEGRATED CIRCUITS					
U1	Preamp Semi custom			L6	456617
U2	Preamp Semi custom			L8	456617
U3	Trigger Semi custom			M10	456616
U4	Voltage reg		8V 1.5A	M4	37561
U5	4051			N2	41897
U6	LMC660CN			M3	457206
U7	LMC660CN			N3	457206
U8	Voltage reg		5V 100mA	M3	40406
U9	LM324			N3	44495
U10	4051			M4	41897
U11	MM5450N			M5	456613
U12	TL780-12CKC reg		12V 1.5A	M4	456274
U13	Voltage reg		-12V 0.1A	P2	456652
U15	74HC4538			K10	457168

Cir ref	Description	Tol%±	Rating	Grid	Part No.
CONNECTORS					
SKA	96 Way DIN 41612 Type C			F5	453848
SK1	2 way 0.1" locking header			P5	41391
CH1	BNC Socket 50R			---	456088
CH2	BNC Socket 50R			---	456088
EXT	BNC Socket 50R			---	456088
MISCELLANEOUS					
L1	10uH Choke	10	¼W	K7	455739
L2	10uH Choke	10	¼W	K7	455739
L3	10uH Choke	10	¼W	K9	455739
L4	10uH Choke	10	¼W	K10	455739
L5	10uH Choke	10	¼W	L11	455739
P1	Mini component carrier solder pin x2			M11	36207
P2	Mini component carrier solder pin x2			M11	36207
P3	Mini component carrier solder pin x2			L10	36207
P5	Mini component carrier solder pin x2			K8	36207
P6	Mini component carrier solder pin x2			K6	36207
P22	Mini component carrier solder pin x2			K8	36207
P23	Mini component carrier solder pin x2			K6	36207
RL1	Reed Relay		5V coil	N6	455318
RL2	Reed Relay		5V coil	N7	455318
RL3	Reed Relay		5V coil	N7	455318
RL4	Reed Relay		5V coil	N8	455318
RL5	Reed Relay		5V coil	L8	455318
RL6	Reed Relay		5V coil	N8	455318
RL7	Reed Relay		5V coil	N9	455318
RL8	Reed Relay		5V coil	N10	455318
RL9	Reed Relay		5V coil	N10	455318
RL10	Reed Relay		5V coil	L10	455318
TP1	Wire 0.045" square brass tin plate			N3	43355

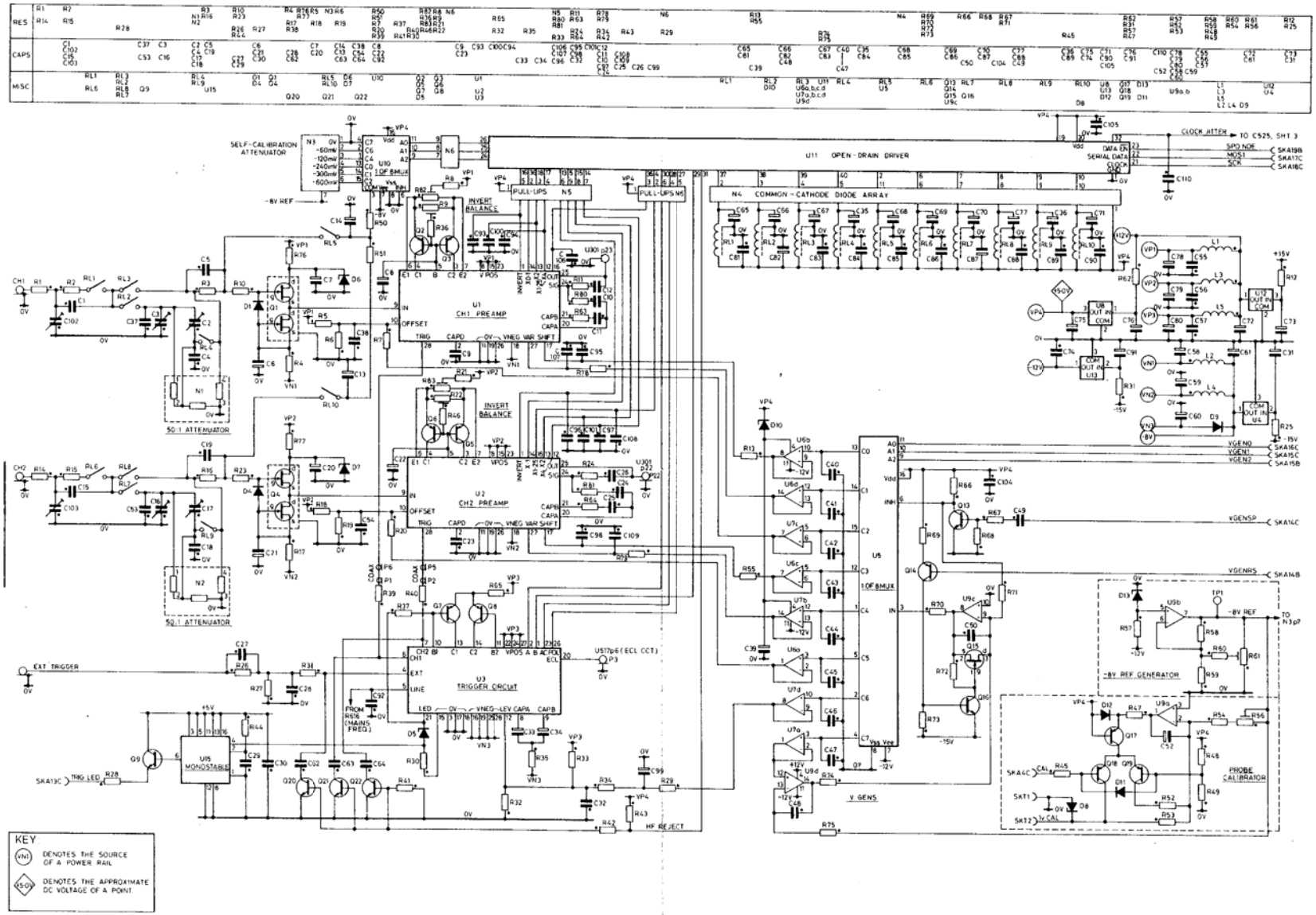


Fig. 6.6.1 Preamp and trigger circuit diagram

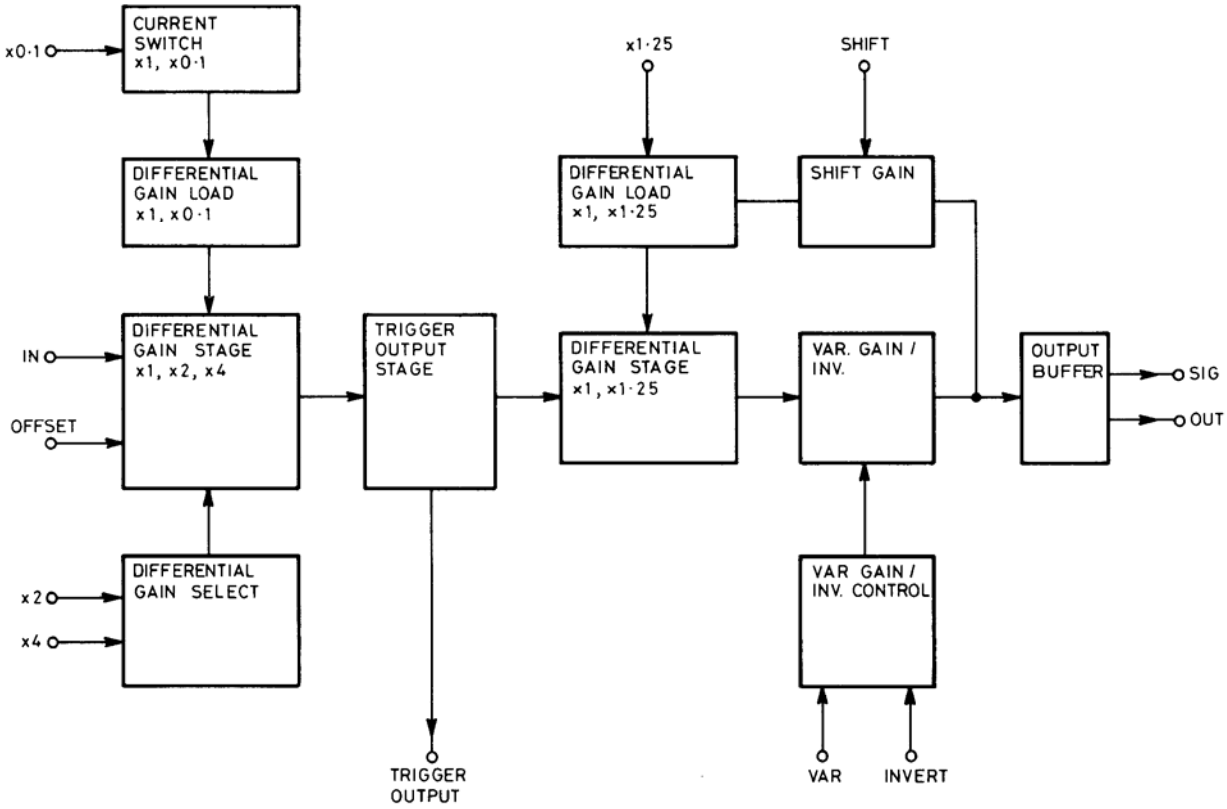


Fig. 6.6.2 Input Pre-amp chip block diagram

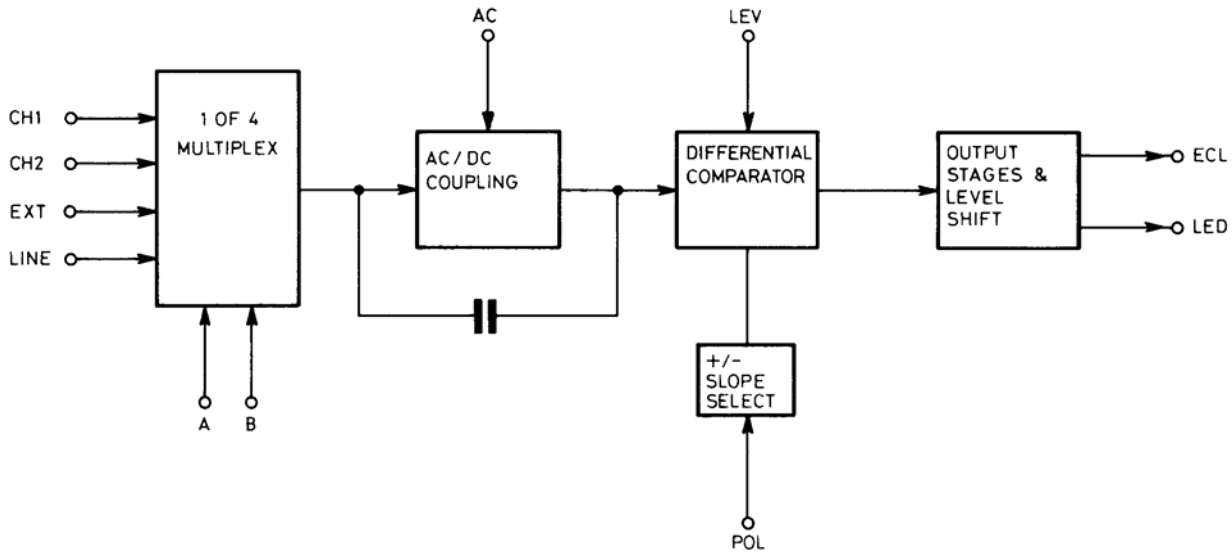


Fig. 6.6.3 Trigger chip block diagram

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ACQUISITION AND CCD - PART OF 400 MAIN BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R301	300R	1	¾W	H9	457289
R302	33R	5	⅛W	F7	43144
R303	33R	5	⅛W	J10	43144
R304	680R	5	⅛W	J10	44224
R305	2K2	5	⅛W	H10	43357
R307	2K7	5	⅛W	H9	44230
R308	47K	1	¼W	H9	455468
R309	30K	1	¼W	G10	455463
R310	39K	1	¼W	H10	455466
R311	120R	5	⅛W	J10	43713
R312	68R	5	⅛W	H10	43148
R313	68R	5	⅛W	J10	43148
R316	33R	5	⅛W	J9	43144
R317	68R	5	⅛W	J9	43148
R318	300R	1	¾W	J9	457289
R321	2K7	5	⅛W	J9	44230
R322	47K	1	¼W	J10	455468
R324	1K5	5	⅛W	F6	44228
R325	680R	1	¼W	F6	455425
R328	33R	5	⅛W	J9	43144
R331	300R	1	¾W	H7	457289
R332	68R	5	⅛W	J7	43148
R333	33R	5	⅛W	J6	43144
R334	680R	5	⅛W	J6	44224
R335	2K2	5	⅛W	J6	43357
R337	2K7	5	⅛W	H7	44230
R338	47K	1	¼W	H6	455468
R339	30K	1	¼W	G7	455463
R340	39K	1	¼W	G6	455466
R341	120R	5	⅛W	J6	43713
R342	68R	5	⅛W	J6	43148
R343	68R	5	⅛W	J6	43148
R345	1K	5	⅛W	J6	44226
R346	33R	5	⅛W	J7	43144
R348	300R	1	¾W	J7	457289
R351	2K7	5	⅛W	J7	44230
R352	47K	1	¼W	J6	455468
R354	10K	5	⅛W	F6	44235
R355	4K7	5	⅛W	F6	44232
R358	33R	5	⅛W	J7	43144
R359	150R	5	⅛W	E9	43714
R360	150R	5	⅛W	E9	43714
R361	2R2	5	⅛W	G7	452690
R362	680R	5	⅛W	F6	44224
R363	1K8	5	⅛W	F6	44229
R364	220R Pot	20	⅓W	G7	455933
R366	1K5	5	⅛W	K8	44228
R367	240R	1	¼W	K8	455413
R368	1K	5	⅛W	K9	44226
R369	1K	5	⅛W	K9	44226
R370	12K	5	⅛W	K8	43246
R371	12K	5	⅛W	K8	43246
R372	680R	5	¼W	G10	28723
R373	470R Pot	20	⅓W	G9	455934
R374	1K5	5	⅛W	G9	44228
R375	390R	5	⅛W	H8	44221
R376	180R	1	¼W	H8	455410
R377	100R	5	⅛W	H10	43150
R378	10R	5	⅛W	G10	43138
R379	10R	5	⅛W	G9	43138
R380	180R	1	¼W	G9	455410
R382	180R	1	¼W	F10	455410
R383	10R	1	¼W	F10	455380
R384	10R	1	¼W	F10	455380
R385	10K Pot	20	⅓W	J5	455938
R386	2K7	5	⅛W	J5	44230
R387	10K Pot	20	⅓W	J5	455938
R388	2K7	5	⅛W	J5	44230
R389	100R	5	⅛W	H8	43150
R390	470R Pot	20	⅓W	G8	455934
R391	240R	1	¼W	G9	455413
R392	220R	1	¼W	G8	455412
R393	470R	5	⅛W	F7	44222
R394	470R	5	⅛W	G9	44222
R395	1K	1	¼W	G9	455428
R396	680R	1	¼W	G8	455424
R397	3K9	5	⅛W	G7	44231
R398	3K9	1	¼W	G7	44231
R400	150R	5	⅛W	K5	43714
R401	150R	5	⅛W	K5	43714
R402	150R	5	⅛W	K5	43714
R403	150R	5	⅛W	K5	43714
R404	330R	5	⅛W	H6	44220
R405	100R	5	⅛W	E7	43150
R406	100R	5	⅛W	E6	43150
R407	100R	5	⅛W	E6	43150
R408	100R	5	⅛W	E6	43150
R409	100R	5	⅛W	E7	43150
R410	100R	5	⅛W	E7	43150
R411	100R	5	⅛W	E7	43150
R412	100R	5	⅛W	E7	43150
R413	330R	5	⅛W	E7	44220
CAPACITORS					
C301	100nF	20	50V	H8	456932
C302	100nF	20	50V	H8	456932
C303	100nF	20	50V	J8	456932
C304	1nF	10	50V	H7	452167
C305	680pF	10	50V	G11	452165
C306	1nF	10	50V	G10	452167
C307	1nF	10	50V	J7	452167
C308	1nF	10	50V	H9	452167
C309	10nF	10	50V	J10	452179
C310	10nF	10	50V	J6	452179
C311	15pF	10	500V	J8	22366
C312	10pF	10	500V	J8	22364
C313	1nF	10	50V	J9	452167
C314	27pF	10	50V	H8	452148
C315	680pF	10	50V	H6	452165
C316	1nF	10	50V	G6	452167
C317	47pF	10	50V	F9	452151
C318	47pF	10	50V	F9	452151

ACQUISITION AND CCD - PART OF 400 MAIN BOARD (Cont)

Cir ref	Description	Tol%±	Rating	Grid	Part No.
CAPACITORS (Cont)					
C319	10nF	10	50V	K6	452179
C320	10nF	10	50V	J10	452179
C321	10uF Tant	20	16V	G6	457212
C322	47uF E	+50/-10	16V	G6	453376
C323	100nF	20	50V	H8	456932
C324	100nF	20	50V	J9	456932
C325	100nF	+80/-20	50V	J10	43498
C326	100nF	20	50V	J7	456932
C327	100nF	20	50V	J8	456932
C328	100nF	+80/-20	50V	J6	43498
C329	100nF	20	50V	J8	456932
C330	4.7uF Tant	20	35V	H8	53249
C331	4.7uF Tant	20	35V	H8	53249
C332	100nF	20	50V	J8	456932
C333	10uF Tant	20	16V	H6	457212
C334	100nF	+80/-20	50V	J7	43498
C335	10pF	10	50V	J6	452143
C336	100nF	+80/-20	50V	H9	43498
C337	100nF	+80/-20	50V	H10	43498
C338	10uF Tant	20	16V	F7	457212
C339	10uF Tant	20	16V	F7	457212
C340	47uF E	+50/-10	16V	H11	453376
C341	100nF	+80/-20	50V	F8	43498
C342	18pF	10	50V	G9	452146
C343	10uF Tant	20	16V	F6	457212
C344	10nF	10	50V	H8	452179
C345	10nF	10	50V	G7	452179
C346	10nF Tant	10	16V	F8	457212
C347	100nF	+80/-20	50V	G9	43498
C348	10nF	10	50V	H7	452179
C349	10nF	10	50V	F7	452179
C350	100pF	10	50V	G9	452155
C351	10nF	10	50V	G7	452179
C352	100nF	+80/-20	50V	G11	43498
C353	10uF Tant	20	16V	F8	457212
C354	10uF Tant	20	16V	G9	457212
C355	10uF Tant	20	16V	G9	457212
C356	100nF	+80/-20	50V	F8	43498
C357	10uF Tant	20	16V	F9	457212
C358	10uF Tant	20	16V	F8	457212
C359	10uF Tant	20	16V	F10	457212
C360	10uF Tant	20	16V	G10	457212
C361	10uF Tant	20	16V	F9	457212
C362	100nF	+80/-20	50V	H8	43498
C363	100nF	+80/-20	50V	G10	43498
C365	10uF	+50/-10	25V	F10	32180
C366	10uF	+50/-10	25V	F10	32180
C367	10nF	10	50V	G9	452179
C368	100nF	+80/-20	50V	F6	43498
C369	10nF	10	50V	H6	452179
C370	1.2-10pF Trimmer			H5	451127
C371	1.2-10pF Trimmer			H5	451127
C373	10uF Tant	20	16V	H9	457212
C374	10nF	10	50V	G5	452179

Cir ref	Description	Tol%±	Rating	Grid	Part No.
DIODES					
D301	Zener	5	5V1 400mW	K8	33928
D303	BAT 85 Schottky		30V 100mA	F8	454507
D304	BAT 85 Schottky		30V 100mA	F9	454507
D305	Zener	5	5V1 400mW	G10	33928
D307	Zener	5	5V1 400mW	F6	33928
D308	1N4148		75V 150mA	H7	23802
D309	1N4148		75V 150mA	K7	23802
D311	1N4148		75V 150mA	H9	23802
D312	1N4148		75V 150mA	J9	23802
TRANSISTORS					
Q301	2N3904			H9	24146
Q302	2N3904			J9	24146
Q303	2N3904			J9	24146
Q304	MPS2369			H9	36625
Q308	MPS2369			J9	36625
Q312	2N3904			H7	24146
Q313	2N3904			J7	24146
Q314	2N3904			J7	24146
Q315	MPS2369			H7	36625
Q319	MPS2369			J7	36625
Q322	BC547B			G10	44951
Q323	BC547B			H8	44951
Q324	2N3906			F6	21533
Q325	2N3906			J7	21533
Q326	2N3906			J7	21533
Q327	2N3906			H9	21533
Q328	2N3906			J9	21533
INTEGRATED CIRCUITS					
U301	MS1007A CCD			J8	456619
U302	LF351N			G10	40130
U303	LF351N			G6	40130
U304	LF351N			F6	40130
U305	10216			H5	39903
U306	74HC374			F7	451728
U307	DAC-08AH			G7	450686
U308	74HC373			F8	452559
U309	DAC-08AH			G8	450686
U310	Variable Reg Posi tive		100mA	F10	457229
U311	MC34080P			G9	456721
U312	MC10319			F9	457017
U313	Variable Reg Neg ative		100mA	F10	455012
U314	DAC-08AH			G7	450686
CONNECTORS					
SKA	96 Way DIN 41612 Type C			F5	453848
MISCELLANEOUS					
L301	10uH Choke	10	¼W	H8	455739
L306	0.27uH Choke	10	¼W	J5	455738
L307	0.27uH Choke	10	¼W	J6	455738
L308	0.27uH Choke	10	¼W	J5	455738
L309	0.27uH Choke	10	¼W	J5	455738

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ACQUISITION AND CCD - PART OF 400 MAIN BOARD (Cont)

Cir ref	*Description*	*Tol%±*	*Rating*	*Grid*	*Part No.*
P300	Mini component solder pin x2	carrier		J8	36207
P301	Mini component solder pin x2	carrier		J8	36207
TP4	Wire 0.045"square brass tin plated			G6	43355

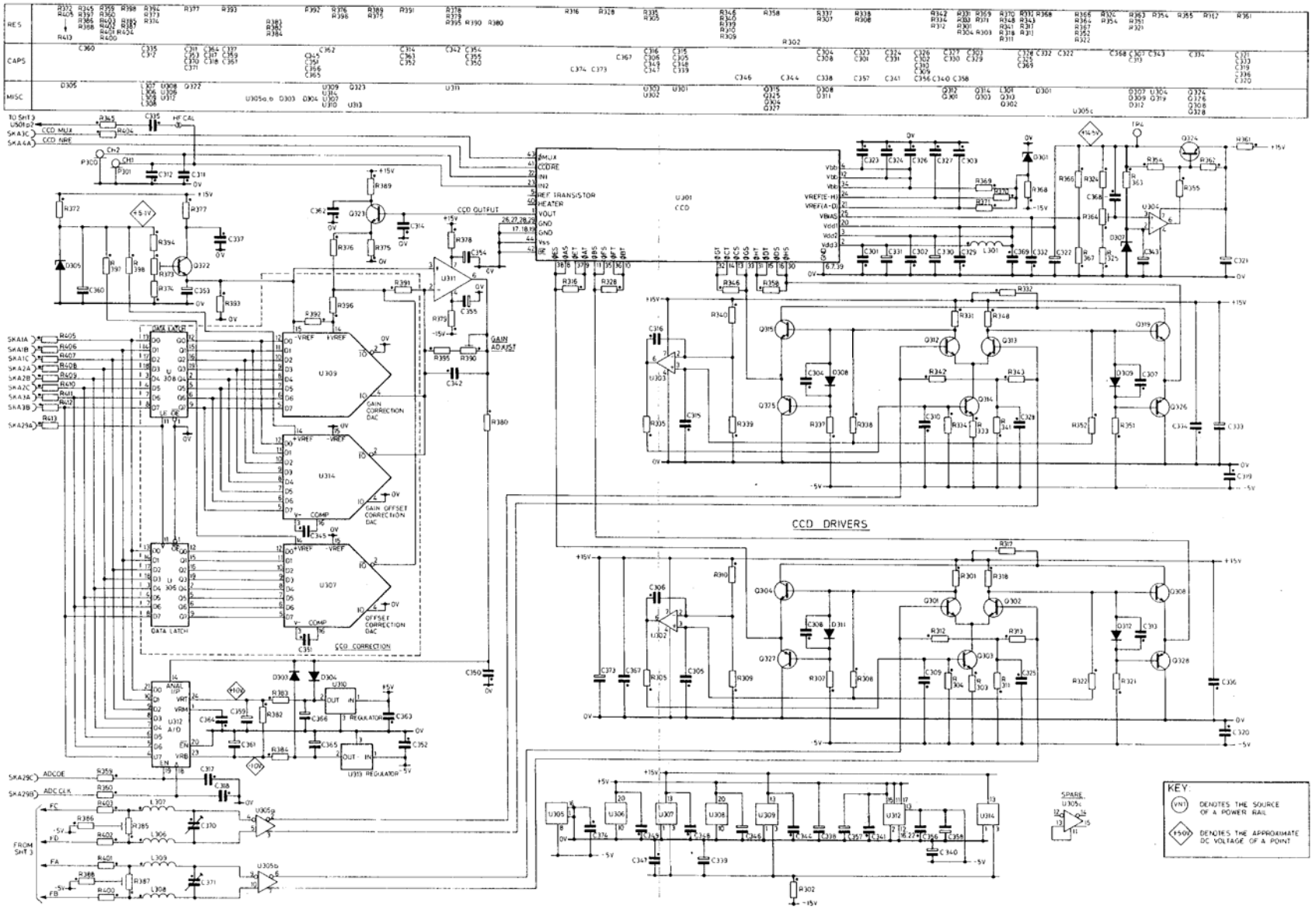


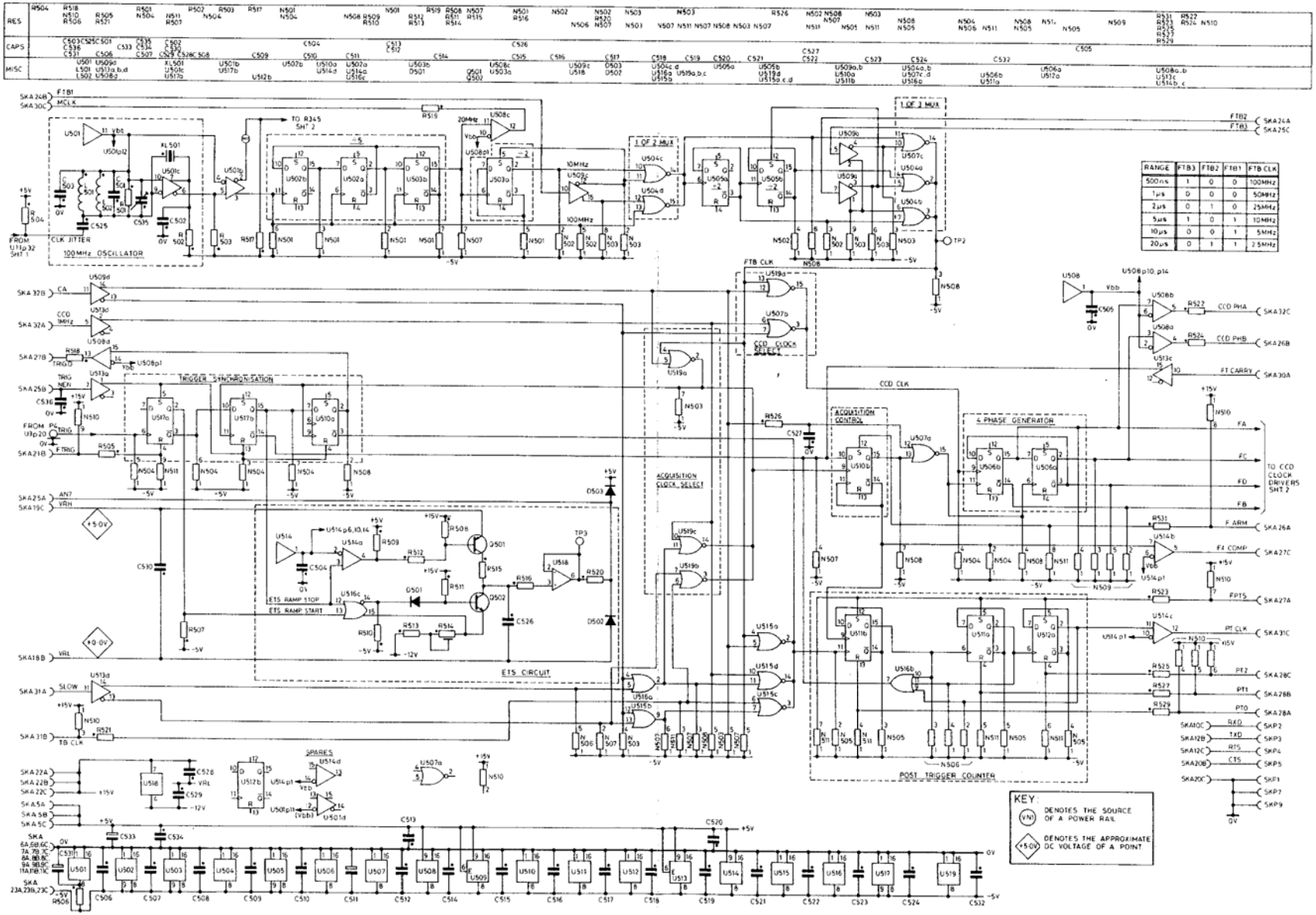
Fig. 6.7 Acquisition (CCD) circuit diagram

ECL CIRCUIT - PART OF 400 MAIN BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R501	10K	5	⅛W	L2	44235
R502	330R	5	⅛W	L3	44220
R503	330R	5	⅛W	L3	44220
R504	100K	5	⅛W	M2	44246
R505	1K5	5	⅛W	F2	44228
R506	10R	5	⅛W	L3	43138
R507	470R	5	⅛W	G4	44222
R508	470K	5	⅛W	G3	44254
R509	820R	5	⅛W	G2	44225
R510	330R	5	⅛W	G4	44220
R511	4K7	5	⅛W	F4	44232
R512	22K	5	⅛W	G2	44238
R513	390R	5	⅛W	F4	44221
R514	220R Pot	20	⅓W	G4	455933
R515	56K	5	⅛W	G3	44243
R516	10K	5	⅛W	F3	44235
R517	470R	5	⅛W	L3	44222
R518	220R	1	¼W	K2	455412
R519	220R	1	¼W	K3	455412
R520	470R	5	⅛W	F4	44222
R521	1K5	5	⅛W	F2	44228
R522	220R	1	¼W	H3	455412
R523	1K5	5	⅛W	F2	44228
R524	220R	1	¼W	G3	455412
R525	1K5	5	⅛W	F2	44228
R526	100R	5	⅛W	K2	43150
R527	1K5	5	⅛W	F2	44228
R529	1K5	5	⅛W	F2	44228
R531	1K5	5	⅛W	F2	44228
RESISTOR NETWORKS					
N501	560R × 6	5	⅛W	L4	453788
N502	560R × 4	5	⅛W	K2	451135
N503	560R × 8	5	⅛W	J2	39258
N504	560R × 6	5	⅛W	J4	453788
N505	560R × 4	5	⅛W	H3	451135
N506	560R × 4	5	⅛W	G4	451135
N507	560R × 6	5	⅛W	J3	453788
N508	560R × 6	5	⅛W	K4	453788
N509	560R × 4	5	⅛W	K5	451135
N510	4K7 × 8	5	⅛W	F2	39255
N511	1K2 × 8	5	⅛W	G2	44877
CAPACITORS					
C501	15pF Cer	10	50V	L2	452145
C502	10pF Cer	10	50V	L3	452143
C503	10nF Cer	10	50V	L2	452179
C504	10nF Cer	10	50V	H2	452179
C505	10nF Cer	10	50V	K3	452179
C506	10nF Cer	10	50V	L3	452179
C507	10nF Cer	10	50V	L4	452179
C508	10nF Cer	10	50V	K4	452179
C509	10nF Cer	10	50V	J2	452179
C510	10nF Cer	10	50V	J2	452179
C511	10uF Tant	20	16V	J4	457212
C512	10nF Cer	10	50V	J4	452179
C513	10nF Cer	10	50V	J3	452179
C514	10nF Cer	10	50V	K2	452179
C515	10nF Cer	10	50V	H2	452179
C516	10nF Cer	10	50V	H4	452179
C517	10nF Cer	10	50V	G3	452179
C518	10nF Cer	10	50V	G2	452179
C519	10nF Cer	10	50V	K2	452179
C520	10nF Cer	10	50V	G2	452179
C521	10nF Cer	10	50V	G2	452179
C522	10nF Cer	10	50V	H3	452179
C523	10nF Cer	10	50V	F4	452179
C524	10nF Cer	10	50V	H4	452179
C525	1pF Cer	+/-0.5pF	50V	L2	452131
C526	47pF	2½	63V	F3	35910
C527	100pF	Cer 10	50V	K2	452155
C528	10nF Cer	10	50V	F4	452179
C529	10nF Cer	10	50V	F4	452179
C530	100nF	+80/-20	50V	F3	43498
C531	10uF Tant	20	16V	K2	457212
C532	100nF	+80/-20	50V	J3	43498
C533	10000uF E	20	10V	G5	457863
C534	100nF	20	50V	F5	456932
C535	1-2-10pF Trimmer			M1	451127
C536	47pF	10	50V	J1	452151
DIODES					
D501	1N4148		75V 150mA	G3	23802
D502	BAT85 Schottky		30V 100mA	F4	454507
D503	BAT85 Schottky		30V 100mA	F3	454507
TRANSISTORS					
Q501	MPS3640			G3	39323
Q502	MPS-H10 or FTR 174			G3	38411
INTEGRATED CIRCUITS					
U501	10216			L2	39903
U502	10231			L3	39247
U503	10231			L4	39247
U504	10102			K2	39243
U505	10131			K1	39246
U506	10131			K4	39246
U507	10102			K4	39243
U508	10125			K3	39245
U509	10124			H2	44366
U510	10231			H3	39247
U511	10231			G3	39247
U512	10231			G2	39247
U513	10124			H1	44366
U514	10125			G2	39245
U515	10102			H3	39243
U516	10105			G4	452076
U517	10H131			H4	451817
U518	LF351N			F3	40130
U519	10102			K3	39243

ECL CIRCUIT - PART OF 400 MAIN BOARD (Cont)

Cir ref	*Description*	*Tol%±*	*Rating*	*Grid*	*Part No.*
CONNECTORS					
SKA	96 Way DIN 41612 Type C			F5	453848
SKP	25 Way D Type	Right	angle	A5	457618
MISCELLANEOUS					
XL501	100MHz Crystal		+/-50ppm	L1	457913
L501	0.27uH Choke	10	¼W	L2	455738
L502	0.27uH Choke	10	¼W	L1	455738
P4	Mini component solder pin x2	carrier		J5	36207
TP2	Wire 0.045" square brass tin plate			K4	43355
TP3	Wire 0.045" square brass tin plate			F3	43355



RANGE	FTB3	FTB2	FTB1	FTB CLK
500ns	1	0	0	100MHz
1µs	0	0	0	50MHz
2µs	0	1	0	25MHz
5µs	1	0	1	10MHz
10µs	0	0	1	5MHz
20µs	0	1	1	2.5MHz

Fig. 6.8 ECL circuit diagram

POWER SUPPLY - PART OF 400 MAIN BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R601	100K	5	⅛W	C8	44246
R602	6K8	5	⅛W	C9	43245
R603	47K	5	⅛W	C9	44242
R604	10K	5	⅛W	D9	44235
R605	4K7	5	⅛W	B10	44232
R606	1K5	5	¼W	B8	21801
R607	22K	5	⅛W	A9	44238
R608	10R	5	⅛W	A9	43138
R609	3K6	1	¼W	C8	455441
R610	1K	1	¼W	C8	455428
R611	5K6	5	¼W	B8	21806
R612	8M2	5	½W 3kV	---	452027
R613	8M2	5	½W 3kV	---	452027
R614	2K2	5	2W	D8	456802
R615	1K	5	⅛W	D9	44226
R616	100K	5	⅛W	B8	44246
R617	33R	5	¼W	C10	28712
R618	56K	5	⅛W	B7	44243
R619	1K1	1	¼W	C8	455429
R620	4K7	5	⅛W	A8	44232
R621	470R Pot	20	⅓W	C8	455934
CAPACITORS					
C601	10nF	10	50V	D9	452179
C602	10nF	10	50V	C8	452179
C603	5.6nF	10	50V	C8	452176
C604	100nF	+80/-20	50V	D9	43498
C605	47uF E	+50/-10	16V	C10	453376
C606	100pF	10	50V	D9	452155
C607	47 uF E	20	25V	C8	457013
C608	10000uF E	20	40V	B9	457785
C609	10nF	+40/-20	250V	B10	22395
C610	100nF	+80/-20	50V	B10	43498
C611	470uF		25V	D10	455705
C612	470uF		25V	D10	455705
C613	47uF E	20	25V	D8	457013
C614	1000uF		10V	E10	455702
C615	47uF E	20	25V	D8	457013
C616	1000uF		10V	E11	455702
C617	47uF E	20	25V	E8	457013
C618	470uF		25V	D11	455705
C619	47uF E	20	25V	E8	457013
C620	100nF	10	250V	D8	39199
C621	47uF E	+50/-10	40V	A8	32188
C622	100nF	+80/-20	50V	C7	43498

Cir ref	Description	Tol%±	Rating	Grid	Part No.
DIODES					
D602	MR750		50V 6A	A2	456783
D603	Zener	5	15V 400mW	B8	33939
D605	1N4148		75V 150mA	D9	23802
D606	MUR405		50V 4A	C10	456705
D607	EGP20A		50V 2A	D10	456785
D608	SB340 Schottky		40V 3A	C11	456786
D609	EGP20A		50V 2A	D11	456785
D610	1N4148		75V 150mA	C8	23802
D611	1S923		200V .25A	D10	3560
D612	1N4148		75V 150mA	D9	23802
BRIDGE RECTIFIERS					
BR601	BY225-100		100V 5A	A8	451943
TRANSISTORS					
Q601	BC547B			C8	44951
Q602	IRF540		100V	A10	456576
Q603	BC547B			C9	44951
INTEGRATED CIRCUITS					
U601	UC3843N			D9	456577
CONNECTORS					
PLE	4 Way 0.1" locking header			B8	457892
PLF	0.25" Terminal Blade			B2	454048
PLG	6 Way 0.1" locking header			D8	457893
PLH	2 Way 0.1" locking header			D10	41391
PLR1	0.25" Spade Terminal			A4	456928
PLR2	0.25" Spade Terminal			A3	456928
SKA	96 Way DIN 41612 Type C			F5	453848
SKM	IEC Input socket, Filter and Fuse Holder			---	456312
MISCELLANEOUS					
FS601	Fuse (see section 1.7)		0.5A	---	457452
FS602	Fuse 20mm (see section 1.7)		5A	B3	457979
L601	4.7uH		2A	D9	457784
L602	4.7uH		2A	D9	457784
L603	4.7uH		2A	E9	457784
L604	4.7uH		2A	E9	457784
L605	1uH 5mR		7A	B8	456711
S1	On/Off Switch			---	456700
T601	Mains Input Transformer		24V	---	458264
T602	Inductor Flyback Converter			B11	456612

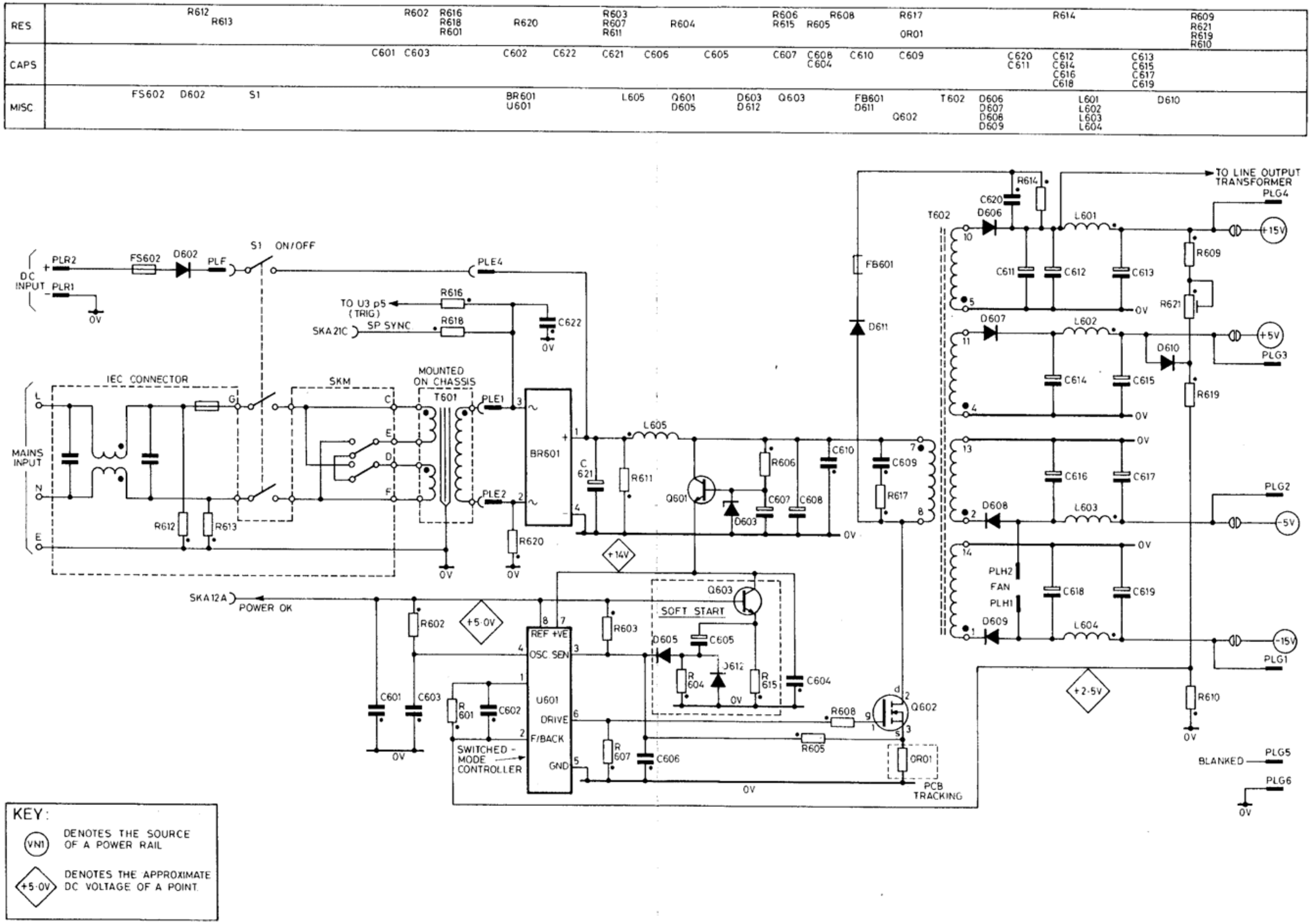


Fig. 6.9 Power supply circuit diagram

VIDEO - PART OF 400 MAIN BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R701	75K	1	¼W	C4	455473
R702	75K	1	¼W	D4	455473
R703	390R	5	⅛W	B3	44221
R704	1M	5	⅛W	D3	44258
R705	82K	5	⅛W	D5	44245
R706	470R Pot	20	⅓W	C3	455934
R707	1K2	5	⅛W	C3	44227
R708	100K	5	⅛W	D5	44246
R709	100K Pot	20	⅓W	C5	455941
R710	100R	5	⅛W	C4	43150
R711	100R	5	⅛W	B4	43150
R712	2K	1	¼W	D4	455435
R713	1K	1	¼W	D4	455428
R714	330R	5	⅛W	D5	44220
R715	100K	5	⅛W	C5	44246
R716	390K	5	⅛W	C4	44253
R717	4R7	1	¼W	C4	457037
R718	50R Pot	10	½W	C2	42155
R719	10K	5	⅛W	D2	44235
R720	3K	1	¼W	C3	455439
R721	1K5	5	⅛W	D3	44228
R722	750R	1	¼W	D3	455425
R723	2K4	1	¼W	D3	455437
R724	1K2	5	⅛W	C3	44227
R725	4K7	5	⅛W	C3	44232
R726	3K	1	¼W	C3	455439
R727	1K5	5	⅛W	C3	44228
R728	750R	1	¼W	C3	455425
R729	2K7	5	⅛W	B4	44230
R730	10K	5	⅛W	D2	44235
R731	4K7	5	⅛W	C3	44232
R732	2K2	5	⅛W	C3	43357
R733	2K2	5	⅛W	C3	43357
R734	100K Pot	20	⅓W	B4	455941
R735	2K2 Pot	20	⅓W	B4	455936
R736	1K5	5	⅛W	B4	44228
R737	100R	5	⅛W	B3	43150
R738	1K	5	⅛W	B3	44226
R739	1K2	5	⅛W	E2	44227
R740	1K	5	⅛W	E3	44226
R741	10K Pot	20	⅓W	D3	455938
R742	8K2	1	¼W	E3	455450
R743	47K	5	⅛W	C7	44242
R744	470R	5	⅛W	B6	44222
R745	500K Pot	10	½W500V	C5	457012
R746	220R Pot	20	⅓W	D5	455933
R747	1K	5	⅛W	C7	44226
R748	2K2	5	¼W	B5	21802
R749	27R	5	⅛W	C7	43143
R750	100R	5	⅛W	C2	43150
R751	150K	5	⅛W	C5	44248
R752	33K	5	⅛W	D4	44240
R753	1R	5	¼W	D8	457028
R754	2K2	5	⅛W	A7	43357
R755	4K7	5	⅛W	E3	44232
R756	4K7	5	⅛W	E2	44232
R757	4K7	5	⅛W	E2	44232
R758	4K7	5	⅛W	E2	44232
R759	1K2	5	⅛W	D2	44227
R760	470R	5	⅛W	E4	44222
R761	4K7	5	⅛W	E3	44232
R762	10K	5	⅛W	B2	44235
R763	10K	5	⅛W	B2	44235
R820	220R	5	¼W	---	21796
R821	10K	5	¼W	---	21809
CAPACITORS					
C702	22nF	20	50V	D3	42445
C703	100nF	+80/-20	50V	D6	43498
C704	47uF E	+50/-10	16V	B3	453376
C705	47uF E	+50/-10	16V	D4	453376
C706	470nF	10	63V	C4	39181
C707	100nF	+80/-20	50V	D5	43498
C710	10uF E	+50/-10	25V	E2	32180
C711	2.2uF	20	100V	B4	452245
C712	1nF	10	50V	B3	452167
C714	2.2nF	10	50	B1	452171
C715	1nF	10	50V	E3	452167
C716	1nF	10	50V	D3	452167
C717	2.2nF	10	50V	B6	452171
C718	4.7nF	5	400V	B7	457662
C719	0.02uF	+40/-20	500V	B5	53819
C720	2.2uF	20	100V	C6	452245
C721	1uF	10	100V	B7	37389
C722	10uF	+50/-10	25V	C6	32180
C723	470nF	10	63V	D5	39181
C724	10nF	10	50V	C4	452179
C725	47uF E	20	25V	E8	457013
DIODES					
D701	1N4148		75V 150mA	D2	23802
D702	1N4148		75V 150mA	C3	23802
D703	BA158		600V 0.5A	C6	456699
D704	1S923		200V 0.2A	C7	3560
D705	UF4004 or MUR140		400V 1A	D8	457783
D706	1S923		200V 250mA	D6	3560
D707	1S923		200V 250mA	D6	3560
D708	1N4148		75V 150mA	B3	23802
D709	1N4148		75V 150mA	D5	23802
D710	1N4148		75V 150mA	B2	23802
D711	1N4148		75V 150mA	D4	23802
D712	Zener	5	5V1 400mW	E2	33928
D713	1N4148		75V 150mA	B3	23802
D714	Zener	5	10V 400mW	D5	33935
D715	1N4148		75V 150mA	D3	23802

VIDEO - PART OF 400 MAIN BOARD (Cont)

Cir ref	Description	Tol%±	Rating	Grid	Part No.
DIODES (Cont)					
D716	1N4148		75V 150mA	D2	23802
D717	1N4148		75V 150mA	D2	23802
D718	1N4148		75V 150mA	D2	23802
D719	1N4148		75V 150mA	B3	23802
TRANSISTORS					
Q701	BC547B			C5	44951
Q702	2N3906			B2	21533
Q705	BC547B			C3	44951
Q706	BC547B			C3	44951
Q707	BC547B			C3	44951
Q708	BC449			B4	42131
Q709	BC450			B4	42130
Q710	BC449			B5	42131
Q711	BC449			B4	42131
Q712	U1898			D4	456615
Q713	2N3906			B4	21533
Q715	BC547B			B7	44951
Q716	IRF740		400V 10A	A7	457787

Cir ref	Description	Tol%±	Rating	Grid	Part No.
INTEGRATED CIRCUITS					
U701	L272			D4	457205
U702	MM5481			C2	456696
U703	74HC4538			E3	457168
CONNECTORS					
PLC	7 way locking header			B5	457718
PLD	5 way locking header			C4	457717
SKA	96 Way DIN 41612 Type C			F5	453848
SKD	5 way IDC header			---	456689
MISCELLANEOUS					
L701	Raster Scan Lin Coil			B5	456693
L702	Raster Scan Height Coil			B6	456692
L703	Raster Scan Shift Coil 1.6mH		100mA	C5	458032
L704	Vertical and Horizontal		Yoke	---	456690
L705	10uH Choke	10	¼W	B4	455739
T701	LOPT			E6	458301

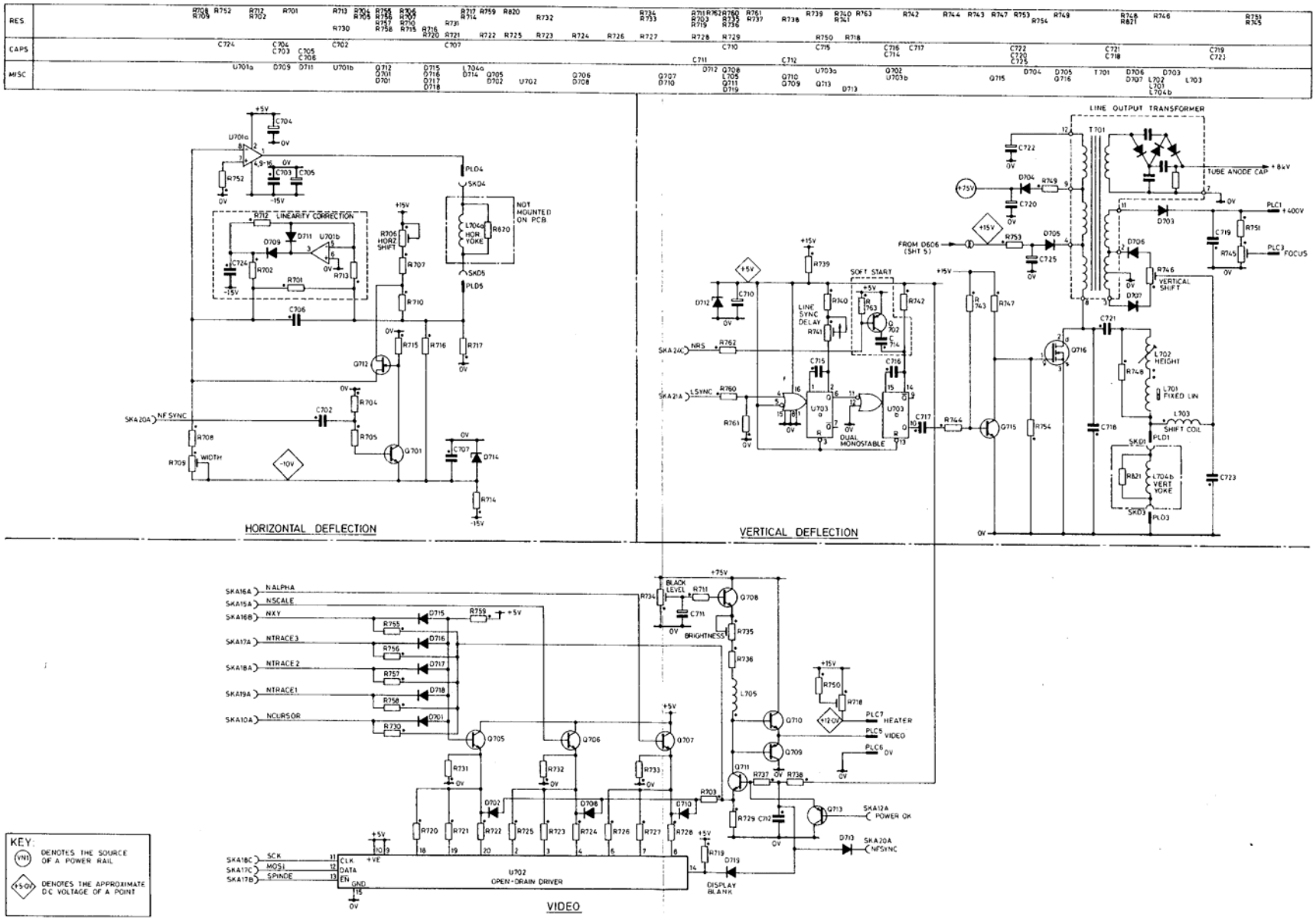


Fig. 6.10 Video and deflection circuit diagram

400 CPU BOARD

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R1	1K	5	⅛W	C10	44226
R2	1K	5	⅛W	B9	44226
R4	10K	5	⅛W	D9	44235
R5	10K	5	⅛W	D9	44235
R6	10K	5	⅛W	D9	44235
R7	220R	5	⅛W	C9	43359
R8	220R	5	⅛W	D10	43359
R9	220R	5	⅛W	D10	43359
R10	470K	5	⅛W	E9	44254
R11	220K	5	⅛W	E9	44250
R12	4K7	5	⅛W	B10	44232
R13	5K6	5	⅛W	B10	44233
R14	10K Pot	20	⅓W	B10	455938
R15	4K7	5	⅛W	B10	44232
R18	3K3	5	⅛W	D3	43358
R19	680R	5	⅛W	B10	44224
R21	270R	5	⅛W	B10	43716
R22	10K	5	⅛W	A2	44235
R23	470K	5	⅛W	C2	44254
R24	10K	5	⅛W	C10	44235
R25	33K	5	⅛W	C10	44240
R26	33K	5	⅛W	C10	44240
R27	33K	5	⅛W	C10	44240
R28	33K	5	⅛W	C10	44240
R29	33K	5	⅛W	C10	44240
R30	33K	5	⅛W	C10	44240
R31	33K	5	⅛W	C10	44240
R33	22K	5	⅛W	D9	44238
R34	390R	5	⅛W	D2	44221
R35	4K7	5	⅛W	C3	44232
R36	12K	5	⅛W	D9	43246
R37	4K7	5	⅛W	A8	44232
R38	4K7	5	⅛W	C3	44232
R39	4K7	5	⅛W	A9	44232
R40	560R	5	⅛W	A9	44223
R41	4K7	5	⅛W	B10	44232
R42	560R	5	⅛W	C10	44223
R43	4K7	5	⅛W	C10	44232
R44	560R	5	⅛W	C10	44223
R45	22K	5	⅛W	C8	44238
RESISTOR NETWORKS					
N1	2K2 × 4 SIL	5	⅛W	D10	455593
CAPACITORS					
C1	10nF	10	50V	C6	452179
C2	10nF	10	50V	B1	452179
C3	10nF	10	50V	B8	452179
C4	10nF	10	50V	B5	452179
C5	10nF	10	50V	D10	452179
C6	10nF	10	50V	B3	452179
C7	10nF	10	50V	D8	452179
C8	10nF	10	50V	C8	452179
C9	10nF	10	50V	C7	452179
C10	10nF	10	50V	C5	452179
C11	10nF	10	50V	D8	452179
C12	22pF	10	50V	C9	452147
C13	22pF	10	50V	C9	452147
C14	100nF	+80/-20	50V	B9	43498
C15	22pF	10	50V	C10	452147
C16	10nF	10	50V	B10	452179
C17	47uF E	+50/-10	16V	D4	453376
C18	47uF E	+50/-10	16V	D4	453376
C19	10nF	10	50V	C9	452179
C20	2.2nF	10	50V	C10	452171
C21	100nF	+80/-20	50V	C10	43498
C22	100nF	+80/-20	50V	C10	43498
C23	100nF	+80/-20	50V	C10	43498
C24	100nF	+80/-20	50V	C10	43498
C25	100nF	+80/-20	50V	C10	43498
C26	100nF	+80/-20	50V	C10	43498
C27	100nF	+80/-20	50V	C10	43498
C28	10uF E	+50/-10	25V	B10	32180
C29	47uF E	20	25V	B9	457013
C30	10nF	10	50V	B9	452179
C31	1uF Tant	20	35V	D3	34895
C32	1nF	10	50V	C1	452167
C33	100nF	+80/-20	50V	D8	43498
C34	10nF	10	50V	B7	452179
C35	100pF	10	50V	C8	452155
C36	10uF Tant	20	10V	C3	52938
DIODES					
D1	Zener	5	4V7 400mW	C2	33927
D2	1N4148		75V 150mA	E8	23802
D3	1N4148		75V 150mA	A8	23802
D4	1N4148		75V 150mA	A9	23802
D5	1N4148		75V 150mA	C2	23802
D6	1N4148		75V 150mA	C8	23802
D7	1N4148		75V 150mA	B8	23802
D8	BAT85 Schottky		30V 100mA		454507
TRANSISTORS					
Q1	BC547B			D9	44951
Q2	BC547B			C3	44951
Q3	BC547B			E8	44951
INTEGRATED CIRCUITS					
U1	MC68HC11AOFN			B9	456702
U2	27C512 (test RAM not fitted)			B5	456704
U3	27C512			B6	456704
U4	27C512			B7	456704
U8	32K × 8 Static RAM (70ns)			C4	456736
U9	74HC573			A8	456735
U10	74HC138			C7	452561
U11	74AC541			A4	457221
U12	74AC541			A5	457221
U13	74HC574			D6	455065
U14	74HC574			D7	455065
U15	74HC574 (Not fitted)			D6	455065
U16	74HC365 (Not fitted)			A9	456697
U17	74HC4046			B10	457167
U18	74HC541			D7	455601
U19	74HC00			C5	451956
U20	74HC00			C6	451956

400 CPU BOARD (Cont)

Cir ref	Description	Tol%±	Rating	Grid	Part No.
INTEGRATED CIRCUITS (Cont)					
U21	74HC14			E9	453961
U22	26LS29			C8	453501
U23	26LS32			D10	453502
U24	400 Gate Array assembly			B2	456703
U25	Voltage Reg		5V 100mA	B9	40406
SWITCHES					
S1	4 Way change over DIL			E10	457612
CONNECTORS					
PLA	96 Way DIN 41612	Type C		E5	453847
PLB	26 Way Header			D10	43952
SKD	Not fitted			D5	------
MISCELLANEOUS					
B1	NiCad		3V6 0.1AH	D2	455604
LK16	Jumper link			D2	453877
LK16	2 way 0.1" header			D2	457908

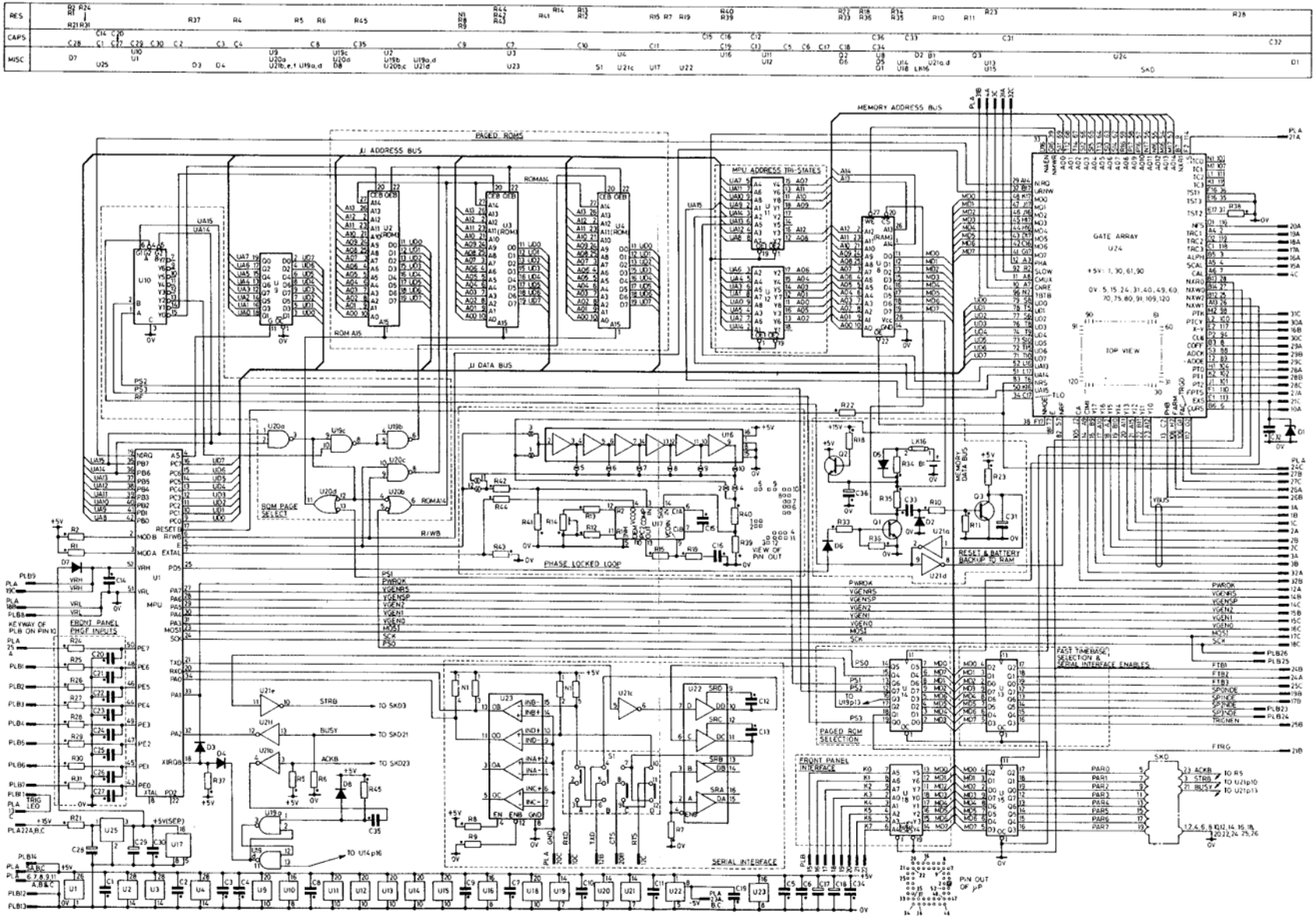


Fig. 6.11.1 CPU board circuit diagram

GATE ARRAY PINOUT

Pin No.	*Description*	*Pin No.*	*Description*
1	+5V	56	A011
2	TRC1 (NTRACE 1)	57	A010
3	ALPH (NALPHA)	58	A09
4	SCAL (NSCALE)	59	A08
5	0V	60	0V
6	CURS (NCURSOR)	61	+5V
7	CAL	62	A07
8	COFF (COFFSET)	63	A06
9	NXR1	64	A05
10	CNRE (CCD NRE)	65	A04
11	CMUX (CCD MUX)	66	A03
12	PHA (CCD PHA)	67	A02
13	PHB (CCD PHB)	68	A01
14	CIMI (CCD 1MHz)	69	A00
15	0V	70	0V
16	YI7 (YBUS7)	71	UD7
17	YI6 (YBUS6)	72	UD6
18	YI5 (YBUS5)	73	UD5
19	YI4 (YBUS4)	74	UD4
20	YI3 (YBUS3)	75	0V
21	YI2 (YBUS2)	76	UD3
22	YI1 (YBUS1)	77	UD2
23	YI0 (YBUS0)	78	UD1
24	0V	79	UD0
25	NXW2	80	0V
26	NXW1	81	E
27	NXW0	82	NRF
28	NXR0	83	NRS
29	NIRQ	84	---
30	+5V	85	---
31	0V	86	---
32	URNW (R/WB)	87	---
33	NEAN	88	ADCK (ADC CLK)
34	TLO (not used)	89	ADOE (ADCOE)
35	TST3	90	+5V
36	TST1	91	0V
37	TST2	92	SLOW
38	NMOE	93	---
39	NMWR	94	CLK (MCLK)
40	0V	95	---
41	MD7	96	TBTB (TB CLK)
42	MD6	97	---
43	MD5	98	PTK (PT CLK)
44	MD4	99	---
45	MD3	100	PTCY (PT CARRY)
46	MD2	101	PT2
47	MD1	102	PT1
48	MD0	103	TC0 (not used)
49	0V	104	PT0
50	UA15	105	CA
51	UA14	106	FAC (FA COMP)
52	UA13	107	TC1 (not used)
53	A014	108	FARM
54	A013	109	0V
55	A012	110	FPTS

GATE ARRAY PINOUT (Cont)

Pin No.	*Description*	*Pin No.*	*Description*
111	TC2 (not used)	116	NFS (NF SYNC)
112	TRGD (TRIG.D)	117	X-Y (NX-Y)
113	EXS (SP SYNC)	118	TRC3 (NTRACE 3)
114	LS (L SYNC)	119	TRC2 (NTRACE 2)
115	TC3 (not used)	120	0V

Fig. 6.11.2 Gate Array Pinout

400 FRONT PANEL

Cir ref	Description	Tol%±	Rating	Grid	Part No.
RESISTORS					
R1	1K	5	⅛W	A3	44226
R2	1K	5	⅛W	E3	44226
R3	22R	5	⅛W	E7	43142
R11	330R	5	⅛W	E7	44220
R12	4K7 Pot	20	⅓W	A3	455937
R13	4K7 Pot	20	⅓W	E3	456284
R14	1R	5	¼W	E4	457028
R15	1R	5	¼W	A2	457028
NOTE: *All other Resistors are part of carbon screen*					
RESISTOR NETWORKS					
N1	22K × 8 SIL	5	⅛W	E7	457605
CAPACITORS					
C1	47uF E	20	25V	A4	457013
C2	47uF E	20	25V	D4	457013
C3	1.5nF	10	50V	A6	452169
C4	1.5nF	10	50V	A6	452169
C5	1.5nF	10	50V	A6	452169
C6	1.5nF	10	50V	A7	452169
C7	1.5nF	10	50V	A5	452169
C8	1.5nF	10	50V	A5	452169
C9	1.5nF	10	50V	A5	452169
C10	1.5nF	10	50V	A6	452169
C13	1.5nF	10	50V	A3	452169
C14	1.5nF	10	50V	E4	452169
DIODES					
D1	Green Rectangular LED 6mm			E9	455498
D2	Green Rectangular LED 6mm			E9	455498
D3	Green Rectangular LED 6mm			E9	455498
D5	Green Rectangular LED 6mm			E11	455498
D6	Green Rectangular LED 6mm			A5	455498
D7	Green Rectangular LED 6mm			A5	455498
D8	Green Rectangular LED 6mm			A4	455498
D9	Green Rectangular LED 6mm			A4	455498
D10	Green Rectangular LED 6mm			A4	455498
D11	Red Rectangular LED 6mm			A3	455497
D12	Red Rectangular LED 6mm			A2	455497
D13	Red Rectangular LED 6mm			A2	455497
D14	Red Rectangular LED 6mm			C5	455497
D15	Green Rectangular LED 6mm			D6	455498
D16	Green Rectangular LED 6mm			D5	455498
D17	Green Rectangular LED 6mm			D5	455498
D18	Red Rectangular LED 6mm			D6	455497
D19	Green Rectangular LED 6mm			D5	455498
D20	Green Rectangular LED 6mm			D5	455498
D21	Red Rectangular LED 6mm			C3	455497
D22	Green Rectangular LED 6mm			D4	455498
D23	Green Rectangular LED 6mm			D4	455498
D24	Green Rectangular LED 6mm			D3	455498
D25	Red Rectangular LED 6mm			D4	455497
D26	Green Rectangular LED 6mm			D4	455498
D27	Green Rectangular LED 6mm			D3	455498
D28	Green Rectangular LED 6mm			C1	455498
D29	Green Rectangular LED 6mm			C2	455498
D30	Green Rectangular LED 6mm			C2	455498
D31	Green Rectangular LED 6mm			D2	455498
D32	Green Rectangular LED 6mm			D2	455498
D33	Green Rectangular LED 6mm			D2	455498
D34	Green Rectangular LED 6mm			D2	455498
D35	Green Rectangular LED 6mm			D2	455498
D36	Green Rectangular LED 6mm			D2	455498
D37	Green Rectangular LED 6mm			D2	455498
D38	Green Rectangular LED 6mm			D2	455498
D39	Green Rectangular LED 6mm			D2	455498
D40	Green Rectangular LED 6mm			D2	455498
D41	1N4003		200V 1A	A2	32771
INTEGRATED CIRCUITS					
U1	MM5450N			B4	456613
U2	MM5481			D3	456696

SWITCHES

NOTE: *All the switches are formed by part of the carbon screen and the conductive mat,*

CONNECTORS

PLC	Part of ribbon cable assy		453751
SKC(U3)	Set of holes in PCB to accept PLC	B6	------

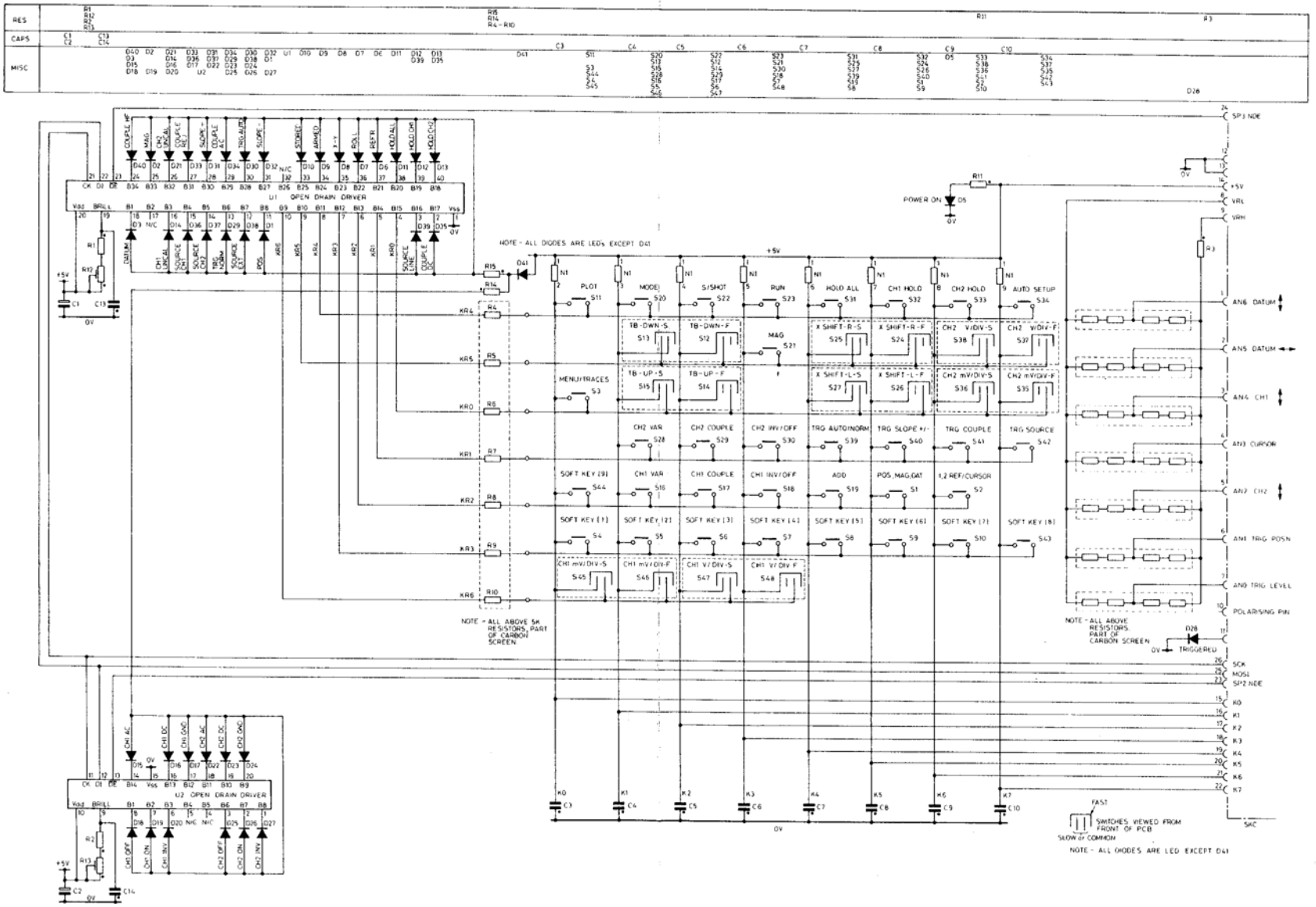


Fig 6.12 Front panel circuit diagram

400 TUBEBASE BOARD

Cir ref	*Description*	*Tol%±*	*Rating*	*Grid*	*Part No.*
RESISTORS					
R4	10K	5	½W		18552
R5	22K	5	½W		18566
R6	22K	5	½W		18566
R7	1K5	5	½W		18552
CONNECTORS					
SKC	7 Way IDC Housing				451419
SKC	Terminals				39846
	CRT socket 7 way				456689

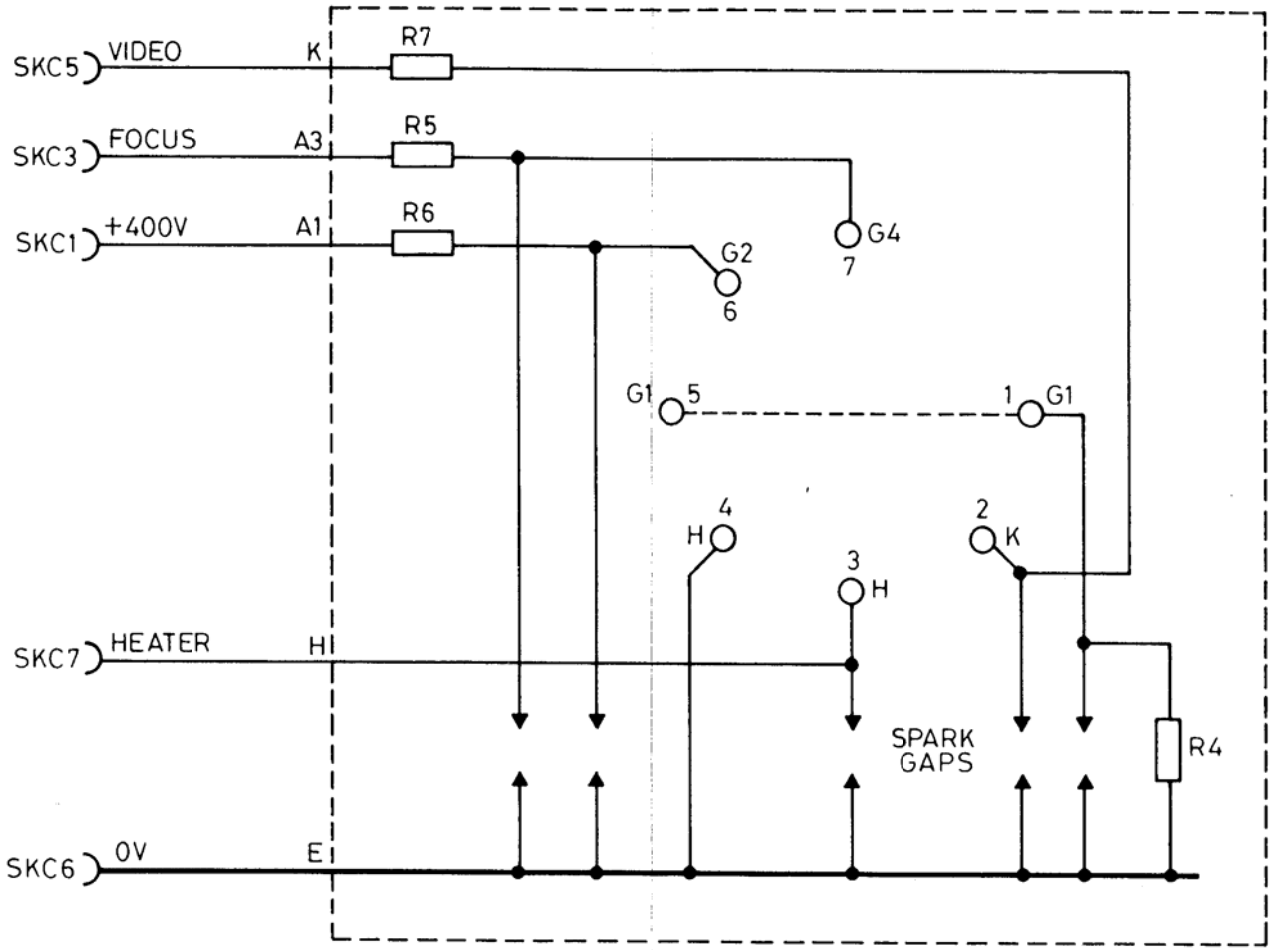


Fig 6.13 Tube base circuit diagram

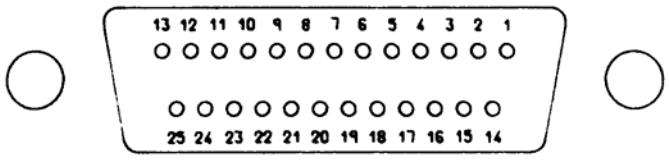


Fig 6.16 RS423 connections

No	Name	Description
1	0V	Protective Ground
2	RXD	Receive Data
3	TXD	Transmit Data
4	RTS	Request to send
5	CTS	Clear to send
7	0V	Signal Ground
9	0V	Ground

RS423 Pin Connections

7.0 MECHANICAL COMPONENTS AND EXPLODED VIEWS

This section contains mechanical views of the 400 DSO and lists all the mechanical parts not previously shown in the manual.

Comp No.	Description	Part No.
1	Filter	457374
2	Front ident coverlay	457432
3	Switch cap square on/off	457262
4	Front switch coverlay	457431
5	Actuating rod	457436
6	Tube	456695
7	Tube mounting corners	457092
8	Spring	457390
9	Front moulding	457055
10	Earthing strip (6 off)	457437
11	Screw M3 x 8 pan HD	33038
12	Tube coils (yoke)	456690
13	Screw M3 x 5 pan HD	33036
14	Front panel inner (metal)	457440
15	Conductive mat (front pcb)	457066
16	Front panel PCB assy	477820
17	Screen attenuator (main pcb)	457899
18	Coupling	457789
19	Side plate LH	457441
20	Screw No 4 x 3/5" pan HD	450460
21	Switch on/off	456700
22	Handle spacer (2 off)	457891
23	Handle	457445
24	Cross support (cpu)	457443
25	Tube base PCB assy	477740
26	Washer nylon	26857
27	Screw No 4 x 5/16" pan HD	35759
28	Screen BNC (main pcb)	457611
29	Side plate RH	457442
30	Screw M3 x 8 cisk HD	33069
31	Screen power supply (main pcb)	457897
32	Heatsink CCD	45715
33	Securing clip CCD	456378

Comp No.	Description	Part No.
34	Screw No 4 x 1/4" pan HD	455765
35	Washer M3 wavy	33016
36	Semiconductor retaining clip	457607
37	Heatsink – power supply	457609
38	Carrier	456316
39	Main PCB assy	477770
40	CPU PCB assy	477760
41	Spacer nylon	457903
42	Fan 12v brushless	456701
43	Spacer nylon	457871
44	Cableform tubebase	457424
45	Cableform scan coils	457426
46	Locknut M6	33026
47	Wavy washer M6	33019
48	Washer M6	33006
49	Transformer	458264
50	Screw M6 x 55 button HD	457118
51	Mains connector	456312
52	Rear moulding	457146
53	Nut M4	33024
54	Rear panel inner (metal)	457601
55	Washer M4	33004
56	Screw M4 x 10 pan HD	33045
57	Knurled nut M5	458279
58	Stepped washer M5	458280
59	Case	457439
60	Rear warning coverlay	457439
61	Rear socket coverlay	457433
62	Rear rating coverlay	457435
63	Switch cap small light grey (31 off)	457313
64	Switch cap large light grey (16 off)	457099
65	Switch cap large dark grey (6 off)	457100
66	Switch cap small blue	457314
67	Screw M4 x 16 pan HD	33047
68	Foot rubber	457447

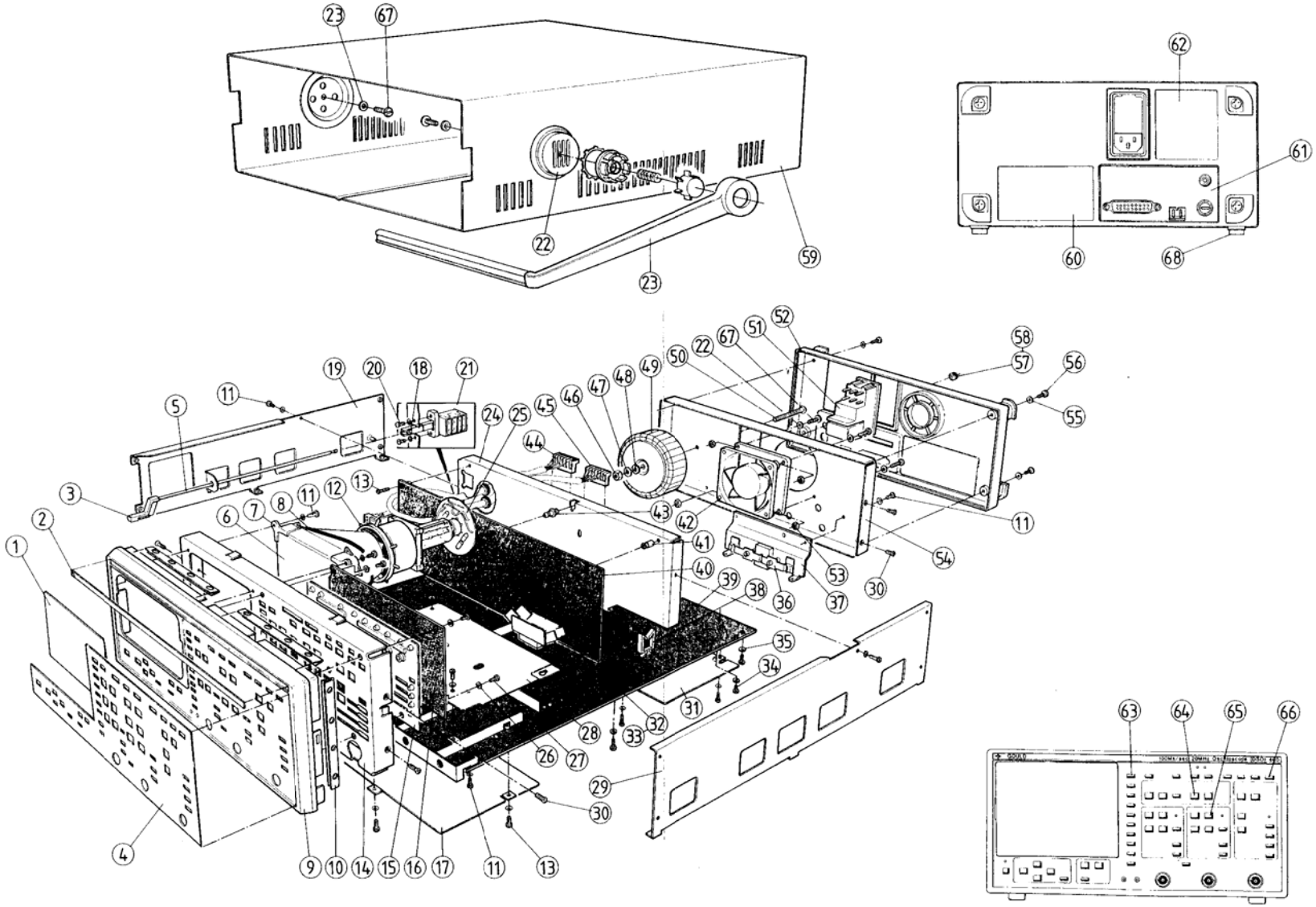


Fig 7.1 Exploded view

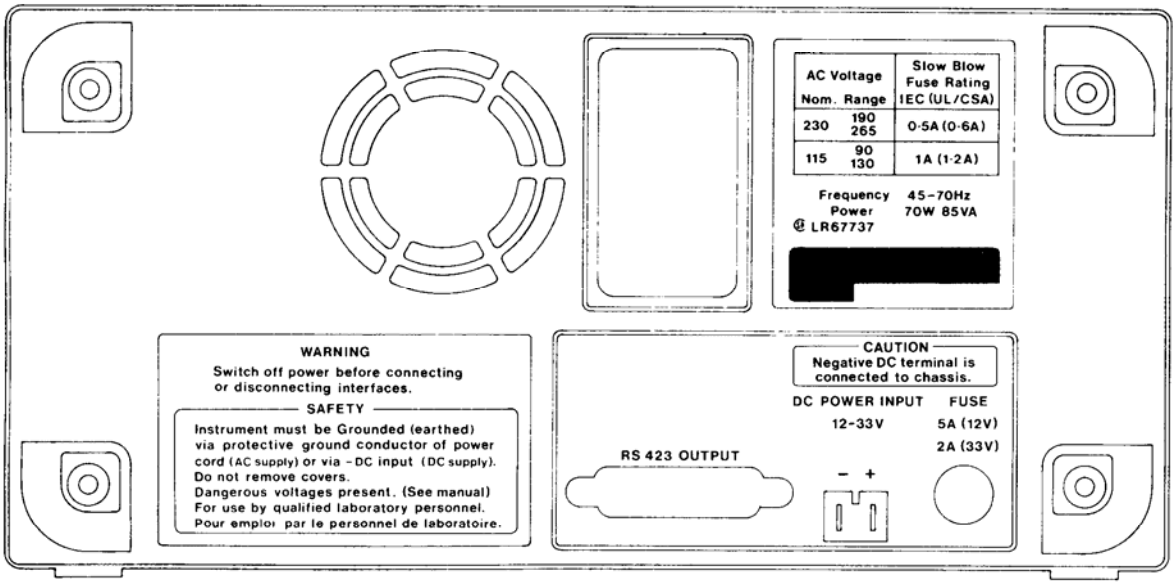


Fig. 7.2 Rear view

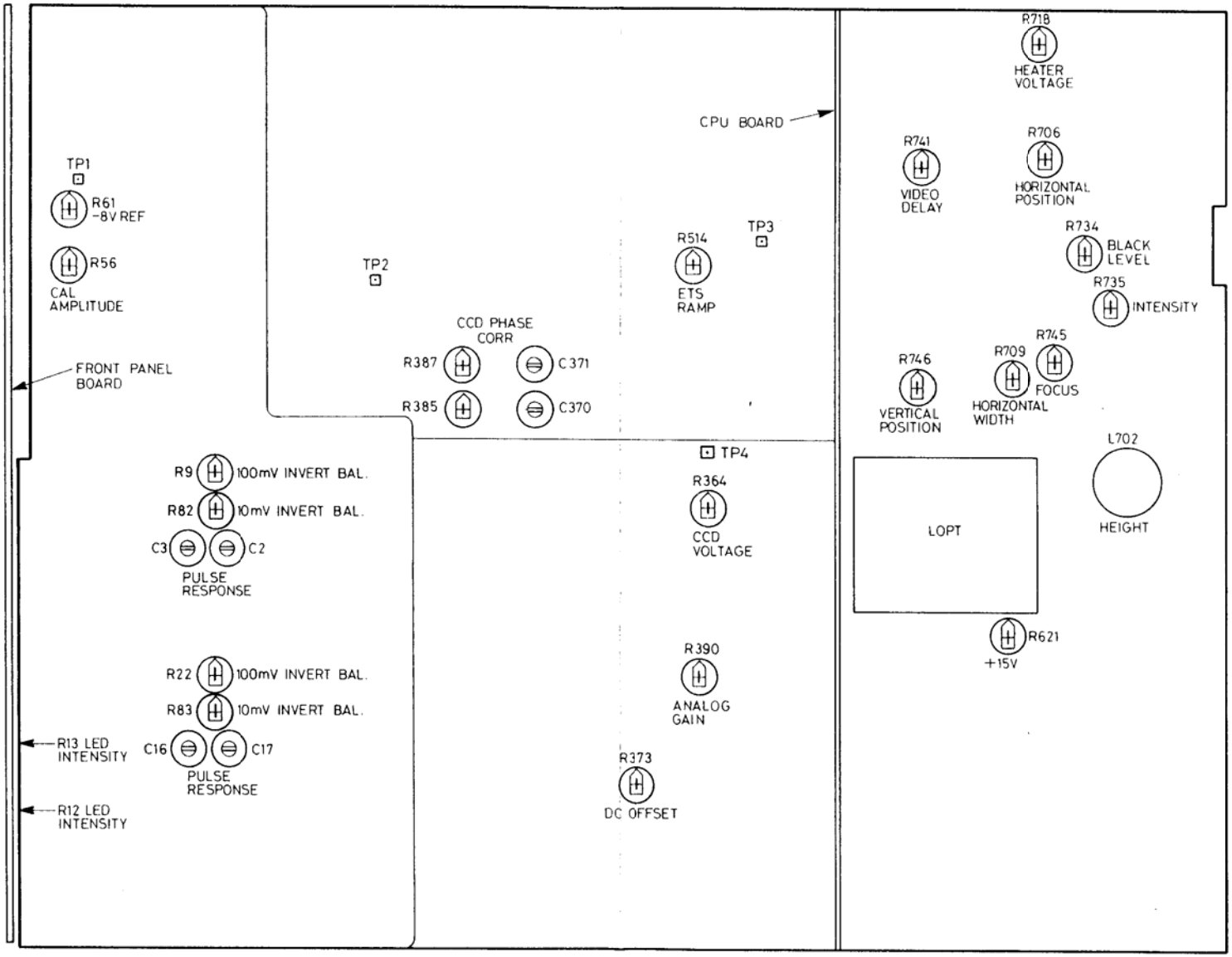


Fig 7.3 Calibration adjustment layout

8.0 SUMMARY OF IN-CIRCUIT MEASUREMENTS

The measurements given below are a compilation of those given in the circuit descriptions, are typical values.

Input Attenuator

U11 pin 38	0V	range 200mV to 5V/div
U11 pin 38	+5V	range 2mV to 100mV/div
U11 pin 38	+5V	input switched to ground
U11 pin 39	+5V	range 200mV to 5V/div
U11 pin 39	0V	range 2mV to 100mV/div
U11 pin 39	+5V	input switched to ground
U11 pin 40	0V	range 200mV to 5V/div
U11 pin 40	+5V	range 2mV to 100mV
U11 pin 40	+5V	input switched to ground

Attenuator control

U11 pins	0V	R1 energized and contacts closed

Custom preamp/attenuator

VN3	−8V
VN1	−8V
VN2	−8V
VP1	+12V
VP2	+12V
VP3	+12V
VP4	+5V

VGEN

U5 pin 11	squarewave 8ms 5V pk-pk	
U5 pin 10	suarewave 16ms 5V pk-pk	
U5 pin 9	squarewave 32ms 5V pk-pk	
U6b pin 8	0V	trace off top of screen
U6b pin 8	−4V	trace mid screen
U6b pin 8	−8V	trace off bottom of screen
U6d pin 14	0V	variable gain X1
U6d pin 14	−7V	variable gain X0.4
U7c pin 7	−4V	typically
U7d pin 8	0V	trigger level maximum below trace
U7d pin 8	−4V	trigger level mid trace
U7d pin 8	−8V	trigger level maximum above trace
U7a pin 1	−8V	

−8V reference

U9b pin 5	−6.2V	typically
U9b pin 6	−6.2V	typically
U9b pin 7	−8V	

Probe calibrator

U9a pin 2	0V	
Q18 base	squarewave 1KHz 3V pk-pk on 2V pedestal	
U9a pin 1	+4V	

CCD and Supplies

U301 pin 4, 12 and 34	−5.6V	typically
U301 pin 24	+0.5V	typically
U301 pin 21	+0.5V	typically
U301 pin 25	+1.8V	typically
U301 pins 2, 3 and 20	+14.5V	

CCD Drivers

U305b pin 2	pulses 1V pk-pk on −1V pedestal. Period dependent on timebase
U305b pin 3	pulses 1V pk-pk on −1V pedestal. Period dependent on timebase
Q315 emitter	pulses 12V pk-pk period dependent on timebase

CCD Correction

U311 pin 3	3V
Q323 base	Multiplexed signal of trace 1 and 2DC level typically 3V with traces at centre of screen
U311 pin 6	multiplexed signal of trace 1 and 2 0V equivalent to centre of screen

Vertical ADc

U310 pin 2	+1.2V
U313 pin 2	−1.2V
U312 pin 18	Clock pulses 5V pk-pk

100MHz Oscillator

U501b pin 3	100MHz Clock

Fast Timebase Generator

U501b pin 3	100MHz
U503b pin 15	20MHz
U503a pin 2	10MHz
U504c pin 14 and U504d pin 15	10 or 100MHz selected by FTB1
U505a pin 3	5 or 50MHz selected by FTB1
U505b pin 14	2.5 or 25MHz selected by FTB1
TP2	2.5, 5, 10, 25, 50 or 100MHz selected by FTB1, FTB2 and FTB3 See table 5.4.12

Trigger sync

U517a pin 3	+ve edge on trigger
U517b pin 15	+ve edge on timebase clock
U510a pin 3	+ve edge sync'd to timebase clock

Acquisition control and CCD clock select

U507b pin 7	logic 0	Timebase 50s to 50+μs/div
U507b pin 7	logic 1	Timebase 20μs to 0.1μs/div
U519d pin 15	1MHz clock	Timebase 50s to 50μs/div
U519d pin 15	see FTB	Timebase 20μs to 0.1μs/div
U519d pin 12	logic 1	Timebase 50s to 50μs/div

Post trigger counter

U516b pin 7	negative going pulse 5μs wide 20ms period Timebase 0.2 ms/div

4 phase clock generator

U506b pin 15	250 KHz clock phase A	Timebase 50s to 50μs/div
U506b pin 14	250KHz clock phase B	Timebase 50s to 50μs/div
U506a pin 2	250KHz clock phase C	Timebase 50s to 50μs/div
U506a pin 3	250KHz clock phase D	Timebase 50s to 50μs/div

Video Horizontal Deflection

C702	negative going pulse 4ms wide 5V pk-pk every 20ms
U701a pin 8	positive going pulse 0.2ms wide 0.5V pk-pk every 20ms
U701a pin 1	positive going 20ms linear ramp 6V pk-pk centered about 0V First 4ms flat with 15V negative pulse at start
R717	positive going 20ms linear ramp 2V pk-pk centered about 0V first 4ms flat
U701b pin 3	negative going 20ms linear ramp 3V pk-pk first 4 and last 7ms flat

Video Vertical Deflection

Q702 base	+5V rises from 0v at switch on
R670	positive going pulse 5V pk-pk 6μs wide every 32μs
U703b pin 10	positive going pulse 5V pk-pk 6μs wide every 32μs
Q715 collector	positive going exponential ramp 12V pk-pk
Q716 drain	positive going pulse 325V pk-pk 20μs wide every 32μs
PLD1	positive going pulse 230V pk-pk 20+s wide every 32μs

Video and brightness control

U702 pins 2, 3 and 4	0V or +5V dependent on brightness setting of graticule
U702 pins 6, 7 and 8	0V or +5V dependent on brightness setting of alphanumerics
U702 pins 18, 19 and 20	0V or +5V dependent on brightness setting of traces and cursor
U713/D719	negative going pulses 5V pk-pk 4ms wide every 20ms
Q705 base	negative going blanked trace and cursor signal 5V pk-pk
Q706 base	negative going blanked graticule 5V pk-pk
Q707 base	negative going blanked alphanumeric signal 5V pk-pk
PLC pin 5	negative going video signal 20V pk-pk on +40V pedestal

Front Panel Switches

Key Row	positive	going 5V pulse 0.5ms wide when a key is pressed
Analog signals	+2V	no PHGF switch pressed
Analog signals	+3V	appropriate 'up' PHGF witch pressed
Analog signals	+1V	appropriate 'down' PHGF switch pressed

Front Panel LEDs

U1 LED Drives	+3V	Typically with LED Off
U1 LED Drives	+1.5V	Typically with LED On
U1 pin 19	+4V	Typically

MPU

U1 pin 52	4.1V	typically

Data, address and control lines to U1 are all 0 to 5V signals

MPU clock and phase locked loop

U17 pin 4	8MHz squarewave
U17 pin 14	2MHz clock
U17 pin 3	2MHz squarewave

Battery Back up

Q2 emitter	+4.6V	Power on
Q2 emitter	+4.0V	Power off
Q3 collector	0V	Power off
Q3 collector	+4V	rises from 0V in approximately 2 secs when instrument switched on
Q1 collector	+4V	Power off
Q1 collector	0V	falls from +4V approximately 1 sec after switch on

Serial interface

U22 pin 22	±4V data	Instrument plotting No load connected
U22 pin 7	+5V data	Instrument plotting No load connected

8

9.0 DEFINITION OF MNEMONICS

Label	*Description*
A0	Memory Address Bus Line 0
A1	Memory Address Bus Line 1
A2	Memory Address Bus Line 2
A3	Memory Address Bus Line 3
A4	Memory Address Bus Line 4
A5	Memory Address Bus Line 5
A6	Memory Address Bus Line 6
A7	Memory Address Bus Line 7
A8	Memory Address Bus Line 8
A9	Memory Address Bus Line 9
A10	Memory Address Bus Line 10
A11	Memory Address Bus Line 11
A12	Memory Address Bus Line 12
A13	Memory Address Bus Line 13
A14	Memory Address Bus Line 14
ADC	Analogue to Digital Converter
ADCCLK	ADC Clock
ADCOE	ADC Output Enable
AN0	Analogue control line 0 (Trigger Level)
AN1	Analogue control line 1 (Trigger Position)
AN2	Analogue control line 2 (CH2 vertical position)
AN3	Analogue control line 3 (Cursor)
AN4	Analogue control line 4 (CH1 Vertical position)
AN5	Analogue control line 5 (Horizontal Datum)
AN6	Analogue control line 6 (Vertical Datum)
CCD	Charge Coupled Device
CA	Continuous Acquisition
CCDMUX	CCD multiplex clock
CCDNRE	CCD read enable - active low
CCD PHA	CCD correction data clock Phase A
CCD PHB	CCD correction data clock Phase B
CCD 1MHz	CCD 1MHZ clock
CH1	Channel 1
CH2	Channel 2
CPU	Central processor unit
COFFSET	Correction offset
CRT	Cathode Ray Tube
CTS	RS423 Clear to Send
DAC	Digital to Analogue Converter
DIL	Dual in line
ECL	Emitter coupled logic
ETS	Equivalent time sampling
EXT	External
FA	CCD 4 phase clock A
FB	CCD 4 phase clock B
FC	CCD 4 phase clock C
FD	CCD 4 phase clock D
FACOMP	Acquisition complete
FARM	Acquisition Armed
FPTS	Fast Post Trigger Counter Strobe
FTB1	Fast timebase control line 1
FTB2	Fast timebase control line 2
FTB3	Fast timebase control line 3
FTRIG	Forced Trigger
HF	High frequency
HORZ	Horizontal
K0	Front panel switches data column 0
K1	Front panel switches data column 1
K2	Front panel switches data column 2
K3	Front panel switches data column 3
K4	Front panel switches data column 4
K5	Front panel switches data column 5
K6	Front panel switches data column 6
K7	Front panel switches data column 7
KR0	Front panel switches data row 0
KR1	Front panel switches data row 1
KR2	Front panel switches data row 2
KR3	Front panel switches data row 3
KR4	Front panel switches data row 4
KR5	Front panel switches data row 5
KR6	Front panel switches data row 6
LED	Light emitting diode
LIN	Linearity
LOPT	Line output transformer
LSYNC	Line Sync Pulse
MCLK	Gate Array Master Clock
MD0	Memory Data Bus Line 0
MD1	Memory Data Bus Line 1
MD2	Memory Data Bus Line 2
MD3	Memory Data Bus Line 3
MD4	Memory Data Bus Line 4
MD5	Memory Data Bus Line 5
MD6	Memory Data Bus Line 6
MD7	Memory Data Bus Line 7
MISO	Master In Serial Out (MPU)
MOSI	Master Out Serial In (MPU)
MPU	Microprocessor
MUX	Multiplexer
NALPHA	Negative logic video drive (Alpha)
NCURSOR	Negative logic video drive (Cursor and Datums)
NSCALE	Negative logic video drive (Graticule)
NFSYNC	Negative logic Frame sync pulse
NTRACE1	Negative logic video drive (Channel 1)
NTRACE2	Negative logic video drive (Channel 2)
NTRACE3	Negative logic video drive (Reference Trace)
NXY	Negative logic video drive (X-Y)
PCB	Printed circuit board
PHA	CCD clock Phase A
PTCARRY	Post trigger counter carry -active low
PTCLK	Post trigger clock
PT0	Post trigger count line 0
PT1	Post trigger count line 1
PT2	Post trigger count line 2
PWROK	Power supply OK control line
RAM	Random access memory
REF	Reference
ROM	Read only memory
RTS	RS423 Request to send data
RXD	RS423 Receive data
SCK	Serial Clock (3 Wire Bus)
SIL	Single in line
SLOW	Slow Timebase Mode
SP SYNC	Supply Sync (Line)
SP0 NDE	Serial Port 0 Data Enable - active low
SP1 NDE	Serial Port 1 Data Enable - active low
SP2 NDE	Serial Port 2 Data Enable - active low

SP3 NDE	Serial Port 3 Data Enable - active low
TBCLK	Timebase Clock
TRIG	Trigger
TRIG'D	Triggered
TRIG NEN	Trigger Enable - active low
TXD	RS423 Transmit Data
UA0	Microprocessor Address Bus Line 0
UA1	Microprocessor Address Bus Line 1
UA2	Microprocessor Address Bus Line 2
UA3	Microprocessor Address Bus Line 3
UA4	Microprocessor Address Bus Line 4
UA5	Microprocessor Address Bus Line 5
UA6	Microprocessor Address Bus Line 6
UA7	Microprocessor Address Bus Line 7
UA8	Microprocessor Address Bus Line 8
UA9	Microprocessor Address Bus Line 9
UA10	Microprocessor Address Bus Line 10
UA11	Microprocessor Address Bus Line 11
UA12	Microprocessor Address Bus Line 12
UA13	Microprocessor Address Bus Line 13
UA14	Microprocessor Address Bus Line 14
UD0	Microprocessor Data Bus Line 0
UD1	Microprocessor Data Bus Line 1
UD2	Microprocessor Data Bus Line 2
UD3	Microprocessor Data Bus Line 3
UD4	Microprocessor Data Bus Line 4
UD5	Microprocessor Data Bus Line 5
UD6	Microprocessor Data Bus Line 6
UD7	Microprocessor Data Bus Line 7
VERT	Vertical
VGEN	Voltage generator
VGEN0	VGEN Address line 0
VGEN1	VGEN Address Line 1
VGEN2	VGEN Address Line 2
VGENRS	Voltage generator ramp reset
VGENSP	Voltage generator select output enable
VREF	Reference Voltage
VRH	Analogue control voltage high from MPU
VRL	Analogue control voltage low from MPU
YBUS0	Y DAC/ADC Data Bus Line 0
YBUS1	Y DAC/ADC Data Bus Line 1
YBUS2	Y DAC/ADC Data Bus Line 2
YBUS3	Y DAC/ADC Data Bus Line 3
YBUS4	Y DAC/ADC Data Bus Line 4
YBUS5	Y DAC/ADC Data Bus Line 5
YBUS6	Y DAC/ADC Data Bus Line 6
YBUS7	Y DAC/ADC Data Bus Line 7

10.0 SERVICE FACILITIES

Service Facilities

Gould and its distributors and agents maintain comprehensive after sales facilities and, whether or not it is still under guarantee, the instrument should be returned to the local Gould service center or distributor through whom it was supplied for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the product was supplied and shipped, with transportation charges prepaid. We accept no responsibility for instruments arriving damaged.

Our Sales and Service Departments and those of approved distributors and agents are ready to assist you at all times.

The Gould Service Department and those of approved distributors and agents can provide maintenance and repair information by telephone or letter, if required.

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